LDO with low quiescent current OTA and capacitance scaling circuit

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Certificate

This is to certify that the thesis titled "**LDO with low quiescent current OTA and capacitance scaling circuit**" being submitted by Aman Bhardwaj to the Indraprastha Institute of Information Technology (IIIT) Delhi, for the award of the Master of Technology, Electronics and Communication Engineering (with specialization in VLSI and Embedded Systems), is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

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Abstract

The efficiency, dependability, and lifespan of any electronic system, particularly battery-powered and portable gadgets, are dependent on a specialized power management unit that offers a clean and controlled power supply. The need for a regulated power supply integrated on a single chip is increasing in various applications ranging from portable devices to biomedical-equipments, which linear regulators accomplish. One such linear regulator is the "Low Dropout Regulator" (LDO), which is utilized to achieve this control even when the power supply or load requirement fluctuates. LDOs are precise and have a quick transient response, making them ideal for controlling on-chip modules.

A specific sort of error amplifier is constructed in this study employing an operational transconductance amplifier (OTA) followed by a buffer that switches on and off for specified load situations. The OTA design aims for a low quiescent current with a high gain, which is then utilized to create two proposed LDO circuits for low load and line regulations. A capacitance scaling circuit is designed for the latter suggested architecture of capacitorless LDO to replicate a nano-farad range capacitance from a picofarad-range on-chip capacitor. A 1.2 V bandgap reference with a start-up circuit is also designed for the reference voltage block.

We present two LDO circuits in this work. The first is a capacitor-based LDO that uses a 1 μF off-chip capacitor to drive a maximum load current of 300 mA throughout a temperature range of -40^{o} C to 125^{o} C while maintaining a low quiescent current of 590nA – 201.4μA for no-load and max-load circumstances. With a maximum current efficiency of 99.93%, this design achieves load regulation of 0.0158mV/mA and line regulation of 9.47mV/mV. The other proposed design is a capacitorless LDO that uses a capacitance scaling circuit to incorporate a 100pF on-chip capacitor to drive a maximum load of 100mA from -40^{o} C to a temperature range 125^{o} C. The quiescent current varies between 433.9 and 616.6 μA. With a maximum current efficiency of 99.843 percent, this design achieves load regulation of 0.0181mV/mA and line regulation of 46.16mV/mV.

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Chapter 1
Introduction

Power management is crucial in the modern era of VLSI design, where power consumption is a critical cornerstone of integrated circuits. Portability is the most significant aspect of gadgets, including laptops, smartphones, smartwatches, and bio-medical devices, such as insulin pumps and pacemakers, attained by the battery used to operate the machine. Low power design should ensure longer battery life. This design should minimize the device's power consumption, or the power delivery to the different components of these macro devices should be done with more efficiency and reliability. However, the battery discharges over time, resulting in the battery's inability to supply constant power. Also, the consistent scaling of technology brings down the transistor's channel length. Thus, clean and regulated voltages are required since the circuitry has gotten very sensitive to the supply variations. Low Dropout Voltage regulator is one of the preferred voltage regulators, which has become a preferred choice for power management of ICs. They can provide regulated output voltage with the varying input voltage, temperature, and load. Even if the battery is drained to a certain level, voltage regulators can provide a controlled supply. Most integrated circuits (ICs) and other modules include the power management unit. The continuous evolution of IC design methodologies has increased the number of IC designs which provides for several voltage domains on a single chip.

Switching regulators are used to convert supply voltage from one domain to another. Especially Buck-Boost converters, which both up-converts and down-converts the voltage, depending on the requirement of the specific module. However, the bucked or boosted voltage has ripples due to the RLC network, introducing oscillations. These oscillations are not suitable for analog circuitry since they are highly susceptible to noise. Noise or ringing in the supply voltage is frowned upon and should be rectified before feeding it to the various domains of the IC. Regulation of this noise-filled signal is crucial for the module's functioning and the increased life expectancy of the device. A Low Drop-out Voltage Regulator, a Linear regulator, is an example. LDOs serve as a bridge between the switching regulators and the subdomain. LDOs offer several advantages over switching regulators, such as avoiding switching noise, compact structure, and simple design (generally comprise a stable voltage reference, error amplifier, pass element, and capacitor). All linear regulators, including LDOs, achieve regulation by dropping

voltage across the pass element. The capacitor is necessary for providing stability to the LDO. For heavier loads, a larger capacitor is required, and they are generally off-chip capacitors, which give better stability, transient response, and PSR. Still, at the same time, they eat up valuable areas and make the system bulky. So, the other such topology that avoids using an off-chip load capacitor is known as "Capacitorless LDO" or "Capless LDO." The lack of an external capacitor provides several cost benefits; nonetheless, a considerable loss in transient performances and power supply noise rejection is frequently observed. Consequently, significant design issues follow the capacitorless LDO voltage regulator, which must be addressed economically and efficiently.

The literature is arranged as follows:

Chapter 2 begins by discussing the background of linear regulators, their categorization, and the specifications that define regulations;

Chapter 3 describes the proposed work, which lays the groundwork for an OTA with a modified dual-mode buffer based LDO for both capacitor-based and capacitorless designs; and

Chapter 4 shows the AC analysis, transient analysis, and parameter confirmations results.

After presenting potential changes for future work in Chapter 5, finally, we close in Chapter 6.

Chapter 2
Linear Regulators

Analog LDO design, as shown, consists of an error amplifier in a negative feedback configuration, which varies the on-resistance of the pass element. Variation of the on-resistance, in turn, changes the amount of current delivered to the load circuit. If the output is different from the Voltage reference, then a feedback resistor divider may be at the feedback path. Because of the negative feedback loop, which comprises an error amplifier, a pass device, and a beta network, output voltage matches reference over slow variations in input voltage or load current.

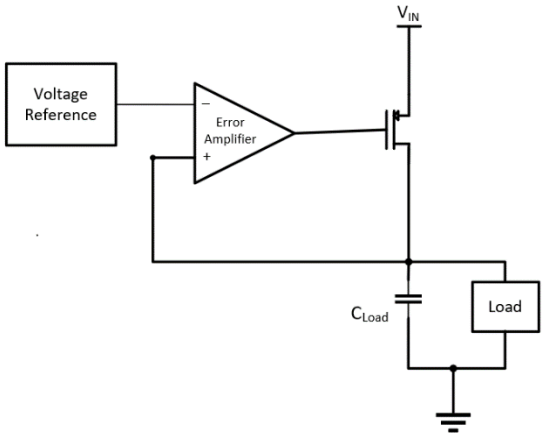

Figure 2.1: PMOS LDO

For high accuracy output voltage at a steady-state, the error amplifier must be a high gain amplifier with sufficient bandwidth to provide a relatively quick feedback loop response. The reaction of the feedback loop for the most extended battery life in battery-operated devices, the current consumption in idle mode

should be kept to a minimum. The output voltage swing should be such that it allows the pass transistor to be fully turned on and fully turned off as and when required. The pass transistor is expected to drive large load currents with lower drop-out voltages across it simultaneously, which suggests a higher aspect ratio for the pass transistor. Only in no-load condition does this transistor carries quiescent current. Choice of the pass element classifies LDO into two categories, (1) N-MOS LDO and (2) P-MOS LDO.

In the NMOS LDO circuit, the feedback is given at the negative input of the error amplifier to maintain the negative feedback configuration since NMOS is in source follower topology. However, this increases the loop's stability by reducing the effect of the gate capacitance of the pass element. Choosing the NMOS element provides significantly lower gate capacitance since the mobility of NMOS is higher than PMOS. Nevertheless, the disadvantage is that the gain will reduce substantially due to the source follower circuit at the second stage, which further calls for a higher gain in the first stage only. Another setback of NMOS LDO is the need for a higher gate voltage of the pass element to obtain a lower drop-out voltage which is met either with the inclusion of a capacitive charge pump or compromising on the slightly higher drop-out voltage.

Another alternative and a more popular choice for pass transistors are PMOS. Since it is connected in common source topology, an inherent phase shift of 180 degrees is provided; hence the feedback is provided at the positive terminal of the error amplifier. Also, the "common source" configuration provides higher gain. Thus, there is no need for very high gain in the first stage.

In contrast to NMOS, where the gate voltage determines the drop-out voltage, a certain amount of drop-out voltage is required for PMOS pass elements. The disadvantage of using PMOS is the inclusion of a low-frequency pole because of the high gate capacitance. Still, with the help of a coupling capacitor or nulling resistor (right hand zero), these effects are repealed. Also, the gate voltage necessary for PMOS is significantly lower than NMOS. Bipolar Junction transistors may also be used as pass elements in the high voltage process, but they require a special Bipolar CMOS DMOS (BCDMOS) process, not discussed in this literature.

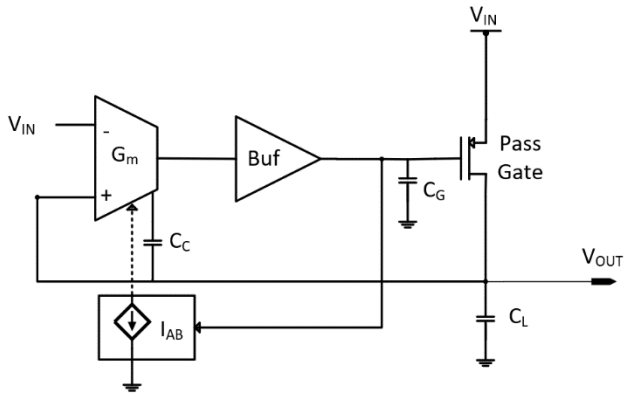

Figure 2.2: OTA based LDO with adaptive biasing

The LDO's error amplifier is used to drive the gate of the pass transistor, which is inherently a capacitive load; an operational transconductance amplifier would be the best choice for the error amplifier because they are voltage-controlled current sources, making them ideal for driving capacitive loads. Unlike operational amplifiers, which are voltage-controlled voltage sources with high input impedance but low output impedance, OTAs have high input and output impedance, making compensation relatively straightforward with a capacitive shunt load. Furthermore, because the error amplifier is the principal power consumer in the LDO architecture, it should be carefully constructed to reduce quiescent current. Low power design necessitates a lower quiescent current, significantly impacting the loop gain. For heavy load conditions, the adaptive biasing block raises the loop gain and the bandwidth of the entire LDO. Higher DC loop gain and bandwidth enhance the regulator's accuracy and transient response. LDOs have difficulty maintaining stability because of the two low-frequency poles, one because of the gate capacitance of power FET and the other due to the capacitive load. The addition of a buffer, as shown in fig., takes care of this issue by splitting one low-frequency pole into two high-frequency poles, which makes them non-dominant.

The voltage reference is an essential component of voltage regulators since it determines the nominal output voltage. The temperature coefficient, which should ideally be zero or extremely close, is the most critical design consideration. There are several methods for determining the voltage reference. A bandgap voltage reference for constant supply across process, voltage, and temperature variations is favored.

This work proposes an OTA-based LDO with dual-mode buffer for both on-chip and off-chip LDO supporting high load current with the fast transient response and low power consumption. A BGR with an in-built start-up circuit is also designed with high tolerance to temperature variation for the reference voltage.

Performance Parameters of Regulators

Drop-out voltage: It is the voltage drop across the pass gate. A low drop-out voltage is preferred since it increases the regulator's efficiency. A minimum amount of drop-out is necessary; however, to keep the pass transistor in saturation; otherwise, it may move to the triode region, which deteriorates the feedback while tampering with the stability of the regulator.

Quiescent Current: The current drawn by the circuit in a no-load, non-switching, yet enabled state is defined as IQ. "No load" indicates that no current flows from the circuit to the output. It is measured as the difference between the current drawn from the input supply and the current provided at load. It is not the no-load input current but rather the "overhead" current necessary to run the primary functioning of the circuitry.

Current Efficiency: It measures the ratio of load current to the total input current.

Load Regulation: It is the ratio of change in output voltage to change in load current. It is characterized as the regulator's ability to sustain the desired output voltage despite changes in load current. It is analogous to the output resistance of the LDO.

Line Regulation: It is the ratio of the change in output voltage to the change in input voltage. It is characterized as the regulator's ability to sustain the desired output voltage despite changes in input voltage.

Line Transient: The line transient response is the fluctuation in output voltage caused by a change in the input voltage. This is also used to determine the circuit's overshoot, undershoot, and settling time.

Load Transient: The line transient response is the fluctuation in output voltage caused by a change in the load current. This is also used to determine the circuit's overshoot, undershoot, and settling time.

Undershoot and Overshoot depend on how fast the load current/input voltage changes during the load/line transients. If the rate of change is less than the bandwidth of the LDO, lower or negligible values of overshoot and undershoot are observed, but if that is not the case, then the shoots can only be reduced by increasing the load capacitor.

Chapter 3
Proposed Design

3.1 Capacitor Based LDO

3.1.1 Design of Error Amplifier

To compare the difference between the reference voltage and the output voltage, LDOs employ an error amplifier in the negative feedback loop. It is already established that a high gain error amplifier with broad bandwidth, high slew rate, and low quiescent current is required for the LDO's high accuracy and transient response. The DC biasing should stay constant under varying load conditions. The typical OTA is popular based on current mirrors due to its broader output voltage swing and single-pole feature.

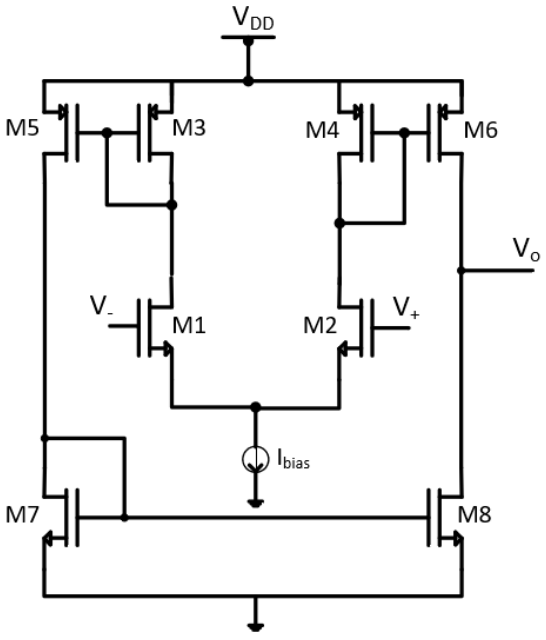

Figure 3.1: Design of Conventional OTA

Transconductance is adjustable in the conventional OTA, as illustrated in figure 3.1, and is dependent on the size of the differential input pair and $M_{6,8}$. Still, the gain is insufficiently high, making it unsuitable for LDO applications. The gain equation shows that the variable bias current does not affect the gain, assuming a constant biasing voltage for MOSFETs to stay in saturation. One possible solution is to lower the overdrive voltage to attain a more significant gain. However, this is not practical since certain transistors carrying higher currents must remain in strong inversion while the remainder must stay in at least moderate inversion. Furthermore, there is a practical limit to the size of transistors. Another method for raising gain is to employ a "cascoded" output stage, although this restricts the amplifier's output swing and hence is not an optimum option. Additionally, the output current is also limited, which reduces the slew rate and thus impacts the transient response. One way to increase the slew rate is to increase the biasing current but that doesn't make it acceptable for low power applications as one of the critical specifications is lower quiescent current. This calls for a High-gain OTA design with a low quiescent current.

High gain OTA, as described above, has a higher gain, lower quiescent current, and a similar frequency response to the conventional OTA. The Rout should be increased to achieve a higher gain, but the cascoded output stage is avoided as the voltage swing gets detreated. Reducing the output stage current is smart as it increases the output resistance and reduces the quiescent current. Still, the reduction in the output stage's current linearly reduces the transconductance, G_m, and the slew rate of the OTA.

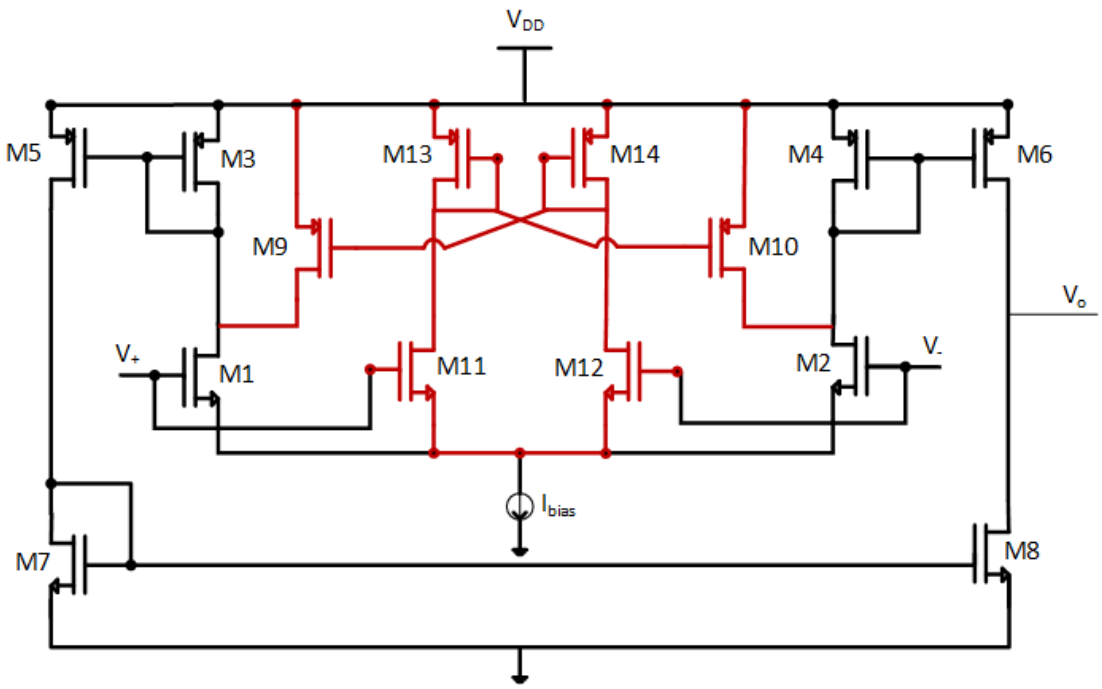

Figure 3.2: Design of High Gain OTA with gain boosting circuitry

This circuitry contributes to lowering the output stage's quiescent current, which boosts the R_{out} and G_m. As seen in figure 3.2, when there is no load, the current flowing from M1 is the summation of the source-to-drain currents of M3 and M9, minimizing the output stage current. M11 and M12 detect the differential input voltage and convert it to branch current, which travels through the current mirror pairs M13-M10 and M14-M9. The reduction in output stage quiescent current makes this a low power OTA with high Rout. M11 and M12 are the second differential input pair, which convert the input voltage to branch current. This current is converted to a voltage by diode-connected M13 and M14. This voltage is fed to M9 and M10 respectively, which act like the G_m boosting network. So, this circuit has two G_m stages. The sum of current from both these G_m stages is converted to a voltage by diode-connected M3 and M4, and finally, this voltage is converted to the current of the second stage. Significant improvements in R_{out} and G_m increase the OTA's total gain. One difficulty may occur due to the diode-connected current mirrors, which create a pole; however, it may easily be turned non-dominant by simply keeping the transistor's resistance very low, which is achieved by raising the W/L.

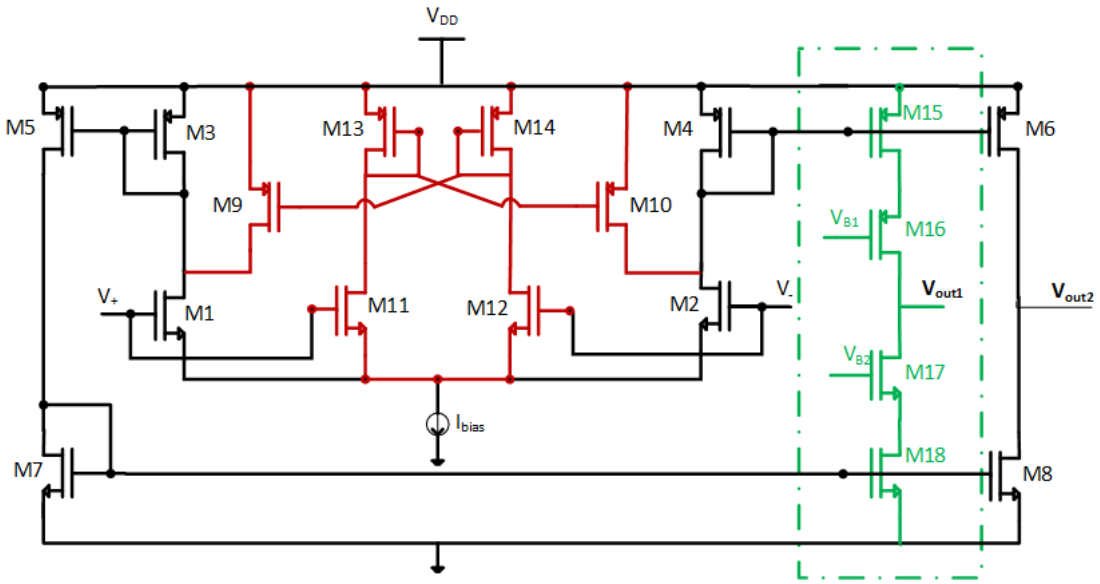

Figure 3.3: High Gain OTA with cascoded class AB second stage

Even though the gain has significantly improved, this OTA is only valid for designing moderate load driving LDO. More gain is needed to drive a much higher load with good transients, and cascoding the second stage is the only option. As shown in figure 3.3, M15, M16, M17, and M18 form a cascoded second stage, which significantly increases the OTA's output impedance, increasing the error amplifier's overall gain. This arrangement of M15-M18 is known as a cascode class-AB amplifier. This high gain OTA has two separate outputs, where the same current is copied from M4 and M7 to both different output branches. The gain is

now suitable for driving higher loads, but the swing is limited. For securing the swing of V_{out1}, the size of the pass transistor could be increased significantly in the LDO implementation. Adding a source follower buffer ensures the stability of the LDO by the pole splitting technique, which splits a low-frequency pole into two high-frequency non-dominant poles.

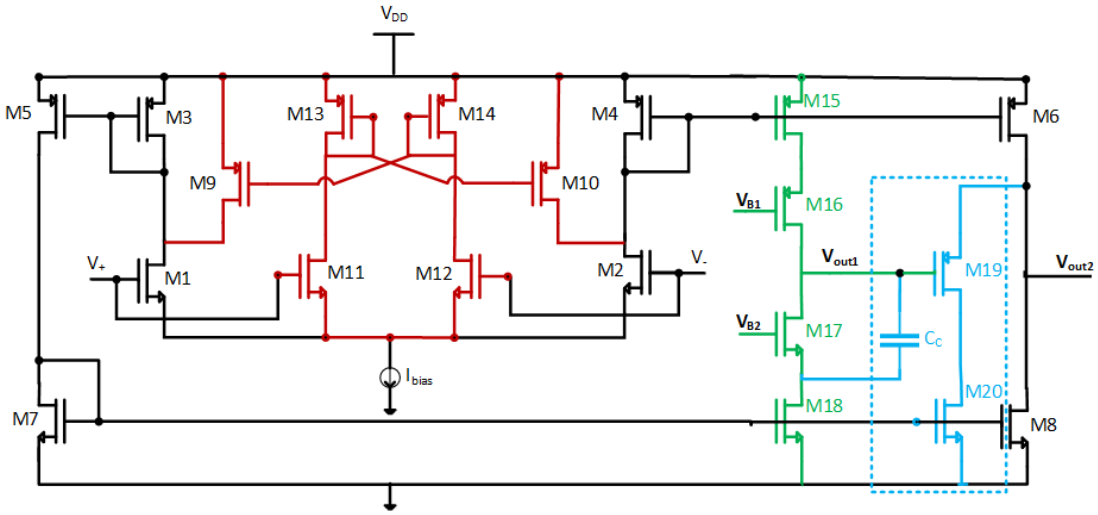

Figure 3.4 Proposed High-Performance OTA with two-mode buffer

For stability of LDO, only one dominant pole should be inside the unity-gain bandwidth, and the rest should be made non-dominant. As shown in figure 3.4, introducing source follower buffer splits the one low-frequency pole into two high-frequency, non-dominant poles. M19 is behaving as the buffer in common-drain topology. Since the OTA is designed such that the LDO can drive high load currents, a huge pass transistor is needed since the swing of V_{out1} should be secured. However, doing so brings the poles at low frequency at Vout1 (gate capacitance of M19) and Vout2 (gate capacitance of pass transistor). For ensuring stability, the phase margin reduces. Using the coupling capacitor, C_C makes these poles relocate to higher frequency again and increases the phase margin. But the transient response will be affected under high load conditions, but the circuit is stable.

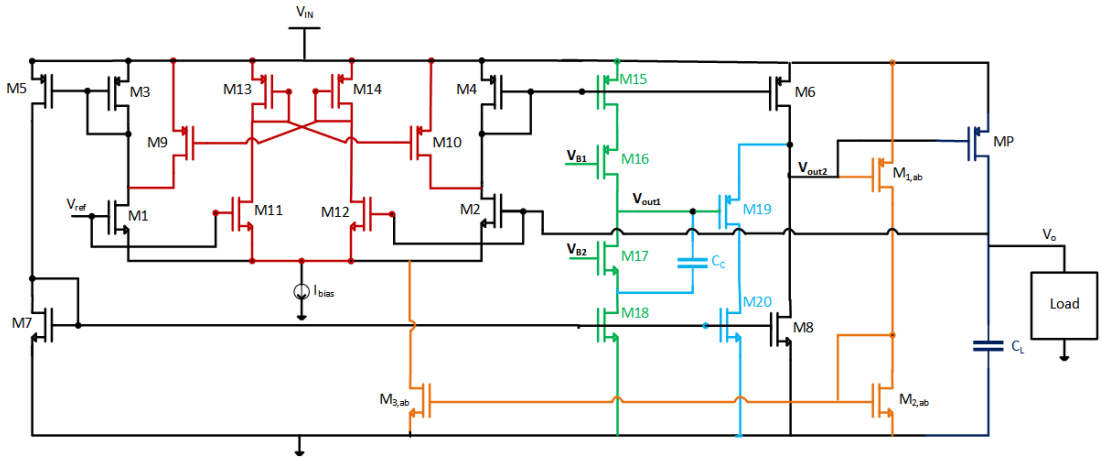

Figure 3.5: Design of Capacitor based LDO employing adaptive biasing

As seen in figure 3.5, a capacitor-based LDO is constructed. Adaptive biasing circuitry is currently used to make the circuit more power-efficient and adaptable, allowing it to work under a wide variety of load fluctuations. The adaptive biasing network comprises $M_{1,\,ab}$, $M_{2,\,ab}$, and $M_{3,\,ab}$ components. $M_{1,\,ab}$ samples the load current flowing from the pass-transistor MP; the copied current is minimal in value due to the small size of $M_{1,\,ab}$ – $M_{3,\,ab}$ in comparison to MP ($M_{1,\,ab}$:MP = 1:5000). The adaptive biasing current modifies the output resistance at Vout1 with variable load current conditions, improving stability and transient response. The duplicated current through $M_{1,\,ab}$ flows through $M_{2,\,ab}$, which mirrors the current to $M_{3,\,ab}$, and this current is given to the input OTA block as a bias. An increase in the bias of the inner OTA block increases the current through the buffer, improving the pass transistor's responsiveness under high load conditions.

Under low load conditions, the pass transistor has a low branch current, which raises the V_o and the input differential voltage due to the negative feedback. Furthermore, the tail current from the adaptive biasing block is in the sub-nano ampere range, resulting in a drop in the gate voltage of the M_{18} due to the substantially lower current through the buffer, which increases the output of the OTA, i.e., V_{out1}. Increased output voltage reduces M_{20}'s drain voltage, and because it is a current copier of M_{18}, the gate voltage drops as well; this causes M_{20} to reach the triode zone and M_{19}, the source follower buffer, to enter the sub-threshold region. As a result, the buffer is turned off for lower load conditions. The second output branch is connected in parallel with the buffer to prevent unnecessary bias current consumption of the buffer under light-load conditions and minimize the quiescent current across the loop via the second output. The V_{out2} is utilized for the OTA output since a lower error amplifier gain is sufficient for lesser loads in LDO. As a result, the second output through M_6 and M_8 powers the pass transistor MP. The lowered gain of the OTA through the second output also guarantees the phase margin to a safe level without compromising transients.

For high loads, M_{19} leaves subthreshold and enters saturation, and M_{20} enters weak inversion region and finally enters saturation; hence the buffer turns on. The

connection of buffer and the second output is in parallel even then the output impedance is not affected since $1/g_{m19} << r_{06} || r_{08}$, so the overall output impedance is due to the source follower M_{19}, and loop is formed from M_{19}'s source.

3.1.2 Pass Transistor

The pass transistor in an LDO is characterized as a g_m unit with load resistance and load capacitance outputs. The pass transistor's gate determines its branch current to source voltage. It is sized according to the maximum load current and the required drop-out voltage, maintaining its state in saturation. PMOS is chosen for its low power consumption and simplicity of design. The pass transistor size is determined using the square law equation for the drain current of a MOSFET. Because the current fluctuation is apparent at the load, a relatively high aspect ratio is expected and preferred. Furthermore, because the suggested error amplifier has a high gain, the concerns caused by the power MOSFET's significant gate capacitance are eliminated.

3.2 Design of Capacitorless LDO

3.2.1Capacitance Scaling Circuit

Capacitor-less LDOs have broad applications in system-on-chip deployed in high-performance devices. The reduced size is a significant factor in VLSI designs. However, to drive high load currents, proportionally high load capacitance is required. For driving hundreds of milliamperes of load current, a load capacitor of hundreds of nano-farads is needed. This capacitor can't be fabricated in IC; hence an off-chip capacitor-based LDO is used. However, an impedance scaling circuit is used to emulate a capacitor of lower magnitude as a capacitor of higher magnitude. It can enable us to formulate a capacitorless LDO with almost similar characteristics as a capacitor-based LDO.

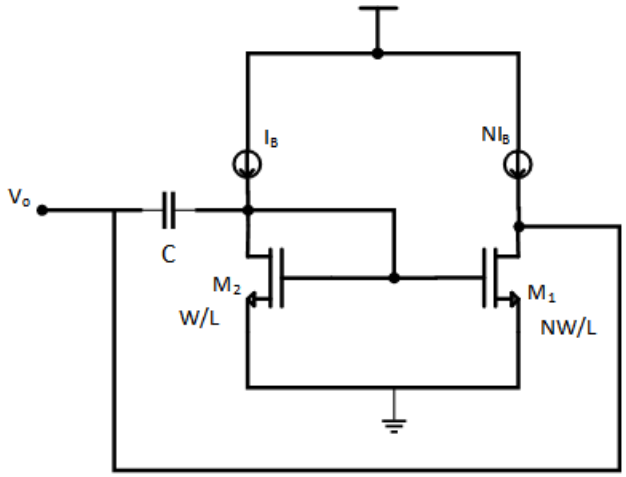

Figure 3.6: Capacitance Scaling Circuit

The impedance scaling network, seen in figure 3.6, employs a current mirror with a 1:N gain and a floating capacitor. Since M_1 and M_2 create a current mirror, the current in both branches will be proportionate. Because the small-signal current via capacitor C is estimated as sVoC, the overall drain-to-source current of M_2 will be $(I_B + sVoC)$, resulting in an N(IB + sVoC) current through M_1. As a result, the total current pulled from Vo equals (N+1)sVoC. This corresponds to the current pulled from an (N+1)C equivalent capacitor placed between Vo and ground.

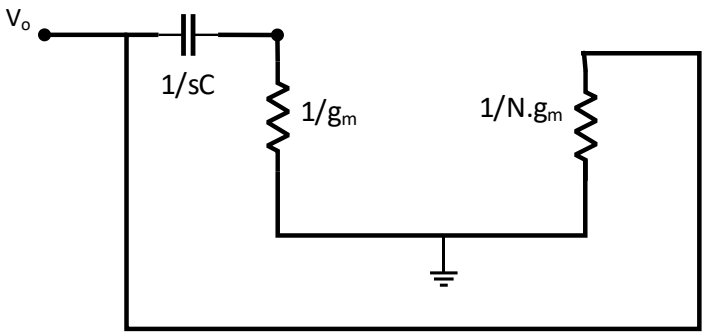

Figure 3.7: Small Signal Model Capacitance Scaling Circuit

The small-signal circuit of the scaling network is shown above in figure 3.7. The input admittance can be evaluated as

$$Y(s) = \frac{N.g_{m2} + (N+1)sC}{1+\frac{sC}{g_{m2}}} \tag{2.1}$$

This can be further approximated as

$$Y(s) \simeq \frac{(N+1)sC}{1+\frac{sC}{g_{m2}}} \tag{2.2}$$

So the following can be inferred

$$\text{Bandwidth} = \frac{g_{m2}}{C} \tag{2.3}$$

And

$$SF = 1+\frac{g_{m1}}{g_{m2}} \tag{2.4}$$

This implies that the maximum frequency at which the circuit behaves as the circuit is limited by the g_m of M2, and the scaling factor (SF) depends on the size of M1. Hence the capacitorless LDO needs to be designed carefully to avoid irregularities in the frequency domain results. The load capacitor is now replaced with the scaling circuit, as shown in figure 3.8, and C_C needs to be adjusted to obtain a good Phase margin which ensures the stability and the transient results of the LDO.

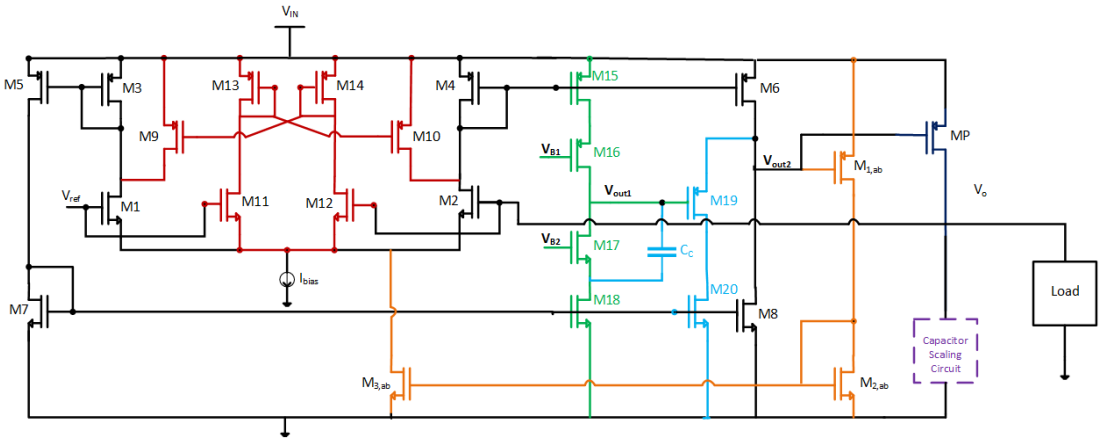

Figure 3.8: Proposed Capacitorless LDO

3.3 Voltage Reference

For obtaining a clean and ripple-free signal from an LDO, a precise reference voltage is given to the LDO, which it takes as a benchmark level for matching the output signal. The voltage reference is connected to the non-inverting input of the error amplifier. Bandgap reference voltage circuit is designed to be insensitive to process, voltage, and temperature variations. For this work, a Bandgap reference voltage circuit for a 1.2V output voltage value is designed.

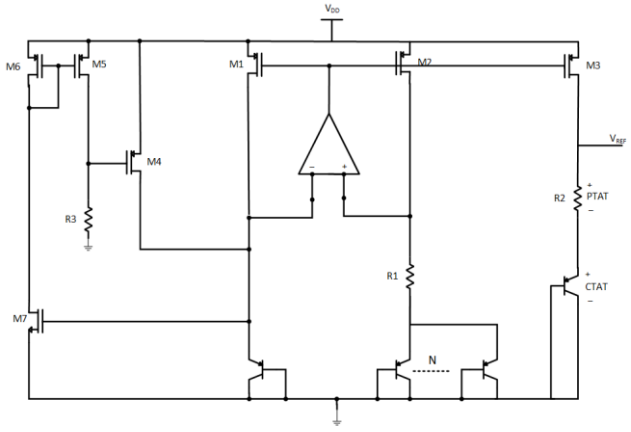

Figure 3.9: Op-Amp based BGR with start-up circuit

A Bandgap reference circuit with a start-up circuit is designed, as shown in figure 3.9. This uses a two-stage operational amplifier controlling the gates of two PMOS to keep the current in CTAT and PTAT branches the same. The op-amp is held in negative feedback, so both the voltages at the input of the opamp are kept the same

via virtual short. The single diode-connected PNP branch is the CTAT and the branch with N diode-connected PNPs is the PTAT. The same current is copied to M3, which has the R2 (PTAT) and diode-connected PNP (CTAT).

$$V_{REF} = V_{CTAT} + V_{PTAT} \tag{2.5}$$

Current through the branch is

$$I_o = \frac{V_T \ln (N)}{R1} \tag{2.3}$$

where

$$V_T = \frac{KT}{q} \tag{2.6}$$

Current mirror M3 is copying the same current to the output branch, so the voltage across R2 is

$$V_{PTAT} = V_{R2} = R2.\frac{V_T \ln (N)}{R1} \tag{2.7}$$

So by varying R1 and R2, V_{PTAT} can be modified.

And the Voltage across CTAT is

$$V_{CTAT} = V_T \ln(\frac{I_o}{I_S}) \tag{2.8}$$

Where I_o is branch current and I_S is the reverse saturation of the diode-connected PNPs, and the complementary effect to absolute temperature is because of the reverse saturation current with is a strong function of temperature.

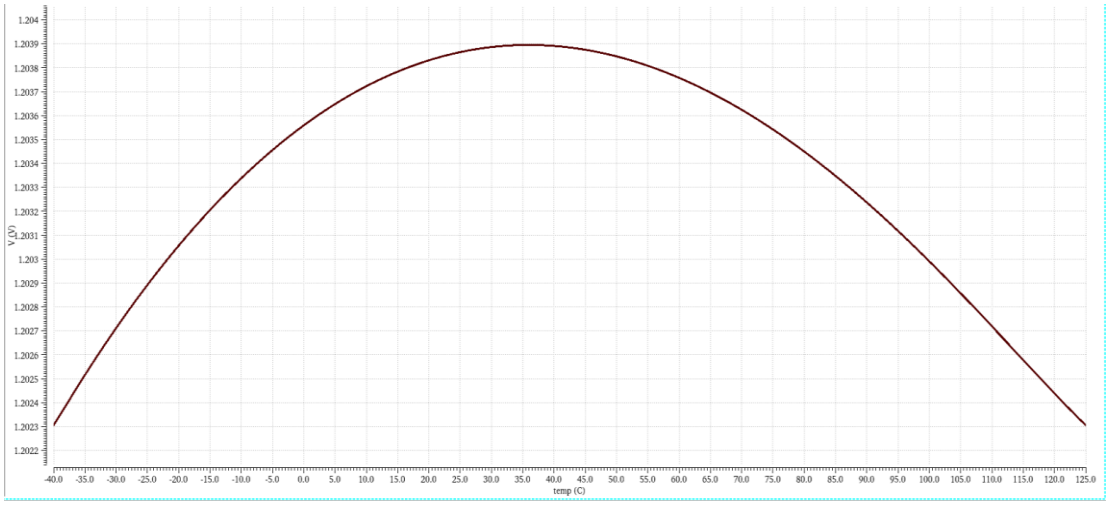

Figure 3.10: Reference Voltage variation with temperature for TT

Since BGR is a self-bias circuit, i.e., no external bias is applied, a start-up circuit is required. BGR has two stable operating regions (1) Normal Operating region and (2) Zero current region. The former is what is desired, but the latter is a concern. The PTAT and CTAT branches carry no current in the zero current region, and the BGR is off. In this state, the gates of PMOSs M1, M2, and M3 reach at VDD, making them off, leading to no current flow in the branches. This is also a stable state for the BGR since the input ports of the opamp are still at equal potential (zero voltage). A start-up circuit for avoiding zero current conditions is needed, which explicitly pulls a current on the branch and disturbs the stability of the BGR. Once that is concerned, the BGR now moves to the other stable operating region, namely, the normal operating region. M4, M5, M6, M7, and R3 comprise the start-up circuit. In a zero current state, the drain of M4 is zero, and the gate of M7 is zero. Since M7 is off, no current passes through M5 and M6, which means the voltage across R3 is zero, so the gate of M4 is zero. VDD is developed across the source and gate of M4. M4 turns on and starts conducting. Its drain voltage increases; the potential at the negative terminal of the opamp is no longer zero, and the opamp starts working, moving the BGR to the normal operating region. During the normal operating region, the gate potential of M7 is high. Hence, the current flows in the branches, and voltage develops across R3; thus, M4 turns off, moving the start-up circuit to an off state, and BGR is in the normal operating region.

3.4 Stability

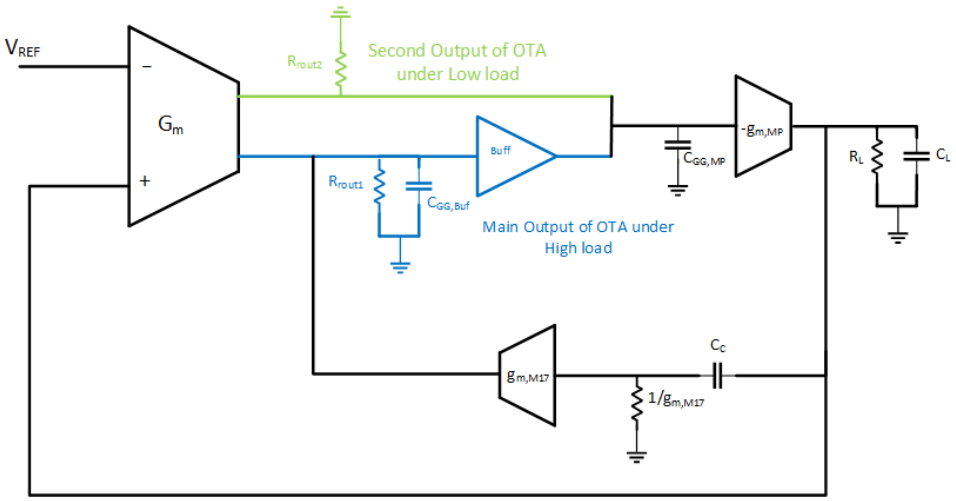

Figure 3.11: Small-signal model of LDO

The small-signal model of the circuit is shown and is considered for the stability analysis. As mentioned before, this LDO operates in two load condition modes. So, it can be simply put that the OTA has two outputs connected to the pass transistor. The main output's resistance is R_{out1} and the second output's resistance is R_{out2}. $C_{G,Buf}$ is the gate capacitance of source follower buffer M_{19}, $C_{G,MP}$ is the gate capacitance of the pass transistor MP. Coupling capacitor C_c forms a path between main output and LDO output and introduces a pole for high-load conditions.

The main output is disconnected during light load conditions since the buffer is off since the bias current is shallow. So, the loop is formed via the second output of OTA. Therefore, the dominant pole is due to the output stage. The output impedance of the OTA is relatively low as it is driving the pass transistor directly.

$$TF\ (s)_{|\text{light load}} = \frac{-G_m g_{m,MP} R_L R_{out2}}{(1+sC_L R_L)(1+sC_{G,MP} R_{out2})} \tag{2.9}$$

The second output does not have a cascoded stage so R_{out2}, is low hence the pole $(1/C_{G,MP} R_{out2})$ is a non-dominant pole. Dominant pole is due to the output stage $(1/C_L R_L)$. As the load current increases the bias current through buffer increases and M_{19} enters strong inversion and M_{20} leaves triode to enters weak inversion further turning the buffer on. Now the OTA drives the pass transistor via buffer through the main output. The transfer function changes as new poles are introduced because of the buffer and coupling capacitor branch. The following transfer function is obtained by simply applying KCL. Under heavy load conditions

this two poles system is formed. However, $g_{m,MP}C_c/ C_{GG,Buf}C_L$ is a non-dominant pole but it is not at very high frequency as compared to the dominant pole, thus in the following fig, it is witnessed that for lower currents of 30µA – 300µA the system looks like it has only one pole , but for high load currents of 3mA-300mA the second pole come into the picture however it is made non-dominant with the action of C_C across the main output through phase compensation at high frequency.

$$\text{TF (s)}_{|\text{High load}} = \frac{-G_m g_{m,MP} R_L R_{out1}}{(1+s\frac{C_{GG,Buf}C_L}{g_{m,MP}C_C})(1+s g_{m,MP} C_C R_{out1} R_L)} \qquad (2.10)$$

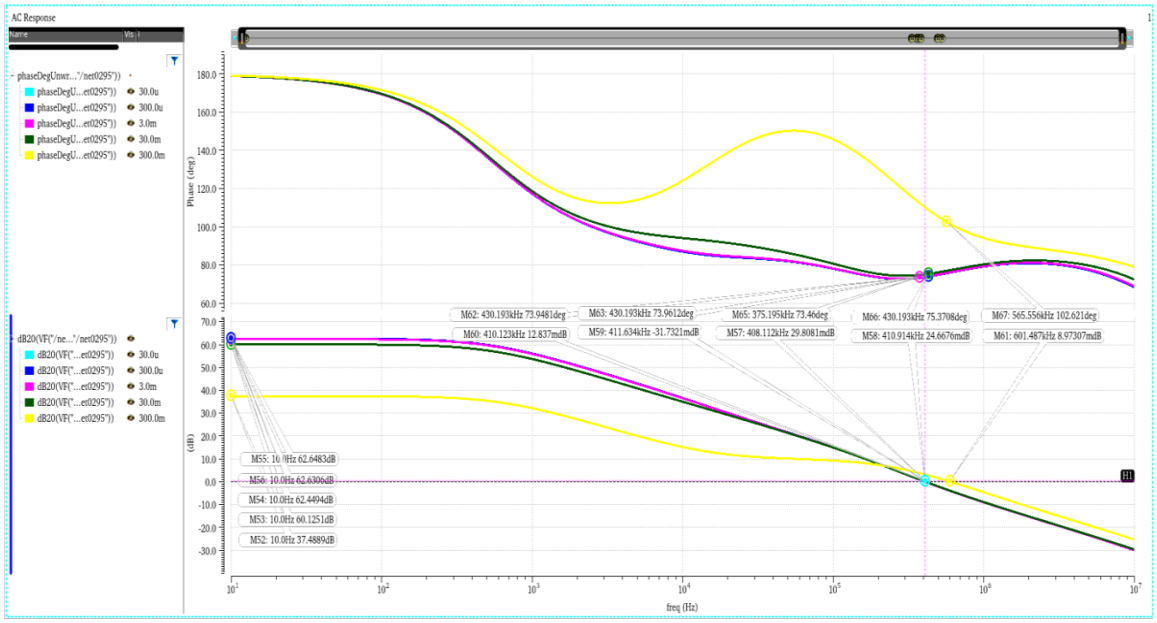

Figure 3.12: Loop-gain and Phase plot of capacitor based LDO with varying loads

Phase and loop gains for varying loads are compiled in table 3.1 for capacitor based LDO

Table 3.1: Loop Gain and phase margin for varying loads for capacitor base LDO at TT process corner and 27^{O}C

Load Current	Loop Gain(dB)	Phase Margin
30µA	62.65	73.95
300µA	62.63	73.96
3mA	62.45	73.46
30mA	60.13	75.37
300mA	37.48	102.62

The variation in phase margin with varying process corners and temperatures were carried out to figure out the stability of the LDO. The chosen process corners were FF, SS, and TT for -40^{O}C, 27^{O}C and 125^{O}C. For the capacitor based LDO the variation of phase margin for the various process corners are shown in figure 3.13, 3.14, and 3.15.

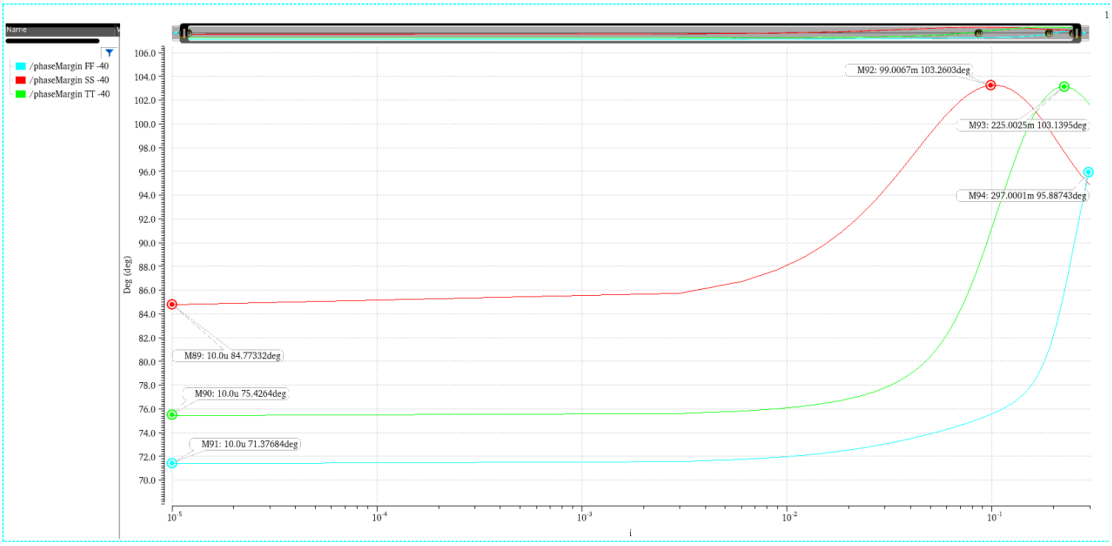

Figure 3.13: Phase margin with varying load current for FF, SS, and TT corners at -40^{O}C (Capacitor based LDO)

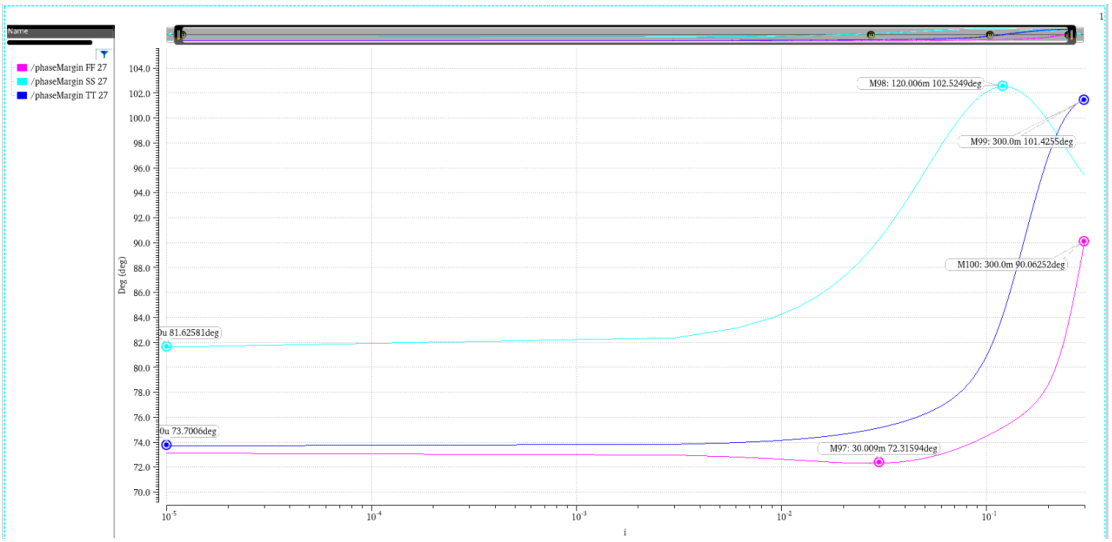

Figure 3.14: Phase margin with varying load current for FF, SS, and TT corners at -27^{0}C (Capacitor based LDO)

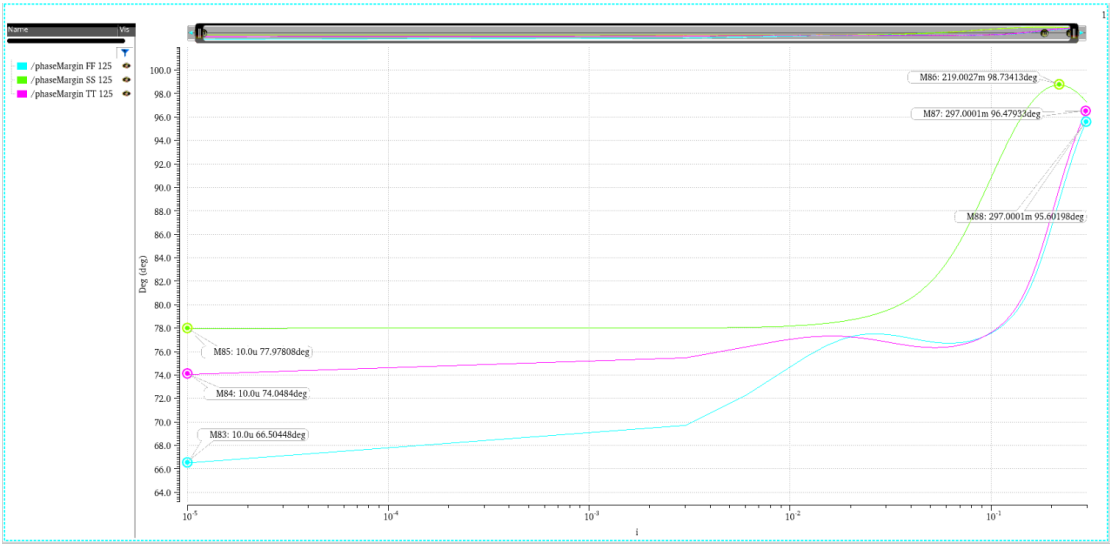

Figure 3.15: Phase margin with varying load current for FF, SS, and TT corners at 125^{0}C (Capacitor based LDO)

The range of phase margin variation is tabulated in table 3.2 over process and temperature variations.

Table 3.2: Range of phase margins for different loads with varying temperature and process corners (Capacitor Based)

Temperature	FF		TT		SS	
	Min	Max	Min	Max	Min	Max
-40^{0}C	71.38^0	95.89^0	75.43^0	103.19^0	84.77^0	103.26^0
27^{0}C	72.32^0	90.06^0	81.63^0	102.52^0	73.70^0	101.43^0
125^{0}C	66.50^0	95.60^0	74.05^0	96.48^0	77.98^0	98.73^0

It can be inferred that for various process corners, the phase margin is greater than 60^0 thus making the circuit stable and noiseless. The lowest phase margin observed is 66.50^0 for FF corner at 125^{0}C and the maximum phase margin observed is 103.19^0 for SS process corner -40^{0}C, it can be inferred that the transient response will be noiseless but it can be slow for higher phase margins.

Similar type of Loop-gain bode plots are obtained for capacitorless LDO design however the highest load current which it can drive is now reduced to 100mA from 300mA but the transfer function is similar as that of a capacitor based LDO since the load capacitance is still high due to the capacitance scaling circuit and the drain to source resistance of the MOSFET in scaling circuit do come in parallel with the load resistance of LDO but it is very high as compared to load so it can be neglected and this is evident from the obtained bode plots, where for lower loads a single pole system is obtained and for heavier loads the second pole so comes into picture but it is compensated.

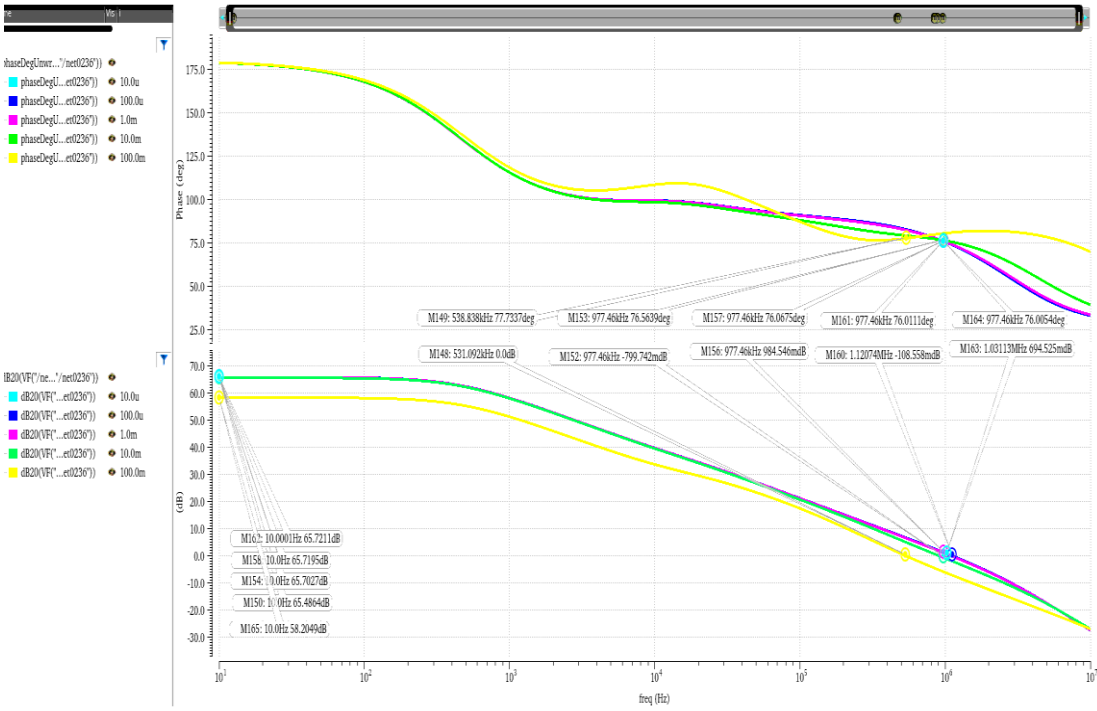

Figure 3.16: Loop-gain and Phase plot of capacitorless LDO with varying loads

Phase and loop gains for varying loads are compiled in table 3.3 for capacitorless LDO.

Table 3.3: Loop Gain and phase margin for varying loads for capacitorless LDO at TT process corner and 27^{o}C

Load Current	Loop Gain(dB)	Phase Margin
10µA	65.72	76.00
100µA	65.72	76.01
1mA	65.70	76.07
10mA	65.49	76.56
100mA	58.20	77.73

The variation in phase margin with varying process corners and temperatures were carried out to figure out the stability of the capacitorless design too.

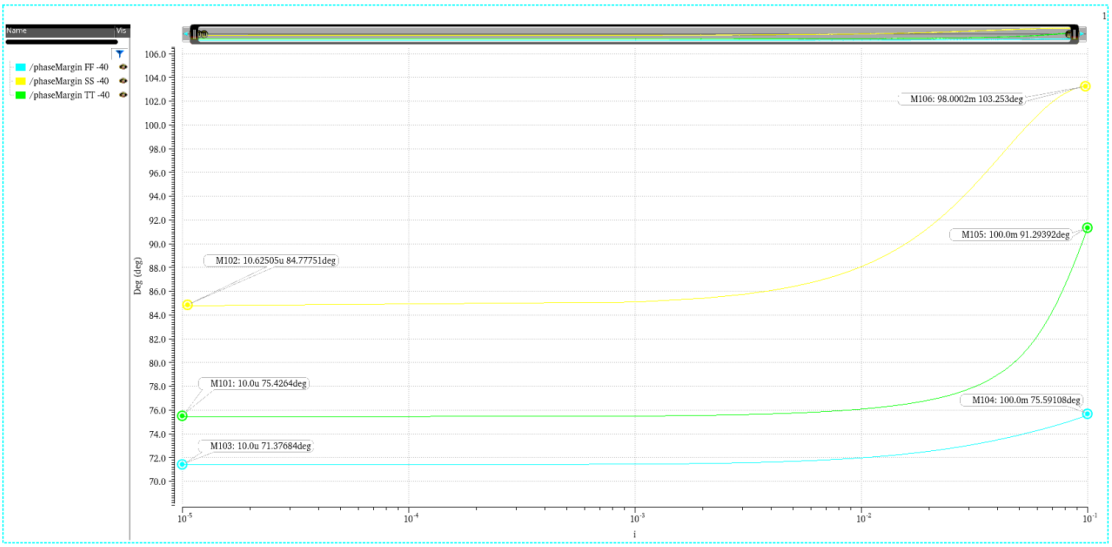

Figure 3.17: Phase margin with varying load current for FF, SS, and TT corners at 125^{0}C (Capacitorless LDO)

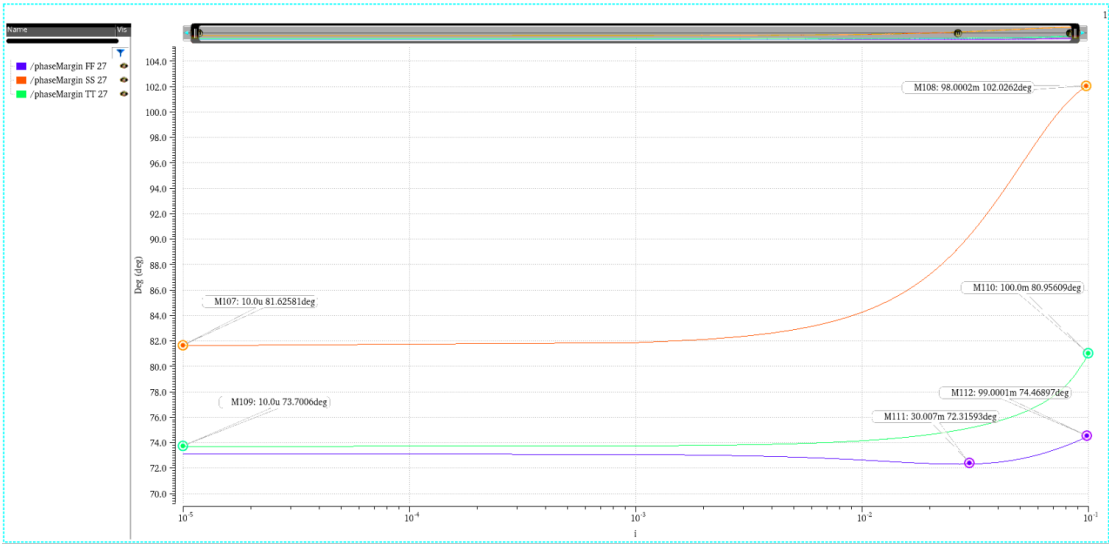

Figure 3.18: Phase margin with varying load current for FF, SS, and TT corners at 125^{0}C (Capacitorless LDO)

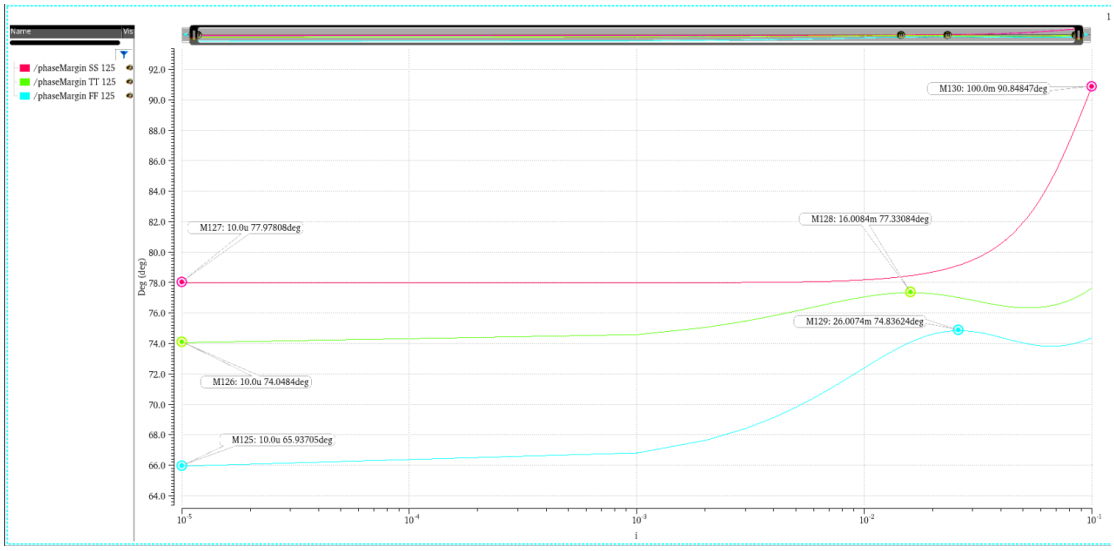

Figure 3.19: Phase margin with varying load current for FF, SS, and TT corners at 125^{0}C (Capacitorless LDO)

The range of phase margin variation is tabulated in table 3.4 over process and temperature variations.

Table 3.4: Range of phase margins for different loads with varying temperature and process corners (Capacitorless)

Temperature	FF		TT		SS	
	Min	Max	Min	Max	Min	Max
-40^{0}C	71.37^0	75.59^0	75.42^0	91.29^0	84.78^0	103.25^0
27^{0}C	72.32^0	74.47^0	73.70^0	80.96^0	81.63^0	102.03^0
125^{0}C	66.94^0	74.84^0	74.05^0	77.33^0	77.98^0	90.85^0

It can be inferred that for various process corners, the phase margin is greater than 60^0 thus making the circuit stable and noiseless. The lowest phase margin observed is 65.94^0 for FF corner at 125^{0}C and the maximum phase margin observed is 103.25^0 for SS process corner -40^{0}C, it can be inferred that the transient response will be noiseless but it can be slow for higher phase margins. The phase margin is greater than 60 degrees for both capacitors based and capacitorless LDO hence noiseless transient responses are expected.

Chapter 4
Simulation Results

4.1 Capacitor Based LDO Results

The output transient response for V_o = 1.2V at V_{IN} = 1.8V for the maximum load current transition from I_L = 0 A (no load) to 300mA (max load) is shown in figure 4.1. It displays a 158.24mV if undershoot which can recover to the regulated voltage with a tolerable error of 3% in 11.5µs.

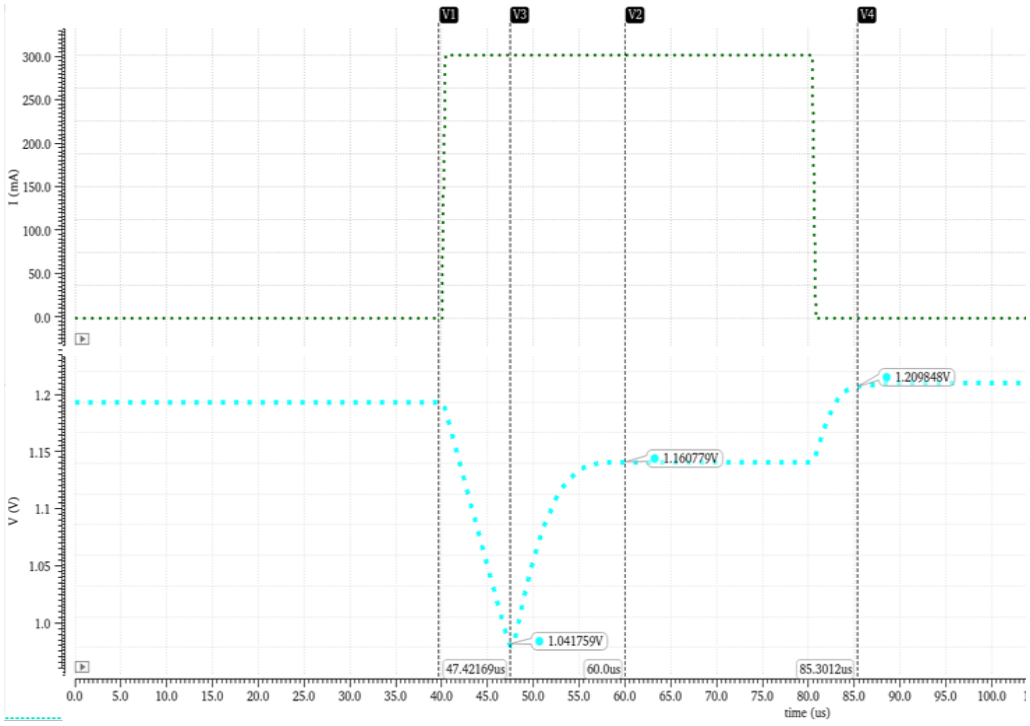

Figure 4.1: Transient response of output voltage with a load of 300mA

Figure 4.2, shows the line transient for the Line regulation curve. The input voltage is varied from 1.6V to 2V. The circuit is operating at a max load condition of 300mA. A

variation of 3.85mV is observed in the output voltage. The obtained line regulation for the capacitor-based LDO is 9.47 mV/V.

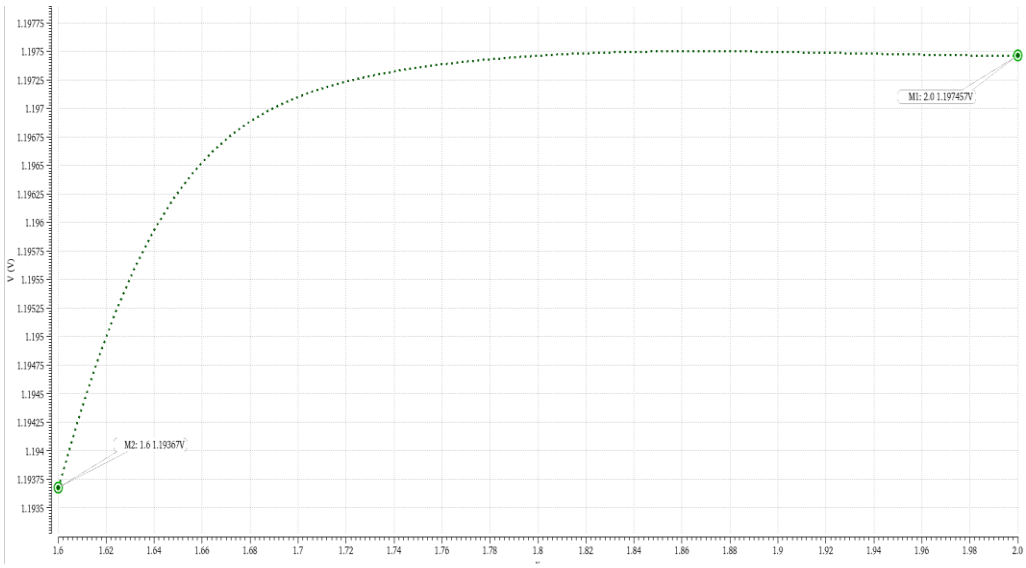

Figure 4.2: Line Regulation for Capacitor Based LDO

Figure 4.3 shows the load regulation curve at V_{in} = 1.8V for V_o = 1.2V. The load current is varied from no-load to max-load condition. Obtained load regulation is 0.0158 mV/mA. It can be observed that at low load conditions for current less than 10mA, the load regulation is weak due to the minimized quiescent current.

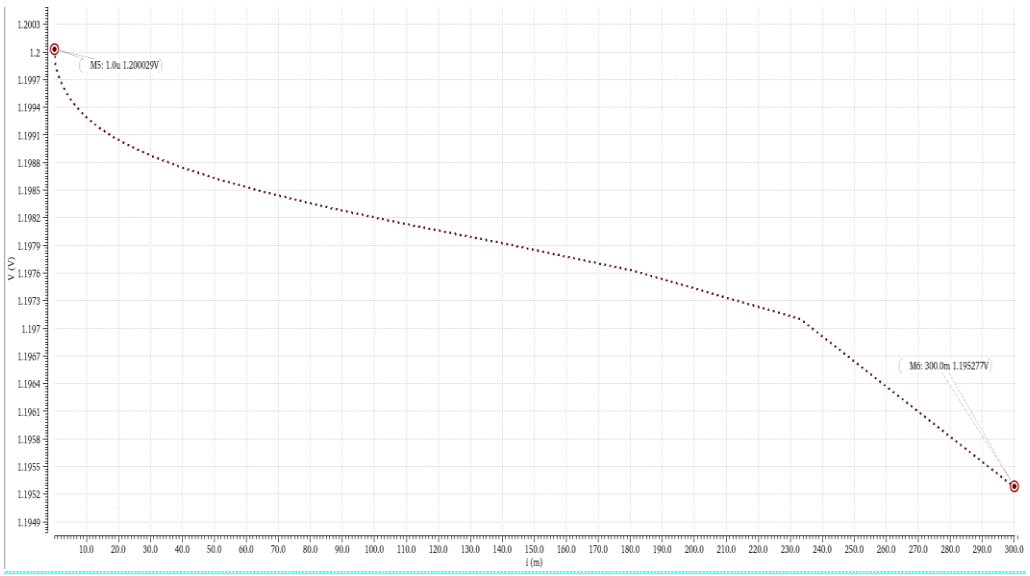

Figure 4.3: Load Regulation for Capacitor based LDO

Since a custom BGR circuit is implemented as the reference voltage, it is important to measure the change in output voltage for temperature variation. The figure below depicts the output voltage fluctuation throughout a temperature range of -40° C to 125° C at the maximum load current of 300mA.

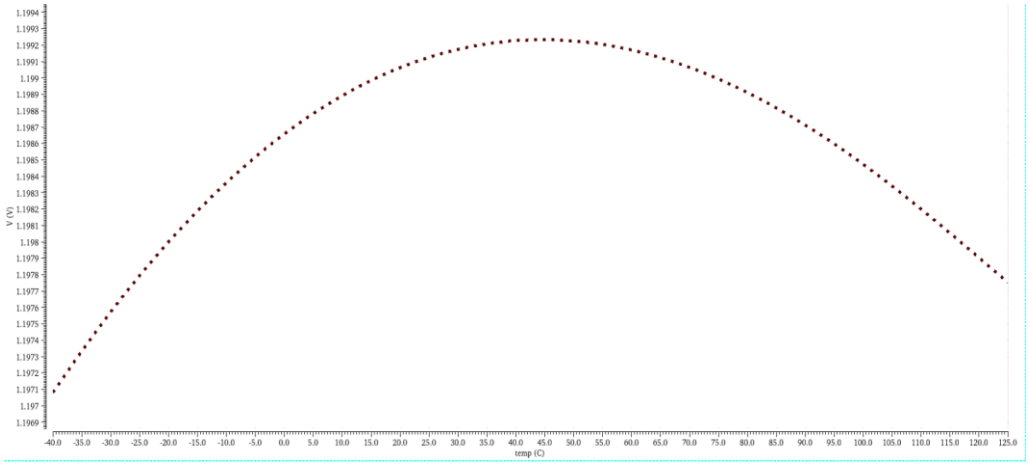

Figure 4.4: Output voltage variation with the temperature at 300 mA load

For the proposed capacitor-based LDO, all the obtained results at varying load currents are tabulated below.

Table 4.1: Performance comparison at varying load currents for capacitor-based LDO

	10 µA	100 µA	1 mA	10 mA	100 mA	300 mA
I_Q (µA)	0.589	0.693	1.604	7.928	94.95	201.4
ΔV_O (mV)	15.35	39.68	47.12	70.25	96.56	158.24

4.2 Capacitorless LDO Results

The capless LDO design is now limited to a load current of 100mA due to the inclusion of a capacitance scaling circuit. Trying to obtain the load capacitance of 1uF from the scaling circuit interferes with the small-signal results. Due to the linear dependency of the scaling factor on the size of MOSFET, the output pole of the LDO gets disrupted. Also, the demand of size of the MOSFET gets way too impractical for high scaling factor (SF).

The output transient response for V_o = 1.2V at V_{IN} = 1.8V for the maximum load current transition from I_L = 0 A (no load) to 100mA (max load) is shown in figure 4.4 It displays a 39.858mV of undershooting which can recover to the regulated voltage with a tolerable error of $\pm$ 0.2% in 2.875µs. For the transition of load current from 100mA to 0mA, an overshoot of 29.7mV is observed which can be recovered to a voltage of tolerable error of $\pm$ 0.2% in 2.792µs.

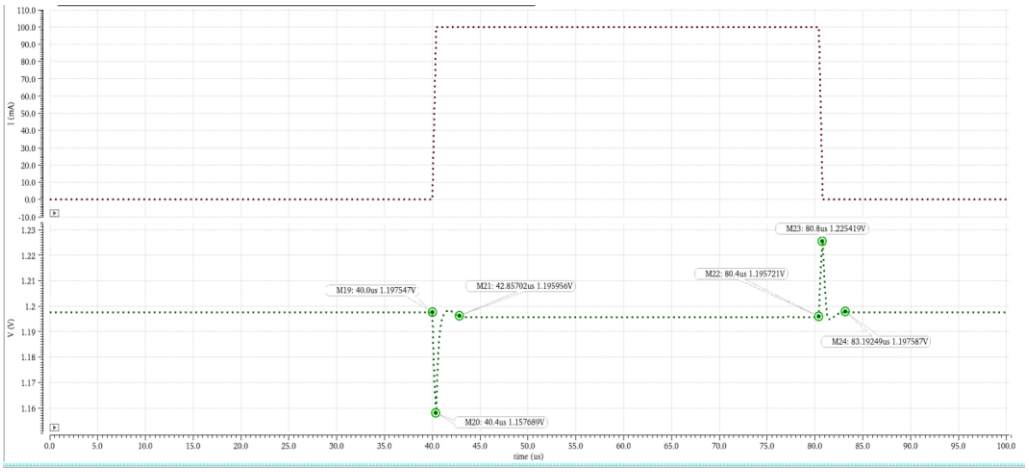

Figure 4.5: Transient response of output voltage with a load of 100mA

Figure 4.4 shows the line transient for the Line regulation curve. The input voltage is varied from 1.6V to 2V. The circuit is operating at max load condition of 100mA. A variation of 18.461mV is observed in the output voltage. The obtained line regulation for the capacitor-based LDO is 46.16 mV/V.

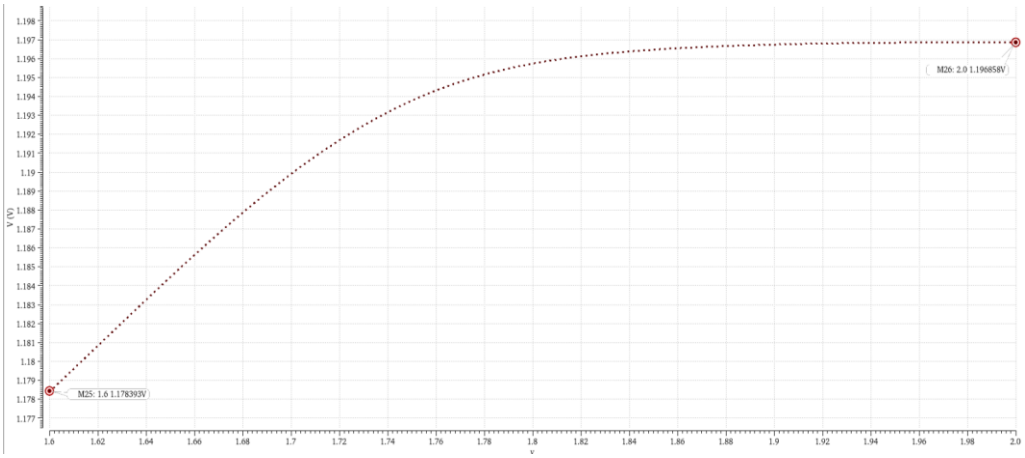

Figure 4.6: Line Regulation for Capacitorless LDO

Figure 4.5 shows the load regulation curve at V_{in} = 1.8V for V_o = 1.2V. The load current is varied from no-load to max-load condition. Obtained load regulation is 0.0181 mV/mA.

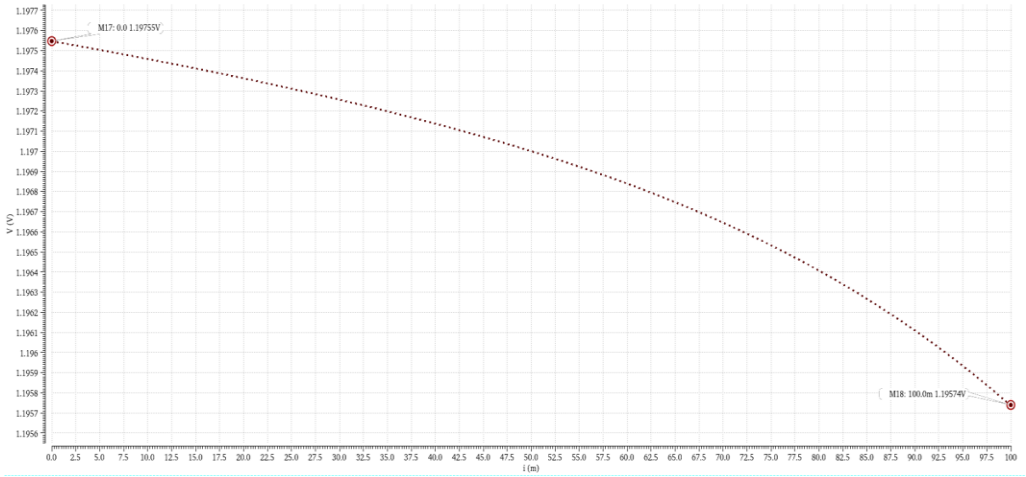

Figure 4.7: Load Regulation for Capacitorless LDO

The following graph shows the voltage change with variation in the temperature from -40^0 C to 125^o C at the maximum load of 100mA.

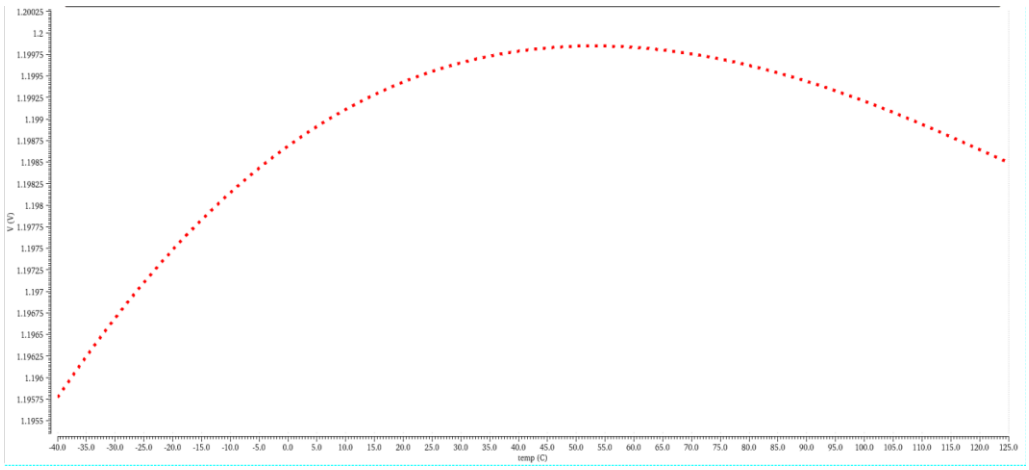

Figure 4.8: Output voltage variation with the temperature at 100 mA load

For the proposed capacitorless LDO, all the obtained results at varying load currents are tabulated below.

Table 4.2: Performance comparison at varying load currents for capacitorless LDO

	10 µA	100 µA	1 mA	10 mA	100 mA
I_Q (µA)	433.979	522.977	523.953	600.883	616.594
ΔV_O (mV)	0.002	0.023	0.23	3.256	39.858
Settling Time (µs)	NA	7.662	4.842	4.447	2.875

*Around 433 µA - 522 µA is consumed by Capacitance scaling circuit only

Chapter 5
Future Work

The capacitance scaling circuit is significantly reliant on the size of the MOSFET used for the scaling factor, as detailed in Chapter 3. Furthermore, the transconductance of the M_2 influences the capacitive bandwidth (Eqn. 2.3). This necessitates that our design drives a relatively lower load current of 100mA. The scaling circuit consumes a relatively high current due to the massive size of the MOSFETs as evident from Eqn. 2.4. As a result, using the present structure to achieve a high scaling factor and a broad capacitive bandwidth is both space and power inefficient. A new adjustment to the scaling network that may be made to reduce MOSFET sizes is mentioned in [8], and this scaling network can be used in our design for wider capacitive bandwidth and a high scaling factor. [8] uses a gain stage between the current mirrors which amplifies the output of M_2 by the gain before reaching the M_1, resulting in the dependence of SF on this gain. This design may also improve the bandwidth for the capacitive behaviour by involving a gain stage in the diode-connected branch which reduced the input impedance of M_2 to $1/A.g_{m2}$.

Future work would include the enhancement of the capacitive scaling circuit for driving more heavier loads with sustained stability and low power consumption. Also, the layout of the design could be implemented and further results can be validated.

Chapter 6
Conclusion

The Low dropout regulators were implemented in GPDK180nm technology. Two designs are proposed one is a capacitor-based LDO with a load capacitance of 1µF with a dropout of 600mV and maximum load current, and the other is a capacitorless LDO with a capacitor scaling circuit amplifying an 100pF to a 90.2nF capacitor with a maximum load current of 100mA. The same error amplifier design is used for both circuits with some modifications in the size of the pass transistor and the value of coupling capacitor for load capacity and small-signal stability, respectively. The designed OTA has two modes of operations for low and high loads, making the circuit significantly low power for smaller load operations by turning the buffer stage off near 3mA load currents.

Capacitor-based LDO requires a load capacitance of 1µF to drive a current load of as high as 300mA while maintaining a shallow quiescent current of 589 nA with 10 µA load and 201 µA while driving 300 mA load. The maximum peak-to-peak voltage observed is 158.24 mV. This design provides a load regulation of 0.0158mV /mA, which is better than all the designs compared. The line regulation of 9.47mV/V makes this circuit relatively ineffective to the supply variations. The maximum current efficiency of 99.933% is better than almost all the other designs compared.

Capacitorless LDO can drive the maximum 100mA load current without affecting the circuit's stability and the transient response. The additional circuitry for scaling increases the quiescent current of this LDO. The current drawn by the capacitive scaling network is almost >80% of the total IQ of the circuit. At a low load of 10 µA, the quiescent current is 433.979 µA, where the error amplifier consumed only around 600 nA. While operating at a maximum load of 100 mA, the total quiescent current obtained is 616.594 µA, out of which the error amplifier consumed 95.56 µA. The maximum peak-to-peak voltage observed is 39.858 mV. This design provides load regulation of 0.0181mV /mA and line regulation of 46.16mV /V, which are not the best but are better than most of the other designs. The maximum current efficiency obtained by this capacitorless design is 99.843%. We finally compare the results of our designs with some other Analog LDOs in Table 7.1.

Table 7.1: Comparison with various analog LDOs

	[1]	[5]	[9]	[10]	[4]	[2]	[8]	Capacitor Based	Capacitorless
Technology (nm)	55	180	180	130	180	180	180	180	180
V_{IN} (V)	0.8	1.4	1.2	0.58-0.9	2	1.4-1.8	1.8	1.8	1.8
V_O (V)	0.6	1.2	1	0.53	1.8	1.2-1.6	1.2	1.2	1.2
I_Q (µA)	0.0016	1.6-200	135.1	4	50-600	0.94-255	265	0.59-201.4	433.979-616.594
I_{Load} (mA)	10	50	100	3	600	300	10	300	100
C_{Load} (µF)	1	1	1	120pF	1	1	NA	1	100pF
ΔV_O (mV)	70	24	25	224	15.6	96	44	158.24	39.858
Max Current Efficiency (%)	99.99	99.6	99.86	99.8	99.88	99.92	97.74	99.933	99.843
Load Regulation(mV/mA)	1.05	0.1	0.075	1.2	0.0083	0.1	4.40	0.0158	0.0181
Line Regulation(mV/V)	0.5	5.5	22.7	29	0.23	5.33	10	9.47	46.16
Settling Time(µs)	NA	1.2	2	<20	3	19.2	50	11.5	2.792

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