A Wordline Voltage Management for NOR Type Flash Memories

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with Specialization in VLSI Design and Embedded System

Student's Declaration

I declare that the dissertation titled "A Wordline Voltage Management System for NOR Type Flash Memories" submitted by Rohan Sinha for the partial fulfillment of the requirements for the degree of Master of Technology in Electronics and Communication Engineering is carried out by me under the guidance and supervision of Dr. M. S. Hashmi at Indraprastha Institute of Information Technology, Delhi and Mr. Vikas Rana at STMicroelectronics, Greater Noida. Due acknowledgements have been given in the report to all material used. This work has not been submitted anywhere else for the reward of any other degree.

..... Place and Date: …….....
Rohan Sinha

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

…….. ……
Dr. Mohammad. S. Hashmi Mr. Vikas Rana

ABSTRACT

Today, in every electronic system, some information must be stored even when the system is not powered. Solid state non-volatile memories are used for storing those information which should not be lost even when the power supply is switched off.

Flash memories are one of the extensively used non-volatile memories used in various portable and handheld devices ranging from wireless sensors to cellular phones. For these devices, high speed operation with low power consumption is an important aspect for efficient operation and long battery life. Here, the speed is largely limited by the time required to access the data from a particular address. Unlike memories like RAMs, flash memories require high voltages for data read, program and erase operations. However, with the evolution of VLSI technology which necessitates scaling down of supply voltages, the high speed switching from low to high voltage becomes difficult. Therefore, a high voltage management system is necessary for providing the requisite high voltages to the memory cells according to the different memory operations and also for interfacing the memory core circuits operating at high voltage level with the peripheral circuits operating at supply voltage level.

In this dissertation, a wordline voltage management system has been developed in 90nm STM10 triple well CMOS technology for fast wordline charging of the memory array which mainly governs the overall access time. The overall design is also complemented with a positive/negative level shifter for high speed interfacing between the memory core circuits and the peripheral circuits. The architecture has been validated for a wide range of high voltage levels and is optimized to perform efficiently across different process corners and temperatures.

ACKNOWLEDGEMENTS

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"Arise, awake, and stop not till the goal is reached" – Swami Vivekananda from Katha Upanishad.

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1 INTRODUCTION

1.1 FLASH MEMORY OVERVIEW

Today, the driving factors in the development of efficient and high density Flash memories are the growing market of embedded systems, MEMS and Memories. Flash memory is a type of non-volatile memory which works on the principle of a floating gate device where charges are stored in the conductive metal layer between the gate and the channel and is surrounded by an insulator. The idea behind this is to store the information in the form of charges and thus in the form of threshold voltage [1].
The dependency of the threshold voltage on the charge stored at the floating gate is given by the equation [1]

$$V_T = K - \frac{Q}{C_{OX}} \qquad (1)$$

where, K is the constant that depends on the gate and substrate material, doping and gate oxide thickness, Q is the charge weighted with respect to its position in the gate oxide, C_{OX} is the gate oxide capacitance and V_T is the threshold voltage of a MOS transistor.

The memory is programmed by Channel Hot electron Injection (CHI) mechanism [1] and erased by Fowler-Nordheim (FN) tunneling mechanism [1]. CHI can be applied selectively to the flash cells so they can be programmed bit by bit individually. The cells are erased in sectors/ blocks where the whole memory is divided into sectors/blocks using triple well technology. Triple well process is used where the memory cells are formed on the p-well surrounded by n-well to isolate the non-selected sectors from the selected sectors during the erase operation.

Erase mechanisms are of two types namely the source side erase and negative gate erase [2], [3]. In the source side erase mechanism, the source terminal is raised to a high voltage, 12v, with the drain floating and control gate grounded. Thus to obtain a high breakdown voltage at the source junction, the n^+ diffused layer is surrounded by a n^- diffused layer [4]. This deeply formed source junction prevents channel length scaling which is required for high density memory cells [4]. For high endurance the erase operation uses the negative gate bias erase scheme [5]. Also, applying negative voltage at the gate with respect to the substrate allows the flow of FN current in more or less uniform manner rather than applying a large positive voltage at the source side of the memory cell [2]. This technique also reduces the switching voltage and minimizes the effect

of band to band tunneling which takes place between the reverse biased source/substrate junction and thus effects the cell reliability [3], [6].

1.1.1 MEMORY CELL STRUCTURE AND ITS OPERATION

Fig.1 shows the structure of a flash memory cell. The memory cell is formed on the p-well surrounded by n-well using triple well technology, to avoid the unwanted flow of current from the p-well to the n-well where 5v is applied to the p-well during the erase operation. The n-well is pulled to the corresponding maximum high voltage during read and program operations and is at supply voltage level or 0V during the erase operation.

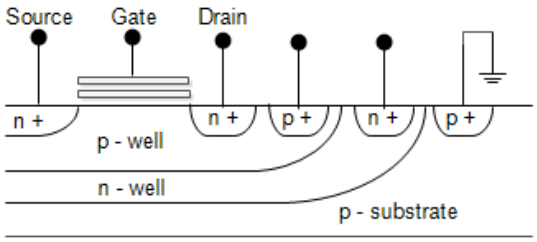

Fig.1. Schematic of flash memory cell

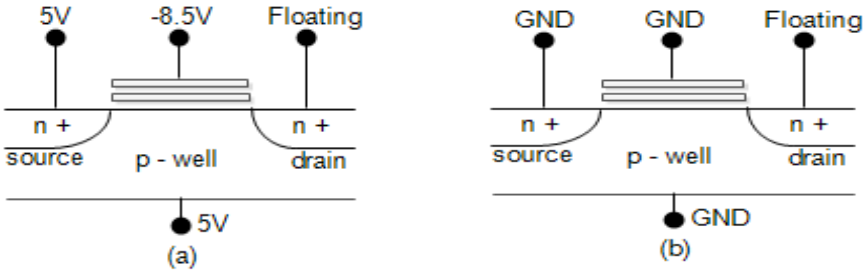

Fig.2. Operating condition of flash memory cell in erase operation (a) selected sector (b) unselected sector

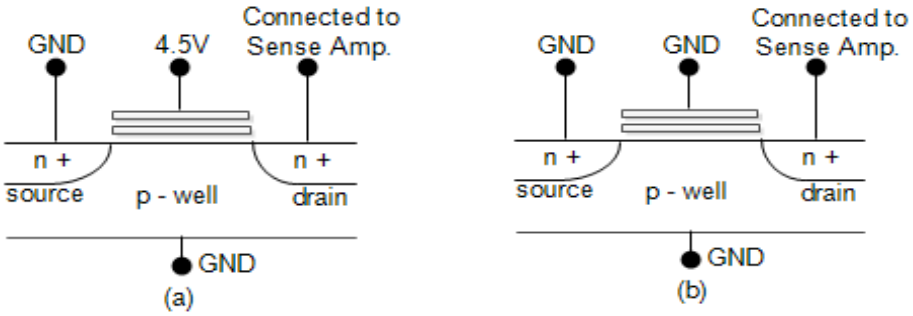

Fig.3. Operating condition of flash memory cell in read operation. (a) Selected memory cell. (b) Unselected memory cell

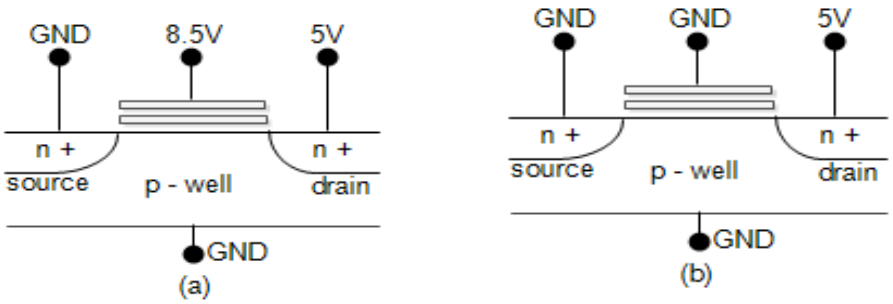

Fig.4. Operating condition of flash memory cell in program operation (a) Selected memory cell (b) Unselected memory cell

Fig.2 shows the operating voltage condition for the NOR type flash memory cell in erase operation for the selected and unselected sectors. Fig.3 and Fig.4 shows the voltage conditions in read and program operations for the selected and non-selected memory cells in a particular sector. In the erase operation, the wordlines of the selected sectors of the cells are kept at -7v while the wordline of the unselected sectors are at 0v. The source junction and the p-wells of the selected and unselected sector are kept at 4v and 0v. Consequently, 11v is applied between the channel and the control gate of the selected cells which induces electron tunneling from the gate to the channel. The drain is kept floating so that there should not be any flow of current between the drain/p-well junction. The p-well of the selected sectors are separated from the unselected sectors using different p-wells buried in n-well. For read and program operation, the source junction and p-well of all the cells are at 0v. The drain terminal which is connected to the bitlines of the memory array is driven at 5v by the program load during the program operation or is connected to the sense amplifier for sensing the current during the read operation [7]. For program operation, the word lines of the selected address are set to 7V whereas, for read, it is set to 4V. The read operation is performed by applying a voltage to the gate of a reference cell whose threshold level is between the threshold of the programmed and the erased cell [7]. The sense amplifier senses the current flowing through the selected memory cell and drives the output to logic “0” or “1” by comparing the current flow of the selected memory cell with that of the reference memory cell. Since, the programming operation is done using CHI, the threshold voltage controllability is higher than the case of FN tunneling [8]. The voltage distribution of the erased bits is controlled by doing soft programming to the bits which are over erased.

1.1.2 SECTOR ORGANIZATION

Memory array organization becomes more and more complex as the demand of high density flash memories is increasing day by day. The size of the sector mostly depends on the type of

application. In practice, it is governed by area, cost and performance tradeoffs. As, the device density becomes higher the sector count increases which complicates the management of decoding circuits necessary for device operation. Sectors in a Flash memory can be arranged in two different ways. In the first case, wordlines are common to all the sectors in the same horizontal strip and the bitlines are local to one sector. In the second case, bitlines are common to all sectors while wordlines are local to each sector. Longer bit-lines affect the sense amplifier speed while longer word-lines increases the time constant due to the increased word line capacitance which affects the access time. Fig.5 shows the memory array organization of 1KB memory. The architecture is the Divided Bit Line NOR (DINOR) architecture where each sector consists of 16 bits in the bit-line direction and 256 bits in the word-line direction which makes a 4 Kb memory. The bit line consists of a sub-bit line (SBL) and a main-bit line (MBL). A source line driver and sector decoder circuit is provided in each sector to isolate the memory sectors from each other.

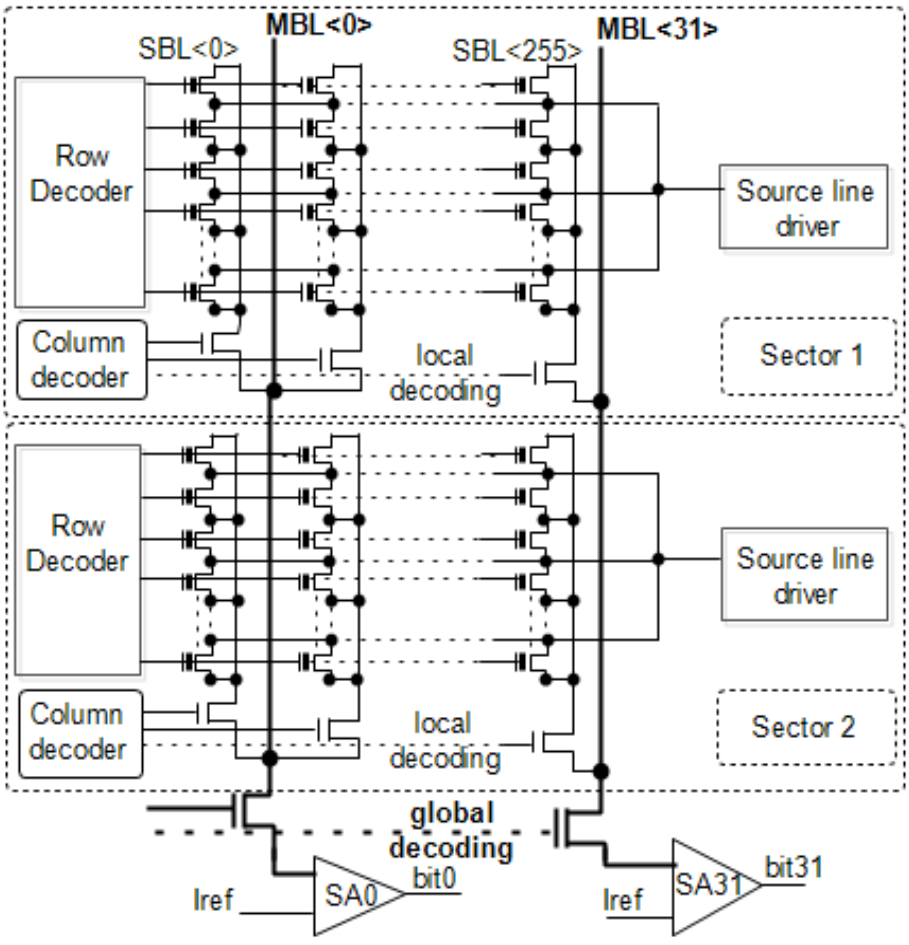

Fig.5. Memory array organization

1.2 MOTIVATION AND AIM OF THE RESEARCH

Today, with the evolution of integration technology, non-volatile memories are not only used for storing information, but integrated with other logic systems to perform various functions like reconfiguring the system on field and storing identification codes for smart cards etc.

Today, modern electronic devices like MEMS sensors, Mobile handheld devices etc. require faster access of data with low power consumption. The most critical functionality which governs the speed of Flash memories is the access time to read the data from a particular address and to reduce the power consumption, low supply voltages are used, which increases the battery life. But flash memories require high voltages for data program, read, and erase operations. Row decoders are used for interfacing between the memory core circuits operating at high voltage level and the peripheral circuits operating at supply voltage level.

Here, we have studied the different Row Decoder Architectures for NOR type Flash memories and developed a new Row Decoding Architecture for fast wordline charging which mainly governs the overall access time and is the main motivation of our research.

1.3 THESIS ORGANIZATION

The thesis is organized as follows. Section 2 describes the importance of Row Decoder in the overall design of the flash memory IP and how its design affects the overall access time of the memory. The important building blocks of the row decoder are also discussed in detail in this section. Finally, some existing architectures are also discussed.

Section 3 details the proposed row decoder architecture and the blocks which are optimized and validated for the desired application and performance. The results are shown and discussed in section 4 and finally the conclusion is frames at section 5. The future work is also briefed in this section.

2 ROW DECODER ARCHITECTURE AND BUILDING BLOCKS

2.1 ROW DECODER

The row decoder is the most compact part of the flash memory after the memory array. In fact, the final driver of the row decoder is an inverter that must fit into the row pitch, which is not trivial at all due to the reduced size of the memory cell [7].

Row decoders are generally divided into two cascaded sections: the first performs the required logical operations to select the desired wordline according to the address signals fed to the memory device; the second stage allows the selected wordlines to be connected to the required high voltages while making the others wordlines unselected.

2.1.1 IMPORTANCE OF ROW DECODER AND CHALLENGES ASSOCIATED WITH IT

For portable devices, like cellular phones and wireless sensors, high speed operation with low power consumption is an important aspect for efficient operation and long battery life. The factor governing the speed with which data is being accessed is determined by the charging time of the word-line capacitances of the individual memory cells in the array. The row decoder is one of the most important blocks for achieving a good access time with low power consumption [7-9] for these devices [9-10]. The faster we charge the cells in a particular wordline, the faster will be its operation.

It is also one of the most complex blocks to design because it has to provide a boosted voltage at the wordlines of the selected memory cells during program and read operation, and negative voltage during erase operation while the wordline of the unselected memory cells are driven to 0V [7]. In addition, during erase verify operation the unselected wordlines should be driven to -2V because the depleted memory cells can conduct even though the wordline is at 0V [7]. During depletion verify operation, the selected wordline is driven to 0v while the unselected wordlines are at -2V.

2.1.2 IMPORTANT BUILDING BLOCKS OF ROW DECODER

The important building blocks of the Row Decoder circuit are briefed below:

- The **predecoder** which is used for address decoding and other logical operations needed to perform different test mode and user mode operations. The devices used in the predecoder are low voltage devices usually operating at supply voltage (*Vdd*) level.
- The **level shifters** placed in the predecoder between the address buffers for interfacing between the digital gates operating at *Vdd* level of 1.2V and the high voltage memory core circuits.
- **Sector decoders** for decoding a particular sector according to the various memory operations. The memory is divided into sectors/blocks where the memory cells of a particular sector are formed on the p-well surrounded by n-well to isolate the non-selected sectors from the selected sectors during the erase operation.
- The **wordline drivers** for driving the wordlines of the memory array according to the address selected.

In the following section, we will be focusing on the different level shifters and discuss their need and importance in row decoder circuit for achieving high speed execution with less power consumption.

2.2 LEVEL SHIFTERS

In CMOS logic circuits, the dynamic energy is directly proportional to square of the supply voltage. Higher the supply voltage, the more is the energy consumption. Thus, the dynamic energy consumption can be reduced if we use low voltage supply in a circuit, without affecting its suitability for the desired purpose. However, in a mixed signal environment, when a low voltage circuit drives a high voltage circuit, the PMOS of the high voltage circuit may not turn off completely by the low voltage input. Thus, the need of level shifter arises wherever there is an interaction between the low voltage drivers and the high voltage gates.

2.2.1 POSITIVE LEVEL SHIFTERS

Positive level shifters are used for interfacing between the memory core circuits operating at positive high voltage level and the digital circuits operating at *Vdd* level. It is one of the most important circuits in flash memories for determining the access time as its switching speed mainly affects the wordline delay time of the memory array which overall affects the access time of the memory [9].

2.2.1.1 POSITIVE LEVEL SHIFTER TYPE-I

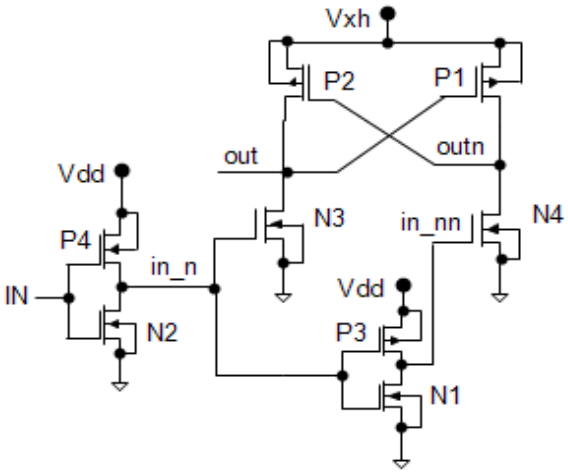

Fig.6. Conventional positive level shifter (Type-I)

Fig. 6 shows the conventional positive level shifter [10] using cross coupled PMOS transistors which latches the output and settles it to either at *Vxh* voltage or at 0V according to the input signal state of the level shifter. Vxh is the high supply voltage that is being generated by the charge pump circuit internal to the memory or from any source external to the chip [11]. N3 and N4 are high threshold voltage (V_t) transistors which has a certain doping profile and gate oxide thickness to sustain the high voltage stress that appears at their drain-gate and drain-source junctions [10]. If initially, node *out* is at 0V and node *outn* is at Vxh level and input node IN switches from low voltage level to high voltage level, then *in_n* goes to *Vdd* level and *in_nn* to ground. Transistor N4 turns on and N3 switches off. Since the *out* and *outn* node is initially at 0V and Vxh level, the driving capability of the pull down transistor N4 has to overcome PMOS latch action before the output changes its state. Also, when the input is switching from low to

high voltage level, both the transistors P1 and N4 are momentarily on and in this state a large number of hot carriers can be generated in the channel region between the source and the drain [11]. In the case of flash memories where the memory write and erase operation is performed tens of thousands of times, holes or electrons can get trapped in the gate oxide of the transistors [11]. This increases the leakage current and the static current consumption in standby mode, when the device is idle or not working [10], [11].

The major limitation of this level shifter is its inability to operate properly for voltages lower than 1V [9] because of high threshold voltage (V_t) of input transistors N3 and N4. The switching speed varies significantly with changes in the voltage *Vxh*, temperature and process corners.

Design guidelines:

The current driving capability of a MOS transistor during saturation is determined by the following equation [12].

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}|V_{gs} - V_t|^2 \qquad (2)$$

If it is in deep triode region then the current equation is

$$I_D \approx \mu C_{OX}\frac{W}{L}|V_{gs} - V_t||V_{ds}| \qquad (3)$$

where, V_{gs} is the gate-to-drain voltage and V_{ds} is the drain-to-source voltage of the MOS transistor. C_{OX} is the gate oxide capacitance, μ is the mobility while W and L are the width and length of the transistor.

At the time of switching, PMOS is in deep triode region and NMOS is at saturation. Since, the gate-source overdrive voltage of NMOS is very less than that of PMOS, the $\frac{W}{L}$ ratio of NMOS and PMOS has to be set accordingly so that the current drive exerted by the NMOS is much larger than the PMOS so that the output can change its state when the input changes. Also, the charging time of the load capacitance at the output of the level shifter or the output rise time is determined by the current driving capability of the PMOS device.

Moreover, the short circuit current "I" in a particular branch is determined by the on resistance seen by the individual transistors coming in the current path from Vxh to ground.

$$I = \frac{Vxh}{R_{on\ N3,N4} + R_{on\ P1,P2}} \qquad (4)$$

Vxh is the high supply voltage that is being generated by the charge pump circuit internal to the memory or from any source external to the chip [13]. $R_{on\,N3,N4}$ and $R_{on\,P1,P2}$ are the drain-source resistance or the output on resistance seen by the NMOS and PMOS transistors [12] which is given by:

$$R_{on\,N3,N4} = G_m || \frac{2}{\lambda \mu C_{ox} \frac{W}{L} |V_{gs} - V_t|^2} \quad (5)$$

$$R_{on\,P1,P2} = G_m || \frac{1}{\mu C_{ox} \frac{W}{L} |V_{gs} - V_t|} \quad (6)$$

Here, during switching, the transistors N3 and N4 are at saturation and V_{gs} is above V_t while the PMOS transistors are in deep triode region. After some time when the drain of the PMOS goes below the gate by $|V_{tp}|$ then it goes to saturation and the on resistance seen by the PMOS is governed by equation 5. G_m is the transconductance of the individual transistors.

2.2.1.2 POSITIVE LEVEL SHIFTER TYPE-II

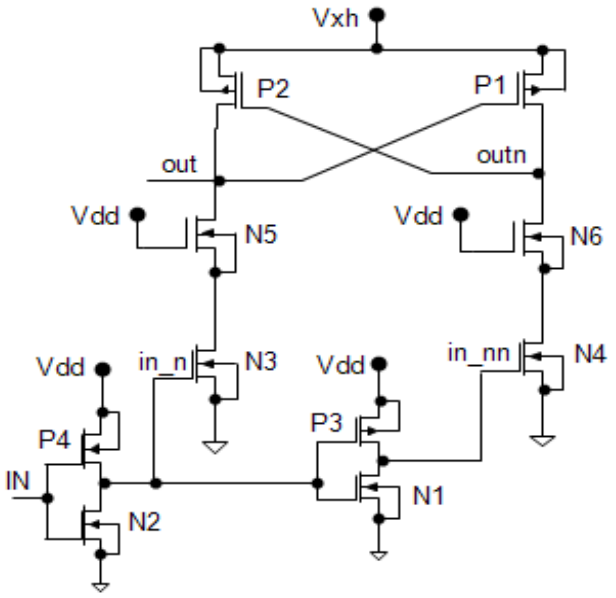

Fig.7. Positive level shifter (Type II)

The positive level shifter presented in Fig. 7 is a conventional level shifter [14] with input devices N3 and N4 as low voltage devices with lower threshold voltage (V_t). The voltage stress

on N3 and N4 is relaxed by putting a cascoded high voltage NMOS transistor between the drain and source junction of the input NMOS transistors and the cross coupled PMOS transistors.
As mentioned in section 2.2.1.1 that at the time of switching, holes or electrons can get trapped at the oxides of N3 and N4 which degrades the threshold voltage of the devices and is a major cause for leakage current. In Fig.7, although transistors N5 and N6 gets stressed because of the high voltage at its drain at the time of switching, N3 and N4 sees (Vdd-$V_{tN3,N5}$) at its drain junction. So, even though the characteristics of cascaded transistors N5 and N6 gets affected, N3 and N4 is relaxed form any stressed situation at their junction. Thus, the disadvantageous current in the standby state in type-I level shifter is eliminated in this design.

The transistors N5 and N6 in series with P2, N3 and P1, N4 increases the resistance in the overall current path from *Vxh* to ground, which decreases its switching speed. Also, as *Vdd* is used to drive the gate of the high voltage transistors N5 and N6, lowering the supply voltage decreases the overdrive seen by N5 and N6 which reduces the speed and performance of the overall circuit. This essentially limits the efficient operation of this level shifter for voltages below 1V [9].
Special designs can be incorporated where the transistors N5 and N6 can be driven by another voltage source *Vcc* which is approximately at ($Vdd + V_{t\,N5,N6}$) and will increase the overdrive voltage seen by N5 and N6. However, putting extra voltage source *Vcc* will greatly complicate the overall design.

2.2.1.3 POSITIVE LEVEL SHIFTER TYPE-III

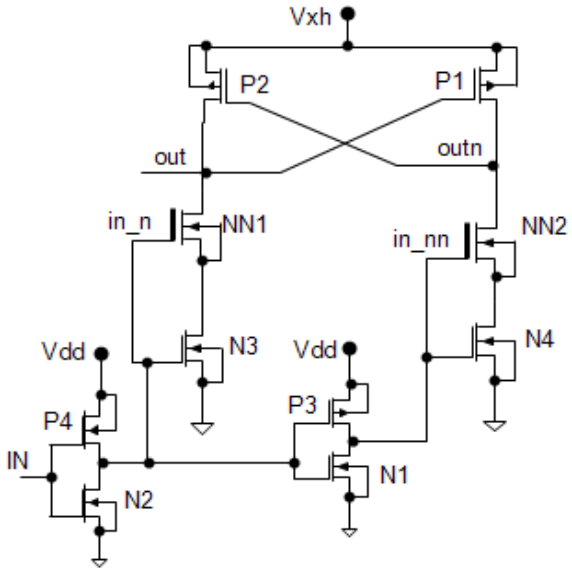

Fig.8. Positive level shifter (Type III)

Fig. 8 shows the conventional positive level shifter with input devices N3 and N4 as low voltage devices with low V_t and N4, N5 is depletion type NMOS devices with approximately "0" V_t [15]. The low overdrive voltage seen by the cascoded transistors N5 and N6 in Fig. 2 is rectified in this design using "0" V_t high voltage NMOS transistors. This also decreases the *ON* resistance path seen by the overall current path from *Vxh* to ground. Through proper sizing and optimization the switching speed achieved can be more than the conventional level shifters shown in Fig. 6 and Fig. 7.

The major limitation of this level shifter is the leakage current associated with it as the depletion MOSFETs conduct current even though the input at its gate is at 0V. The transistors N3 and N4 can have leakage current because of aging and various short channel effects associated with it as the transistors scale.

2.2.1.4 POSITIVE LEVEL SHIFTER TYPE-IV

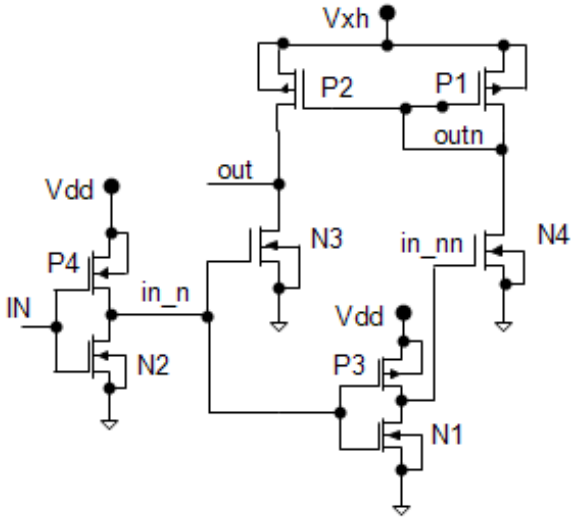

Fig.9. Positive level shifter (Type IV)

Another conventional positive level shifter depicted in Fig. 9 is a current mirror based level shifter [16]. The advantage with this type of level shifter is that the PMOS transistors are not latched and the input NMOS transistors can pull the output nodes faster which in turn increases the switching speed [16].

However, this type of level shifter cannot operate below 1V since high voltage transistors are used as input devices [9]. Also, a constant static current through P1 and N4 when *in_nn* is high causes large standby power consumption [16]. Another disadvantage of this level shifter is

that it cannot be used as an input to a negative level shifter in positive/negative or high/low level shifters since the *outn* node will clamp to (*Vdd* - $V_{t\,P1}$) and will not be able to switch off the input PMOS transistor of the negative level shifter whose gate will be connected to node *outn* [10].

2.2.1.5 POSITIVE LEVEL SHIFTER TYPE-V

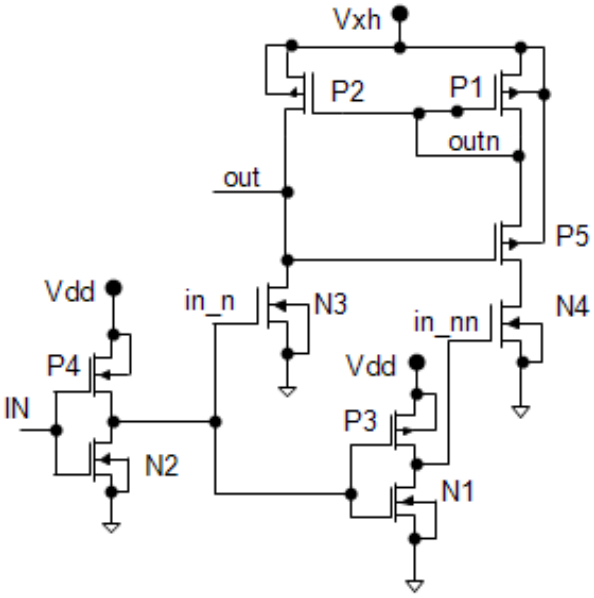

Fig.10. Positive level shifter (Type V)

The static power consumption through P1 and N4 in positive level shifter type-IV is eliminated in this design shown above in Fig. 10 [17]. P5 ensures that when out node charges to *Vxh* level, no static current can flow through the P1, N4 branch.

Here, if *IN* is low, *in_n* is high and *in_nn* is low, N3 conducts and pulls the node out low. As N4 is turned off, outn is charged through P1 until the gate and drain of P1 reaches (*Vxh* - $V_{t\,P1}$). If *IN* is high, then *in_n* is low and *in_nn* is high, N4 conducts, leading to a current flow through N4, P1 and P5. As P1 and P2 is a current mirror, this current also flows through P2, charging node *out* [17]. As *out* rises, P5 is turned off so that no static current can flow through P1, P5 and N4.

This level shifter also has the disadvantage of pulling the node *outn* to a maximum of (*Vdd* - $V_{t\,P1}$) and will not be able to switch off the input PMOS transistor of the negative level shifter whose gate will be connected to node *outn* [10].

2.2.2 NEGATIVE LEVEL SHIFTERS

Similar to the positive level shifter discussed in previous section, negative level shifters are used for the applications which require the interaction between the *Vdd* level signals with the negative high voltage signals. In this section we will discuss some state of the art negative level shifters which are used to change the voltage level from *Vdd* to a negative voltage where the negative voltage is coming from a negative charge pump. Negative charge pumps are boost converters used internal to the chips and is used to convert the supply voltage to a negative high voltage.

2.2.2.1 NEGATIVE LEVEL SHIFTER TYPE-I

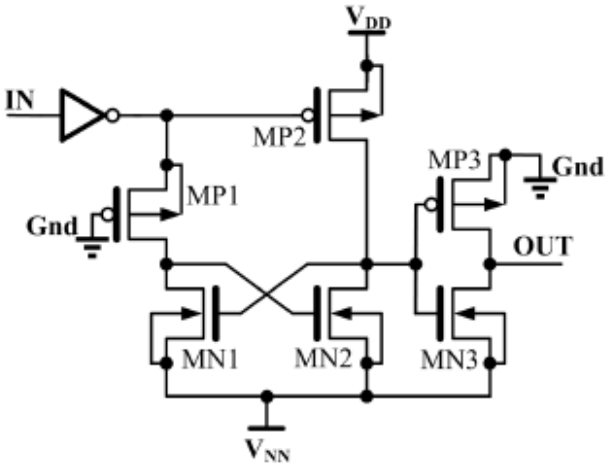

Fig.11. Negative level shifter (Type I)

Fig.11 shows the Type-I conventional negative level shifter [18] which switches from *gnd* to negative voltage which is coming from a negative charge pump [19]. The circuit is a feedback based structure rather than a cross coupled latch. Also, instead of using two PMOS transistors as input devices with an inverter for providing the direct and complementary inputs, it uses only one PMOS as input device and uses an inverter to switch the output voltage.

The maximum voltage stress on transistors MP1, MP2, MN1 and MN2 is ($Vdd + |V_{NN}|$) when V_{NN} is at negative high voltage level. This stresses the device if there is very less margin for the interaction between the positive and the negative voltages. For example, the transistors used here are 7V devices and if *Vdd* is at 2.5V, V_{NN} is at -7V and the input is at logic "1" level,

the transistors MP2 will get a drain-source and drain-bulk stress and transistors MN1 and MN2 will see a gate-source/bulk and drain-source/bulk stress.

The drawback of this level shifter is that it has no pull-down driving capability in normal mode i.e. in standby/read/program mode, when V_{NN} is at *gnd* level and if the signal *IN* is low. Then MP2 is at off state and the output node OUT is floating. Hence, there is no dc path to ground to drive the next stage. The output node can also jump to any arbitrary voltage because of coupling from other metal line which is an undesirable state since it can affect the stages which the output of the negative level shifter is driving.

The level shifter shown above in Fig.11 struggles to operate properly because as the supply voltage scales down, the threshold voltage becomes difficult to scale down with the supply voltage *Vdd* [10] since the high threshold voltage of the high voltage (HV) transistor is comparable to half of *Vdd*.

We can also enhance the driving capability of the input devices by increasing the W/L ratio of the transistors, however, that increases the parasitic capacitances and enhances the switching noise caused by gate-drain coupling and also increases the silicon area [20].

2.2.2.2 NEGATIVE LEVEL SHIFTER TYPE-II

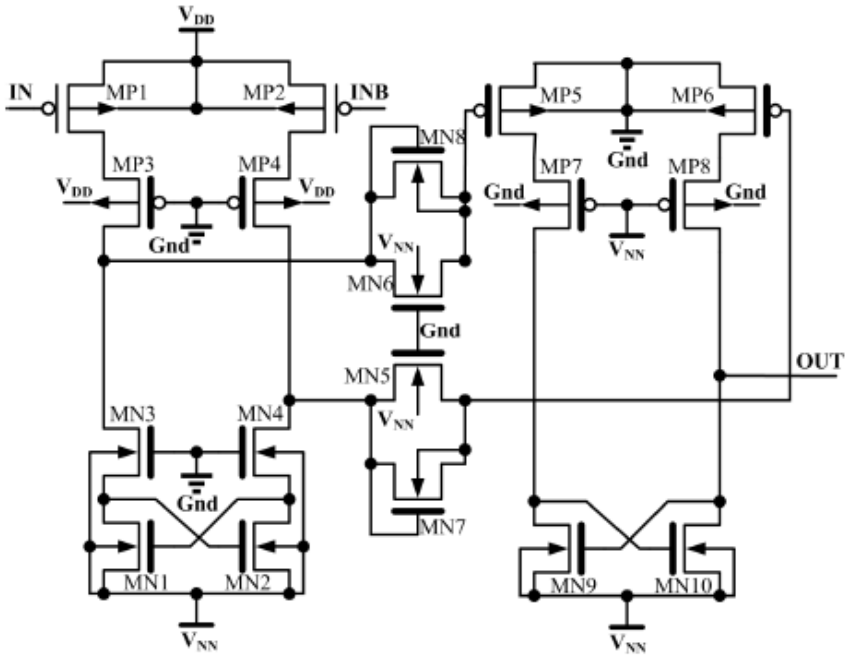

Fig.12. Negative level shifter (type II)

The Type-II conventional negative level shifter is shown in Fig. 12 which consists of two serially connected cross-coupled level shifters [21]. The first level shifter receives the input signal with swing from *Vdd* to *gnd* and provides an output with swing from a negative voltage *Vdd* to V_{NN} where, V_{NN} is a negative high voltage. The second level shifter receives the output of the first level shifter as input and drives the final output node from V_{NN} to *gnd*. Whenever the input changes its state, the pull-up PMOS transistors MP1 and MP2 have to overcome the NMOS latch action so that the output node can switch its state from *Vdd* to V_{NN} or from V_{NN} to *Vdd* voltage level. The current driving capability of the pull-up PMOS transistors is determined by the overdrive voltage and the W/L ratio. The overdrive voltage is mainly governed by the supply voltage *Vdd*. As *Vdd* is scaling down, the driving capability of the input PMOS transistors is reducing dramatically, leading to the increase in the transient time. To maintain adequate driving capability, the size of MP1 and MP2 has to be much larger than MN1 and MN2, resulting in large silicon area and increased capacitance which increases the switching noise [20].

In the meantime, we can eliminate the second stage of this negative level shifter with the pass transistor gates which are used for connecting the output of the first stage negative level shifter with the input of the second stage negative level shifter. This scheme can be used for applications which require both the supply voltage and the negative high voltage to drive its input node. Furthermore, the voltage stress seen at the drain-bulk junction by the transistors MN3, MN4 and MP3, MP4 can be eliminated by connecting the bulk of these devices to its source terminal which is incorporated in the proposed sector decoder design shown in Fig. 17. Also, if there is a need to switch the output node from V_{NN} to *gnd* rather than from V_{NN} to *Vdd* then we can put an inverter where the source of the pull up device is connected to *gnd* as exhibited in Fig. 11.

2.2.3 POSITIVE/NEGATIVE LEVEL SHIFTER

In this section, we will discuss about the conventional positive/negative level shifter circuit [10] which is used to convert the *Vdd* level voltage to high positive or negative voltage according to the need of the operation selected.

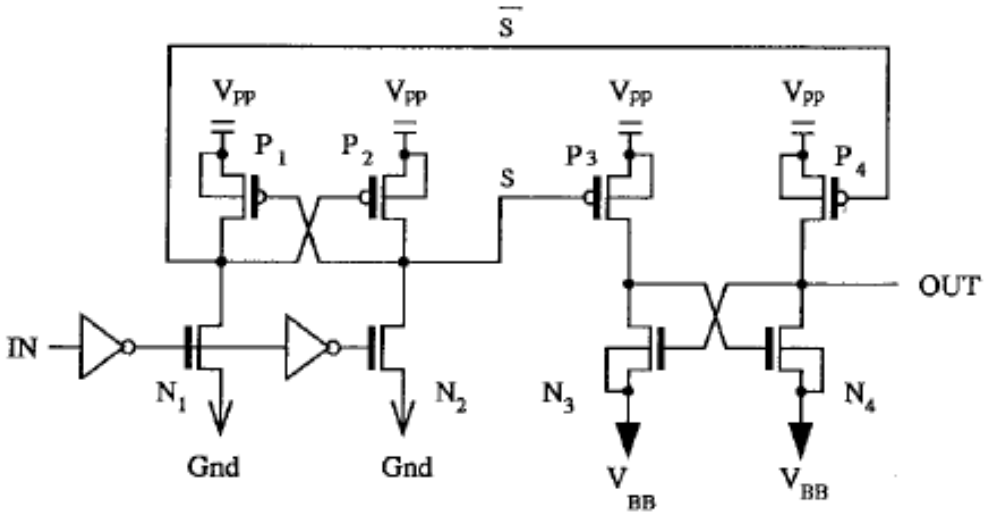

Fig.13. Positive/Negative level shifter

As mentioned in section 2, the row decoder circuit which uses negative gate erase type Flash memory requires both the positive high-level and negative low-level signals at the gate of the memory cell. This transition from high to low i.e. 4V to -2V or 0V to -7V is required during the erase verify and the erase operation. During read and program mode, the level shifter has to transit between 4V to 0V and 7V to 0V. *Vpp* will be at 4V during read and erase verify, 7V during Program, 2.5V during Erase, while, *Vbb* will be at -7V and -2V during Erase and Erase verify operation and it at 0V for all the other modes.

The switching speed of the output signals for the second level shifter is slow because of the switching delay of the first stage level shifter. This increases the switching current and the total power consumption becomes significantly large [10].

Also, as mentioned in section 2.2.2 that if we want to avoid any interaction between the positive and the negative voltages during any operation, which can violate the device safe operating area, then the design shown in Fig. 12 can be incorporated without the second stage and the pass transistors, which can provide both the positive voltage and the negative voltage at its output node. But, using such technique will drastically increase the output switching time as the second stage will add more delay in addition to the first stage. It can be explained by commenting that adding cascoded PMOS devices MP3 and MP4 will increase the resistance and parasitic capacitance along the output path which will decrease the output charging and discharging time.

A suitable solution is given in section 3.2.2 which takes into account these stipulations where the variation of the positive level shifter is reduced by using a positive level shifter which has the least variation in the switching speed with process variations and temperature. The supporting results are given in section 4.1 where the different types of positive level shifters are compared with the proposed level shifter in terms of switching speed delay, its variation and power consumption.

The solution for the negative level shifter is more application specific where the cascoded PMOS MP3 and MN4 is eliminated in the design given in Fig. 18, to make a symmetric switching from high to low and low to high voltage levels.

The simulations for the proposed negative/positive level shifter design are given in section 4.2.

2.3 LITERATURE STUDY OF SOME EXISTING ROW DECODER ARCHITECTURES

A number of row decoder architectures are presented and discussed in [5], [8], [22] and [23].

In Paper [5], the positive and negative signals generated in the row decoder circuit for driving the selected wordlines of the memory cell are coming from the positive charge pump and the negative charge pump separately. The wordline presented is a NMOS based driver. The drawback of this architecture is the use of NMOS based drivers which limit the full swing of the high voltage output signals. Also, the logic circuits used should be more since the positive signals and negative signals are driving the gate of the memory cell from two different sides.

Paper [8] discusses about the row decoder, the select gate decoder and the source line driver for driving the memory array. The signal AXA0~19 is a positive/negative level shifted signal which is driving the corresponding wordline drivers according to the address selected. The sector decoding is done by the BXA0~3 signals which produces the necessary voltages (positive/negative) in accordance with the different modes of memory operation. The BXA0~ 3 signals is generated by the predecoder circuit which is combination of logic circuits to provide the desired supply voltage to the wordline driver for driving the wordlines of the memory array. This architecture applies negative voltage at the gate during the program operation and to the bulk or p-well of the selected sectors during the erase operation, but the memory cell presented here, applies negative voltage only at the gate during the erase operation.

[22] Shows the row decoder circuit which consists of the wordline driver and three level shifters. The wordline driver is a parallel connection of two back to back inverters connected in an inverted fashion to each other i.e. the PMOS of one inverter is connected in parallel to the NMOS of the other inverter and vice versa. The level shifter placed in the path of the wordline of

the memory array is positive/negative level shifter while the level shifters which are placed for providing the requisite voltages to the wordline driver is a positive level shifter and a negative level shifter. A positive level shifter using the latch circuit is also discussed.

In [23] the algorithm for the different read operation of the memory array is given which discusses about the critical issues and the row and column decoding architecture is shown.

3 PROPOSED DESIGNS

3.1 POSITIVE LEVEL SHIFTER

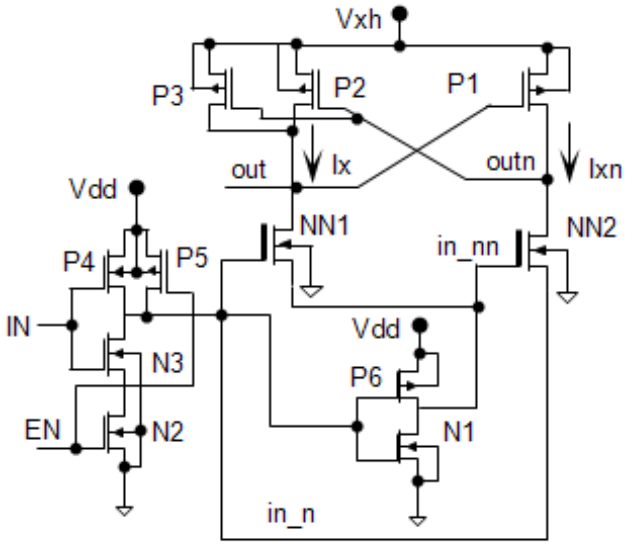

Fig.14. Proposed positive level shifter

Table I: Proposed positive level shifter operation (in volts, V)

IN	EN	in_n	in_nn	out	outn
Vdd/0	0	Vdd	0	0	Vxh
Vdd	Vdd	0	Vdd	Vxh	0
0	Vdd	Vdd	0	0	Vdd

The proposed positive level shifter is depicted in Fig. 14. The leakage current associated with the level shifter illustrated in Fig. 8 in section 2 is reduced by connecting the source of NN1 and NN2 to the output of the two inverters. Therefore, when the signal at node IN is low, *in_n* is at

Vdd and *in_nn* is at 0V. Thus, the source of transistor NN2 is at 1.2V when its gate is at 0V which enhances the threshold voltage of depletion type MOSFETs, evident from Fig. 15, and prevents the flow of leakage current. NN1 experiences the same phenomena when the input signal at node IN is high. This also helps to reduce the stress that is seen at the drain-source junction of the depletion type MOSFETs. The overall operation is also summarized in table I.

The level shifter has been designed in 90nm STM10 CMOS technology. It is simulated and optimized for minimum energy delay product, symmetric switching and high robustness for different high output voltages. The robustness of the design has been verified by simulating it at different process corners and temperatures. For, fair comparison, all the conventional positive level shifters are also designed in the same technology and is compared with the proposed design.

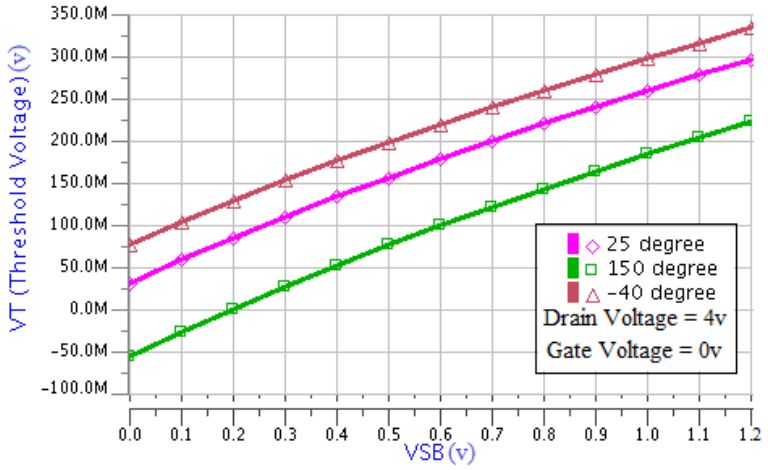

Fig. 15: Threshold voltage variation of depletion type NMOS with source-bulk voltage.

The short circuit current flowing across the two branches of the proposed design is given by equations 1 and 2 [1], [7]:

$$I_x = \frac{Vxh}{R_{on\,N1} + R_{on\,NN1} + (R_{on\,P2} || R_{on\,P3})} \qquad (1)$$

$$I_{xn} = \frac{Vxh}{R_{on\,N2} + R_{on\,N3} + R_{on\,NN2} + R_{on\,P1}} \qquad (2)$$

Where, I_x and I_{xn} are the current flowing across the branches *out* and *outn* and R_{on} is the output *ON* resistance of the transistors [1] governed by equations 3 and 4 when the transistors are in saturation and deep triode region respectively. V_{gs} is the gate-source voltage of seen by the

transistors, V_t is the threshold voltage, μ is the mobility, C_{ox} is the gate oxide capacitance, W is the width and L is the length of the individual transistors.

$$R_{on} = G_m || \frac{2}{\lambda \mu C_{ox} \frac{W}{L} |V_{gs} - V_t|^2} \quad (3)$$

$$R_{on} \approx G_m || \frac{1}{\mu C_{ox} \frac{W}{L} |V_{gs} - V_t|} \quad (4)$$

It is clear from the current equations given in equation 1 and 2 that the increase in I_x due to the decrease in the resistance path from *Vxh* to ground is cancelled by the decrease in the current I_{xn}. Thus, the power consumption is approximately same as that of the conventional type III positive level shifter of section 2. Moreover, the output resistance of the PMOS load connected to *out* node is reduced by connecting two PMOS devices in parallel to enhance its output load charging capability.

Furthermore, presence of EN signal discards the need of input buffers which block the digital signals to change the output state of the level shifter when a particular sector or wordline is being disabled [10].

One major concern in this design can be that the leakage current is still seen from the low voltage transistors P4, P5 and P6 when their respective inputs are at Vdd level when we scale down the devices. But, as the devices are not stressed by high voltage operations the reliability lifetime of these devices are higher than the NN1 and NN2 transistors. Additionally, the area has been increased in this design as compared to other designs because of the inclusion of P3 and the long channel lengths of NN1 and NN2 transistors, but with added functionality and the freedom to abolish the buffer at the output for symmetric switching delay. NN1 and NN2 have to be doped in a specific way to behave as a "0" V_t transistor and their minimum channel length is about 2.5 times the minimum channel length of the high voltage transistors.

3.2 PROPOSED ROW DECODER ARCHITECTURE

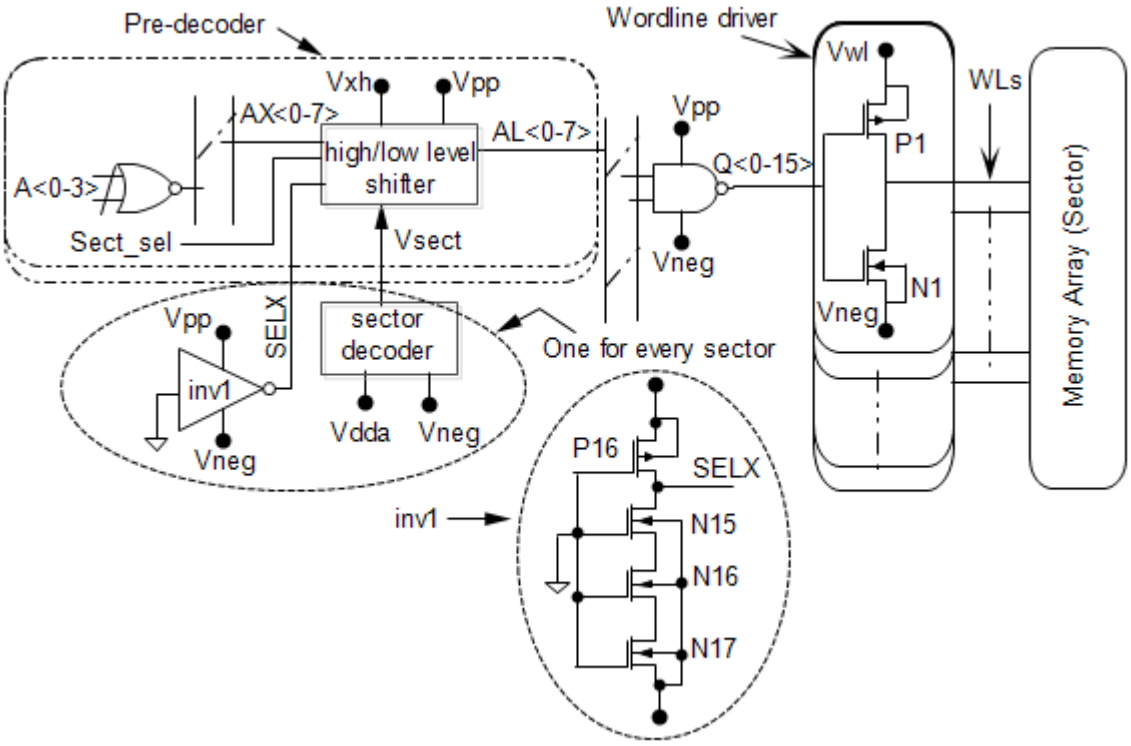

Fig.16. Proposed row decoder architecture

Table II: operating voltage conditions of the proposed row decoder circuit (in volts, V)

	Vxh	Vpp	Vwl	IN	SELX	Vneg	Vsect	Sect_sel	ER
Read	4	4	4	0	4	0	0	1.2	0
Program	7	7	7	0	7	0	0	1.2	0
Standby	0	4	4	0	4	0	0	0	0
Erase	2.5	0	0	2.5/0	-7	-7	-7/0	0	1.2
Erase verify	4	4	4	0	4	-2	-2	1.2	0
Depletion Verify	4	4	0	0	4	-2	-2	1.2	0

The proposed row decoder architecture is depicted in Fig. 16. Here, the no. of wordlines particular to one sector is 16. Its major blocks are Pre-decoder, sector decoder and wordline drivers for driving the 16 wordlines per sector. Negative gate biasing scheme that favors channel

length scaling for high density memory cells is used in erase condition [13], [14]. This technique also reduces the switching voltage and minimizes the effect of band-to-band tunneling which takes place between the reverse biased source/substrate junction [14] and thus improves the cell reliability. Table II shows the voltages at the different critical nodes of the row decoder.

The wordline driver consists of transistors P1 and N1 for driving the wordlines of the memory array. *Vwl* decodes the high voltage and is same as *Vpp* except the condition when the memory is in depletion verify condition. It is driven to *gnd* during depletion verify so that to check the threshold voltage of the selected memory cells, if they have gone below 0V or not. The memory cells whose threshold got depleted during the erase condition can be recovered by doing soft program to the depleted cell individually. The sizes of P1 and N1 are mainly governed by the layout pitch of the memory cell and are fixed accordingly. Inverter, inv1, is a skewed inverter which doesn't conduct or flips its state for *Vneg* of upto -3V when *Vpp* is at 4V, where Vneg comes from a negative charge pump [8]. *Vxh* and *Vpp* can either be generated by a positive charge pump or can be provided by any source external to the chip [8].

A<0-3> are the logical signals which are being generated by a microcontroller or a digital block internal to the chip according to the various memory operations selected. AX<0-7> are the level shifted decoded signals that will trigger the corresponding word lines of the memory cell depending on the address that is selected. AX<0-7> will be at *Vxh* level when selected or at 0v if not selected during the program and read operations where *Vxh* and *Vpp* are voltage levels coming from the charge pump which is set to 4.5v/8.5v according to read/program operation. During standby both *Vxh* and *Vpp* are at 4.5v and the Q<0-15> signals of the corresponding word lines are pulled to *Vpp* level. *Vxh* is at 2.5V when the circuit is at erase mode while *Vpp* is pulled down to 0v. During this mode, the word-lines are pulled down to -8.5V or 0V depending on the sector decoder output signal. The sector decoder output is at -8.5V if the sector is being erased or at 0V if it is not. *Vneg* is negative high voltage which is coming from a negative charge pump and is at -8.5v during erase operation and -2.5V during erase verify operation. It is kept at 0v during all the other operations. Table II shows the operating voltage levels of the various nodes of the row decoder according to the different memory operations. The wordline charging time for the high voltage levels during the read and program operation are given in section 4.3. Monte Carlo analysis is also done to validate the distribution of the wordline charging time for the typical condition.

3.2.1 NEGATIVE LEVEL SHIFTER AS SECTOR DECODER

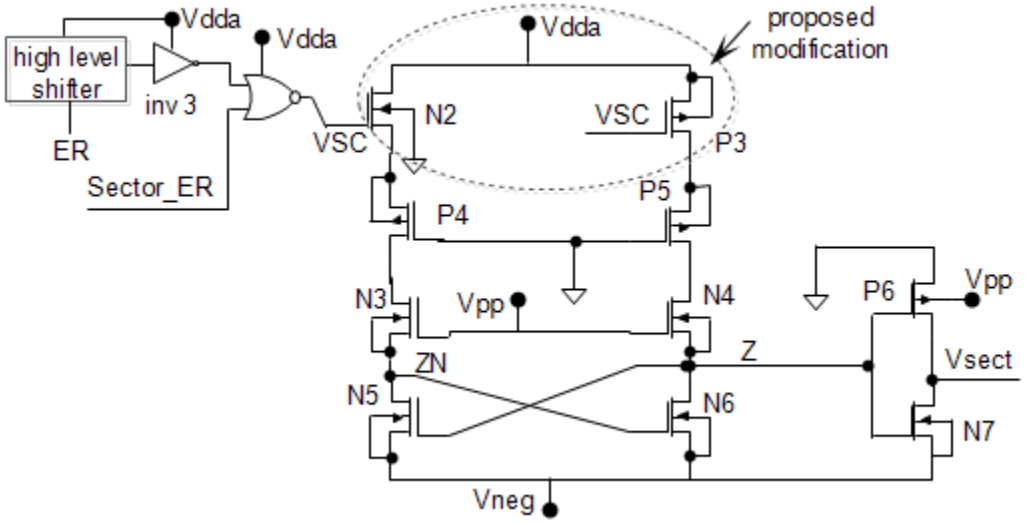

Fig.17. Sector decoder circuit

Table III: Sector decoder operation during different memory operation (in volts, v)

Memory Operation	Sector_ER	ER	VSC	Z	Vneg	Vpp	Vsect
Read, Program	0	0	0	Vdda	0	4/7	0
Erase	Vdda/0	Vdd	0/Vdda	-Vt/-7	-7	0	-7/0
Erase or Depletion verify	0	0	0	Vdda	-2	4	-2

Fig. 17 shows the sector decoder circuit where the conventional negative level shifter [8] has been modified to drive node *Vsect* according to the various operations selected. Here, both NMOS and PMOS are used as input devices which are connected to a single input without using two PMOS with an inverter between the two inputs as used in the conventional negative level shifter [8]. The high level shifter shown in Fig. 17 is a conventional high level shifter [14]. *Vdda* is a supply voltage of 2.5V. Signal IN is at 0V which drives *Vsect* to 0V during read, program and standby mode and to -2V during erase verify operation. During erase when ER signal is high i.e. at 1.2V, if *Sector_ER* signal is high then *Vsect* is set to *Vneg* otherwise it is at 0V. The maximum voltage stress on transistors N5 and N6 without N3 and N4 is (*Vdda* + |*Vneg*|) while

with N3 and N4 it is (|*Vneg*| – *Vtn*), where *Vtn* is the threshold voltage of N3 and N4. P4 and P5 prohibit the source or drain junction of N2 and P3 to interact with the positive voltage during erase operation. Thus, the voltage stress on the devices is relaxed which increases the device reliability and improves its lifetime. The voltage levels of the different nodes according to the different memory operations are given in table III.

3.2.2 POSITIVE/NEGATIVE LEVEL SHIFTER

Fig.18 shows the proposed positive/negative level shifter. NN1 and NN2 are depletion type MOSFETs with approximately "0" threshold voltage. The sources of these MOSFETs are kept at 1.2V when their respective gates are at 0V which increases the threshold voltage due to the body bias effect and reduces the leakage current. The *Sector_sel* signal is for selecting/deselecting the sectors and is at 1.2V if the sector is selected or at 0V if it is unselected. During erase, the *Sector_sel* goes to 0V for all the sectors irrespective of whether it is selected or not. P15 and N11 drive the node *ss* to 0V during erase. The signal *SELX* is at *Vpp* for all the conditions and is at *Vneg* during erase which switches off transistor N13 and blocks the *Vneg* signal to flow in that path. Inverter, inv2, is a standard inverter used for driving the transistor P2 which drives the unselected sectors to 0V during the erase operation. Moreover, the node *ss* is at 0V which provides N14 a sufficient drive to pull the output node to -7V. The simulation results are given in section 4.2 to authenticate the circuit operation across the different process corner, temperature and voltage variations. Table IV shows the different voltages of the critical nodes of the positive/negative level shifter for the different memory operations.

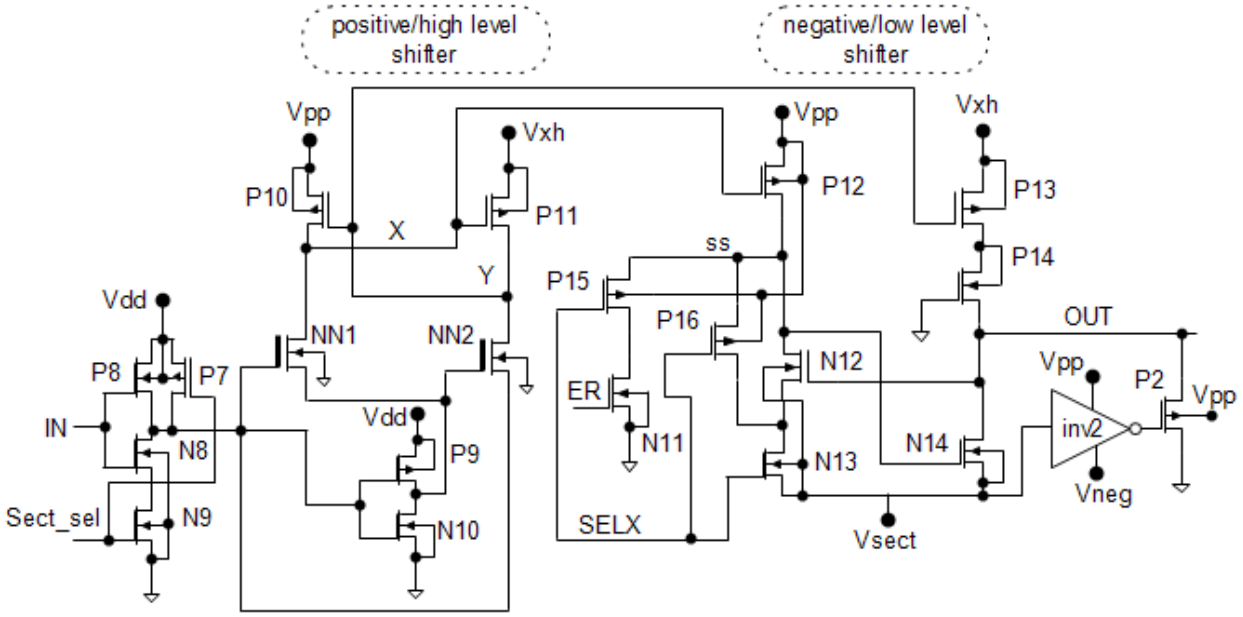

Fig.18. Stress relaxed high/low or positive/negative level shifter circuit for row decoder architecture

Table IV: Voltage conditions of the row decoder circuit for the selected sector (in volts, V)

	Read	Program	Erase	Erase Verify	Depletion Verify
Vxh	4	7	2.5	4	4
Vpp	4	7	0	4	4
Vneg	0	0	-7	-2	-2
Vsect	0	0	-7/0	-2	-2
IN	Vdd/0	Vdd/0	Vdd/0	Vdd/0	Vdd/0
Sector_sel	Vdd	Vdd	0	Vdd	Vdd
X	4/0	7/0	0	4/0	4/0
Y	0/4	0/7	2.5	4/0	4/0
ss	0/4	0/7	0	-2/4	-2/4
ER	0	0	Vdd	0	0
SELX	4	7	-7	4	4
OUT	4/0	7/0	-7/0	4/-2	4/-2

4 RESULTS AND DISCUSSIONS

The circuits proposed in this dissertation are designed and validated in 90nm STM10 triple well CMOS process and simulated in ELDO Spice circuit simulator. For fair comparison, the level shifters discussed in Section 2 are also implemented in the same technology and optimized through repetitive sizing and simulation. The transition characteristic of the different level shifter circuits are simulated for a *Vxh* of 4V, supply voltage of 1.2V, all the five process corners and at three different temperatures of -40℃, 25℃ and 125℃. The typical condition includes typical process corner for both PMOS and NMOS transistor, Supply voltage (*Vdd*) of 1.2V and a temperature of 25℃. The worst case condition is observed at slow-slow process corner, *Vdd* at 1.08V and temperature at 125℃. The best case condition is observed at fast-fast process corner, Vdd at 1.33V and temperature at -40℃.

In following section, firstly, the simulation results of the different positive level shifters will be shown and the inference from these results will be discussed. Secondly, the results of the proposed positive/negative level shifter circuit are compared with the conventional circuit and finally, the wordline charging time for the proposed row decoder will be shown for the different process conditions and temperatures.

4.1 POSITIVE LEVEL SHIFTERS

In this section, the first part will display the power consumption, switching speed or rise time and fall time of the proposed positive/high level shifters with the conventional positive level shifters discussed in section 2.2.1. The waveforms shown below are for the typical, worst and best case conditions which is observed at the above mentioned conditions. The positive level shifters are validated for a load capacitance of 50fF and 25fF at the *out* and *outn* nodes respectively.

Secondly, the total variation of the switching delay for the individual positive level shifters is also flashed with respect to the temperature for the different process corners at *Vdd* and *Vxh* at 1.2V and 4V respectively. Lastly, the distribution curves of the switching time for the different level shifters are demonstrated for 1000 Monte Carlo simulations at *Vdd* voltage of 1.2V, *Vxh* of 4V and temperature at 25℃. The process corner taken for this simulation is the statistical corner which takes into account the entire process corner and other device variations.

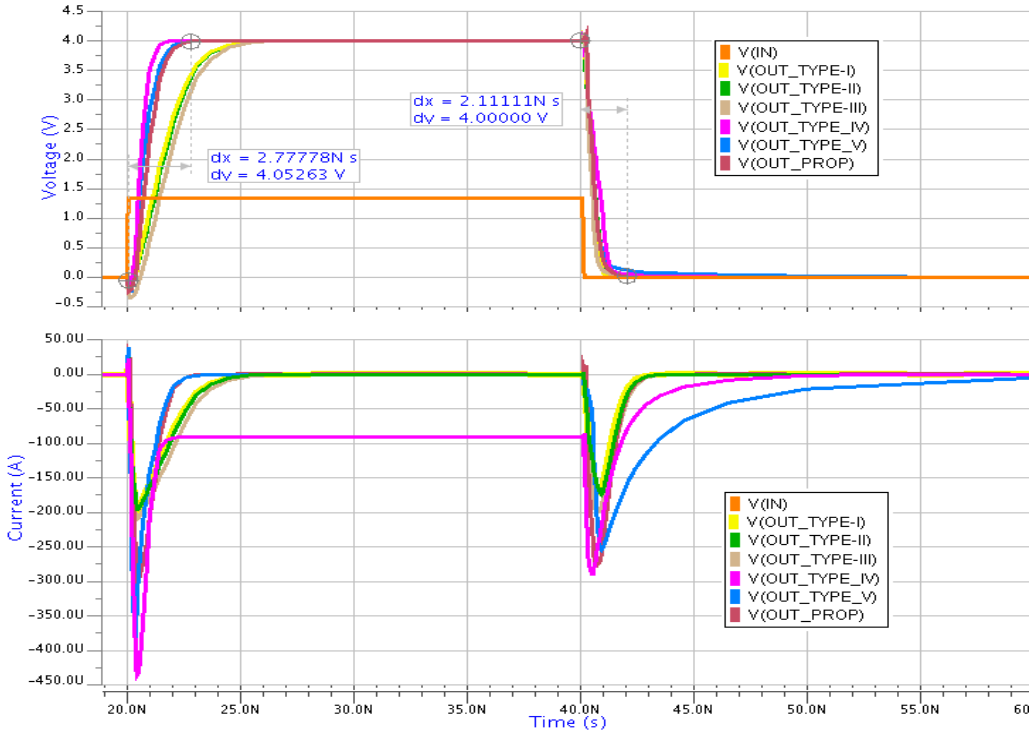

Fig.19. Switching delay and current consumption of the positive level shifter circuits for the best case condition

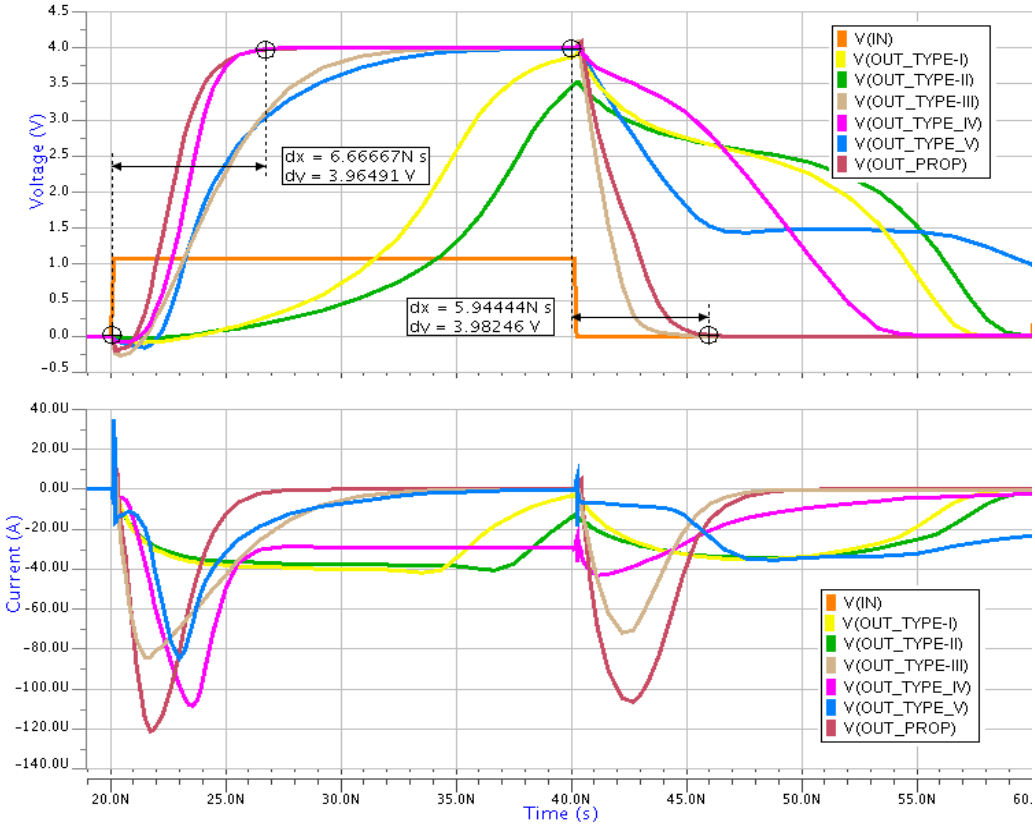

Fig.20. Switching delay and current consumption of the positive level shifter circuits for the worst case condition

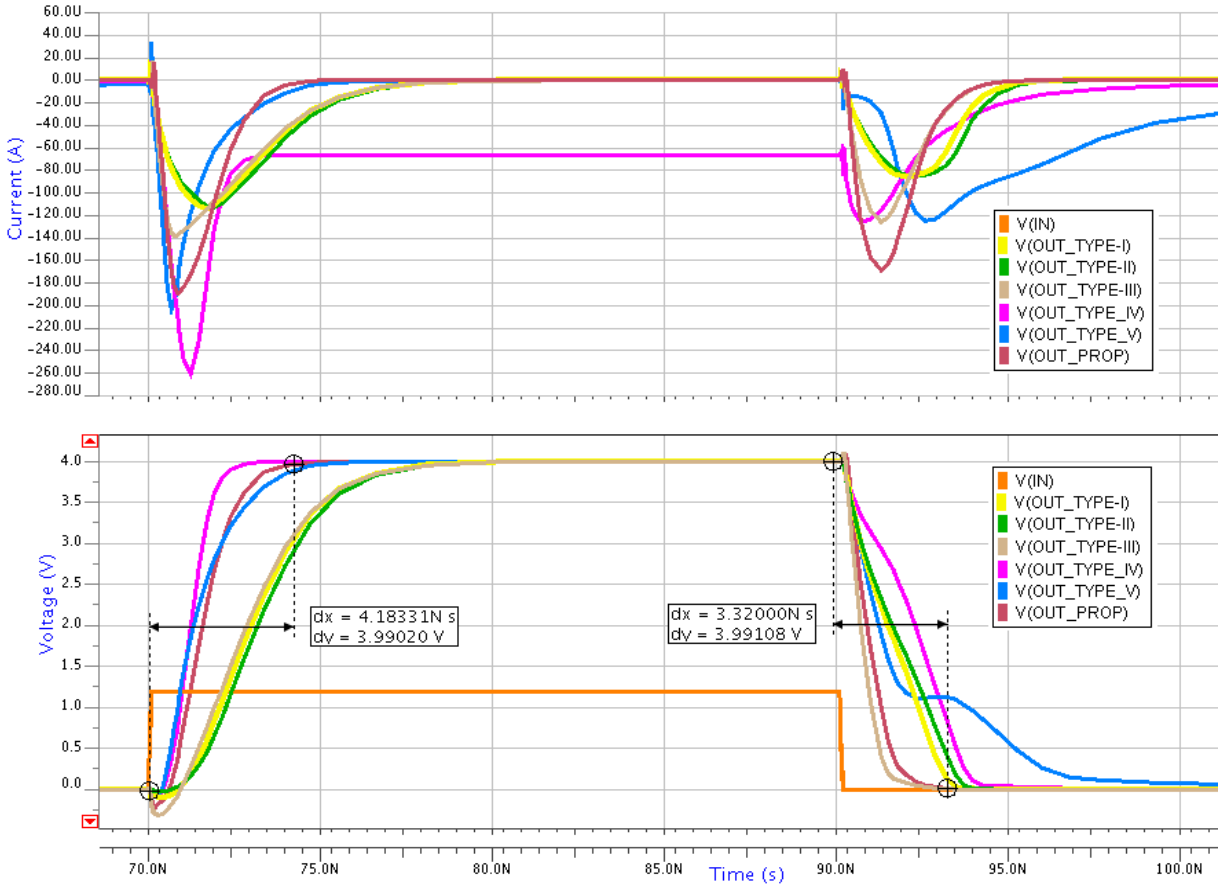

Fig.21. Switching delay and current consumption of the positive level shifter circuits for the typical condition

Table V: Summary of the output charging and discharging time of the positive level shifters discussed in section 2.

Level Shifter	Worst Case Charging Time (ns)	Worst Case Discharging Time (ns)	Typical Charging Time (ns)	Typical Discharging Time (ns)	Best Case Charging Time (ns)	Best Case Discharging Time (ns)
Proposed	6.66	5.94	4.18	3.32	2.77	2.11
Type I	Failed	18.35	7.10	3.27	4.29	1.00
Type II	Failed	19.49	7.48	3.60	4.42	1.10
Type III	11.25	3.36	7.15	1.85	4.72	1.07
Type IV	5.17	13.00	2.36	4.26	1.42	1.46
Type-V	15.12	Failed	4.53	8.06	2.03	2.51

Table VI: Total variation of the output charging and discharging time of the positive level shifters

Level Shifter	Total variation of the output charging time (ns)	Total variation of the output discharging time (ns)
Proposed	3.89	3.83
Type I	Failed	17.35
Type II	Failed	18.39
Type III	6.53	2.29
Type IV	3.75	11.54
Type-V	13.09	Failed

Table VII: Summary of the average power consumption of the different positive level shifters

Level Shifter	Worst Case power consumption (mW)	Typical case power consumption (mW)	Best Case power consumption (mW)
This Work	0.075	0.069	0.055
Type I	0.105	0.062	0.055
Type II	0.115	0.065	0.057
Type III	0.066	0.068	0.070
Type IV	0.105	0.178	0.249
Type-V	0.070	0.109	0.120

Table VIII: Summary of the Monte Carlo analysis of the different positive level shifters for Vdd=1.2V and Vxh=4V

Level Shifter	Average value of rise time (ns)	Standard deviation of rise time (σ)	Average value of fall time (ns)	Standard deviation of fall time (σ)
Proposed	3.60	0.146	2.32	0.118
Type I	7.22	0.444	3.31	0.602
Type II	7.47	0.467	3.64	0.648
Type III	7.21	0.311	1.85	0.074
Type IV	2.40	0.150	4.02	0.525
Type-V	4.51	0.955	8.28	1.09

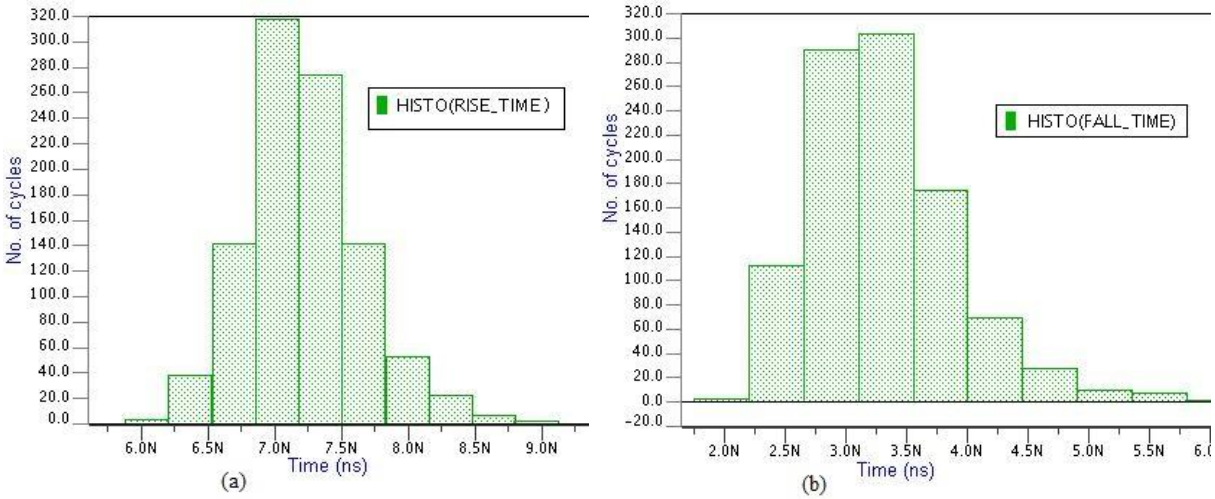

Fig.22. Distribution curve of type-I positive level shifter for 1000 Monte Carlo simulations (Vxh=4V, Vdd=1.2V) (a) rise time (b) fall time

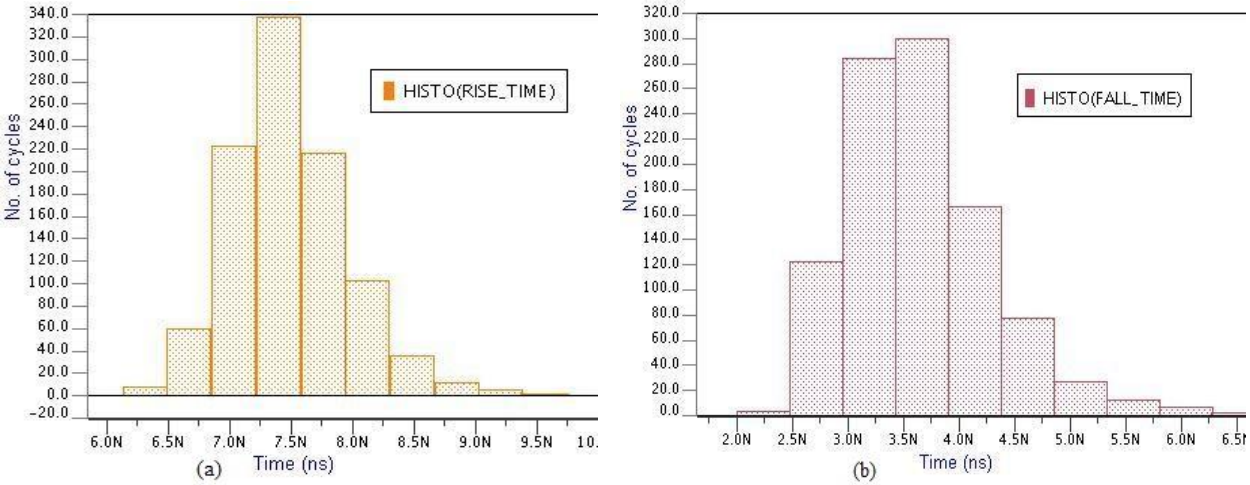

Fig.23. Distribution curve of type-II positive level shifter for 1000 Monte Carlo runs (Vxh=4V, Vdd=1.2V) (a) rise time (b) fall time

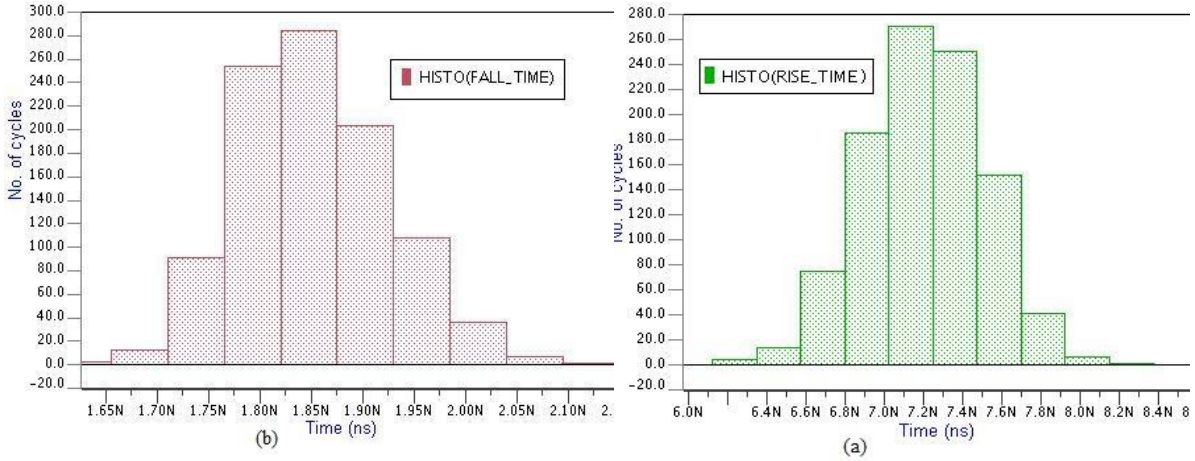

Fig.24. Distribution curve of type-III positive level shifter for 1000 Monte Carlo runs (Vxh=4V, Vdd=1.2V) (a) rise time (b) fall time

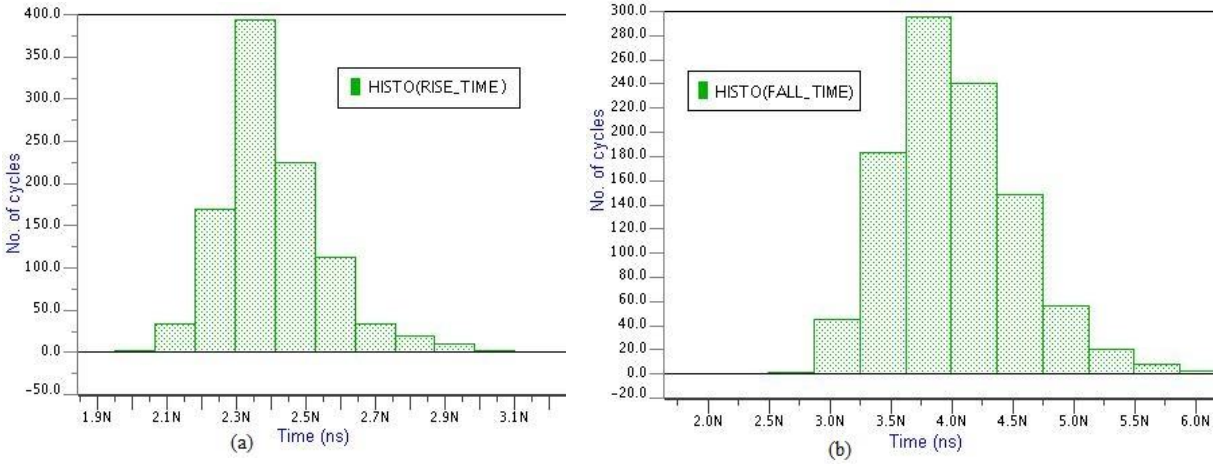

Fig.25. Distribution curve of type-IV positive level shifter for 1000 Monte Carlo runs (Vxh=4V, Vdd=1.2V) (a) rise time (b) fall time

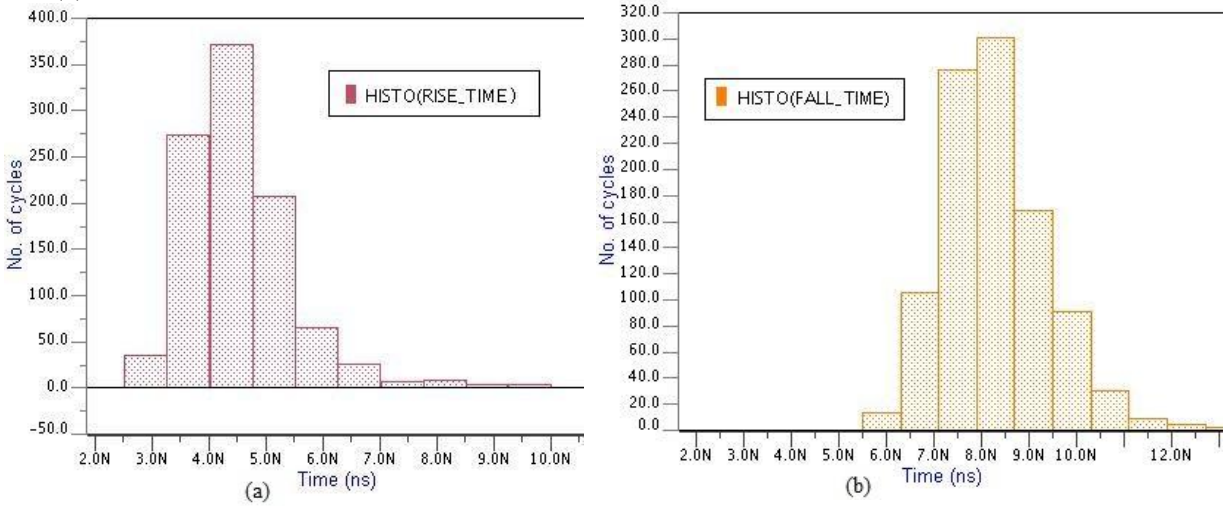

Fig.26. Distribution curve of type-V positive level shifter for 1000 Monte Carlo runs (Vxh=4V, Vdd=1.2V) (a) rise time (b) fall time

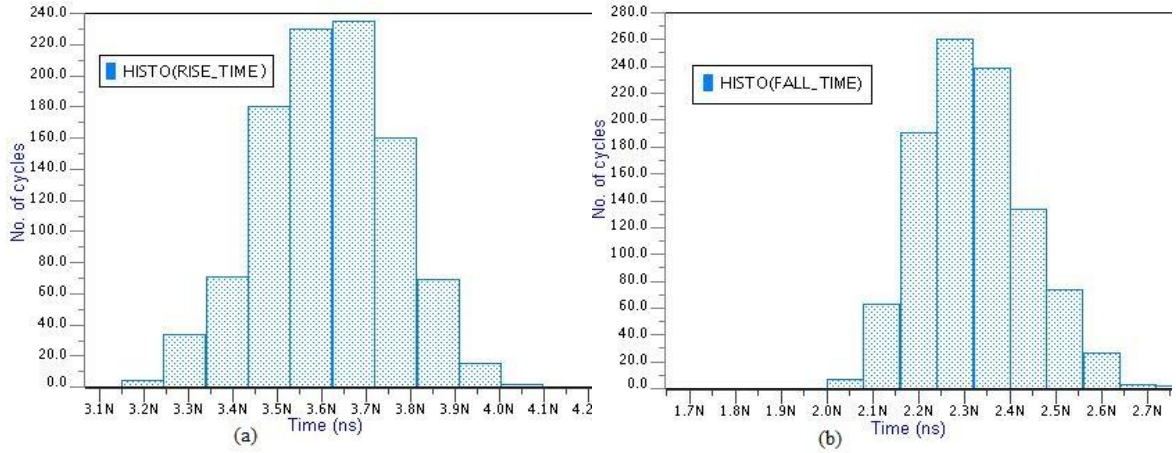

Fig.27. Distribution curve of proposed positive level shifter for 1000 Monte Carlo runs (Vxh=4V, Vdd=1.2V) (a) rise time (b) fall time

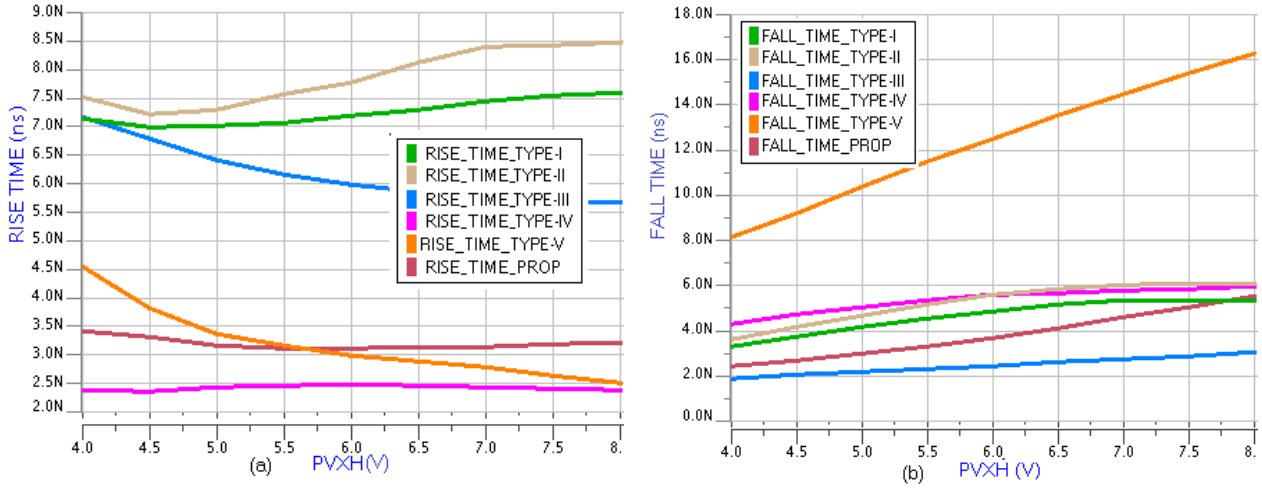

Fig.28. Switching delay of the positive level shifters at typical process corner with variation in Vxh voltage with Vdd at 1.2V (a) rise time (b) fall time

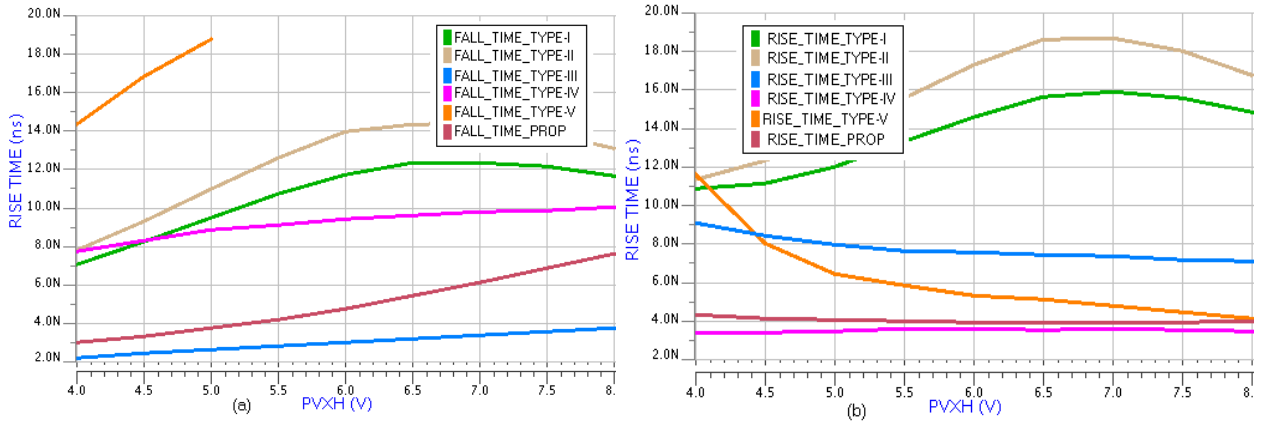

Fig.29. Switching delay of the positive level shifters at slow-slow process corner with variation in Vxh voltage with Vdd at 1.08V (a) fall time (b) rise time

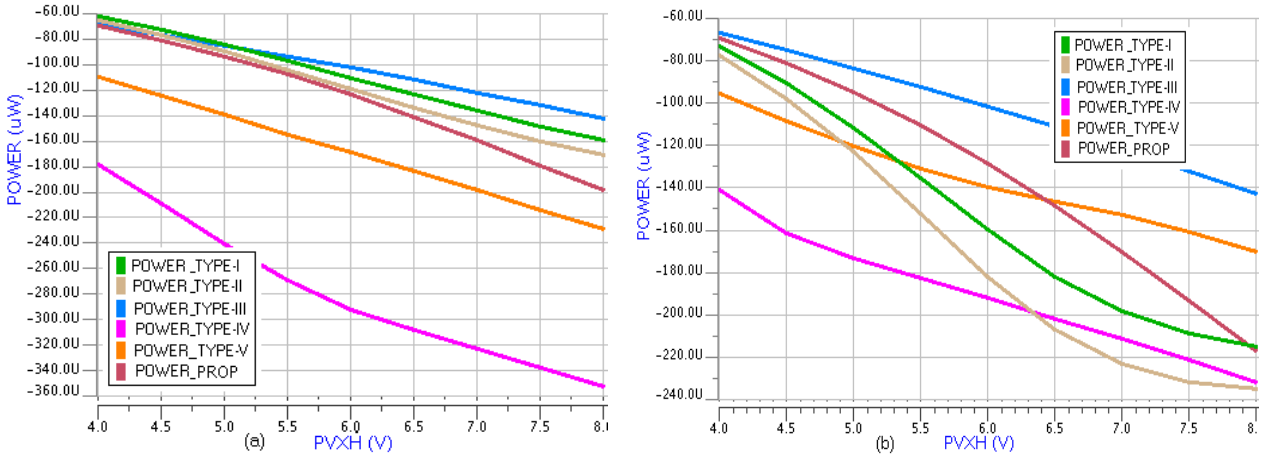

Fig.30. Average power consumption of the positive level shifters with variation in Vxh voltage (a) typical corner with Vdd at 1.2V (b) slow corner with Vdd at 1.08V

Discussion:

Fig.19-21 shows the switching characteristics of the different positive level shifters from *Vdd* to *Vxh*=4v for the typical, best and worst case conditions. The typical, best and worst case conditions observed are already mentioned in the beginning of this section. It shows that the switching characteristics of the positive level shifter type I, II, IV and V varies significantly with the process conditions and supply voltage variations because of the high voltage devices used as input devices which are being driven by the low voltage signals. Also, there is a bump observed at the fall time for the type-V positive level shifter because of the coupling capacitance (Cgd) of P2 which pulls down the outn node which is initially charged to (*Vdd*- *Vt*), thus making P2 to sustain the drive exerted by N3 when in_n is at *Vdd* level which also increases the dynamic power consumption of the level shifter.

The switching variation of the type II and the proposed level shifter is greatly reduced because of the collective use of the low voltage input devices and the depletion type high voltage devices in cascode between the input transistors and the cross coupled PMOS transistors. The proposed level shifter shows improvement in the rise time because of P3 connected parallel to P2 which increase the output load charging time. But the power consumption increase because of the decrease of the on resistance path during the switching of the level shifter. The overall summary of the output charging and discharging time is also given in table V and VI while table VII tells about the average power consumption of the different level shifters observed for the three extreme conditions. Table VIII summarizes the Monte Carlo results of the different positive level shifters. The distribution curves for the rise and fall time are also shown in Fig. 22-27. Table VIII tells that the sigma (standard deviation) variation is less for the proposed level shifter for both the rise and the fall time. The simulation is performed for *Vdd*=1.2V, *Vxh*=4v, Temperature=25℃ and at the statistical process corner which takes into care all the process variations.

Fig. 28 and 29 shows the output rise and fall time while Fig. 30 shows the variation in the average power consumption for the variation in *Vxh* voltage at the typical ad the slow process corner with *Vdd* at 1.2V, Temperature at 25℃ for the typical condition and *Vdd* at 1.08V, Temperature at 125℃, for the slow process condition. It can be seen that the switching delay of the proposed level shifter doesn’t vary too much as *Vxh* varies. Also the power consumption of the proposed level shifter varies linearly for the wide range of variation in temperature, voltage and process conditions which will help the designer to predict its behavior for a certain condition even if its power consumption is little bit higher than some of the conventional level shifters.

4.2 POSITIVE/NEGATIVE LEVEL SHIFTER

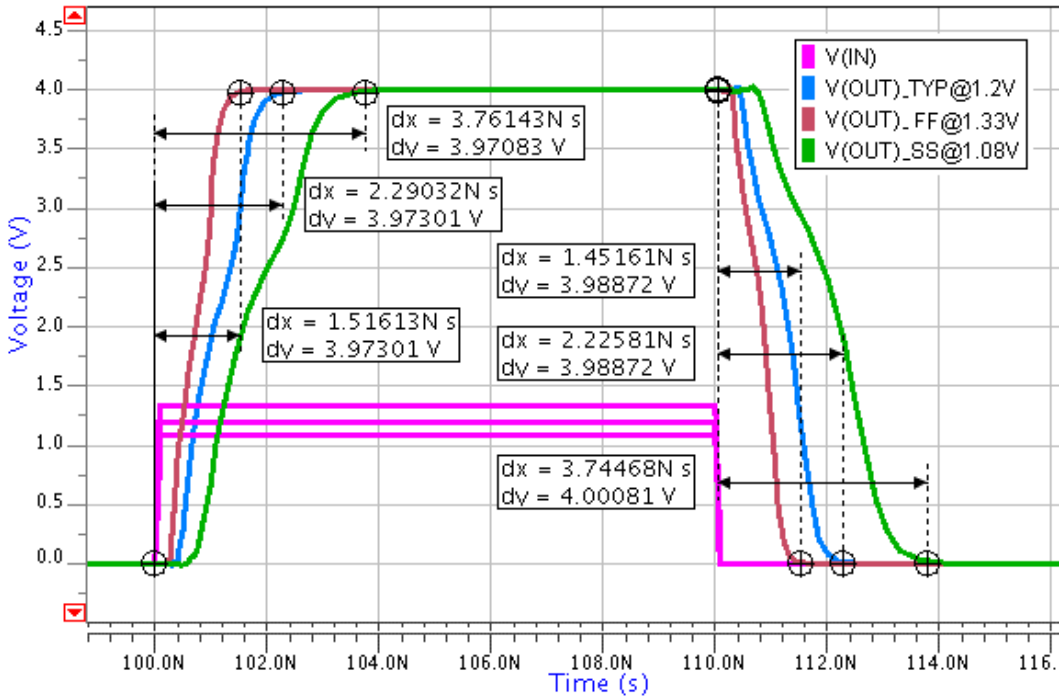

Fig.31. Switching delay of the positive/negative level shifter for Vxh and Vpp at 4V

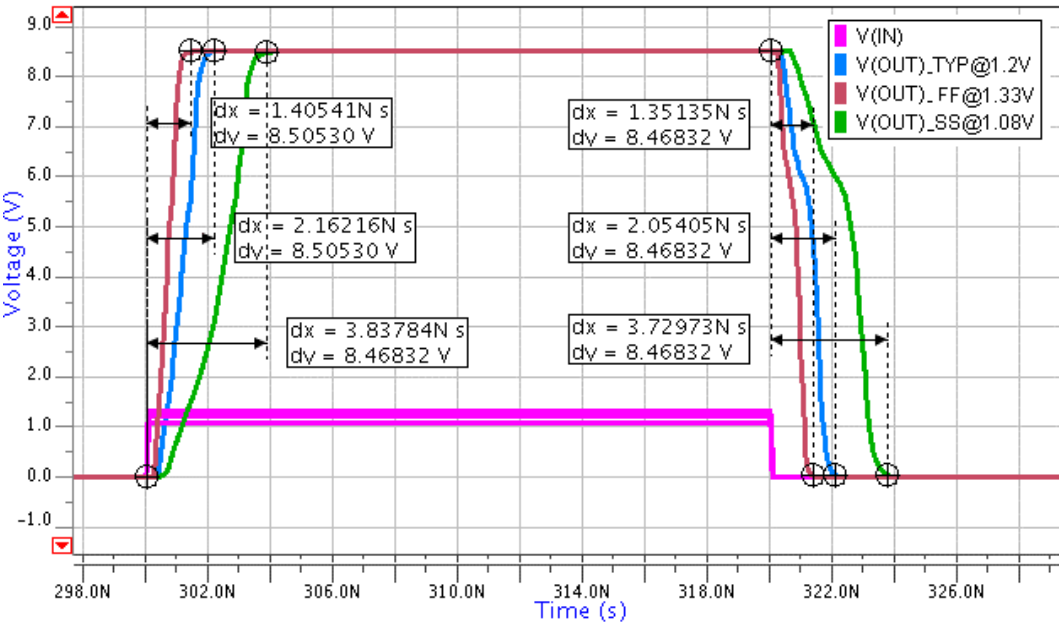

Fig.32. Switching delay of the positive/negative level shifter for Vxh and Vpp at 8V

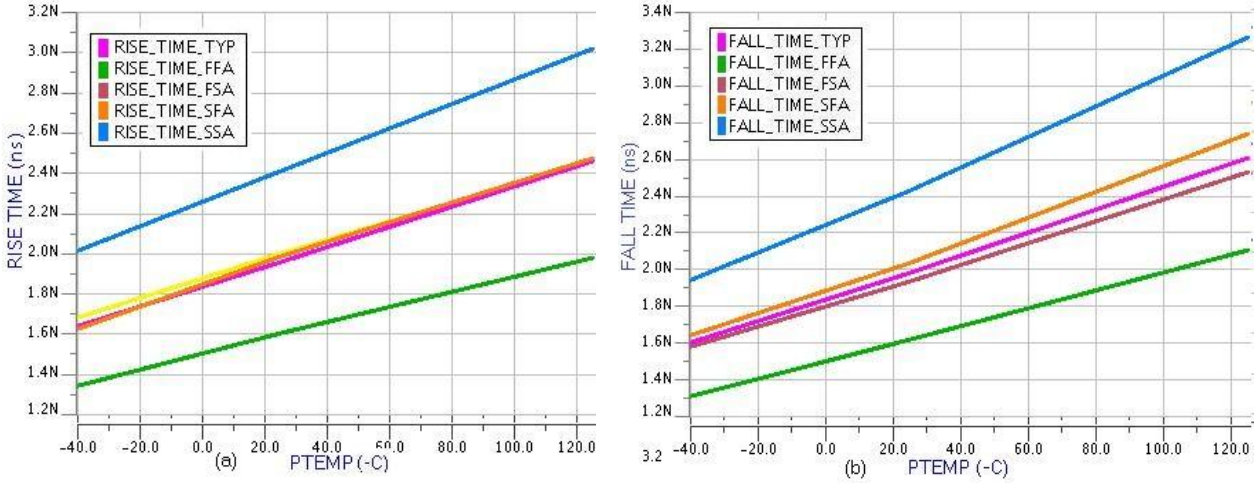

Fig.33. Switching delay of the positive/negative level shifter with variation in temperature for Vxh, Vpp at 4V and Vdd at 1.2V (a) rise time (b) fall time

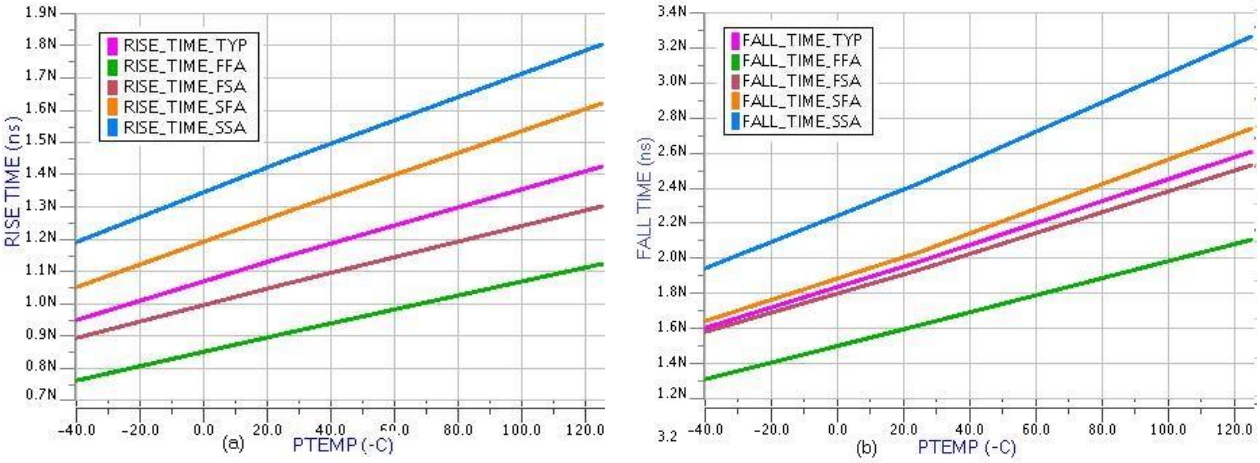

Fig.34. Switching delay of the positive/negative level shifter with variation in temperature for Vxh, Vpp at 8V and Vdd at 1.2V (a) rise time (b) fall time

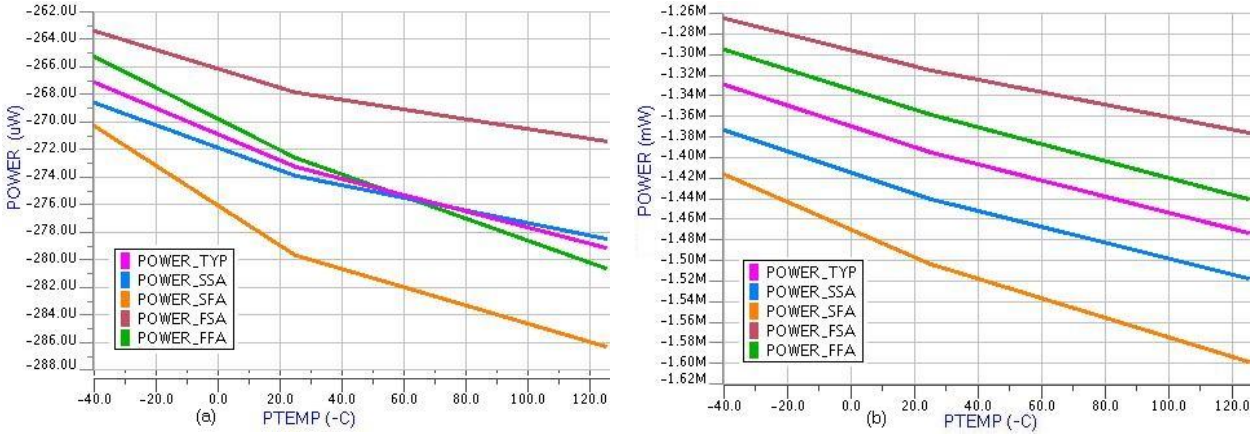

Fig.35. Average power consumption of the positive/negative level shifter with variation in temperature (a) Vxh, Vpp at 4v and Vdd at 1.2V (b) Vxh, Vpp at 8v and Vdd at 1.2V

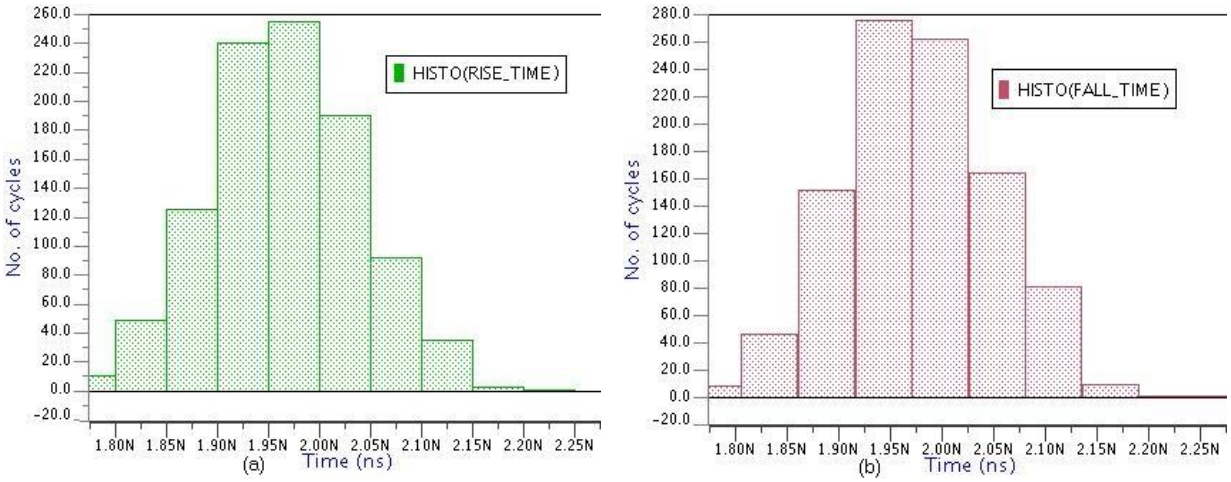

Fig.36. Distribution curve of the positive/negative level shifter for 1000 Monte Carlo simulations (a) rise time for Vxh, Vpp at 4V and Vdd at 1.2V (b) fall time for Vxh, Vpp at 4V and Vdd at 1.2V

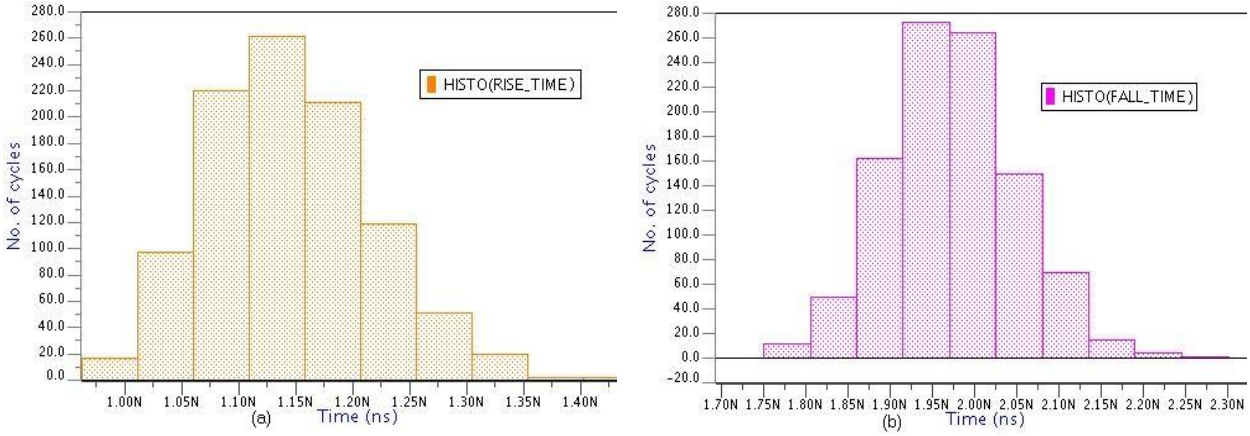

Fig.37. Distribution curve of the positive/negative level shifter for 1000 Monte Carlo simulations (a) rise time for Vxh, Vpp at 8V and Vdd at 1.2V (b) fall time for Vxh, Vpp at 8V and Vdd at 1.2V

Table IX: Summary of the Monte Carlo analysis for the positive/negative level shifter

Level Shifter	Average value of rise time (ns)	Standard deviation of rise time (σ)	Average value of fall time (ns)	Standard deviation of fall time (σ)
Vxh=4V, Vdd=1.2V	1.98	0.082	1.95	0.090
Vxh=8V, Vdd=1.2V	1.13	0.071	1.95	0.085

Discussion:

Here, first of all the switching delay of the proposed high/low or positive/negative level shifter is shown in Fig. 31 and 32 for *Vxh* and *Vpp* at 4V and 8V respectively. The output rise and fall time is quoted for the typical, fast and slow process corner with the corresponding supply voltages. It is observed from the figures that the output rise and fall time are quite equal for the two *Vxh* voltage levels which also helps to discard the need of using buffers which are used to makes the output switching symmetric.

Fig. 33 and 34 shows the variation of the output rise and fall time with respect to variation in temperature for the typical condition for *Vxh*, *Vpp* at 4V and *Vxh*, *Vpp* at 8V. It can be inferred from the figure that the switching delay is same for both the output rise and fall time. Fig. 35 shows the average power consumption of the high/low level shifter for the different *Vxh*, *Vpp* voltages with respect to change in temperature at the typical condition. It shows that the power consumption of the high/low level shifter is in mW for the case when *Vxh*, *Vpp* is at 8V. This condition can be analyzed for the fact that the high/low level shifter is designed and sized to work efficiently for *Vxh* and *Vpp* at 4V which is the read mode condition and is a critical condition for the memory. This is a major drawback of this level shifter for the conditions where the memory is programmed for hundreds of thousands of times during which the *Vpp* and *Vxh* will supply 7V to the high/low level shifter.

Figures 36 and 37 show the distribution curve of the switching delay of the level shifter circuit for 1000 Monte Carlo simulations and the standard deviation is given in table IX. Fig. 36 shows the results for *Vdd*=1.2V, *Vxh*=4V, *Vpp*=4v, Temperature=25℃ and at statistical process corner which takes into care all the process variations. Fig. 37 shows the results for *Vdd*=1.2V, *Vxh*=8V, *Vpp*=8v, Temperature=25 ℃ . Table IX summarizes the Monte Carlo analysis of the Positive/Negative level shifter.

4.3 ROW DECODER

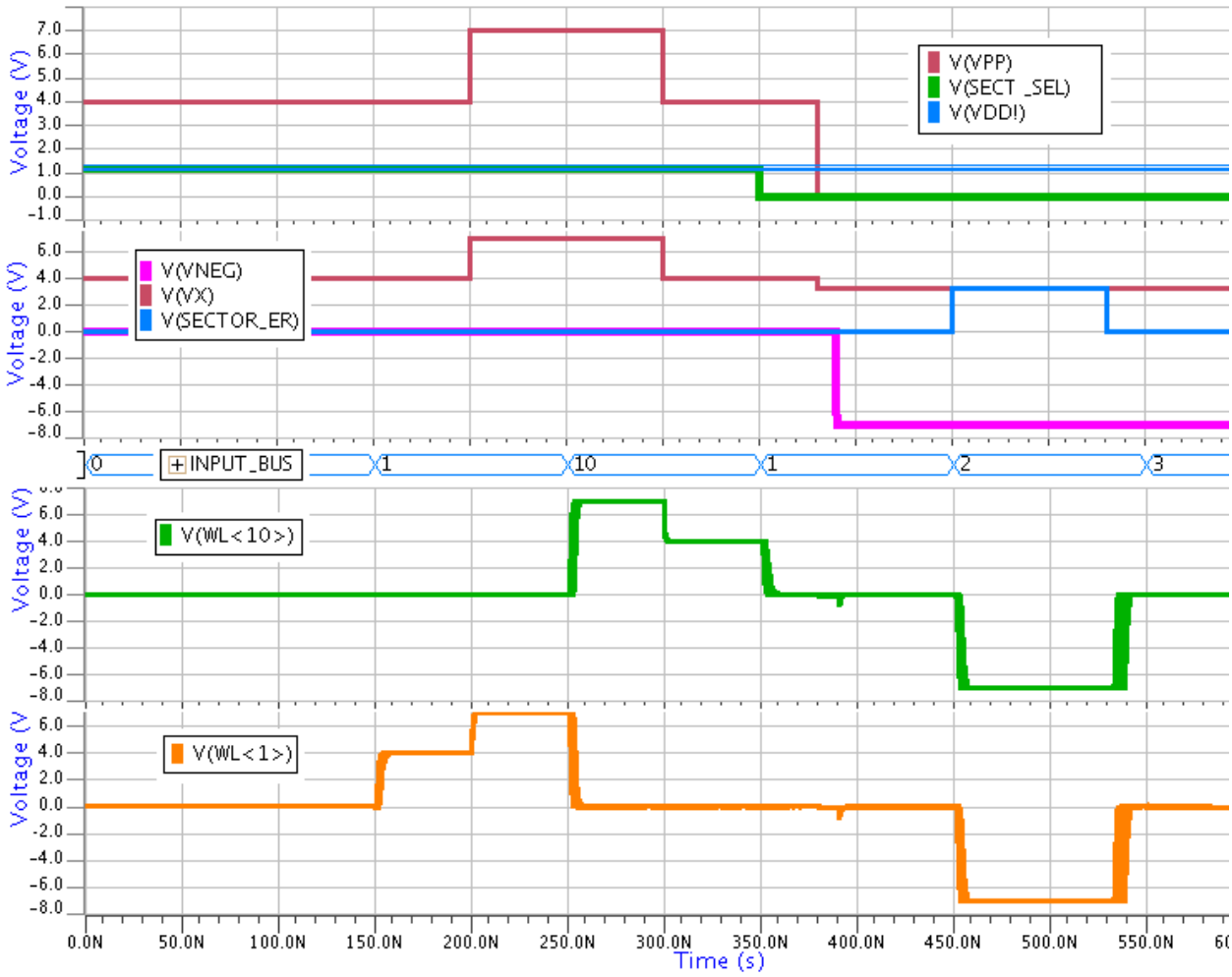

Fig.38. Read, Program and Erase operations shown collectively for a particular sector along the different process corners and temperatures.

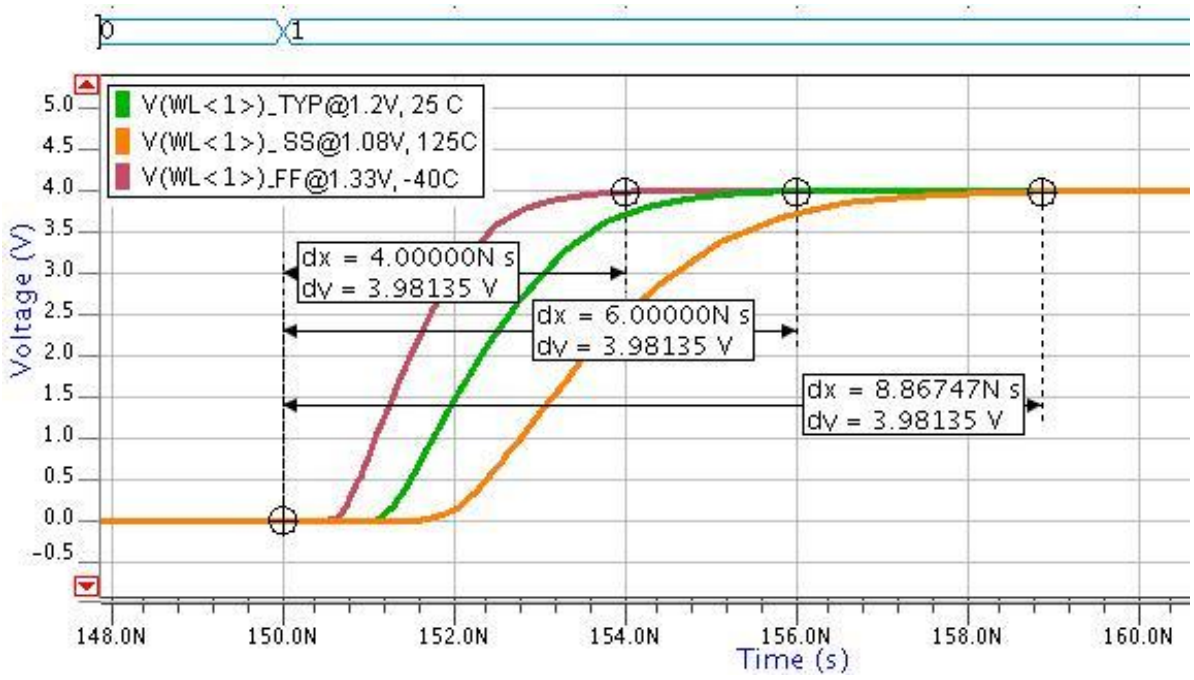

Fig.39. Wordline charging time for the typical, worst and best case condition for Vxh and Vpp at 4V

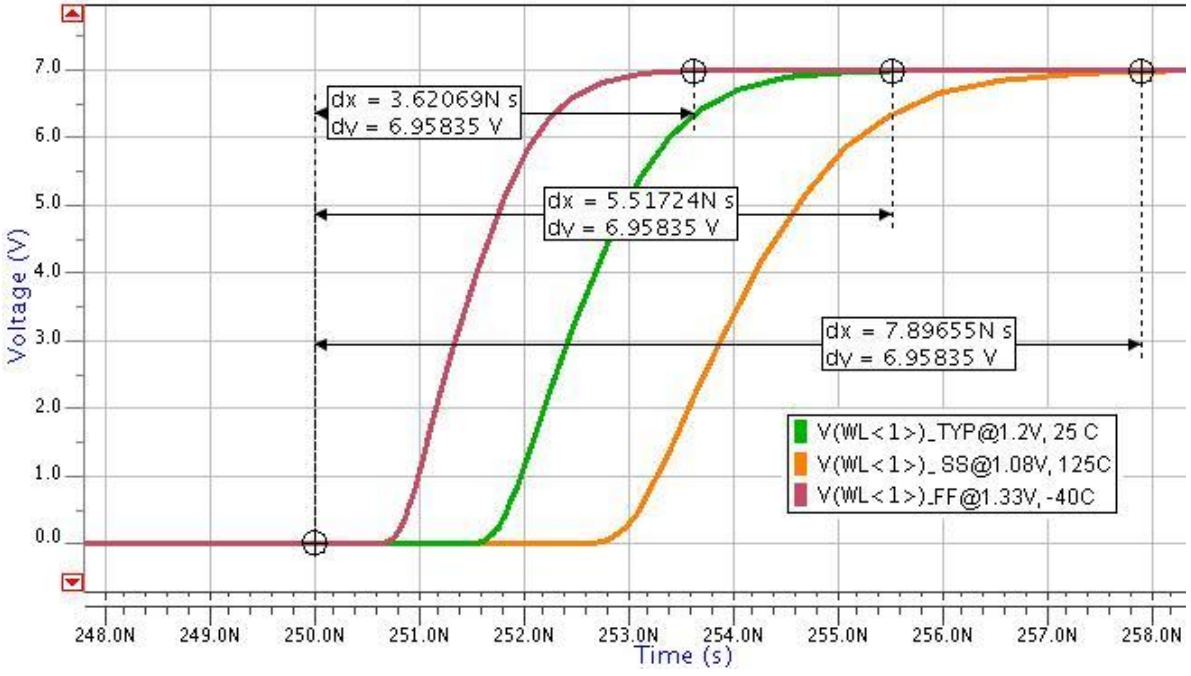

Fig.40. Wordline charging time 1for the typical, worst and best case condition for Vxh at 8V

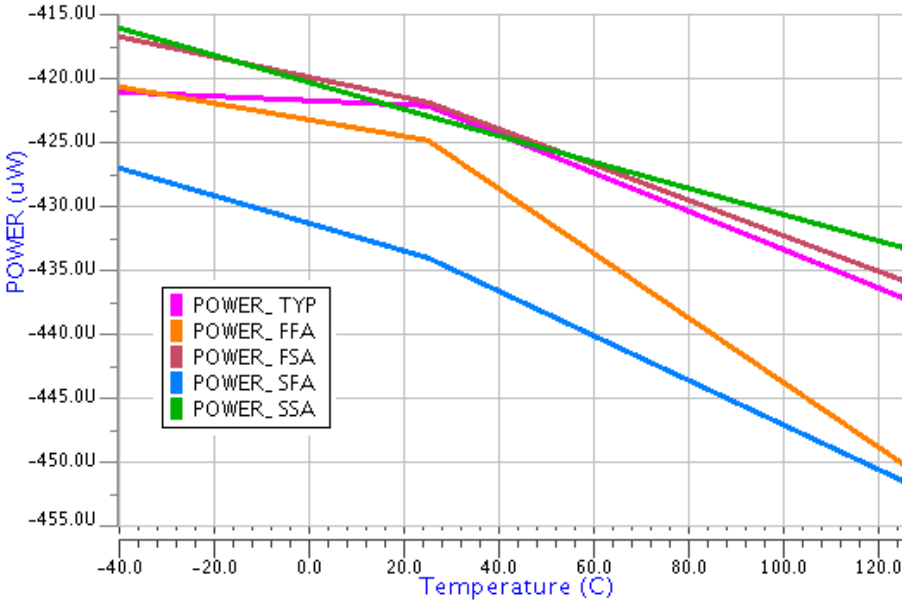

Fig.41. Average power consumption of the row decoder along the different process corners for read condition and Vpp, Vxh at 4V and Vdd at 1.2V

Discussion:

Here, the user mode operations that is memory read, program and erase are shown in Fig. 38 for all the different process, temperature and supply voltage variations. It can be seen that the *Sect_sel* signal disables the respective wordline of the memory array even though the address is selected for that particular sector. This helps in sector selection and de-selection locally without the use of tri-state buffers at the digital interfaces of the memory which will simplify the overall design. *Sector_ER* signals determines the sector which is to be erased or not and accordingly helps in switching of the positive/negative level shifter.

Fig. 39 and 40 shows the wordline charging time for the read and program operation where the wordline is charged to 4V for read and 7V for program operation. The critical and important being the read because the wordline charging time for this operation will mainly govern the overall access time while for program it is not too important because the program pulse itself is in micro seconds. It can be seen from Fig. 39 that the worst case charging time during the read condition is 8.867 ns which is observer for *Vdd* = 1.08V, temperature = 125℃ and slow process corner. Although, it can be seen from Fig. 41 that the worst case average power consumption is observed for PMOS slow and NMOS fast process corner with respect to variation in temperature and Vpp, *Vxh* at 4v and *Vdd* at 1.2V. Here, PMOS slow infers to high threshold voltage and NMOS fast infers for low threshold voltage.

5 CONCLUSION

5.1 SUMMARY

A row decoder architecture, incorporating novel high/low level shifter and sector decoder, has been designed to achieve a high speed wordline decoding. A positive level shifter is also proposed in this work which can switch faster from low input voltage to high output voltage with less variations with changes in temperature and process conditions. The average power consumption calculated for the row decoder circuit for the typical condition is 0.422mW. For the high/low or positive/negative level shifter circuit it is 0.274mW and it is 0.069 mW for the proposed positive or high level shifter.

The device characteristics for the proposed row decoder and its building blocks i.e. sector decoder and high/low or positive /negative level shifter is given in Table X which tells us about the test conditions and the safe operating voltage limit of the transistors used in the row decoder circuit. Table XI will inform about the device operating voltage limit for the proposed positive level shifter.

Table X: Device characteristics of the proposed row decoder architecture

2.5V device	N2, P3
7V device	P1, P2, P4-P6, P10-P16, N1, N3-N7,N12-N17, NN1,NN2
1.2V device	N8-N11, P7-P9
Erase time	150ms
Program time	100us

Table XI: Operating voltage limit of the transistors used in the proposed positive level shifter

Vxh voltage device	P1-P3, NN1, NN2
1.2V device	N1-N3, P4-P6

5.2 FUTURE WORK

The row decoder architecture has been a crucial one for the efficient operation of the memory address decoding. The length of the row decoder or the number of devices that are placed in the row decoder mainly governs the x-axis pitch of the memory since it is placed next to the memory array. With time, many architectures has been proposed for the fast and efficient decoding of the memory.

In this dissertation, we have also tried to open up some new techniques of decoding the memory array which can decode the memory address faster taking less chip area. This work can further help the researchers and engineers working in this field to think in a new dimension to design the row decoder and its building blocks for flash memories.

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