Asymmetric High-Density Low Leakage SRAM Cells

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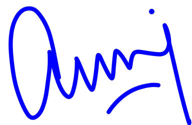
THESIS CERTIFICATE

This is to certify that the thesis titled, **"Asymmetric High-Density Low Leakage SRAM Cells"**, submitted by **Ajay Shroti**, to the Indraprastha Institute of Information Technology, Delhi, for the award of the degree of **Master of Technology**, is original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulation relating to the degree. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.



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ABSTRACT

Embedded memories occupy up to 70% of the area and account for 30-50% power consumption in advanced digital SoCs. A large part of this power is leakage power. Therefore, high-density, low-leakage SRAM cells are desirable. We propose two asymmetrical SRAM cells and benchmark with conventional 6T, 5T, and 4T SRAM cells. The first SRAM cell is a 4TA asymmetrical SRAM cell. We designed it under iso-stable constraints. We show that in a 130nm CMOS technology, the proposed 4TA cell is denser by up to 7% than 6T SRAM cells and has about 4X lower leakage than 6T SRAM cells. However, the performance is lower in 4TA as compared to 6T SRAM. The second SRAM is a 5TA asymmetrical SRAM cell. We designed 5TA under iso-area constraints. Our analysis shows that the proposed 5TA cell has about 10X and 6.23X lower leakage than the conventional SRAM cell in 130nm and 65nm CMOS technology, respectively at a similar performance point.

KEYWORDS: 6T SRAM, 5T SRAM, 4T SRAM, Figures of Merit, Write Margin, Static Noise Margin, Performance, Asymmetric 4TA SRAM, Asymmetric 5TA SRAM

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ABBREVIATIONS

IIITD	Indraprastha Institute of Information Technology, Delhi
SRAM	Static Random Access Memory
SoCs	System on Chips
6T	Six Transistor
5T	Five Transistor
4T	Four Transistor
FOMs	Figures Of Merit
SNM	Static Noise Margin
PVT	Process, Voltage and Temperature

NOTATION

μ	Mean
σ	Sigma

CHAPTER 1

INTRODUCTION

1.1 Motivation

SRAM, or static random-access memory, is a type of nonvolatile memory that maintains information as long as power is applied. SRAM is used in SOCs as cache memory because SRAM has a faster write/read access time than other types of memory, increasing the SOCs's speed and performance. The performance of SOCs increases with the expansion of SRAM capacity. However, both leakage and overall area increase. Conventional six-transistor (6T) SRAM is the most commonly used SRAM and accounts for up to 70% of the die area in modern SOCs [1], consumes a major share of leakage during standby periods [2] and scaling of 6T SRAM is not possible because the stability and performance of 6T SRAM reduces. These are the limitations of using 6T SRAM in SOCs. This highlights the need for an SRAM design to minimize leakage and area footprint and provide high performance.

1.2 SRAM Architecture

A memory array is made up of a 2-dimensional 2^Mx2^N array of memory cells, where M and N represent the column and row address widths, respectively. Each cell stores a single bit of data. To access the contents of the array, you need to assert the word lines (WLs) of a particular row, which is referred to as the address. The data required by the user is stored in the bit cells of that row.

An SRAM array consists of multiple circuits that work sequentially to read and store data. Figure 1.1 provides an overview of all the sub-circuits of the SRAM memory. Here is a brief explanation of each sub-circuit:

A bit-cell is used to store a single bit of data. A word line enables multiple words of memory. Column decoders are used to select the addressed memory word. Column

multiplexers connect the BL and BLB of the selected columns to the sense amplifiers to read the cell value. Write drivers are used to write into the memory cells. Row decoders decode the address given to the memory and activate the corresponding row of the memory array.

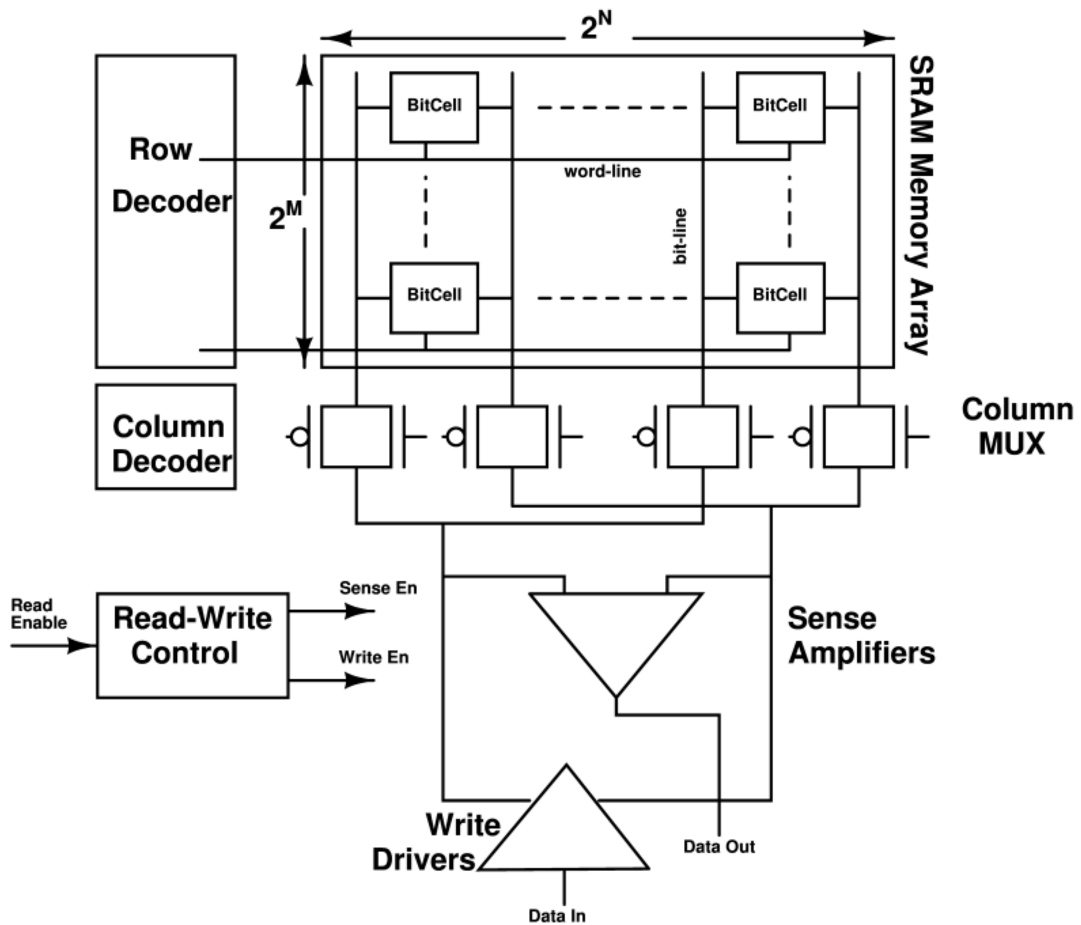

Figure 1.1: SRAM Architecture

CHAPTER 2

Literature Review

2.1 6T SRAM

The conventional 6T SRAM cell is shown in Fig. 2.1. It consists of two CMOS cross-coupled inverters, PU1-PD1 and PU2-PD2, which is responsible for storing a single bit of data. Where (PU1 and PU2) load transistors, driver transistors (PD1 and PD2), and two access transistors, PG1 and PG2, control access to the cross-coupled inverters for read and write operations.

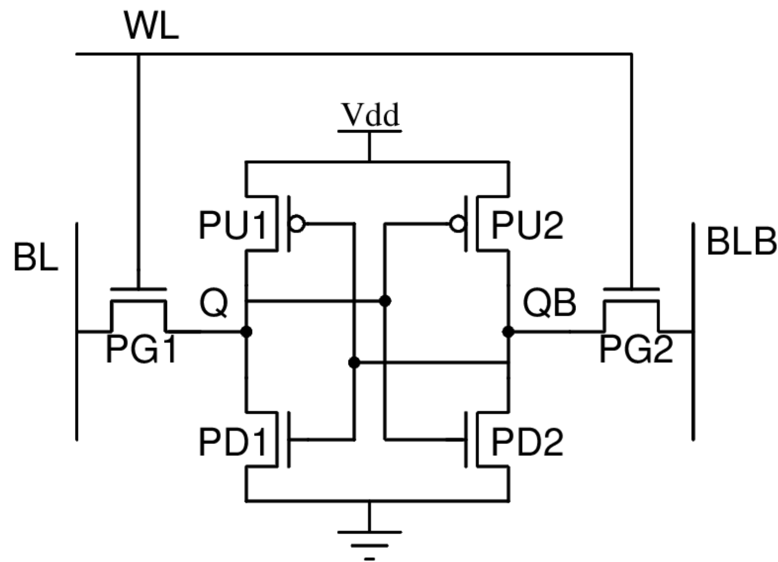

Figure 2.1: 6T SRAM

Read Operation As shown in Fig 2.2. The word line (WL) is activated to initiate a read operation by turning ON the access transistor and pre-charging the bit lines (BL and BLB). If ‘0’ is stored at Q then BL discharges through PG1 and PD1 then the bit lines act as outputs, and a sense amplifier detects voltage changes on BL or BLB to determine the stored data value at ‘Q’.

Write Operation As shown in Fig 2.2. A new data value is supplied on the bit lines (BL and BLB) for a write operation. The word line is activated, enabling PG1 and PG2, and the new data will be stored at ‘Q’ in the SRAM cell, depending on the bit line value.

During standby mode, the word lines are inactive, turning off PG1 and PG2, and the SRAM cell retains its stored data without any changes.

Sizing should be done according to the cell and pull-up ratios to ensure correct read and write operation and maintain high cell stability. Where the cell ratio (CR) and the pull-up ratio (PR) [18]-[19] are defined as

$$CR = \left(\frac{W(PD2)}{L(PD2)}\right) / \left(\frac{W(PG1)}{L(PG1)}\right)$$
$$PR = \left(\frac{W(PU1)}{L(PU1)}\right) / \left(\frac{W(PG1)}{L(PG1)}\right)$$

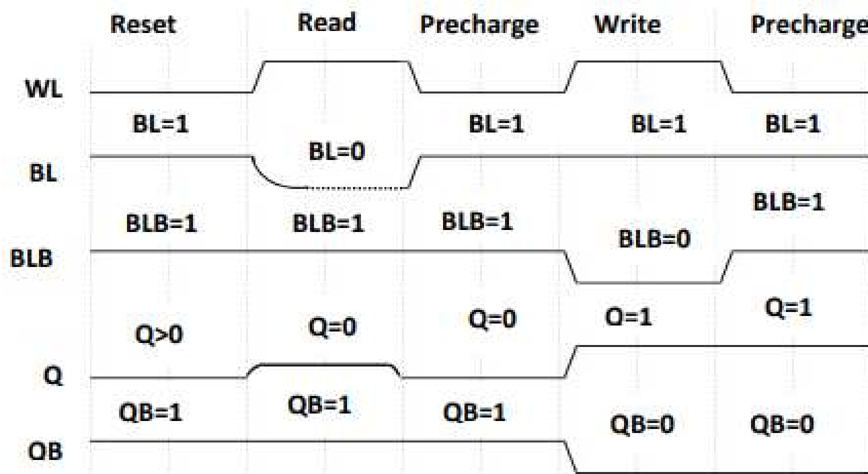

Figure 2.2: 6T SRAM waveform

Scaling of 6T SRAM is not possible because by reducing the size of 6T SRAM the stability and performance reduces so conventional 5T SRAM is proposed to further scaling of memories.

2.2 5T SRAM

The conventional 5T SRAM cell is shown in Fig. 2.4. It consists of two CMOS cross-coupled inverters, PU1-PD1 and PU2-PD2, which is responsible for storing a single bit of data. Where (PU1 and PU2) load transistors, driver transistors (PD1 and PD2), and one access transistor, PG1 control access to the cross-coupled inverters for read and write operations.

Read operation As shown in Fig 2.4. The word line (WL) is activated to initiate a read operation by turning ON the access transistor and pre-charging the bit lines BL.

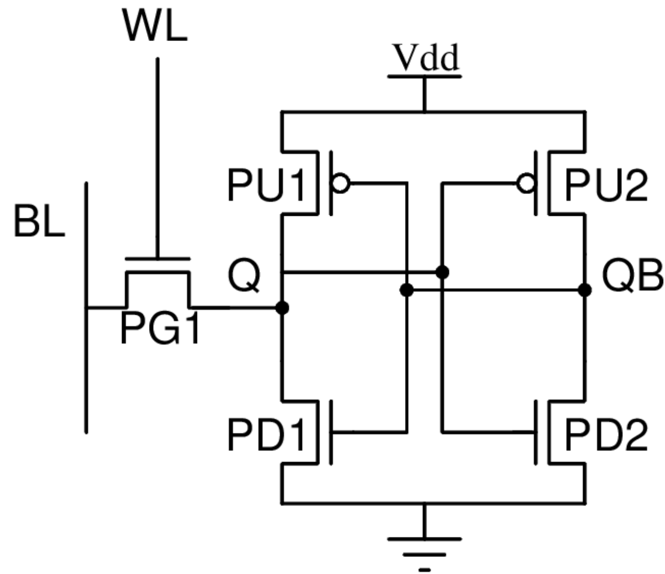

Figure 2.3: 5T SRAM

If ‘0’ is stored at Q then BL discharges through PG1 and PD1 then the bit lines act as outputs, and a sense amplifier detects voltage changes on BL or BLB to determine the stored data value at ‘Q’.

Write Operation As shown in Fig 2.4. During a write operation, a new data value is supplied on the bit line BL. The word line is activated, enabling PG1, and the new data will be stored at ‘Q’ in the SRAM cell, depending on the bit line value. However, writing ‘1’ is not possible in 5T SRAM because, in 5T, there is no PG2, so during writing ’1’ BL is set to VDD, the Q is initially at ’0’, and PD1 strength is more than PG1, and QB is at ’1’ so PD1 is always on so PD1 discharges the node Q to the ground and not allow the storing of ’1’, Write ’1’ is possible with a write assist scheme like boosting word line voltage or reducing the supply voltage VDD. However, as shown in Table 3.3, these techniques may result in reduced speed, increased memory area, and increased write time and overall power. In this work, we use VDD lowering of 0.6V and WL boosting of 0.3V to write ‘1’ in 5T SRAM at 130nm, and in 65nm a droop of 0.25V, and a WL boost of 0.2V is used.

For an iso-stable read operation, this cell is 3% denser than a 6T SRAM cell, and its leakage is about the same as 6T SRAM. For Iso-Area, the leakage is also the same as 6T, but in 5T, writing ’1’ is not possible without a write assist scheme. Then 4T SRAM is proposed for further scaling memories and solve 5T SRAM write problem

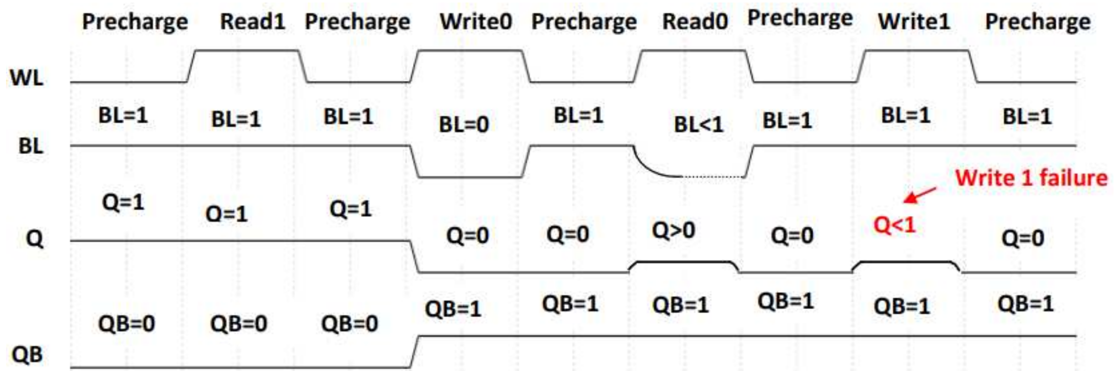

Figure 2.4: 5T SRAM waveform

2.3 4T SRAM

The conventional 4T SRAM cell is shown in Fig. 2.5. It consists of two CMOS cross-coupled NMOS, PD1, and PD2, which are responsible for storing a single bit of data. Where PD1 and PD2 are driver transistors, and two access transistors, PG1 and PG2, control access to the cross-coupled inverters for read and write operations.

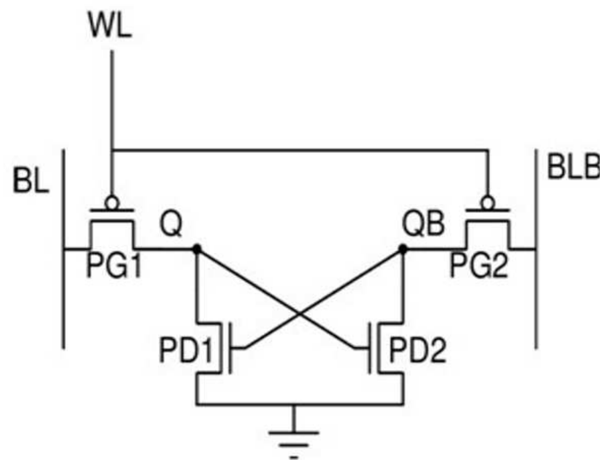

Figure 2.5: 4T SRAM

Read Operation As shown in Fig 2.6. The word line (WL) is activated to initiate a read operation by turning ON the access transistor and pre-charging the bit lines (BL and BLB). If ‘0’ is stored at Q then BL discharges through PG1 and PD1 then the bit lines act as outputs, and a sense amplifier detects voltage changes on BL or BLB to determine the stored data value at ‘Q’.

Write Operation As shown in Fig 2.6. A new data value is supplied on the bit lines (BL and BLB) for a write operation. The word line is activated, enabling PG1 and

PG2, and the new data will be stored at ‘Q’ in the SRAM cell, depending on the bit line values.

During standby mode, the word lines are inactive, turning off PG1 and PG2, and the SRAM cell retains its stored data without any changes.

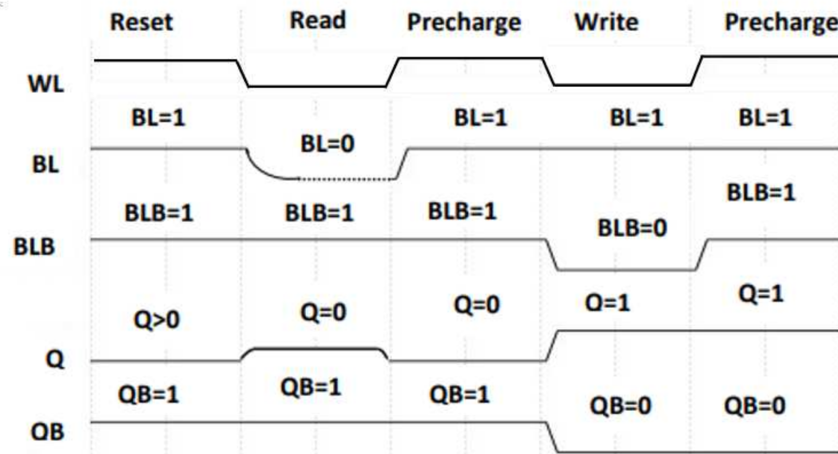

Figure 2.6: 4T SRAM Waveform

In a 130nm to maintain the iso stable read, the size of the driver transistors PD1 and PD2 must be larger than that of the 6T SRAM. As a result, there is up to an 11% increase in area and up to 2.5X increase in leakage compared to the 6T SRAM.

For the Iso area, 4T has a lower static read noise margin than 6T SRAM and up to 2.5X and 1.58X higher leakage compared to the 6T SRAM in 130nm and 65nm respectively. Therefore, there is a need for an efficient SRAM cell that has lower leakage without degradation of performance. Then researchers have proposed a range of Static Random-Access Memory (SRAM) cells to address various issues related to leakage, power, speed, and area.

2.4 Other Existing SRAM Cells

Some approaches, described in [3]-[7], use a more number of transistors per bit-cell and different threshold voltage (Vt) transistors to reduce leakage and improve performance However, this approach does not reduce area and faces challenges during fabrication because the transistor requires different diffusion type to change the threshold voltage, resulting in higher costs.

Another approach, as proposed in [8], utilizes an asymmetric inverter pair to create a cell with one write port with a single Bit Line (BL) and one read port with differential BL. The cell uses the complement of input data to perform the write operation, preventing the single write BL from discharging if the written value is '0'. Thus, the write '0' power is significantly less than the write '1' power. However, this approach requires an additional transistor per bit-cell, resulting in increased memory area.

In [9], another approach is proposed that uses one extra transistor per bit cell compared to a conventional 6T SRAM cell to reduce power and soft error. It reduces power consumption but increases the area.

In [10], the 5T SRAM cell is proposed by eliminating one access transistor from the conventional 6T SRAM cell. The proposed cell has reduced area and leakage, but writing '1' is only possible in 5T SRAM with a write assist scheme. Hence, the approach uses VDD lowering and a word line boosting scheme for writing '1'. However, this approach requires an additional power supply in the memory array, leading to increased memory cost and more complex circuitry in the memory cell to produce the supply.

In [11]-[12], another approach is proposed a 5T SRAM, the writing '1' done without any conventional write-assist mechanism. This approach utilizes additional circuitry per column to write '1' in the memory cell. However, the proposed circuitry contains many transistors, and the area penalty is more significant.

In [14]-[17], they use different voltage supplies for writing and reading in SRAM

Therefore, these proposed approaches have varying drawbacks. Thus, SRAM cells are needed that have lower leakage and higher density. We proposed two different SRAM cells that provide lower leakage, high density, and similar performance.

CHAPTER 3

Proposed Memory SRAM cells

3.1 Proposed 4TA SRAM Cell

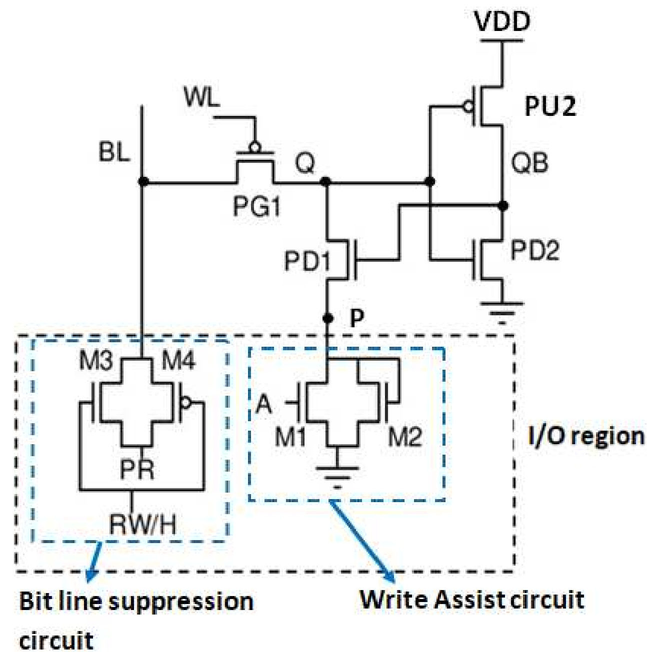

Figure 3.1: 4TA SRAM Cell

The proposed 4TA SRAM cell is shown in Fig. 3.1. It consists of PMOS access transistor PG1, NMOS driver transistors PD1 and PD2, and load transistor PU2. The bit line in the proposed cell is connected to a bit line suppression circuit, which is shared across the column and used to connect a BL to a signal PR by using M3 and M4 transistors, and an RW/H signal controls these transistors. The bit line suppression circuit helps in the reduction of the voltage of the bit line (VDD-V_{TM3}) in the standby mode to reduce the drain-source voltage V_{DSPG1} of transistor PG1, reduces leakage through access transistor PG1 when PG1 is OFF. Here, V_{TM3} is the threshold voltage of the transistor M3.

The write assist circuit is also shared across the column. It consists of a diode-connected transistor M2 parallel to an M1 NMOS transistor controlled by signal A. The write assist circuit sets the node P voltage to V_{GSM2} during a write '1' operation

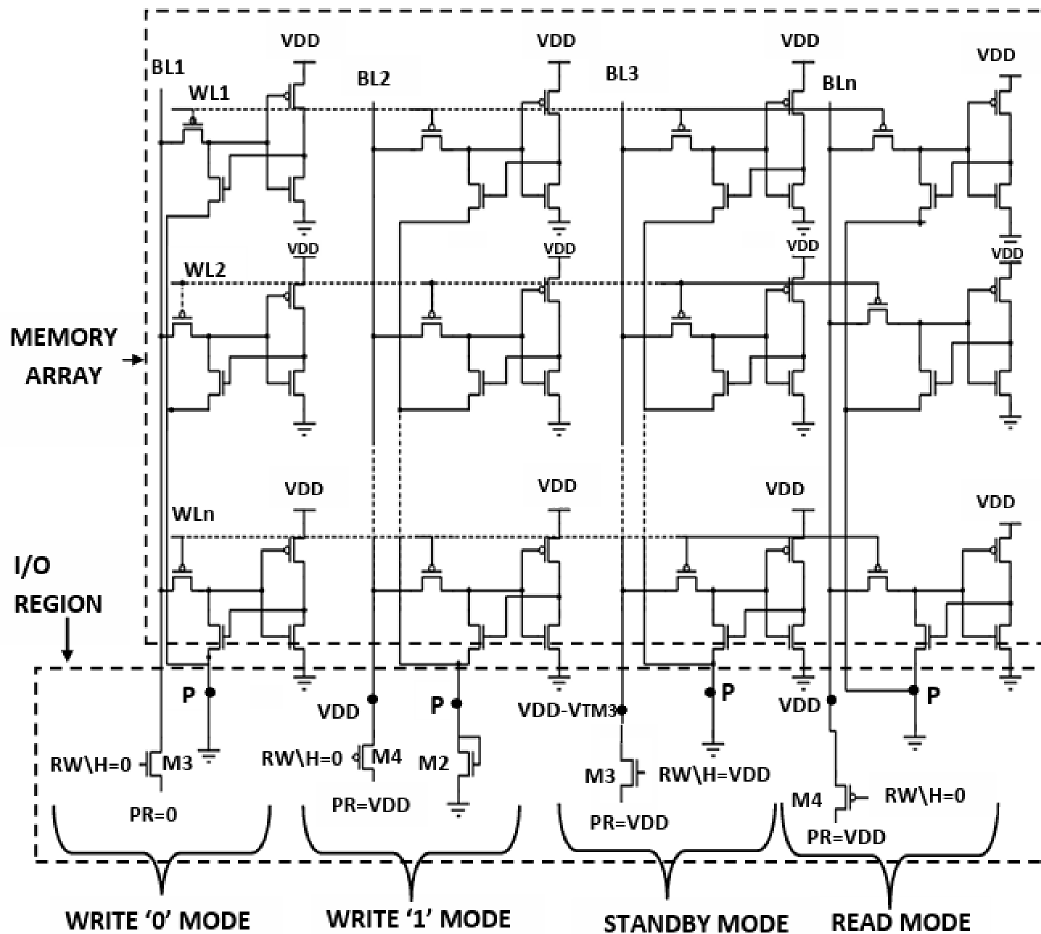

Figure 3.2: 4TA SRAM array with Assist circuitry in different modes of operation.

to reduce the drain-source voltage V_{DSPD1} of Driver transistor PD1. This reduces the strength of the Driver transistor PD1 and enables writing '1' through access transistor PG1 at node Q. Here, V_{GSM2} is the gate-source voltage of the transistor M2. During read, write'0', and standby mode, signal A is set to VDD, causing node P to be connected to the ground.

The voltage levels of the signals A, PR, RW/H, BL, and WL depend on the different modes of operation, as shown in Table 3.1.

3.1.1 Write operation

Write '1'- During the write '1' operation, as shown in Fig. 3.3, the signal A is set to logic low, which turns OFF the transistor M1. This causes node P to be connected to a diode-connected transistor M2, as shown in Fig.3.2. As a result, the node P voltage is set to V_{GSM2}, causing a reduction in the drain-source voltage V_{DS} of PD1, increases its resistance, thereby reducing its strength, enabling the writing of '1' through PG1. The

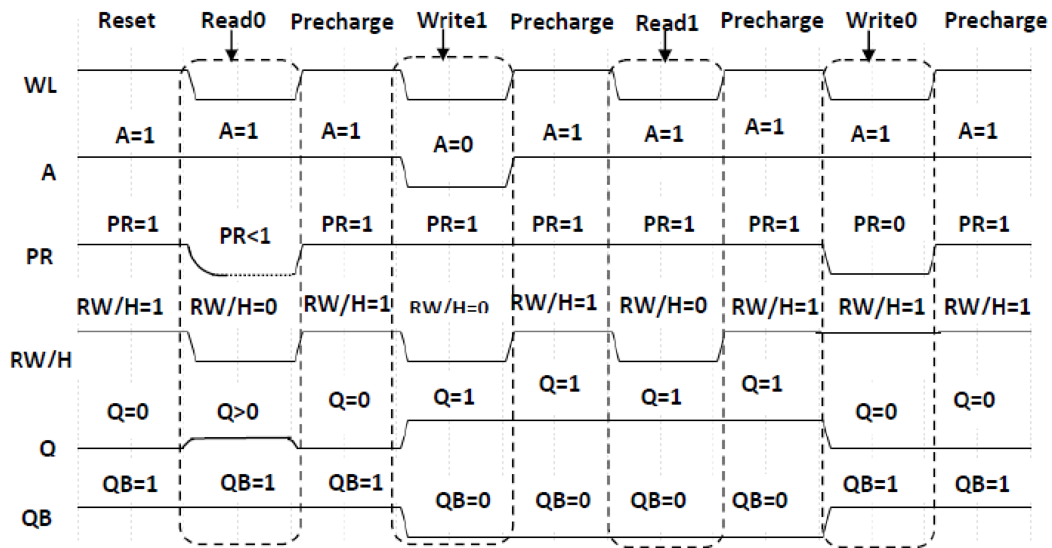

Figure 3.3: 4TA SRAM Read and Write Operation

Table 3.1: Voltage Level of Signals in 4TA SRAM Cell

Operation	A	PR	RW/H	BL	WL
Read	VDD	VDD	0V	VDD	0V
Write0	VDD	0V	VDD	0V	0V
Write1	0V	VDD	0V	VDD	0V
Hold	VDD	VDD	VDD	VDD-V_{TM3}	VDD

signal PR is set to logic high, and the signal RW/H is set to logic low, which causes the BL voltage to be at logic high. The word line (WL) is set to logic low, and transistor PG1 is turned ON.

Assuming that '1' is stored previously, the node Q voltage remains at logic high. However, if a logical '0' is stored previously, In this case, node Q will be charged to VDD through PG1.

Write '0'- During the write '0' operation, as shown in Fig. 3.2, the signal A is set to logic high, which turns on the transistor M1. As a result, the node P voltage is set to ground voltage, as shown in Fig.3.3. The signal PR is set to logic low, and the signal RW/H is set to logic high, which causes the BL voltage to be at ground voltage. The word line is set to logic low, and transistor PG1 is turned ON.

Assuming that '0' is stored at node Q previously, the node Q voltage remains at the ground voltage. However, if '1' is stored at node Q previously, Q will be discharged to ground voltage via PG1 and PD1.

3.1.2 Read operation

During the read operation, as shown in Fig. 3.2, the signal A is at logic high, which turns ON the transistor M1. As a result, the node P voltage is set to the ground voltage, as shown in Fig. 3.3. The signal PR is set to logic high, and the signal RW/H is set to logic low, which causes the BL voltage to be at logic high.

If '0' is stored at node Q. When the signal WL becomes logic low, transistor PG1 is turned ON, and BL discharges through PG1 and PD1. When '1' is stored at node Q, the voltage of BL remains at a high logic level, and the BL acts as an output. The sense amplifier detects voltage fluctuations on BL to determine the stored data value at Q, representing the SRAM cell data.

3.1.3 Standby Operation

During the standby operation, as shown in Fig. 3.3, the signal A is set to logic high, which turns ON the transistor M1. As a result, the node P voltage is set to the ground voltage. The signals PR and RW/H are set to logic high, which causes the voltage of BL to be at (VDD-V_{TM3}), as shown in Fig.3.2. Where V_{TM3} is the threshold voltage of transistor M3. This reduces the drain-source voltage of the access transistor, which helps reduce the bit line leakage through the access transistor when WL is logic high. However, the ON resistance of the transistors M1 and M2 reduces the strength of the driver transistor PD1, which, in turn, causes a reduction in standby efficiency.

During a write operation in a bit cell, the other cells in the same column are put into hold mode and share the write circuitry in write mode, causing the node P voltage to V_{GSM2}, which significantly reduces the strength of the driver transistor by decreasing the drain-source voltage of PD1. Therefore, if '0' is stored on node Q and any noise changes the voltage of node Q, PD1 may not be able to discharge node Q to the ground because node P is not at the ground voltage, reducing the standby efficiency of the standby cell in a column during write, which is presented in Table 3.3.

Table 3.2: Size of Transistors in 6T,5T,4T, and 4TA SRAM cells and Assist Circuitry

Transistors	6T	5T	4T	4TA
PG1(W/L)	0.60/0.15	0.60/0.15	0.60/0.15	0.60/0.15
PG2(W/L)	0.60/0.15	NA	0.60/0.15	NA
PD1(W/L)	0.90/0.15	0.90/0.15	1.60/0.15	1.40/0.15
PD2(W/L)	0.90/0.15	0.90/0.15	1.60/0.15	0.45/0.15
PU1(W/L)	0.45/0.15	0.45/0.15	NA	NA
PU2(W/L)	0.45/0.15	0.45/0.15	NA	0.45/0.15
M1,M2(W/L)	NA	NA	NA	2.00/0.15
M3,M4(W/L)	NA	NA	NA	1.00/0.15

Table 3.3: Comparison of FOMs For 6T,5T,4T, and 4TA SRAM Cells

FOMs	6T	5T	4T	4TA
Read SNM(µ/σ) FS/1.62V/125°C	30.81	30.81	30.80	30.81
Hold SNM (Q=‘0’)(µ/σ) FS/1.62V/125°C	55.25	55.25	28.29	59.53
Hold SNM (Q=‘1’)(µ/σ) FS/1.62V/125°C	55.25	55.25	28.29	28.09
HSNM of neighboring cells in column during write in a bit cell (µ/σ)	55.25	55.25	28.29	15.18
Write Margin (write ‘1’)(µ/σ) SF/1.62V/-40°C	50.89	17.31	10.40	17.57
Write Margin (write ‘0’)(µ/σ) SF/1.62V/-40°C	50.89	41.05	10.40	10.57
Write Time (nsec) SF/1.62V/-40°C	0.110	3.000	0.600	0.560
Cell Current (µA) SS/1.62V/125°C	135.0	135.0	67.30	66.50
BL discharge rate (mV/psec) SS/1.62V/125°C	8.05	8.05	3.00	2.500
Leakage (pA)(Q=‘0’) TT/1.8V/25°C	36.20	35.20	90.00	9.000
Leakage (pA)(Q=‘1’) TT/1.8V/25°C	36.20	33.10	90.00	33.40
Area (32X32 array)(um^2)	7004	6850	7794	6519

3.1.4 Result and Comparative Analysis

SRAM cells are benchmarked along various Figures of Merit (FOMs), such as Read Static Noise Margin (RSNM), Hold Static Noise Margin (HSNM), Write Margin, Leakage, Cell current, Write Time, Bit line discharge rate, and Area [18]-[19]. To benchmark the proposed 4TA SRAM, we designed the 32X32 SRAM array that can be configured as SRAM.

We characterized all the Figures of Merit (FOMs) of cells using 130 nm CMOS technology. We ran Monte Carlo simulations (1,000 samples) to estimate FOMs and computed all the FOMs on their Worst Process, Voltage, and Temperature (PVT). We ensure that all the FOMs are 6-sigma qualified to ensure good yield.

Area

The layout of a 4x4 array is a component of a 32X32 array of 6T SRAM, 5T SRAM, 4T SRAM, and 4TA SRAM cells in 130 nm CMOS technology with the iso-stable read size is shown in Figs. 3.4-3.7, respectively. TABLE 3.2 shows the device sizes for SRAM cells and assist circuitry. The layouts show the share diffusion regions, n-wells, polys, contacts, and vias in an SRAM architecture by flipping adjacent cells horizontally and vertically. Table II shows the total area of all SRAM cells. For a 32X32 SRAM array, the 4TA SRAM with assist circuitry has a 7% higher density than the 6T SRAM, 5% higher density than the 5T, and 16% higher density than the 4T SRAM.

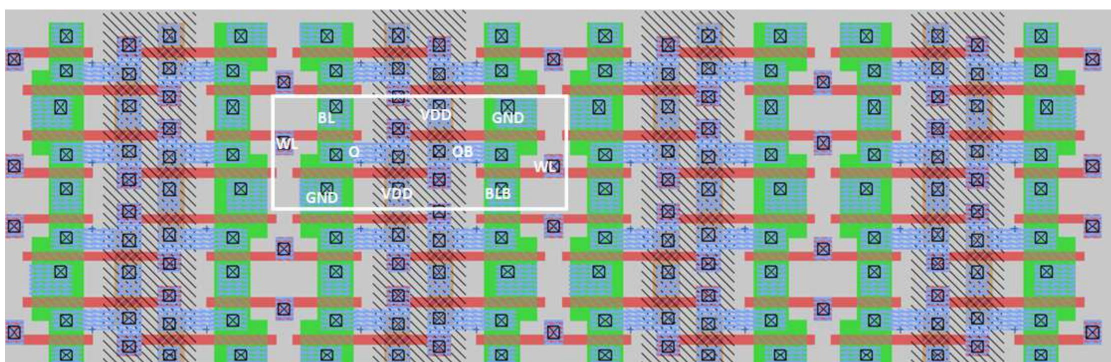

Figure 3.4: 4X4 6T SRAM Layout highlighting single cell (130nm)

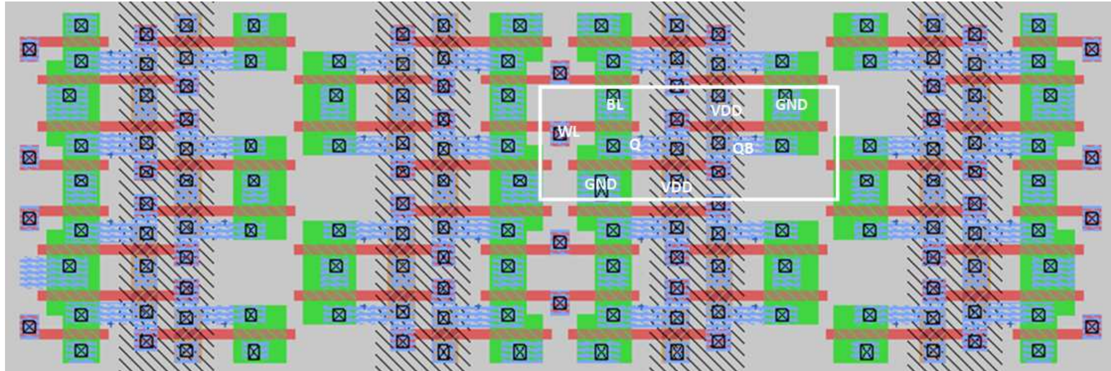

Figure 3.5: 4X4 5T SRAM Layout highlighting single cell (130nm)

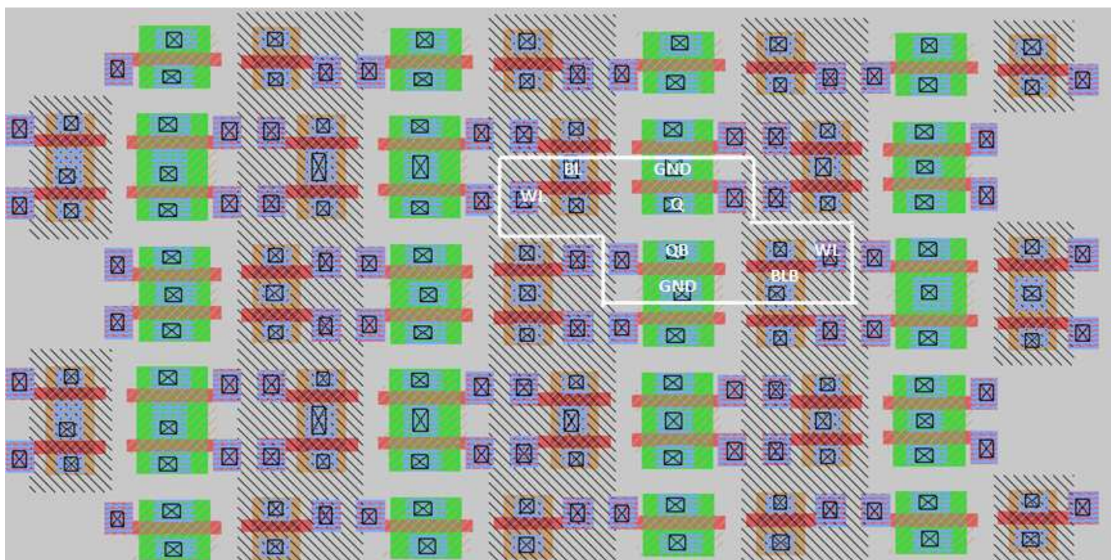

Figure 3.6: 4X4 4T SRAM Layout highlighting single cell (130nm)

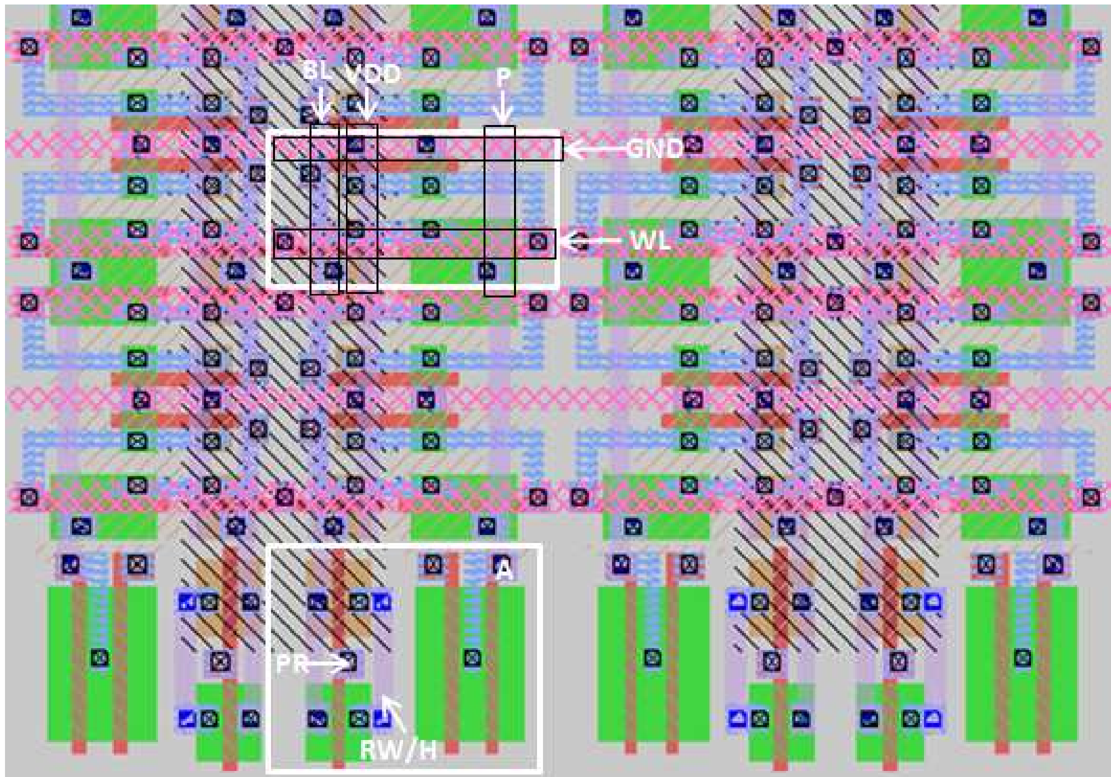

Figure 3.7: 4X4 4TA SRAM highlighting single cell and assist circuit (130nm)

Figures Of Merit

Static Noise Margin

SNM is a measure of cell stability and ensures that memory content is not corrupted during the memory operation. RSNM represents the maximum noise voltage that the cross-coupled nodes can endure without causing the cell's data to flip during a read operation. Since all the cells were designed for iso-stable read, all cells have the same RSNM,

HSNM is a measure of noise voltage that can be tolerated at the cross-coupled nodes without flipping the cell data during standby mode. The HSNM of 4TA also degraded because the 4TA does not have a load transistor (PU1) like 6T. If '1' is stored at node Q, then if the noise changes the voltage of node Q, there is no load transistor (PU1) in 4TA to support node Q voltage, thus degrading the HSNM. We observed that the HSNM of 4TA is degraded by 49% compared to 6T.

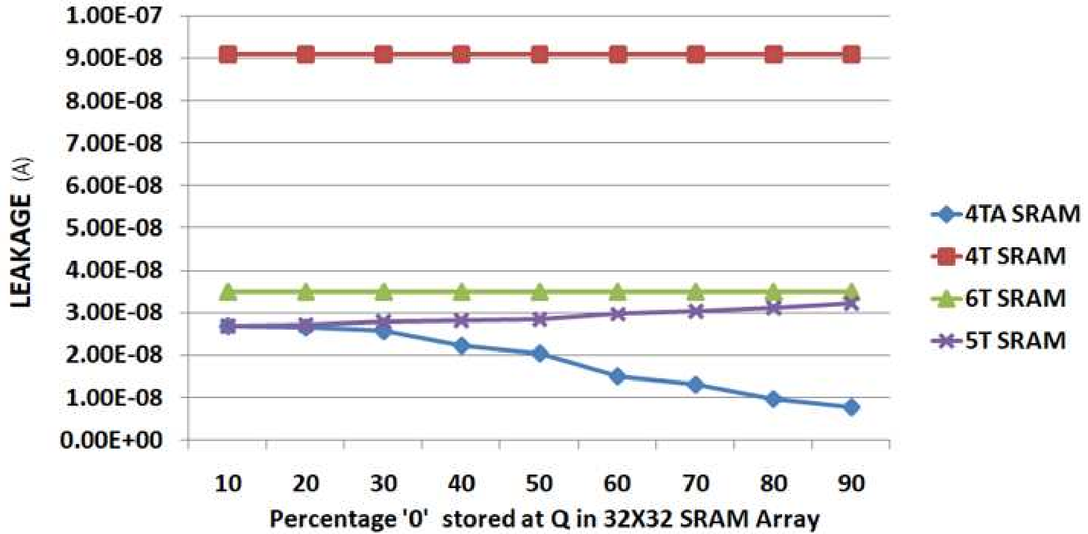

Figure 3.8: 32X32 4TA memory array leakage

Leakage

Leakage is the current that flows when the cell is in hold mode. In our analysis, we used battery life as the inverse of leakage. It is important to note that the leakage of the 4TA SRAM is data-dependent, as shown in Fig. 3.8. When '0' is stored at node Q, then access transistor PG1 leaks lower because the bit line suppression circuit reduces its drain-source voltage, and PD1 also leaks lower, but when '1' is stored at Q, then driver transistor PD1 leaks more because, it's size in 4TA SRAM cell is larger than that of 6T, which leads to more leakage but supply leakage is lower in 4TA SRAM cell than 6T due to fewer transistors. Therefore, When '0' is stored at node Q, the leakage is reduced up to 75%, 74%, and 90%, respectively, compared to conventional 6T, 5T, and 4T SRAM cells. However, when '1' is stored at node Q, the leakage in the 4TA SRAM cell is equivalent to that of the conventional 6T and 5T SRAM cell but 63% lower than the conventional 4T SRAM cell.

Write Margin

The write margin for the 4TA and 4T SRAM cells is defined as the the maximum voltage of WL at which new data can be written into the cell when bit-lines are precharged to VDD. For 6T and 5T SRAM cells, the write margin is defined as the minimum voltage of WL at which new data can be written into the cell when bit-lines are at 0V. In the 4TA SRAM cell, the process of writing '0' is done through the driver transistor PD1 as

the access transistor PG1 is PMOS and does not pass full zero. On the other hand, in 6T SRAM, both the access transistor and driver transistor are NMOS, which discharges the node Q to write ‘0’. This leads to a 79% degradation in the Write Margin for writing ‘0’ in the 4TA SRAM cell compared to the 6T SRAM. Write ‘1’ is done through BL via PG1 in the 4TA SRAM cell, while in the 6T SRAM, both PG1 and PU1 are used for writing ‘1’. This results in a 65% degradation in Write Margin for write ‘1’ in the 4TA SRAM cell compared to the 6T SRAM

Cell Current

Cell current is the current that flows through the read transistor during the read operation. To measure it, the BL is precharged to the VDD, while the WL is set to 0V. The current passing through the read transistor PG1 is then measured and presented as the read current. During the read operation in the 4TA SRAM cell, the ON resistance of the write assist circuit transistor M1 reduces the strength of the Pulldown Transistor (PD1), thereby reducing the cell current through the access transistor (PG1). As a result, the cell current of the 4TA SRAM cell is degraded by 2X compared to the 6T SRAM.

Performance

Performance is directly proportional to the BL discharge rate. The BL discharge rate is computed as the single-ended voltage creation rate on the BL during the read operation for 4TA. It is effectively the ratio of the BL discharge value to the time it takes to discharge the BL by that value. The BL capacitance is extracted for 32 rows to calculate the discharge rate. However, the 4TA SRAM cell’s performance is degraded by 3X compared to 6T. Hence, The proposed 4TA SRAM is a good fit for lower leakage and high-density applications but operates at lower frequencies.

Write Time

Write Time is the time to write a 0 and 1 in a bit cell. In 4TA SRAM, we found that the write time degrades due to the assist circuitry. In 4TA SRAM, the write slowed down to 6.62X and 1.03X compared to 6T and 4T SRAM, respectively, but improved to 3.83X

then 5T SRAM because in 5T SRAM, write is done by VDD lowering and word line boosting, which increases the write time for 5T SRAM.

Fig. 3.9 shows the benchmarking of the various FOMs in the form of a radar chart for all cells. The larger the footprint, the better the cell FOM.

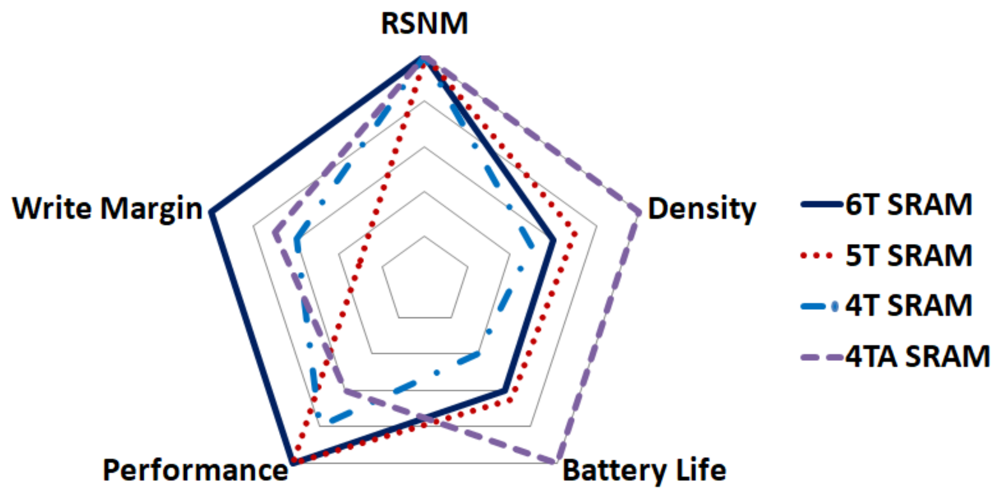

Figure 3.9: Comparision of 6T,5T,4T and 4TA SRAM cells across various FOMs

Hence the 4TA SRAM cell has 7%, 5%, and 16%, respectively, higher density than conventional 6T, 5T, and 4T SRAM cells. It has up to 75%, 74%, and 90%, respectively, lower leakage than the conventional 6T, 5T, and 4T SRAM cell for an iso-stable 32X32 memory array. but the performance of 4TA is degraded by 3X compared to 6T, so we move to another SRAM, which is a five-transistor SRAM known as 5TA.

3.2 Proposed 5TA SRAM Cell

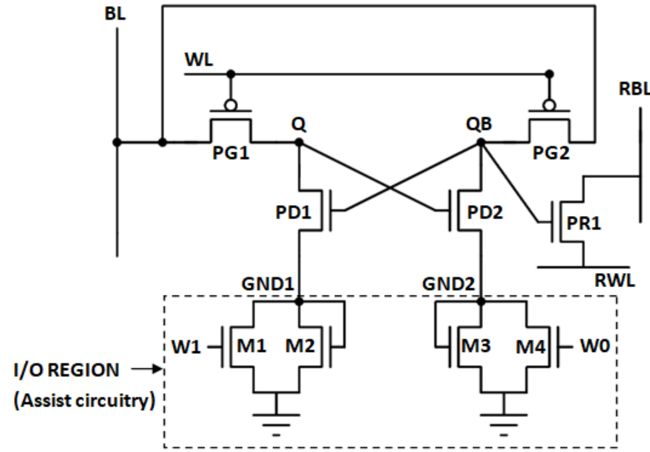

Figure 3.10: 5TA SRAM cell

The proposed 5TA SRAM cell is shown in Fig. 3.10. It consists of two PMOS access transistors, PG1 and PG2, two NMOS driver transistors, PD1 and PD2, and one read transistor, PR1. A write-assist circuit is shared across the column in memory and consists of four NMOS transistors, M1, M2, M3, and M3. The data bits are stored in the back-to-back NMOS pair, i.e., PD1 and PD2. The sources of PG1 and PG2 are coupled and connected to the BL (bit line), and both PG1 and PG2 are driven by the WL (word line). The read operation uses transistor PR1, which is controlled by the node QB. The drain of PR1 is connected to the RBL (Read bit line), and the source is connected to an RWL (Read word line) The PD1 source is connected to a diode-connected transistor M2 and M1 transistor controlled by signal W1, and the PD2 source is connected to a diode-connected transistor M3 and M4 transistor controlled by signal W0.

The voltage levels of the signals W0, W1, WL, BL, RBL, and RWL in different modes of SRAM operation, as shown in Table 3.3.

In this SRAM, data is maintained either through direct connection to the ground or through leakage current. When Q=1 and QB=0, the data at node Q is maintained through leakage current flow through PG1, and at node QB, data is maintained through direct connection to ground via PD2.

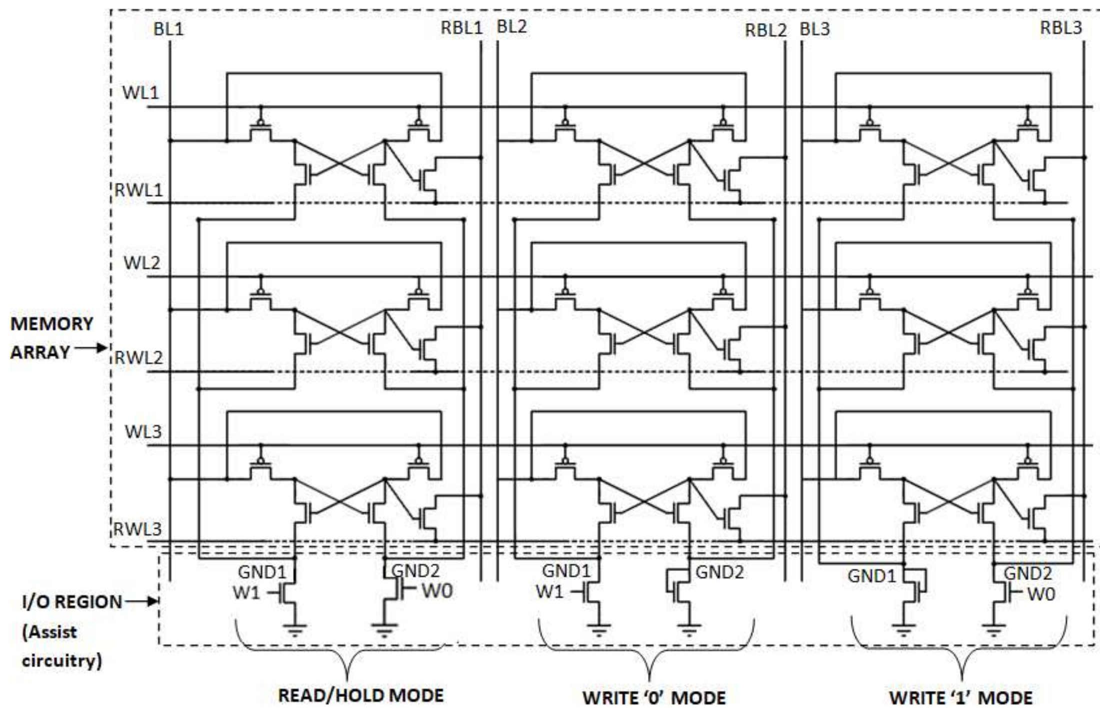

Figure 3.11: 5TA SRAM array with Assist circuitry in different modes of operation.

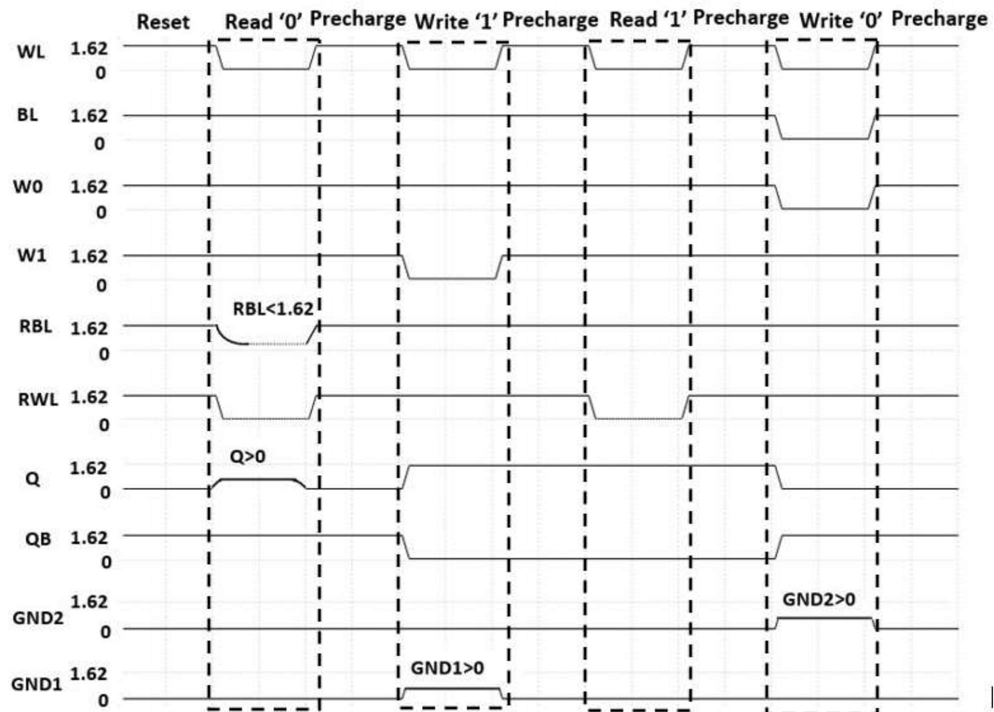

Figure 3.12: 5TA SRAM Read and Write Operation

3.2.1 Write operation

Write '1'- During the write '1' operation, as shown in Fig. 3.12, The WL is set to 0V, causing transistor PG1 to be turned ON. BL voltage is set to VDD. W0 is set to VDD, which turns ON M4, causing node GND2 to be connected to a 0V. The signal W1 is set to 0V, which turns OFF the transistor M1. This causes node GND1 to be connected to a diode-connected transistor M2, as shown in Fig. 3.11. As a result, the node GND1 voltage rises, causing a reduction in the drain-source voltage V_{DS} of PD1, increasing its resistance, and thereby reducing its strength, enabling the writing of '1' through PG1. If a '0' is stored at node Q previously, node Q will be charged to VDD through PG1.

Write '0'- During the write '0' operation, as shown in Fig. 3.12, The WL is set to 0V, causing transistor PG1 to be turned ON. BL voltage is set to VDD. W1 is set to VDD, which turns ON M1, causing node GND1 to be connected to a 0V. The signal W0 is set to 0V, which turns OFF the transistor M3. This causes node GND2 to be connected to a diode-connected transistor M3, as shown in Fig. 3.11. As a result, the node GND2 voltage rises, causing a reduction in the drain-source voltage V_{DS} of PD2, increasing its resistance, thereby reducing its strength, enabling the writing of '1' through PG2 at node QB. If '1' is stored at node Q previously, Q will be discharged to ground voltage via PG1 and PD1.

3.2.2 Read operation

The 5TA SRAM has decoupled read-through transistor PR1. During the read operation, the RWL is set to 0V, RBL is set to VDD, and Assist circuitry during the read operation is shown in Fig. 3.11. The signals W1 and W0 are at VDD, which turns ON the transistors M1 and M3. As a result, the node GND1 and GND2 voltages are set to the 0V. During the read operation, as shown in Fig. 3.12, If '1' is stored at node QB, then transistor PR1 is ON causing RBL discharges through PR1, If '1' is stored at QB then transistor PR1 is off, and RBL does not discharge. Then sense amplifier detects voltage changes on RBL to determine the stored data value at Q, representing the SRAM cell data.

Table 3.4: Voltage Level of signals in 5TA SRAM Cell

Operation	W0	W1	WL	BL	RBL	RWL
Read	VDD	VDD	VDD	VDD	VDD	0
Write0	VDD	0	0	VDD	VDD	VDD
Write1	0	VDD	0	VDD	VDD	VDD
Hold	VDD	VDD	VDD	VDD	VDD	VDD

Table 3.5: Size of Transistors in 6T,5T,4T, and 5TA SRAM cells and Assist Circuitry in 130nm

Transistors	6T	5T	4T	5TA
PG1(W/L)	0.60/0.15	0.60/0.15	0.6/0.15	0.45/0.18
PG2(W/L)	0.60/0.15	NA	0.60/0.15	0.45/0.18
PD1/PD2(W/L)	0.90/0.15	0.90/0.15	1.0/0.15	0.8/0.15
PU1/PU2(W/L)	0.45/0.15	0.45/0.15	NA	NA
PR1(W/L)	NA	NA	NA	0.7/0.15
M1,M2(W/L)	NA	NA	NA	20.00/0.15
M3,M4(W/L)	NA	NA	NA	20.00/0.15

3.2.3 Standby Operation

During the standby operation, as shown in Fig. 3.12, the signals W1 and W0 are at VDD, which turns ON the transistors M1 and M3. As a result, the node GND1 and GND2 voltages are set to the 0V. The BL is set to VDD, and WL is set to 0V, causing transistors PG1 and PG2 to be turned OFF. Assist circuitry during the standby operation is shown in Fig. 3.11.

3.2.4 Result and Comparative Analysis

SRAM cells are benchmarked along various Figures of Merit (FOMs), such as Read Static Noise Margin (RSNM), Hold Static Noise Margin (HSNM), Write Margin, Leakage, Cell current, Write Time, Bit line discharge rate, and Area [18]-[19]. To benchmark the proposed 5TA SRAM, we designed the 64X64 SRAM array that can be configured as SRAM.

We characterized all the Figures of Merit (FOMs) of cells using 130 nm and 65nm CMOS technology. We ran Monte Carlo simulations (1,000 samples) to estimate FOMs and computed all the FOMs on their Worst Process, Voltage, and Temperature (PVT). We ensure that all the FOMs are 6-sigma qualified to ensure good yield. TABLES 3.6 and 3.8 present the benchmark of 6T SRAM, 5T SRAM, 4T SRAM, and proposed 5TA

Table 3.6: Comparison of FOMs For 6T,5T,4T, and 5TA SRAM Cells in 130nm Technology

FOMs	6T	5T	4T	5TA
Read SNM (mV) FS/1.62V/125°C	430.6	435.6	270.3	-
Read SNM(μ/σ) FS/1.62V/125°C	35.81	36.51	17.08	-
Hold SNM (mV) FS/1.62V/125°C	631.8	635.9	463.6	470.0
Hold SNM (μ/σ) FS/1.62V/125°C	55.25	56.1	23.76	17.03
HSNM of cells in column during write in a bit cell (mV)	631.8	635.9	463.6	210
HSNM of cells in column during write in a bit cell (μ/σ)	55.25	56.1	23.76	8.033
HSNM of cells in row during write in a bit cell (mV)	430.6	435.6	270.6	270
HSNM of cells in row during write in a bit cell (μ/σ)	35.81	36.51	17.08	13.33
Write Margin (mV) SF/1.62V/-40°C	850.2	633.7	393.8	950.0
Write Margin (μ/σ) SF/1.62V/-40°C	50.89	17.31	10.40	37.55
Write Time (nsec) SS/1.62V/125°C	0.10	3.000	0.600	0.580
Cell Current (μA) SS/1.62V/125°C	135.0	135.0	67.30	181.2
RBL discharge rate (mV/psec) SS/1.62V/125°C	3.020	3.030	1.500	3.300
Leakage (pA) TT/1.8V/25°C	36.20	35.90	90.0	3.600
Area (64X64 array)(um^2)	28016	27996	27624	27924

Table 3.7: Size of Transistors in 6T,5T,4T, and 5TA SRAM cells and Assist Circuitry in 65nm

Transistors	6T	5T	4T	5TA
Device Used	PG,PD-NSVTLP PU-PSVTLP	PG,PD-NSVTLP PU-PSVTLP	PD-NSVTLP PG-PSVTLP	PD-NHVTLP PG-PSVTLP PR-NSVTLP
PG1/PG2(W/L)	0.18/0.06	0.18/0.06	0.25/0.06	0.28/0.07
PD1/PD2(W/L)	0.27/0.06	0.30/0.06	0.5/0.15	0.38/0.125
PU1/PU2(W/L)	0.135/0.06	0.135/0.06	NA	NA
PR1(W/L)	NA	NA	NA	0.19/0.06
M1,M2(W/L)	NA	NA	NA	5.00/0.06

Table 3.8: Comparison of FOMs For 6T,5T,4T, and 5TA SRAM Cells in 65nm Technology

FOMs	6T	5T	4T	5TA
Read SNM (mV) FS/1.08V/125°C	122.0	131.0	76.04	-
Read SNM(μ/σ) FS/1.08V/125°C	6.460	6.70	6.5	-
Hold SNM (mV) FS/1.08V/125°C	343.9	345.9	103.0	102.0
Hold SNM (μ/σ) FS/1.08V/125°C	26.28	27.8	6.52	6.150
HSNM of cells in column during write in a bit cell (mV)	343.9	345.9	103.0	101.0
HSNM of cells in column during write in a bit cell (μ/σ)	26.28	27.8	6.72	6.510
HSNM of cells in row during write in a bit cell (mV)	122.00	131.0	76.04	60.00
HSNM of cells in row during write in a bit cell (μ/σ)	6.460	6.7	6.5	3.000
Write Margin (mV) FS/1.08V/125°C	300.0	300	645.0	666.0
Write Margin (μ/σ) FS/1.08V/125°C	13.03	13.03	35.0	33.80
Write Time (psec) FS/1.08V/125°C	47.6	310	56	62.60
Cell Current (μA) FS/1.08V/125°C	3.630	3.64	3.35	3.630
RBL discharge rate (mV/psec) FS/1.08V/125°C	2.130	2.14	1.87	2.150
Leakage TT/1.08V/25°C (pA) FF/1.08V/125°C (nA)	78.50 11.96	78.5 11.95	20 3.36	12.60 1.970
Area (64X64 array)(um^2)	4885	4881	4997	4990

SRAM cells for different FOMs. The size of transistors used in SRAM cells is presented in TABLES 3.5 and 3.7.

Comparision Of Figures Of Merit

Leakage

Leakage is the current that flows when the cell is in hold mode. In a 5TA SRAM, the length of the access transistor is larger, and fewer transistors are used in 5TA, causing lower leakage. We found that 5TA SRAM has 10X lower leakage in 130nm and 6.28X lower leakage in 65nm than 6T SRAM. In our analysis, we used battery life as the inverse of leakage.

Cell Current

Cell current is the current that flows through the read transistor during the read operation. To measure it, the RBL is precharged to the VDD to measure the cell current, while the WBL is set to 0V. The current passing through the read transistor is then measured and presented as the read current. In a 5TA SRAM, the cell current depends on the size of the PR1 transistor. Sizing up the PR1 transistor increases read current. For 5TA SRAM, the cell current is improved by 1.34X at 130nm and 1.27X at 65nm as compared to the 6T SRAM

Performance

Performance is directly proportional to the RBL/BL discharge rate. The RBL/BL discharge rate is computed as the single-ended voltage creation rate on the RBL/BL during the read operation for 5TA. It is effectively the ratio of the RBL/BL discharge value to the time it takes to discharge the RBL/BL by that value. The RBL/BL capacitance is extracted for 64 rows to calculate the discharge rate. We found that the time to discharge the RBL is lower due to higher cell current, causing the performance to improve by 1.07X at 130nm and 1.01X at 65nm as compared to 6T SRAM

Static Noise Margin

RSNM is a measure of cell stability and ensures that memory content is not corrupted during the read operation. The proposed 5TA SRAM is a read-disturb-free SRAM because 5TA has a decoupled read. and its RSNM is the same as the HSNM, which is the maximum noise voltage that can be tolerated at the cross-coupled nodes during standby mode.

Upon comparing HSNM, it can be observed that the HSNM of the proposed 5TA SRAM is degraded by 69% and 74% at 130nm and 65nm, respectively, in terms of u/σ, when compared to 6T SRAM. The reason for this is that in 5TA, there is no PMOS load transistor to hold the value of '1' at node Q. Therefore, holding of '1' is carried out by leakage through the PMOS access transistor.

In a 5TA SRAM shown in Fig .2, during a write operation in a bit cell, the cells other than the write cell in the same column are in hold mode and share the write circuitry in write mode, this raises the node GND1 voltage, which reduces the strength of the driver transistor by decreasing the drain-source voltage of PD1. Therefore, if '0' is stored on node Q and any noise changes the voltage of node Q, PD1 may not be able to discharge node Q to the ground because node GND1 is not at the ground voltage, reducing the standby efficiency of the standby cell in a column during write.

Then cells shared in a row are also in hold mode their word line is ON and bitline is precharged to VDD then the bitline tries to charge both the Q and QB nodes through the access transistor hence this reduces the standby efficiency of the cell. We observe that the HSNM of cells in a column during write in a bit cell degrades by 85% and 75% at 130nm and 65nm, respectively as compared to 6TSRAM. The HSNM of cells in a row during write in a bit cell degraded by 60% and 38% at 130nm and 65nm, respectively as compared to 6TSRAM

Since at any given point of time few cells are in these modes, the memory operation continues to be in a statistically safe region operation.

Write Margin

The write margin for the 5TA is defined as the maximum voltage of WL at which new data can be written into the cell when bit-lines are precharged to VDD. In a 5TA SRAM, during the write ‘1’ operation, the source of the driver transistor PD1 is not at ground voltage, which prevents the driver transistor from discharging the internal not to ground, causing write ‘1’ can be done easily through access transistor but 5TA has higher sigma variation than 6T SRAM. In terms of u/σ, the write margin of the 5TA SRAM is degraded by 1.46X at 130nm and improved by 2.67X at 65nm as compared to the 6T SRAM.

Write Time

Write Time is the time to write a ‘0’ and ‘1’ in a bit cell. In 5TA SRAM, we found that the write time degrades due to the assist circuitry. In 5TA SRAM, the write slowed down to 5.8X at 130nm and 1.3X at 65nm as compared to 6T SRAM.

Area

The layout of a 4x4 array is a component of a 64X64 array of 6T SRAM, 5T SRAM, and 4T SRAM in 130 nm CMOS technology as shown in Figs. 3.4-3.6, respectively. and layout of 5TA SRAM cell in 130nm shown in Fig. 3.13. In the case of 6T,5T, and 5TA SRAM, each cell is flipped horizontally and vertically such that the adjacent cells can share the diffusion regions, n-wells, polys, contacts, and vias, but in the case of 4T SRAM layout is made in Z-locked topology, where the layout is mirrored vertically, but translated horizontally.

The layout of a 4x4 array of 6T SRAM, 5T SRAM, 4T SRAM, and 5TA SRAM in 65nm CMOS technology is shown in Figs. 3.14-3.17, respectively. Tables 3.5 and 3.7 show the device size used in 130nm and 65nm, respectively. The total area of all SRAM cells for a 64X64 SRAM array is shown in Tables 3.6 and 3.8. Fig. 3.18 shows the benchmarking of the various FOMs in the form of a radar chart for all cells. The larger the footprint, the better the cell.

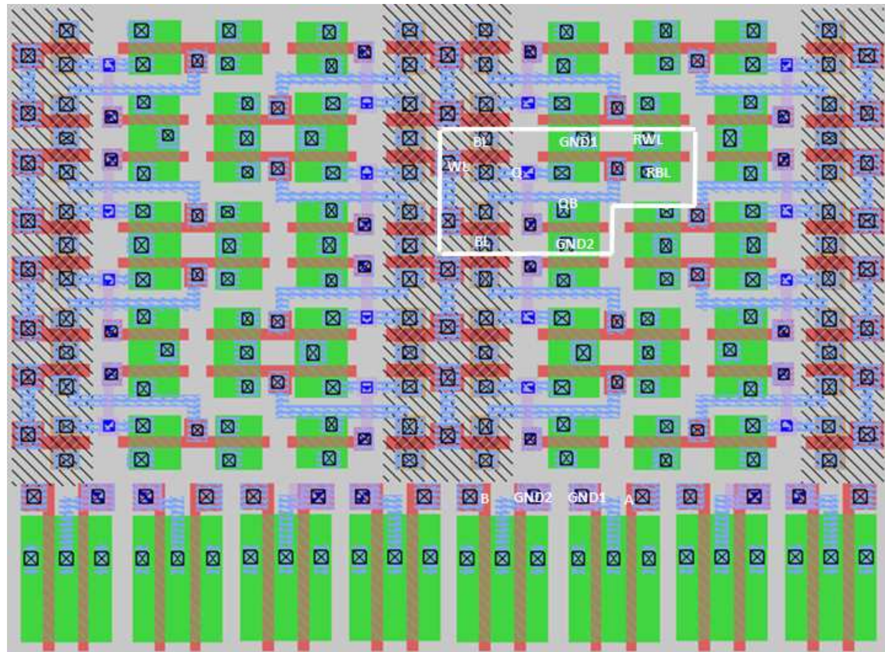

Figure 3.13: 4X4 Proposed 5TA SRAM highlighting single cell and assist circuit (130nm)

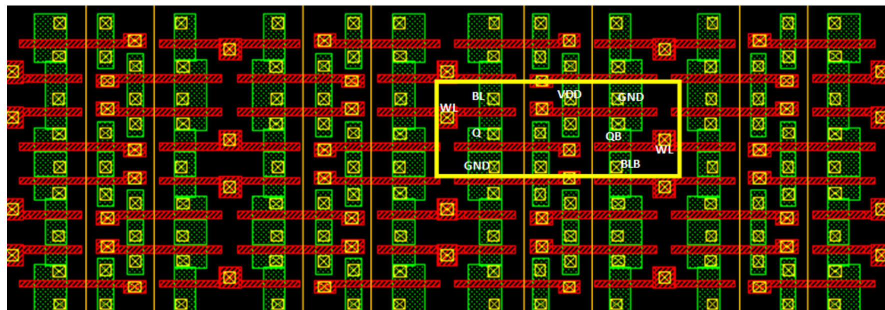

Figure 3.14: 4X4 6T SRAM highlighting single cell and assist circuit (65nm)

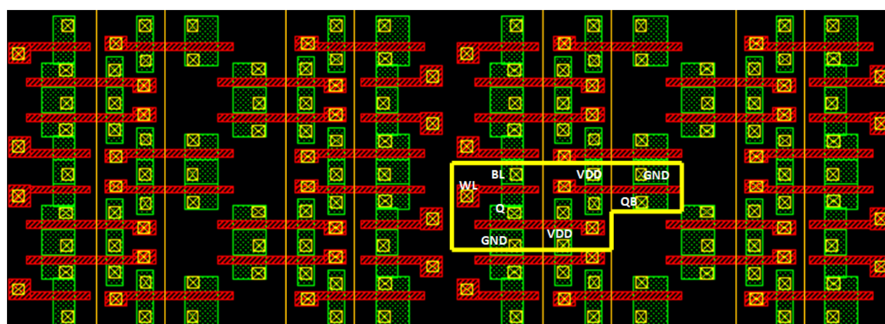

Figure 3.15: 4X4 5T SRAM highlighting single cell and assist circuit (65nm)

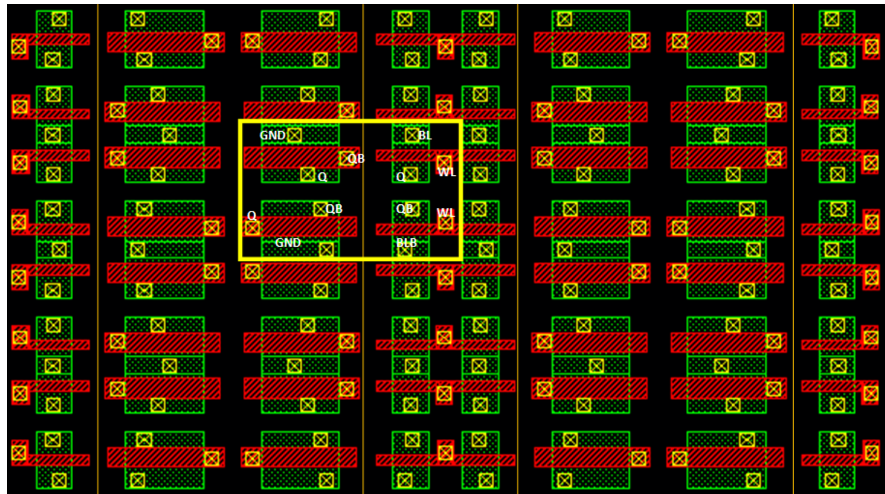

Figure 3.16: 4X4 4T SRAM highlighting single cell and assist circuit (65nm)

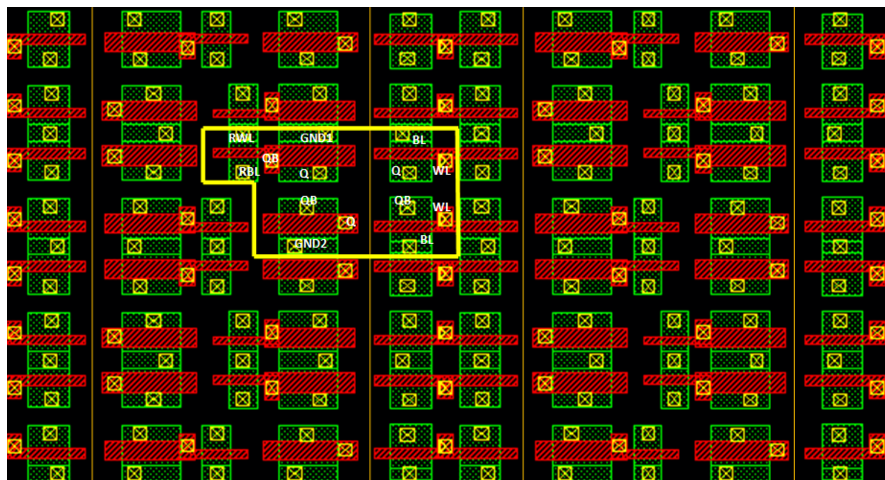

Figure 3.17: 4X4 Proposed 5TA SRAM highlighting single cell (65nm)

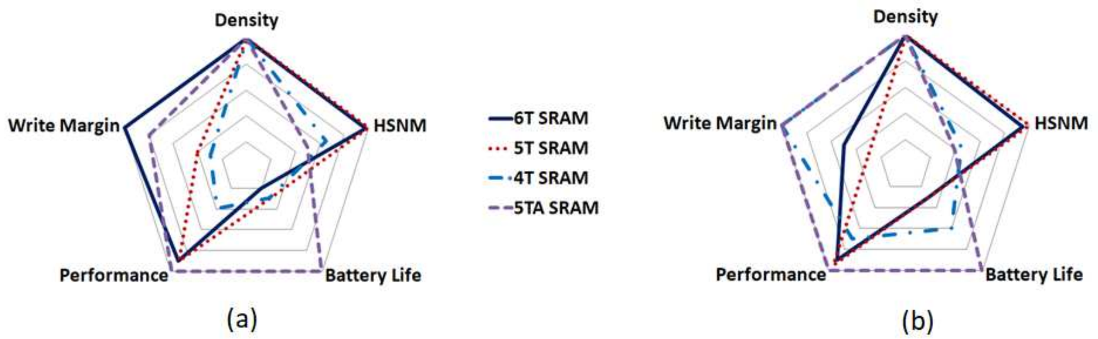

Figure 3.18: Comparision of 6T,5T,4T, and 5TA SRAM cells across various FOMs in (a)130nm (b)65nm

CHAPTER 4

Conclusion

In this work, we propose two asymmetric SRAM cell benchmarks with conventional 6T, 5T, and 4T SRAM cells. We show that the Iso-Stable read 4TA SRAM cell has a higher density of 7% compared 6T SRAM cell, respectively. Additionally, the 4TA SRAM cell has up to 4X lower leakage than conventional 6T, but the performance is lower in the 4TA SRAM cell as compared to the 6T SRAM cell. Then, we designed an Iso-Area 5TA SRAM cell in 130nm and 65nm CMOS technology. It has 10X lower leakage than the 6T SRAM cell in 130nm and 6.23X lower leakage than the 6T SRAM cell in 65nm technology. Furthermore, the 5TA SRAM cell exhibits higher cell current. Hence, our results indicate that the Proposed 4TA SRAM cell is preferred to design low leakage and denser memories. The proposed 5TA cell is the preferred choice for designing low-leakage and high-speed memories.

In reference to the thesis-

Our research paper, titled **”Design of High-Density Iso-Stable Asymmetric Memory Cell with Up to 10X Reduced Leakage”** has been accepted at ISCAS 2024, which will be presented on 22 May 2024 in Singapore

Our other paper, titled **” Design and Benchmark of Iso-Area 5T Asymmetric (5TA) SRAM Cell With Up to 10X Lower Leakage”** is currently under review in TCAS-II (ISICAS-2024).

We are in the process of filing patents for both the Proposed SRAM cells.

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