Accounting for the Correlation between Low-threshold and High-threshold Transistors using Analytical Techniques

BY

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CERTIFICATE

This is to certify that the thesis titled $Accounting\ for\ the\ Correlation\ between\ Low-threshold\ and\ High-threshold\ Transistors\ using\ Analytical\ Techniques$ submitted by Prashasti Pandey for the partial fulfillment of the requirements for the degree of Master of Technology in Electronics and Communication Engineering is a record of the bonafide work carried out by her under my guidance and supervision at Indraprastha Institute of Information Technology, Delhi. This work has not been submitted anywhere else for the reward of any other degree/ diploma.

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Abstract

With the scaling of semiconductor technology nodes, the impact of process-induced variations has increased. Statistical static timing analysis accounts for global and local variations in the timing analysis. The present methodology considers all the devices to have correlated variations at the global level. However, because of the difference in the fabrication steps of multi-threshold voltage transistors, their variations are not entirely correlated. Ignoring the varying correlations can lead to inaccuracies in the timing analysis. In this work, we have proposed an analytical method to compute variance in the currents and CMOS inverter delays as a function of device parameter variations and their correlations. Furthermore, we have compared the standard deviations obtained using the proposed analytical model and the experimental standard deviations obtained using Monte Carlo simulations. The results show that the error in the standard deviation of saturation currents obtained using the analytical model with respect to the experimental data is less than 1% and that in the inverter delay is less than 5%. Additionally, the results obtained using the proposed model with varying correlations between low and high-threshold transistors show the same trend as those obtained using Monte Carlo simulations. Hence, the proposed modeling technique could be employed in the future for timing analysis that statistically accounts for global variations among miscorrelated transistors.

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Chapter 1

Introduction

As the semiconductor design is scaling, the complexity of manufacturing processes is increasing. This makes the fabrication process more prone to fluctuations.

Process variations are induced for many reasons, such as variations in the chemical mechanical polishing stage and imperfections in the lens or the optical system. These generally lead to variations in the critical geometrical dimensions like oxide thickness, the transistor's width, and the transistor's length.

Process variations are divided into two broad categories: systematic and non-systematic. Systematic variations are due to well-known manufacturing fluctuations within technology and are handled during the layout stage. The non-systematic variations are random and are of significant concern. These occur due to optical proximity errors like line edge roughness (LER) and random dopant fluctuations (RDF).

The non-systematic process variations are further classified as global variations (inter-die) and local variations (intra-die). Global variations are the same throughout the lot/wafer and affect all devices similarly. In contrast, the local variations affect different devices of the same die differently.

Process variations directly affect the device parameters like oxide thickness, width and length dimensions, and other critical dimensions; this effectively changes the electrical parameters of the device, like the threshold voltage, gate capacitance, and saturation current. As the cell delay is a function of transistor current, it gets directly impacted by the global and local process variations.

1.1 Multi-threshold Transistor

The threshold voltage of a MOSFET is defined as the input gate voltage at which a significant amount of current starts to flow from the source to the drain.
Threshold voltage is controlled by controlling the doping in the substrate of a MOSFET. By using additional implants during MOSFET fabrication, we can obtain MOSFETs of various threshold voltages within a circuit or die. Generally, there are three types of transistors having different threshold voltages:

1. Low-threshold voltage transistors (LVT)
2. How-threshold voltage transistors (HVT)
3. Standard (Nominal) threshold voltage transistors (SVT).

Using different threshold voltage transistors empowers the designers to manage the flow of current and delays for different design paths in the same circuit.

1.2 Motivation

With the growing need for better performance and higher frequency of operation, multi-threshold voltage transistors have often been used in recent semiconductor designs to optimize timings. Static timing analysis (STA) tools are used to analyze the impact of various process variations in circuits having transistors of multi-threshold voltages (multi-V_t). Currently, STA tools take all the devices to the same corner to get the worst and the best timings [1]; however, the manufacturing steps of transistors having different threshold voltages are only partially correlated. The non-ideal correlation between multi-V_t transistors leads to the non-ideality in the correlation of currents and delays of the cells with different threshold voltage transistors. There-

fore, we need to incorporate the changes in the correlation between the delay of different threshold voltage transistors to make timing analysis more robust. This work is motivated to address this requirement.

1.3 Contribution

In this work, we have derived an analytical model to compute the standard deviation in the current and inverter delays as a function of device parameter variations. Further, we have extended the approach to incorporate the correlation between multi-V_t transistors into the analytical model. Additionally, we have carried out experiments to validate the proposed model. The results show that the proposed model can compute the variance in delays of multi-V_t transistors at various correlation coefficient values. The results shown in this work can be further used to carry out STA to assess the impact of correlation in a multi-V_t circuit.

1.4 Thesis Organization

This work is divided into five chapters: In Chapter 2 we have briefly discussed the existing literature relevant to this work. In Chapter 3, we have derived the analytical model for computing the standard deviation in saturation current and inverter delay. In Chapter 4, we have presented all the experimental values and the comparison between the data computed using the proposed analytical model and the data extracted by Monte Carlo simulations. In Chapter 5, we have derived the analytical model to include the correlation between multi-V_t transistors in the computation of variances in the saturation current and the inverter delay. The comparison between the experimental data and computed data is also presented in this chapter.

Chapter 2

Literature Survey

This chapter briefly reviews the existing literature relevant to this work. In [2], the authors have thoroughly explained the genesis of process variations and how the current and delays are impacted. They have also discussed the maximum delay approximation for points where multiple paths converge on a timing graph with various correlation factors ρ. They have also mentioned the complexity of non-normal distributions, which arises when the maximum operation is performed during SSTA on a timing graph. Several approaches like the numerical-integration method, Monte-Carlo simulations, probabilistic analysis, and path-based and block-based methods, were discussed through which SSTA is performed. The path-based approach deals with the correlation that arises between different paths due to geometrical proximity. The block-based approach deals with the spatial correlation problem, in which the gates in closer proximity are tightly correlated, whereas those a bit far away on the path are loosely correlated.

In [3], the authors have mentioned the drawbacks of path-based SSTA and introduced a novel statistical incremental timer which performs breadth-first traversal (path-based approach use depth-first traversal), which helps to overcome the drawbacks by enabling incremental processing and also by identifying the critical path based on their novel concept of tightness probability. The tightness probability measures the

probability of variations of a particular path for a particular process corner. It enables us to compute the maximum path delay value between different paths analytically with very little computation. The incremental timer propagates the sensitivities (delay with respect to variations in different device parameters) and also propagates the tightness probabilities. The authors have presented a time-efficient and memory-efficient method to implement path-based SSTA, but the idea of spacial correlation and how will it be integrated with this is missing.

In [4], the authors have presented an analytical approach to compute delay as a function of variations in different device parameters. They have presented a method to approximate the delay function using first-order Taylor series approximation about the nominal values of various device parameters. Also, they have discussed methods to compute the effects of both inter-die and intra-die variations, along with taking spatial correlation into account. The authors have also mentioned an approach to approximate interconnect delays. However, their approximation model is valid only for Gaussian random variations, thus leaving scope to incorporate non-Gaussian distributions, which generally arise while performing MAX operation on a timing path[2].

In [5], the authors have built over the contributions of [3], [4], [6] and have approximated the delay with respect to variations in various device parameters using Taylor series approximation where the degree of polynomial for individual parameters depends on the magnitude of variation and the desired level of accuracy. They also discussed a method to analytically perform MAX operation during timing graph traversal[7], for which they used regression modeling. They have also discussed that their regression model is applicable to any kind of variations and eliminates the need for random variations/delays to be Gaussian in nature, as in [4]. Though [5] provides a good level of accuracy along with incorporating both local and global variations

and also the spatial correlation, the impact of correlation between different threshold voltage transistors is omitted. This work is motivated to address this need.

In [8], the authors have put forward the necessity to take into account threshold voltage variation within the same die (intra-die V_t variation) as its impact on both the delay and leakage current is significant. The delay variation was shown to be highest when only a single input was toggled, whereas the smallest variability was shown when more input toggles were considered. Though this work takes into account single V_t transistors, it established that the intra-die V_t variations are of serious concern.

In work[9], the authors have discussed a simplified SSTA framework named Parametric On-Chip Variations (POCV). They have proposed a framework where each gate is modeled separately as a Gaussian distribution, and only a single POCV coefficient (mean/sigma) will be propagated along the timing graph.

All these works on statistical static timing analysis have successfully dealt with path-to-path correlation, spatial correlation, and both local and global variations using different methodologies. However, the impact of correlated variation amongst different V_t transistors is not incorporated in the existing literature. However, in recent times, most designs use multi-threshold voltage transistors. The commonality in the fabrication processes of multi-V_t transistors results in correlation in their device parameters. Hence, the delays and other timing attributes correlate between the cells implemented using multi-V_t transistors. In this work, the correlation in the timing attributes of the cells implemented using multi-V_t transistors is investigated in the following chapters.

Chapter 3

Analytical Model for Variations in Saturation Current and CMOS Invertor Delay

3.1 MOSFET Variation Model in Model File

The device model file for a given technology contains the SPICE model for different MOSFETs. It also defines parameter variations in devices for different conditions. Variations for each device are defined for Typical-Typical, Fast-Fast, Slow-Slow, Fast-Slow, and Slow-Fast corners. It also defines statistical variation to enable Monte-Carlo simulations/analysis.

The device parameter variations are defined in the SPICE model as linear equations of four random variables a_9, a_{10}, a_{11} and a_{12} as shown in the following equations:

$$t_{\text{ox}} = t_1 a_9 + t_2 a_{10} + t_3 a_{11} + t_4 a_{12} \tag{3.1}$$

$$dxw = w_1 a_9 + w_2 a_{10} + w_3 a_{11} + w_4 a_{12} \tag{3.2}$$

$$dvth0 = v_{\text{t1}} a_9 + v_{\text{t2}} a_{10} + v_{\text{t3}} a_{11} + v_{\text{t4}} a_{12} \tag{3.3}$$

$$du0 = u_1 a_9 + u_2 a_{10} + u_3 a_{11} + u_4 a_{12} \tag{3.4}$$

Here $t_{ox}, dxw, dvth0$ and $du0$ are oxide thickness,variation in width of the transistor,variation in threshold voltage of the transistor and variation in mobility of the

transistor, respectively. The coefficients of these linear equations are defined in the following tables:

	t_1	t_2	t_3	t_4
LVT NMOS	-1.60×10^{-13}	-1.08×10^{-11}	-2.55×10^{-13}	7.73×10^{-12}
LVT PMOS	-1.60×10^{-13}	-1.08×10^{-11}	-2.55×10^{-13}	7.73×10^{-12}
HVT NMOS	5.84×10^{-13}	-1.30×10^{-11}	3.04×10^{-13}	2.88×10^{-13}
HVT PMOS	-3.4×10^{-13}	-1.19×10^{-11}	-5.1×10^{-13}	5.77×10^{-12}

Table 3.1: Coefficients corresponding to t_{ox} variations.

	w_1	w_2	w_3	w_4
LVT NMOS	9.39×10^{-11}	3.00×10^{-9}	-7.30×10^{-10}	-2.80×10^{-10}
LVT PMOS	9.39×10^{-11}	3.00×10^{-9}	-7.30×10^{-10}	-2.80×10^{-10}
HVT NMOS	1.88×10^{-10}	2.70×10^{-9}	-9.50×10^{-10}	-2.30×10^{-10}
HVT PMOS	1.88×10^{-10}	2.70×10^{-9}	-9.50×10^{-10}	-2.30×10^{-10}

Table 3.2: Coefficients corresponding to width (dxw) variations.

	v_{t1}	v_{t2}	v_{t3}	v_{t4}
LVT NMOS	-5.90×10^{-3}	-5.05×10^{-3}	7.41×10^{-3}	3.60×10^{-3}
LVT PMOS	-4.73×10^{-3}	-54.07×10^{-3}	5.79×10^{-3}	2.88×10^{-3}
HVT NMOS	-7.31×10^{-3}	-6.09×10^{-3}	3.66×10^{-3}	5.76×10^{-3}
HVT PMOS	-4.41×10^{-3}	-4.66×10^{-3}	5.86×10^{-3}	3.05×10^{-3}

Table 3.3: Coefficients corresponding to threshold voltage V_t variations.

	u_1	u_2	u_3	u_4
LVT NMOS	4.80×10^{-5}	3.00×10^{-6}	-9.86×10^{-5}	2.80×10^{-17}
LVT PMOS	-1.50×10^{-4}	-4.70×10^{-4}	-4.66×10^{-6}	3.23×10^{-17}
HVT NMOS	-1.05×10^{-5}	-3.46×10^{-5}	-3.97×10^{-5}	$+1.26\times10^{-17}$
HVT PMOS	-2.70×10^{-5}	-3.72×10^{-5}	-4.41×10^{-5}	7.70×10^{-17}

Table 3.4: Coefficients corresponding to mobility (du0) variations.

The random variables a_9, a_{10}, a_{11} and a_{12} are defined in the model file as Gaussian random variables with mean '0' and standard deviation '1'.

3.2 Variations and their Dispersion

To compare which device parameter has more spread or more variation, a normalized statistical quantity is calculated, i.e. dispersion. In statistics it is denoted by CV, that is Coefficient of Variation

$$\text{CV} = \frac{\sigma}{\mu}$$

where σ represents standard deviation and μ represents mean. The CVs for all the relevant device parameters in the model file were computed and are shown in Tab. 3.5 and 3.6.

PARAMETER	MEAN μ	Standard Deviation σ	Dispersion (CV)
t_{ox}_n_lvt (nm)	2.41	1.295×10^{-2}	0.54%
dxw_n_lvt (nm)	120	3.0818	2.50%
dvth0_n_lvt (V)	0.24925	0.0114	4.50%
du0_n_lvt ($\frac{m^2}{Vs}$)	0.0152801	1.1106×10^{-4}	0.72%
t_{ox}_p_lvt (nm)	2.41	1.295×10^{-2}	0.54%
dxw_p_lvt (nm)	200	3.0818	1.54%
dvth0_p _lvt (V)	-0.202698	0.0090	4.44%
du0_p _lvt ($\frac{m^2}{Vs}$)	0.0230515	4.9266×10^{-04}	2.09%

Table 3.5: Dispersion of device parameters in low-Threshold Voltage MOSFET

PARAMETER	MEAN	SIGMA	DISPERSION
t_{ox}_n_hvt (nm)	2.41	1.2947	0.54%
dxw_n_hvt (nm)	120	2.0883	1.70%
dvth0_n_hvt (V)	0.42225	0.0117	2.70%
du0_n_hvt ($\frac{m^2}{Vs}$)	0.01528	5.3716×10^{-05}	0.35%
t_{ox}_p_hvt (nm)	2.41	1.2994×10^{-2}	0.54%
dxw_p_hvt (nm)	180	2.8659	1.59%
dvth0_p_hvt (V)	-0.368698	0.0093	2.52%
du0_p_hvt ($\frac{m^2}{Vs}$)	0.0230515	3.7065×10^{-04}	1.60%

Table 3.6: Dispersion of device parameters in high-Threshold Voltage MOSFET

As the dispersion of all the device parameters of of the transistors is less than 5%, Taylor Approximation can possibly be used to model the impact of their variation on saturation current and gate delay. In subsequent paragraphs, we have derived the analytical model to compute the variance in saturation current and variance in

inverter delay.

3.3 Taylor Approximation Model

Taylor approximation of a function $f(x)$ about a point $x = a$ is given as follows.

$$f(x) \approx f(a) + \frac{f^{'}(x)}{1!}(x-a) + \frac{f^{''}(x)}{2!}(x-a)^2.... \tag{3.5}$$

In case of multi-variable function, the partial derivatives are used in place of derivatives. The partial derivative is with respect to each variable multiplied with delta variation in that variable. In this work, variations in four parameters is taken into consideration, and the Taylor approximation based on four variables is:

$$f(x)+\Delta f \approx f(t_{\text{ox0}}, w_0, v_{\text{th0}}, u_0)+\frac{\partial f(x)}{\partial t_{\text{ox}}}\Delta t_{\text{ox}}+\frac{\partial f(x)}{\partial w}\Delta w+\frac{\partial f(x)}{\partial v_{\text{th}}}\Delta v_{\text{th}}+\frac{\partial f(x)}{\partial u}\Delta u \tag{3.6}$$

Here, the $f(t_{\text{ox0}}, w_0, v_{\text{th0}}, u_0)$ signifies value of function $f(x)$ at the nominal values of device parameters. Partial derivatives signify the sensitivities of the function $f(x)$ with respect to individual variables (device parameters).

3.4 Variance in Drain Saturation Current $I_{\mathbf{d}}$

Using Taylor Approximation, I_d can be approximated as:

$$I_\text{d} + \Delta I_\text{d} \approx I_{\text{d}_{(t_{\text{ox0}}, w_0, v_{\text{th0}}, u_0)}} + \frac{\partial I_\text{d}}{\partial t_{\text{ox}}}\Delta t_{\text{ox}} + \frac{\partial I_\text{d}}{\partial w}\Delta w + \frac{\partial I_\text{d}}{\partial v_{\text{th}}}\Delta v_{\text{th}} + \frac{\partial I_\text{d}}{\partial u}\Delta u \tag{3.7}$$

Since the partial derivatives indicate respective sensitivities, it can be written as:

$$\frac{\partial I_\text{d}}{\partial t_{\text{ox}}} = c_1 \tag{3.8}$$

$$\frac{\partial I_\text{d}}{\partial w} = c_2 \tag{3.9}$$

$$\frac{\partial I_{\mathrm{d}}}{\partial v_{\mathrm{th}}} = c_3 \tag{3.10}$$

$$\frac{\partial I_{\mathrm{d}}}{\partial u} = c_4 \tag{3.11}$$

Using sensitivities c_1, c_2, c_3 and c_4 Saturation current I_{d} can be written as:

$$I_{\mathrm{d}} + \Delta I_{\mathrm{d}} \approx I_{\mathrm{d}_{(\mathrm{t_{ox0}},\mathrm{w_0},\mathrm{v_{th0}},\mathrm{u_0})}} + c_1\Delta t_{\mathrm{ox}} + c_2\Delta w + c_3\Delta v_{\mathrm{th}} + c_4\Delta u \tag{3.12}$$

The variance of $\mathrm{I_d}$ can be computed as:

$$Var(I_d) = Var(I_{\mathrm{d}} + \Delta I_{\mathrm{d}}) \approx Var(I_{\mathrm{d}_{(\mathrm{t_{ox0}},\mathrm{w_0},\mathrm{v_{th0}},\mathrm{u_0})}} + c_1\Delta t_{\mathrm{ox}} + c_2\Delta w + c_3\Delta v_{\mathrm{th}} + c_4\Delta u) \tag{3.13}$$

$$\begin{aligned} Var(I_{\mathrm{d}}) \approx\ & Var(c_1\Delta t_{\mathrm{ox}}) + Var(c_2\Delta w) + Var(c_3\Delta v_{\mathrm{th}}) + Var(c_4\Delta u) + 2[Cov(c_1\Delta t_{\mathrm{ox}}, c_2\Delta w) \\ & + Cov(c_1\Delta t_{\mathrm{ox}}, c_3\Delta v_{\mathrm{th}}) + Cov(c_1\Delta t_{\mathrm{ox}}, c_4\Delta u) + Cov(c_2\Delta w, c_3\Delta v_{\mathrm{th}}) + Cov(c_2\Delta w, c_4\Delta u) \\ & + Cov(c_3\Delta v_{\mathrm{th}}, c_4\Delta u)] \end{aligned} \tag{3.14}$$

We have used the following property of the sum of random variables to obtain the above equation:

$$Var(X_1 + X_2 + X_3 + ... + X_{\mathrm{n}}) = \sum_{i=1}^{n} Var(X_{\mathrm{i}}) + 2\sum_{i=1}^{n}\sum_{j=i+1}^{n} Cov(X_{\mathrm{i}}X_{\mathrm{j}})$$

Further, we can write:

$$\begin{aligned} Var(I_{\mathrm{d}}) \approx & {c_1}^2 Var(t_{\mathrm{ox}}) + {c_2}^2 Var(w) + {c_3}^2 Var(v_{\mathrm{th}}) + \\ & {c_4}^2 Var(u) + 2(c_1c_2Cov(t_{\mathrm{ox}}, w) + c_1c_3Cov(t_{\mathrm{ox}}, v_{\mathrm{th}}) + c_1c_4Cov(t_{\mathrm{ox}}, u) + c_2c_3Cov(w, v_{\mathrm{th}}) \\ & + c_2c_4Cov(w, u) + c_3c_4Cov(v_{\mathrm{th}}, u)) \end{aligned} \tag{3.15}$$

Using the following equation to expand the variance and co-variance terms:

$$Var(aX + b) = a^2 Var(X)$$

$$Cov(aX + b, cY + d) = acCov(X, Y)$$

To analytically derive the covariance between different device parameters, we can write the variation equation 3.1-3.4 in terms of random vectors and the following matrix equation:

$$Y = AX$$

where, A is the coefficient matrix of $t_{\mathrm{n}}, w_{\mathrm{n}}, v_{\mathrm{n}}$ and u_{n} and X is the random variable matrix of a_9, a_{10}, a_{11} and a_{12}.

The random variables a_9, a_{10}, a_{11} and a_{12} are independent Gaussian random variables with standard deviation '1' and mean '0', their Variance becomes '1' and covariance with other random variables '0'. Hence, we can write the the covariance matrix of random variables a_9, a_{10}, a_{11} and a_{12} as follows:

$$C_{\mathrm{X}} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.16}$$

Thus the covariance matrix of device parameters C_{Y} can be written as:

$$C_{\mathrm{Y}} = \begin{bmatrix} t_1 & t_2 & t_3 & t_4 \\ w_1 & w_2 & w_3 & w_4 \\ v_{\mathrm{th}1} & v_{\mathrm{th}2} & v_{\mathrm{th}3} & v_{\mathrm{th}4} \\ u_1 & u_2 & u_3 & u_4 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} t_1 & w_1 & v_{\mathrm{th}1} & u_1 \\ t_2 & w_2 & v_{\mathrm{th}2} & u_2 \\ t_3 & w_3 & v_{\mathrm{th}3} & u_3 \\ t_4 & w_4 & v_{\mathrm{th}4} & u_4 \end{bmatrix} \tag{3.17}$$

To derive the above equation, we have used the following relationship of covariance matrices C_Y and C_X of two linearly related random vectors $Y = AX$:

$$C_{\mathrm{Y}} = AC_{\mathrm{x}}A^T$$

3.5 Variance in Gate Delay

Variations in delay can be modeled similarly to the variance model of saturation current I_{d}. The device parameters and their variation model are the same for both saturation current I_{d} and the gate delay. Hence, the covariance matrix for device parameter random vectors will be the same for both cases.

Delay can be linearly approximated using Taylor Approximation as follows:

$$D + \Delta D = D_{(\mathrm{t_{ox0}},\mathrm{w_0},\mathrm{v_{th0}},\mathrm{u_0})} + \frac{\partial D}{\partial t_{\mathrm{ox}}}\Delta t_{\mathrm{ox}} + \frac{\partial D}{\partial w}\Delta w + \frac{\partial D}{\partial v_{\mathrm{th}}}\Delta v_{\mathrm{th}} + \frac{\partial D}{\partial u}\Delta u$$

where, $D_{(\mathrm{t_{ox0}},\mathrm{w_0},\mathrm{v_{th0}},\mathrm{u_0})}$ is value of delay when all the device parameters are at their nominal value.

The variance of delay can be written as:

$$\begin{aligned} Var(D) = {c_1}^2 Var(t_{\mathrm{ox}}) + {c_2}^2 Var(w) + {c_3}^2 Var(v_{\mathrm{th}}) + {c_4}^2 Var(u) + 2[c_1 c_2 Cov(t_{\mathrm{ox}}, w) \\ + c_1 c_3 Cov(t_{\mathrm{ox}}, v_{\mathrm{th}}) + c_1 c_4 Cov(t_{\mathrm{ox}}, u) + c_2 c_3 Cov(w, v_{\mathrm{th}}) \\ + c_2 c_4 Cov(w, u) + c_3 c_4 Cov(v_{\mathrm{th}}, u)] \end{aligned} \tag{3.18}$$

Further, the Covariance matrix is calculated as:

$$C_{\mathrm{Y}} = \begin{bmatrix} t_1 & t_2 & t_3 & t_4 \\ w_1 & w_2 & w_3 & w_4 \\ v_{\mathrm{th1}} & v_{\mathrm{th2}} & v_{\mathrm{th3}} & v_{\mathrm{th4}} \\ u_1 & u_2 & u_3 & u_4 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} t_1 & w_1 & v_{\mathrm{th1}} & u_1 \\ t_2 & w_2 & v_{\mathrm{th2}} & u_2 \\ t_3 & w_3 & v_{\mathrm{th3}} & u_3 \\ t_4 & w_4 & v_{\mathrm{th4}} & u_4 \end{bmatrix} \tag{3.19}$$

and the sensitivity coefficient c_1, c_2, c_3 and c_4 are calculated experimentally.

Chapter 4

Experimental Validation of Proposed Analytical Model

4.1 Experimental Setup

In this work, we have used a 45nm technology model file[10]. We have conducted all the simulations using Cadence virtuoso[11] and Cadence ADE-XL[12] to perform Monte Carlo simulations. We have done Monte Carlo simulations with 5000 sample runs to derive the mean and standard deviations of saturation currents and the delays.

4.1.1 Experimental setup for Saturation Current $I_{\mathbf{d}}$

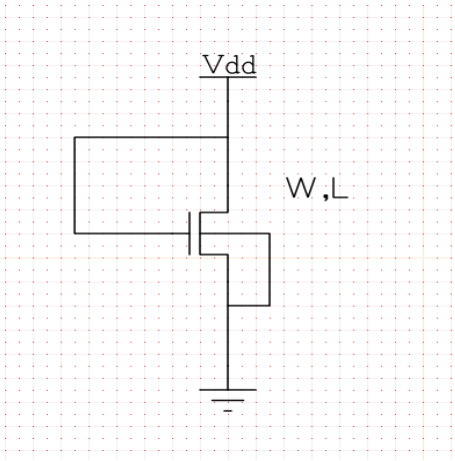

Figure 4.1: Circuit used for Saturation Current simulations

We have taken all four types of transistors in saturation mode, as shown above. The nominal values of different device parameters for all four types of transistors considered are shown in Tab 4.1.

	t_{ox0} (nm)	w_0 (nm)	v_{t0} (V)	u_0 (m^2/Vs)
LVT NMOS	2.41	120	0.24925	0.0152801
LVT PMOS	2.41	200	-0.202698	0.0230515
HVT NMOS	2.40	120	0.42225	0.0152801
HVT PMOS	2.40	180	-0.368698	0.0230515

Table 4.1: Nominal values of device parameters

4.2 Experimental setup for Delay Simulations

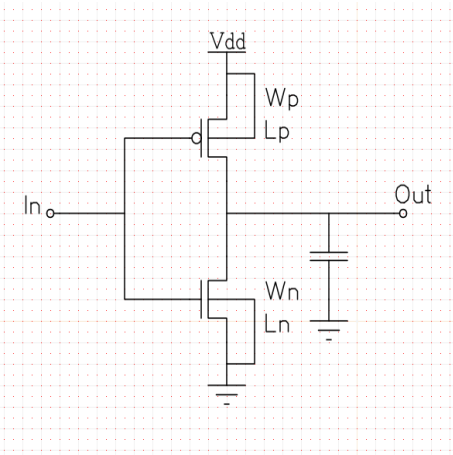

Figure 4.2: Circuit used for Delay simulations

Delays were extracted using circuit shown in Fig 4.2. The device parameters and simulation setup values are shown in Tab. 4.2.

	w_n(nm)	w_p (nm)	Input Slew(ps)	C_L (fF)
LVT INVERTER	520	780	20	2.82
HVT INVERTER	520	780	20	2.23

Table 4.2: Simulation setup values of Inverter Delay

4.3 Sensitivity Extraction

As described in the previous chapter, the variance of both saturation current and delay can be computed using:

1. Variance of device parameters.
2. Covariance amongst device parameters.
3. Sensitivity with respect to different device parameters.

We define the sensitivity parameter S_Y^X as the sensitivity of parameter X with respect to Y as follows:

$$S_Y^X = \frac{\Delta X}{\Delta Y} \tag{4.1}$$

The sensitivity for parameter X with respect to Y is computed as:

$$S_Y^X = \frac{X_{+5\%} - X_{-5\%}}{Y_{+5\%} - Y_{-5\%}}$$

where, $Y_{+5\%}(Y_{-5\%})$ is the value of parameter Y with +5%(-5%) variation,and $X_{+5\%}(X_{-5\%})$ is the value of X when parameter Y is at +5% (-5%)variation value. The sensitivity of each device parameter was extracted experimentally. All the samples were plotted and were found to be approximately linear in the $\pm 5\%$ variation range.

4.3.1 Sensitivity with respect to oxide thickness t_{ox}

The variation in the saturation current with respect to the threshold voltage is shown in the Fig 4.3.

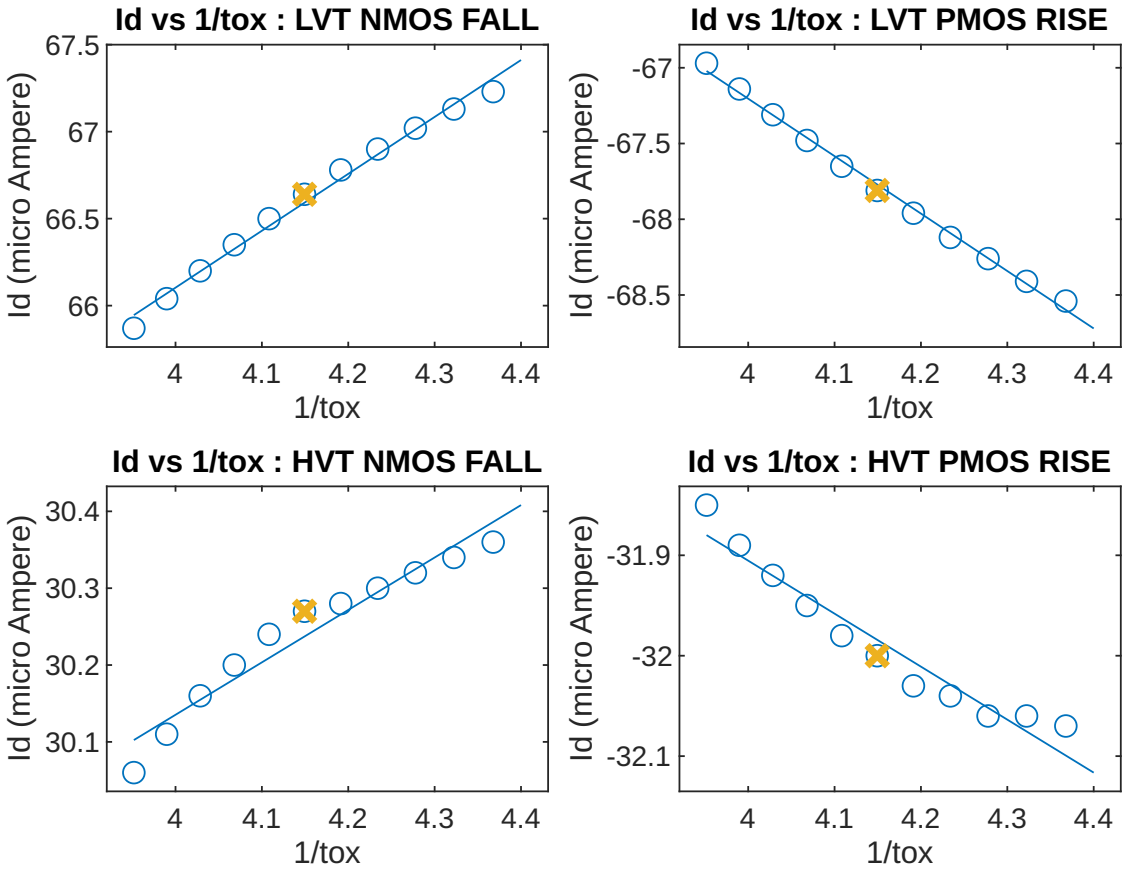

Figure 4.3: Current Variation with respect to t_{ox}.

The computed sensitivities are shown in Tab. 4.3.

S.no	MOSFET Type	Sensitivity w.r.t t_{ox} (A/m)
1.	NMOS LVT	-5640
2.	PMOS LVT	6541.5
3.	NMOS HVT	912.9
4.	PMOS HVT	1078.8

Table 4.3: Sensitivity of saturation current I_d with respect to t_{ox}.

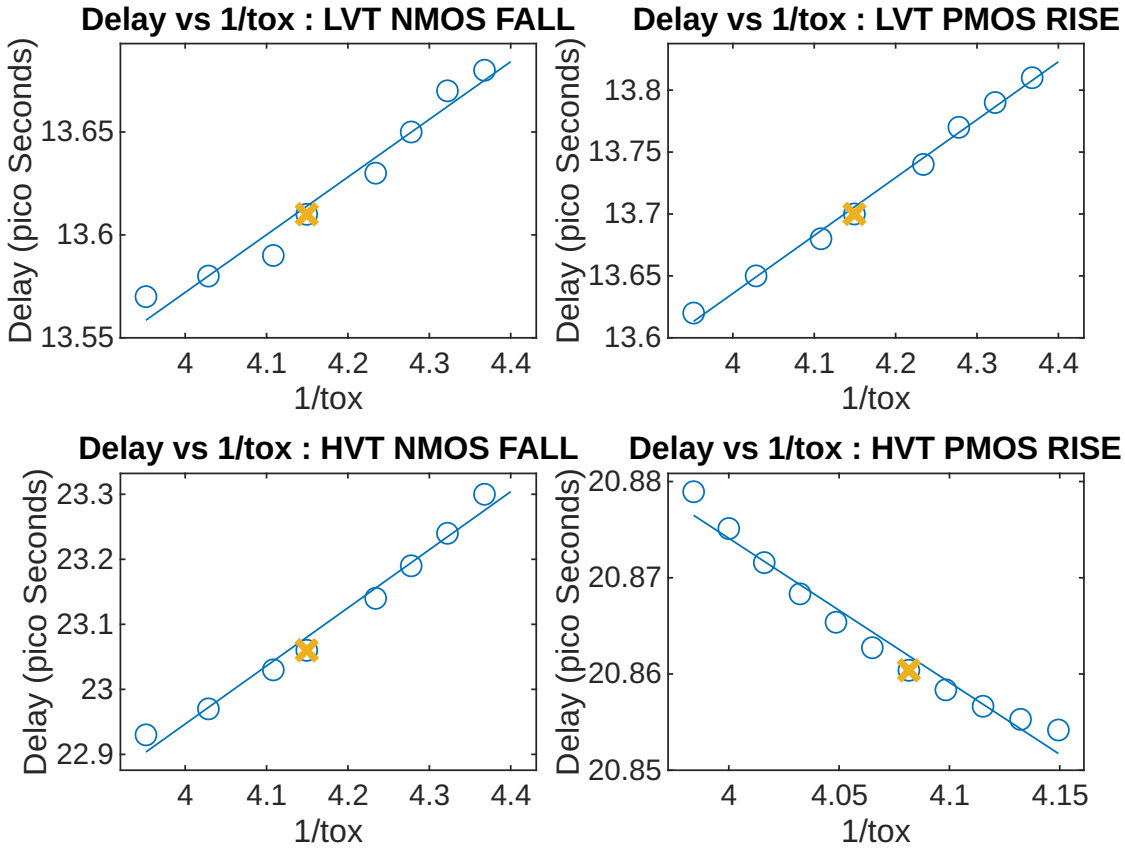

Figure 4.4: Delay variation with respect to t_{ox}.

The computed sensitivities are shown in Tab 4.4.

S.no	MOSFET Type	Sensitivity w.r.t t_{ox} (s/m)
1.	NMOS LVT -FALL	-0.000456
2.	PMOS LVT -RISE	-0.00078
3.	NMOS HVT -FALL	-0.00153
4.	PMOS HVT -RISE	0.000403

Table 4.4: Sensitivity of Delay D with respect to t_{ox}.

The variation in delay with respect to oxide thickness is shown in Fig 4.4.

4.3.2 Sensitivity with respect to width w

The variation in saturation current with respect to variation in width is shown in Fig 4.5.

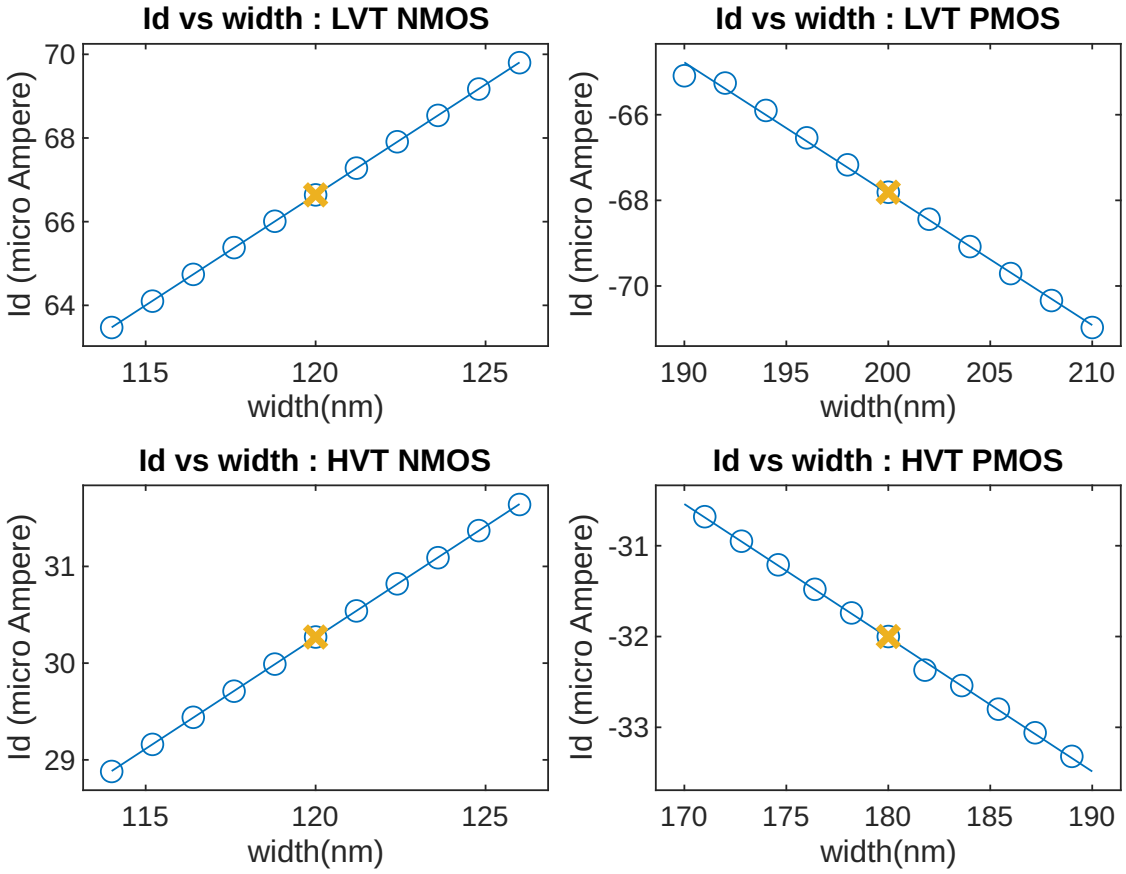

Figure 4.5: Current Variation with respect to width w.

The computed sensitivities are shown in Tab 4.5. The variation in delay with respect to variation in width is shown in Fig 4.6.

S.no	MOSFET Type	Sensitivity w.r.t w (A/m)
1.	NMOS LVT	527.5
2.	PMOS LVT	-267.0
3.	NMOS HVT	-146.7
4.	PMOS HVT	230.0

Table 4.5: Sensitivity of saturation current I_{d} with respect to w.

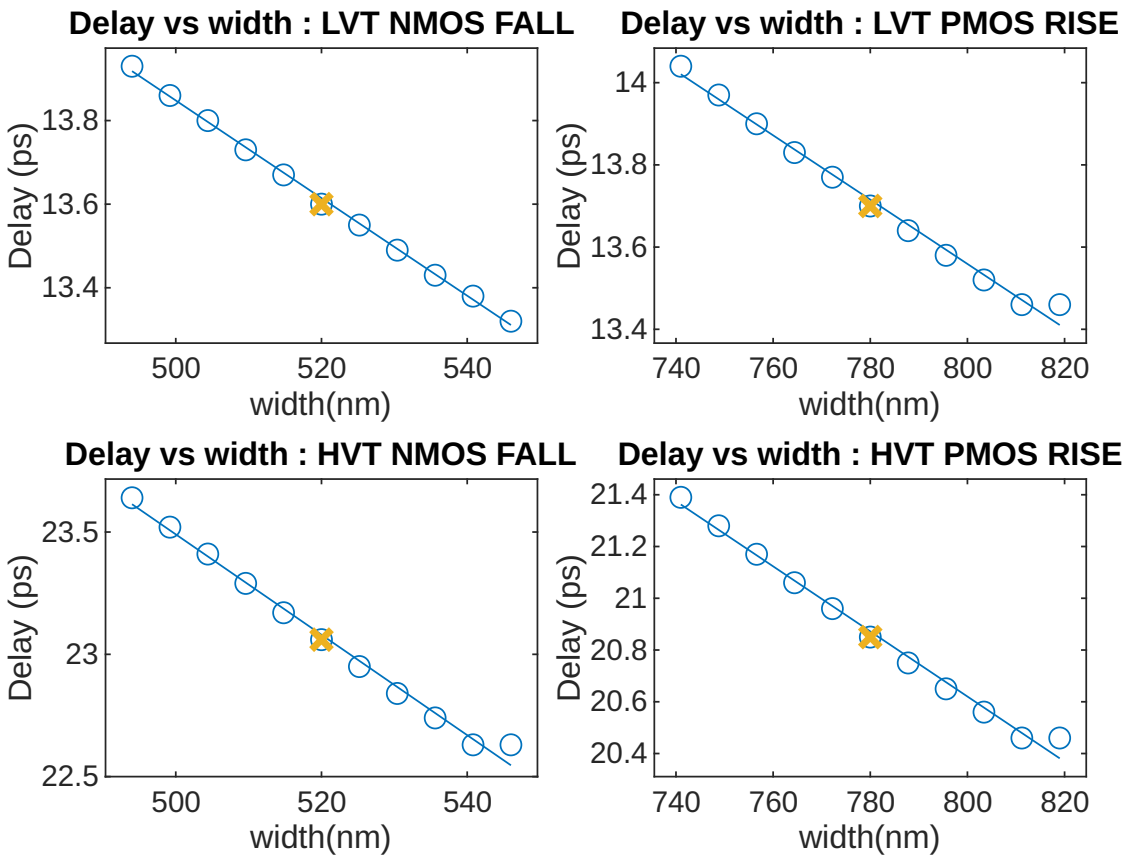

Figure 4.6: Delay variation with respect to width w.

The computed sensitivities are shown in Tab 4.6.

S.no	MOSFET Type	Sensitivity w.r.t w (s/m)
1.	NMOS LVT -FALL	-1.2×10^{-5}
2.	PMOS LVT -RISE	-7.4×10^{-6}
3.	NMOS HVT -FALL	-1.9×10^{-5}
4.	PMOS HVT -RISE	-1.2×10^{-5}

Table 4.6: Sensitivity of Delay D with respect to w.

4.3.3 Sensitivity with respect to threshold voltage V_t

The variation in saturation current with respect to variation in threshold voltage is shown in Fig 4.7.

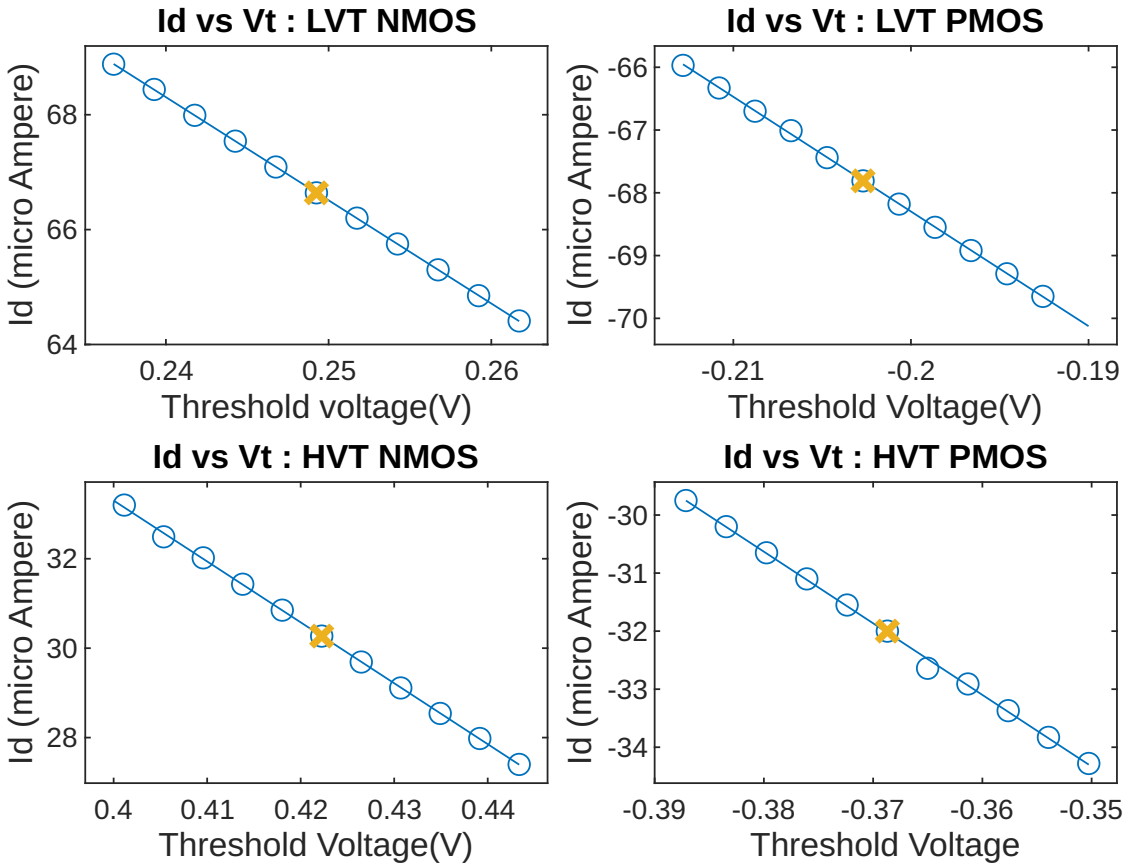

Figure 4.7: Current variation with respect to V_t.

The computed sensitivities are shown in Tab 4.7.

S.no	MOSFET Type	Sensitivity w.r.t v_{th} (A/V)
1.	NMOS LVT	-179.2$\times 10^{-6}$
2.	PMOS LVT	-182.0$\times 10^{-6}$
3.	NMOS HVT	-128.8$\times 10^{-6}$
4.	PMOS HVT	-137.0$\times 10^{-6}$

Table 4.7: Sensitivity of saturation current I_{d} with respect V_t.

The variation in delay with respect to variation in threshold voltage is shown in Fig 4.8.

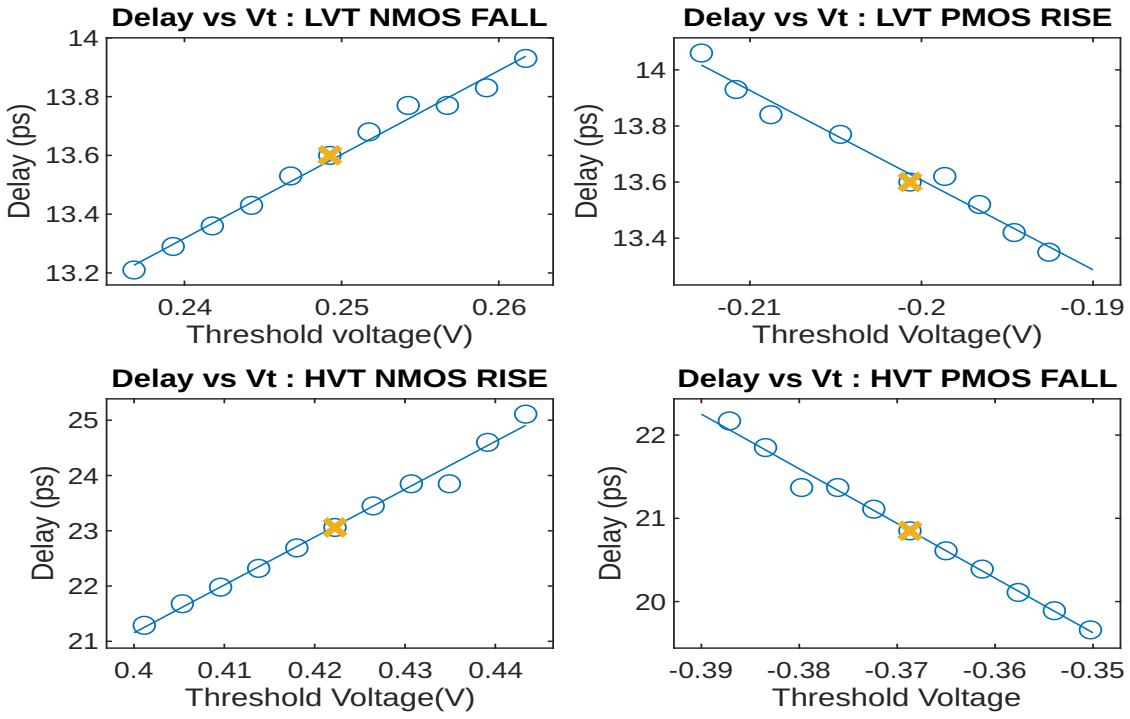

Figure 4.8: Delay variation with respect to V_t.

The computed sensitivities are shown in Tab 4.8.

S.no	MOSFET Type	Sensitivity of delay w.r.t v_{th} (s/V)
1.	NMOS LVT -FALL	28.9×10^{-12}
2.	PMOS LVT -RISE	-3.5×10^{-11}
3.	NMOS HVT -FALL	9.1×10^{-11}
4.	PMOS HVT -RISE	-6.8×10^{-11}

Table 4.8: Sensitivity of Delay D with respect to V_t.

4.3.4 Sensitivity with respect to mobility u

The variation in saturation current with respect to variation in mobility is shown in Fig 4.8.

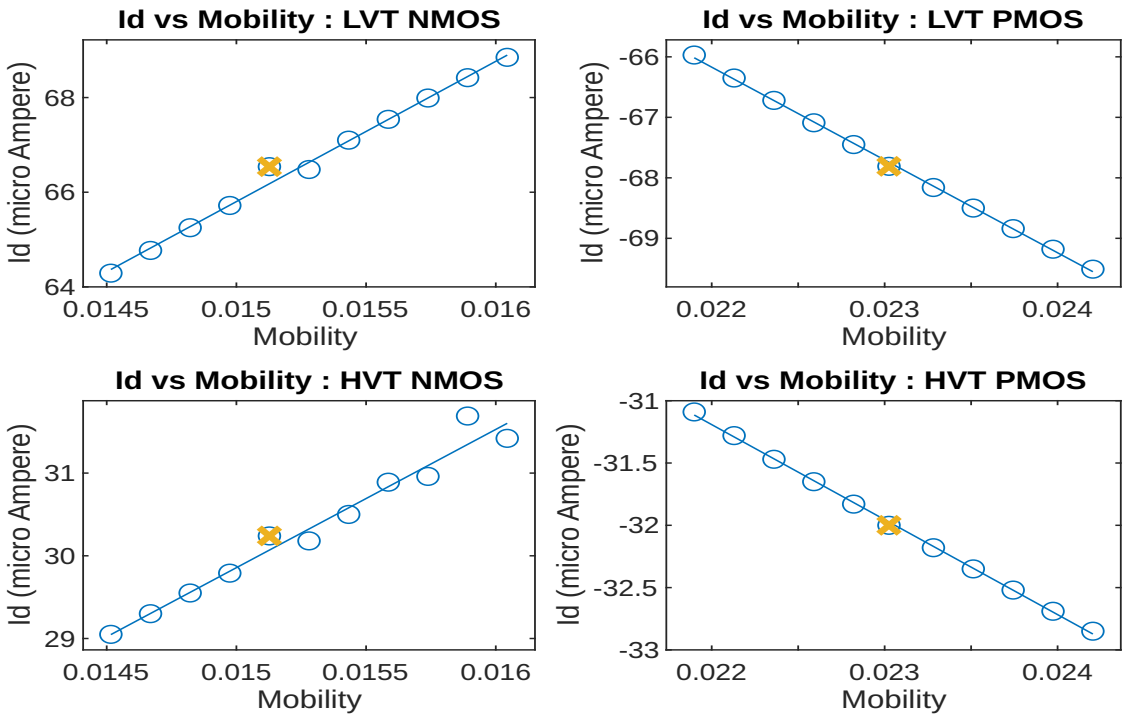

Figure 4.9: Current Variation with respect to Mobility.

The computed sensitivities are shown in table 4.9.

S.no	MOSFET Type	Sensitivity w.r.t u (AVs/m^2)
1.	NMOS LVT	0.002984
2.	PMOS LVT	-0.00154
3.	NMOS HVT	0.00155
4.	PMOS HVT	-0.000763

Table 4.9: Sensitivity of saturation current I_d with respect to u.

The variation in delay with respect to variation in mobility is shown in Fig 4.9.

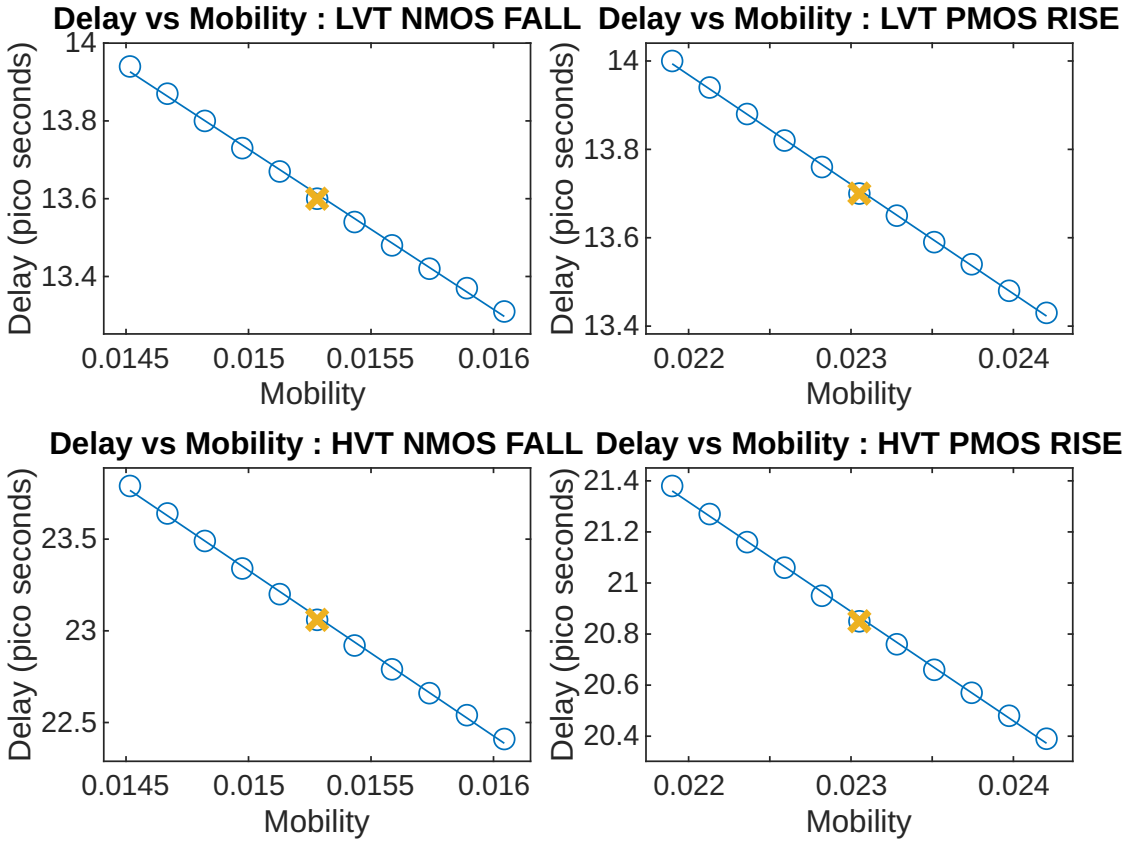

Figure 4.10: Delay Variation with respect to Mobility.

The computed sensitivities are shown in table 4.10.

S.no	MOSFET Type	Sensitivity w.r.t u (s^2V/m^2)
1.	NMOS LVT -FALL	-4.12$\times 10^{-10}$
2.	PMOS LVT -RISE	-2.47$\times 10^{-10}$
3.	NMOS HVT -FALL	-9.03$\times 10^{-10}$
4.	PMOS HVT -RISE	-4.30$\times 10^{-10}$

Table 4.10: Sensitivity of Delay D with respect to u.

4.4 Calculation of variance in saturation current I_d using analytical model

4.4.1 Variance of I_d in LVT NMOS

	t_{ox}(A/m)	w(A/m)	v_{th} (A/V)	u (AVs/m^2)
	c1	c2	c3	c4
LVT NMOS	-5640	527.5	-0.000179	0.002984

Table 4.11: Sensitivity of n-type low-threshold voltage MOSFET saturation current with respect to device parameters.

	VARIANCE	units
t_{ox}	1.77$\times 10^{-22}$	m^2
w	9.62$\times 10^{-}18$	m^2
v_{th}	1.28$\times 10^{-4}$	V^2
u	1.20$\times 10^{-8}$	$(m^2/Vs)^2$

Table 4.12: Variance of n-type low-threshold voltage MOSFET device parameters.

	COVARIANCE	units
COV(t_{ox},w)	-3.4402$\times 10^{-20}$	m^4
COV(t_{ox},v_{th})	8.1455$\times 10^{-14}$	mV
COV(t_{ox},u)	-1.4946$\times 10^{-17}$	$\frac{m^3}{Vs}$
COV(w,v_{th})	-2.2132$\times 10^{-11}$	mV
COV(w,u)	8.549$\times 10^{-14}$	$\frac{m^3}{Vs}$
COV(v_{th},u)	-1.0296$\times 10^{-6}$	$\frac{m^2}{s}$

Table 4.13: Co-Variance of n-type low-threshold voltage MOSFET device parameters.

Using the analytical equation for variance derived in chapter 3:

$$Var(I_{\text{d}}) = {c_1}^2 Var(t_{\text{ox}}) + {c_2}^2 Var(w) + {c_3}^2 Var(v_{\text{th}}) + {c_4}^2 Var(u) + 2[c_1 c_2 Cov(t_{\text{ox}}, w) +$$

$$c_1 c_3 Cov(t_{\text{ox}}, v_{\text{th}}) + c_1 c_4 Cov(t_{\text{ox}}, u) + c_2 c_3 Cov(w, v_{\text{th}}) + c_2 c_4 Cov(w, u) + c_3 c_4 Cov(v_{\text{th}}, u)]$$

Putting the values of sensitivities c_1, c_2, c_3 and c_4 and values of variances and the co-variances:

$$VAR(I_{\text{d}}) = (5.614 \times 10^{-15} + 2.67 \times 10^{-12} + 4.12 \times 10^{-12} + 1.07 \times 10^{-13})$$

$$+2(1.02\times 10^{-13} + 8.23\times 10^{-14} + 2.52\times 10^{-16} + 2.09\times 10^{-12} + 1.35\times 10^{-13} + 5.5\times 10^{-13})$$

$$= 6.92 \times 10^{-12} + 5.92 \times 10^{-12}$$

$$= 1.282 \times 10^{-11} A^2$$

Similarly when only two device parameters are considered i.e. only width w and threshold voltage v_{th}, then variance becomes:

$$Var(I_{\mathrm{d}}) = {c_2}^2 Var(w) + {c_3}^2 Var(v_{\mathrm{th}}) + 2[c_2 c_3 Cov(w, v_{\mathrm{th}})]$$

$$VAR(I_{\mathrm{d}}) = (2.67 \times 10^{-12} + 4.12 \times 10^{-12} + 2 \times 2.09 \times 10^{-12})$$

$$= 1.1 \times 10^{-11} A^2$$

4.4.2 Variance of I_d in LVT PMOS

	t_{ox}(A/m)	w (A/m)	v_{th} (A/V)	u (AVs/m^2)
	c1	c2	c3	c4
LVT PMOS	6541.52	-267	-0.000182	-0.00154

Table 4.14: Sensitivity of p-type low-threshold voltage MOSFET saturation current with respect to device parameters.

	VARIANCE	units
t_{ox}	1.68×10^{-22}	m^2
w	9.47×10^{-18}	m^2
v_{th}	8.03×10^{-5}	V^2
u	2.42×10^{-7}	$(\frac{m^2}{Vs})^2$

Table 4.15: Variance of p-type low-threshold voltage MOSFET device parameters.

	COVARIANCE	units
COV(t_{ox},w)	-3.33$\times 10^{-20}$	m^2
COV(t_{ox},v_{th})	6.40$\times 10^{-14}$	mV
COV(t_{ox},u)	4.95$\times 10^{-15}$	$\frac{m3}{Vs}$
COV(w,v_{th})	-1.75$\times 10^{-11}$	$\frac{m^3}{Vs}$
COV(w,u)	-1.40$\times 10^{-12}$	mV
COV(v_{th},u)	2.59$\times 10^{-6}$	$\frac{m^2}{s}$

Table 4.16: Co-Variance of p-type low-threshold voltage MOSFET device parameters.

Using the analytical equation for variance derived in chapter 3:

$$Var(I_{\mathrm{d}}) = {c_1}^2 Var(t_{\mathrm{ox}}) + {c_2}^2 Var(w) + {c_3}^2 Var(v_{\mathrm{th}}) + {c_4}^2 Var(u) + 2[c_1 c_2 Cov(t_{\mathrm{ox}}, w) +$$

$$c_1 c_3 Cov(t_{\mathrm{ox}}, v_{\mathrm{th}}) + c_1 c_4 Cov(t_{\mathrm{ox}}, u) + c_2 c_3 Cov(w, v_{\mathrm{th}}) + c_2 c_4 Cov(w, u) + c_3 c_4 Cov(v_{\mathrm{th}}, u)]$$

Putting the values of sensitivities $c1, c2, c3$ and $c4$ and values of variances and covariances-

$$VAR(I_{\mathrm{d}}) = (7.23 \times 10^{-15} + 6.75 \times 10^{-13} + 2.66 \times 10^{-12} + 5.76 \times 10^{-13})$$

$$+2(5.82\times 10^{-14} - 7.62\times 10^{-14} - 4.99\times 10^{-14} - 8.52\times 10^{-13} - 5.77\times 10^{-13} + 7.29\times 10^{-13})$$

$$= 3.92 \times 10^{-12} - 1.54 \times 10^{-12}$$

$$= 2.38 \times 10^{-12} A^2$$

Similarly when only two device parameters are considered i.e. only width w and threshold voltage v_{th}, then variance becomes:

$$Var(I_{\mathrm{d}}) = {c_2}^2 Var(w) + {c_3}^2 Var(v_{\mathrm{th}}) + 2[c_2 c_3 Cov(w, v_{\mathrm{th}})]$$

$$VAR(I_{\mathrm{d}}) = (9.12 \times 10^{-13} + 2.60 \times 10^{-12} + 2 * (-9.79 \times 10^{-13})$$

$$= 1.56 \times 10^{-12} A^2$$

4.4.3 Variance of I_d in HVT NMOS

	t_{ox} (A/m)	w (A/m)	v_{th} (A/V)	u (AVs/m^2)
	c1	c2	c3	c4
HVT NMOS	1078.8	230	-0.000137	0.00155

Table 4.17: Sensitivity of n-type high-threshold voltage MOSFET saturation current with respect to device parameters

	VARIANCE	
t_{ox}	1.70×10^{-22}	m^2
w	4.48×10^{-18}	m^2
v_{th}	1.37×10^{-4}	V^2
u	2.89×10^{-9}	$(\frac{m^2}{Vs})^2$

Table 4.18: Variance of n-type high-threshold voltage MOSFET device parameters.

	COVARIANCE	units
COV(t_{ox},w)	-2.05$\times 10^{-20}$	m^2
COV(t_{ox},v_{th})	7.782$\times 10^{-14}$	mV
COV(t_{ox},u)	4.33$\times 10^{-16}$	$\frac{m^3}{Vs}$
COV(w,v_{th})	-3.11$\times 10^{-12}$	mV
COV(w,u)	-9.97$\times 10^{-15}$	$\frac{m^3}{Vs}$
COV(v_{th},u)	1.42$\times 10^{-07}$	$\frac{m^2}{s}$

Table 4.19: Co-Variance of n-type high-threshold voltage MOSFET device parameters.

Using the analytical equation for variance derived in chapter 3:

$$Var(I_{\mathrm{d}}) = {c_1}^2 Var(t_{\mathrm{ox}}) + {c_2}^2 Var(w) + {c_3}^2 Var(v_{\mathrm{th}}) + {c_4}^2 Var(u) + 2[c_1 c_2 Cov(t_{\mathrm{ox}}, w) +$$

$$c_1 c_3 Cov(t_{\mathrm{ox}}, v_{\mathrm{th}}) + c_1 c_4 Cov(t_{\mathrm{ox}}, u) + c_2 c_3 Cov(w, v_{\mathrm{th}}) + c_2 c_4 Cov(w, u) + c_3 c_4 Cov(v_{\mathrm{th}}, u)]$$

Putting the values of sensitivities $c1, c2, c3$ and $c4$ and values of variances and covariances-

$$VAR(I_{\mathrm{d}}) = (1.98 \times 10^{-16} + 2.37 \times 10^{-13} + 2.6 \times 10^{-12} + 6.91 \times 10^{-15})$$

$$+2(-5.07\times10^{-15} - 1.15\times10^{-14} + 7.23\times10^{-16} + 9.8\times10^{-14} - 3.55\times10^{-15} - 3.02\times10^{-14})$$

$$= 2.844 \times 10^{-12} - 9.6808 \times 10^{-14}$$

$$= 2.941 \times 10^{-12} A^2$$

Similarly when only two device parameters are considered i.e. only width w and threshold voltage v_{th}, then variance becomes:

$$Var(I_{\mathrm{d}}) = {c_2}^2 Var(w) + {c_3}^2 Var(v_{\mathrm{th}}) + 2[c_2 c_3 Cov(w, v_{\mathrm{th}})]$$

$$VAR(I_{\mathrm{d}}) = (2.37 \times 10^{-13} + 2.6 \times 10^{-12} + 2 \times 9.8 \times 10^{-14})$$

$$= 3.03 \times 10^{-}12A^2$$

4.4.4 Variance of I_d in HVT PMOS

	t_{ox}(A/m)	w (A/m)	v_{th} (A/V)	u (AVs/m^2)
	c1	c2	c3	c4
HVT PMOS	912.85	-146.66	-0.0001228	-0.000763

Table 4.20: Sensitivity of p-type high-threshold voltage MOSFET saturation current with respect to device parameters.

	VARIANCE	units
t_{ox}	1.75×10^{-22}	m^2
w	8.28×10^{-18}	m^2
v_{th}	8.48×10^{-5}	V^2
u	1.39×10^{-7}	$(\frac{m^2}{Vs})^2$

Table 4.21: Variance of p-type high-threshold voltage MOSFET device parameters.

	COVARIANCE	units
COV(t_{ox},w)	-3.30$\times 10^{-20}$	m^2
COV(t_{ox},v_{th})	7.16$\times 10^{-14}$	mV
COV(t_{ox},u)	4.44$\times 10^{-15}$	$\frac{m^3}{Vs}$
COV(w,v_{th})	-1.97$\times 10^{-11}$	mV
COV(w,u)	-1.005$\times 10^{-12}$	$\frac{m^3}{Vs}$
COV(v_{th},u)	1.82$\times 10^{-6}$	$\frac{m^2}{s}$

Table 4.22: Co-Variance of p-type high-threshold voltage MOSFET device parameters.

Using the analytical equation for variance derived in chapter 3:

$$Var(I_{\mathrm{d}}) = {c_1}^2 Var(t_{\mathrm{ox}}) + {c_2}^2 Var(w) + {c_3}^2 Var(v_{\mathrm{th}}) + {c_4}^2 Var(u) + 2[c_1 c_2 Cov(t_{\mathrm{ox}}, w) +$$

$$c_1 c_3 Cov(t_{\mathrm{ox}}, v_{\mathrm{th}}) + c_1 c_4 Cov(t_{\mathrm{ox}}, u) + c_2 c_3 Cov(w, v_{\mathrm{th}}) + c_2 c_4 Cov(w, u) + c_3 c_4 Cov(v_{\mathrm{th}}, u)]$$

Putting the values of sensitivities c_1, c_2, c_3 and c_4 and values of variances and covariances-

$$VAR(I_{\mathrm{d}}) = (1.146 \times 10^{-16} + 1.78 \times 10^{-13} + 1.28 \times 10^{-12} + 8.1 \times 10^{-14})$$

$$+2(4.42\times 10^{-15} - 8.03\times 10^{-15} - 3.1\times 10^{-15} - 3.55\times 10^{-13} - 1.12\times 10^{-13} + 1.71\times 10^{-13})$$

$$= 1.54 \times 10^{-12} - 6.05 \times 10^{-13}$$

$$= 9.35 \times 10^{-13} A^2$$

Similarly when only two device parameters are considered i.e. only width w and threshold voltage v_{th}, then variance becomes:

$$Var(I_{\text{d}}) = {c_2}^2 Var(w) + {c_3}^2 Var(v_{\text{th}}) + 2[c_2 c_3 Cov(w, v_{\text{th}})]$$

$$VAR(I_{\text{d}}) = (1.88 \times 10^{-13} + 1.34 \times 10^{-12} + 2 \times (-3.74 \times 10^{-13}))$$

$$= 7.88 \times 10^{-13} A^2$$

4.4.5 Comparison of results obtained using the proposed model with the experimental results

We have compared the results of saturation current extracted experimentally using Monte Carlo simulations with the results computed using the analytical model derived in Chapter 3. The results are shown in the Tab. 4.23 and 4.24 along with the corresponding percentage error.

	Experimental Variance (I_d)	Computed Variance (I_d)	Experimental Std. Dev. (I_d)	Computed Std. Dev. (I_d)	% ERROR (Std.Dev)
LVT NMOS	1.28×10^{-11}	1.28×10^{-11}	3.58×10^{-6}	3.58×10^{-6}	0.05
LVT PMOS	2.10×10^{-12}	2.09×10^{-12}	1.45×10^{-6}	1.44×10^{-6}	0.68
HVT NMOS	2.99×10^{-12}	2.94×10^{-12}	1.73×10^{-6}	1.71×10^{-6}	0.86
HVT PMOS	9.46×10^{-13}	9.35×10^{-13}	9.73×10^{-7}	9.67×10^{-7}	0.61

Table 4.23: Comparison of the results obtained using the proposed model with experimental results for saturation current when four device parameters are considered

These results show that the maximum error in the computation of standard deviation of saturation current is less than 1%. Hence, the proposed model is quite accurate and is able to adequately capture the essential details of variations..

	Experimental Var(I_d)	Computed Var(I_d (w,v_{th}))	Experimental Std.Dev(I_d)	Computed Std.Dev (I_d(w,v_{th}))	% ERROR (Std.Dev)
LVT NMOS	1.28×10^{-11}	1.10×10^{-11}	3.58×10^{-6}	3.31×10^{-6}	7.5
LVT PMOS	2.10×10^{-12}	1.56×10^{-12}	1.45×10^{-6}	1.25×10^{-6}	13.8
HVT NMOS	2.99×10^{-12}	3.12×10^{-12}	1.73×10^{-6}	1.74×10^{-6}	0.6
HVT PMOS	9.46×10^{-13}	7.88×10^{-13}	9.73×10^{-7}	8.75×10^{-7}	10.1

Table 4.24: Comparison of the results obtained using the proposed model with experimental results for saturation current when only two device parameters (w and V_t) are considered

These results show that the maximum error in the computation of standard deviation of saturation current when the variations in only two device parameters is considered is less than 15%. Hence, the proposed model is can be used for approximate calculations.

4.5 Calculation of variance Delay D variance using analytical model

4.5.1 Variance of Fall Delay in LVT Invertor

	t_{ox} (s/m)	w (s/m)	v_{th} (s/V)	u (Vs^2/m^2)
	c1	c2	c3	c4
LVT NMOS	-0.000456	-1.173×10^{-05}	2.88×10^{-11}	-4.12×10^{-10}

Table 4.25: Sensitivity of fall delay of LVT-Invertor with respect to device parameters

	VARIANCE	units
t_{ox}	1.76×10^{-22}	m^2
w	9.62×10^{-18}	m^2
v_{th}	1.28×10^{-4}	V^2
u	1.20×10^{-8}	$(\frac{m^2}{Vs})^2$

Table 4.26: Variance of n-type low-threshold voltage MOSFET device parameters

	COVARIANCE	units
COV(t_{ox},w)	-3.44×10^{-20}	m^2
COV(t_{ox},v_{th})	8.14×10^{-14}	mV
COV(t_{ox},u)	-1.49×10^{-17}	$\frac{m^3}{Vs}$
COV(w,v_{th})	-2.21×10^{-11}	mV
COV(w,u)	8.55×10^{-14}	$\frac{m^3}{Vs}$
COV(v_{th},u)	-1.03×10^{-6}	$\frac{m^2}{s}$

Table 4.27: Co-Variance of n-type low-threshold voltage MOSFET device parameters

Using the analytical equation for variance derived in chapter 3:

$$Var(D) = {c_1}^2 Var(t_{ox}) + {c_2}^2 Var(w) + {c_3}^2 Var(v_{th}) + {c_4}^2 Var(u) + 2[c_1 c_2 Cov(t_{ox}, w) +$$

$$c_1 c_3 Cov(t_{ox}, v_{th}) + c_1 c_4 Cov(t_{ox}, u) + c_2 c_3 Cov(w, v_{th}) + c_2 c_4 Cov(w, u) + c_3 c_4 Cov(v_{th}, u)]$$

Putting the values of sensitivities c_1, c_2, c_3 and c_4 and values of variances and covariances-

$$Var(D) = (3.67 \times 10^{-29} + 1.32 \times 10^{-27} + 1.07 \times 10^{-25} + 2.045 \times 10^{-27})$$

$$+2(-1.84\times10^{-28} - 1.072\times10^{-27} - 2.81\times10^{-30} + 7.49\times10^{-27} + 4.135\times10^{-28} + 1.23\times10^{-26})$$

$$= 1.104 \times 10^{-25} + 3.78 \times 10^{-26}$$

$$= 1.48 \times 10^{-25} s^2$$

Similarly when only two device parameters are considered i.e. only width w and threshold voltage v_{th}, then variance becomes:

$$Var(D) = {c_2}^2 Var(w) + {c_3}^2 Var(v_{th}) + 2[c_2 c_3 Cov(w, v_{th})]$$

$$Var(D) = (1.20 \times 10^{-27} + 1.17 \times 10^{-25} + 2 \times (7.49 \times 10^{-27}))$$

$$= 1.33 \times 10^{-25} s^2$$

4.5.2 Variance of Rise Delay in LVT Invertor

	t_{ox} (s/m)	w (s/m)	v_{th} (s/V)	u (Vs^2/m^2)
	c1	c2	c3	c4
LVT PMOS	-0.00078	-7.44×10^{-6}	-3.50×10^{-11}	-2.47×10^{-10}

Table 4.28: Sensitivity of Rise Delay of LVT-Invertor with respect to device parameters

	VARIANCE	units
t_{ox}	1.68×10^{-22}	m^2
w	9.47×10^{-18}	m^2
v_{th}	8.03×10^{-5}	V^2
u	2.42×10^{-7}	$(\frac{m^2}{Vs})^2$

Table 4.29: Variance of p-type low-threshold voltage MOSFET device parameters

	COVARIANCE	units
COV(t_{ox},w)	-3.33×10^{-20}	m^2
COV(t_{ox},v_{th})	6.40×10^{-14}	mV
COV(t_{ox},u)	4.95×10^{-15}	$\frac{m^3}{Vs}$
COV(w,v_{th})	-1.75×10^{-11}	mV
COV(w,u)	-1.40×10^{-12}	$\frac{m^3}{Vs}$
COV(v_{th},u)	2.59×10^{-6}	$\frac{m^2}{s}$

Table 4.30: Co-Variance of p-type low-threshold voltage MOSFET device parameters

Using the analytical equation for variance derived in chapter 3:

$$Var(D) = {c_1}^2 Var(t_{ox}) + {c_2}^2 Var(w) + {c_3}^2 Var(v_{th}) + {c_4}^2 Var(u) + 2[c_1 c_2 Cov(t_{ox}, w) +$$

$$c_1 c_3 Cov(t_{ox}, v_{th}) + c_1 c_4 Cov(t_{ox}, u) + c_2 c_3 Cov(w, v_{th}) + c_2 c_4 Cov(w, u) + c_3 c_4 Cov(v_{th}, u)]$$

Putting the values of sensitivities $c1, c2, c3$ and $c4$ and values of variances and covariances-

$$Var(D) = (1.027 \times 10^{-28} + 5.24 \times 10^{-28} + 9.85 \times 10^{-26} + 1.48 \times 10^{-26})$$

$$+2(-1.93\times10^{-28}+1.75\times10^{-27}+9.55\times10^{-28}-4.56\times10^{-27}-2.58\times10^{-27}+2.25\times10^{-26})$$

$$= 1.14 \times 10^{-25} + 3.575 \times 10^{-26}$$

$$= 1.5 \times 10^{-25} s^2$$

Similarly when only two device parameters are considered i.e. only width w and threshold voltage v_{th}, then variance becomes:

$$Var(D) = {c_2}^2 Var(w) + {c_3}^2 Var(v_{\text{th}}) + 2[c_2 c_3 Cov(w, v_{\text{th}})]$$

$$Var(D) = (5.871 \times 10^{-28} + 5.5884 \times 10^{-26} + 2 \times (-3.64 \times 10^{-27}))$$

$$= 8.63 \times 10^{-26} s^2$$

4.5.3 Variance of Fall Delay in HVT Invertor

	t_{ox} (s/m)	w (s/m)	v_{th} (s/V)	u (Vs^2/m^2)
	c1	c2	c3	c4
HVT NMOS	-0.00153	-1.94×10^{-5}	9.05×10^{-11}	-9.03×10^{-10}

Table 4.31: Sensitivity of fall delay of HVT-invertor with respect to device parameters

Parameters	VARIANCE	units
t_{ox}	1.70×10^{-22}	m^2
w	4.48×10^{-18}	m^2
v_{th}	1.37×10^{-4}	V^2
u	2.89×10^{-9}	$(\frac{m^2}{Vs})^2$

Table 4.32: Variance of n-type high-threshold voltage MOSFET device parameters

Co-variances	Values	
COV(t_{ox},w)	-2.04 $\times 10^{-20}$	m^2
COV(t_{ox},v_{th})	7.78 $\times 10^{-14}$	mV
COV(t_{ox},u)	4.33 $\times 10^{-16}$	$\frac{m^3}{Vs}$
COV(w,v_{th})	-3.11 $\times 10^{-12}$	mV
COV(w,u)	-9.97 $\times 10^{-15}$	$\frac{m^3}{Vs}$
COV(v_{th},u)	1.42 $\times 10^{-7}$	$\frac{m^2}{s}$

Table 4.33: Co-Variance of n-type high-threshold voltage MOSFET device parameters

Using the analytical equation for variance derived in chapter 3:

$$Var(D) = {c_1}^2 Var(t_{ox}) + {c_2}^2 Var(w) + {c_3}^2 Var(v_{th}) + {c_4}^2 Var(u) + 2[c_1 c_2 Cov(t_{ox}, w) +$$

$$c_1 c_3 Cov(t_{ox}, v_{th}) + c_1 c_4 Cov(t_{ox}, u) + c_2 c_3 Cov(w, v_{th}) + c_2 c_4 Cov(w, u) + c_3 c_4 Cov(v_{th}, u)]$$

Putting the values of sensitivities c1,c2,c3,c4 and values of variances and co-variances-

$$Var(D) = (3.98 \times 10^{-28} + 1.69 \times 10^{-27} + 1.12 \times 10^{-24} + 2.35 \times 10^{-27})$$

$$+2(-6.07\times10^{-28} - 1.08\times10^{-27} + 5.98\times10^{-28} + 5.46\times10^{-27} - 1.75\times10^{-28} - 1.16\times10^{-26})$$

$$= 1.124 \times 10^{-24} - 3.425 \times 10^{-26}$$

$$= 1.089 \times 10^{-24} s^2$$

Similarly when only two device parameters are considered i.e. only width w and threshold voltage v_{th}, then variance becomes:

$$Var(D) = {c_2}^2 Var(w) + {c_3}^2 Var(v_{\text{th}}) + 2[c_2 c_3 Cov(w, v_{\text{th}})]$$

$$VAR(D) = (1.69 \times 10^{-27} + 1.12 \times 10^{-24} + 2 \times 5.46 \times 10^{-27})$$

$$= 1.13 \times 10^{-24} s^2$$

4.5.4 Variance of Rise Delay of HVT Invertor

	t_{ox} (s/m)	w (s/m)	v_{th} (s/V)	u ($\frac{m^2}{Vs}$)
	c1	c2	c3	c4
HVT PMOS	0.000403	-1.2$\times 10^{-05}$	-6.81$\times 10^{-11}$	-4.3$\times 10^{-10}$

Table 4.34: Sensitivity of rise delay of HVT-invertor with respect to device parameters

Parameter	VARIANCE	Units
t_{ox}	1.75$\times 10^{-22}$	m^2
w	8.28$\times 10^{-18}$	m^2
v_{th}	8.49$\times 10^{-5}$	V^2
u	1.39 $\times 10^{-7}$	$(\frac{m^2}{Vs})^2$

Table 4.35: Variance of p-type high-threshold voltage MOSFET device parameters

Parameter	Values	Units
COV(t_{ox},w)	-3.30$\times 10^{-20}$	m^2
COV(t_{ox},v_{th})	7.16$\times 10^{-14}$	mV
COV(t_{ox},u)	4.44$\times 10^{-15}$	$\frac{m^3}{Vs}$
COV(w,v_{th})	-1.97$\times 10^{-11}$	mV
COV(w,u)	-1.00$\times 10^{-12}$	$\frac{m^3}{Vs}$
COV(v_{th},u)	1.83$\times 10^{-6}$	$\frac{m^2}{s}$

Table 4.36: Co-Variance of p-type high-threshold voltage MOSFET device parameters

Using the analytical equation for variance derived in chapter 3:

$$Var(D) \approx c_1{}^2 Var(t_{ox}) + c_2{}^2 Var(w) + c_3{}^2 Var(v_{th}) + c_4{}^2 Var(u) + 2[c_1 c_2 Cov(t_{ox}, w) +$$

$$c_1 c_3 Cov(t_{ox}, v_{th}) + c_1 c_4 Cov(t_{ox}, u) + c_2 c_3 Cov(w, v_{th}) + c_2 c_4 Cov(w, u) + c_3 c_4 Cov(v_{th}, u)]$$

Putting the values of sensitivities c_1, c_2, c_3 and c_4 and values of variances and co-variances-

$$Var(D) \approx (2.85 \times 10^{-29} + 1.2 \times 10^{-27} + 3.94 \times 10^{-25} + 2.57 \times 10^{-26})$$

$$+2(1.6\times 10^{-28} - 1.96\times 10^{-27} - 7.68\times 10^{-28} - 1.61\times 10^{-26} - 5.18\times 10^{-27} + 5.32\times 10^{-26})$$

$$= 4.21 \times 10^{-25} + 5.87 \times 10^{-26}$$

$$= 4.79 \times 10^{-25} s^2$$

Similarly when only two device parameters are considered i.e. only width w and threshold voltage v_{th}, then variance becomes:

$$Var(D) = {c_2}^2 Var(w) + {c_3}^2 Var(v_{\text{th}}) + 2[c_2 c_3 Cov(w, v_{\text{th}})]$$

$$VAR(D) = (1.33 \times 10^{-27} + 3.97 \times 10^{-25} + 2 \times (-1.71 \times 10^{-26}))$$

$$= 3.65 \times 10^{-25} s^2$$

4.5.5 Comparison of Results obtained using the proposed model with the experimental results

We have compared the results of inverter delays extracted experimentally using Monte Carlo simulations with the results computed using the analytical model derived in Chapter 3. The results are shown in the Tab 4.37 along with the corresponding percentage error.

	Experimental Variance (Delay (s^2))	Computed Variance (Delay (s^2))	Experimental Std. Dev. (Delay (s))	Computed Std. Dev. (Delay (s))	% Error
LVT FALL	1.88×10^{-25}	1.48×10^{-25}	4.33×10^{-13}	3.85×10^{-13}	11.00
LVT RISE	8.18×10^{-26}	8.60×10^{-26}	2.86×10^{-13}	2.93×10^{-13}	2.40
HVT FALL	1.00×10^{-24}	1.12×10^{-24}	1.00×10^{-12}	1.04×10^{-12}	4.40
HVT RISE	4.80×10^{-25}	4.79×10^{-25}	6.93×10^{-13}	6.93×10^{-13}	0.00

Table 4.37: Comparison of results obtained using the proposed model with the experimental results for inverter delay.

These results show that the error in the computation of standard deviation of inverter delay less than 11%. Hence, the proposed model an be used in timing analysis for further calculations.

	Experimental Variance (Delay (s^2))	Computed Variance (Delay (s^2))	Experimental Std. Dev. (Delay (s))	Computed Std. Dev. (Delay (s))	% Error
LVT FALL	1.87×10^{-25}	1.33×10^{-25}	4.33×10^{-13}	3.65×10^{-13}	15.7
LVT RISE	8.18×10^{-26}	8.63×10^{-26}	2.86×10^{-13}	2.94×10^{-13}	2.80
HVT FALL	1.00×10^{-24}	1.16×10^{-24}	1.00×10^{-12}	1.06×10^{-12}	6.10
HVT RISE	4.8×10^{-25}	3.65×10^{-25}	6.93×10^{-13}	6.04×10^{-13}	12.8

Table 4.38: Comparison of results obtained using the proposed model with the experimental results for inverter delay when only two device parameters (w and V_t) are considered .

These results show that the maximum error in the computation of standard deviation of inverter delay when the variations in only two device parameters is considered is around 15%. Hence, the proposed model with two device parameter instead of four variable could possibly be used for calculation.

Chapter 5

Statistical Variation in correlated multi-V_t transistors

5.1 Analytical Model of the sum of inverter delays

In the 45nm technology device model, the process parameters for LVT-transistors are a_5, a_6, a_7 and a_8 and for HVT-transistors are a_9, a_{10}, a_{11} and a_{12}. The device parameter variation with respect to the process parameter for LVT and HVT is described in the model file as shown below:

$$\begin{bmatrix} t_{ox_l} \\ w_l \\ v_{th_l} \\ u_l \end{bmatrix} = \begin{bmatrix} t_1 & t_2 & t_3 & t_4 \\ w_1 & w_2 & w_3 & w_4 \\ v_{\text{th}1} & v_{\text{th}2} & v_{\text{th}3} & v_{\text{th}4} \\ u_1 & u_2 & u_3 & u_4 \end{bmatrix} \begin{bmatrix} a_5 \\ a_6 \\ a_7 \\ a_8 \end{bmatrix} \tag{5.1}$$

$$\begin{bmatrix} t_{ox_h} \\ w_h \\ v_{th_h} \\ u_h \end{bmatrix} = \begin{bmatrix} t_5 & t_6 & t_7 & t_8 \\ w_5 & w_6 & w_7 & w_8 \\ v_{\text{th}5} & v_{\text{th}6} & v_{\text{th}7} & v_{\text{th}8} \\ u_5 & u_6 & u_7 & u_8 \end{bmatrix} \begin{bmatrix} a_9 \\ a_{10} \\ a_{11} \\ a_{12} \end{bmatrix} \tag{5.2}$$

We can write a combined matrix of both LVT and HVT transistors as follows:

$$\begin{bmatrix} t_{ox_l} \\ w_l \\ v_{th_l} \\ u_l \\ t_{ox_h} \\ w_h \\ v_{th_h} \\ u_h \end{bmatrix} = \begin{bmatrix} t_1 & t_2 & t_3 & t_4 & 0 & 0 & 0 & 0 \\ w_1 & w_2 & w_3 & w_4 & 0 & 0 & 0 & 0 \\ v_{\text{th}1} & v_{\text{th}2} & v_{\text{th}3} & v_{\text{th}4} & 0 & 0 & 0 & 0 \\ u_1 & u_2 & u_3 & u_4 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & t_5 & t_6 & t_7 & t_8 \\ 0 & 0 & 0 & 0 & w_5 & w_6 & w_7 & w_8 \\ 0 & 0 & 0 & 0 & v_{\text{th}5} & v_{\text{th}6} & v_{\text{th}7} & v_{\text{th}8} \\ 0 & 0 & 0 & 0 & u_5 & u_6 & u_7 & u_8 \end{bmatrix} \begin{bmatrix} a_5 \\ a_6 \\ a_7 \\ a_8 \\ a_9 \\ a_{10} \\ a_{11} \\ a_{12} \end{bmatrix} \tag{5.3}$$

The parameters $a_5, a_6, a_7, a_8, a_9, a_{10}, a_{11}$ and a_{12} are correlated due to the commonality in the fabrication process. Hence, we cannot treat them as fully independent. Hence, in a circuit that contains both types of transistors, we need to consider a correlation coefficient between these two types of transistors.

Therefore to study the impact of the correlation of process parameters between these two types of transistors, we have artificially defined the correlation coefficient of ρ in the device model.

We define ρ between the corresponding process parameter pairs as follows:

- Correlation between a_5 and a_9 = ρ
- Correlation between a_6 and a_{10} = ρ
- Correlation between a_7 and a_{11} = ρ
- Correlation between a_8 and a_{12} = ρ

The correlation between other pairs of process parameters is assumed to be zero. The covariance between process parameters is calculated using:

$$COV(X, Y) = \rho \sigma_X \sigma_Y$$

where, ρ is the correlation coefficient between X and Y, σ_X and σ_Y are their standard deviations respectively.

As the standard deviation of the process parameters is assumed to be '1' in the model file, the covariance matrix of the process parameters can be written as:

$$C_{\mathrm{X}} = \begin{bmatrix} 1 & 0 & 0 & 0 & \rho & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & \rho & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & \rho & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & \rho \\ \rho & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & \rho & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & \rho & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & \rho & 0 & 0 & 0 & 1 \end{bmatrix} \tag{5.4}$$

Now, since we can write equation 5.3 in the form $Y = AX$, we can compute the covariance in the device parameter using $C_Y = AC_XA^T$.

Hence, the covariance matrix C_Y can be written as:

$$C_Y = \begin{bmatrix} t_1 & t_2 & t_3 & t_4 & 0 & 0 & 0 & 0 \\ w_1 & w_2 & w_3 & w_4 & 0 & 0 & 0 & 0 \\ v_{th1} & v_{th2} & v_{th3} & v_{th4} & 0 & 0 & 0 & 0 \\ u_1 & u_2 & u_3 & u_4 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & t_5 & t_6 & t_7 & t_8 \\ 0 & 0 & 0 & 0 & w_5 & w_6 & w_7 & w_8 \\ 0 & 0 & 0 & 0 & v_{th5} & v_{th6} & v_{th7} & v_{th8} \\ 0 & 0 & 0 & 0 & u_1 & u_2 & u_3 & u_4 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 & \rho & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & \rho & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & \rho & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & \rho \\ \rho & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & \rho & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & \rho & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & \rho & 0 & 0 & 0 & 1 \end{bmatrix}$$
$$\begin{bmatrix} t_1 & w_1 & v_{th1} & u_1 & 0 & 0 & 0 & 0 \\ t_2 & w_2 & v_{th2} & u_2 & 0 & 0 & 0 & 0 \\ t_3 & w_3 & v_{th3} & u_3 & 0 & 0 & 0 & 0 \\ t_4 & w_4 & v_{th4} & u_4 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & t_5 & w_5 & v_{th5} & u_5 \\ 0 & 0 & 0 & 0 & t_6 & w_6 & v_{th6} & u_6 \\ 0 & 0 & 0 & 0 & t_7 & w_7 & v_{th7} & u_7 \\ 0 & 0 & 0 & 0 & t_8 & w_8 & v_{th8} & u_8 \end{bmatrix} \tag{5.5}$$

Next, we consider the sum of the delays of these two types of transistors. The sum operation is a basic operation in static timing analysis, and the sum of the delays, which shows statistical spread, gets significantly impacted by the correlation in their delays. Hence, it is worth exploring the impact of the correlation coefficient on the sum of the inverter delays.

We know that variance in delay is given by equation (3.18), and the sum of the delays

of two different V_t transistors would be a function of 8 random vectors.

$$\begin{aligned} D_{dh} + D_{dl} \approx & D_{dh_0} + D_{dl_0} + c_{1h}\Delta t_{ox_h} + c_{2h}\Delta w_h + c_{3h}\Delta v_{th_h} + c_{4h}\Delta u_h \\ & + c_{1l}\Delta t_{ox_l} + c_{2l}\Delta w_l + c_{3l}\Delta v_{th_l} + c_{4l}\Delta u_l \end{aligned} \tag{5.6}$$

Where,

- D_{dl} is the delay due to low-V_t transistor
- D_{dh} is the delay due to high-V_t transistor
- c_{nl} are the sensitivities of low-V_t transistor with respect to different device parameters.
- c_{nh} are the sensitivities of high-V_t transistor with respect to different device parameters.
- t_{ox_h}/t_{ox_l} is the oxide thickness of high/low-V_t transistor respectively
- w_h/w_l is the width of high/low-V_t transistor respectively
- v_{th_h}/v_{th_l} is the threshold voltage of high/low-V_t transistor respectively
- u_h/u_l is the mobility of high/low-V_t transistor respectively

The variance of the sum of two inverter delays can be written as:

$$\begin{aligned} Var(D_{dh} + D_{dl}) \approx & Var(D_{dh_0} + D_{dl_0} + c_{1h}\Delta t_{ox_h} + c_{2h}\Delta w_h + c_{3h}\Delta v_{th_h} + c_{4h}\Delta u_h \\ & + c_{1l}\Delta t_{ox_l} + c_{2l}\Delta w_l + c_{3l}\Delta v_{th_l} + c_{4l}\Delta u_l) \end{aligned} \tag{5.7}$$

Using the variances and co-variances derived using equation(5.5), the variance of the sum of inverter delays can be written as:

$$
\begin{aligned}
Var(D_{dh} + D_{dl}) \approx & c_{1h}^2 Var(\Delta t_{ox_h}) + c_{2h}^2 Var(\Delta w_h) + c_{3h}^2 Var(\Delta v_{th_h}) + c_{4h}^2 Var(\Delta u_h) \\
& + c_{1l}^2 Var(\Delta t_{ox_l}) + c_{2l}^2 Var(\Delta w_l) + c_{3l}^2 Var(\Delta v_{th_l}) + c_{4l}^2 Var(\Delta u_l) \\
& + 2 \times \sum_{i=1,j=i+1}^{i=7,j=8} Cov(X_i, Y_j)
\end{aligned}
\tag{5.8}
$$

Where, X_i and Y_i are the various device parameters.

5.2 Comparison of computation with the experimental results

Using the sensitivities derived in Chapter 4 and the co-variances derived using equation (5.5), the variance of the sum of inverter delays are calculated and shown in the Tab. 5.1-5.4:

The analysis and the comparative results for the sum of inverter delays are presented for the following cases:

- When the same transitions are considered, i.e., fall-fall and rise-rise.
- When the opposite transitions are considered, i.e., fall-rise and rise-fall

5.2.1 Results for same transition in both LVT and HVT inverters

	Computed	Experimental	Computed	Experimental	Error %
ρ	Variance	Variance	Std.Dev	Std.Dev	
0	1.24×10^{-24}	1.29×10^{-24}	1.11×10^{-12}	1.14×10^{-12}	2.6
0.2	1.39×10^{-24}	1.47×10^{-24}	1.18×10^{-12}	1.21×10^{-12}	2.4
0.5	1.61×10^{-24}	1.72×10^{-24}	1.27×10^{-12}	1.31×10^{-12}	3.1
0.8	1.83×10^{-24}	2.00×10^{-24}	1.35×10^{-12}	1.41×10^{-12}	4.2
1.00	1.98×10^{-24}	2.14×10^{-24}	1.41×10^{-12}	1.46×10^{-12}	3.4

Table 5.1: Variance in the sum of the fall delay of LVT inverter and fall-delay of HVT inverter

	Computed	Experimental	Computed	Experimental	Error %
ρ	Variance	Variance	Std.Dev	Std.Dev	
0	6.30×10^{-25}	6.41×10^{-25}	7.94×10^{-13}	8.00×10^{-13}	0.75
0.2	7.37×10^{-25}	7.50×10^{-25}	8.58×10^{-13}	8.66×10^{-13}	0.92
0.5	8.97×10^{-25}	9.09×10^{-25}	9.47×10^{-13}	9.53×10^{-13}	0.63
0.8	1.05×10^{-24}	1.06×10^{-24}	1.03×10^{-12}	1.08×10^{-12}	0.38
1.0	1.16×10^{-24}	1.17×10^{-24}	1.08×10^{-12}	1.08×10^{-12}	0.00

Table 5.2: Variance in the sum of the rise delay of LVT-inverter and rise delay of HVT-inverter

The results in Tab. 5.1 and 5.2 shows that the maximum error in the computed results and the results extracted from Monte Carlo simulations is less than 5%. This signifies that the proposed model is accurate and can be used for timing analysis.

It is observed that the standard deviation increases as the correlation between the LVT

and HVT transistor increases. With increase in correlation the impact of variations on the delay in the two types of transistors move in the same direction. Therefore the spread increases.

5.2.2 Results for opposite transition in LVT and HVT inverter

Next, we show the results for the sum of rise and fall of LVT and HVT inverter and vice-versa.

	Computed	Experimental	Computed	Experimental	Error %
ρ	Variance	Variance	Std.Dev	Std.Dev	
0	6.28×10^{-25}	6.59×10^{-25}	7.92×10^{-13}	8.12×10^{-13}	2.5
0.2	5.24×10^{-25}	5.34×10^{-25}	7.23×10^{-13}	7.30×10^{-6}	0.9
0.5	3.68×10^{-25}	3.65×10^{-25}	6.06×10^{-13}	6.04×10^{-13}	0.3
0.8	2.12×10^{-25}	2.00×10^{-25}	4.60×10^{-13}	4.47×10^{-13}	2.9
1.0	8.97×10^{-26}	8.31×10^{-26}	2.99×10^{-13}	2.88×10^{-13}	3.9

Table 5.3: Variance in the sum of the fall delay of LVT-inverter and rise delay of HVT-inverter

	Computed	Experimental	Computed	Experimental	Error %
ρ	Variance	Variance	Std.Dev	Std.Dev	
0	1.24×10^{-24}	1.10×10^{-24}	1.12×10^{-12}	1.10×10^{-12}	1.8
0.2	1.09×10^{-24}	1.05×10^{-24}	1.04×10^{-12}	1.03×10^{-12}	1.0
0.5	8.57×10^{-25}	8.43×10^{-25}	9.26×10^{-13}	9.18×10^{-13}	0.8
0.8	6.26×10^{-25}	6.33×10^{-25}	7.91×10^{-13}	7.95×10^{-13}	0.5
1.0	4.72×10^{-25}	4.88×10^{-25}	6.86×10^{-13}	6.98×10^{-13}	1.7

Table 5.4: Variance in the sum of the rise delay of LVT inverter and fall delay of HVT inverter

The results show that the error in the computed results and the results extracted from Monte Carlo simulations is less than 4%. This signifies that the proposed model is accurate and can be used for timing analysis. It is observed that the standard deviation decreases as the correlation between the LVT and HVT transistor increases, which appears anomalous. However, the reason for this behavior is as follows. From the calculations shown in sections 4.5.1 to 4.5.4, we can observe that the most significant factor in the variance of delay calculations is the variation of the threshold voltage V_t.

	Sensitivity of Delay w.r.t V_t
NMOS LVT	+28.9$\times 10^{-12}$
PMOS HVT	-6.8$\times 10^{-11}$
NMOS HVT	+9.1$\times 10^{-11}$
PMOS LVT	-3.5$\times 10^{-11}$

Table 5.5: Sensitivity of delays with respect to threshold voltage V_t

As shown in Table 5.5, the sensitivities of delay to threshold voltage V_t are opposite for NMOS and PMOS transistors. This eventually leads to a compensating effect on the statistical spread of the sum of inverter delays. This compensating effect increases with an increase in the correlation between LVT and HVT transistors. Therefore, the overall standard deviation of the sum decreases with an increase in the correlation coefficient.

The traditional STA tools take the correlation as $\rho = 1$, whereas the realistic correlation between multi-V_t transistors is less than 1. This implies that the actual standard deviation of the sum of delays would be higher than what is taken by the STA tools for LVT and HVT inverter connected in series. Hence, the tool would give optimistic results for the worst-case analysis. Using this model, we can remove this optimism

by computing the realistic sum of delays corresponding to the correlation coefficient. However, it is worth pointing out that these results have risen from the assumptions that the process parameter a_5 correlates with a_9, a_6 correlates with a_{10}, and so on. Hence, when a realistic covariance matrix obtained from the foundry is employed for timing analysis, the results presented in this thesis need to be re-assessed.

Chapter 6

Conclusion

The motivation for this work was to incorporate the changes in the correlation between the delays of different threshold voltage transistors to make the timing analysis more robust. In this work, we derived an analytical model to compute the delays of the inverter and compute the sum of the inverter delays with the correlation factor ρ. The results show that for the sum of the delays, the maximum variation observed between the computed results and the Monte Carlo results was less than five percent. The results show that the proposed analytical model is quite accurate and can be further used to improve the timing analysis for the circuits having different threshold voltage transistors.

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