Impact of Radiation Hardened Flip-Flop Design Choices on Sustainability

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Certificate

This is to certify that the thesis titled "Impact of Radiation Hardened Flip-Flop Design Choices on Sustainability" being submitted by **Farogh Alam**, to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of **Master of Technology**, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Abstract

As CMOS technology continues to scale, integrated circuits are increasingly susceptible to radiation-induced disruptions, necessitating resilient yet efficient hardening techniques. Conventional radiation-hardened flip-flops often incur significant penalties in power, area, and performance, while overlooking sustainability concerns. This thesis proposes a novel radiation-hardened flip-flop architecture that enhances robustness against transient and upset events by employing a master-slave configuration with comprehensively protected storage nodes and controlled delay elements. The design is optimized to reduce both area and power overheads while effectively mitigating fault propagation.

Additionally, we introduce a unified Power, Performance, Area, and Sustainability (PPAS) evaluation framework that holistically assesses circuit efficiency, incorporating both embodied and operational energy components to quantify environmental impact. Implemented in 65nm CMOS technology and validated using Cadence Virtuoso, the proposed flip-flop demonstrates enhanced resilience and improved energy-conscious performance compared to existing solutions. The comparative analysis highlights consistent advantages in area, power, and environmental sustainability. By embedding sustainability metrics into early-stage design evaluation, this work contributes to the advancement of dependable and eco-friendly integrated circuits suitable for radiation-exposed applications.

Keywords: Radiation hardening, soft errors, single-event transient, Flip-Flop, sustainability, Embodied Carbon Footprint Metric, Operational Carbon Footprint Metric

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CHAPTER 1

Introduction

1.1 Motivation

With the relentless scaling of complementary metal-oxide-semiconductor (CMOS) technology, integrated circuits (ICs) have become increasingly vulnerable to radiation-induced soft errors. The reduction in node capacitance and operating voltage lowers the critical charge required for stable logic, heightening susceptibility to single-event transients (SETs) and single-event upsets (SEUs) [1], [2]. High-energy particles, such as cosmic neutrons or alpha particles, can generate charge within the silicon substrate, leading to unintended state changes in sequential elements like flip-flops [3],[4]. This growing challenge, exacerbated by increasing device density, threatens data integrity in safety-critical applications [5].

Conventional mitigation strategies, such as spatial redundancy (e.g., triple modular redundancy) [6], [7] and temporal redundancy (e.g., delayed sampling) [8], [9] , improve reliability but often incur substantial penalties in area, power, and performance. Hardened-by-design (HBD) approaches, including dual interlocked storage cells (DICE) and Schmitt trigger-based flip-flops [10], [11], enhance resilience against SEUs yet struggle to fully address SET propagation and introduce notable design overheads. Furthermore, with aggressive technology scaling, the effectiveness of traditional techniques diminishes, calling for more efficient solutions that balance reliability, power, and area without compromising practicality.

As semiconductor fabrication becomes increasingly complex and energy-intensive, a paradigm shift in evaluation methodologies is essential. The traditional power, performance, and area (PPA) trade-off is no longer sufficient; sustainability has emerged as a critical fourth pillar in IC design [22]. This necessitates holistic frameworks that assess both operational efficiency and manufacturing energy costs, driving the need for early integration of sustainability metrics in the design flow.

This work addresses these evolving challenges by presenting a novel radiation-hardened flip-flop design that achieves high soft error resilience while minimizing area and power overheads. Additionally, it introduces a new evaluation methodology—Power, Performance, Area, and Sustainability (PPAS)—that extends traditional metrics to include embodied and operational energy footprints. This approach promotes sustainability-conscious decisions early in the design cycle, balancing radiation tolerance with eco-friendly circuit development.

1.2 Research Objectives

This thesis addresses these challenges through two primary objectives:

1. Develop a radiation-hardened flip-flop architecture that:
    - Achieves superior soft error resilience
    - Minimizes area overhead
    - Reduces power consumption versus conventional designs
2. Establish a Power, Performance, Area, and Sustainability (PPAS) evaluation framework that:
    - Developes embodied carbon footprint matrics
    - Develops operational carbon footprint metrics
    - Provides normalized Total carbon footprint sustainability metrics for comparative analysis

1.3 Thesis Organization

This thesis is structured as follows:

- **Chapter 1** introduces the challenges and motivations
- **Chapter 2** reviews prior radiation-hardening techniques
- **Chapter 3** details the HNMS-FF architecture
- **Chapter 4** presents comparative and simulation results
- **Chapter 5** describes the PPAS evaluation framework
- **Chapter 6** provides conclusions and future directions

CHAPTER 2

Background and Related Work

2.1 Soft Errors and Their Growing Significance

As complementary metal-oxide-semiconductor (CMOS) technology continues to scale, ensuring the reliability of integrated circuits has become a formidable challenge. One of the most pressing issues at these advanced nodes is the increasing susceptibility of circuits to radiation-induced soft errors. This vulnerability arises from a combination of reduced supply voltages and significantly lower node capacitance, which together lead to smaller stored signal charges. As a result, even small perturbations—whether due to electromagnetic interference, coupling noise, or radiation-induced transients—can flip a logic value, compromising data integrity.

Among these noise sources, ionizing radiation poses the greatest threat in well-designed systems. The dominant radiation sources are high-energy neutrons from cosmic rays and alpha particles emitted from radioactive decay in packaging materials. When such particles interact with the silicon substrate, they generate a dense column of electron-hole pairs (EHPs) along their trajectory. If this ionization occurs near a sensitive node, such as a reverse-biased p-n junction, the generated charge can be rapidly collected by drift and diffusion mechanisms. This charge collection results in a current pulse, producing a single event transient (SET) at the node. If the magnitude of the SET is sufficient to alter the logic level and the transient is captured by a memory element during a clock edge, it leads to a single event upset (SEU)—a soft error.

The severity of the problem is amplified in logic circuits due to the high number of sequential elements like flip-flops, which lack inherent error correction and often operate at reduced voltages for energy efficiency. As device dimensions shrink and integration density increases, the critical charge, the minimum charge required to cause a bit flip—continues to decrease. Consequently, even low-energy particles can cause upsets, and the soft error rate (SER) in logic circuits increases exponentially. Moreover, the charge collection process is enhanced by physical effects such as the funneling phenomenon [16], where the ion track distorts the depletion region and accelerates charge collection deeper into the substrate. The full charge collection process, including both fast drift and slower diffusion components, generates voltage transients that can easily corrupt stored data if not properly mitigated. Thus, in today's ultra-scaled CMOS technologies, soft errors have transitioned from being a concern primarily in space systems to becoming a critical reliability challenge even in terrestrial applications like data centers, automotive electronics, and edge computing devices.

2.2 Hardened Flip-Flop Designs: Existing Approaches

Conventional soft error mitigation strategies fall into two broad categories: redundancy-based techniques and hardened-by-design (HBD) approaches. Redundancy can be either spatial, such as Triple Modular Redundancy (TMR) [17], or temporal, like delayed sampling. TMR replicates the flip-flop three times and uses majority voting to determine the correct output. While effective against SEUs within the flip-flop latches, TMR does not handle SETs on input data lines and incurs substantial area and power overheads—roughly threefold—along with added delay from the voter logic.

Temporal redundancy [17] addresses SETs by sampling the input data at staggered time intervals, ensuring that short-lived transients are not captured by all sampling instances. Like TMR, it also relies on majority voting but introduces latency and increases power consumption due to additional clocking and storage resources.

To reduce the cost of redundancy, HBD approaches modify the flip-flop structure itself to make it inherently more resilient to soft errors. A well-known example is the Dual Interlocked Storage Cell (DICE), which stores data across multiple nodes with interlocked feedback to prevent a single-node upset from flipping the stored state. While DICE-based flip-flops improve robustness against SEUs, they do not fully prevent SET propagation and still introduce area and power overheads. Given the limitations of existing techniques, especially in scaled technologies, there is a strong need for more efficient flip-flop designs that can suppress soft errors with minimal cost in area, power, and performance.

2.2.1 SET and SEU Error Tolerant Flip-Flop (SETU_TOFF)

A widely adopted method for mitigating single-event upsets (SEUs) and single-event transients (SETs) is the use of redundant latches to capture input data at multiple time instances[12]. In this architecture, two high-sensitivity redundant latches operate at slightly different phases of the clock cycle to store the same data at staggered times. This temporal redundancy allows the circuit to detect and correct transient faults by evaluating discrepancies between the stored values. A voter logic unit then compares the outputs of both latches and determines the correct data to propagate forward. If a transient error affects one latch, the other remains unaffected, ensuring reliable operation. This method effectively enhances error tolerance without introducing excessive power and area penalties. The circuit diagram illustrating this architecture is shown in Fig. 2.1.

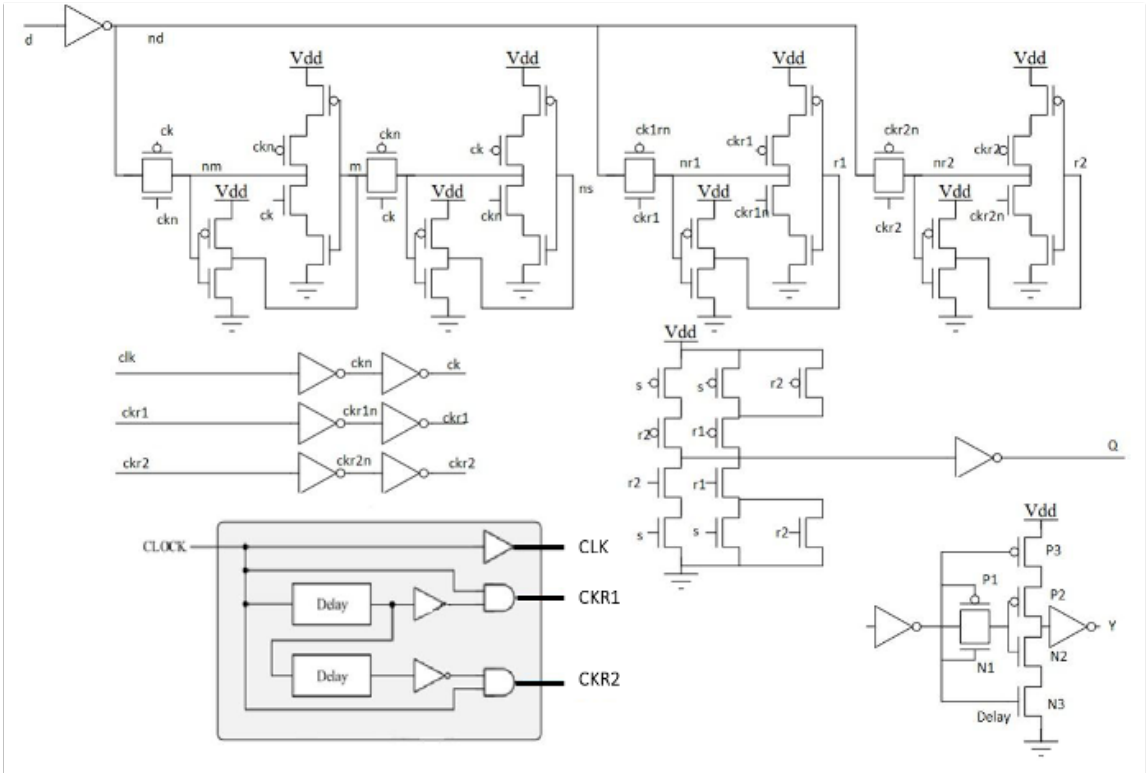

Figure 2.1: SETU-TOFF Flip-Flop (SETU-FF) [12]. A soft error-resilient flip-flop architecture using temporal redundancy.

2.2.2 Soft Error Detection and Recovery Flip-Flop (SEDR-FF)

The Soft Error Detection and Recovery Flip-Flop (SEDR-FF) [13] integrates multiple functional modules to provide enhanced fault tolerance and error recovery. The architecture consists of a Clock and Error Controller (C-E Controller), a Data Selector (MUX), a Master Latch (M-latch), a Slave Latch (S-latch), a Redundant Latch (R-latch), a History Latch (H-latch), and an Error Detector (E-detector). Under normal operation, the MUX selects the input data (D) for storage, while the M-latch and S-latch perform standard flip-flop functions. The S-latch employs a Dual Interlocked Storage Cell (DICE) to mitigate SEU-induced errors. The R-latch operates on a pulsed clock to provide an additional layer of redundancy.

A key feature of this design is the H-latch, which retains the previously stored flip-flop value and prevents erroneous data propagation through its integrated C-cell. The Error Detector (E-detector) continuously monitors discrepancies between the S-latch and R-latch, generating an error signal (Err out) when inconsistencies arise. If an error is detected, the circuit retrieves the last correct value from the H-latch to restore data integrity. By combining redundancy with error detection and correction mechanisms, the SEDR-FF provides a robust solution for mitigating transient faults. The circuit implementation of the SEDR-FF is depicted in Fig. 2.2.

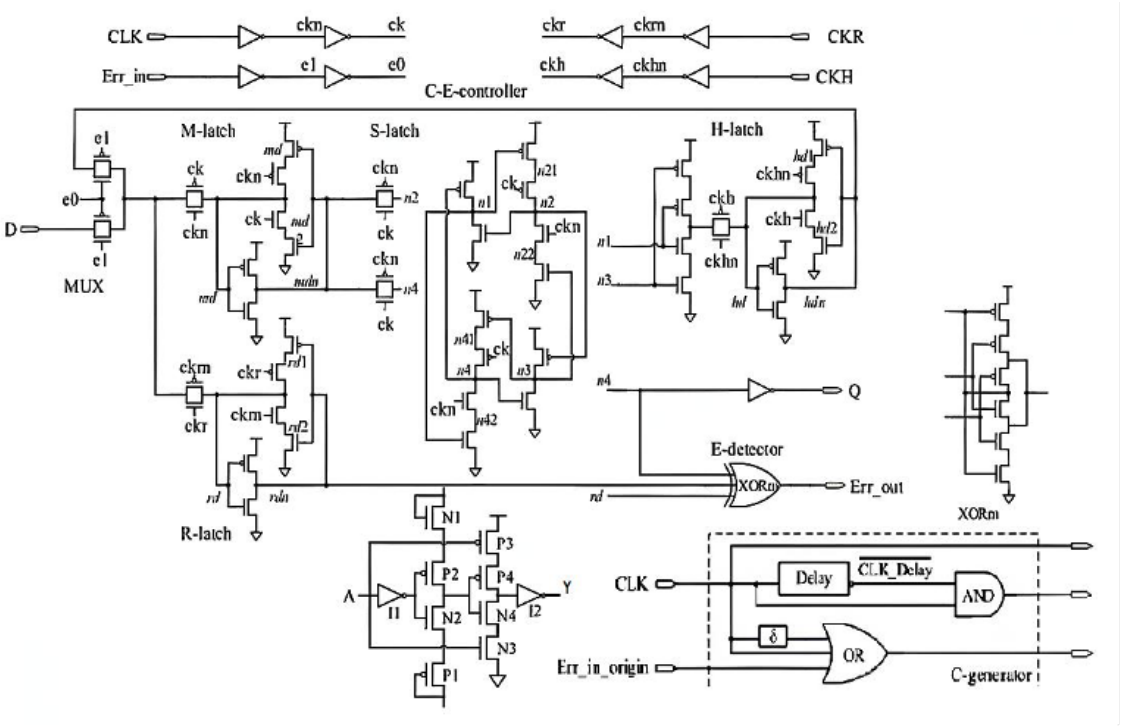

Figure 2.2: Soft Error Detection and Recovery Flip-Flop (SEDR-FF) [13]. A flip-flop integrating redundancy and error recovery mechanisms.

2.2.3 Resilient Adaptive Voltage Flip-Flop (RAV-FF)

The Resilient Adaptive Voltage Flip-Flop (RAV-FF) [14] employs a specialized delay element (DE) to regulate clock signal transitions, enhancing stability under radiation-induced disturbances. The delay element consists of two key components: a metal-oxide capacitor (MCAP) and a current-controlling transistor (CC). The MCAP charges and discharges in sync with the clock signal (CK), producing a delayed clock signal (ci2) essential for sequential operations. Since MCAP charges faster than it discharges, the discharge speed at node cni2 is used to fine-tune the rising delay of the clock signal. The CC component maintains a stable delay across varying temperature conditions, ensuring consistent flip-flop operation under diverse environmental factors.

When the CK signal is low, the input data is temporarily held in node n2. As soon as the delayed clock signal transitions high, the data is transferred, ultimately reaching the RAV-FF output. Additionally, a Consistency Evaluation unit, comprising four transistors, continuously compares the outputs of the standard flip-flop and the delayed flip-flop. If both outputs remain consistent, it allows normal data propagation. However, in case of a mismatch due to a soft error, it preserves the previous value, effectively masking the error. This self-correcting mechanism enhances the flip-flop's resilience to transient faults while maintaining low power overhead. The circuit implementation of RAV-FF is illustrated in Fig. 2.3.

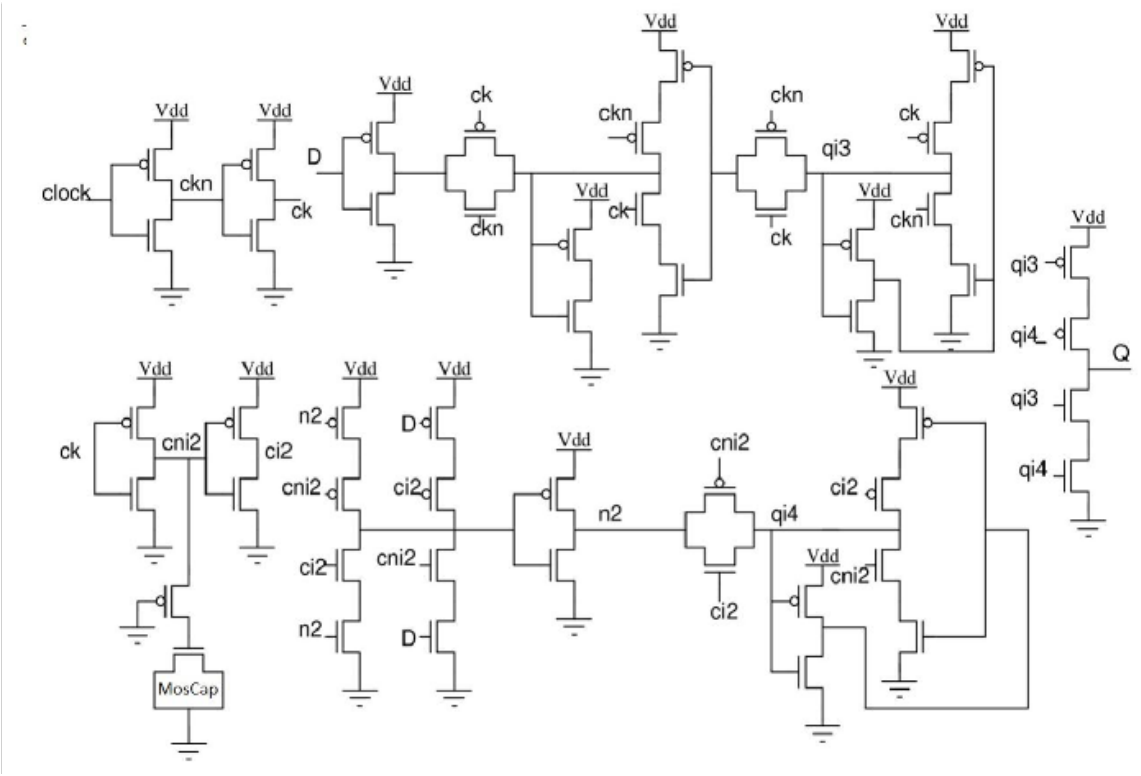

Figure 2.3: Resilient Adaptive Voltage Flip-Flop (RAV-FF) [14]. A flip-flop design with adaptive delay elements for improved soft error resilience.

2.3 Sustainability in VLSI Design

With the rapid proliferation of electronics in modern systems, the environmental impact of semiconductor design and manufacturing has become an area of increasing concern. On one hand, the shift from mechanical to electronic solutions leads to higher energy demands during operation; on the other hand, the fabrication of these components itself is resource-intensive. For instance, TSMC's electricity demand in 2023 alone was reportedly on par with the entire peak electricity consumption of a large country like India. Recognizing this growing challenge, industry leaders such as Intel, Apple [19], and STMicroelectronics [18] have outlined carbon neutrality targets in their sustainability reports. However, reports from manufacturers such as TSMC indicate that meeting these goals remains difficult, particularly due to the rising energy intensity of advanced technology nodes. While significant efforts have been made to reduce emissions during manufacturing—such as life cycle analysis (LCA), material toxicity evaluation, and multi-criteria decision frameworks—most of these approaches focus on system- or product-level assessments [20]. For example, metrics like the Toxic Potential Indicator and eco-reliability have been proposed to guide sustainable design decisions, and recent works have introduced carbon footprint estimation tools for chiplet-based architectures. Despite these advances, current practices still lack a structured methodology to incorporate sustainability metrics at the circuit design level, where fundamental decisions about architecture, logic style, and resilience are made. Furthermore, the traditional focus on area, power, and performance

(PPA) metrics often overshadows environmental considerations. This missing link in existing literature motivates the need for new figures of merit that explicitly consider both reliability and environmental impact during early-stage VLSI design. This missing link in existing literature motivates the need for new figures of merit that explicitly consider both reliability and environmental impact during early-stage VLSI design.

CHAPTER 3

Proposed HNMS-FF Architecture

The proposed flip-flop, named the Hardened Node Master-Slave Flip-Flop (HNMS-FF), adopts a master-slave configuration with fully hardened storage nodes.The circuit implementation is illustrated in Fig. 4. During normal operation, when the clock signal is low (clk = 0, transparent mode), the transmission gates are activated, allowing the input D to propagate to the output Q through two parallel paths with distinct delays. The first path enables direct data transmission through the transmission gate and storage elements, whereas the second path introduces a high-delay element in the clock path. The delayed clock signal (Ckd) modulates the timing of data propagation, effectively filtering out single-event transient (SET) pulses. By ensuring a controlled delay between the two paths, transient glitches are prevented from propagating to the output.

When the clock transitions high (`clk = 1`, latching mode), the modified storage elements retain the data state, enhancing robustness against soft errors. The integration of a high-delay clock element further strengthens the design's reliability by mitigating SET-induced timing vulnerabilities.

To illustrate the circuit's behavior, consider the initial condition where $N1 = 0$, $N2 = 0$, $PU = PD = 1$, and $Q = 1$. If a negative transient fault (TF) occurs at Q, causing a temporary drop to 0, the 2P-1N element retains its original value, ensuring that Q_b remains unchanged at 0. In parallel, the 1P-2N element responds to $Q = 0$ and $PU = 1$ by setting $Q_a = 1$, which attempts to pull $N1$ high. However, the discharge mechanism at $N1$ counteracts this effect, restoring $N1$ and $N2$ back to 0 and recovering Q to its original state of 1.

Conversely, when the initial condition is $N1 = 1$, $N2 = 1$, $PU = PD = 0$, and $Q = 0$, a positive transient fault (TF) at Q momentarily drives it to 1. Here, the 1P-2N element maintains $Q_a = 1$, preventing unintended data corruption. Simultaneously, the 2P-1N element reacts to $Q = 1$ and $PD = 0$ by toggling Q_b to 0, which attempts to pull $N2$ low. However, the charging mechanism at $P1$ ensures that $N2$ remains at 1, thereby stabilizing $N1$ and $N2$ at 1 and restoring Q to 0.

The circuit implementation of the HNMS-FF is shown in Fig. 3.1.

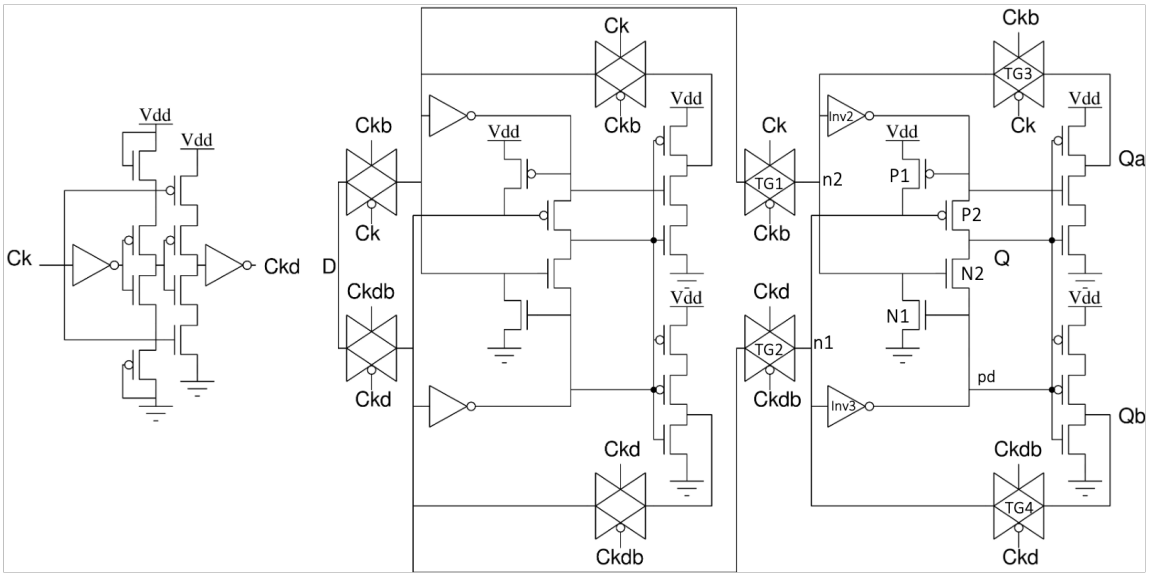

Figure 3.1: Hardened Node Master-Slave Flip-Flop (HNMS-FF). A robust flip-flop design with high-delay filtering elements to suppress SET effects.

To model single-event effects (SEE) in simulations, a time-dependent double-exponential pulse is employed [15]:

$$I(t) = I_0 \left(e^{-t/T_a} - e^{-t/T_b}\right)$$

where $I(t)$ is the transient current pulse, I_0 is the peak value of current, T_a is the rise time, and T_b is the fall time of the current pulse.

The simulation results validating the SET filtering capability of the HNMS-FF are presented in the next chapter.

CHAPTER 4

Implementation and Comparative Analysis

4.1 Performance Evaluation

To evaluate the efficiency and robustness of radiation-hardened flip-flops, several critical figures of merit (FoMs) are taken into account, each representing a key aspect of performance. These include area, clock-to-Q delay (CQ-delay), dynamic power consumption, leakage power, linear energy transfer (LET) threshold, and maximum tolerable pulse width. Together, these parameters provide a comprehensive view of the design's compactness, performance, energy efficiency, and fault resilience in the presence of radiation-induced events.

Table 4.1: Comparative Analysis of Radiation-Hardened Flip-Flops

Parameter	**SETU TOFF**	**SEDR FF**	**RAV FF**	**HNMS-FF (This Work)**
Area (μm^2)	84.032	130.468	72.800	64.558
CQ-delay (ps)	201.31	193.75	323.52	530.86
Setup (ps)	98	85	120	125
Hold (ps)	85	63	105	114
Dynamic Power (nW)	8630.88	6933.84	12591.64	5724.00
Leakage Power (nW)	85.54	18.56	132.74	42.34
LET (MeV-cm^2/mg)	26.56	42.25	74.84	91.74
Max. Pulse Tol. (ps)	110	175	310	380

Area

The area metric refers to the physical silicon footprint required for layout implementation. In this work, an innovative stacked standard cell arrangement has been employed, effectively doubling the vertical dimension in comparison to the conventional 13-track (13T) standard cell height used in STM's 65nm technology. This 26-track vertical structure integrates a shared ground rail between dual power supply rails, enhancing area utilization. The layouts for each circuit are illustrated in Figures 4.1 to 4.4.

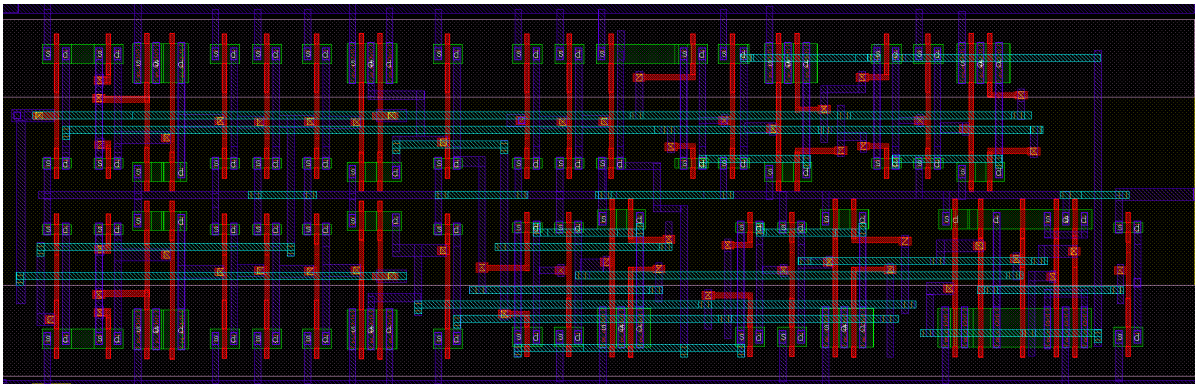

Figure 4.1: Layout of SETU TOFF Flip-Flop [12]

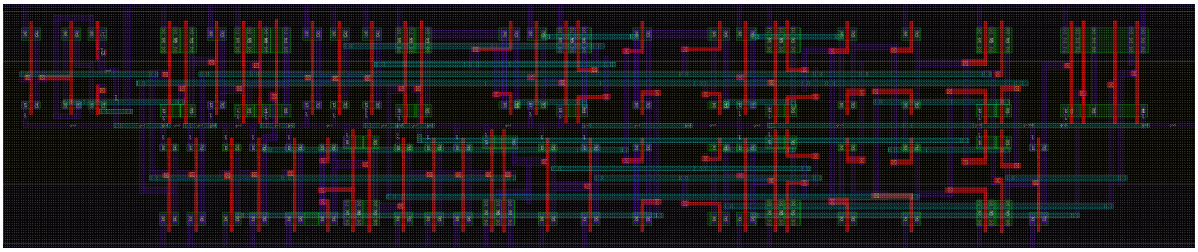

Figure 4.2: Layout of SEDR Flip-Flop [13]

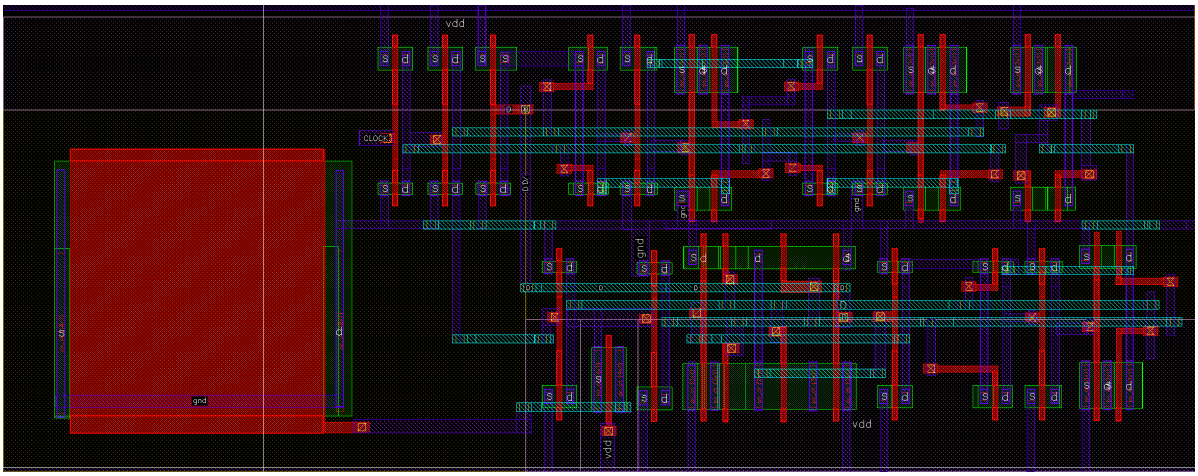

Figure 4.3: Layout of RAV Flip-Flop [14]

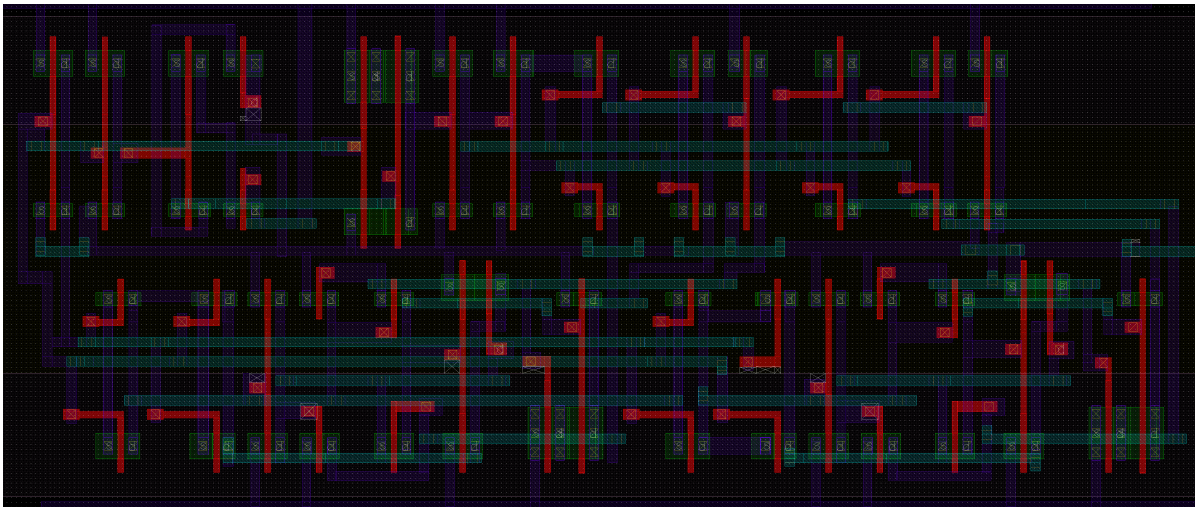

Figure 4.4: Layout of Proposed HNMS-FF

Clock-to-Q Delay

Clock-to-Q delay denotes the time interval between a triggering clock edge and the corresponding output transition. Minimizing this delay is typically advantageous for high-speed applications, although it can be strategically increased to enhance soft error tolerance. For radiation-hardened designs, longer CQ delays are often accepted in exchange for improved transient fault resilience.

As timing behavior is critical to reliable operation, the next focus turns to the constraints on data stability surrounding the clock edge—specifically, the setup and hold times.

Setup and Hold Times

Setup Time

Setup time is the minimum duration before the active clock edge during which the input data must remain stable to be correctly latched by a flip-flop or register. If violated, the output may become metastable or incorrect. In transient simulations, setup time is measured by sweeping the data transition closer to the clock edge until a violation occurs.

Hold Time

Hold time is the minimum duration after the active clock edge during which the input data must remain stable. Violating hold time can lead to incorrect data capture. It is determined by sweeping the input transition after the clock edge during simulations.

Table 4.2: Temperature Variation Analysis of CK-Q Delay

Temp (°C)	Parameter	SETU-TOFF	SEDR-FF	RAV-FF	Proposed (P-FF)
3*-40	CK-Q delay (rise)	132.86 ps	129.51 ps	296.30 ps	377.74 ps
	CK-Q delay (fall)	121.18 ps	116.59 ps	327.68 ps	476.50 ps
	Average	127.02 ps	123.05 ps	311.99 ps	427.12 ps
3*25	CK-Q delay (rise)	142.30 ps	147.46 ps	304.73 ps	335.18 ps
	CK-Q delay (fall)	130.22 ps	142.72 ps	331.77 ps	415.52 ps
	Average	136.26 ps	145.09 ps	318.25 ps	375.35 ps
3*125	CK-Q delay (rise)	158.68 ps	158.16 ps	320.73 ps	302.31 ps
	CK-Q delay (fall)	147.32 ps	148.48 ps	335.58 ps	394.92 ps
	Average	153.00 ps	153.32 ps	328.16 ps	348.62 ps

Table 4.2 shows CQ delays of all flip-flops at different temperatures, it shows proposed flip-flop higher delay consistency across temperature variations, required for higher soft error resilience.

Dynamic Power

Dynamic power refers to the energy consumed by the flip-flop during switching activities. It is primarily dependent on the switching frequency, supply voltage, output load capacitance, and activity factor. In radiation-hardened designs, balancing power efficiency with reliability is crucial, as excessive power can lead to thermal issues, while overly conservative designs might waste valuable energy. Dynamic power is the dominant power component during circuit operation, defined by:

$$P_{\text{dynamic}} = \alpha \times C \times V_{DD}^2 \times f$$

In simulations, it's computed as:

$$P_{\text{dynamic}} = V_{DD} \times Q_{\text{dynamic}} \times f \times \alpha$$

where Q_{dynamic} is the transient charge consumed during switching. From Table 4.1, the proposed HNMS-FF has the lowest dynamic power (5724 nW), indicating excellent energy efficiency, especially beneficial in battery-operated and energy-critical systems.

Leakage Power

Leakage power represents the static power consumed when the circuit is idle, mainly due to sub-threshold leakage and gate oxide leakage in CMOS transistors. While often overshadowed by dynamic power in high-frequency circuits, leakage becomes increasingly significant in scaled technologies and always-on blocks.

Leakage power is estimated as:

$$P_{\text{leakage}} = I_{\text{leakage}} \times V_{DD}$$

Average leakage current is taken across static logic states. Radiation-hardened flip-flops tend to exhibit higher leakage due to redundant nodes and extra transistors. However, the proposed HNMS-FF maintains a favorable balance, achieving lower leakage than designs like RAV FF by using stacked devices and power-gating opportunities. From Table 4.1, the proposed HNMS-FF maintains a mid-range leakage profile (42.34 nW), balancing leakage and robustness better than SETU TOFF and RAV FF.

Linear Energy Transfer (LET)

Linear Energy Transfer (LET) threshold quantifies a circuit's resilience against radiation-induced strikes, particularly heavy ions. A higher LET value indicates that the flip-flop can withstand more energetic particles without erroneous state changes.

LET quantifies how much energy a particle deposits per unit distance:

$$LET = \frac{I \cdot \Delta t}{q \cdot d \cdot \rho}$$

In simulation, double exponential current pulse for modeling single event transients (SETs).

Among the compared designs, the proposed HNMS-FF shows the highest LET threshold of 91.74 MeV-cm^2/mg, indicating superior fault immunity. This improvement is attributed to spatial redundancy and node hardening techniques integrated into the design. This is shown in table 4.1 as well as Fig. 4.5

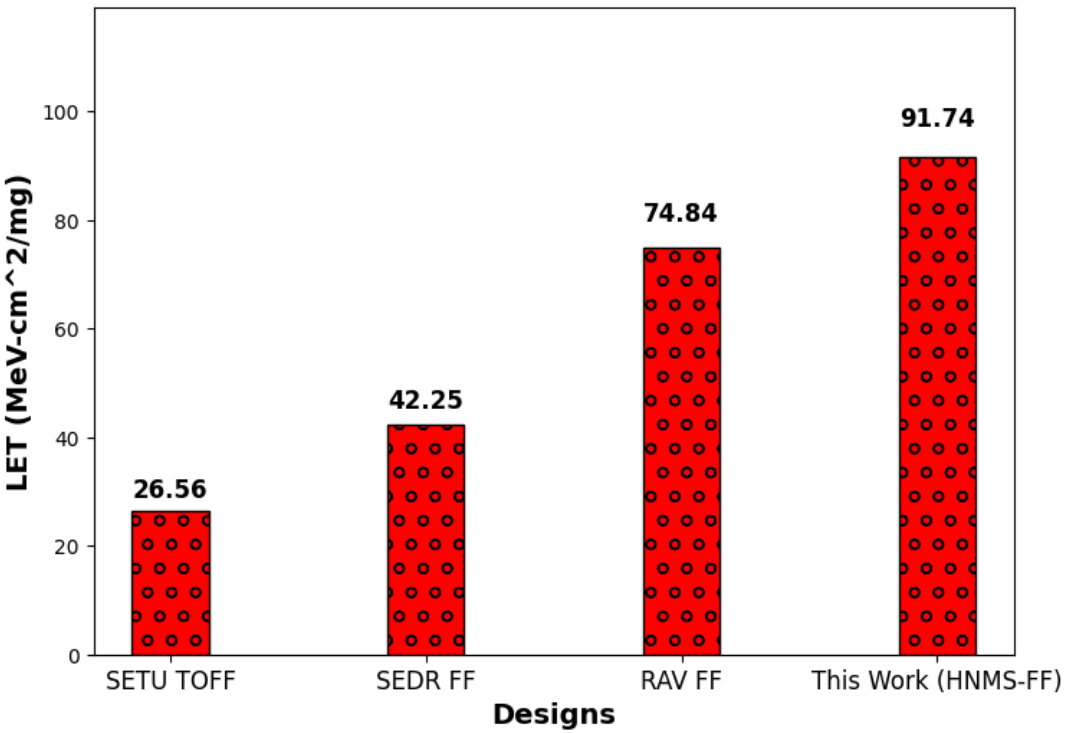

Figure 4.5: LET threshold comparison of various flip-flop architectures. The proposed flip-flop exhibits the highest radiation tolerance, as indicated by its higher LET value (91.74 MeV-cm^2/mg), outperforming SETU TOFF, SEDR FF, and RAV FF.

Maximum Tolerable Pulse Width

Maximum tolerable pulse width reflects the duration of a transient glitch that a flip-flop can tolerate without changing its output state. This metric directly relates to a flip-flop's ability to mask single-event transients (SETs) caused by radiation. Longer tolerable pulse widths suggest greater immunity to transient faults. The HNMS-FF demonstrates the highest resilience, tolerating pulses up to 380 ps, which significantly surpasses prior designs and supports its use in radiation-prone environments such as space and avionics.

4.2 SET Fault Injection and Mitigation Behavior

To validate the actual behavior of each flip-flop under SET conditions, transient faults were manually injected at sensitive nodes during simulations. Two sets of waveforms were recorded for each flip-flop:

- The first shows the output behavior when an SET is injected and the error is detected.
- The second shows the output behavior when an SET is injected and the error is not detected because of high SET pulse width.

Figures 4.6 to 4.13 present these waveform results.

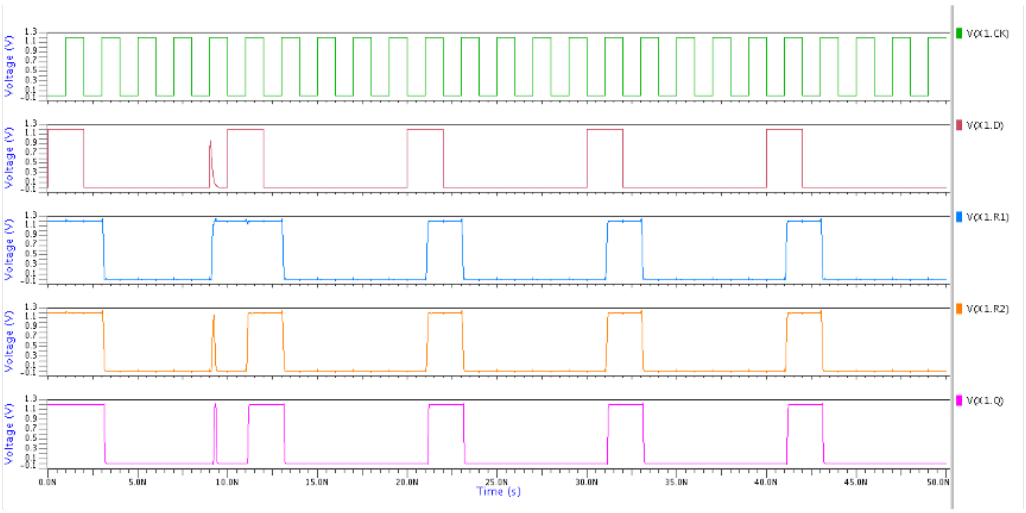

Figure 4.6: SET error detected and voter output latches the correct output in SETU TOFF.

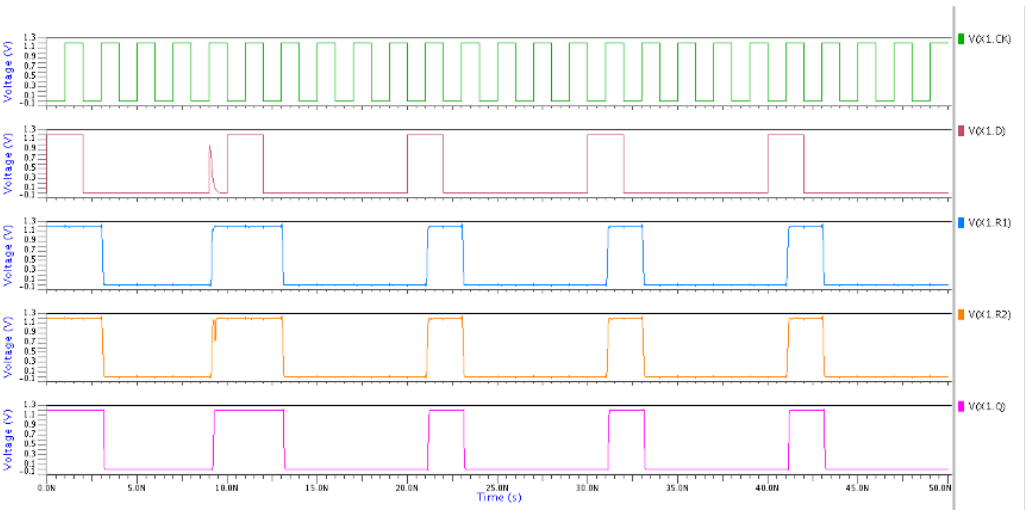

Figure 4.7: SET error not detected and voter output latches the incorrect output in SETU TOFF.

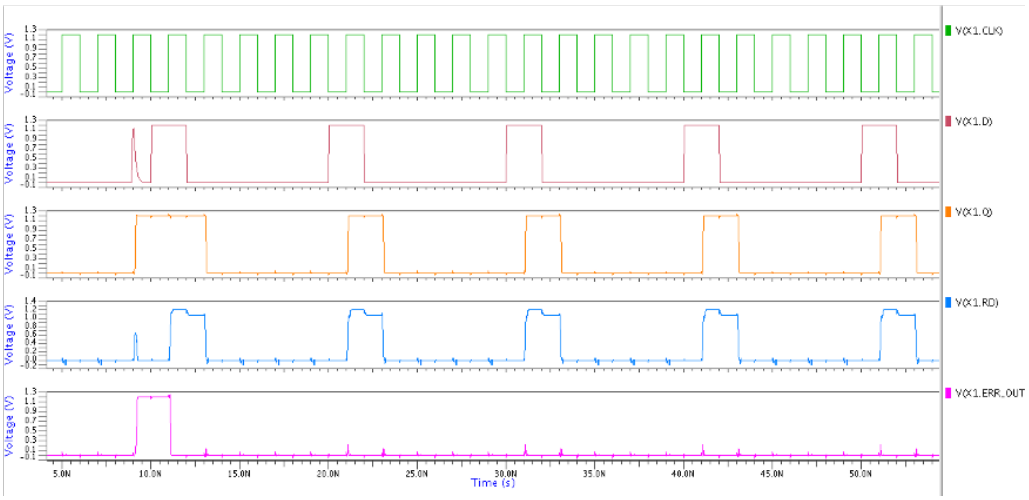

Figure 4.8: SET error detected and error logic output give error pulse in SEDR-FF.

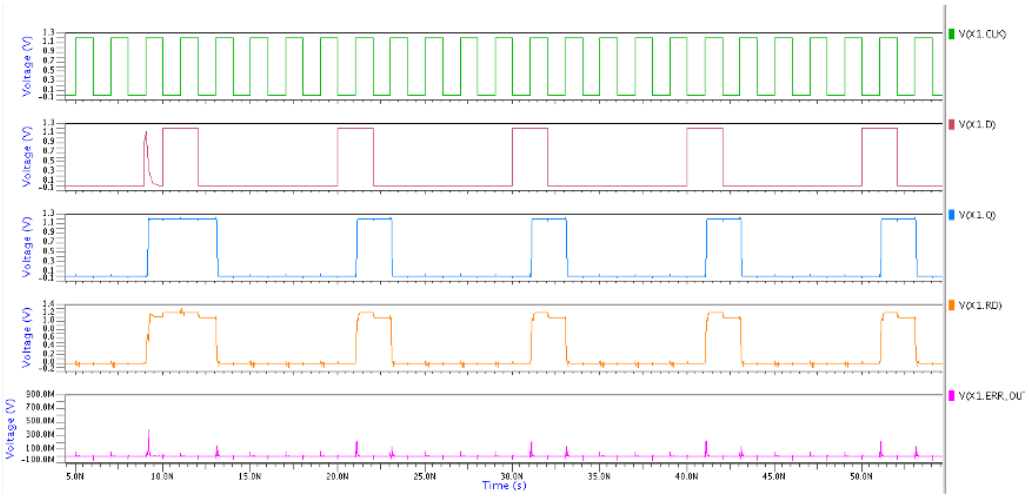

Figure 4.9: SET error not detected and error logic output did not give error pulse in SEDR-FF.

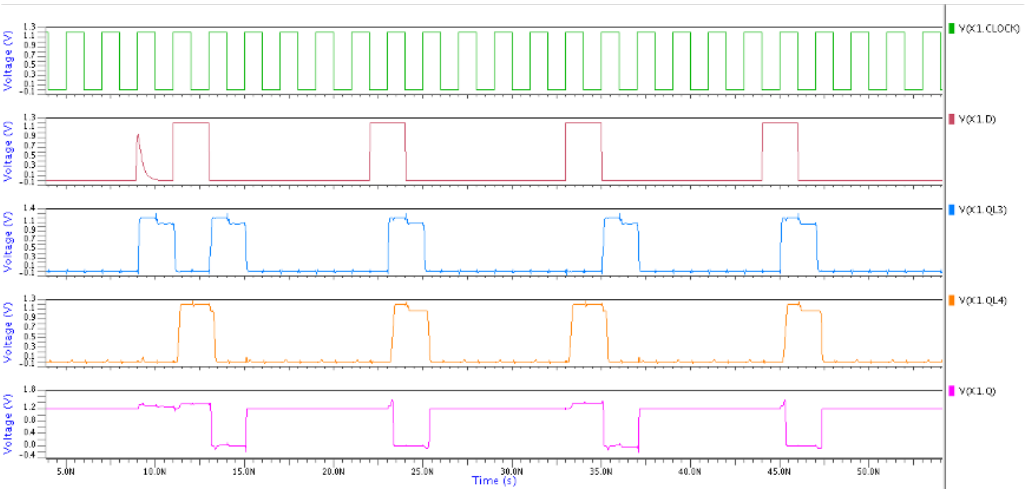

Figure 4.10: SET error detected in RAV-FF.

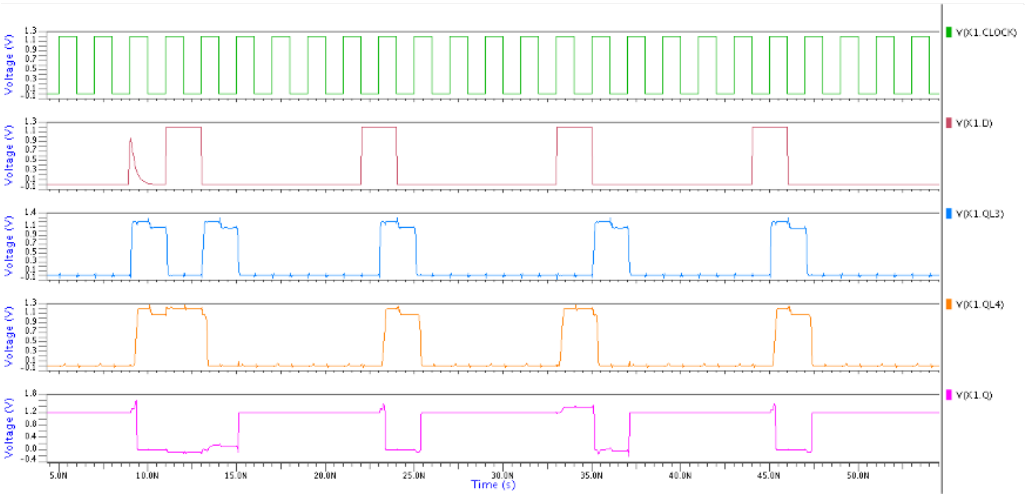

Figure 4.11: SET error not detected in RAV-FF.

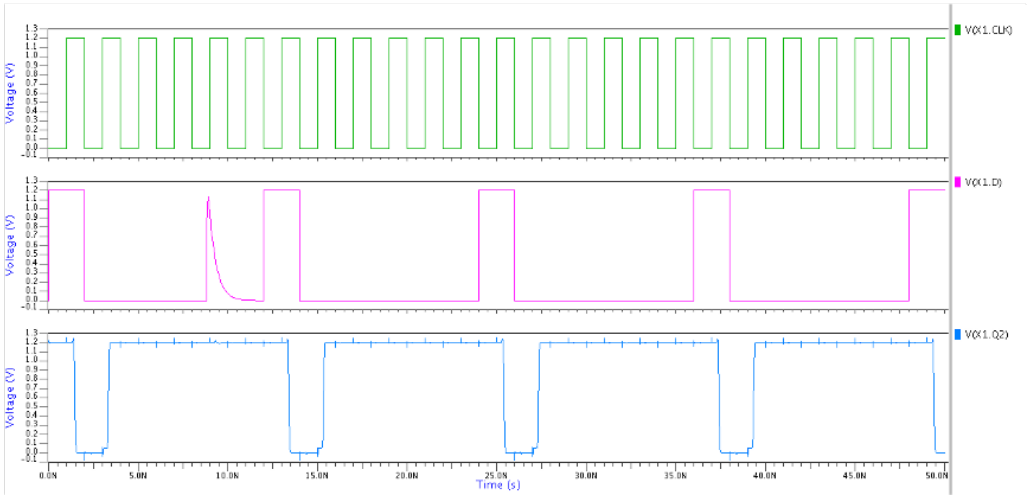

Figure 4.12: SET detection in HNMS-FF. Despite the injected glitch, internal feedback paths prevent propagation to the output.

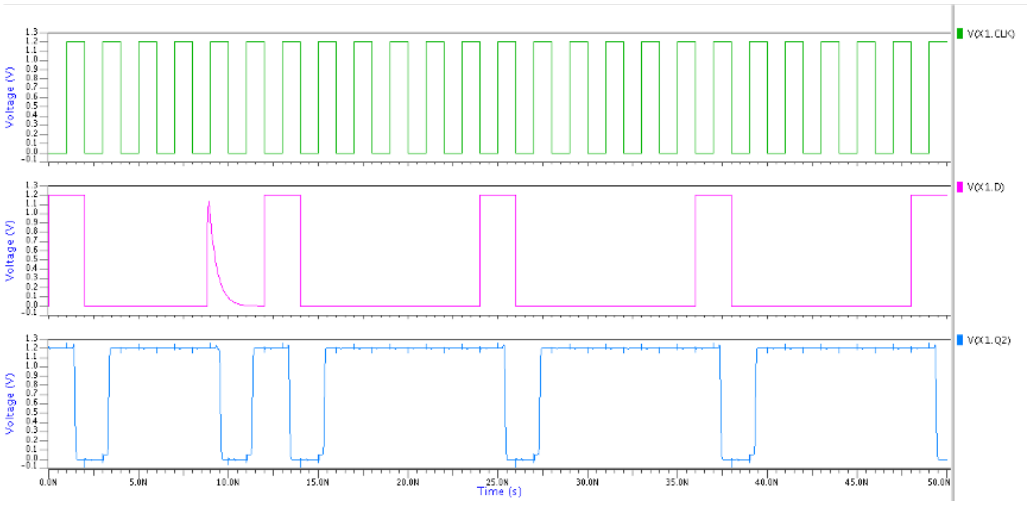

Figure 4.13: SET error did not mitigated and error persist in output in HMS-FF.

4.3 Consistency with Prior Studies

To ensure the accuracy and fairness of performance evaluation, the circuits SETU-TOFF [12], SEDR-FF [13], and RAV-FF [14] were independently re-simulated under uniform test conditions. The results obtained were found to be highly consistent with those reported in their respective studies [12][13]14],thereby reinforcing the credibility of our comparative analysis.

For SETU-TOFF, which uses temporally separated redundant latches and majority voting for soft error masking, our simulations reproduced the expected behavior. The flip-flop demonstrated successful suppression of transient faults with minimal timing and power overhead, closely matching the original results. The observed clock-to-Q delay increase was modest, consistent with the claims in [12].

In the case of SEDR-FF, which employs delayed sampling, error detection, and history-based recovery through multiple latches, our simulation confirmed effective SET/SEU protection with moderate power and low setup overhead. The LET tolerance in our results was observed to be around 42 MeV·cm^2/mg, which aligns well with the LET range of 20–50 MeV·cm^2/mg under normal incident angle reported in [13]. Additionally, our observed clk-to-Q delay for SEDR-FF remained the lowest among the three circuits, again consistent with the timing characteristics shown in the original paper.

For RAV-FF, which integrates a current-controlled capacitor-based delay element to enhance robustness and reduce temperature sensitivity, our simulations yielded an LET threshold of approximately 75 MeV·cm^2/mg, which closely matches the $\sim$77 LET reported in [14]. In terms of performance, RAV-FF exhibited the highest clk-to-Q delay due to its internal delay path, while SETU-TOFF and SEDR-FF showed mid and low delay respectively—reflecting the same relative behavior described in [14].

4.4 Discussion

The proposed HNMS-FF demonstrates clear advantages in terms of layout efficiency and resilience to radiation-induced faults, setting it apart from existing hardened flip-flop designs. By employing a novel stacked standard cell architecture, the HNMS-FF achieves a compact area footprint, which makes it a highly efficient design for applications requiring space-conscious layouts. The area reduction, however, comes at the cost of a slightly higher propagation delay, which, though larger than some of the benchmarked flip-flops, is a deliberate trade-off. This increase in delay is offset by the significant gains in fault tolerance and overall resilience to Single Event Upsets (SEUs).

The higher clock-to-Q delay observed in the proposed flip-flop is directly linked to its enhanced ability to withstand radiation strikes. As radiation-induced faults typically manifest as short-duration pulses, the increased delay improves the flip-flop's ability to tolerate these pulses without experiencing critical errors. Therefore, while this results in slower performance in non-radiation-affected environments, it provides superior robustness under radiation-prone conditions, making it ideal for high-reliability applications.

The HNMS-FF effectively balances key design metrics such as power consumption, performance, and radiation hardness. Compared to other designs, it achieves the lowest dynamic power consumption while maintaining a competitive leakage power profile. This energy efficiency is crucial in power-sensitive environments such as space-grade electronics, where power constraints are stringent.

Additionally, the superior Linear Energy Transfer (LET) threshold and the maximum toler-

able pulse width, as demonstrated in the comparative analysis, highlight the design's robustness under particle strike conditions. The proposed flip-flop outperforms existing designs in terms of radiation tolerance, making it an attractive candidate for space missions, military processors, and other applications that require fault-tolerant and reliable circuits.

In summary, while the HNMS-FF has a higher propagation delay, its design optimizes fault tolerance and energy efficiency. It strikes a crucial balance between performance and reliability, making it a compelling choice for electronics used in radiation-intensive environments, where reliability is of paramount importance. The trade-off in performance is justified by the significant improvements in overall fault tolerance, which is often more critical in such applications.

CHAPTER 5

Sustainability Evaluation Framework

In our work, we introduce a two-part sustainability metric that quantifies the environmental impact during both the fabrication and operational phases [16], [17], [18]. This metric is integrated into the PPAS framework to guide designers toward eco-friendly design choices from the early stages of the development cycle.

5.1 Embodied Carbon Footprint Metric (eCFP)

The embodied carbon footprint metric estimates the environmental impact of manufacturing by accounting for the energy consumption and associated emissions during fabrication. It is defined by the expression:

$$\text{eCFP} = \text{BE} \times \text{Area} \times \text{EMI} \times \text{API} \tag{5.1}$$

In this equation, BE represents the base energy per unit area (expressed in energy units/μm^2) as determined from a standard wafer process. The Area refers to the physical layout size of the design in μm^2, and it has a direct impact on the overall sustainability.

The EMI (Extra Metal Impact) models the overhead caused by using additional metal layers in the layout. It is calculated using:

$$\text{EMI} = 1 + (\text{TR} - 1) \times \text{CF} \tag{5.2}$$

where TR (Track Ratio) is the ratio of total routing tracks in a metal layer to the number of tracks still available for SoC-level routing, and CF (Congestion Factor) is a constant set to 0.3.

The API (Additional Process Impact) captures the extra energy needed for additional process steps and is calculated as:

$$\text{API} = ((\text{Total Masks} - \text{Standard Masks}) \times \text{Mask Factor}) + 1 \tag{5.3}$$

where the Mask Factor is 0.045, assuming each added mask step increases energy usage by 4.5%. By evaluating all designs using this metric, we can better compare their environmental

impact during fabrication. A lower value reflects a more energy-efficient and sustainable implementation.

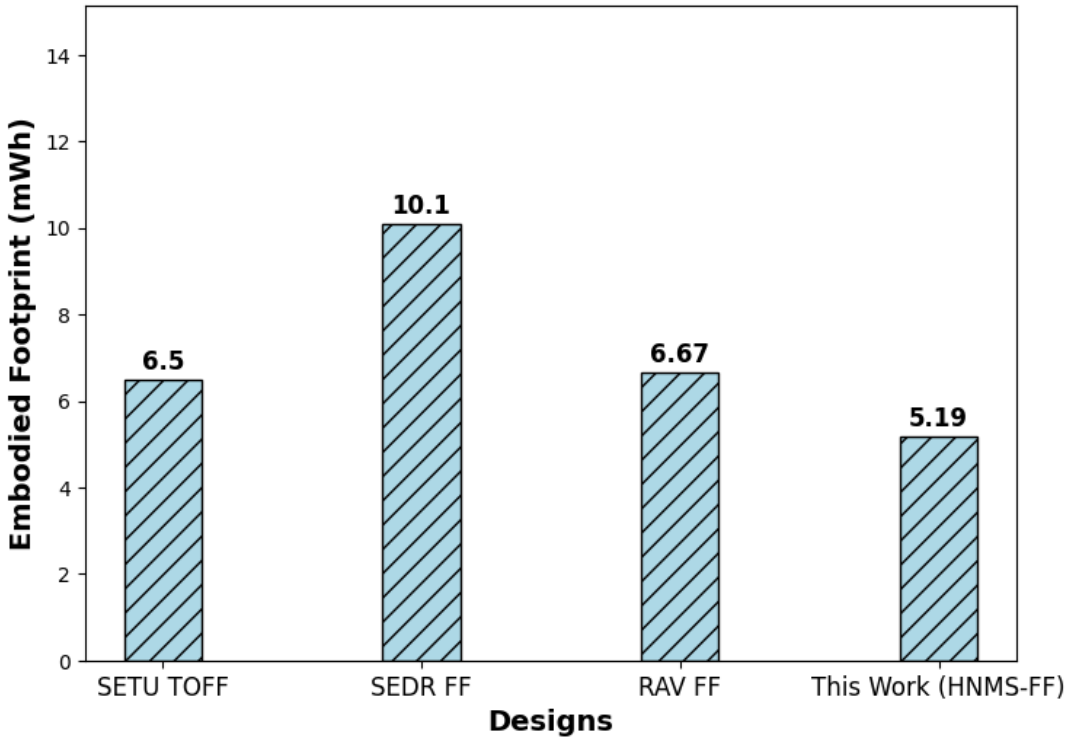

Figure 5.1: Embodied Carbon Footprint Metric (eCFP) comparison for SETU-FF, SEDR-FF, RAV-FF and HNMS-FF designs.

Embodied Carbon Footprint Metric Analysis in Fig. 5.1. illustrates the embodied carbon footprint of various radiation-hardened flip-flop designs, comparing their manufacturing energy footprints. This metric reflects the environmental cost of fabrication and is mainly influenced by the layout area and additional process requirements. As seen in the Table 1, SEDR-FF, having the largest layout area, exhibits the highest embodied footprint (10.10 mWh). Interestingly, SETU-FF, despite having a slightly larger area than RAV-FF, shows a lower embodied metric (6.50 mWh), likely because if RAV-FF incorporates trench-capacitor process steps that increase energy cost even with a smaller layout footprint (6.67 mWh). Among all, the HNMS-FF achieves the lowest embodied footprint (5.19 mWh), due to its compact layout and absence of complex fabrication requirements. These results emphasize that while layout area remains a dominant factor in embodied energy, minimizing additional process steps can significantly enhance sustainability.

Therefore, the HNMS-FF not only offers improved reliability but also contributes positively from an environmental perspective. These insights can guide future design decisions where both radiation hardness and sustainability are critical requirements.

5.2 Operational Carbon Footprint Metric (oCFP)

The operational carbon footprint metric evaluates the energy consumed over the device's operational lifetime. It is expressed as:

$$\text{oCFP} = T_{\text{total}} \times (P_{\text{dynamic}} + P_{\text{leakage}}) \tag{5.4}$$

Dynamic power is calculated as:

$$P_{\text{dynamic}} = Q_{\text{dyn}} \times \alpha \times V_{\text{active}} \times f \times \text{ATR} \tag{5.5}$$

where Q_{dyn} is the dynamic charge per switching event, α is the activity factor, V_{active} is the active supply voltage, f is the frequency, and ATR is the Active Time Ratio.

Leakage power is given by:

$$P_{\text{leakage}} = I_{\text{active}} V_{\text{active}} \frac{T_{\text{active}}}{T_{\text{total}}} + I_{\text{standby}} V_{\text{standby}} \frac{T_{\text{standby}}}{T_{\text{total}}} \tag{5.6}$$

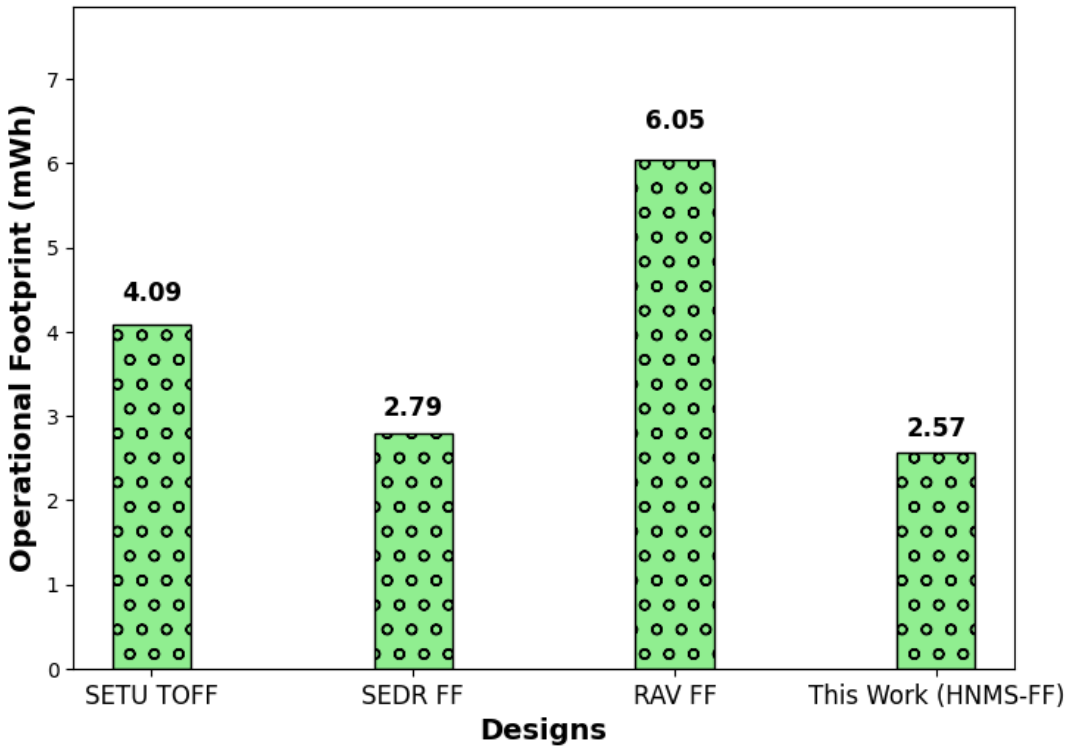

Figure 5.2: Operational Carbon Footprint Metric (oCFP) comparison for SETU-FF, SEDR-FF, RAV-FF and HNMS-FF designs.

Operational Carbon Footprint Metric Analysis in Fig. 5.2. illustrates the operational foot-

print of four different flip-flop designs, reflecting the energy consumed during their actual usage. This metric depends on both dynamic and leakage power characteristics, which in turn are influenced by the circuit's internal switching activity, operating frequency, and total runtime. In this analysis, a consistent activity factor ($\alpha = 0.1$), operating frequency (500 MHz), and run time were applied across all designs to ensure a fair comparison.

From the graph, it is evident that RAV-FF exhibits the highest operational footprint (6.05 mWh), attributed to its higher dynamic power and extra capacitive elements. On the other hand, SETU-FF and SEDR-FF show moderate operational footprints (4.09 mWh and 2.79 mWh, respectively). The HNMS-FF demonstrates the lowest operational energy consumption among all (2.57 mWh), indicating its optimized architecture that reduces both switching activity and leakage paths.

Thus, from a usage perspective, the HNMS-FF proves to be the most sustainable choice. The results suggest that optimizing both the dynamic and leakage components is essential in minimizing operational energy.

5.3 Total Carbon Footprint

Fig. 5.3. presents the total carbon footprint—comprising both embodied and operational contributions—for each of the four flip-flop design.

As shown in Fig. 5.3, the Hardened Node Master-Slave Flip-Flop (HNMS-FF) achieves the lowest total footprint at 7.76 mWh, significantly outperforming SETU-FF (10.59 mWh), RAV-FF (12.72 mWh), and SEDR-FF (12.89 mWh). The relatively high embodied footprint of SEDR-FF and the elevated operational footprint of RAV-FF lead to their larger overall footprints. By contrast, HNMS-FF balances minimized layout complexity with efficient dynamic operation—resulting in the most sustainable design among those evaluated. This demonstrates that HNMS-FF not only improves radiation hardening but also delivers superior lifecycle energy performance compared to existing architectures.

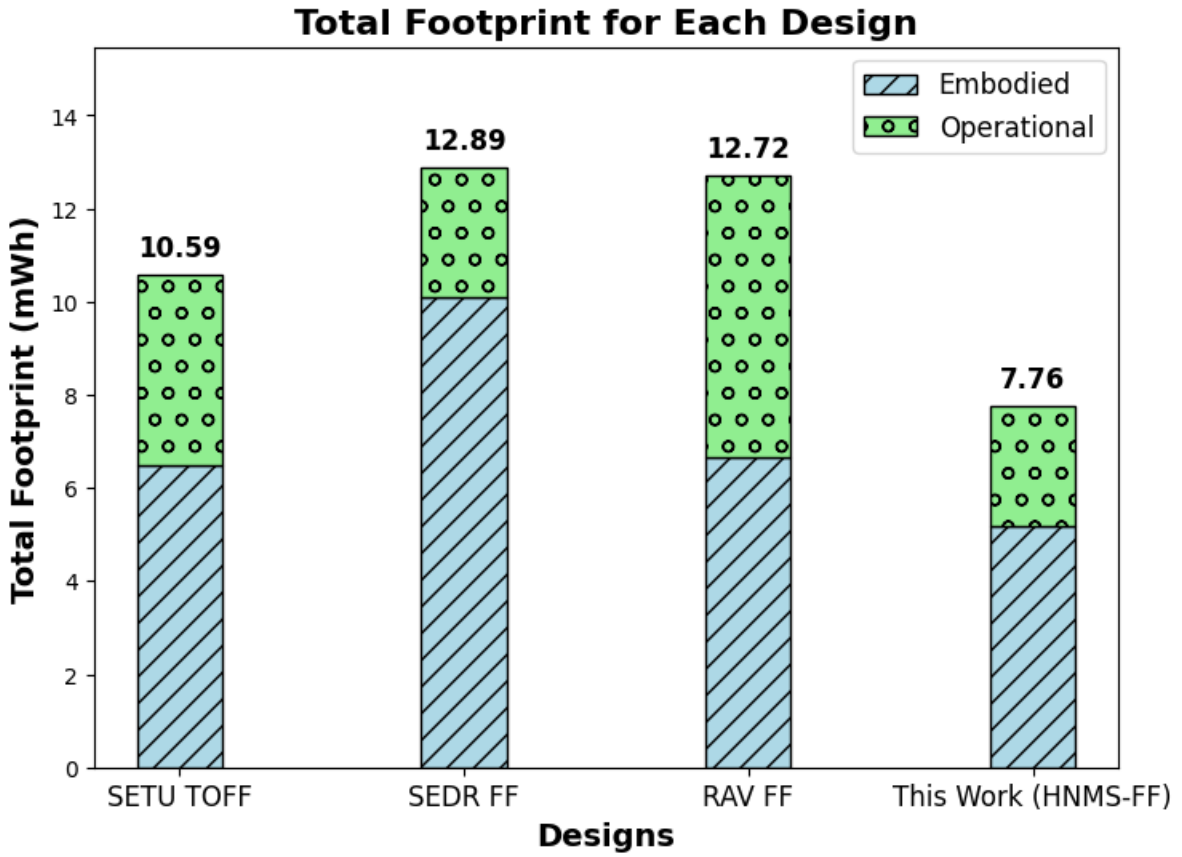

Figure 5.3: Total energy footprint (eCFP + oCFP) for SETU-FF, SEDR-FF, RAV-FF and HNMS-FF designs.

The comparative analysis of total carbon footprint (CFP) for various flip-flop designs at two operating frequencies—500MHz (Case A) and 100MHz (Case B)—reveals distinct trends in the contributions of operational and embodied components (shown in Fig. 5.4). In Case A, where the frequency is 500MHz, operational CFP (oCFP) dominates the total footprint due to increased dynamic power consumption, which scales with both switching activity and frequency. This results in higher oCFP values for designs like SEDR FF and RAV FF, pushing their total CFP to 12.89mWh and 12.72mWh, respectively. The proposed HNMS+FF design, however, demonstrates superior energy efficiency, achieving the lowest total CFP of 7.76mWh despite operating at the same frequency.

In Case B, at a lower frequency of 100MHz, the influence of dynamic power diminishes and leakage power becomes the dominant contributor to oCFP. Consequently, the embodied CFP (eCFP) becomes more significant in the total footprint. Here, although the oCFP of SEDR FF is slightly lower than that of HNMS+FF due to reduced dynamic activity, its higher leakage current and substantial embodied footprint result in a total CFP of 10.81mWh—much higher than the 6.04mWh observed for the proposed design. This underscores the importance of minimizing both leakage and embodied energy in low-power applications such as IoT, where frequency and activity factors are low.

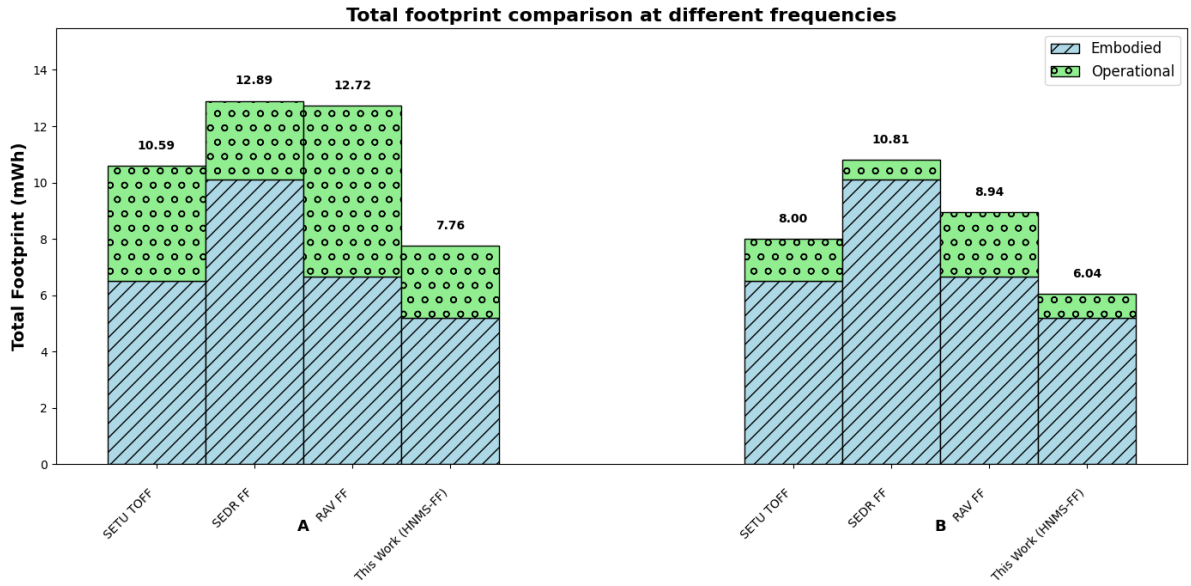

Figure 5.4: Total footprint comparison at different frequencies for various flip-flop designs. The chart distinguishes between embodied (eCFP) and operational (oCFP) carbon footprints across two cases: (A) 500MHz and (B) 100MHz.

Overall, the data highlights that while high-frequency designs are mainly impacted by operational energy, low-frequency scenarios emphasize the role of embodied energy and leakage power. The proposed HNMS+FF flip-flop proves to be more sustainable across both cases by offering lower total CFP, driven by architectural optimizations that reduce both dynamic and static energy use as well as fabrication-related impact.

CHAPTER 6

Conclusion and Future Directions

This work addresses the dual challenges of radiation resilience and sustainability in modern integrated circuit design. The proposed flip-flop demonstrates enhanced robustness against radiation-induced faults while achieving notable improvements in power and area efficiency compared to conventional designs. By introducing the Power, Performance, Area, and Sustainability (PPAS) framework, this study offers a holistic method for evaluating circuit designs not only by their functional performance but also by their environmental impact.

The PPAS framework brings a much-needed shift in evaluation practices by incorporating both fabrication-related (embodied) and operational energy considerations. The proposed design is shown to consistently lower environmental impact, achieving around **3**3% reduction in total carbon footprint and around **2**0% improvement in LET threshold compared to baseline designs. These results make it a strong candidate for dependable applications where both reliability and sustainability are critical.

However, these improvements come at the cost of performance, compared to the reference design. Despite this trade-off, the overall benefits in resilience and sustainability justify its use in eco-conscious, safety-critical systems.

Overall, this work emphasizes the importance of early-stage sustainability-aware design decisions. It bridges the gap between fault tolerance and eco-friendly VLSI development, paving the way for integrated circuits that meet rigorous dependability standards while contributing to environmentally responsible engineering.

Future Directions

While this work demonstrates significant advancements in radiation-hardened and sustainable flip-flop design, several promising avenues remain unexplored. Future research should focus on extending the PPAS framework to more advanced process nodes, where leakage currents and process variations pose new challenges to both reliability and sustainability. Additionally, developing EDA tools with built-in PPAS optimization could enable widespread adoption by automating eco-conscious design decisions during synthesis and physical implementation. Further exploration of 3D-IC integration and standardized sustainability benchmarks for radiation-tolerant circuits would strengthen the industry's ability to balance environmental impact with mission-critical performance requirements.

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List of papers based on Thesis

1. Alam, F., Grover, A. “Sustainable Radiation-Hardened Flip-Flop Design Using PPAS Framework” [In Preparation]

2. A. Grover, A. Jain, N. M. Khan, T. G. Rao, F. Alam, and P. Kumar, “Sustainability framework for computing element design" [Accepted]