Impact of Charge Pump Design Choices on Sustainability for IoT Applications

by

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Impact of Charge Pump Design Choices on Sustainability for IoT Applications

A Thesis Report

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Abhishek Chaurasiya

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Certificate

This is to certify that the thesis titled "**Impact of Charge Pump Design Choices on Sustainability for IoT Applications**" being submitted by **Abhishek Chaurasiya**, to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of **Master of Technology**, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Abstract

This work presents a comprehensive study on the design, implementation, and sustainability assessment of a modified version of a Dickson charge pump circuit. The circuit is implemented to operate at $1.2\,\mathrm{V}$ and achieves an output of $3.6\,\mathrm{V}$ used for Internet of Things (IoT) applications. The design is implemented for two different load conditions- a lighter load of $1\,\mu\mathrm{A}$ and a slightly heavier load of $50\,\mu\mathrm{A}$. Conventional performance metrics are calculated and compared to observe the electrical behavior of both designs. In addition, this work uses a novel sustainability-aware framework to account for the carbon emissions involved. The Embodied Carbon Footprint (eCFP) metric accounts for the fabrication-related emissions, while the Operational Carbon Footprint (oCFP) metric captures the emissions during the operation of the design over its lifecycle. This work benchmarks both electrical and sustainability indicators to analyze the impact of design choices on sustainability and offers a trade-off between performance and carbon footprint for a design.

Keywords: Dickson Charge Pump, Internet of Thing (IoT), System-on-Chip (SoC), Embodied Carbon Footprint, Operational Carbon Footprint

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Abbreviations

IIITD	Indraprastha Institute of Information Technology Delhi
SoC	System on Chip
CMOS	Complementary Metal Oxide Semiconductor
IoT	Internet of Things
ICs	Integrated Circuits
PCE	Power Conversion Efficiency
eCFP	Embodied Carbon Footprint
oCFP	Operational Carbon Footprint
MIMCAP	Metal Insulator Metal Capacitor
MOSCAP	Metal Oxide Semiconductor Capacitor
CMP	Chemical Mechanical Planarization
DPQ	Dynamic Power Quantity
SPQ	Static Power Quantity
LPQ	Leakage Power Quantity

Notation

μ	Micron
α	Activity Factor
MHz	Mega Hertz
kWh	Kilo Watt Hour

CHAPTER 1

Introduction

1.1 Motivation

In the age of rapid technological advancement in modern electronics, the demand for compact, energy-efficient, low-power, portable Internet of Things (IoT) based systems has increased significantly. This demand fueled the need for complex semiconductor integrated circuits (ICs) with on-chip voltage conversion capabilities. These systems require multiple voltage domains to perform different operations, which require voltages higher than the input voltage levels to drive their internal circuitry. Charge Pump circuits are DC-DC converters that use switched-capacitor techniques to increase or decrease the given input voltage level. These circuits are smaller in size and do not need bulky off-chip inductors, making them ideal for use in System-on-Chip (SoC).

While power, performance, and area (PPA) remain critical metrics for any electronic design, the sustainability of a design equally remains significant, especially when there is a significant environmental impact on semiconductor manufacturing. A comprehensive sustainability assessment of a design comprises estimating its overall carbon footprint, including the emissions generated during its fabrication process and the emissions accounted for during design deployment.

1.2 Circuit

In this work, a 2-stage modified Dickson charge pump design [1] is utilized as shown in Fig. 1.1 to observe its behavior under varying load conditions. A lighter load of $1\,\mu$A (*stage_2_1u*) and a slightly heavier load of $50\,\mu$A (*stage_2_50u*) are used as the output load current for the operation by varying the transistor size and operating clock frequency (f_{op}), keeping all other design parameters the same for both cases. Table (1.1) presents the optimized transistor sizing for both the implemented designs. A 50% duty cycle is maintained for both CLK and CLKB signals. Proper transistor sizing and optimal frequency adjustment ensure better pump-up speed, better PCE, and stable output voltage levels.

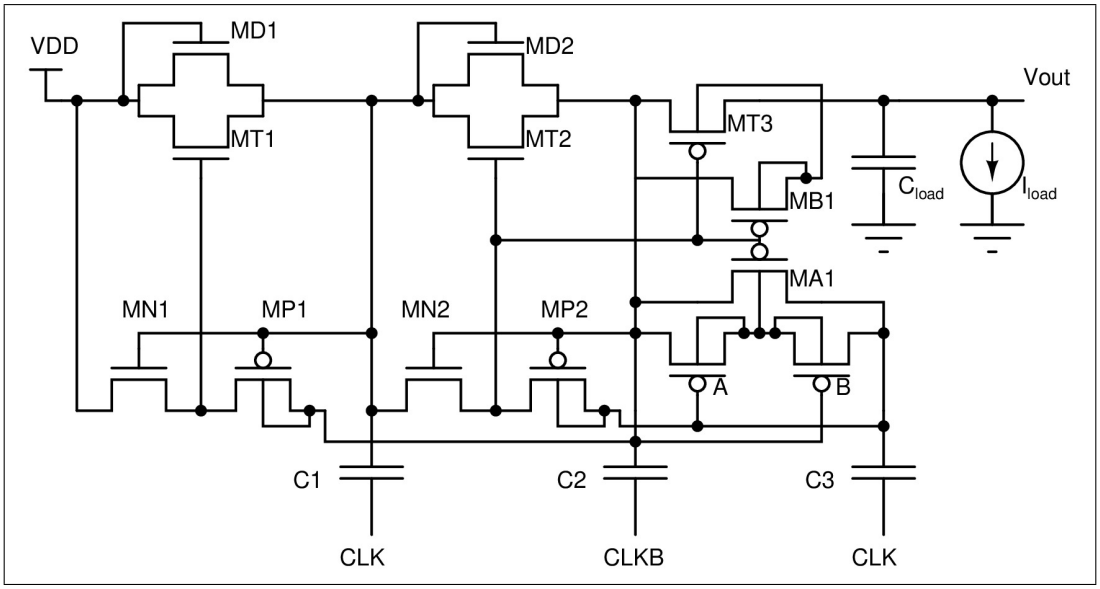


Figure 1.1: 2-stage modified Dickson Charge Pump Circuit

Table 1.1: Transistor Dimensions for 2-stage Charge Pump Designs with $1\ \mu$A and $50\ \mu$A load

MOS Transistor	**stage_2_1u**		**stage_2_50u**	
	Width W (μm)	Length L (μm)	Width W (μm)	Length L (μm)
MD#	0.42	0.06	2.1	0.06
MT# (NMOS)	0.42	0.06	2.1	0.06
MT# (PMOS)	0.42	0.06	2.4	0.06
MN#	0.3	0.06	1.2	0.06
MP#	0.3	0.06	0.72	0.06
A	0.3	0.06	0.84	0.06
B	0.3	0.06	0.84	0.06
MA1	0.3	0.06	0.3	0.06
MB1	0.3	0.06	0.3	0.06

CHAPTER 2

Background and Related Work

In recent times, the evolution of the semiconductor industry has been fueled by device scaling and performance enhancement techniques. Complex System-on-Chips (SoCs) are designed to focus on area and cost optimization. This rapid progress often comes at the cost of significant environmental impact. It involves the emission of device shrinking, which adds more complexity to the fabrication of integrated circuits (ICs), leading to a surge in their carbon footprint. The rapidly increasing emissions threaten the benefits of employing IoT-based systems if they remain unaddressed.

Employing modern semiconductor fabrication techniques such as FinFETs, UTBB FDSOI substrates [2], multi-patterning lithography [3], and extreme ultraviolet (EUV) process [4] to manufacture complex and performance-oriented chips demands an enormous amount of water and rare-earth-like raw materials, raising serious environmental concerns. For instance, enormous fabrication facilities like TSMC consume more electricity annually than the entire country of Sri Lanka [5]. As a result, semiconductor manufacturing contributes significantly to the emission of global greenhouse gases (GHG).

Efforts to reduce emissions in this field are visible, and the sustainability goal is to reach net-zero emissions. However, current sustainability practices target the emissions during the manufacturing stage [6]-[8], leaving a significant gap at the design phase. Carbon tracking methods exist under the Greenhouse Gas Protocol, classifying emissions into three scopes [9]:

- **Scope 1:** It accounts for the direct emissions generated due to the use of facility resources, fuel combustion, etc.
- **Scope 2:** It covers the carbon emissions from the energy consumed to operate the fabrication facilities and data centers.
- **Scope 3:** It accounts for the emissions generated in order to maintain the supply chain and other logistics.

Historically, the existing metrics focused on evaluating and comparing power, performance, and area (PPA). The existing metrics fail to provide design-specific sustainability assessments. The sustainability of an IC depends not only on the emissions during its fabrication but also on the design practices employed while designing the layout. Apart from the manufacturing phase, there is no metric to evaluate the emissions during the design's operational lifetime. Such a metric that accounts for the emissions during the design and the deployment phase is needed.

The charge pump design is a suitable choice to analyze in this work due to its voltage scaling abilities. [10] provides a deeper understanding of a charge pump circuit behavior by employing optimized design strategies and topologies.

In today's world, charge pump circuits are widely used in various applications. Radiofrequency identification (RFID) tags using non-volatile memories (NVMe) [11] like EEPROM and Flash extensively use charge pumps to generate higher programming voltages [12]-[14]. AMOLED display driver ICs [15] use charge pumps to pixel arrays. Charge pumps assist in boosting the input voltages used in energy harvesting systems [16]-[18]. The charge pump circuit plays a crucial role in IoT applications [19]-[21] by boosting the supply voltage for proper operation.

Charge pumps are broadly categorized into two topologies – Dickson and Voltage Doubler-based. Voltage Doublers require a larger pumping capacitor, causing a much larger overhead area during fabrication. It also suffers from higher voltage ripple and is sensitive to the parasitic effects under a smaller load. Hence, the Dickson charge pump is used for analysis in this work, targeting IoT-based applications. It is designed using a combination of a pumping capacitor and a diode-connected transistor, which is used as a charge transfer switch (CTS). This arrangement reduces voltage ripple, improves load regulation, and distributes voltage gain across stages. This thesis work uses a modified version of a high-speed Dickson Charge Pump design [1], providing better Power Conversion Efficiency (PCE), lower voltage ripple, reduced parasitic effect, and improved ramp-up speed.

In addition to the evaluation of traditional performance metrics, this work also provides an analysis of the sustainability aspect of the design. We introduced a novel Carbon Footprint (CFP) framework- the Embodied Carbon Footprint (eCFP) metric, evaluating the emissions in terms of the fabrication cost and raw materials used, and the Operational Carbon Footprint (oCFP) metric, accounting for the emissions by the total energy consumed during its lifetime of operation. By analyzing both the footprint metrics as proposed, this work discusses the impact of the design choices on the overall sustainability of the design.

CHAPTER 3

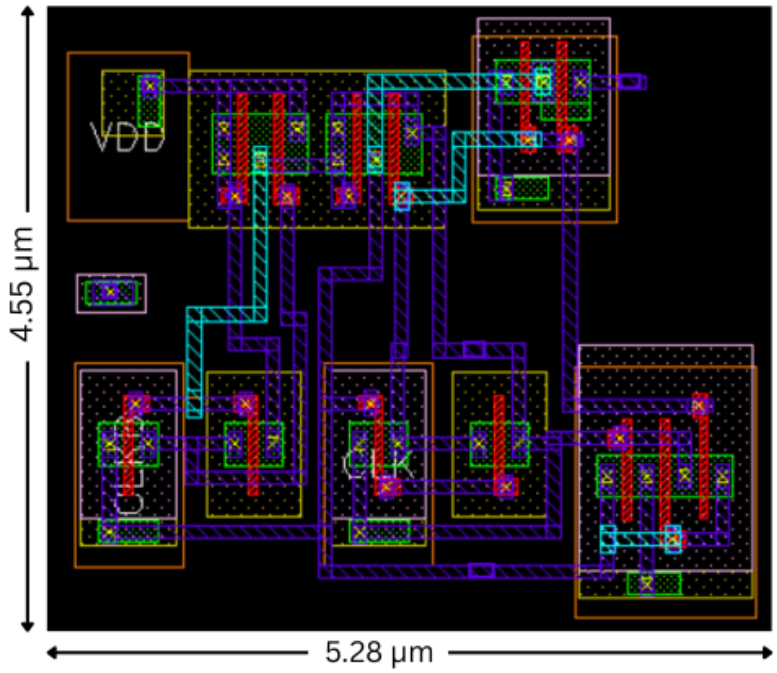
Post-Layout Analysis

The post-layout simulation results are shown in this section. Table (3.1) shows all the design parameters chosen for both simulation designs. ELDO simulations are performed under a nominal (typical-typical) process and high temperature ($125\,^{\circ}\mathrm{C}$) to evaluate the conventional performance parameters.

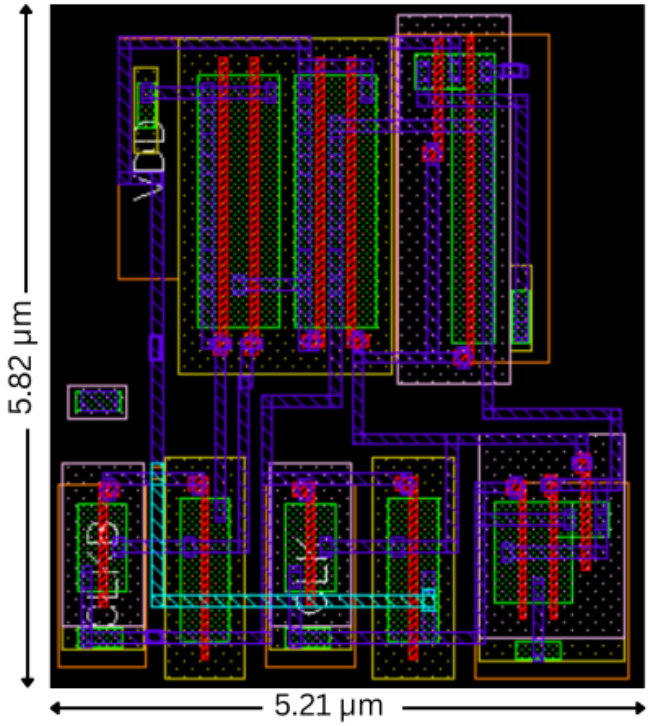
Table 3.1: Design Parameters for 2-stage Charge pump with $1\,\mu$A and $50\,\mu$A load Configurations

Design Parameters	**stage_2_1u**	**stage_2_50u**
Input Supply (VDD)	1.2 V	1.2 V
Pumping Capacitor (C_{pump})	10 pF	10 pF
Auxiliary Capacitor (C_{aux})	0.2 pF	0.2 pF
Operating Frequency (f_{op})	50 MHz	100 MHz
Load Capacitor (C_{load})	20 pF	20 pF
Load Current (I_{load})	$1\,\mu$A	$50\,\mu$A

3.1 Charge Pump Design Layouts

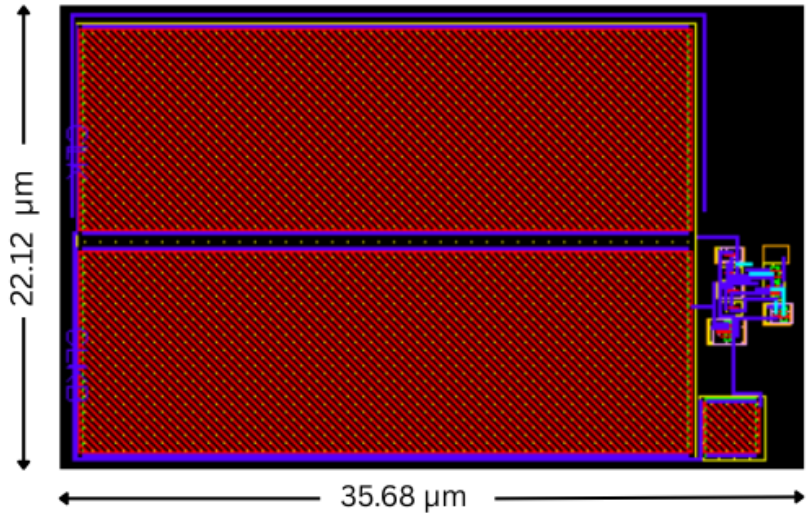


(a)

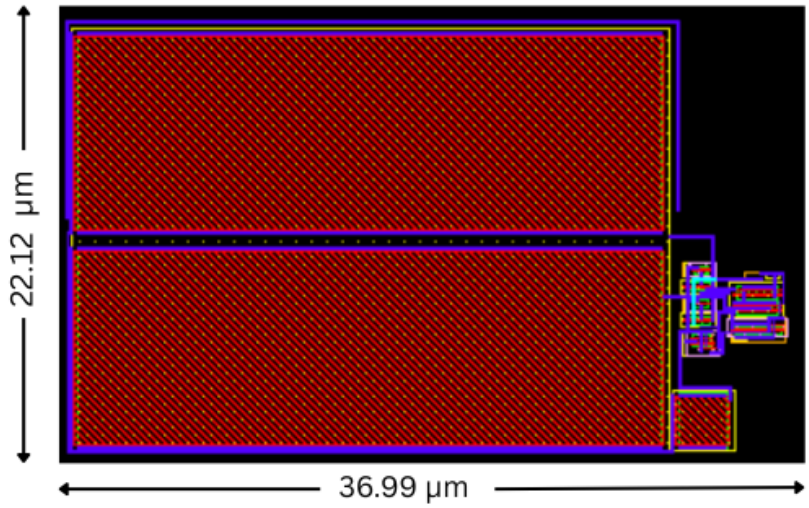


(b)

Figure 3.1: Layout of 2-Stage MIMCAP-based Charge Pump design with (a) 1 μA load (b) 50 μA load.



(a)



(b)

Figure 3.2: Layout of 2-Stage MOSCAP-based Charge Pump design with (a) $1\,\mu$A load (b) $50\,\mu$A load.

3.2 Output Voltage

Fig. 3.3 shows the peak output voltage level comparison between the two designs in a 2-stage circuit. *stage_2_1u* design has almost 99% voltage transferability, while *stage_2_50u* design has 91% voltage transferability. The output voltage level drops when driving a slightly heavy load ($50\,\mu$A) as compared to the lighter load ($1\,\mu$A). Ideally, the output voltage (V_{out}) is expressed in Eq (3.1) as:

$$V_{\text{out}} = (\text{N} + 1) \times \text{VDD} \tag{3.1}$$

3.3 Ramp-up Time

It is the time when the output rises to 90% of the steady-state output value from the reference voltage (VDD). The *stage_2_50u* design has a 57.5% lower ramp-up time than the *stage_2_1u* design. This is because the circuit driving a higher load has wider transfer transistors than the circuit driving a lighter load. The *stage_2_50u* design also has a shorter ramp-up time than the reference design for a 2-stage implementation. Fig. 3.4 shows the comparison of ramp-up time between the two implemented designs and the reference design.

3.4 Power Conversion Efficiency

The implemented charge pump configuration reduces parasitic losses and improves the charge transfer efficiency. PCE also depends on the output load conditions. The *stage_2_1u* design has much lower efficiency than the *stage_2_50u* design. In this work, PCE is calculated in terms of charge transfer taking into account the total charge at the output (Q_{out}) and the total charge injected (Q_{in}) in the circuit. Fig. 3.5 illustrates the PCE comparison between the implemented and reference designs. The implemented design achieves an efficiency of approximately 8.4% higher than the original design under a $50\,\mu$A load condition.

3.5 Peak to Peak Output Ripple Voltage

In charge pump circuits, the peak-to-peak voltage ripple refers to the voltage fluctuations observed at the output during the steady state. It arises due to non-ideal behavior in capacitor switching, clock signal transitions (CLK & CLKB), and the current load used in the charging/discharging phase. It is observed that as the load on the circuit increases, fluctuations become more dominant. Within the implemented designs, *stage_2_1u* has extremely lesser peak

output ripple than *stage_2_50u* and the reference design as shown in Fig. 3.6. Despite incorporating wider transfer transistors, the *stage_2_50u* design exhibits larger voltage fluctuations due to the increased load and limitations of proportionate scaling in critical design specifications such as pumping (C_{pump}) and auxiliary (C_{aux}) capacitors. These capacitors are essential for replenishing the charge during operation. Consequently, this results in a greater peak-to-peak voltage ripple in the *stage_2_50u* design. In contrast, the implemented $1\ \mu$A load design shows a 26.92% reduction in ripple compared to the zero load reference design as shown in Fig. 3.6.

Table(3.2) presents the FoM comparison among the implemented and the reference designs.

Table 3.2: Comparison of Figures of Merits (FoMs) for implemented 2-stage charge pump designs with $1\ \mu$A and $50\ \mu$A load and the Reference Design

Figure of Merits (FoMs)	**stage_2_1u**	**stage_2_50u**	**Ref. Design**
Output Voltage (V)	3.55	3.27	3.50
Ramp-up Time (µs)	0.66	0.28	0.40
Power Conversion Efficiency (PCE)	10.11%	91.10%	84%
Output Ripple Voltage (mV)	0.95	14.00	1.30

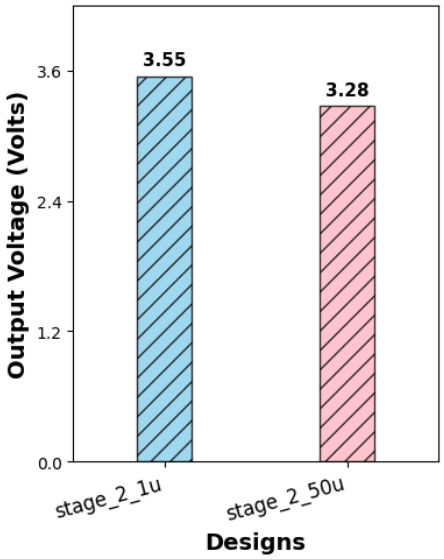


Figure 3.3: Output voltage comparison of implemented 2-stage Dickson Charge Pump Design

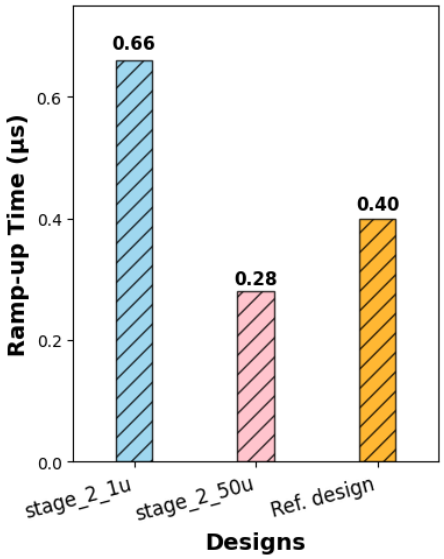


Figure 3.4: Ramp-up time comparison of the implemented and the reference 2-stage Dickson Charge Pump Design

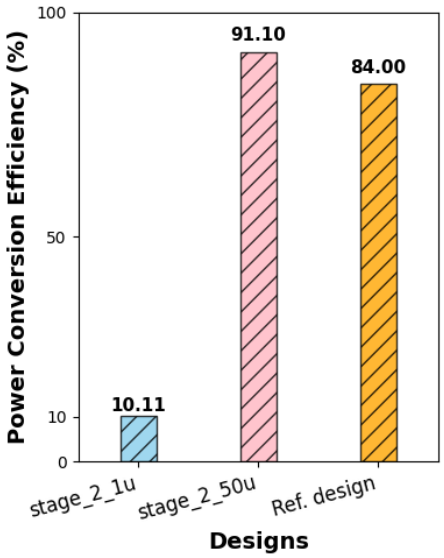


Figure 3.5: Power Conversion Efficiency comparison of the implemented and the reference 2-stage Dickson Charge Pump Design

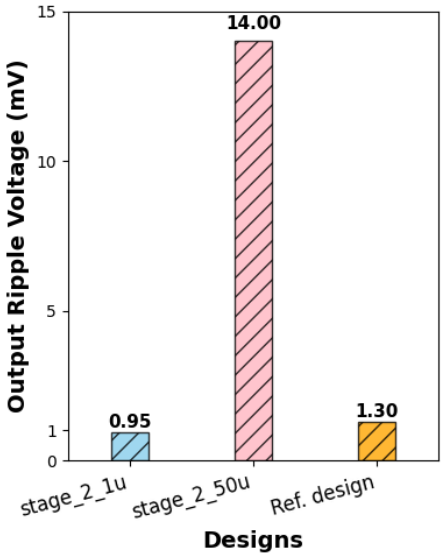


Figure 3.6: Output Ripple Voltage comparison of the implemented and the reference 2-stage Dickson Charge Pump Design

CHAPTER 4

Sustainability metric and analysis on circuit

The proposed sustainability framework comprises the embodied carbon footprint (eCFP) and the operational carbon footprint (oCFP) metrics. Carbon emissions related to the manufacturing of a chip fall under the eCFP, while the emissions incurred during chip deployment are evaluated using the oCFP. Combining the energy-equivalent emission from both metrics, we estimate the total carbon footprint (tCFP) associated with a design.

Emissions may vary with the technology node used, the complexity of the design, the application for which the design is produced, and the source of energy supplied to the manufacturing facility. This novel framework assists SoC designers in choosing between the design alternatives based on the circuit's total environmental cost.

The focus of this thesis is on the application of this framework to the Dickson Charge Pump circuit used for IoT applications.

4.1 Embodied Carbon Footprint

Due to increasing demand, modern IoT-based semiconductor devices need to be manufactured in billions. This requires a huge amount of energy for its fabrication. Hence, there is a need for a sustainability metric, such as the embodied carbon footprint (eCFP), that considers the environmental impact of the design during fabrication. It is calculated in kilowatt-hours (kWh) per IP and is expressed in Eq (4.1) as:

$$\begin{aligned} \text{eCFP} = \quad & \text{Energy Consumption per IP} \\ & \times \text{Mask Overhead} \\ & \times \text{Congestion Penalty Factor} \end{aligned} \tag{4.1}$$

- **Energy Consumption per IP-**

  This is calculated by taking the energy used to process a wafer per unit of wafer area multiplied by the IP area. It is calculated in kilowatt-hours (kWh) and is expressed by Eq (4.2) as:

$$\text{Energy per IP} = \left(\frac{\text{Energy of wafer in kWh}}{\text{Area of wafer}} \right) \times \text{Area of IP} \tag{4.2}$$

- **Mask Overhead-**

  The use of additional masks leads to extra effort in the fabrication process. In a standard process, the number of masks required is defined. The use of additional masks leads to an increase in the eCFP of a design. Additional masks are required when using different V_t devices or different capacitor types (MOSCAP or MIMCAP). A mask overhead factor is introduced in the eCFP metric to account for the emissions due to the use of extra masks. It is calculated in Eq (4.3) as:

$$\text{Mask Overhead} = ((\text{Total Mask} - \text{Ref. Mask}) \times \text{MF} + 1) \tag{4.3}$$

  Here, Total Mask refers to the number of available masks in a given process, Ref. Mask refers to the number of masks used as a reference in a design. The mask factor (MF) data is taken from [8] with $MF = 0.045$, suggesting a 4.5% increase in the energy consumed per additional mask. This incremental energy is constant for any kind of mask related to the process. The data also shows roughly 18% rise in energy consumption when increase the metal stack from 6 to 8 layers.

- **Congestion Penalty Factor-**

  Usually, designs are limited to utilizing only the first metal layer while higher metal layers are used for signal routing. Using a second metal layer in a design may result in a decrease in the availability of routing resources. This can lead to increased congestion at the SoC level. The congestion penalty factor is calculated in Eq (4.4) as:

$$\text{CPF} = 1 + \left(\frac{\text{Total No. of Tracks}}{\text{Number of Tracks Left}} - 1 \right) \times \text{CF}_1 \tag{4.4}$$

  The total number of tracks means the total number of possible routing tracks in the lowest metal layer for a SoC design. The number of tracks left refers to the number of routing tracks that are actually available for routing. The Congestion Factor (CF) is added to quantify the eCFP for a design.

Evaluation of eCFP for the charge pump designs implemented in this work majorly depends upon the active silicon area of design, type of capacitors used, and fabrication efforts in terms of mask overhead and congestion factor in terms of the number of higher metal layers used while designing the layout.

4.1.1 Active Area

The area is one of the critical factors in IoT devices due to their miniature sizes and ultra-dense multi-purpose SoCs. We observed a 13% area improvement while designing the custom charge pump layout using M1 & M2 metal layers compared to the layout using only the M1 layer. This significant area improvement leads to lower energy consumption per IP design, contributing to reduced eCFP.

A typical layout of the implemented 2-stage Dickson charge pump is designed using only a single metal layer, as shown in Fig. 4.1, which shows the spacing between two PMOS stacks

with separate NWELL(NW). The separate NW ensures separate transistor body biasing for the designed PMOS stacks. There is a minimum of 1-micron spacing between adjacent NW regions, ensuring compliance with the design rule check (DRC) constraints. This spacing between two NW regions arises due to the limitation of using only a single metal layer, leading to the unoptimized transistor placement. The extra spacing results in an increased layout area. To compensate for the extra spacing without violating DRC rules, Fig. 4.2 utilizes the M1 and M2 layers to design the charge pump layout. Using the M2 layer ensures optimized transistor placement, eliminating the need for extra spacing between two NW regions. An NMOS transistor stack is placed in the empty region between two PMOS stacks. This leads to a smaller area footprint than the layout designed using only the M1 metal layer.

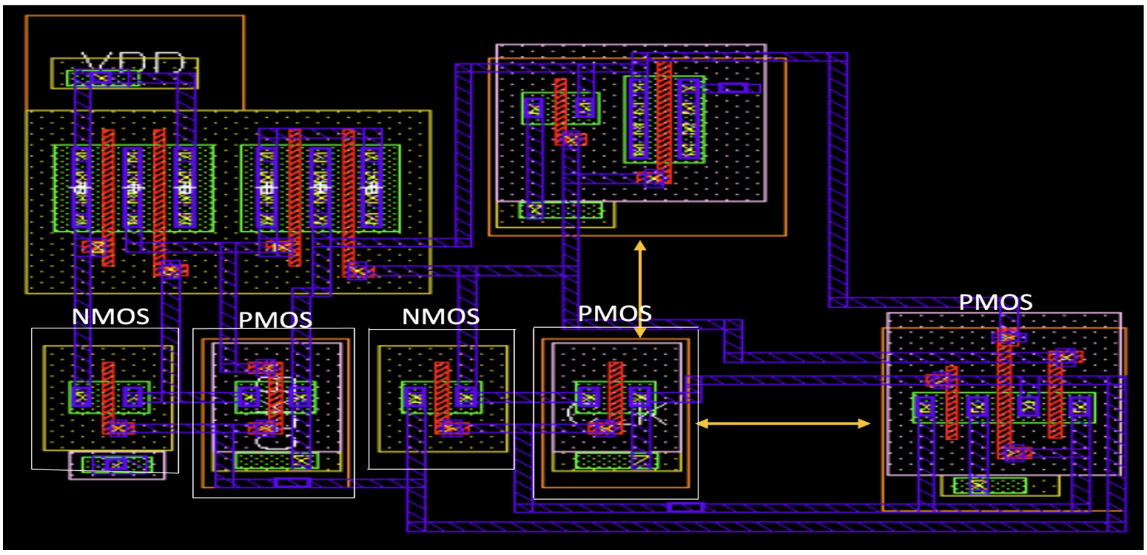


Figure 4.1: Layout of an implemented 2-stage Dickson Charge Pump Design using only M1 metal layer

In this work, *stage_2_1u* and *stage_2_50u* designs are implemented using both MOSCAP and MIMCAP, as shown in Fig. 3.1 and 3.2. MOSCAP-based design occupies a huge silicon area while MIMCAP-based design occupies very little area. MIMCAPs do not consume active silicon area and utilize higher metal layers to generate the capacitance. Fig. 4.3 includes the area comparison between both designs, highlighting a significant area recovery in MIMCAP-based designs.

4.1.2 Impact of Capacitor Selection

As the chip becomes more complex, the number of charge pump instances also increases. High-end IoT SoCs with multiple voltage domains used in embedded NVMe, RF Communi-

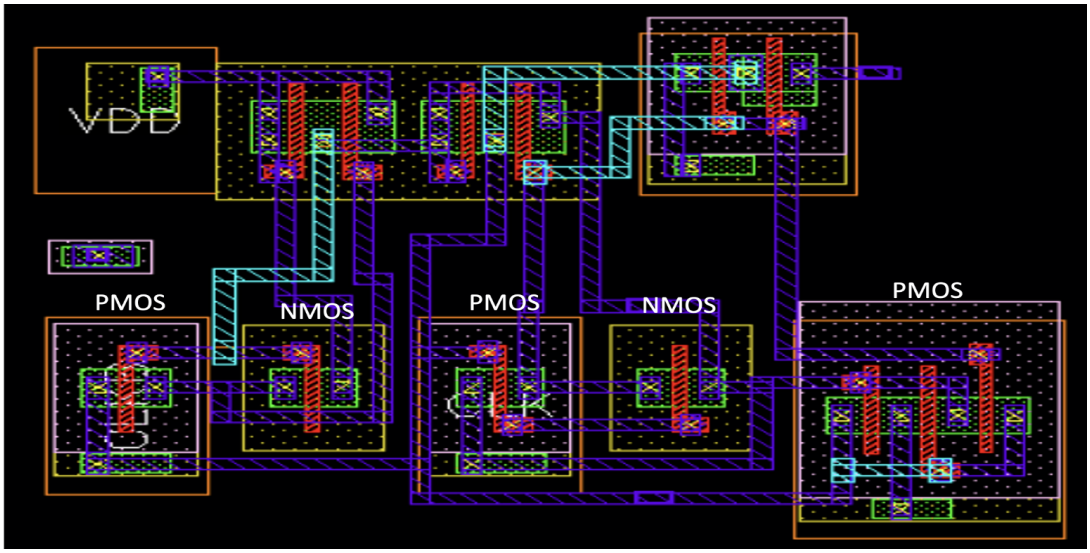


Figure 4.2: Layout of an implemented 2-stage Dickson Charge Pump Design using both M1 and M2 metal layers

Table 4.1: Capacitor Type Selection Based on Chip Area and Instance Count

Chip Area (in mm^2)	Number of Pumps used	Total Pump Area (in mm^2)	% Area Occupied	Capacitor Suggestion
2	1	0.030	1.51	MIMCAP
2	4	0.121	6.07	MIMCAP
5	1	0.818	16.36	MOSCAP
20	4	3.272	16.36	MOSCAP

cations, etc., require multiple pump instances. Simple IoT sensors and control units, including wearable and biomedical SoCs, require one or two pump instances only. Capacitor selection becomes critical with the addition of each instance as it directly influences on-chip silicon area, fabrication complexity, and cost. [22] considers the design trade-offs while selecting between MOSCAP and MIMCAP to be used in a design. MIMCAPs exhibit lower parasitics than MOSCAPs; hence, they are favourable for compact and efficient charge pump designs.

Table 4.1 shows the suggested capacitor type based on the assumed chip area and the number of charge pump instances used. Assuming an extreme case, we fed the area of *stage_2_50u* design with a maximum of 4 pump instances.

The data in the table shows that when the SoC area is constrained and the number of pumps used is in the range of 1-4, then MIMCAP-based pumps should be used as they occupy less chip area. When area is not the primary concern and the focus is on cost and process simplicity, MOSCAP-based pumps should be used. Hence, maintaining a proper trade-off between the SoC area and the number of pump instances used is critical to capacitor type selection.

Table 4.2: Post-layout simulation results of the eCFP of implemented 2-stage MOSCAP and MIMCAP-based charge pump designs with $1\,\mu$A and $50\,\mu$A current load.

Design	**IP Area** (μm^2)	**Ref. Masks**	**Extra Masks**	**Total Masks**	**# M2 Tracks**	**# Metal Tracks in Porous Layer**	**Embodied CFP** (mWh/IP)
stage_2_1u_mim	24.024	36	2	38	26	10	1.85
stage_2_50u_mim	30.348	36	2	38	29	6	2.12
stage_2_1u_mos	789.2416	36	0	36	26	10	55.76
stage_2_50u_mos	818.3294	36	0	36	29	6	52.50

4.1.3 Fabrication Efforts

MOSCAP-based pumps are area-hungry but fabrication-friendly. On other hand, MIMCAP-based pumps consume very little silicon area but require a complex fabrication process and additional mask costs. With the use of MIMCAP-based pumps, as the instance count increases, it poses the challenge in terms of increased cost, fabrication complexity, extra masks used, and reduced yield & reliability. In this work, 2 extra masks were utilized to integrate MIMCAPs as per standard industry practices. Requiring additional masks, tighter control on dielectric thickness, uniform inter-metal spacing, a dedicated Chemical Mechanical Planarization (CMP) process, and extra area required for shielding from noise and parasitic coupling results in higher per-wafer costs.

Using M1 and M2 layers might lead to the utilization of more routing resources and added congestion at the SoC level; it provides significant area improvement. The congestion factor is also included in the metric to quantify the impact on eCFP. Fig. 4.3 shows the area and the eCFP of the designs implemented.

Table 4.2 presents the post-layout simulation results of the eCFP for the implemented designs. The table summarizes the key design parameters, including the number of metal layers used, additional masks, total area, and the resultant eCFP of the design.

4.2 Operational Carbon Footprint

The operational carbon footprint (oCFP) metric evaluates the carbon emissions of a design during its lifetime of operation. The oCFP metric comprises dynamic (DPQ), static (SPQ), and leakage power quantity (LPQ) in a design. oCFP is expressed by Eq (4.5) as:

$$\text{oCFP} = (\text{DPQ} + \text{SPQ} + \text{LPQ}) \times T_{\text{op}} \tag{4.5}$$

where T_{op} is the operating lifetime in hours.

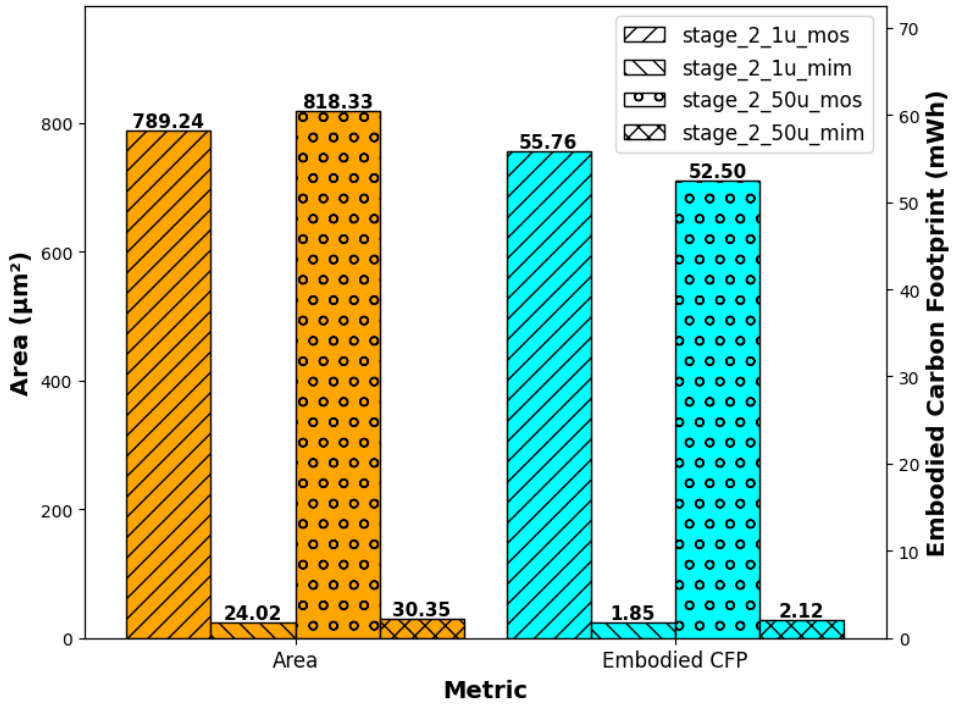


Figure 4.3: Area and Embodied CFP comparison of implemented 2-stage MOSCAP and MIMCAP-based charge pump designs with $1\,\mu$A and $50\,\mu$A current load.

- **Dynamic Power Quantity-**

  DPQ accounts for the power consumed during the dynamic transition of the signal between states. It is given by Eq (4.6) as:

$$\text{DPQ} = \sum \alpha V_{\text{op}} f_{\text{op}} Q_{\text{dyn}} \tag{4.6}$$

  where α is the activity factor, V_{op} is the operating voltage, f_{op} is the operation frequency and Q_{dyn} is the dynamic charge.

- **Static Power Quantity-**

  SPQ accounts for the internal power consumed due to the biasing of the circuit at the steady state. It is defined by Eq (4.7) as:

$$\text{SPQ} = \sum V_{\text{Bias}} \times I_{\text{Bias}} \tag{4.7}$$

  where V_{Bias} and I_{Bias} are the biasing voltage and current, respectively.

- **Leakage Power Quantity-**

  LPQ accounts for the leakage power consumption during the active, standby, and retention modes of operation. It is defined by Eq (4.8) as:

$$\text{LPQ} = P_{\text{standby}} + P_{\text{active}} + P_{\text{retention}} \tag{4.8}$$

In this work, the oCFP metric analyzes the sustainability of the implemented charge pump circuit used for IoT systems. In charge pumps, the oCFP depends primarily on the activity factor (α), the total active lifetime of the device (T_{op}), biasing, and the Static Power Quantity

(SPQ). Additionally, device operation is independent of the type of capacitor used in the fabrication of the design; the oCFP remains the same for MOSCAP and MIMCAP-based pumps and only varies with the current load used. oCFP for charge pumps is expressed in Eq (4.9) as:

$$\text{oCFP} = \text{SPQ} \times T_{\text{op}} \tag{4.9}$$

4.2.1 Device Activity

Since IoT nodes are designed for continuous operation and are always active, the activity factor $\alpha = 1$ is taken with a total active operating time of 20,000 hours over 5 years for the implemented designs.

4.2.2 Biasing Considerations

In the implemented designs, biasing is crucial for proper charge transfer across stages, better PCE, and lower power losses. A constant DC bias voltage (V_{Bias} = VDD = 1.2V) is supplied for *stage_2_1u* and *stage_2_50u* designs. In *stage_2_1u*, a major portion of the total supplied current is consumed as bias current (I_{Bias}). This leads to poor efficiency and higher oCFP per unit of delivered current. On the other hand, the *stage_2_50u* demonstrates better efficiency and lower per unit of CFP because the majority of the current is delivered to the load, and a fraction of it goes into circuit biasing. Table (4.3) presents the biasing considerations for both designs.

Table 4.3: Biasing Considerations for $1\,\mu$A and $50\,\mu$A Load Charge Pump Designs

Biasing Conditions	**stage_2_1u**	**stage_2_50u**
Biasing Voltage (V_{Bias})	1.2V	
Biasing Current (I_{Bias})	$9.23\,\mu$A	$4.87\,\mu$A

4.2.3 Static Power Quantity

For IoT-based systems where circuits are always on, SPQ becomes a major contributor in the evaluation of the oCFP metric. SPQ determines the internal power consumed by the biasing circuitry during the steady state of operation.

The $50\,\mu$A load design has greater biasing overhead than the $1\,\mu$A load design. Consequently, *stage_2_1u* exhibits 89.3% higher SPQ than *stage_2_50u* design. This shows an inverse relationship between SPQ and PCE - the SPQ tends to decrease as PCE increases. Additionally, a higher operating frequency (f_{op}) results in a higher SPQ. Combining these factors,

Table 4.4: Post-layout simulation results of the oCFP of implemented 2-stage charge pump designs with $1\ \mu$A and $50\ \mu$A current load.

Design	**Biasing Voltage** (in V)	**Biasing Current** (in μA)	**SPQ** (in nW)	**Operational CFP** (mWh/IP)
stage_2_1u	1.2	9.23	11,077	387.70
stage_2_50u	1.2	4.87	5,850	204.75

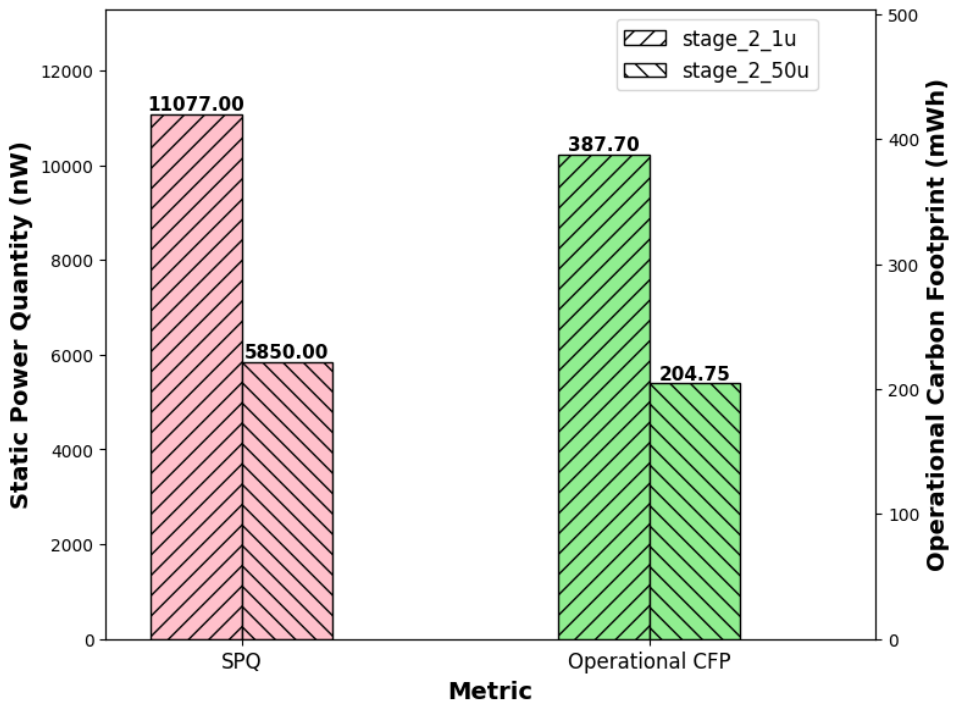


Figure 4.4: SPQ and Operational CFP comparison of implemented 2-stage charge pump designs with $1\ \mu$A and $50\ \mu$A current load.

stage_2_50u demonstrates a lower oCFP than *stage_2_1u* design despite operating at twice the frequency. This reduction in oCFP for a $50\ \mu$A load design highlights that it has a lesser biasing overhead and SPQ than a $1\ \mu$A load design. Fig. 4.4 illustrates the SPQ and oCFP for both designs.

Table(4.4) presents the post-layout simulation results of the oCFP for the implemented designs. The table summarizes the key design parameters, including the biasing voltage and current, SPQ, and the resultant oCFP of the design.

4.3 Total Carbon Footprint

The total carbon footprint (tCFP) combines the embodied carbon footprint (eCFP) and the operational carbon footprint (oCFP) metrics to estimate the overall sustainability of the design. It evaluates the total energy-equivalent carbon emissions associated with the fabrication of the

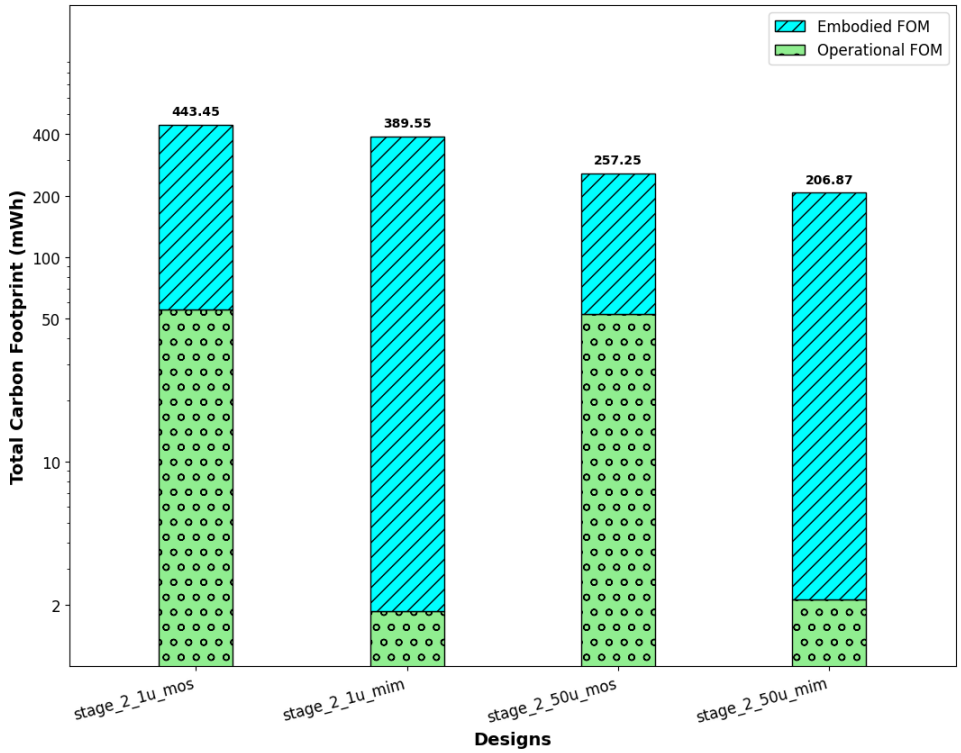


Figure 4.5: Total CFP of implemented 2-stage MOSCAP and MIMCAP-based charge pump designs with $1\ \mu$A and $50\ \mu$A current load.

design as well as during the operation over its lifetime.

As observed, usage of MIMCAPs drastically reduces the eCFP in a design. While oCFP remains the same, MIMCAP-based designs have the lowest tCFP. Fig. 4.5 shows the tCFP of the implemented designs. Although the *stage_2_50u* design has a higher eCFP than the *stage_2_1u* design, it has a lower tCFP due to greater operational efficiency despite having a slightly heavier load. Consequently, for a sustainable IoT design, *stage_2_50u* design using MIMCAPs has the lowest tCFP among all the implemented designs when the SoC area is constrained, and a few instances are required. This shows that ultra-lighter load designs using the currently implemented charge pump topology are not always greener due to the biasing overhead contributing to poor operational efficiency.

CHAPTER 5

Conclusion

In this work, a modified version of the Dickson charge pump circuit is implemented for IoT applications. The circuit is analysed under two different load conditions – $1\ \mu$A and $50\ \mu$A. Conventional electrical performance parameters are evaluated on the basis of power, performance, and area (PPA). Beyond PPA, this work also integrates a sustainability-driven framework in the implemented design using two different metrics- eCFP and oCFP. Combining the two metrics, we calculated the tCFP of the designs, which demonstrates that traditional low-power and low-load designs are not always sustainable. For instance, the implemented Dickson charge pump design with a slightly heavier load of $50\ \mu$A appears to be more sustainable than a lighter load of $1\ \mu$A using MIMCAPs when estimating their total CFP due to its better operational efficiency. The findings suggest that for a lighter current load, other charge pump design topologies may yield better results over the implemented topology in terms of PPA and sustainability.

This paper highlights the importance of co-opting the design configuration based on electrical performance parameters as well as its overall CFP. This adaptability empowers the semiconductor industry to develop sustainability-aware ICs, contributing towards the goal of achieving net-zero emissions.

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List of papers based on Thesis

1. A. Grover et al., “Sustainability Framework for Computing Element Design,” 2025 International Conference on ICT for Sustainability (ICT4S), Dublin, Ireland, June 2025.
2. A. Grover et al., “Framework to Estimate and Benchmark Sustainability of Circuit Design,” 2025 IEEE Region 10 Symposium (TENSYMP), New Zealand, July 2025.