Impact of “Flip-Flop” Design Choices on Sustainability for HPC Application

by

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14 May, 2025

Impact of “Flip-Flop” Design Choices on Sustainability for HPC Application

A Thesis Report

submitted by

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in partial fulfilment of the requirements
for the award of the degree of

Master of Technology

to

Electronics and Communication Engineering
Indraprastha Institute of Information Technology Delhi
New Delhi - 110020

14 May, 2025

Certificate

This is to certify that the thesis titled "**Impact of "Flip-Flop" Design Choices on Sustainability for HPC Application**" being submitted by **Piyush Kumar**, to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of **Master of Technology**, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 14 May 2025

Acknowledgements

I would like to express my deepest gratitude to my thesis guide,**Dr.Anuj Grover**, for their unwavering support, guidance, and encouragement throughout my research. Their expert advice, insightful feedback, and constant motivation have been instrumental in completing this thesis. I am genuinely thankful for their patience and valuable time, which helped me navigate the challenges of this research.

I would also like to extend my sincere thanks to my thesis batchmates,**Najeeb, Abhishek, Gopal, Samridhi, and others**, for their collaborative efforts, continuous support, and constructive discussions that played a crucial role in shaping the outcomes of this work. Their shared knowledge, teamwork, and camaraderie have made this journey both enriching and enjoyable.

This thesis would not have been possible without the collective support of my guide and batchmates, and I am truly grateful for their contributions.

Abstract

As environmental concerns rise, the industry faces pressure to reduce energy consumption. Research has been going on to design energy-efficient designs, particularly in low-power, high-performance applications. Flip-flops are an integral component that is used in almost all digital circuits and analogue/Digital mixed systems, as they are very important for data storage and processing. As dynamic power mainly depends on activity factor and frequency, and accordingly, power dissipation can vary based on input data and clock. In this thesis, both single-edge triggered flip flops (SETFF) and dual-edge trigerred flip flops (DETFF) have been studied.To achieve the same data throughput as in a single-edge triggered flip-flop, a dual-edge triggered flip-flop is an optimum way to reduce power dissipation. In this thesis, SETFF and DETFF designs are evaluated for both Iot and HPC applications. This thesis also proposes a novel Sustainability Framework to allow designers to assess, benchmark, and choose the most efficient and environment-friendly architecture for their product development at the early design phase (i.e., schematic and layout). At the System-on-Chip (Soc) level, flip-flops make a significant contribution due to their widespread use across various intellectual property (IP) blocks. Therefore, analysing these flip-flops for their role in greener circuit designs is crucial, as it plays a key part in advancing sustainable design practices. The overall analysis shows that the operational footprint is far more important than the embodied footprint for HPC applications.

Keywords: Flip-flop ; single-edge triggered ; dual-edge triggered ; Sustainability ; environment-friendly ; intellectual property ; greener circuits

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Abbreviations

IIITD	Indraprastha Institute of Information Technology Delhi
VLSI	Very Large Scale Integration
PPAS	Power, Performance, Area, and Sustainability
ICT	Information and Communication Technology
CMOS	Complementary Metal Oxide Semiconductor
FSM	Finite State Machine
DVFS	Dynamic Voltage Frequency Scaling
IC	Integrated Circuit
SoC	System on Chip
PDLC	Product Development Life Cycle
FoM	Figures of Merit
LCA	Life Cycle Analysis
CFP	Carbon Footprint
eCFP	Embodied Carbon Footprint
oCFP	Operational Carbon Footprint
BE	Base Energy
TR	Track Ratio
APSI	Additional Process Step Impact
IoT	Internet of Things
HPC	High-Performance Computing
ATR	Active Time Ratio
STR	Standby Time Ratio
SOTR	Switched-off Time Ratio
CF	Congestion Factor
PF	Performance Factor
EMI	Extra Metal Impact
TGFF	Transmission Gate Flip-Flop
LMDETFF	Latch Mux Dual Edge Triggered Flip-Flop

CHAPTER 1

Introduction

1.1 Motivation

Power , performance and area (PPA) are the important figure of merits of any VLSI circuits. Finite state machine (FSM), sequential circuits, etc. are the most important part of any digital circuits.And flip flops comsume around 30 to 40 % of total power consumption in such circuits.The most efficient way to analyse power usage is using the concept of Dynamic Voltage Frequency Scaling (DVFS).DVFS is a technique used in VLSI circuits to balance power consumption and performance.It dynamically adjusts voltage and clock frequency to manage workloads i.e. lowering the voltage and frequency during idle states and increasing the voltage during high performance.Using this concept we can provide a choice to the designer to choose the right set of flip flop according to the power usage to minimise the environmental impact.Moreover,at lower votage and frequencies DVFS technique reduces Electromigration, voltage stress,etc. which helps in device degradation and improved lifespan. Carbon impact of VLSI circuits comes from their energy use,epecially in data centers and Iot devices , this technique helps in lowering CO2 emissions.Hence, apart from PPA , sustainability plays a key contribution towards future greener circuits.

1.2 Flip-Flop Architectures

A storage element typically holds its value as an electrical charge on a capacitor. In CMOS flip-flops, the design can be either static or dynamic based on how the stored charge is maintained. Static flip-flops use positive feedback loops to preserve their state reliably, whereas dynamic flip-flops rely on periodic refreshing to counteract charge leakage and retain their data.In this thesis, three flip flops have been studied mainly TGFF,LMDETFF [2] and TSPC.

1.2.1 Architecture 1: Transmission Gate Flip-Flop (TGFF)

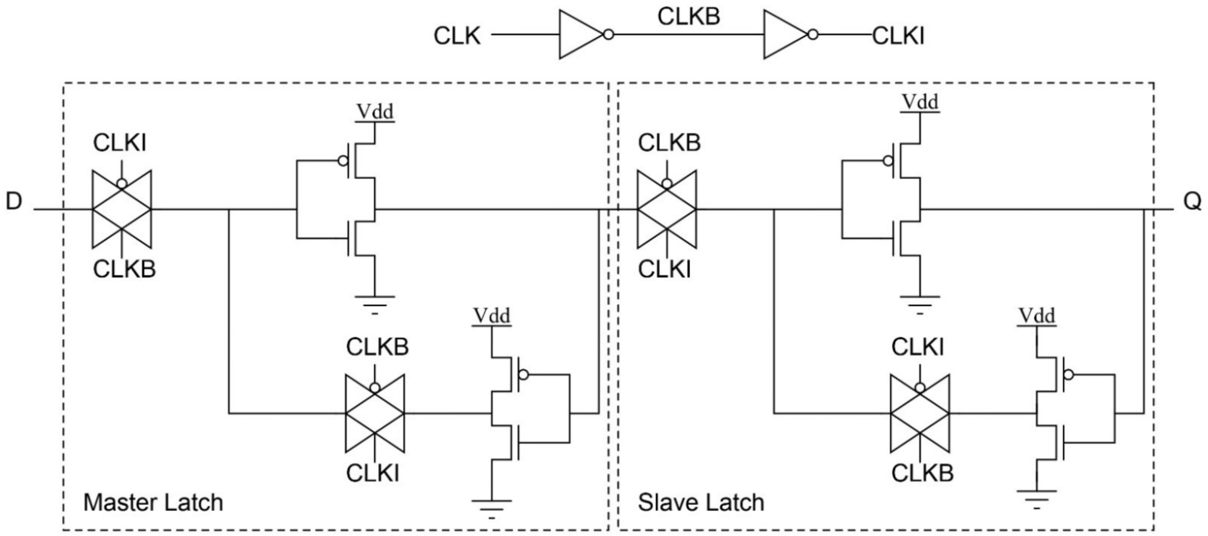

Figure 1.1: Schematic of Transmission Gate Flip-Flop (TGFF)

Description: TGFF [9]is a single edge triggered flip-flop that uses transmission gates for switching and data storage. It is widely used for its balance between speed and power. It consists of two transmission gates and two inverters in a master-slave configuration.

Key Features:

- Low power due to reduced logic depth
- High speed suitable for performance cores
- Sensitive to clock loading

1.2.2 Architecture 2: Latch Mux Dual-Edge Triggered Flip-Flop (LMDETFF)

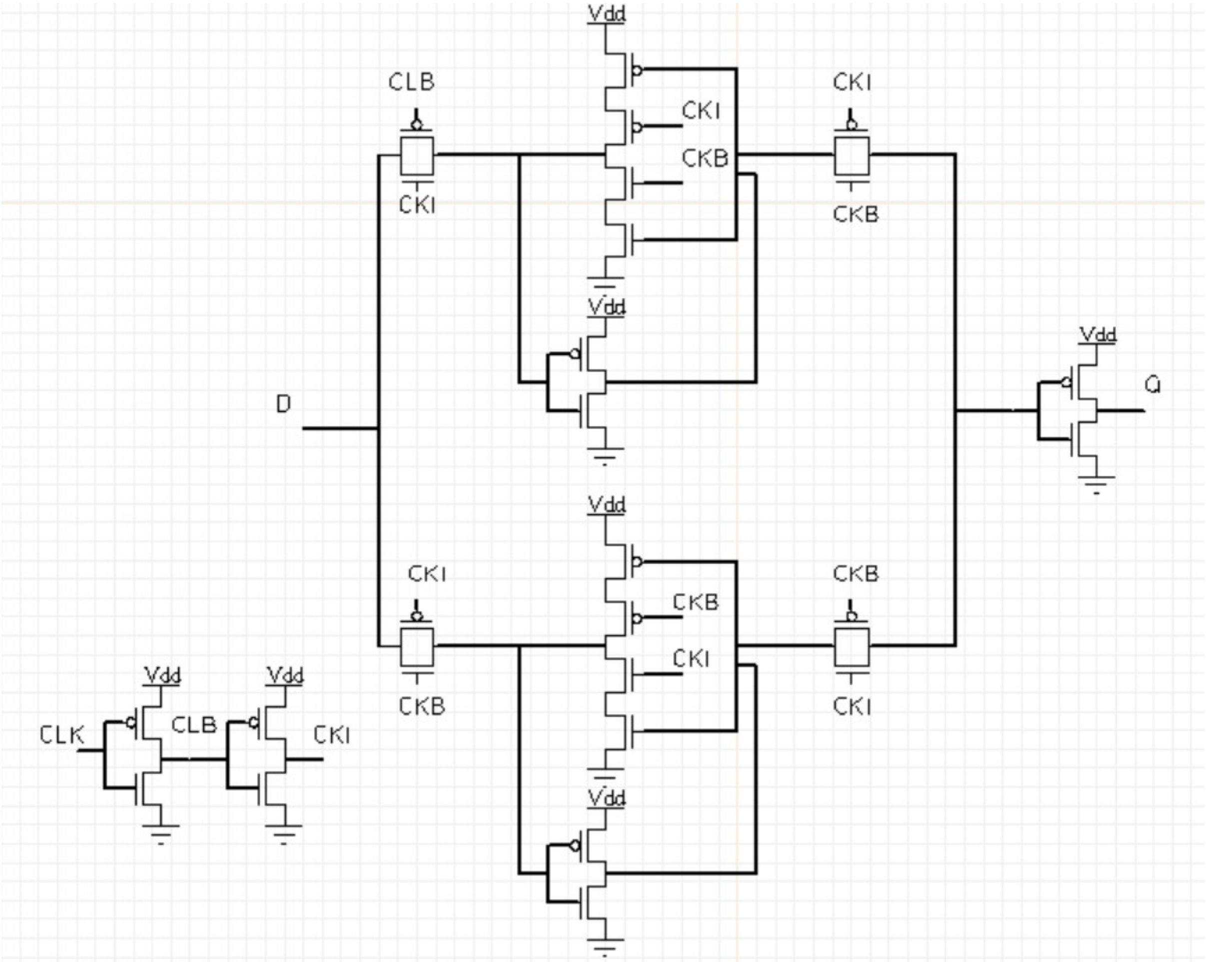

Figure 1.2: Structure of Dual-Edge Triggered Flip-Flop (Latch-MUX Based)

Description: Latch mux dual edge triggered flip-flop is a Dual-Edge Triggered Flip-Flop (DETFF) captures data on both the rising and falling edges of the clock signal, effectively doubling the data throughput at the same clock frequency. The Latch-MUX based implementation is one of the most area-efficient and power-saving designs for DETFFs.

Key Features:

- Samples on rising and falling edges of the clock
- Helps reduce clock power by 50%
- Needs careful latch-MUX timing control

1.3 Background work of each architectures

Flip-flops (FFs) serve as essential storage elements in digital circuits, occupying substantial space in components like registers, counters, and finite state machines. Given their extensive applications, it is crucial to thoroughly understand their operation and key performance metrics [3], including speed, power dissipation, setup time, hold time, and area. Consequently, significant research has been dedicated to exploring various techniques aimed at enhancing flip-flop performance and optimizing their design.

1.3.1 TGFF: Overview

Flip-flops (FFs) come in various types, each with distinct advantages and disadvantages. Among them, the D-FF is widely used due to its simple operation. It can be classified as either static or dynamic, as illustrated in Fig. 1.3 and Fig. 1.4. In static flip-flops, data is retained using latches [11], while dynamic flip-flops store data as charge on node capacitance, requiring periodic clock pulses to maintain the data state. Although static flip-flops generally consume more transistors than dynamic ones, dynamic flip-flops are susceptible to glitches and charge sharing, potentially altering the circuit node voltage and affecting data integrity.

A Transmission Gate Flip-Flop (TGFF) is a specific implementation of the D-FF that utilizes transmission gates instead of traditional logic gates for data control. A transmission gate comprises parallel-connected NMOS and PMOS transistors, controlled by complementary signals. This configuration allows bidirectional data flow with minimal resistance when enabled and high impedance when disabled.

The TGFF typically adopts a master-slave architecture 1.1, consisting of two latches connected in series. The master latch captures the input data on one phase of the clock signal, while the slave latch updates the output on the opposite phase, ensuring edge-triggered behavior.

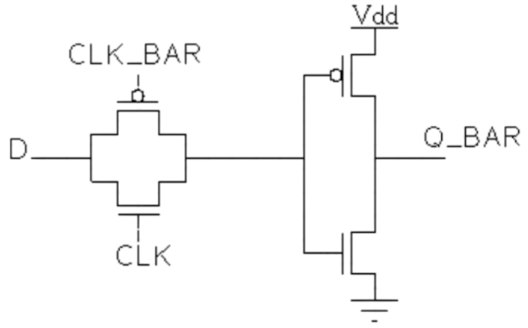

Figure 1.3: Dynamic D-FF

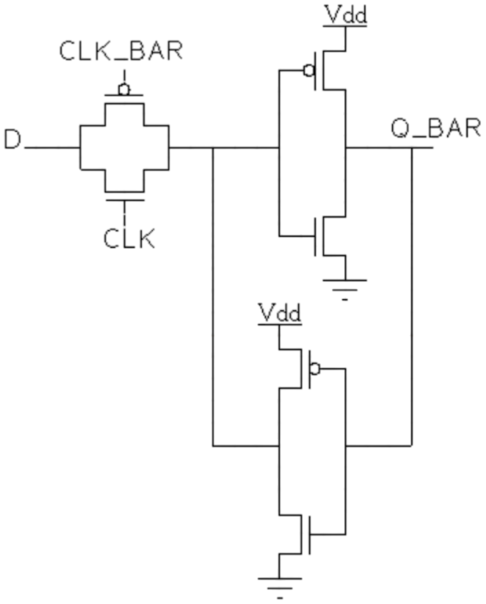

Figure 1.4: Static D-FF

1.3.2 Working OF TGFF

- **When Clock (clk) is LOW (0)**: Master Latch Active: Transmission gates T1 and T4 are ON, while T2 and T3 are OFF. New data (D) continuously enters through T1. Data Path: Data flows through the path: D → T1 → Node 4. At Node 4, data is stored until the clock transitions to HIGH. Slave Latch Inactive: The slave latch retains the previously stored output (Q) shown in fig 1.5. Data at the slave latch remains unchanged (path: Node 5 → Node 6 → Node 7 → Node 8 → Node 5).

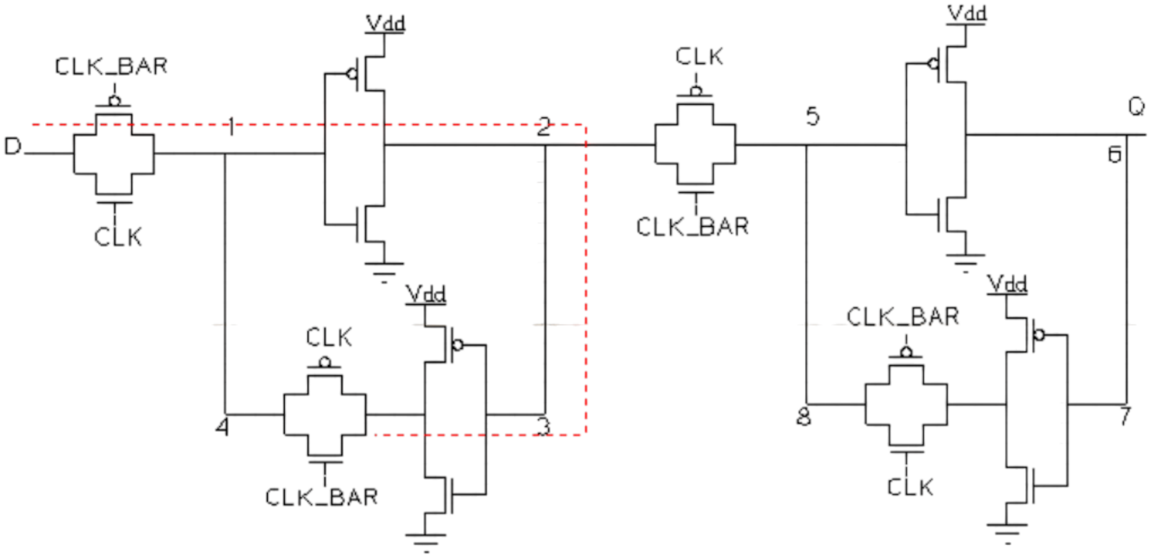

Figure 1.5: when clock is low

- **When Clock (clk) is HIGH (1)**:Master Latch Inactive: Transmission gates T2 and T3 are ON, while T1 and T4 are OFF. The master latch does not allow new data to enter since T1 is OFF. Data Transfer: The previously stored data at Node 4 passes through the path: Node 4 → Node 1 → Node 2 → Node 5 → Node 6 → Q. The output (Q) reflects the data stored in the master latch. Slave Latch Active: The data is also sent to the slave latch via T3, but it does not change the output until the next rising edge of the clock shown in fig 1.6.

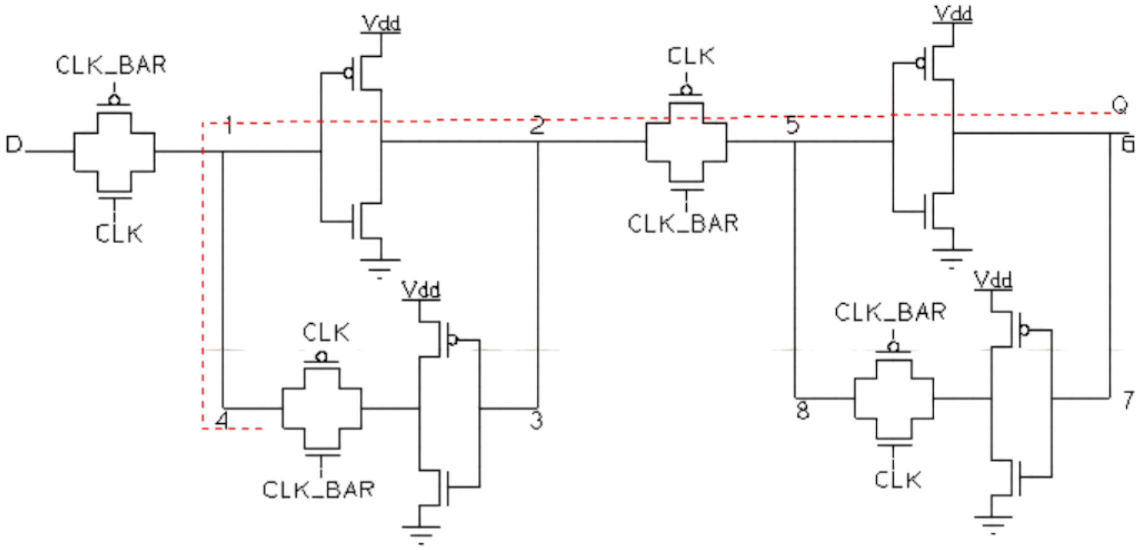

Figure 1.6: when clock is high

1.3.3 Advantage of TGFF

- **Low Power Consumption**: Transmission gates reduce power usage by minimising voltage swings and short-circuit currents during transitions..
- **High Speed**: The reduced number of transistors and direct data paths contribute to faster operation.
- **Compact Design**: The TGFF consists of a total of 20 transistors. Fewer components lead to a smaller silicon footprint, beneficial for high-density integrated circuits.

1.3.4 Challenges and Considerations

While Transmission Gate Flip-Flops (TGFFs) offer several advantages, they also come with certain challenges:

- **Complexity of Clock Signals**: TGFF require both complementary clock signals (CLK and CLK_BAR), which adds complexity to the clock distribution network.
- **Charge Sharing and Leakage Issues**: In dynamic conditions, charge sharing between nodes can result in incorrect logic levels. Additionally, leakage currents can degrade performance over time.

- **Sensitivity to Process Variations**: Manufacturing inconsistencies can affect the threshold voltages of transistors, which can, in turn, impact the reliability of transmission gates.

1.3.5 Research and Developments

Recent studies have focused on improving the performance of Triggered Global Flip-Flops (TGFFs):

- **Clock Gating Techniques**: By implementing clock gating, unnecessary switching activity is reduced, which in turn lowers dynamic power consumption.
- **Radiation-Hardened Designs**: For applications in radiation-prone environments, such as space, TGFFs have been adapted to withstand single-event upsets (SEUs) by incorporating redundancy and feedback mechanisms.
- **Technology Scaling**: As semiconductor technologies advance, TGFFs are being optimized for lower voltage operations and smaller geometries, allowing them to maintain performance while reducing power consumption and area.

1.3.6 LMDETFF: Overview

The clock frequency is determined by the system specifications, and it can be reduced through the use of dual edge-triggered flip-flops (DETFFs). As the name suggests, DETFFs respond to both rising and falling clock edges. This allows for a reduction of the clock frequency by half while maintaining the same data throughput. Consequently, the power consumption of the clock distribution network is decreased, making DETFFs attractive for low-power applications. Even in high-performance applications, using DETFFs offers certain advantages. Since the clock speed is reduced by a factor of two, there is no longer a need to propagate a relatively high-speed clock signal.

1.3.7 Working of LMDETFF

LM-DETFF [4]is a Static DETFF; each latch consists of back-to-back connected inverters and a transmission gate as shown in 1.7.

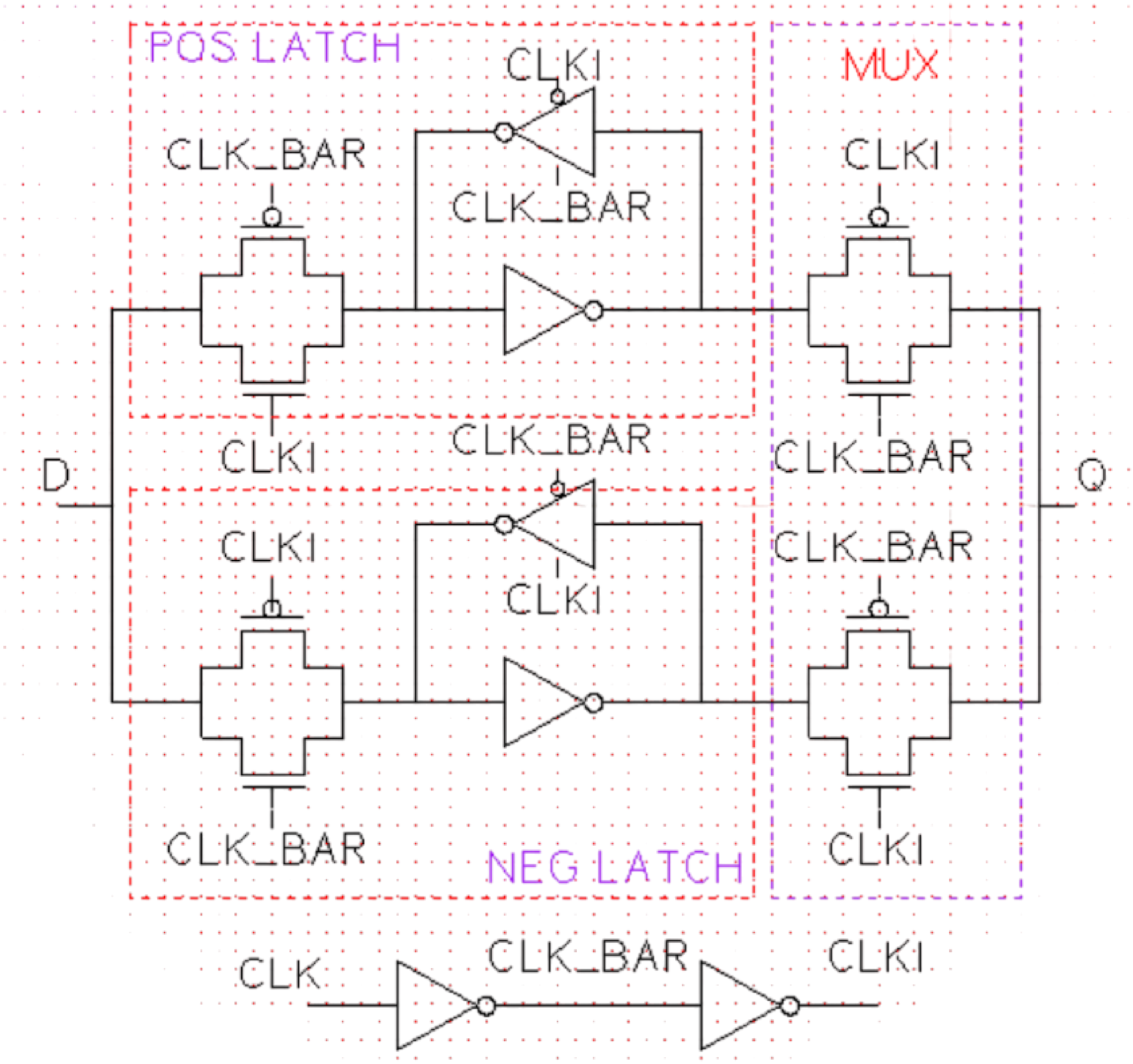

Figure 1.7: Static LM-DETFF

- **CLK = 1 (High State)**: The positive latch captures and stores the input data, while the negative latch holds the previous data. The multiplexer forwards the negative latch data to the output.

- **Falling Edge (1 to 0)**: The positive latch data is transferred to the output through the multiplexer. The positive latch is disabled, safely storing the current input for the next cycle.

- **CLK = 0 (Low State)**: The negative latch captures the input data, while the positive latch maintains its state. The multiplexer forwards the positive latch data to the output.

- **Rising Edge (0 to 1)**: The negative latch data is forwarded to the output via the multiplexer. The negative latch is disabled, securely holding the input data for the next cycle.

1.3.8 Advantages of LMDETFF

- **Power Efficiency**: Latch-MUX DETFFs improve power efficiency by capturing data on both clock edges. This allows for a reduction in clock frequency, which leads to lower dynamic power consumption in the clock distribution network.
- **High Throughput**: These flip-flops can achieve data rates comparable to SETFFs while operating at half the clock frequency, making them ideal for high-speed applications.
- **Area Optimization**: The Latch-MUX design is often more area-efficient than other DETFF architectures, as it minimizes the need for additional clocking circuitry.

1.3.9 Challenges and Considerations

While Latch-MUX DETFFs provide various advantages, there are specific design considerations that need to be taken into account.

- **Clock Skew**: It is essential to minimize clock skew between the two latches to ensure reliable operation.
- **Glitch Avoidance**: Careful design is necessary to prevent glitches during MUX switching, as these can result in incorrect data capture.
- **Process Variations**: The design should be robust against variations in manufacturing processes to maintain consistent performance under different conditions.

1.3.10 Research and Developments

Recent research has focused on improving the performance and reliability of Latch-MUX Dual-Edge Triggered Flip-Flops [7](DETFFs). Key areas of advancement include:

- **Low-Power Designs**: New innovations are aimed at reducing power consumption further, making these flip-flops more suitable for battery-powered and portable devices.
- **Robustness Improvements**: Enhancements in design techniques have resulted in increased tolerance to process variations and environmental factors.
- **Integration with Advanced Technologies**: Latch-MUX DETFFs are being adapted for use in emerging technologies, such as quantum-dot cellular automata and other nanoscale architectures.

1.4 Power Consumption in Logic Circuits

The power consumption [5] of logic circuits, including flip-flops, is a crucial metric in digital circuit design. This section elaborates on the key concepts, equations, and components that influence power consumption and energy expenditure in flip-flop designs

1.4.1 Instantaneous Power Calculation

The instantaneous power consumed by any circuit can be expressed as:

$$P(t) = I_{DD}(t) \cdot V_{DD}$$

Where:

- $P(t)$ is the instantaneous power,
- $I_{DD}(t)$ is the supply current at time t,
- V_{DD} is the supply voltage.

This equation assumes that the supply voltage V_{DD} is stable and constant throughout the operation.

1.4.2 Energy Consumption over Time

The total energy consumed by the circuit over a time interval T is the integral of the instantaneous power:

$$E = \int_0^T I_{DD}(t) \cdot V_{DD} \, dt$$

This integral gives the energy consumed during the time period T, which depends on various factors such as internal switching activity and leakage currents.

1.4.3 Key Components of Power Consumption

Power consumption in a flip-flop can be broken down into the following components:

- **Switching Power**: Power consumed during the switching of the flip-flop, often the dominant component.
- **Short Circuit Power**: Occurs when both NMOS and PMOS transistors conduct simultaneously, creating a direct path from the supply to ground.
- **Leakage Power**: Arises due to leakage currents (e.g., subthreshold leakage, gate leakage, or junction leakage) when transistors are supposed to be off.

1.4.4 Internal Power Consumption Breakdown

Internal power consumption can be further divided into:

- Internal flip-flop power,
- Local clock power consumed in the clock buffer that drives the flip-flop,
- Local data power consumed in the logic stages and transistors of the flip-flop driven by the data input and driving the data output.

1.4.5 Peak Power and Average Power

Peak Power Consumption

The peak power is the maximum instantaneous power consumed during operation and is particularly important for estimating the worst-case scenario for a system (e.g., battery life in a mobile device):

$$P_{\text{peak}} = \max\left(I_{DD}(t) \cdot V_{DD}\right)$$

This metric is critical during the design phase to ensure that the clock and power distribution networks can handle the worst-case current draw without failure.

Average Power Consumption

The average power is the total energy consumed divided by the time interval. It is useful for understanding how much power the circuit uses on average, but it can vary based on the input data patterns and switching activity.

1.4.6 Power-Delay Product (PDP)

The Power-Delay Product (PDP) is a key figure of merit used to compare the energy efficiency of different flip-flop designs. It represents the amount of energy expended per switching event:

$$\text{PDP} = P_{\text{avg}} \cdot T_{\text{delay}}$$

Where:

- P_{avg} is the average power,
- T_{delay} is the propagation delay.

Minimizing PDP is crucial for optimizing flip-flops in low-power designs, as it ensures minimal energy per switching event without compromising speed.

1.4.7 Energy-Delay Product (EDP)

The Energy-Delay Product (EDP) is another metric used when performance is a higher priority than power consumption. It combines the energy consumed per operation and the delay to get an overall performance indicator:

$$\text{EDP} = \text{PDP} \cdot T_{\text{delay}}$$

This metric is particularly useful in high-speed circuits where performance needs to be optimized without significant power penalties.

1.4.8 Switching Power and Clock Power

In digital circuits, switching power is often the primary component. The low-power design objective aims to minimize switching power while ensuring the necessary functionality and performance. Techniques such as clock gating and dynamic voltage scaling are commonly employed to achieve this

CHAPTER 2

Post-Layout Analysis

2.1 Objective of the Analysis

- Compare power, performance, area, and sustainablity across different flip-flop architectures.
- Evaluate the dynamic and static power dissipation in various flip-flop architectures
- Analyse the impact of supply voltage scaling and frequency scaling techniques on overall power efficiency.
- Determine the silicon area requirements for each flip-flop type. Explore trade-offs between area reduction and performance
- Identify the impact of charge leakage, charge sharing, and setup/hold time violations.
- Assess the robustness of flip-flop designs under varying temperature conditions and process variations.
- Introduce metrics for carbon footprint analysis of flip-flop designs.

2.2 Specifications and Simulation Parameters

SPECIFICATION	**VALUE**
Technology	Row 65 nm
Operating Voltage	1.3 V
Output Load	20 Ff
Clock frequency	2 GHz(TGFF) 1 GHz(LMDETFF)
Iso-Delay	300 ps
Layout track used	26

Table 2.1: Specifications used in post layout analysis

In high-performance computing (HPC) systems, analyzing circuit delays and power consumption is essential for ensuring reliable and efficient operation.The reason to take 300 ps iso delay is that we need an optimum point so that we could achieve a higher performance without failing the circuits. But as the frequency of operation increases, the dynamic power consumption increases sharply. Hence, there is always a trade-off between power and performance, which the designer has to face, and according to his application, he has to decide. Also, the layout track used is a 26-track layout. The reason is that although 13 tracks is practised in industries, it takes a large area horizontally. Hence, for the area optimisation, a 26-track library is used. The simulation setup includes various voltage levels, temperature conditions, and process corners to account for different performance scenarios, including worst-case situations. The breakdown of the simulation setup is as follows:

2.2.1 Delay Calculations [12]

- **CLK-to-Q Delay** This calculation is performed at a voltage of 1.17 V under the SS corner at 125°C. This condition helps analyze the delay in the worst-case slow corner and high temperature, which typically results in increased propagation delay.
- **Setup Time Calculation** The setup time is calculated at 1.17 V under the SS (Slow-Slow) corner condition at 125°C, similar to the CLK-to-Q delay. This scenario simulates the worst-case conditions, where the setup time is maximized due to slower transistor performance resulting from low voltage and high temperature.
- **Hold Time Calculation** The calculation is based on a voltage of 1.43 V, under the FF corner at -40°C. This scenario involves high voltage and low temperature conditions because higher voltage generally enhances the switching speed of transistors, while low temperatures can worsen hold-time violations due to slower edge transitions.

2.2.2 Power Calculations

- **Power Consumption** Power is calculated at a nominal voltage of 1.3 V, under standard TT corner conditions, at 25°C. This scenario represents typical operating conditions where both the voltage and process parameters are at standard values, establishing the baseline power consumption.

Summary of Simulation Setup

The simulation setup for the flip-flop design includes various voltage, temperature, and process conditions. The following table summarizes the simulation parameters and conditions for delay, setup time, hold time, and power calculations:

Parameter	**Simulation Voltage**	**Corner**	**Temperature**
CLK-to-Q Delay	1.17 V	SS (Slow-Slow)	125°C
Setup Time	1.17 V	SS (Slow-Slow)	125°C
Hold Time	1.43 V	FF (Fast-Fast)	-40°C
Power Consumption	1.3 V	TT (Typical-Typical)	25°C

Table 2.2: Simulation Setup for Flip-Flop Design Analysis

2.3 Layout Design Specifications

In high-performance digital circuit designs, such as those used in High-Performance Computing (HPC), flip-flops are essential components that must be optimized for speed, power consumption, and area efficiency.

In this thesis, the layout of the flip-flop has been designed in 26 tracks using various materials and metal layers, specifically polysilicon, the M1 metal layer, the M2 metal layer, vias, and contacts. Among these design choices, the use of the M2 metal layer for the ground connection between the two VDD rails is a key factor in determining the performance of the flip-flop.

2.3.1 Analysis of Layouts(TGFF)

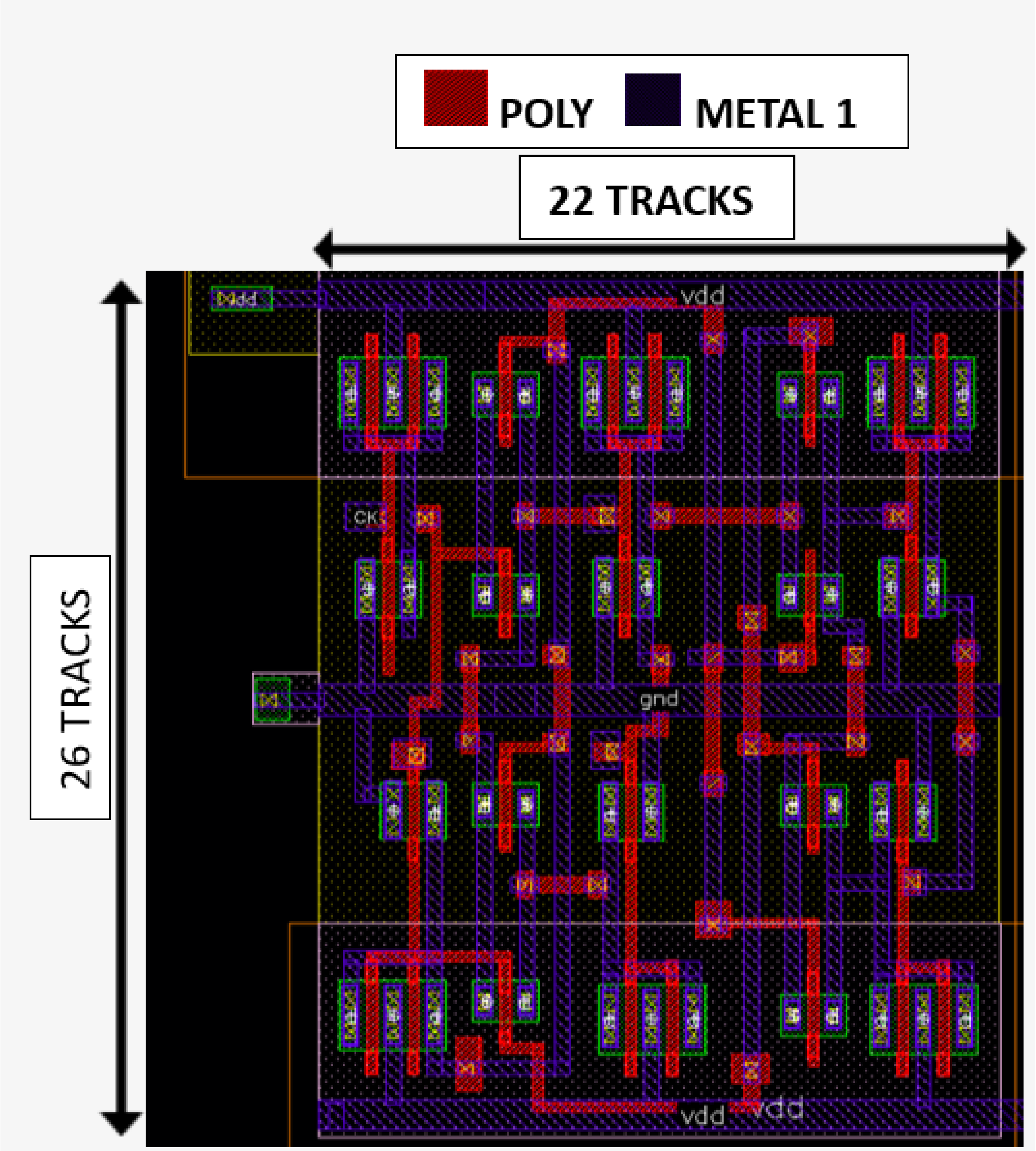

Figure 2.1: TGFF layout without additional M2 layer

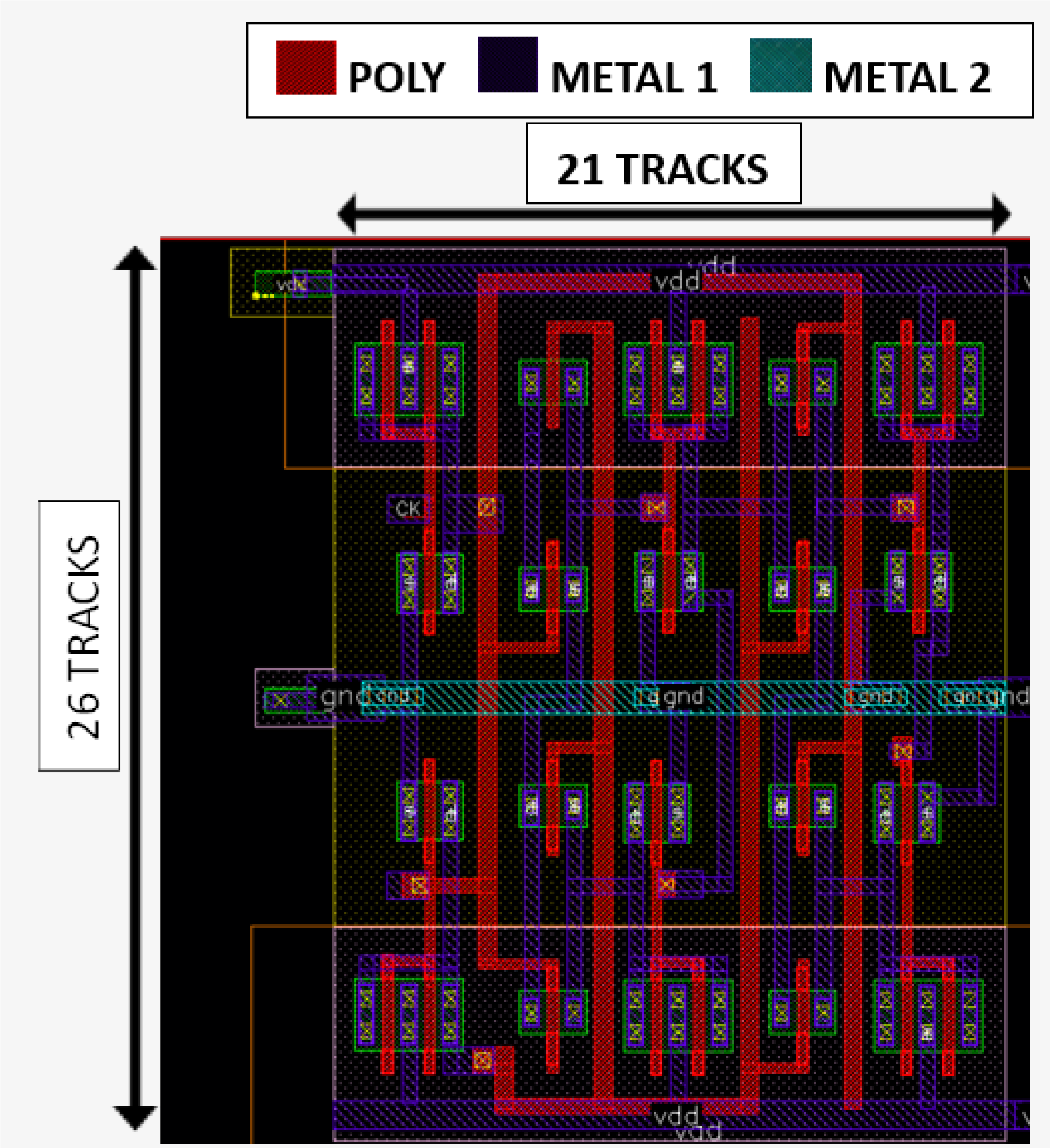

Figure 2.2: TGFF layout with additional M2 layer

Observation: The high-performance layout is designed with 26 tracks, while the layout 2.1 uses only polysilicon and the M1 metal layer for routing, resulting in an width of 22 tracks. In contrast, layout 2.2 includes an additional M2 metal layer for the ground connection, which reduces the overall area by one track. This reduction is significant and could have a substantial impact at the System-on-Chip (SoC) level

2.3.2 Analysis of Layouts(LM-DETFF)

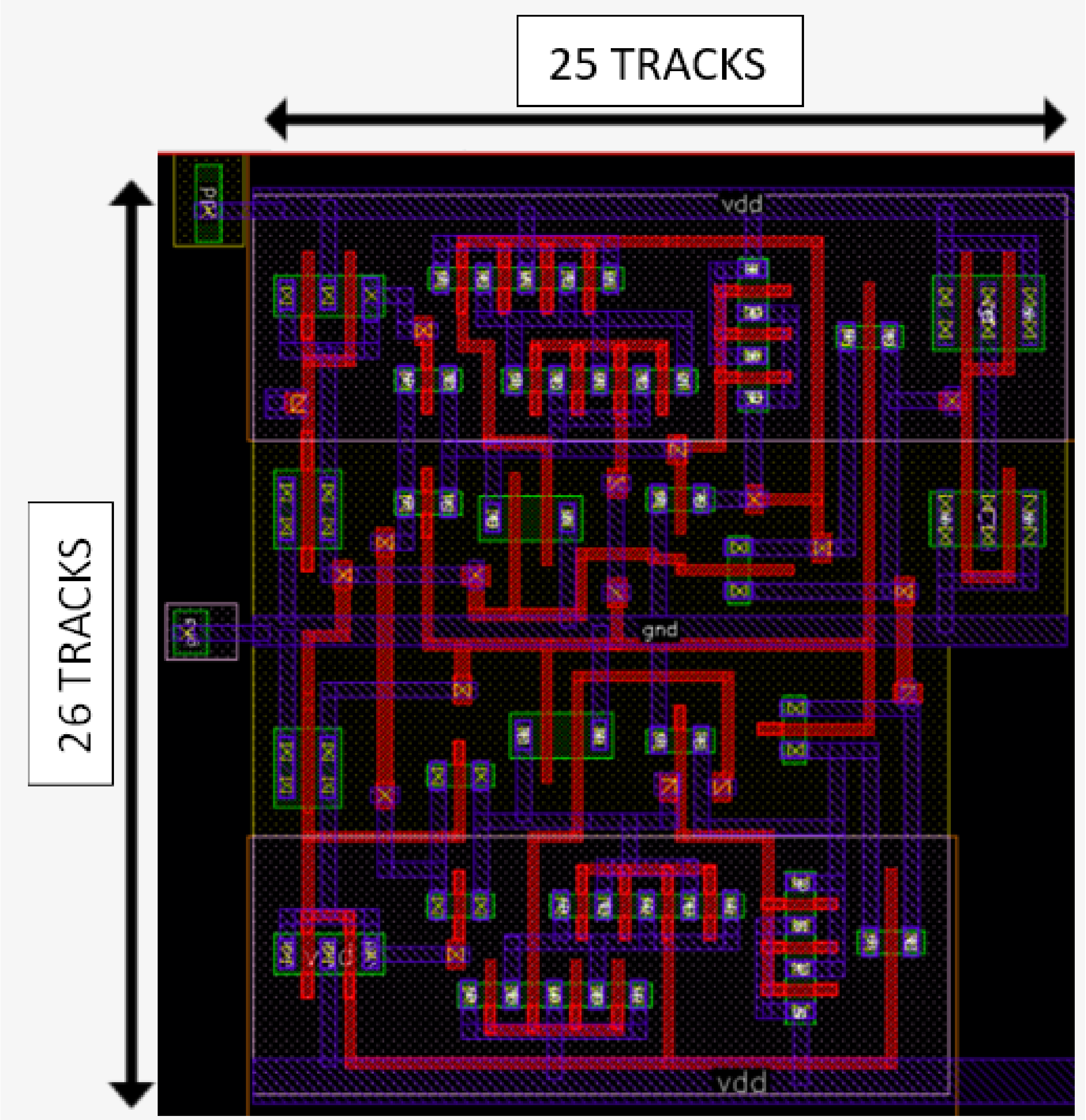

Figure 2.3: LMDETFF layout without additional M2 layer

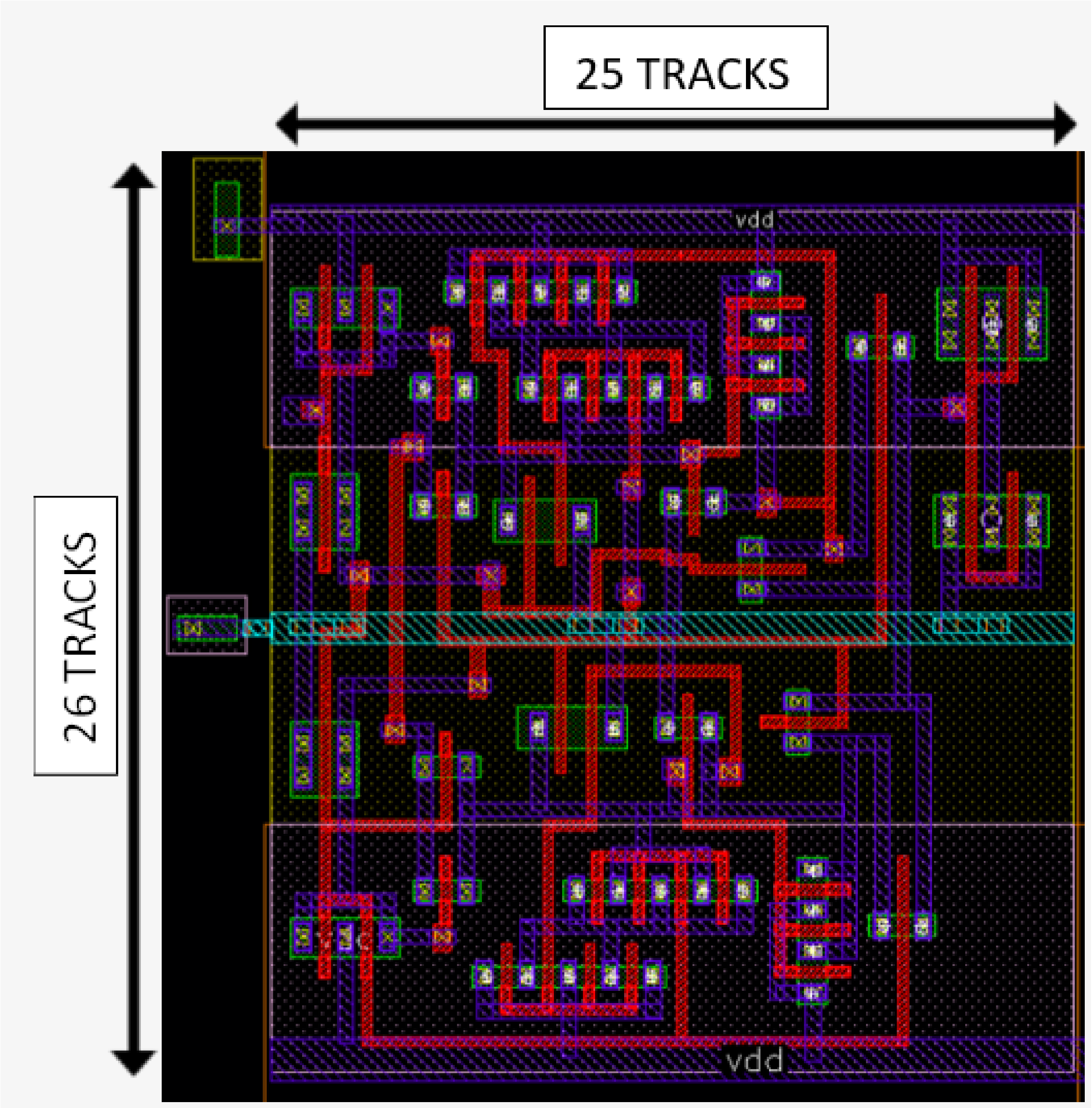

Figure 2.4: LMDETFF layout with additional M2 layer

Observation: The LMDETFF layout is designed using 26 tracks configuration, while the layout 2.3 uses only polysilicon and M1 metal layer for routing, resulting in an width of 25 tracks. In contrast, layout 2.4 includes an additional M2 metal layer for the ground connection, but overall its area remains the same.

2.4 Result and its Comparative Analysis

Design Name	**Area (um^2)**	**M2 Metal Used**	**Operating Frequency (MHz)**	**CLK-2-Q Delay (ps)**	**Setup Time (ps)**	**Hold Time (ps)**	**Leakage Current (nA)**	**Data Power (µW)**	**Clock Power (µW)**	**PDP (fJ)**
TGFF	22.88	0	2000	268	35	0.7	7.17	1.45	4.72	3.57
TGFF	21.84	1	2000	261	36	4.3	4.16	1.43	4.60	2.65
LMDETFF	26.00	0	1000	289	49	-3.3	8.06	0.31	0.99	2.70
LMDETFF	26.00	1	1000	291	49.5	-4	7.89	0.48	0.95	2.72

Table 2.3: Comparison Flip-Flop Designs

2.4.1 AREA:

- **TGFF:**The area of the TGFF flip-flop is around 22.88 µm^2 for the first design and 21.84 µm^2 for the second, with a slight difference due to the M2 metal usage.
- **LMDETFF:**Both LMDEFF designs occupy 26 µm^2, which is slightly larger than TGFF.

2.4.2 CLK-2-Q Delay:

TGFF has lower CLK-2-Q delay compared to LMDEFF, indicating faster data transfer and more efficient timing.The reason being LMDETFF has more transistors compared to TGFF.

2.4.3 Setup Time/Hold Time:

- TGFF has a shorter setup time, leading to faster data synchronization compared to LMDEFF.
- LMDEFF has a negative hold time, which can be problematic as it might lead to timing violations. In contrast, TGFF maintains a positive hold time.

2.4.4 Leakage Current:

- TGFF has lower leakage current, making it more energy-efficient compared to LMDEFF.

2.4.5 Data Power:

- LMDEFF consumes significantly less data power than TGFF, indicating better power efficiency in certain low-power applications.

2.4.6 Clock Power:

- LMDEFF consumes significantly less clock power compared to TGFF, making it more power-efficient for clock-heavy operations.

2.4.7 Power Delay product(PDP):

- LMDEFF has a slightly lower PDP compared to TGFF, indicating better power efficiency relative to its delay.

2.5 Summary of Findings:

PARAMETERS	**CONCLUSION**
Area (µm^2)	TGFF is more area-efficient.
Operating Frequency (MHz)	TGFF has lower delay, making it faster. But DETFF has more throughput
Setup Time (ps)	TGFF has a shorter setup time, enabling faster synchronization.
Hold Time (ps)	TGFF has positive hold time, while LMDEFF may face timing violations.
Leakage Current (µA)	TGFF has lower leakage current, making it more power-efficient.
Data Power (µW)	LMDEFF consumes less data power.
Clock Power (µW)	LMDEFF consumes less clock power, more efficient for clock-heavy designs.
PDP (fF)	LMDEFF has a lower PDP, indicating better power efficiency.

Table 2.4: Specifications used in post layout analysis

CHAPTER 3

Sustainability Metric and Analysis on circuit

3.1 Introduction : Sustainability

In this section, a proposed framework is presented to evaluate the sustainability of circuits, designs, or architectures based on Life Cycle Assessment (LCA). The sustainability of a VLSI design is assessed in terms of its embodied and operational footprints.

Estimating the Carbon Footprint (CFP) [15] of any product is a data-intensive process. Often, necessary data may not be available during the early stages of the Product Development Life Cycle (PDLC), when designers need to make critical decisions. To address this limitation, our framework is designed to utilize historical trends and available data, allowing for reasonable comparisons between alternative design choices.

It is important to note that VLSI circuit and system designers generally do not have the opportunity to select the materials or their sources used in the manufacturing process, the type of energy consumed (whether renewable or non-renewable), the location of chip fabrication, or the logistics of transportation. These choices are typically beyond the designer's control. Instead, the decisions faced by designers are independent of these broader considerations and operate at a different level of abstraction compared to early-stage manufacturing or supply chain management.

Consequently, the output of this framework is not intended to provide an exact CFP for the design. Rather, it offers intelligent guidance to help designers make decisions that can potentially reduce environmental impact. The metric [6]is expressed in energy units, which can later be converted into CO2 equivalent values, providing an estimate of the design's potential environmental impact in terms of carbon emissions.

3.2 Embodied Carbon Footprint (eCFP) metric

The embodied carbon footprint (eCFP) encompasses the emissions generated throughout the entire design and manufacturing process. Equation (3.1) illustrates the eCFP, which is calculated as a product of the following components: 'Base Energy per μm^2' (BE), 'Cell Area,' 'Extra Metal Impact' [8] (EMI), and 'Additional Process Step Impact' (APSI) within the designed cell layout.

$$\text{eCFP} = \text{BE} \times \text{Cell Area} \times \text{EMI} \times \text{APSI} \tag{3.1}$$

- **Base energy per μm^2 (BE):** BE is calculated by amortizing the total energy consumed per wafer that is processed in a base/ standard/ reference process, over per unit area as shown in Eq. (3.2).

$$\text{BE} = \frac{\text{Energy consumed per standard wafer}}{\text{Wafer area}\,(\mu m^2)} \tag{3.2}$$

In this study, we examine the energy consumed during the processing of a 300mm diameter wafer with a six-metal layer stack in a standard 65nm manufacturing process, which amounts to 4204 kWh per wafer.

- **Cell Area:** Embodied CFP of a design is directly proportional to its area. It is considered in μm^2 unit.

- **Extra Metal Impact (EMI):** A designer may need to compare two different layout implementations of a circuit. A layout can be denser if it utilizes more metal layers. While a denser layout can help reduce its effective Cost per Function Point (eCFP), using extra metal layers can leave fewer routing resources available for system-on-chip (SoC) level routing. This reduction in available resources can lead to increased congestion and, consequently, greater area utilization at the system level. Therefore, although there may be improvements at the cell level, this approach can result in an overall disadvantage at the system level. Electro-Magnetic Interference (EMI) reflects the impact of the reduced availability of routing resources on system-level eCFP.

  Equation (3.3) defines the Track Ratio as the proportion of total tracks available in an additional metal layer compared to the remaining tracks allocated for SoC-level routing after considering those used in intra-cell layout design.

$$\text{TR} = \frac{\text{Total tracks available in the metal layer}}{\text{Tracks available for routing in the metal layer}} \tag{3.3}$$

The impact of additional metal on energy consumption during fabrication is represented in Equation (3.4). In this context, the congestion factor (CF) acts as a multiplier, converting the usage of extra metal tracks into a corresponding effect on cell area. This, in turn, affects the effective Cell Fabrication Power (eCFP) metric.

$$\text{EMI} = 1 + \Big(\text{TR} - 1\Big) \times \text{CF} \tag{3.4}$$

In this work, the value of CF is set to 0.3 based on an example of a RISC processor to illustrate the impact of increased SoC congestion on the effective CFP of a design.

- **Additional Process Step Impact (APSI):** The BE factor mentioned above reflects the energy consumed during the processing of a standard wafer. However, process variants—such as different types of devices (e.g., transistors with varying threshold voltages), various capacitor types, or additional metal layers—can lead to increased energy consumption due to the extra steps involved in wafer processing. The calculation of APSI is performed using Equation (3.5).

$$\text{APSI} = ((\text{Total masks} - \text{Reference masks}) \times \text{Mask Factor}) + 1 \tag{3.5}$$

In this work, we considered that a wafer processed using the standard 65nm technology by STMicroelectronics requires 36 masks and their related processing steps.

In this work, we assume that each additional process step requires an extra 4.5% energy, which corresponds to a Mask Factor value of 0.045 which report an approximate 18% increase in energy usage when moving from a 6-layer metal stack (4204 kWh) to an 8-layer metal stack (4895 kWh) at the 65nm technology node. This rise corresponds to adding four extra masks—specifically, one metal mask and one via mask for each additional metal layer. Additionally, the standard number of masks used in wafer fabrication for STMicroelectronics' 65nm process serves as a reference point.. This is based on data published in a conference paper [8]. Depending on the actual energy consumed during these additional process steps, this value may be revised in the future.

3.3 Operational Carbon footprint metric (oCFP):

The operational carbon footprint (oCFP) measures the carbon footprint(CF) associated with the energy consumed by hardware during its operational life. The proposed oCFP estimates the energy consumed across all operational modes of the device. In Equation (3.6), oCFP is calculated by summing the dynamic power and leakage power over the total operational period of the device, denoted as T_{total}. This total period varies depending on the specific requirements of the application and the conditions of use.

$$\text{oCFP} = T_{\text{total}} \times (\text{Dynamic power} + \text{Leakage power}) \tag{3.6}$$

3.3.1 Application specific operation profile

Electronics [13]are utilized in a wide range of applications, each with distinct operational conditions, performance requirements, and usage profiles. Circuits designed using foundational libraries can be targeted toward specific applications. Depending on the particular application, the operational profile of a design—meaning the duration during which it is expected to operate in high-performance, regular, low-power, or standby mode—can vary. This variation has a direct impact on oCFP.Here, in this thesis, HPC is the main application and based on the application for which the chip is being developed, the operating lifetime of the product changes.

Operating Modes	**HPC based operating time ratios**
Active - ATR	40%
Standby - STR	40%
Switched off - SOTR	20%
Operational lifetime (hours)	25000

Table 3.1: Operating Time Ratio

For HPC, we consider a lifespan of about 3 years, during which it remains active for most of its life and is in switched-off mode for a short period.

To estimate the operational capacity factor of a foundation cell (oCFP), its operational lifetime is divided into three phases: Active, Standby, and Switched-off. These phases are expressed as ratios of the total operating time (T_{total}), which are referred to as the Active Time Ratio (ATR), Standby Time Ratio (STR), and Switched-off Time Ratio (SOTR). These ratios are detailed in Table 3.1.

3.3.2 Dynamic Power

Dynamic power is the power consumed by a foundation cell during that part of its operational life when it is active. Therefore, the Dynamic Power component in Eq. (3.7) is normalized for the ratio of total operating time when the cell is powered up and expected to drive output.

Here the dynamic charge consumed during operation (Q_{dyn}), is multiplied with the switching activity (α), which is the ratio of times/ cycles in which the inputs/ outputs of the circuit change. This is then multiplied with the operational voltage of active mode V_{active}, and operating frequency f.

$$\text{Dynamic power} = Q_{\text{dyn}} \times \alpha \times V_{\text{active}} \times f \times \frac{\text{ATR}}{100} \tag{3.7}$$

To simplify things, we have focused on only one type of active state of a system. However, advanced System-on-Chips (SoCs) typically operate at various supply levels and operational frequencies based on the system's performance requirements. In these cases, the Active Time Ratio (ATR) is divided into components to represent the different voltage-frequency combinations in which the system operates.

3.3.3 Leakage Power

For the context of this framework, the power consumed by the system due to its component leakages is considered Leakage power. It is estimated as in Eq. (3.8).

$$\begin{aligned}\text{Leakage power} = {} & \left[I_{\text{active}} \times V_{\text{active}} \times \left(\frac{\text{ATR}}{100} \times \text{PF}^{\text{PWM}}\right)\right] \\ & + \left[I_{\text{standby}} \times V_{\text{standby}} \times \left(\frac{\text{STR}}{100} + \left(\text{PWM} \times \frac{\text{ATR}}{100} \times (1 - \text{PF})\right)\right)\right]\end{aligned} \tag{3.8}$$

The first term in Equation (3.8) represents the leakage power consumed in active mode, where I_{active} is the leakage current during this mode. Designs aimed at low-power applications often utilize pulse width modulation (PWM), a technique that reduces the supply voltage as soon as the desired computation is completed. As a result, the system can operate in a low-leakage standby mode for an extended period, effectively saving power. Circuit implementations that operate at higher speeds can transition into standby mode more quickly. In Equation (3.8), the PWM variable is set to 1 for designs that incorporate pulse width modulation.

In this section, we introduce a Performance Factor (PF) to estimate the additional duration a design will operate in standby mode. PF is defined as the ratio of the time required for a specific design to complete an operation compared to the time taken by a reference design for the same operation. The PF for a design is calculated by considering its worst-case delay. As a result, each design has a distinct PF value that reflects its delay in comparison to that of the reference design. The second term in Equation (3.8) represents the leakage power consumed in standby mode, where I_{standby} denotes the leakage current during this period. This term also accounts for the extra time that a high-performing system operates at V_{standby} while using the PF.

3.4 Impact of sustainability on Flip Flop Designs

A well-designed assessment framework must be robust, adaptable, verifiable, coherent, fair, repeatable, scalable, and relevant [18]. In this section, we showcase the flexibility and strength of the framework by applying it to compare various architectures or implementations of the desired functionality in foundation cells.The designs have been implemented in 65nm Low Standby Power technology from STMicroelectronics. A macro-level circuit design sustainability evaluation in the same technology is presented in [16].

3.4.1 Embodied Carbon Footprint (eCFP) metric

To evaluate the versatility of the framework, consider the impact of layout efficiency and extra metal track usage on sustainability.

Design Name	**IP Area)**	**Reference Mask (Upto M6**	**Extra Mask**	**Total Mask**	**Total Tracks**	**Upper metal layer used**	**No. of metal tracks aviable in porous layer for intracell routing (M1))**	**Track available in upper metal layer**	**Embodied FOM (KWh/IP))**
TGFF M1	22.88	36	0	36	26	0	0	26	1.36E-06
TGFF M1 + 1M2	21.84	36	0	36	26	1	0	24	1.32E-06
LMDETFF M1	26	36	0	36	26	0	0	26	1.55E-06
LMDETFF M1 + 1M2	26	36	0	36	26	1	0	24	1.57E-06

Table 3.2: Embodied Footprint Comparison

- **Impact of Area on using Extra Metal Layer**: Foundation cells, such as buffers, combinational gates, latches, and flip-flops, are typically designed using only the lowest metal layer (Metal-1 or M1). The Transmission Gate Flip-Flop (TGFF) [17], which features a master-slave latch configuration, as illustrated in Fig. 1.1. Refer layouts,2.1 and 2.2 as utilizing one addditional M2 layer contributes to a denser layout.

  However, as shown in Fig. 3.1, eCFP estimated using Eq. (3.1) is lower in M1+1M2 implementation than M1 only implementation. Adding 1 track of M2 reduces flipflop area from 22.9 μm^2 to 21.8 μm^2, and hence, despite the increased impact on system-level routing (estimated using EMI) due to congestion but the area has a broader impact on footprint, eCFP reduces from 1.36 mWh to 1.32 mWh due to significant impact of area reduction.

- **Impact of congestion on using Extra Metal Layer**:Latch mux based flip flops consists of more no of transistors than TGFF [17], which features a master-slave latch and mux configuration, as illustrated in Fig. 1.7. Refer layouts,2.3 and 2.4 as utilizing one addditional M2 layer has no effect on change in area.

  Although the use of 1 additional track of M2 in the layout results in increased congestion at the SoC level and, therefore EMI impact sets in as per Eq. (3.4). Due to congestion ecfp increases from 1.55 mWh to 1.57 mWh.

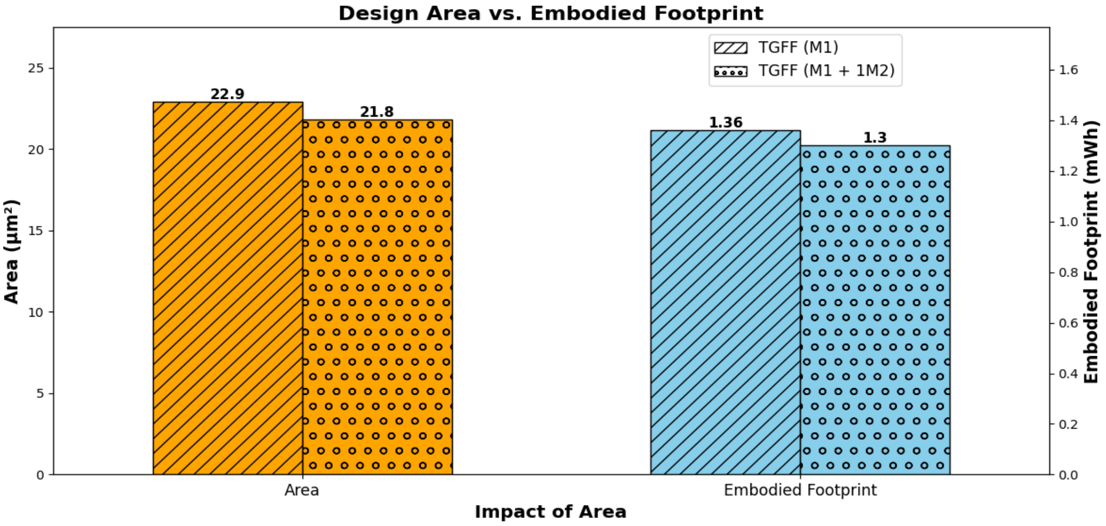

Figure 3.1: Impact of area on embodied footprint on using an additional upper metal routing layer M2 for designing TGFF.

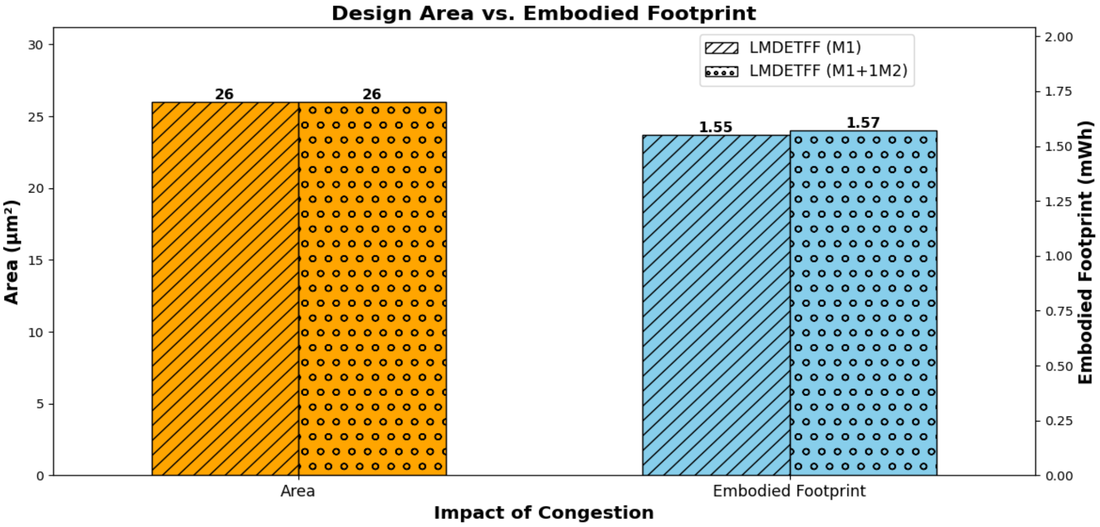

Figure 3.2: Impact of congestion on using an additional upper metal routing layer M2 for designing LMDETFF.

3.4.2 Operational Carbon Footprint (oCFP) metric

Table 3.3: Operational Footprint Comparison

Design Name	**Active Area(um2)**	**Time Taken To Complete Single Calculation By This Design(ps)**	**Time Taken To Complete Single Calculation By Reference Design (WorstCase Design)(ps)**	**RPR**	**Activity factor**	**Operating Frequency (MHz)**	**Dynamic Power(nW)**	**Leakage Power (nW)**	**OPEX FOM (KWh/IP))**
TGFF M1	22.88	268	291	0.9209621993	0.1	2000	1820	7456.8	2.86E-04
TGFF M1 + 1M2	21.84	261	291	0.8969072165	0.1	2000	5980	4326.4	2.35E-04
LMDETFF M1	26	289	291	0.9931271478	0.1	1000	1300	6843.2	2.58E-04
LMDETFF M1 + 1M2	26	291	291	1	0.1	1000	1430	7140.64	2.70E-04

- **Impact of Application Profile**

  oCFP of designs are calculated using Eq. (3.6), which depicts dependence on operating time ratios and the operational lifetime of a product, as shown in Table 3.3. Flip Flops are designed for low dynamic power and lower leakage depending on the application. Here , both TGFF and LMDETFF have been studied for operational carbon footprint.

- **Impact of activity factor oCFP (TGFF/LMDETFF)**: The operational carbon footprint depends on multiple factors, but mainly on power. Hence, on evaluation, it was found that on increasing the activity factor of the designs considering the same frequency , oPCF also incresaes which can be seen in fig 3.4 and fig 3.3

  In case of fig 3.3, TGFF using an additional M2 layer reduces the operational carbon footprint by 39% approx , which is due to a reduction in dynamic power, as referred to in the table 2.3, because the flop is operating at higher frequencies. Similar case can be seen at 10 % activity factor.

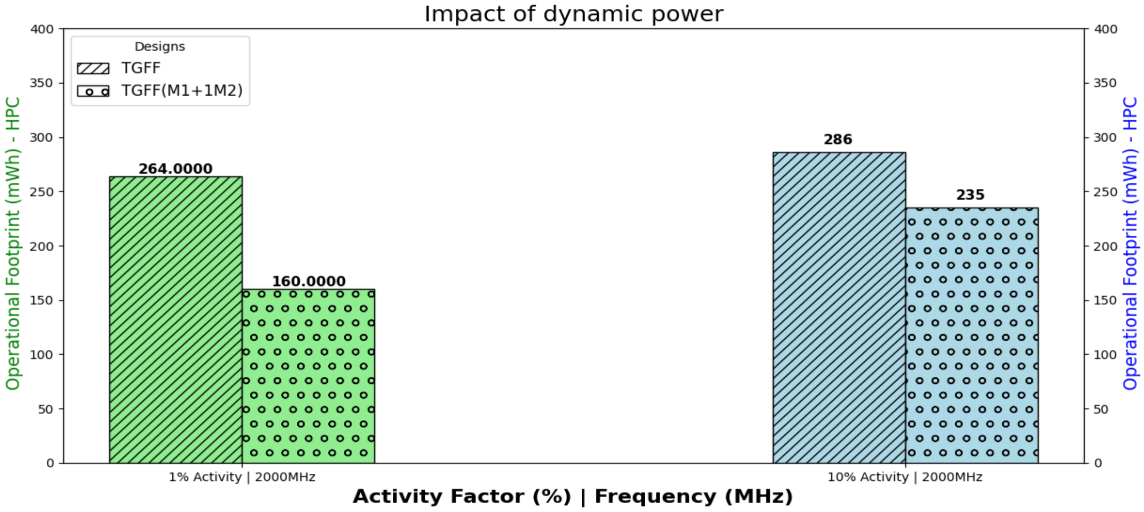

Figure 3.3: Impact of activity factor on oCFP (TGFF)

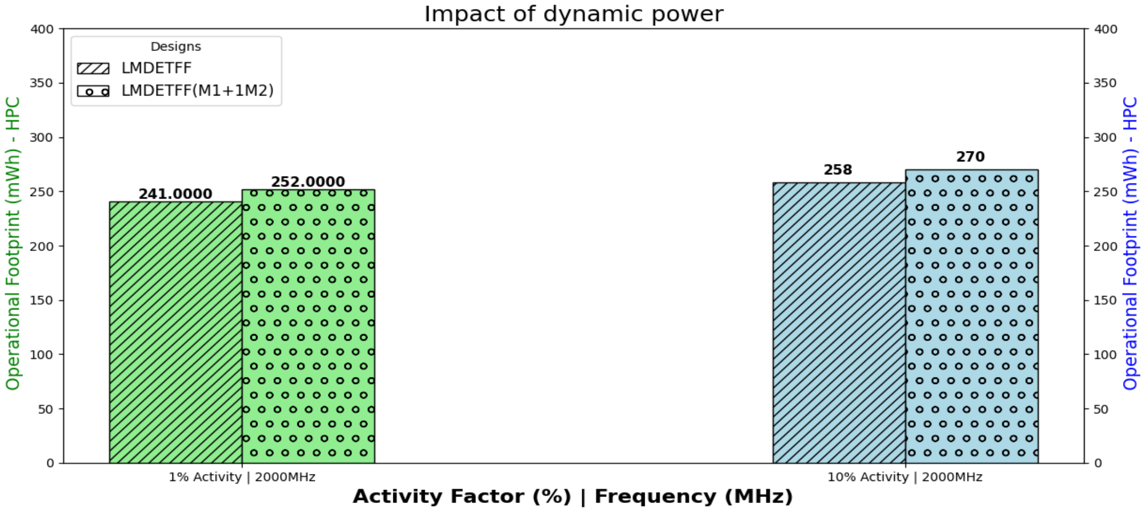

Figure 3.4: Impact of activity factor on oCFP (LMDETFF)

3.4.3 OPEX on Varying alpha and Frequency

For robustness of the designs , the metric has been evaluated at different frequency and activity factor to analyse its effect on operational carbon footprint. So the LMDETFF is evaluated at activity factor of 1% at 50 MHz can be used for low power core [10]application and 1% activity factor at 1000 MHz, can be used for high power core within the same application. The result is shown in fig 3.5

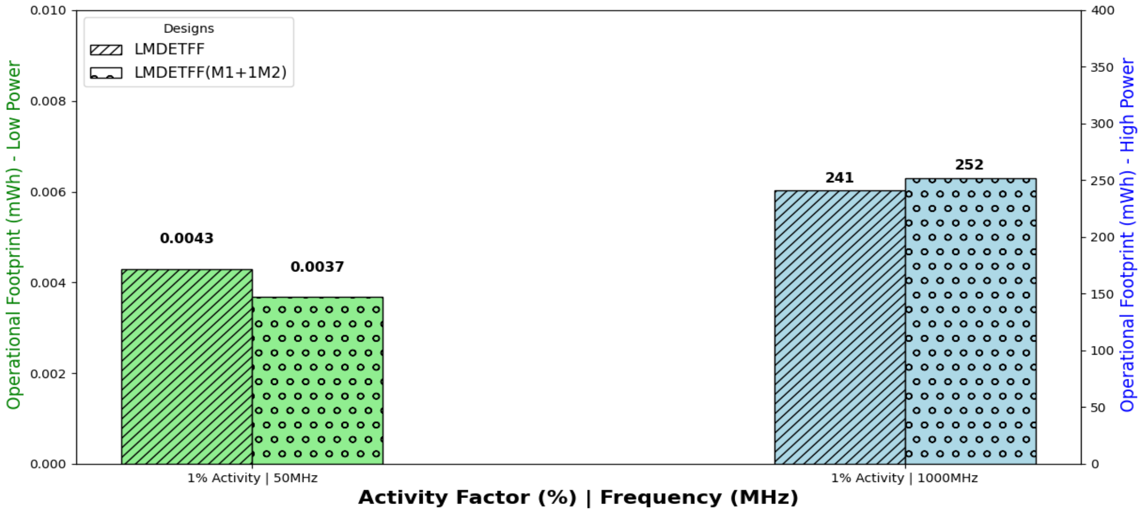

Figure 3.5: Impact of activity factor and frequency on oCFP

- The primary source of power consumption in low-power circuits is leakage power, but due to the lower operating frequency and less switching activity, this leakage power remains relatively low, resulting in a lower operational footprint.

- For high power applications operational footprint is higher due to increased switching activity factor and frequency. Here, dynamic power outperforms leakage.

- The reason for less OPCF in low power because it majorily depends on leakage and as we utilise one additional metal layer could be as we go to higher metal layer parasitic capacitance goes down due to increased distance from the substrate. On the contrary, the M2 layer will have more intermetal capacitance due to the M1 and M3 layers, but its significance is lower than the substrate capacitance.

  But, for high power core OPCF mainly depends on dynamic power which is directly proportional to alpha, parasitic capacitance and voltage. Hence, its operational carbon footprint is more on even using one additional M2 layer.

3.4.4 Total Footprint:

It is observed in the fig 3.6 that the total footprint for a high-performance application mainly depends on its operational carbon footprint since high-performance SoCs are designed for continuous and high-frequency applications and most of the time in their entire lifecycle they operate, such as data processing,AI and high-speed computing.

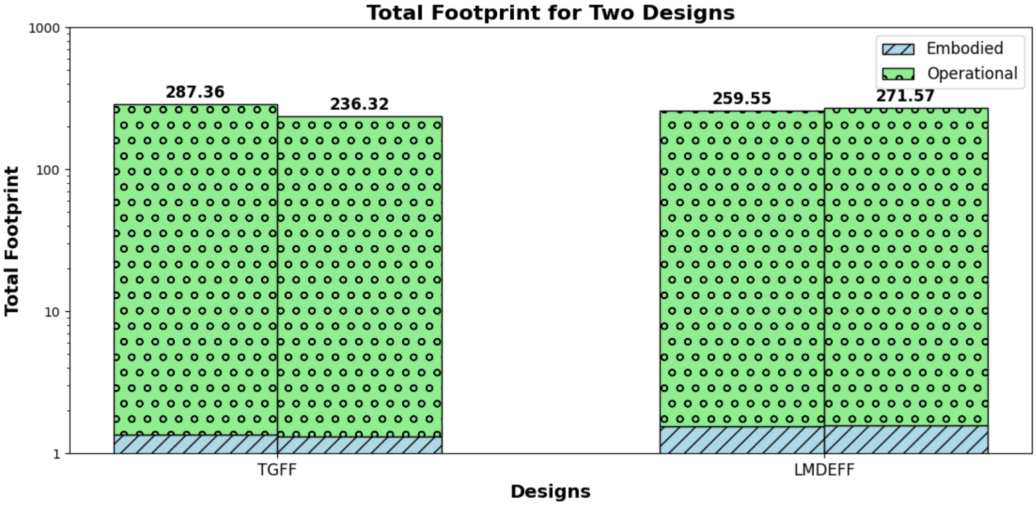

Figure 3.6: Total Footprint

Over the entire lifecycle, the operational energy consumed is much more than the initial embodied energy especially, under high loads.

- **Observation 1:** For high-performance computing applications where power efficiency and more throughput are required, a designer can choose LMDETFF with only M1 metal layer used, as its total footprint is approximately less than 9.98% of that of TGFF with only M1 metal layer used.

- **Observation 2:** For low power and moderate speed applications, a designer can choose TGFF with one additional M2 layer as its overall carbon footprint is approximately less than 13.02% % of that of LMDETFF with one extra M2 track.

CHAPTER 4

CONCLUSION

Traditionally, the performance of semiconductor integrated circuits (ICs) has been evaluated based on three key metrics: Power, Performance, and Area (PPA). However, the rapid proliferation of information and communication technology (ICT) devices has led to a significant increase in both manufacturing and operational energy demands. Over the past two decades, numerous innovations have emerged aimed at assessing the sustainability of electronic devices. Unfortunately, these contributions have either concentrated on improvements at the manufacturing level or focused on a higher-level abstraction of ICs. As a result, designers of foundational libraries have not been effectively engaged in the push for sustainability. In this work, we propose a sustainability framework that provides designers with methods to evaluate sustainability during the early stages of design implementation.

Here, be evaluating these parameters on the basis of sustainability metric gives a designer a perspective to utilise which type of flip flop based on its utilization inside a core it could be high power or low power , less throughput or more throughput or even based on area.

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List of papers based on Thesis

1. A. Grover et al., "Sustainability Framework for Computing Element Design," 2025 International Conference on ICT for Sustainability (ICT4S), Dublin, Ireland, June 2025.
2. A. Grover et al., "Framework to Estimate and Benchmark Sustainability of Circuit Design," 2025 IEEE Region 10 Symposium (TENSYMP), New Zealand, July 2025.