Impact of Level Shifter Design Choices on Sustainability

by

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Certificate

This is to certify that the thesis titled "**Impact of Level Shifter Design Choices on Sustainability**" being submitted by **Abhishek Jain (MT23208)**, to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of **Master of Technology**, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Abstract

In this advancing era of technology and innovation, semiconductor development has exploded, enabling researchers to develop cutting-edge, ultra-low-power, and high-speed integrated circuits. However, this scaling progress in semiconductors is having a detrimental impact on the environment by overexploiting its available resources. Hence, to mitigate this impact, the VLSI industry is shifting its focus toward environmentally sustainable IC manufacturing, moving beyond the traditional Power, Performance, and Area (PPA) approach. Currently, most proposed sustainability evaluation approaches operate at higher abstraction levels, such as the SoC/product level, rather than at the individual logic cell level. In this work, we address this requirement by proposing a novel sustainability evaluation paradigm and validating it on different Level Shifter cell architectures. A Level Shifter is a low-power design technique used to facilitate data communication between multi-voltage domains in an SoC. Along with the proposed paradigm, we also introduce a unique double-row layout design technique for Level Shifters to enhance area optimization and analyze its impact on sustainability.

Keywords: Level Shifter ; Subthreshold ; Sustainability Metric ; Embodied Footprint ; Operational Footprint ; Low-power

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Abbreviations

PPA	Power, Performance, and Area
SoC	System on Chip
PPAS	Power, Performance, Area, Sustainability
SLS	Subthreshold Level Shifter
LCA	Life Cycle Analysis
GHG	Green House Gas
CFP	Carbon footprint
eCFP	Embodied carbon footprint
oCFP	Operational carbon footprint
FoM	Figures of merit
CCLS	Cross-coupled Level Shifter
WCMLS	Wilson Current Mirror Level Shifter
DSELS	Deep Sub-threshold Energy Efficient Level Shifter
RSWCRLS	Robust Subthreshold Level Shifter with Wide Conversion Range
LPSVTLS	Low-Power Subthreshold to Above-Threshold Voltage Level Shifter
C3MLS	Ultra-Wide-Range Energy-Efficient Level Shifter with CCLS/CMLS Hybrid Structure
DCG	Dynamic Current Generators
PD	Pull-down
PU	Pull-up
VT	Threshold voltage
MIMCAP	Metal-Insulator-Metal capacitor
IoT	Internet of Things
Auto	Automotive
HPC	High-Performance Computing
PE	Portable Electronics
CF	Congestion factor
POF	Porosity Factor
ATR	Active Time Ratio
STR	Standby Time Ratio
SOTR	Switched-off Time Ratio
PF	Performance factor

Notation

μ	'Mean' or 'micro'
σ	'Standard deviation'
α	'Switching Activity factor'
f_{op}	'Frequency of operation'
Q_{dyn}	'Dynamic charge consumed during active operation mode'
V_{active}	'Active mode supply voltage'
$V_{standby}$	'Standby mode supply voltage'
V_{static}	'Static biasing supply voltage'
I_{active}	'Leakage current drawn during active mode from Active supply'
$I_{standby}$	'Leakage current drawn during standby mode from Standby supply'
I_{static}	'Static biasing current'
T_{total}	'Total operating time in a application'
I_{static}	'Static biasing current'
PWM	'Pulse Width Modulation enabling boolean variable'

CHAPTER 1

Introduction

1.1 Motivation

Rapid advancement in semiconductor technology has led to the development of high-performance and reliable integrated circuits that facilitate complex and high-speed operations with an aim to maintain an optimal Power, Performance, and Area (PPA) tradeoff [1]. However, this achievement comes with environmental challenges, as increasing manufacturing complexity and operational power consumption contribute to resource depletion and sustainability concerns [2, 3]. Hence, VLSI industries have begun shifting their focus beyond the traditional evaluation metrics of Power, Performance, and Area (PPA) to incorporate Sustainability (S) as a key consideration to form a Power, Performance, Area, and Sustainability (PPAS) evaluation framework.

Many semiconductor giants like TSMC, Apple, Samsung, STMicroelectronics, Intel, and Qualcomm have recently issued their sustainability reports forecasting their carbon-neutrality goals [4, 5, 6, 7, 8, 9]. In the year 2022, a report by Bloomberg stated that energy consumed by Taiwan Semiconductor Manufacturing Company Limited (TSMC) exceeded the total energy consumption of Sri Lanka [10].

As per [11], it is evident that advancing semiconductor fabrication technologies are becoming increasingly energy-demanding, making it essential to address their growing impact on the environment [12]. Although in the past two decades, there has been significant advancement in this domain, most of them have focused on a higher abstraction level of an IC or a product. Thus, a paradigm for cell-level PPAS analysis is needed. Hence, this work aims to address that need with a preliminary strategy. It also validates the proposed sustainability evaluation metrics on a diverse set of Level Shifters.

1.2 Sustainability

The concept of sustainability, introduced in the 1987 Brundtland Report [13], has been defined and interpreted in various ways over time. However, in this work, sustainability is defined as designing a product in a manner that minimizes its long-term environmental impact. In the VLSI industry, design sustainability is analyzed using methodologies like Life Cycle Analysis (LCA) and the Green House Gas (GHG) emission protocol. GHG protocol classifies an industrial product's emission into 3 levels [14]:

- **Scope 1**: Direct emissions from industry operations such as fuel combustion within facilities, transit-related pollutants, and industrial chemical discharge.
- **Scope 2**: Indirect emissions from purchased energy arise from fab operations, facility maintenance, & data centers, with carbon emissions proportional to energy consumption.
- **Scope 3**: Other Indirect Emissions such as Logistics, supply chain processes, and raw material production in business operations.

Life Cycle Analysis facilitates the categorization of a product's emissions based on GHG protocol-defined scopes. The carbon footprint (CFP) emissions are primarily estimated based on two key components [14]:

- **Embodied carbon footprint (eCFP)**: This encompasses the environmental impact across the entire process of design and manufacturing, covering stages such as prototyping, raw material selection, processing, fabrication, testing, and validation. eCFP can vary depending on the manufacturing location, technology employed, fabrication complexity, and supply chain efficiency.
- **Operational carbon footprint (oCFP)**: This includes the total energy consumed throughout the operational lifespan of a product, covering all modes such as active, standby, and switched-off states. Assessing energy usage across these states is essential for understanding its overall environmental impact. oCFP can vary based on factors such as the usage environment, the specific application, and the user's operating habits.

In this work, we propose a sustainability evaluation paradigm that enables designers to make environmentally conscious design choices early in the SoC design flow, specifically at the schematic and layout levels.

1.3 Level Shifter

A Level Shifter is a low-power design technique used to facilitate data communication between multi-voltage domains in an SoC [15]. It provides an interface between multiple islands in an SoC, where each island may operate at different voltage levels. The use of multi-voltage islands within a single SoC has become a highly effective and widely adopted technique in modern SoC development. This enables designers to operate different SoC components at varying voltage levels, allowing high-performance units to receive higher voltages while lower-activity components operate at reduced voltages for improved power efficiency [16].

A Level Shifter can have two or more voltage supplies connected to it, depending on the design architecture. However, a standard Level Shifter typically operates with two supplies. In this work, these are referred to as VDDL and VDDH, where VDDL represents the lower voltage and VDDH represents the higher voltage. Level Shifter standard cells are inserted and placed in an SoC after the power distribution grid is established in the physical layout [16].

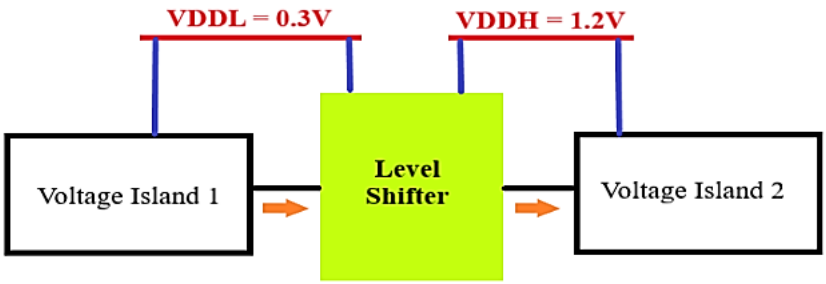


Figure 1.1: Level Shifter reference block diagram

A Subthreshold Level Shifter (SLS) is a specialized type of Level Shifter in which one of the voltage islands operates in the subthreshold region [17]. In the subthreshold region, circuit behavior is largely influenced by leakage current, and the drain current increases exponentially with respect to the gate voltage [18]. Operating in it saves power & provides high amplification.

Low-power applications such as IoT and wearable technologies increasingly adopt subthreshold operation as a viable strategy for minimizing energy consumption [19, 20]. In this work, a set of different SLSs is implemented to shift the voltage from the subthreshold level (VDDL = 0.3V) to the nominal voltage (VDDH = 1.2V), and has been implemented, simulated, and analyzed using the proposed sustainability evaluation paradigm. A reference block diagram of the Level Shifter is shown in Fig. 1.1. Furthermore, the level-shifted input signal waveform for the target voltage shift is presented in Fig. 1.2.

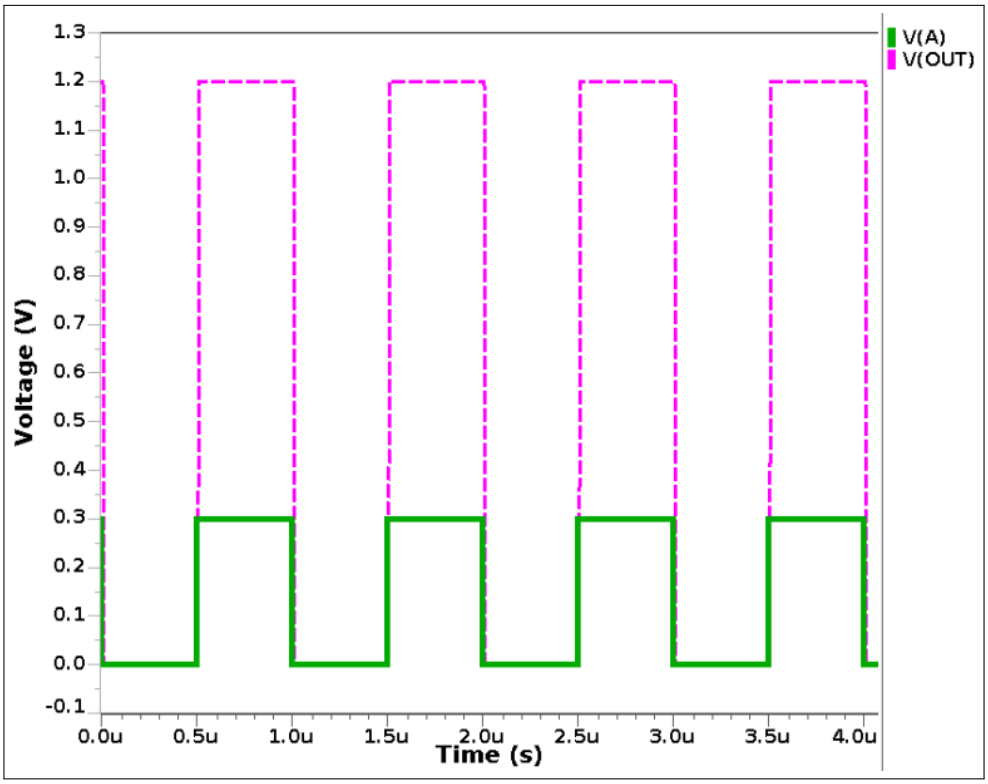


Figure 1.2: Level-shifted waveform for the target voltage shift from the input signal (A) = 0.3V to the output signal (OUT) = 1.2V.

CHAPTER 2

Background and Related Work

2.1 Sustainability contributions in VLSI

Over the past two decades, numerous novel contributions have advanced the shift toward sustainability-driven VLSI design. Some of them have been presented here.

2.1.1 EE-Toolbox based sustainable material selection (2000)

In an initial work proposed in the year 2000 [21], the authors presented a material-specific sustainability analysis based on some key evaluation metrics available in the EE-toolbox software. The metrics assessed products based on various factors, including toxicity potential, recyclability, energy consumption (raw material processing energy and operational energy), and process-related environmental impact.

2.1.2 Sustainable IC Framework (2017)

A 2017 study [22] emphasizes the increasing ecological footprint of IC fabrication, which is becoming comparable to operational energy use, particularly in low-power systems. To address this, the authors developed a scalable framework for evaluating fabrication-induced environmental costs across technology nodes ranging from 130nm to 32nm. It also demonstrated how variations in the metal stack for SoC development influence the environmental footprint by implementing different SoC designs.

2.1.3 Chasing Carbon: Product Life Cycle analysis (2022)

In 2022, a comprehensive study analyzed the CFP of commonly used products through their Life Cycle Analysis (LCA) [14]. It highlighted that while advancements in algorithms, software, and hardware have enhanced energy efficiency, the overall environmental impact remains significant. In recent years, hardware production and infrastructure have become the primary contributors to emissions, surpassing energy consumption during a product's operational lifespan. It provides a graphical analysis of the CFP exerted by the products.

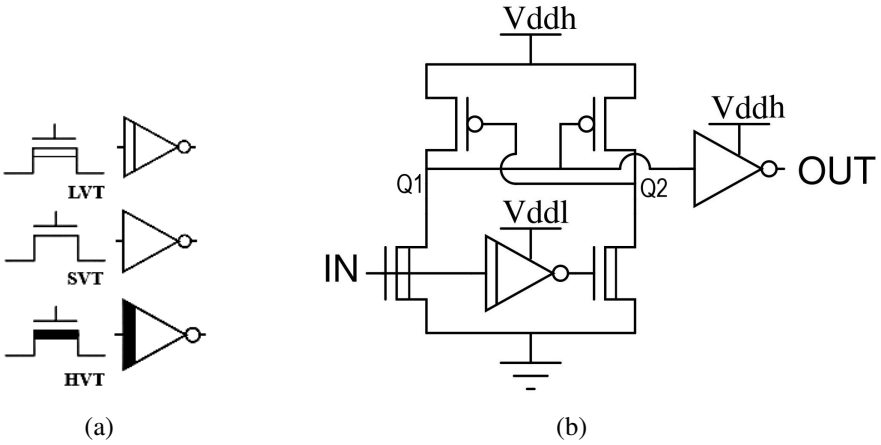
2.1.4 Eco-Reliability Metric (2024)

In 2024, [23] introduced a novel Eco-reliable metric to assess VLSI circuit sustainability by integrating reliability factors with the environmental impact of manufacturing. It expanded the design analysis horizon beyond conventional Power, Performance, and Area to enable efficient system- and circuit-level evaluation by incorporating Sustainability. It is determined by integrating circuit reliability metrics like Mean Time to Failure (MTTF) and Mean Time Between Failures (MTBF) with environmental considerations such as System Earth equivalent Time, life cycle carbon footprint, and Earth's available resources.

2.2 Level Shifter Architectures

In this work, two conventional Level Shifters and four advanced Level Shifters have been analyzed, implemented, & evaluated using the proposed sustainability metrics. These designs were specifically selected for analysis due to their suitability for subthreshold operation and are thus referred to as Subthreshold Level Shifters (SLS). Each design brings a unique perspective that shapes design decisions and enriches the depth of sustainability analysis. Fig. 2.1(a) shows the schematic conventions used for designing the SLS architectures.

2.2.1 Cross-coupled Level Shifter (CCLS)



(a) (b)

Figure 2.1: (a) Schematic convention (b) Cross-coupled Level Shifter (CCLS) [24] schematic

Cross-coupled Level Shifter is also known as Differential Cascode Voltage Switch. It utilizes a pair of cross-coupled PMOS transistors in the pull-up (PU) network to form a feedback mechanism, thus ensuring stable voltage levels at the output nodes Q1 and Q2 as illustrated

in Fig. 2.1(b). To modify the output state based on the input, the pull-down (PD) NMOS transistors must be sufficiently strong to counteract this feedback effect. PD NMOS are hence strengthened by using either low-threshold voltage (VT) device variants or larger-sized devices, both of which lead to increased fabrication mask requirements [24].

The feedback system reduces leakage by maintaining the output nodes at steady logic states, effectively lowering static power consumption. However, it requires a strong contention current, which results in higher dynamic power usage.

2.2.2 Wilson Current Mirror Level Shifter (WCMLS)

Conventionally, a Current Mirror Level Shifter (CMLS) operates by utilizing a current mirroring technique, enabling consistent current replication across its branches. This ensures a steady current flow while interfacing different voltage domains. This approach allows for reliable voltage translation while preserving signal integrity across SLS transistor devices [24].

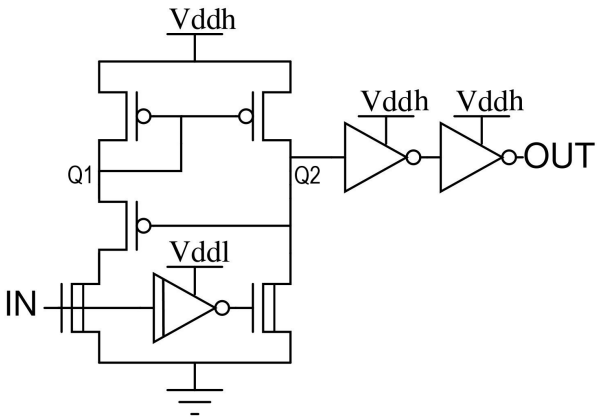


Figure 2.2: Wilson Current Mirror Level Shifter (WCMLS) [24] schematic

Unlike CCLS, CMLS operates without a cross-coupled feedback network, avoiding transitional conflicts between pull-down (PD) and pull-up (PU) MOS transistors. Hence, CMLS experiences less contention. However, because of constant static current flow in one of the current mirror branches, it experiences high static power dissipation. To enhance current stability, a current-limiting MOS can be incorporated into the reference branch at the Q1 node, resulting in the Wilson Current Mirror Level Shifter (WCMLS), as illustrated in Fig. 2.2. Here, the current-limiting MOS should work in subthreshold region properly to allow voltage transition.

2.2.3 Deep Sub-threshold Energy Efficient Level Shifter (DSELS)

DSELS is based on the CCLS feedback mechanism principle; however, it integrates an self-adaptive pull-up network to enhance switching speed. A multi-VT transistor approach is uti-

lized to improve level-shifting performance while reducing area requirements, as shown in Fig. 2.3. A unique feature of this architecture is that it uses a PMOS-NMOS cross-coupled (PNCC) current limiter, which significantly limits the current contention and leakage by developing a feedback loop. For proper operation, the PNCC PMOS must operate in the subthreshold region ($|V_{GS_p}| < |V_{T_p}|$) to regulate sufficient current flow, enabling the activation of the PNCC NMOS, which subsequently transfers 'VDDH - V_{T_n}' to its source terminal i.e. at node Z or Zb [25].

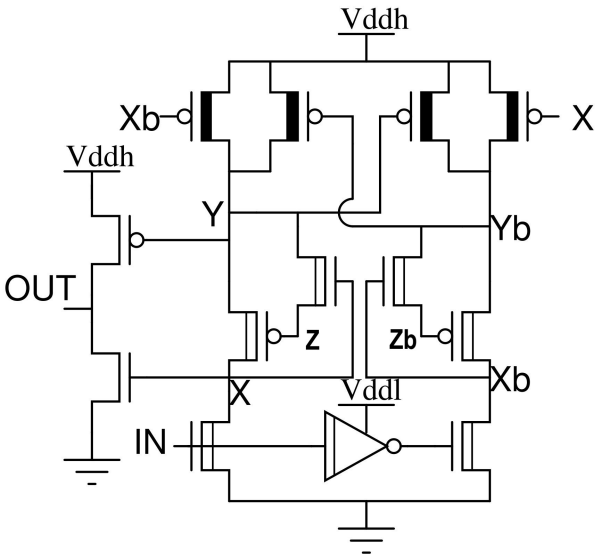


Figure 2.3: Deep Sub-threshold Energy Efficient Level Shifter (DSELS) [25] schematic

In this design, accurate transistor sizing is essential since it directly influences the threshold voltage (VT). This, in turn, defines the input voltage at the PMCC PMOS gate, given by 'VDDH - V_{T_n}', which is supplied from the PNCC NMOS source at node Z or Zb. Additionally, the output stage incorporates an inverter driven by two independent inputs, ensuring reduced leakage and improved energy efficiency. DSELS is compact and power-efficient but suffers from signal integrity issues due to floating nodes such as Z and Zb, leading to performance degradation from intra-metal parasitics. Hence, despite its smaller manufacturing area, the layout design remains complex and demands higher design efforts.

2.2.4 Robust Subthreshold Level Shifter with Wide Conversion Range (RSWCRLS)

In RSWCRLS, the CCLS design is optimized by integrating an NMOS-diode-based current limiter in the pull-up network of both branches, minimizing current contention and improving level-shifting efficiency and robustness. Introducing a current limiter in the cross-coupled PU network weakens its pull-up strength by limiting and stabilizing the current [26].

However, the NMOS-diode based current limiter causes a VT voltage drop at the internal

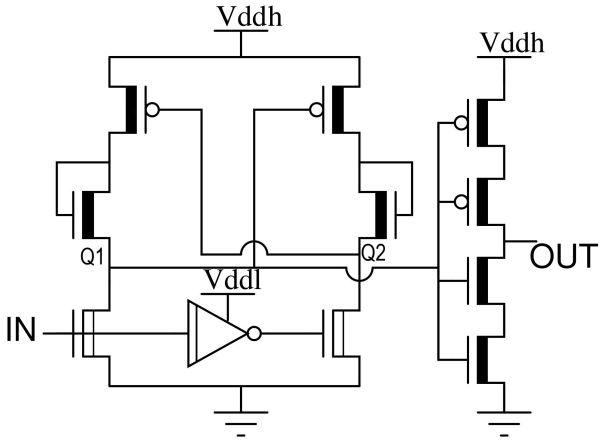


Figure 2.4: Robust Subthreshold Level Shifter with Wide Conversion Range (RSWCRLS) [26] schematic

nodes Q1 and Q2, restricting the Level Shifter's full-swing operation. Thus, causing a high short-circuit current in the circuit. To address this problem, the internal node Q1 is connected to a stacked HVT inverter setup, as illustrated in Fig. 2.4. This significantly reduces the contention.

2.2.5 Low-Power Subthreshold to Above-Threshold Voltage Level Shifter (LPSVTLS)

LPSVTLS adheres to the CCLS approach while incorporating special dynamic current generators (DCG) in the pull-up network to enhance the output transition speed. It activates automatically during input voltage level transitions. Enhancing the transition speed reduces the propagation delay [27].

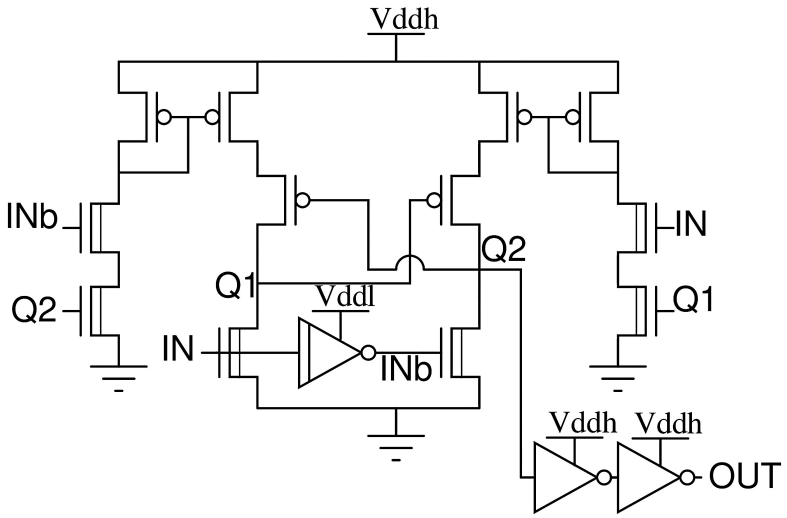


Figure 2.5: Low-Power Subthreshold to Above-Threshold Voltage Level Shifter (LPSVTLS) [27] schematic

A major benefit of this design is that DCG operates only during voltage transitions, min-

imizing static power consumption. The current generators are integrated within the cross-coupled PU network and modulates its drive strength by controlling the branch current, thereby allowing the pull-down (PD) network to stabilize the output for reliable level shifting. The schematic for this architecture is illustrated in Fig. 2.5.

2.2.6 Ultra-Wide-Range Energy-Efficient Level Shifter with CCLS/CMLS Hybrid Structure (C3MLS)

C3MLS achieves ultra-wide voltage range level shifting by combining the advantages of Cross-coupled (CCLS) and Current mirror (CMLS) based architectures [24]. It overcomes one architecture's limitations by leveraging the strengths of the other. As discussed in previous sections, CCLS-based design exhibits low static power consumption but suffers from high contention, whereas CMLS-based designs experience less contention but have higher leakage. So, in C3MLS, integrating the current mirror circuitry along with the cross-coupled network in both branches (as shown in Fig. 2.6) enhances performance while optimizing overall power dissipation.

Like LPSVTLS, this design also utilizes dynamic current generators (DCG) to significantly reduce static power consumption. However, in this configuration, the DCGs are connected in parallel with a standard CCLS topology implemented symmetrically on both sides. C3MLS also features high-threshold voltage (HVT) pull-up devices that control the strength of the PU network, ensuring smooth voltage transitions at nodes Q1 and Q2. This approach ensures reliable voltage shifting even with minimal transistor sizing.

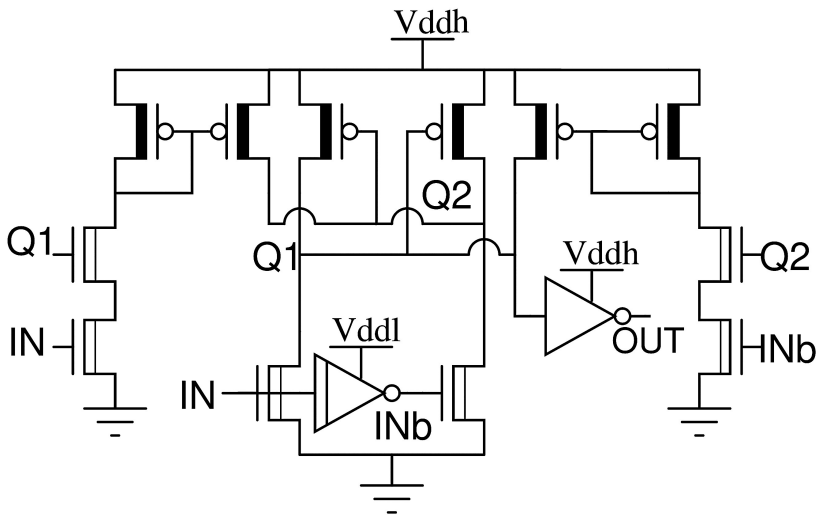


Figure 2.6: Ultra-Wide-Range Energy-Efficient Level Shifter with CCLS/CMLS Hybrid Structure (C3MLS) [24] schematic

CHAPTER 3

Post-Layout Analysis: Methodology and key Performance metrics

3.1 Performance metric significance and Methodology

As discussed in Section 1.3, the Level Shifters implemented in this work operate with two voltage supplies, VDDH and VDDL. Therefore, the following section covers the post-layout simulation methods and the importance of key Figures of Merit (FoM) for these dual-supply Level Shifters. All the selected Level Shifter architectures are designed to shift the voltage from VDDL = 0.3V to VDDH = 1.2V, operating with an external load of 100µF and a frequency of 1MHz under TT corner conditions at 25°C. The post-layout simulation observations for the chosen Level Shifters are listed in Table 3.1

3.1.1 Dynamic Power (nW)

It is the power consumed during Level Shifter's active operation, determined by the switching activity (α), operating voltage, charge consumed in the level-shifting process, and operating frequency (f_{op}). For evaluation, a α of 0.5 and an f_{op} of 1MHz were considered. In this work, the dynamic power consumption is calculated separately for VDDH and VDDL and then combined to determine the total dynamic power consumption.

3.1.2 Static Power (nW)

It is the power consumed during standby mode, i.e., when the Level Shifter is not operating. It is primarily caused by device leakage, which may arise due to parasitic effects and manufacturing non-idealities. It is calculated separately for current drawn from VDDH and VDDL, then their power contributions are combined to obtain the total static power consumption.

3.1.3 Propagation delay (ns)

For a level-shifting operation, the propagation delay is measured at the 50% transition (rise/fall) point of the output voltage waveform (OUT) relative to the 50% transition (rise/fall) point of the input voltage waveform (A). The reference waveform is shown in Fig. 1.2.

Table 3.1: Post Layout simulation observations for key Figure of Merits (FoM)

Design Version[a] **[Only M1] - I [M1+M2 GND] – II**		**Level Shifter configuration used**[b] **(CC/CM)**	**VT types used**[c]		**No. of extra masks used**[d]	**Dynamic Power (nW)**	**EPT (fJ)**	**Static Power (nW)**	**Propagation Delay (ns)**	**Area** (μm^2)	**Cell width (no. of tracks)**	**% Variations for Delay** (σ/μ)
			NMOS	***PMOS***								
CCLS [24]	I	CC	LVT	LVT	2	105	210	63.7	10.5	19.76	19	11.0% (1.15/10.44)
	II		SVT	SVT		107	214	31.6	10.8	17.68	17	10.9% (1.18/10.82)
WCMLS [24]	I	CM	LVT	LVT	2	109	218	506	15.1	9.36	9	34.7% (6.82/19.64)
	II		SVT	SVT		108	217	493	15.3	9.36	9	30.1% (5.42/18.02)
DSELS [25]	I	CC	LVT	LVT	3	8.54	17.1	4.13	33.7	12.48	12	32.2% (11.96/37.1)
	II		SVT	SVT HVT		7.6	15.2	2.07	29.9	11.44	11	30.1% (9.83/32.69)
RSWCRLS [26]	I	CC	LVT	LVT	4	5.16	10.3	11.1	13.4	10.4	10	16.8% (2.47/14.73)
	II		HVT	HVT		5	10	11.8	13.3	9.36	9	16.7% (2.42/14.53)
LPSVTLS [27]	I	CC + CM	LVT	LVT	2	26.7	53.4	3.75	14.7	17.68	17	202.9% (230.3/113.5)
	II		SVT	SVT		28.8	57.6	5.38	15.1	15.6	15	345.0% (896.4/259.8)
C3MLS [24]	I	CC + CM	LVT	LVT	3	15.1	30.3	10.6	15.9	13.52	13	28.0% (5.14/18.35)
	II		SVT	SVT HVT		14.8	29.7	12.2	15.3	11.44	11	27.7% (4.9/17.66)

[a] "Design Version" refers to the different layout implementations of a specific Level Shifter design architecture. Details of 'Version I' and 'Version II' are provided in Fig. 3.2.

[b] "Level Shifter configuration used" indicates whether a Cross-Coupled (CC) or Current Mirror (CM) configuration is implemented, impacting power consumption.

[c] STMicroelectronics 65nm technology provides the following VT device variants: High VT (HVT), Standard VT (SVT), and Low VT (LVT).

[d] "No. of extra masks" denotes the additional optical masks needed beyond a basic design for fabrication, with each extra VT requiring an additional mask.

3.1.4 No. of fabrication masks used in the design

To enhance performance while optimizing area efficiency, some Level Shifters employ a multi-threshold transistor approach. By utilizing multi-threshold variants, a designer can enhance PD NMOS strength with LVT devices, weaken PU PMOS with HVT devices, or apply both techniques to achieve the desired performance and power trade-offs. This approach enables us to effectively balance power consumption and shifting performance.

However, adopting this approach or using any additional devices like Metal-Insulator-Metal capacitor (MIMCAP) requires extra lithographic steps beyond the usual process, leading to more fabrication masks, increased manufacturing complexity, and a higher CFP. A standard fabrication process in 65nm Low Standby technology by STMicroelectronics requires 36 fabrication mask.

3.1.5 Monte-Carlo simulation for Propagation delay: σ/μ variations

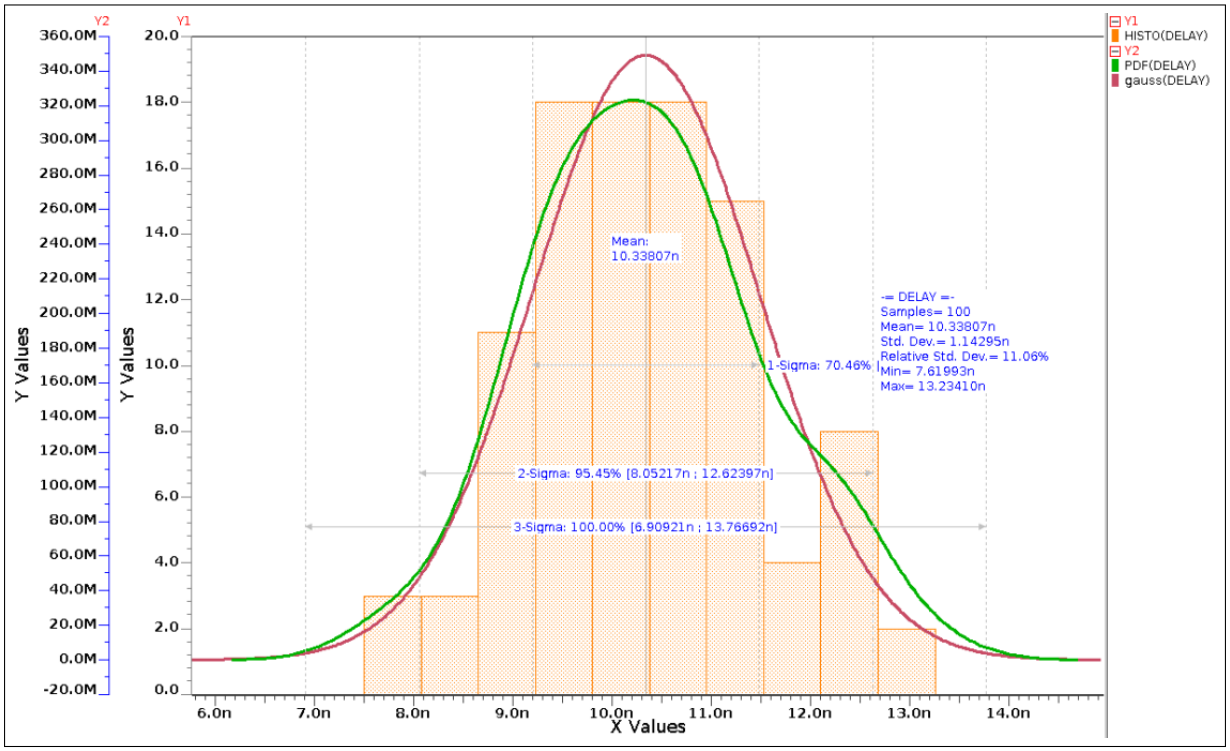


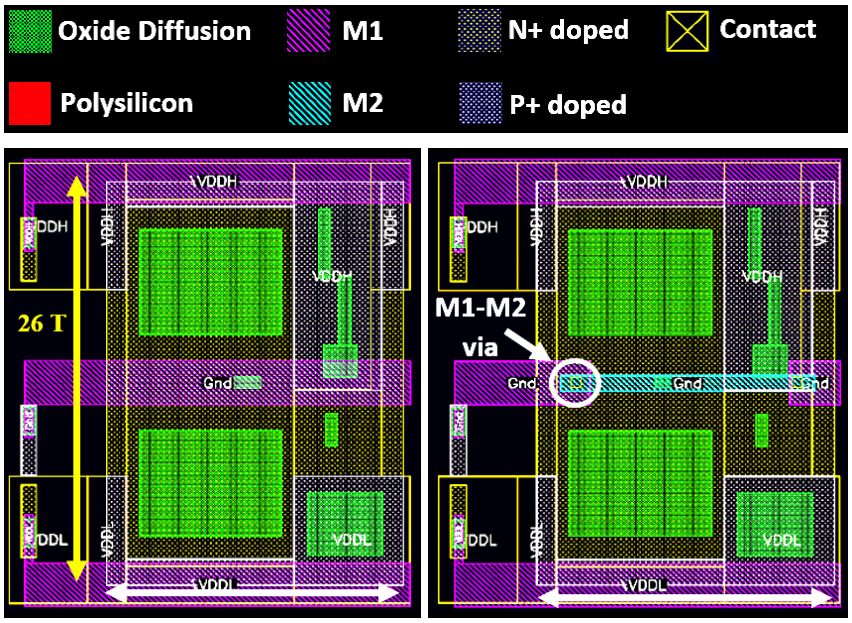
Figure 3.1: Monte-Carlo σ/μ variations for Propagation delay in CCLS design for 100 samples with μ of 10.34 ns and σ of 1.14 ns

To evaluate the impact of fabrication-induced variations on propagation delay, Monte Carlo simulations were conducted on each Level Shifter's layout through post-layout analysis. A lower σ/μ ratio may indicate higher robustness. The analysis, influenced by sample size and sigma qualification requirements, is performed using 100 samples in this work. Fig. 3.1 shows

a Monte-Carlo illustration done for CCLS design, from which it can be observed that for 100 samples, it has a μ of 10.34 ns and σ of 1.14 ns, thus having a variation of 11%. A similar analysis for all Level Shifter designs is shown in Table 3.1.

3.1.6 Design Layout Area (μm^2)

In this work, the Level Shifter layouts have been implemented in a unique double-row format. Since, in STMicroelectronics' 65nm library, standard cells are designed in a 13-Tracks (13T) single-row format, the double-row configuration here corresponds to 26-Tracks (26T) being used. The 26T design approach implemented here shares a common ground (GND) rail between the two power supply rails, VDDH and VDDL. These supply rails are routed across the 26T PR boundary to optimize area utilization. This technique is implemented in two design variants: (a) Version I, where the layout is designed using only the Metal 1 (M1), as shown in Fig. 3.2(a), and (b) Version II, where the shared ground (GND) rail is implemented using Metal 2 (M2), while all other connections remain routed through M1, as shown in Fig. 3.2(b).



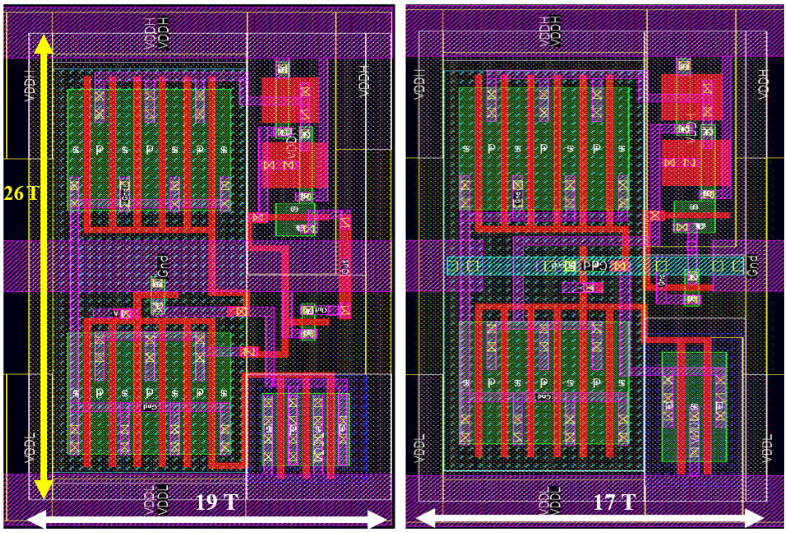
(a) (b)

Figure 3.2: (a) Version I layout (b) Version II layout. Conventions followed for designing the Level Shifter Layouts using two-row format, i.e. twice the standard 13-Tracks cell height configuration. The design layout uses a shared ground (Gnd) supply rail positioned between two power supply rails — VDDH (1.2V) and VDDL (0.3V). Each design layout has been implemented in two variations: Version I, which utilizes only Metal 1 (M1) layer for routing, and Version II, where the shared ground (Gnd) supply rail is implemented using Metal 2 (M2), while all other intra-cell connections remain routed through M1.

As shown in Fig. 3.2(b), the M2 ground (GND) rail is electrically connected to the M1 GND supply rail using M1-M2 vias, ensuring reliable conductivity. Some of the major layers used in designing the Level Shifter layouts is also shown in Fig. 3.2.

In this work different versions of each Level Shifter architecture's layout have been implemented in order to assess the impact of circuit performance, cell density, parasitic effects, and routing congestion on sustainability. A detailed discussion of these designed layouts is provided below, highlighting their role in balancing design and environmental trade-offs.

3.1.6.1 CCLS



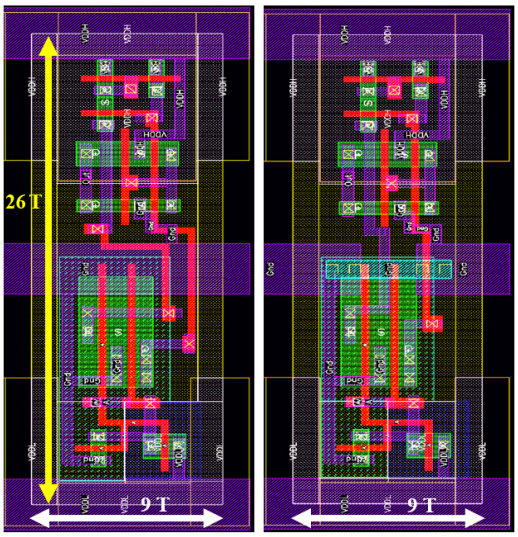
(a) (b)

Figure 3.3: (a) CCLS Version I (b) CCLS Version II. CCLS layout design variations: Version I – The routing is restricted to the M1 metal layer; thus, 19 vertical tracks (19T) are required and Version II – The GND rail is implemented using Metal 2 (M2) layer, while the remaining routing is maintained in M1, optimizing track usage to 17T.

The CCLS design layout implemented in this work incorporates additional 'VTL_N' and 'VTL_P' CAD layers, necessitating two extra lithographic masks for fabrication. As shown in Fig. 3.3, Version I of the CCLS design has a cell width of 19 vertical tracks, i.e., 19T, while Version II optimizes the width to 17T by incorporating an M2 track. This reduction in the cell width of 2 tracks significantly reduces the cell area.

3.1.6.2 WCMLS

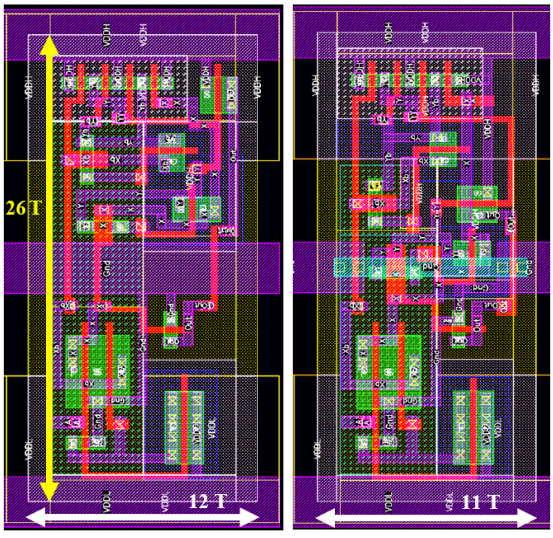
The WCMLS design layout implemented in this work incorporates additional 'VTL_N' and 'VTL_P' CAD layers, necessitating two extra lithographic masks for fabrication. As shown in Fig. 3.4, Version I of the CCLS design has a cell width of 9 vertical tracks (i.e., 9T), while Version II also retains a width of 9T even after incorporating an M2 track for layout design. This is due to the additional DRC overhead associated with M1-M2 via connections.



(a) (b)

Figure 3.4: (a) WCMLS Version I (b) WCMLS Version II. WCMLS layout design variations: Version I – The routing is restricted to the M1 metal layer; thus, 9 vertical tracks (9T) are required and Version II – The GND rail is implemented using the Metal 2 (M2) layer, while the remaining routing remains in M1; however, this did not lead to a reduction in track usage.

3.1.6.3 DSELS



(a) (b)

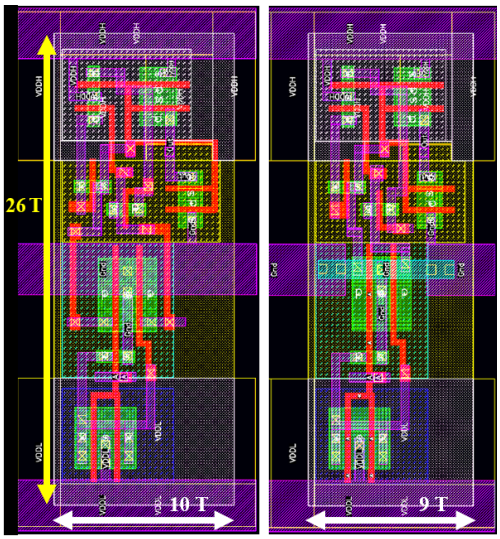
Figure 3.5: (a) DSELS Version I (b) DSELS Version II. DSELS layout design variations: Version I – The routing is restricted to the M1 metal layer; thus, 12 vertical tracks (12T) are required and Version II – The GND rail is implemented using Metal 2 (M2) layer, while the remaining routing is maintained in M1, optimizing track usage to 11T.

The DSELS design layout implemented in this work incorporates additional ‘VTL_N’, ‘VTL_P’, and ‘VTH_P’ CAD layers, necessitating three extra lithographic masks for fabrication. As shown in Fig. 3.5, Version I of the DSELS design has a cell width of 12 vertical tracks, i.e.,

12T, while Version II optimizes the width to 11T by incorporating an M2 track. This reduction in the cell width of 1 track reduces the cell area slightly.

3.1.6.4 RSWCRLS

The RSWCRLS design layout implemented in this work incorporates additional 'VTL_N', 'VTL_P', 'VTH_N', and 'VTH_P' CAD layers, necessitating four extra lithographic masks for fabrication. As shown in Fig. 3.6, Version I of the RSWCRLS design has a cell width of 10 vertical tracks, i.e., 10T, while Version II optimizes the width to 9T by incorporating an M2 track. This reduction in the cell width of 1 track reduces the cell area slightly.

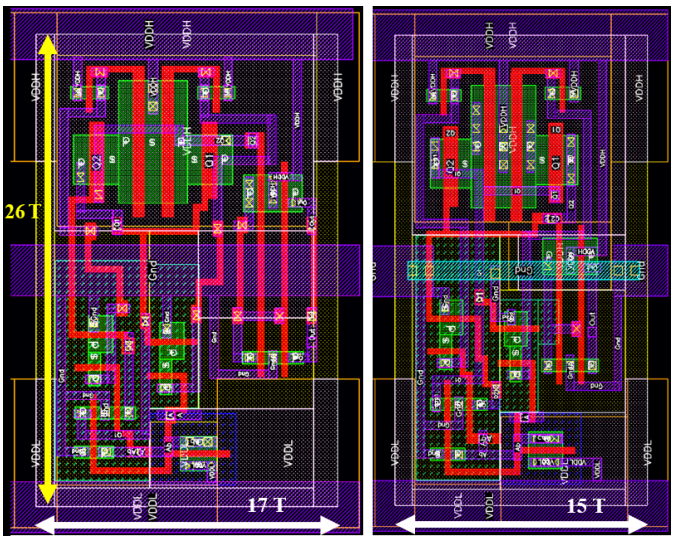


(a) (b)

Figure 3.6: (a) RSWCRLS Version I (b) RSWCRLS Version II. RSWCRLS layout design variations: Version I – The routing is restricted to the M1 metal layer; thus, 10 vertical tracks (10T) are required and Version II – The GND rail is implemented using Metal 2 (M2) layer, while the remaining routing is maintained in M1, optimizing track usage to 9T.

3.1.6.5 LPSVTLS

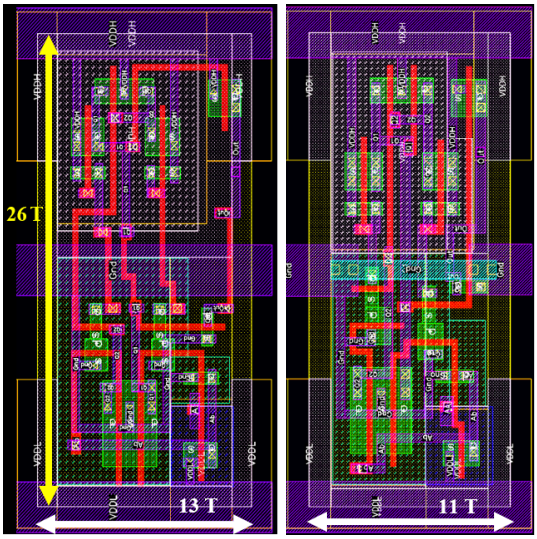
The LPSVTLS design layout implemented in this work incorporates additional 'VTL_N' and 'VTL_P' CAD layers, necessitating two extra lithographic masks for fabrication. As shown in Fig. 3.7, Version I of the LPSVTLS design has a cell width of 17 vertical tracks, i.e., 17T, while Version II optimizes the width to 15T by incorporating an M2 track. This reduction in the cell width of 2 tracks significantly reduces the cell area.



(a) (b)

Figure 3.7: (a) LPSVTLS Version I (b) LPSVTLS Version II. LPSVTLS layout design variations: Version I – The routing is restricted to the M1 metal layer; thus, 17 vertical tracks (17T) are required and Version II – The GND rail is implemented using Metal 2 (M2) layer, while the remaining routing is maintained in M1, optimizing track usage to 15T.

3.1.6.6 C3MLS



(a) (b)

Figure 3.8: (a) C3MLS Version I (b) C3MLS Version II. C3MLS layout design variations: Version I – The routing is restricted to the M1 metal layer; thus, 13 vertical tracks (13T) are required and Version II – The GND rail is implemented using Metal 2 (M2) layer, while the remaining routing is maintained in M1, optimizing track usage to 11T.

C3MLS layouts implemented in this work incorporate additional 'VTL_N', 'VTL_P', & 'VTH_P' CAD layers, necessitating 3 extra lithographic masks for fabrication. As shown in Fig. 3.8, C3MLS Version I has a cell width of 13 vertical tracks, i.e., 13T, while Version II optimizes it to 11T by using the M2 track. The reduction of 2 tracks in cell width notably reduces cell area.

CHAPTER 4

Sustainability Metric and Evaluation

4.1 Proposed Sustainability Metrics

In Section 1.2, the classification and components of carbon footprint/emission were briefly discussed. In this section, the developed sustainability evaluation metric is discussed in detail and validated on the selected set of Level Shifter Designs for IoT, Automotive (Auto), High-Performance Computing (HPC) and Portable Electronics (PE) applications. These metrics are designed to be designer-centric, enabling sustainability-aware decisions when selecting the most environmentally friendly Level Shifter for SoC integration. It will allow designers to estimate the manufacturing (embodied) and operational emissions associated with a computing standard cell, such as the Level Shifter.

The metrics report the footprint in units of energy (mWh), which can be converted to equivalent CO_2 as required. The developed metrics are as follows:

4.1.1 Embodied carbon footprint (eCFP) metric

The embodied footprint includes emissions generated during the manufacturing process and the extraction of raw materials for hardware fabrication. In this work, we have modeled the fabrication-related embodied emission estimation using Eq. (4.1).

$$\begin{aligned}\text{eCFP} = &(\text{Base Fabrication Energy}) \times (\text{Cell Area}) \times (\text{Extra Metal layer usage Impact}) \\ &\times (\text{Extra Processing Step Impact}) \times (\text{Porosity Impact})\end{aligned} \tag{4.1}$$

Each component shown in Eq. (4.1) is elaborated in the following sections.

4.1.1.1 Base Fabrication Energy per μm^2 of Silicon

It represents the average energy consumption per unit area (μm^2), derived from the total energy used in standard wafer fabrication and normalized by the wafer surface area, as expressed in Eq. (4.2). In this work, the energy required to fabricate a 300mm diameter wafer with a 6-metal layer stack in a standard 65nm process is considered to be 4204 kWh per wafer as per [22].

$$\text{Base Fabrication Energy per } \mu m^2 = \frac{\text{Standard wafer energy consumption}}{\text{Total wafer surface area } (\mu m^2)} \tag{4.2}$$

4.1.1.2 Cell Area

The Embodied footprint depends majorly on the silicon area. Hence eCFP in Eq. (4.1) is directly proportional to the layout area of the Level Shifter cell. In this work, the cell area is considered in μm^2. A larger cell or SoC area would allow fewer dies to be manufactured per wafer. Hence, the energy per die would increase.

4.1.1.3 Extra Metal layer usage Impact

In any technology, standard cells are implemented using the lowest available metal layer. For instance, in STM 65nm technology, M1 serves as the lowest available metal layer. Designing a standard cell in the lowest metal layer may result in larger area consumption. Incorporating upper metal layers (here, for instance, Metal 2 or M2) alongside the lowest layer in standard cell design (M1) can result in a denser layout. Although this area reduction may reduce manufacturing energy consumption, it also limits the available routing tracks for SoC interconnections, thus causing congestion. This increased congestion can lead to higher fabrication complexity and, ultimately, a greater embodied footprint.

$$\text{Extra Metal layer usage Impact} = 1 + \left(\frac{\text{Total tracks available in M2 metal layer}}{\text{Tracks available for routing in M2 metal layer}} - 1 \right) \times \text{CF} \tag{4.3}$$

Eq. (4.3) represents the congestion impact on the cell-level embodied footprint. Since congestion contributes incrementally to the environmental impact, the additional track usage is considered an additive effect in the embodied footprint estimation. This additive term includes a multiplication factor, CF (congestion factor), which represents the proportional impact of additional track utilization. In this work, it is considered to be 0.3 based on certain observations derived from experiments on RISC-V to consider the impact of an additional metal track.

4.1.1.4 Extra Processing Step Impact

As discussed in Section 3.1.4, incorporating VT device variants like LVT and HVT in Level Shifters necessitates additional lithography masks. Each extra mask increases fabrication complexity and energy consumption, thereby contributing to a higher embodied footprint. Eq. (4.4) shows how to estimate the impact of extra mask usage on the embodied footprint.

$$\text{Extra Processing Step Impact} = ((\text{Total masks} - \text{Reference masks}) \times \text{Mask Factor}) + 1 \quad (4.4)$$

Here, the Mask Factor is a multiplier that quantifies the proportional impact of each additional mask. In this work, the Mask Factor is set to 0.045, meaning each additional mask is estimated to contribute an average impact of $\sim$4.5%. This factor is derived from estimates as per [22], which indicate a $\sim$18% rise in energy consumption when transitioning from a 6-layer (4204 kWh) to an 8-layer (4895 kWh) metal stack at the 65nm node. This increase corresponds to the use of four additional masks—one metal and one via mask per added metal layer. Furthermore, the reference number of masks used in standard wafer fabrication for STMicroelectronics 65nm technology, according to the Design Rule Manual, is 36.

4.1.1.5 Porosity Impact

Porosity is a design concept that is used in macros, especially in memories. It typically refers to the availability of free space or metal tracks in the lower metal layers of the layout, which can later be utilized for inter-cell routing purposes. Porosity is usually considered for the metal layer below the topmost layer used in the design of the macro-layout. If porosity is present in a design, it can be interpreted as a reduction in fabrication complexity for the individual macro. This is because the porous tracks are utilized for intercell routing rather than contributing to the current macro's layout. As a result, the fabrication energy demand is lessened, indicating a lowered or even favorable impact on the embodied energy.

Eq. (4.5) models the impact of porosity, where POF denotes the Porosity Factor, representing the contribution of each porous track to overall fabrication energy consumption. It is set to 1 based on experimental observations, but may vary with actual industrial data. However, as discussed, this concept primarily applies to macros or memories, since standard cells such as Level Shifters, built predominantly on the lowest metal layer, exhibit no porosity. Therefore, the number of porous tracks available for routing is zero, resulting in a 'Porosity Impact' value of 1, i.e., no porosity contribution in Embodied Footprint here.

$$\text{Porosity Impact} = 1 - \left(\frac{\text{No. of porous tracks available for routing}}{\text{Total no. of tracks in the porous metal layer}}\right) \times \text{POF} \quad (4.5)$$

4.1.2 Operational carbon footprint (oCFP) metric

The operational footprint includes emissions generated during the operating lifespan of a hardware system. It accounts for dynamic, static/biasing, and leakage power consumption emissions across different operational phases of the IC's total operating time (T_{total}) as shown in Eq. (4.6). The lifespan is categorized into 3 operational phases: Active, Standby, and Switched-off. Another operational phase, known as 'retention', involves lowering the supply voltage when the circuit is idle, allowing stored data to be retained. However, since Level Shifters do not support retention functionality, this mode is neither discussed nor considered in the formulas and analysis presented here.

$$\text{oCFP} = T_{\text{total}} \times (\text{Dynamic power} + \text{Static power} + \text{Leakage power}) \tag{4.6}$$

These operational phases are measured as proportions of the total operating time (T_{total}), defined as Active Time Ratio (ATR), Standby Time Ratio (STR), and Switched-off Time Ratio (SOTR) respectively. These ratios and total operating time can differ based on the chosen usage application like IoT, Automotive (Auto), High-Performance Computing (HPC), and Portable Electronics (PE). In this work, Level Shifters were implemented in 65nm STMicroelectronics technology and analyzed initially to meet specifications for IoT applications. Hence, for sustainability paradigm validation of Level Shifters in IoT applications, here ATR, STR, SOTR, and T_{total} were considered 5%, 25%, 70%, and 20000 hours, respectively. The operating times and ratios for other applications are also listed in Table 4.1. While the provided ratios are hypothetical, actual values for ATR, STR, and SOTR for intended applications can be obtained from the respective domain experts or responsible teams within the relevant industry.

Table 4.1: Operating lifetime and Time ratio % for operational phases based on usage Application

Operating Phases	**Time Ratios based on Application**			
	IoT	***HPC***	***Auto***	***PE***
Active (ATR)	5%	40%	15%	10%
Stand-by (STR)	25%	40%	45%	30%
Switched-off (SOTR)	70%	20%	40%	60%
Operational Lifetime in hours (T_{total})	20000	25000	10000	35000

The oCFP metric components in Eq. (4.6) are further explained in the following sections.

4.1.2.1 Dynamic Power

Dynamic power is the power consumed by a Level Shifter during the active operational phase of its lifespan i.e. when it is level shifting the input voltage signal. As shown in Eq. (4.7), the Dynamic power emissions are estimated for the ATR of T_{total} i.e. only for active mode and depend on the switching activity (α), active mode operating voltage (V_{active}), charge consumed in the level-shifting process (Q_{dyn}), and operating frequency (f_{op}).

$$\text{Dynamic power} = Q_{\text{dyn}} \times \alpha \times V_{\text{active}} \times f_{\text{op}} \times \frac{\text{ATR}}{100} \tag{4.7}$$

4.1.2.2 Static Power

Static power is the power consumed by a circuit during its steady state to maintain the necessary biasing within the circuit, as shown in Eq. (4.8). It is calculated by summing the biasing consumptions associated with all the power supplies present in the circuit. This component is considered only in circuits where a constant biasing current (I_{static}) is drawn from the biasing voltage (V_{static}); otherwise, I_{static} is assumed to be zero, causing the static power component to become 0. Since the chosen set of Level Shifters does not require biasing, the bias current is zero, and consequently, the static power consumption is also zero.

$$\text{Static power} = \sum V_{\text{static}} \times I_{\text{static}} \tag{4.8}$$

4.1.2.3 Leakage Power

Leakage power is the power dissipated due to device leakages in a Level Shifter, even when the circuit is not actively switching. Leakage power is consumed during both active and standby modes. Hence, as shown in Eq. (4.9), its estimation accounts for active and standby ratios, i.e., ATR and STR, respectively. The metric can be extended to include leakage during the retention phase; however, as previously mentioned, retention is not relevant to Level Shifter analysis and is therefore excluded from the equation.

$$\begin{aligned}\text{Leakage power} = &\left[I_{\text{active}} \times V_{\text{active}} \times \left(\frac{\text{ATR}}{100} \times \text{PF}^{\,\text{PWM}} \right) \right] \\ &+ \left[I_{\text{standby}} \times V_{\text{standby}} \times \left(\frac{\text{STR}}{100} + \left(\text{PWM} \times \frac{\text{ATR}}{100} \times (1 - \text{PF}) \right) \right) \right]\end{aligned} \tag{4.9}$$

Here, I_{active} represents the leakage current drawn during the active operation mode from the active mode supply (V_{active}), and I_{standby} represents the leakage current drawn during the standby operation mode from the standby mode supply (V_{standby}).

Furthermore, here, a concept of Performance factor (PF) is introduced, which allows for accounting for systems that integrate Pulse Width Modulation. It is a specialized technique in which the circuit's voltage supply level may be reduced after the required computation is completed, effectively shortening the active mode duration and leakage. After this, the circuit transitions into standby mode, thus reducing active mode power consumption.

$$\text{PF} = \frac{\text{Time taken by a given Level Shifter to perform shifting operation}}{\text{Time taken by a reference Level Shifter to perform the same operation (Worst delay)}} \quad (4.10)$$

As shown in Eq. (4.10), PF represents the time ratio of a given design that completes an operation compared to the reference design that performs the same operation in the worst time (will be taken as reference time). Thus, PF translates the performance delay-based active-to-standby transition capability of a circuit relative to the reference circuit into a time ratio. This enables designers to benchmark new Level Shifter designs against a reference design that exhibits the worst-case delay in performing the level shifting operation. To enable this modulation analysis, a boolean variable, PWM, needs to be set to 1.

4.2 Sustainability evaluation Observations and trends in Level Shifters

This section validates the proposed sustainability metrics using the selected Level Shifter designs. The analysis begins with eCFP metric trends, followed by oCFP metric trends, and concludes with a comprehensive evaluation of both. This approach enables designers to select a sustainability-aware Level Shifter design based on specific requirements and usage scenarios.

4.2.1 Embodied footprint related

This section showcases the calculation of the previously proposed embodied footprint metric (eCFP) for Level Shifters, along with its component data and observed trends. Table 4.2 provides the necessary Level Shifters data for estimating the embodied footprint (eCFP) using Eq. (4.1).

For instance, Version I of CCLS has a cell area of 19.76 μm^2, uses 2 additional VT-related

fabrication masks, and does not use any M2 tracks, thus resulting in an eCFP of 1.282 mWh. While Version II of CCLS has a cell area of 17.68 μm^2, it uses 2 additional VT-related fabrication masks and 2 additional M2 tracks (as the single M2 track drawn in Version II has a width equal to twice that of 2 M2 tracks), resulting in an eCFP of 1.175 mWh.

Similar eCFP estimations can be made for other designs and their versions using the data presented in Table 4.2.

Table 4.2: Embodied footprint experimental data for Level Shifter architectures

Level Shifter Design	**Design Version**	**Cell Area (μm^2)**	**No. of Additional fabrication masks**	**No. of Total fabrication masks**	**Upper metal routing layer**	**Total tracks in upper metal layer**	**Tracks remaining in upper metal layer**	**Embodied footprint 'eCFP' (mWh)**
CCLS	I	19.76	2	38	M2	26	26	1.282
	II	17.68	2	38	M2	26	24	1.175
WCMLS	I	9.36	2	38	M2	26	26	0.607
	II	9.36	2	38	M2	26	24	0.622
DSELS	I	12.48	3	39	M2	26	26	0.843
	II	11.44	3	39	M2	26	24	0.792
RSWCRLS	I	10.4	4	40	M2	26	26	0.730
	II	9.36	4	40	M2	26	24	0.674
LPSVTLS	I	17.68	2	38	M2	26	26	1.147
	II	15.6	2	38	M2	26	24	1.037
C3MLS	I	13.52	3	39	M2	26	26	0.913
	II	11.44	3	39	M2	26	24	0.792

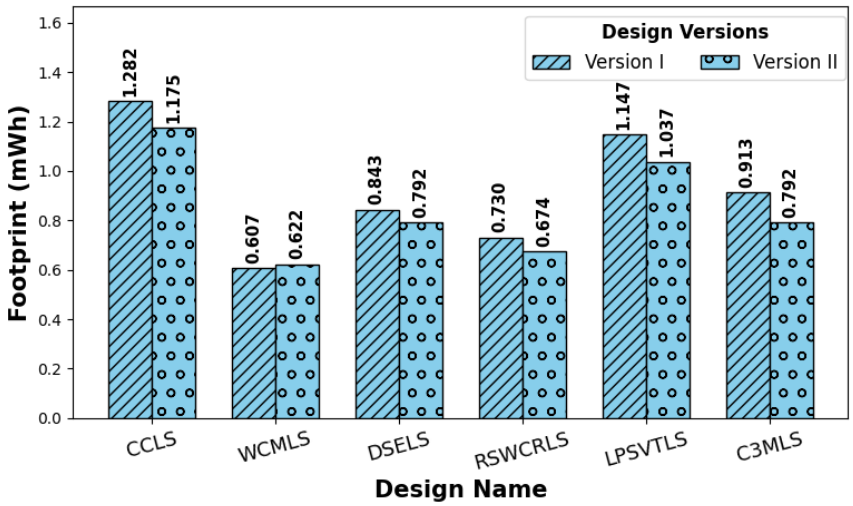


Figure 4.1: Embodied footprint (eCFP) for Version I and II of CCLS, WCMLS, DSELS, RSWCRLS, LPSVTLS, and C3MLS Level Shifters

The estimated eCFP values for all the Level Shifter designs and versions are plotted in Fig. 4.1. The following subsections explain the impact of area, additional mask usage, congestion on eCFP and other trends observed related to it from Fig. 4.1.

4.2.1.1 Area impact

The Level Shifter, which has less cell area, will tend to have a lesser Embodied footprint. This can be inferred from Table 4.2 and Fig. 4.1, where Version I of CCLS has a cell area of 19.76 μm^2, while Version I of WCMLS has a cell area of 9.36 μm^2, resulting in eCFP values of 1.282 mWh and 0.607 mWh, respectively. Similar observations can be seen in other designs, Versions I and II, as well.

4.2.1.2 Additional metal layer usage impact (congestion)

The Level Shifter Version II uses an additional M2 routing track compared to Version I of the Level Shifter. This may decrease the cell area; however as discussed in Section 4.1.1.3, it may lead to higher congestion and hence higher complexity of fabrication. This can be inferred from Table 4.2 and Fig. 4.1, where Version I and II of WCMLS have the same cell area of 9.36 μm^2. However, due to the additional M2 track usage in Version II, its eCFP is estimated to be 622 μWh, which is 15 μWh higher than that of Version I.

4.2.1.3 Additional mask usage impact

As discussed in Section 4.1.1.4, some Level Shifters use VT variant devices to enhance their performance while maintaining the optimal area. This approach increases the lithography steps or mask count, leading to higher fabrication complexity and, consequently, a higher eCFP. This can be inferred from Table 4.2 and Fig. 4.1, where Version II of WCMLS and RSWCRLS have the same cell area of 9.36 μm^2 and the same congestion impact. However, due to the 2 additional VT mask usage in the RSWCRLS version, its eCFP is estimated to be 674 μWh, which is 52 μWh higher than that of WCMLS.

4.2.1.4 Worst eCFP based design

From Fig. 4.1, it can be observed that both versions of the CCLS design exhibit the highest eCFP, likely due to their larger area footprint. Therefore, CCLS is the least sustainable design choice in terms of manufacturing impact.

4.2.1.5 Best eCFP based design

From Fig. 4.1, it can be observed that both versions of the WCMLS design exhibit the least eCFP, likely due to their least area footprint. Therefore, WCMLS emerges as the most sustainable design choice in terms of manufacturing impact.

4.2.2 Operational footprint related

This section showcases the calculation of the proposed operational footprint metric (oCFP) for Level Shifters, along with its component data and observed trends. Table 4.3 provides the necessary Level Shifters data for estimating the operational footprint (oCFP) for an IoT application with α = 0.3 & f_{op} = 100 MHz using Eq. (4.6).

Table 4.3: Level Shifters Operational footprint for IoT application with α = 0.3 & f_{op} = 100 MHz

Level Shifter Design	**Design Version**	**A = Time taken for a operation in present design (ns)**	**B = Time taken for same operation in reference design (ns)**	**Performance factor (PF) = A/B**	**Leakage power (for VDDH and VDDL) (nW)**	**Dynamic power (for VDDH and VDDL) (nW)**	**Operational footprint 'oCFP' (mWh)**
CCLS	I	10.5	33.7	0.311	19.101	6334.478	6.717
	II	10.8	33.7	0.32	9.478	6443.476	6.633
WCMLS	I	15.1	33.7	0.448	151.878	6529.143	9.567
	II	15.3	33.7	0.454	148.041	6498.769	9.46
DSELS	I	33.7	33.7	1.0	1.239	520.502	0.545
	II	29.9	33.7	0.887	0.622	463.913	0.476
RSWCRLS	I	13.4	33.7	0.398	3.333	317.513	0.384
	II	13.3	33.7	0.395	3.526	310.817	0.381
LPSVTLS	I	14.7	33.7	0.436	1.126	1607.431	1.63
	II	15.14	33.7	0.449	1.614	1730.321	1.763
C3MLS	I	15.9	33.7	0.472	3.183	934.629	0.998
	II	15.3	33.7	0.454	3.65	891.758	0.965

In this section and Table 4.3, an IoT application with switching activity (α) of 0.3 and an operating frequency (f_{op}) of 100 MHz is considered the target usage scenario for the oCFP estimation and analysis. The corresponding oCFP values for all the Level Shifter designs and versions are plotted in Fig. 4.2. The following subsections explain the impact of operational performance on oCFP and other trends observed related to it from Fig. 4.2.

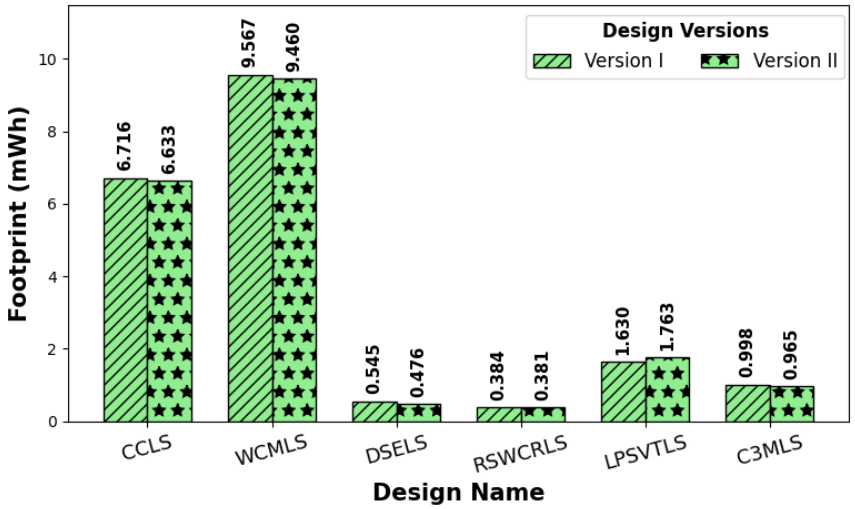


Figure 4.2: Operational footprint (oCFP) for Version I and II of CCLS, WCMLS, DSELS, RSWCRLS, LPSVTLS, and C3MLS Level Shifters for IoT application with α = 0.3 and f_{op} = 100 MHz

4.2.2.1 Dynamic consumption impact

As discussed in Section 4.1.2.2, dynamic consumption is dependent on switching activity and operating frequency which can differ based on usage application. Consequently, variations in these factors can lead to differences in dynamic power consumption. The dynamic power consumption for the selected set of Level Shifters is shown in Table 4.3. These values are reported for a single IoT target application with a switching activity factor (α) of 0.3 and an operating frequency (f_{op}) of 100 MHz. It can be observed from the table that conventional Level Shifters, CCLS and WCMLS, consume 5 to 10 times more dynamic power compared to advanced Level Shifter designs.

4.2.2.2 Leakage consumption impact

As discussed in Section 4.1.2.3, leakage consumption depends on the time a circuit remains in active or standby operating mode. In this application, as discussed before, IoT timing ratios are followed with V_{active} = 1.2V and V_{standby} = 1.2V for analysis. The leakage power consumption for the selected Level Shifters is shown in Table 4.3. From the table, it can be observed that the conventional Level Shifter, WCMLS, exhibits the highest leakage among all designs.

4.2.2.3 Worst oCFP based design

From Fig. 4.2, it can be observed that both versions of the WCMLS design exhibit the highest oCFP, due to their high operational power consumption. Therefore, in the long term, WCMLS is the least sustainable design choice in terms of operational impact for the intended IoT applications.

4.2.2.4 Best oCFP based design

From Fig. 4.2, it can be observed that both versions of the RSWCRLS design exhibit the least oCFP, due to their lower operational power consumption. Therefore, in the long term, RSWCRLS emerges as the most sustainable design choice in terms of operational impact for the intended IoT applications.

4.2.3 Total footprint related

Table 4.4: Summarized Footprints for Level Shifters for IoT application with α = 0.3 & f_{op} = 100 MHz

Level Shifter Design	Design Version	Embodied footprint 'eCFP' (mWh)	Operational footprint 'oCFP' (mWh)	Total footprint (mWh)
CCLS	I	1.282	6.717	7.998
	II	1.175	6.633	7.808
WCMLS	I	0.607	9.567	10.174
	II	0.622	9.460	10.082
DSELS	I	0.843	0.545	1.388
	II	0.792	0.476	1.268
RSWCRLS	I	0.730	0.384	1.114
	II	0.674	0.381	1.055
LPSVTLS	I	1.147	1.630	2.777
	II	1.037	1.763	2.800
C3MLS	I	0.913	0.998	1.911
	II	0.792	0.965	1.757

In Sections 4.2.1 and 4.2.2, the individual impacts of manufacturing and operational footprints for each Level Shifter design were analyzed. However, this section examines their combined effect on sustainability for an IoT application with α = 0.3 and operating frequency f_{op} = 100 MHz. It highlights how the selection of a sustainable Level Shifter design varies depending on user requirements and objectives. Table 4.4 provides the summarized eCFP, oCFP, and total CFP for IoT application with α = 0.3 and f_{op} = 100 MHz. These values are plotted in Fig. 4.3

4.2.3.1 Worst Total CFP based design

From Fig. 4.3, it can be observed that both versions of the WCMLS design have the highest Total CFP, making it the least sustainable design choice for the intended IoT applications.

4.2.3.2 Best Total CFP based design

From Fig. 4.3, it can be observed that both versions of the RSWCRLS design have the lowest Total CFP, making it the most sustainable design choice for the intended IoT applications.

4.2.3.3 Conventional vs advanced Level Shifters CFP

Figure 4.3 shows that the total CFP for conventional Level Shifters is approximately 3 to 10 times greater than that of advanced Level Shifter designs. Hence, the advanced Level Shifters appear to be much more sustainable than the conventional ones.

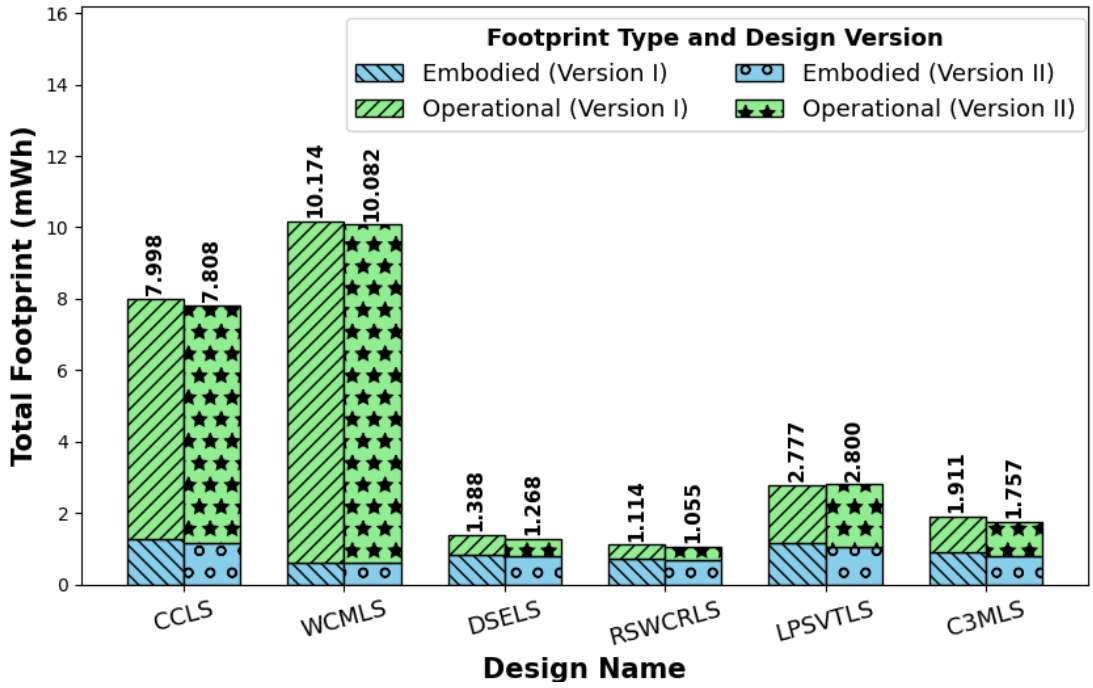


Figure 4.3: Total footprint for Version I and II of CCLS, WCMLS, DSELS, RSWCRLS, LPSVTLS, and C3MLS Level Shifters for IoT application with α = 0.3 and f_{op} = 100 MHz

4.2.3.4 Comparative order of sustainability

Figures 4.1, 4.2, and 4.3 illustrate the comparative sustainability of different Level Shifter designs based on eCFP, oCFP, and Total Footprint. The increasing order of sustainability-aware Level Shifter selection priority for IoT application with α = 0.3 and f_{op} = 100 MHz is summarized in Table 4.5. Here, each design is represented with a distinct color to visualize its ranking across eCFP, oCFP, and Total Footprint. In this IoT application usage, it is evident that oCFP plays a dominant role in determining the Total CFP.

This demonstrates that the proposed metrics enable designers to identify the most sustainable Level Shifter based on specific client requirements.

Table 4.5: Comparative Sustainability Ranking of Level Shifters for IoT application with α = 0.3 and f_{op} = 100 MHz based on different types of Footprint

Design order of CFP (Increasing) / CFP type	Embodied footprint 'eCFP' (mWh)	Operational footprint 'oCFP' (mWh)	Total footprint (mWh)
1	WCMLS I	RSWCRLS II	RSWCRLS II
2	WCMLS II	RSWCRLS I	RSWCRLS I
3	RSWCRLS II	DSELS II	DSELS II
4	RSWCRLS I	DSELS I	DSELS I
5	DSELS II	C3MLS II	C3MLS II
6	C3MLS II	C3MLS I	C3MLS I
7	DSELS I	LPSVTLS I	LPSVTLS I
8	C3MLS I	LPSVTLS II	LPSVTLS II
9	LPSVTLS II	CCLS II	CCLS II
10	LPSVTLS I	CCLS I	CCLS I
11	CCLS II	WCMLS II	WCMLS II
12	CCLS I	WCMLS I	WCMLS I

4.2.4 Footprint trends for other Application Usage and Domains

In Sections 4.2.1, 4.2.2, and 4.2.3, a sustainability analysis was performed for the Level Shifters, targeting IoT applications with $\alpha = 0.3$ and $f_{op} = 100$ MHz. This validated the proposed metrics' effectiveness, with Table 4.5 highlighting sustainability-based preferences among Level Shifter designs for this scenario. However, this section extends validation of these metrics across broader usage scenarios, including multiple IoT cases and other application domains: Automotive (Auto), High-Performance Computing (HPC), and Portable Electronics (PE).

Table 4.6 presents the estimated Footprint values for the validated range of usage scenarios and applications. It includes five IoT usage scenarios (combinations of α and f_{op}) with respective time ratios, along with three additional application domains: Automotive, High-Performance Computing, and Portable Electronics. A comparative CFP ranking of the selected set of Level Shifters, based on the increasing CFP values derived from the proposed metrics, is presented in Table 4.7. The same color encoding used in Table 4.5 is applied here to represent each design.

From Table 4.7, it can be observed that in certain scenarios, the sustainability-based CFP ranking of the Level Shifters varies due to the cumulative impact of eCFP and oCFP values. Hence, by using these metrics, a designer can make a more well-informed choice while integrating them into an SoC based on the intended target application.

Table 4.6: Estimated Footprints for Level Shifters with other target Application and usage scenarios

Level Shifter Design	**Design Version**	**Embodied footprint 'eCFP' (mWh)**	**Total footprint (mWh)**							
			IoT					**Auto**	**HPC**	**PE**
			α **= 0.001** f_{op} **= 0.5 MHz**	α **= 0.01** f_{op} **= 0.5 MHz**	α **= 0.1** f_{op} **= 1 MHz**	α **= 0.1** f_{op} **= 50 MHz**	α **= 0.3** f_{op} **= 100 MHz**	α **= 0.1** f_{op} **= 2000 MHz**	α **= 0.2** f_{op} **= 3000 MHz**	α **= 0.05** f_{op} **= 1000 MHz**
CCLS	I	1.282	1.664	1.665	1.685	2.718	7.997	65.007	1269.450	39.123
	II	1.175	1.365	1.366	1.386	2.443	7.813	65.804	1290.508	39.209
WCMLS	I	0.607	3.645	3.646	3.666	4.733	10.174	68.936	1316.562	45.781
	II	0.622	3.583	3.584	3.605	4.666	10.082	68.571	1310.246	45.440
DSELS	I	0.843	0.868	0.868	0.869	0.955	1.388	6.073	105.026	3.937
	II	0.792	0.804	0.804	0.806	0.882	1.268	5.444	93.616	3.527
RSWCRLS	I	0.730	0.797	0.797	0.798	0.850	1.114	3.972	64.455	2.738
	II	0.674	0.744	0.744	0.745	0.796	1.055	3.853	63.073	2.652
LPSVTLS	I	1.147	1.169	1.170	1.175	1.440	2.780	17.247	322.712	10.579
	II	1.037	1.069	1.070	1.075	1.361	2.803	18.376	347.212	11.209
C3MLS	I	0.913	0.977	0.977	0.980	1.132	1.911	10.323	188.051	6.514
	II	0.792	0.865	0.865	0.868	1.014	1.757	9.783	179.387	6.164

Table 4.7: Comparative Sustainability Ranking of Level Shifters for other target applications and usage scenarios

Increasing order of Design's CFP	**Embodied footprint 'eCFP' (mWh)**	**Total footprint (mWh)**							
		IoT					**Auto**	**HPC**	**PE**
		α = **0.001** f_{op} = **0.5 MHz**	α = **0.01** f_{op} = **0.5 MHz**	α = **0.1** f_{op} = **1 MHz**	α = **0.1** f_{op} = **50 MHz**	α = **0.3** f_{op} = **100 MHz**	α = **0.1** f_{op} = **2000 MHz**	α = **0.2** f_{op} = **3000 MHz**	α = **0.05** f_{op} = **1000 MHz**
1	WCMLS I	RSWCRLS II	RSWCRLS II	RSWCRLS II	RSWCRLS II	RSWCRLS II	RSWCRLS II	RSWCRLS II	RSWCRLS II
2	WCMLS II	RSWCRLS I	RSWCRLS I	RSWCRLS I	RSWCRLS I	RSWCRLS I	RSWCRLS I	RSWCRLS I	RSWCRLS I
3	RSWCRLS II	DSELS II	DSELS II	DSELS II	DSELS II	DSELS II	DSELS II	DSELS II	DSELS II
4	RSWCRLS I	C3MLS II	C3MLS II	C3MLS II	DSELS I	DSELS I	DSELS I	DSELS I	DSELS I
5	DSELS II	DSELS I	DSELS I	DSELS I	C3MLS II	C3MLS II	C3MLS II	C3MLS II	C3MLS II
6	C3MLS II	C3MLS I	C3MLS I	C3MLS I	C3MLS I	C3MLS I	C3MLS I	C3MLS I	C3MLS I
7	DSELS I	LPSVTLS II	LPSVTLS II	LPSVTLS II	LPSVTLS II	LPSVTLS I	LPSVTLS I	LPSVTLS I	LPSVTLS I
8	C3MLS I	LPSVTLS I	LPSVTLS I	LPSVTLS I	LPSVTLS I	LPSVTLS II	LPSVTLS II	LPSVTLS II	LPSVTLS II
9	LPSVTLS II	CCLS II	CCLS II	CCLS II	CCLS II	CCLS II	CCLS I	CCLS I	CCLS I
10	LPSVTLS I	CCLS I	CCLS I	CCLS I	CCLS I	CCLS I	CCLS II	CCLS II	CCLS II
11	CCLS II	WCMLS II	WCMLS II	WCMLS II	WCMLS II	WCMLS II	WCMLS II	WCMLS II	WCMLS II
12	CCLS I	WCMLS I	WCMLS I	WCMLS I	WCMLS I	WCMLS I	WCMLS I	WCMLS I	WCMLS I

CHAPTER 5

Conclusion

In this work, we propose a set of metrics to analyze the carbon footprint and emissions associated with a standard cell (here, Level Shifter), considering both manufacturing and operational impacts over its expected lifespan. These metrics were validated using a set of conventional and advanced Level Shifter architectures designed to shift voltage levels from a subthreshold voltage of 0.3V to a nominal voltage of 1.2V. Beyond metric formulation, the Level Shifters were implemented in STMicroelectronics Low Standby Power 65nm technology, followed by post-layout analysis. The sustainability evaluation was performed for multiple application domains like IoT, Automotive, High-Performance Computing, and Portable Electronics. Along with this, a unique double-row standard cell technique was implemented for layout design, incorporating the upper metal layer (M2) to optimize area utilization. The impact of this approach on sustainability was also analyzed in terms of congestion, fabrication area, lithography process complexity, and parasitic effects.

It was observed that the sustainability ranking of Level Shifters varied depending on whether the assessment focused on Embodied Footprint (eCFP), Operational footprint (oCFP), or the Total footprint. When considering only eCFP, designs with larger area, more fabrication masks, and higher metal usage for layout design tended to exhibit a larger footprint. While considering only the oCFP, designs with higher leakage or dynamic power consumption, depending on the usage application, tended to exhibit a larger footprint. However, in the holistic Total Footprint assessment, design sustainability rankings varied based on the combined influence of Embodied and Operational Footprints.

Thus, by utilizing these designer-centric sustainability metrics and incorporating them into the physical design EDA tools, industries can evaluate the sustainability of Level Shifters early in the design flow stage. This enables the selection of the most sustainable Level Shifter from the available design options for integration into the usage-based multi-voltage domain SoC or product. This cell-level sustainability evaluation approach can allow us to design an overall environment-friendly product.

Looking ahead, this work lays the groundwork for a range of potential extensions and broader applicability. One key direction is to incorporate *Design Effort* and *Reusability* into the Embodied footprint metric, as it provides a more comprehensive view of the complexity, compatibility, and potential yield when implementing newer or advanced designs compared to existing simpler alternatives. Additionally, it would be worthwhile to integrate these metrics directly into open-source EDA tools and validate their effectiveness using real industrial datasets.

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List of papers based on Thesis

1. A. Grover et al., "Sustainability Framework for Computing Element Design," 2025 International Conference on ICT for Sustainability (ICT4S), Dublin, Ireland, June 2025.

2. A. Jain and A. Grover, "Sustainability Benchmark of Subthreshold Level Shifters for IoT Applications," 2025 IEEE Region 10 Symposium (TENSYMP), New Zealand, July 2025.

3. A. Grover et al., "Framework to Estimate and Benchmark Sustainability of Circuit Design," 2025 IEEE Region 10 Symposium (TENSYMP), New Zealand, July 2025.