# Impact of "Operational Transconductance Amplifiers" Design choices on Sustainability


**by**

**Sameer Ahmed**
MT23185

**Under the Supervision of Dr. Anuj Grover**

Department of Electronics and Communication Engineering
Indraprastha Institute of Information Technology Delhi
New Delhi - 110020


**May 14, 2025**

May 2025

# Impact of "Operational Transconductance Amplifiers" Design choices on Sustainability

*A Thesis Report*

*submitted by*

**Sameer Ahmed**

*in partial fulfilment of the requirements*
*for the award of the degree of*

**Master of Technology**

*to*

Department of Electronics and Communication Engineering
Indraprastha Institute of Information Technology Delhi
New Delhi - 110020

**May 14, 2025**

# Certificate

This is to certify that the thesis titled "**Impact of "Operational Transconductance Amplifiers" Design choices on Sustainability**" being submitted by **Sameer Ahmed** to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of **Master of Technology**, is an original research work carried out under the guidance of Dr. Anuj Grover. In my opinion, the thesis meets the required standards as prescribed by the institute's regulations.

**Dr. Anuj Grover**
Associate Professor
Department of Electronics and Communication Engineering
Indraprastha Institute of Information Technology Delhi
New Delhi 110020

Date: May 14, 2025

# Acknowledgements

I am deeply grateful to my supervisor, Dr. Anuj Grover, for his invaluable guidance, insightful feedback, and consistent support throughout this research journey. My thanks also extend to the faculty and colleagues at IIIT Delhi for their constructive inputs, and to my family and friends for their unwavering encouragement. This research, which explores sustainable design practices in analog circuit implementation, would not have been possible without such collaborative spirit.

# Abstract

This thesis investigates a comprehensive sustainability assessment framework for operational transconductance amplifiers (OTAs) by extending the traditional power, performance, and area (PPA) metrics to include environmental impact considerations in the form of embodied and operational footprints. Three OTA architectures—Folded Cascode OTA (FC-OTA), Local Positive Feedback based FC-OTA (LPFB FC-OTA), and Input Differential Pair for Bulk-Driven OTA (IDPBD-OTA)—were evaluated using a 180nm process technology in Cadence Virtuoso. The simulation results reveal that despite the IDPBD-OTA possessing a larger physical layout (and hence higher embodied footprint), its extremely low power consumption minimizes its operational footprint, rendering it the most sustainable option overall. The work emphasizes the need for an integrated evaluation of circuit performance and sustainability—an approach that could guide energy-efficient design practices in the semiconductor industry.

**Keywords**: Operational Transconductance Amplifier (OTA), Sustainability, Carbon Emission, Embodied Footprint, Operational Footprint.

# Contents

# List of Tables

# List of Figures

# Abbreviations

| | |
|---|---|
| **OTA** | Operational Transconductance Amplifier |
| **FC-OTA** | Folded Cascode OTA |
| **LPFB FC-OTA** | Local Positive Feedback based FC-OTA |
| **IDPBD-OTA** | Input Differential Pair for Bulk-Driven OTA |
| **PM** | Phase Margin |
| **UGB** | Unity Gain Bandwidth |
| **SR** | Slew Rate |
| **CMRR** | Common-Mode Rejection Ratio |
| **FVF** | Flipped Voltage Follower |
| **eCFP** | Embodied Carbon Footprint |
| **oCFP** | Operational Carbon Footprint |

# Notation

| | |
|---|---|
| $A_{\textbf{vol}}$ | Open-loop DC Gain (in dB) |
| $V_{\textbf{in}}$ | Input Voltage |
| $V_{\textbf{out}}$ | Output Voltage |
| $A_d$ | Differential Gain |
| $A_{cm}$ | Common-Mode Gain |
| $V_{DD}$ | Supply Voltage |
| $I_{DD}$ | Supply Current |
| $T_{op}$ | Operational Lifetime of the Circuit |

# CHAPTER 1

# Introduction

## 1.1 Context and Motivation

In the integrated circuit (IC) industry, design quality, reliability, and efficiency have traditionally been determined by the well-established metrics of power, performance, and area (PPA). Power consumption not only affects thermal management and battery life but also overall system efficiency, while performance directly correlates with the speed and computational capacity of the IC; area, in turn, is critical for manufacturing costs and integration density. Recently, however, the focus has expanded beyond PPA to embrace sustainability, prompting designers to assess environmental impacts throughout the entire lifecycle—from the extraction of raw materials and semiconductor fabrication to device operation and eventual disposal or recycling[1].

Recent studies have underscored the environmental challenges associated with nanoscale semiconductor manufacturing. Life cycle assessments of embedded non-volatile memory dies, for example, reveal that the fabrication processes for these devices are highly resource-intensive. These assessments detail substantial energy consumption, significant water usage, and high greenhouse gas emissions in semiconductor fabrication, emphasizing the need for more sustainable manufacturing practices and innovative process optimizations. The environmental footprint of these processes now compels the industry to expand its evaluation criteria, considering not only energy efficiency and thermal performance but also the broader sustainability of IC production[2].

Addressing these challenges, industry leaders are proactively reducing carbon emissions and minimizing the environmental burden of semiconductor manufacturing. Organizations like Imec have performed comprehensive, bottom-up lifecycle assessments of logic technology nodes, offering actionable recommendations to lower carbon emissions and progress toward net-zero targets. Beyond fabrication, sustainability also involves improving operational efficiency, extending device longevity, and ensuring responsible end-of-life management. As regulatory pressures increase and consumer demand for environmentally responsible electronics intensifies, the semiconductor sector is tasked with the dual responsibility of driving technological innovation while concurrently mitigating its environmental impact.

## 1.2 Operational Transconductance Amplifiers in Modern Analog Design

At the core of analog and mixed-signal circuits lie operational transconductance amplifiers (OTAs). These devices, which convert differential input voltages into proportional output currents, are indispensable in applications ranging from modulators and filters to precision signal processing systems. Historically, OTA design has centered on PPA-centric optimization methods. Yet, as sustainability challenges gain prominence, it becomes imperative to reexamine these traditional methodologies. This work emphasizes that while OTAs continue to play a pivotal role in system performance, their design must now also account for environmental impacts such as power efficiency and footprint, thereby paving the way for greener analog electronics[3].

## 1.3 Bridging Traditional Performance with Sustainability

Traditional figures of merit (FoMs) in analog design—such as open-loop DC gain, phase margin, unity gain bandwidth, slew rate, and common-mode rejection ratio (CMRR)—have been the benchmarks for decades. These metrics capture the electrical performance and stability of OTA architectures under various operating conditions. However, with the growing urgency of environmental concerns, it is essential to expand this evaluation framework. In addition to the established FoMs, modern design assessments must incorporate parameters like power consumption, layout area, and the associated carbon footprint. Such an integrated evaluation not only ensures that devices perform optimally but also aligns their production and operation with sustainable engineering practices.

## 1.4 Overview of Key Figures of Merit (FoM)

This thesis evaluates OTA performance using a comprehensive set of metrics that address both conventional and sustainability concerns:

1. **Open-Loop DC Gain:** Indicates the intrinsic amplification capability of the OTA in the absence of feedback, serving as a primary performance indicator.
2. **Phase Margin:** Reflects the stability of the amplifier by measuring the angular difference at the unity gain frequency, crucial for avoiding overshoots and ensuring signal fidelity.
3. **Unity Gain Bandwidth (UGB):** Specifies the operational frequency range where the OTA maintains unity gain, directly impacting its suitability for high-speed applications.

4. **Slew Rate:** Denotes the maximum rate at which the OTA can respond to rapid input changes, ensuring accurate tracking of fast transient signals.
5. **Common-Mode Rejection Ratio (CMRR):** Evaluates the OTA's ability to suppress common-mode noise, essential for preserving signal integrity in noisy environments.
6. **Power Consumption and Layout Area:** Quantify both the operational efficiency and the environmental footprint of the design, reflecting the growing need for sustainable circuit solutions.

A detailed discussion of these metrics, including derivations and practical implications for both performance and sustainability, is presented in subsequent chapters.

## 1.5 Thesis Organization

This thesis is organized into five chapters to provide both an in-depth technical analysis and a broad perspective on sustainable analog design:

- **Chapter 1: Introduction**—Provides the context, motivation, and an overview of the key performance and sustainability metrics that drive the research.
- **Chapter 2: Literature Review and Theoretical Background**—Covers the theoretical foundations including detailed descriptions of OTA architectures and a review of traditional figures of merit alongside emerging sustainability considerations.
- **Chapter 3: Simulation and Comparative Evaluation**—Details the simulation setups (both open-loop and closed-loop), reports performance data for each OTA architecture, and analyzes layout considerations.
- **Chapter 4: Sustainability Evaluation Framework**—Introduces an integrated framework (PPAS) that quantifies environmental impact by combining embodied and operational footprints, along with a detailed discussion of sustainability metrics.
- **Chapter 5: Conclusions and Future Work**—Summarizes the key findings, discusses the trade-offs between performance and sustainability, and outlines future research directions.

# CHAPTER 2

# Literature Review and Theoretical Background

## 2.1 Figures of Merit

The performance evaluation of operational transconductance amplifiers (OTAs) is critical for optimizing their use in both analog and mixed-signal applications. In this work, several key figures of merit (FoMs) are employed to objectively compare the performance of different OTA architectures under identical operating conditions[7]. These metrics not only quantify the electrical characteristics of the amplifiers but also offer a pathway for assessing their environmental footprint. The principal FoMs discussed herein are:

### 1. Open-Loop DC Gain

The open-loop DC gain ($A_{vol}$) quantifies the intrinsic amplification capability of the OTA in the absence of a feedback loop. It is defined as:

$$A_{vol} = 20\log_{10}\left(\frac{V_{out}}{V_{in}}\right) \quad \text{(dB)} \tag{2.1}$$

This parameter is a primary indicator of device performance and is among the first metrics evaluated during OTA characterization.

### 2. Phase Margin (PM)

Phase margin indicates the stability of the amplifier by measuring the angular difference between the loop gain phase and the critical $-180^\circ$ at the unity gain frequency. It is expressed as:

$$\text{Phase Margin} = 180^\circ + \angle\left[LG(j\omega)H(j\omega)\right]_{|GH|=1} \tag{2.2}$$

A higher phase margin generally translates to improved stability, ensuring minimal overshoot and ringing in the output signal.

## 3. Unity Gain Bandwidth (UGB)

The unity gain bandwidth is defined as the frequency at which the amplifier's gain falls to unity (0 dB). It sets the effective frequency range for reliable operation and is particularly crucial for applications requiring high-speed performance.

$$\text{UGB} = f\Big|A(f) = 1\Big| \tag{2.3}$$

## 4. Slew Rate (SR)

The slew rate measures the maximum rate at which the OTA can change its output voltage in response to a rapid input transition. Mathematically, it is represented by:

$$\text{Slew Rate} = \max\left(\frac{dV_{out}}{dt}\right) \tag{2.4}$$

A high slew rate is essential for accurately tracking fast transient signals without distortion.

## 5. Common-Mode Rejection Ratio (CMRR)

CMRR evaluates the OTA's ability to reject common-mode signals in favor of differential signals, which is vital for maintaining signal integrity in noisy environments. It is defined as:

$$\text{CMRR} = 20\log_{10}\left(\frac{A_d}{A_{cm}}\right) \quad \text{(dB)} \tag{2.5}$$

where $A_d$ is the differential gain and $A_{cm}$ is the common-mode gain.

## 6. Power Consumption and Area Efficiency

For a comprehensive evaluation, power consumption is considered under practical (closed-loop) operating conditions:

$$\text{Total Power} = V_{DD} \times I_{DD} \tag{2.6}$$

## 2.2 OTA Architectures

Operational transconductance amplifiers are the cornerstone of analog circuit design. Their diverse architectures have evolved to meet specific performance requirements while increasingly being evaluated for their sustainability implications. This section presents three key OTA architectures examined in this study.

### 2.2.1 Folded Cascode OTA (FC-OTA)

The Folded Cascode OTA (FC-OTA) is a widely adopted architecture that strikes a balance between high intrinsic gain and moderate power consumption. As described in the literature, the FC-OTA employs a differential input pair (transistors M1 and M2) followed by common-gate amplifier stages (transistors M7 and M8), and a self-biased cascode current mirror (transistors M9 through M12). This design ensures high output impedance without the adverse effects of an additional frequency pole, thereby reducing the need for compensation capacitance. Careful biasing (via voltages $V_{b1}$ and $V_{b2}$) is critical for maintaining all transistors in saturation and achieving optimal performance[4].

Figure 2.1 shows the complete schematic of the Folded Cascode OTA. Notice the differential pair forming the input stage and the cascoded structure which is key to achieving high DC gain.

### 2.2.2 Local Positive Feedback-based FC-OTA (LPFB FC-OTA)

Building on the FC-OTA, the Local Positive Feedback-based FC-OTA (LPFB FC-OTA) incorporates a feedback mechanism to boost the effective transconductance of the input stage. In this technique, part of the current generated by the input differential pair is recycled through an auxiliary transconductance circuit, effectively introducing a negative resistance element at the input. This modification increases the output resistance and, consequently, the overall DC gain of the amplifier[5].

Figure 2.2 illustrates the complete schematic for the LPFB FC-OTA. The added feedback loop is the key differentiator from the traditional FC-OTA, leading to enhanced gain performance.

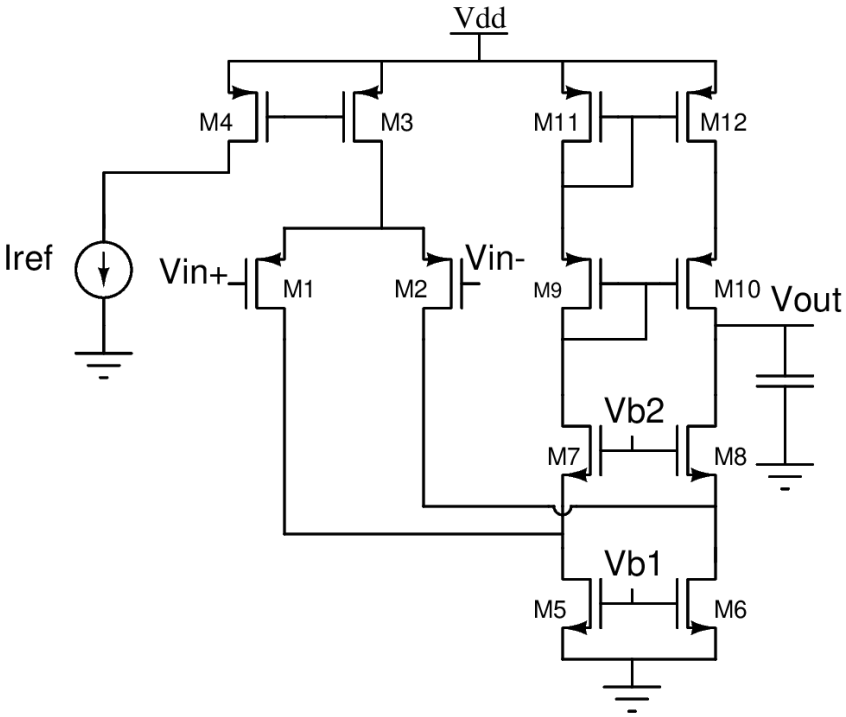


Figure 2.1: Schematic of Folded Cascode OTA (FC-OTA)

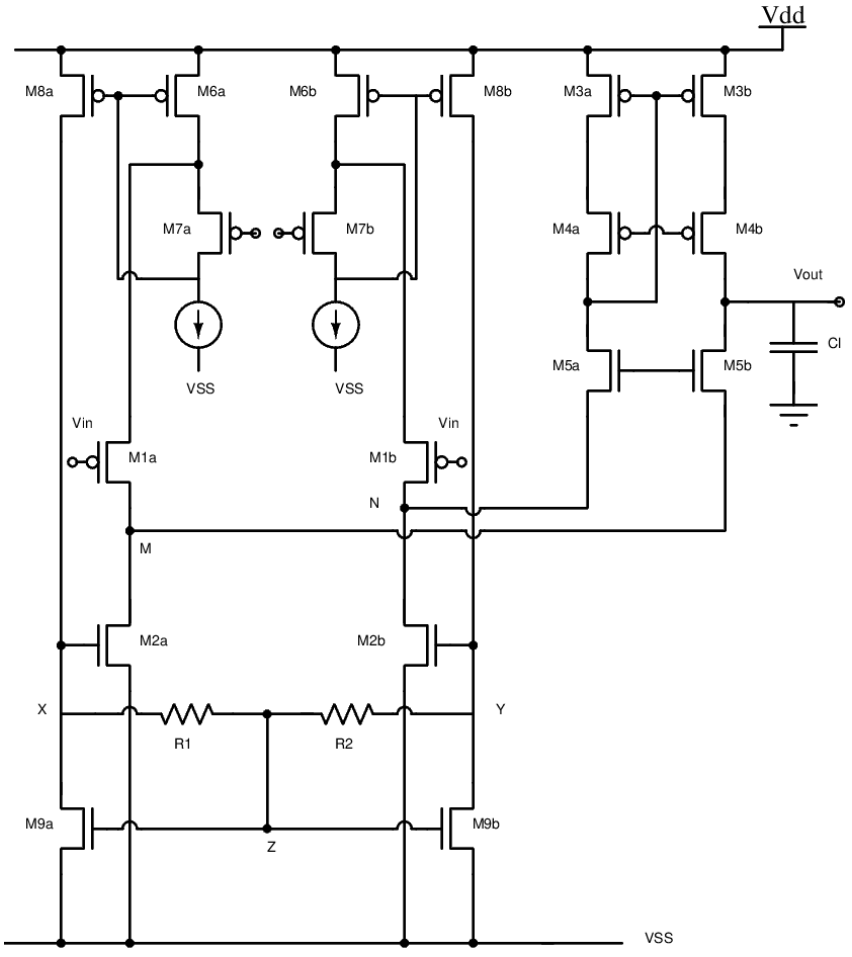


Figure 2.2: Schematic of LPFB FC-OTA

### 2.2.3 Input Differential Pair for Bulk-Driven OTA (IDPBD-OTA)

This work presents a low voltage, high transconductance input differential pair designed for bulk-driven amplifiers. The proposed architecture incorporates two bulk-driven flipped voltage follower (FVF) cells as nonlinear tail current sources to enhance slewing behavior. This approach effectively doubles the transconductance compared to conventional designs. Furthermore, the enhanced topology is integrated with a standard bulk-driven input differential pair through cross-coupled connections, leading to a substantial increase in transconductance. These circuit-level modifications help to reduce the overall power consumption of the amplifier making it fit for the ultralow power (ULP) analog circuit[6].

Figure 2.3 displays the schematic of the IDPBD-OTA. The design highlights the cross-coupled bulk-driven differential pair complemented by auxiliary FVF-based tail current sources, which are critical for enhancing performance under low-power conditions.

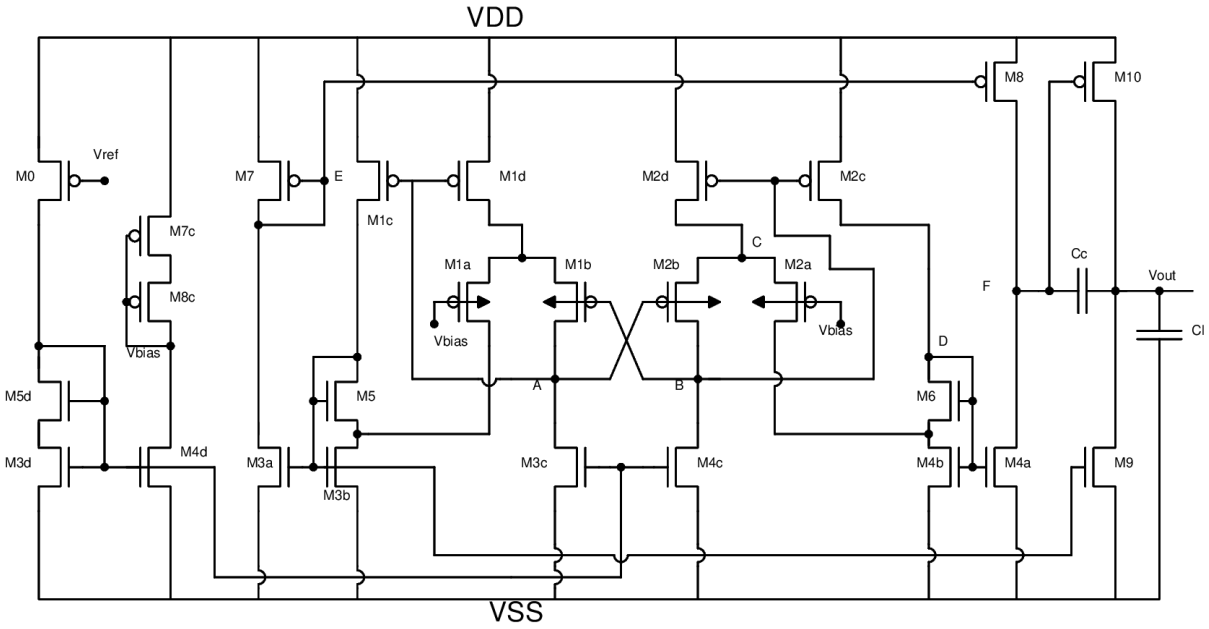


Figure 2.3: Schematic of IDPBD-OTA

## 2.3 Sustainability in VLSI Design

With the rapid expansion of electronics in modern systems, concerns over the environmental impact of semiconductor design and manufacturing have grown markedly. The shift from mechanical to electronic solutions has led to heightened energy demands during operation, while the manufacturing processes remain exceptionally resource-intensive. For example, TSMC's electricity usage in 2023 reportedly rivaled the peak consumption of a large nation such as India. In response, industry leaders like Intel, Apple, and STMicroelectronics have set carbon neutrality targets in their sustainability reports [2]. However, as manufacturers such as TSMC have pointed out, achieving these goals is challenging due to the increasing energy intensity of advanced technology nodes.

Numerous initiatives have aimed to curb emissions during the manufacturing process through life cycle analysis (LCA), material toxicity evaluations, and multi-criteria decision frameworks. Despite these efforts, most approaches have concentrated on system- and product-level assessments. Metrics such as the Toxic Potential Indicator and eco-reliability have been proposed to guide sustainable design decisions, and recent studies have even introduced carbon footprint estimation tools for chiplet-based architectures [8]. Nonetheless, there remains a significant gap in applying structured sustainability metrics at the circuit design level, where decisions about architecture, logic style, and resilience are fundamentally made.

Traditionally, the semiconductor industry has prioritized the area, power, and performance (PPA) metrics, often overshadowing environmental considerations. This persistent focus on PPA has left a critical void—a need for new figures of merit that directly incorporate both reliability and environmental impact from the earliest stages of VLSI design. Addressing this shortfall is essential for fostering innovations that not only meet performance standards but also align with the growing imperative for sustainable design practices.

# CHAPTER 3

# Simulation and Comparative Evaluation

## 3.1 Simulation Setup

To ensure a comprehensive assessment of the amplifier architectures, the simulation setup considers both open-loop and closed-loop configurations for evaluating key Figures of Merit (FoMs). These configurations allow for a precise analysis of performance characteristics under practical operating conditions[7].

### 3.1.1 Open-Loop Simulation

The following FoMs were evaluated in an open-loop setup:

- **DC Gain ($A_{vol}$)**: The amplification factor in the absence of feedback, determined using Equation (2.1).
- **Phase Margin**: Stability metric evaluated from the frequency response of the amplifier loop gain, calculated using Equation (2.2).
- **Unity Gain Bandwidth (UGB)**: The frequency at which the gain reduces to unity, indicative of bandwidth limitations.

All open-loop simulations are performed using Cadence Virtuoso at a constant supply voltage of $1.8\,\mathrm{V}$ and a standard capacitive load of $15\,\mathrm{pF}$ under all process corner at $27\,^{\circ}\mathrm{C}$. Figure 3.1 illustrates the open-loop experimental setup.

### 3.1.2 Closed-Loop Simulation

The closed-loop configuration was used to evaluate FoMs that require feedback for accurate characterization:

- **Slew Rate**: Maximum rate of change of the output voltage, obtained from transient response analysis.
- **Common-Mode Rejection Ratio (CMRR)**: Quantifies the amplifier's ability to reject common-mode signals compared to differential signals, computed via Equation (2.5).

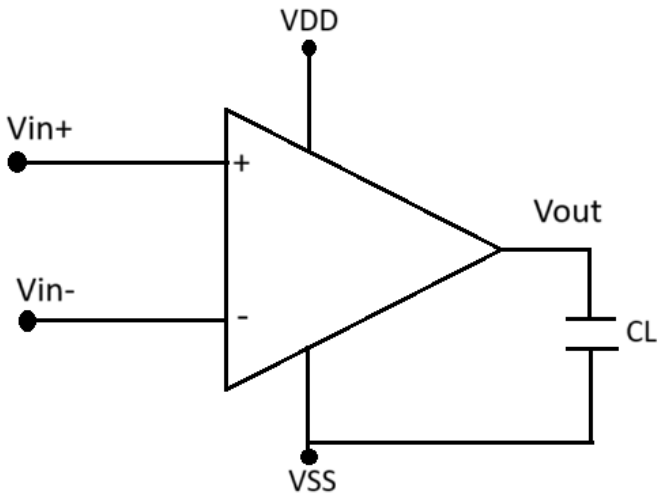


Figure 3.1: Open-Loop Simulation Setup.

- **Power Consumption**: Evaluated in the closed-loop setup to represent real-world operational behavior, using Equation (2.6).

The closed-loop experiments also maintain a load of $15\,\mathrm{pF}$ and a supply voltage of $1.8\,\mathrm{V}$, ensuring consistency with the open-loop conditions. Figure 3.2 shows the experimental setup for the closed-loop measurements.

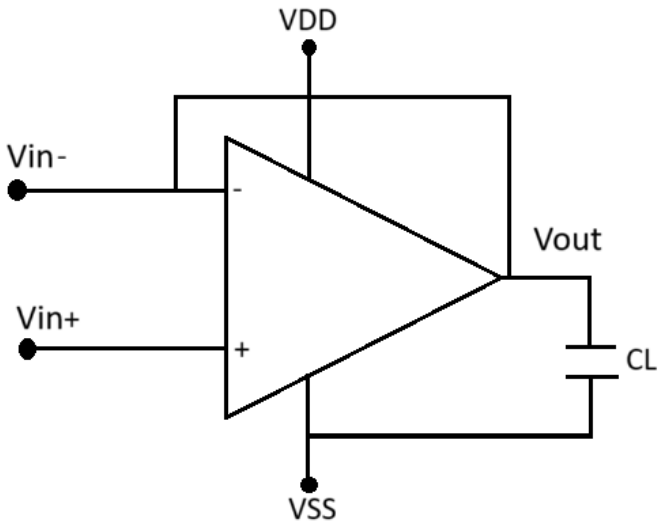


Figure 3.2: Closed-Loop Simulation Setup.

### 3.1.3 Performance Data and Analysis

The following performance data have been collected for three OTA architectures—FC-OTA, LPFB FC-OTA, and IDPBD-OTA—across five process corners (NN, SS, SF, FS, and FF).

**Table 3.1**
Performance Data for FC-OTA (Process Corners: NN, SS, SF, FS, FF)

| **Parameter** | **NN** | **SS** | **SF** | **FS** | **FF** |
|---|---|---|---|---|---|
| DC Gain (dB) | 84.78 | 90.76 | 92.25 | 80.45 | 82.49 |
| Phase Margin [°] | 79.58 | 74.30 | 74.94 | 78.30 | 82.28 |
| UGW (MHz) | 4.12 | 3.75 | 4.04 | 3.81 | 4.35 |
| Slew Rate (V/µs) | 1.129 | 0.710 | 0.945 | 0.992 | 1.794 |
| CMRR (dB) | 107.33 | 93.96 | 116.65 | 88.21 | 115.45 |
| Power (mW) | 0.122 | 0.101 | 0.103 | 0.112 | 0.145 |

**Table 3.2**
Performance Data for LPFB FC-OTA (Process Corners: NN, SS, SF, FS, FF)

| **Parameter** | **NN** | **SS** | **SF** | **FS** | **FF** |
|---|---|---|---|---|---|
| DC Gain (dB) | 85.89 | 82.03 | 79.29 | 82.15 | 80.37 |
| Phase Margin [°] | 71.96 | 72.49 | 72.70 | 71.18 | 71.37 |
| UGW (MHz) | 1.45 | 1.423 | 1.422 | 1.566 | 1.535 |
| Slew Rate (V/µs) | 0.318 | 0.305 | 0.321 | 0.308 | 0.323 |
| CMRR (dB) | 124.22 | 109.08 | 125.41 | 108.99 | 126.89 |
| Power (mW) | 0.6415 | 0.6449 | 0.6373 | 0.6531 | 0.6458 |

#### 3.1.3.1 FC-OTA Performance

Table 3.1 summarizes the Figures of Merit (FoMs) for the Folded Cascode OTA (FC-OTA). In this topology, the DC gain varies from 80.45 dB to 92.25 dB, with phase margins ranging from 74.30°to 82.28°. The unity gain bandwidth (UGW) is in MHz, while the slew rate spans from 0.710 to 1.794 V/$\mu$s. Additionally, the CMRR varies between 88.21 dB and 116.65 dB, and the power consumption remains in the sub-milliwatt range.

#### 3.1.3.2 LPFB FC-OTA Performance

Table 3.2 presents the performance data for the Local Positive Feedback based FC-OTA (LPFB FC-OTA). Its DC gain ranges from 79.29 dB to 85.89 dB and the phase margin is maintained around 71° to 72.70°. The unity gain bandwidth is significantly lower (approximately 1.42–1.57 MHz). The slew rate remains near 0.318 V/$\mu$s, while the CMRR is recorded between 108.99 dB and 126.89 dB. The power consumption is on the order of 0.64 mW.

**Table 3.3**
Performance Data for IDPBD-OTA (Process Corners: NN, SS, SF, FS, FF)

| **Parameter** | **NN** | **SS** | **SF** | **FS** | **FF** |
|---|---|---|---|---|---|
| DC Gain (dB) | 59.32 | 62.20 | 57.89 | 56.61 | 56.63 |
| Phase Margin [°] | 79.83 | 70.08 | 81.10 | 79.01 | 76.88 |
| UGW (kHz) | 71.62 | 92.46 | 113.59 | 89.94 | 144.83 |
| Slew Rate (V/ms) | 16.64 | 16.58 | 18.93 | 14.67 | 22.94 |
| CMRR (dB) | 97.87 | 108.45 | 98.68 | 110.26 | 99.40 |
| Power (µW) | 3.312 | 2.813 | 5.776 | 4.29 | 6.794 |

#### 3.1.3.3 IDPBD-OTA Performance

Performance data for the Input Differential Pair for Bulk-Driven OTA (IDPBD-OTA) are provided in Table 3.3. This architecture exhibits a lower DC gain (56.61 dB to 62.20 dB) and a variable phase margin. Notably, the unity gain bandwidth is expressed in kHz (ranging from 71.62 kHz to 144.83 kHz), and the slew rate, given in V/ms, shows significant variation. The CMRR is moderate compared to the other topologies, while the power consumption is extremely low (measured in microwatts), rendering this design particularly appealing for energy-constrained applications.

### 3.1.4 Discussion

The dual-configuration simulation approach provides valuable insights into the trade-offs between performance and sustainability:

- **FC-OTA:** This architecture delivers high DC gain with moderate power consumption. However, its performance metrics (gain, phase margin, slew rate) are noticeably sensitive to process variations.
- **LPFB FC-OTA:** The incorporation of local positive feedback results in stable phase margins and enhanced CMRR across different process corners. Although its unity gain bandwidth is lower compared to FC-OTA, the trade-off is acceptable given the improved feedback performance, despite slightly higher power consumption.
- **IDPBD-OTA:** With the lowest power consumption—measured in microwatts—this OTA is especially attractive for low-power and sustainable designs. The lower DC gain and higher variability in slew rate and UGW suggest that this design is optimized more for energy efficiency than for peak performance.

## 3.2 Layout Design and Matching

The analog layouts for the OTA designs have been meticulously engineered to ensure optimal performance and high matching accuracy. Critical devices have been matched using common centroid and interdigitation matching techniques, and guard rings have been strategically placed around sensitive circuitry to reduce substrate noise and process variation effects. These measures are essential for minimizing mismatch and enhancing the overall reliability of the circuits.

### 3.2.1 Layout Area and Track Utilization

The overall layout area and routing track usage are key indicators of design compactness and resource efficiency in analog layouts. Table 3.4 summarizes the layout area and track utilization for the three OTA designs. Specifically, the IDPBD-OTA occupies an area of $8297.64\,\mu\mathrm{m}^2$ with 43 tracks used out of 117 available, the LPFB FC-OTA occupies $2914.56\,\mu\mathrm{m}^2$ using 48 out of 88 tracks, and the FC-OTA uses $3674.16\,\mu\mathrm{m}^2$ with 33 out of 126 tracks.

**Table 3.4**
Layout Area and Track Utilization

| **OTA Design** | **Area ($\mu$m$^2$)** | **Track Usage (Used / Total)** |
|---|---|---|
| IDPBD-OTA | 8297.64 | 43 / 117 |
| LPFB FC-OTA | 2914.56 | 48 / 88 |
| FC-OTA | 3674.16 | 33 / 126 |

### 3.2.2 Analog Layout Figures

Figures 3.6, 3.5, and 3.3 illustrate the complete analog layouts for the IDPBD-OTA, LPFB FC-OTA, and FC-OTA designs respectively. These figures highlight the careful placement of matching structures and the guard rings in regions where they are required.

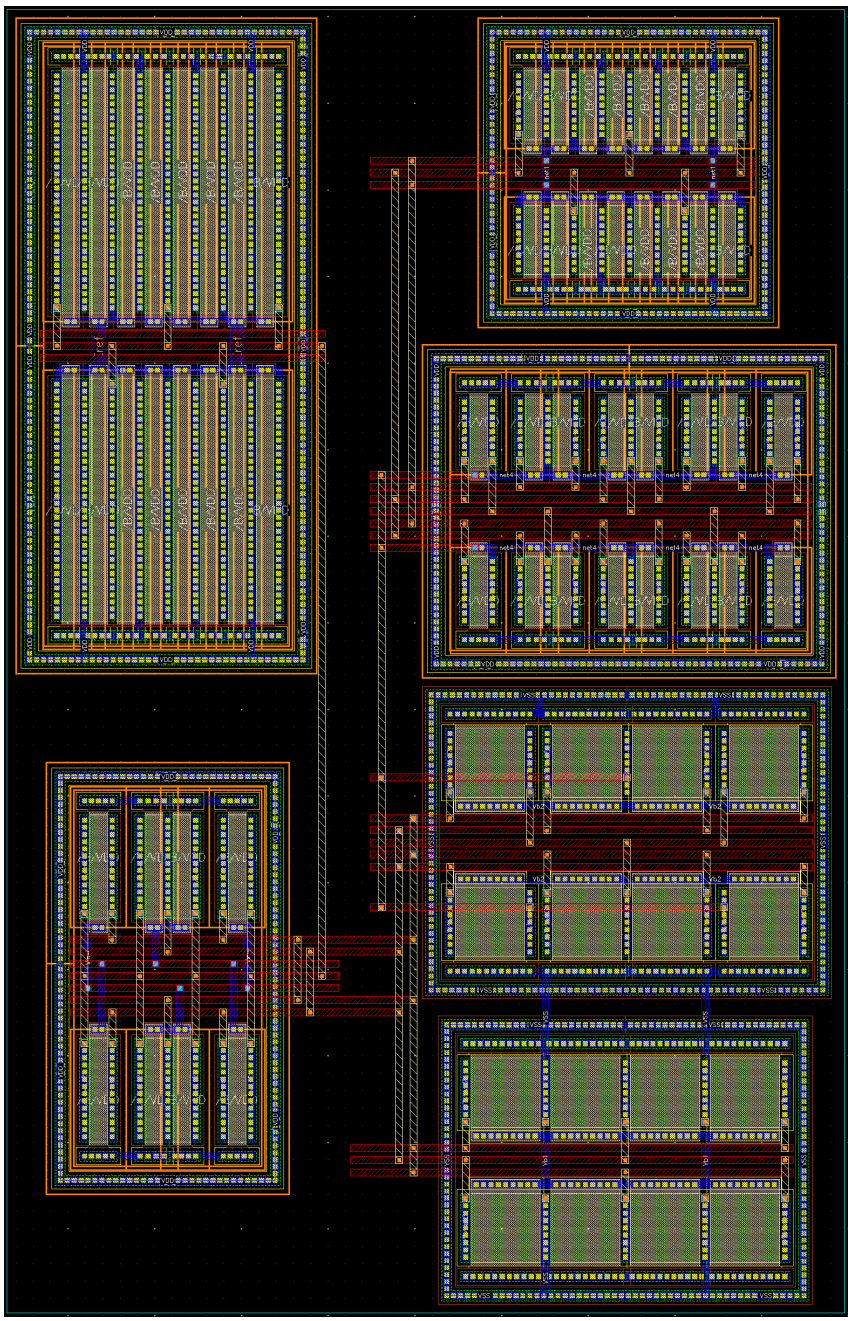

Figure 3.3: Complete layout of the FC-OTA design.

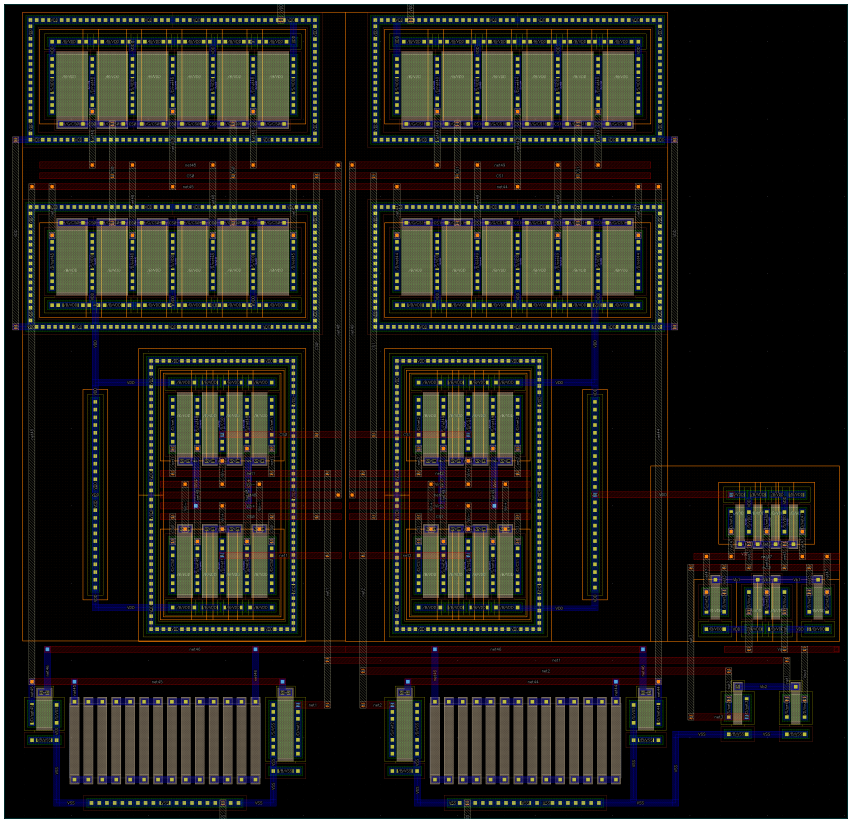

Figure 3.4: Complete layout of the LPFB FC-OTA design with poly resistor.

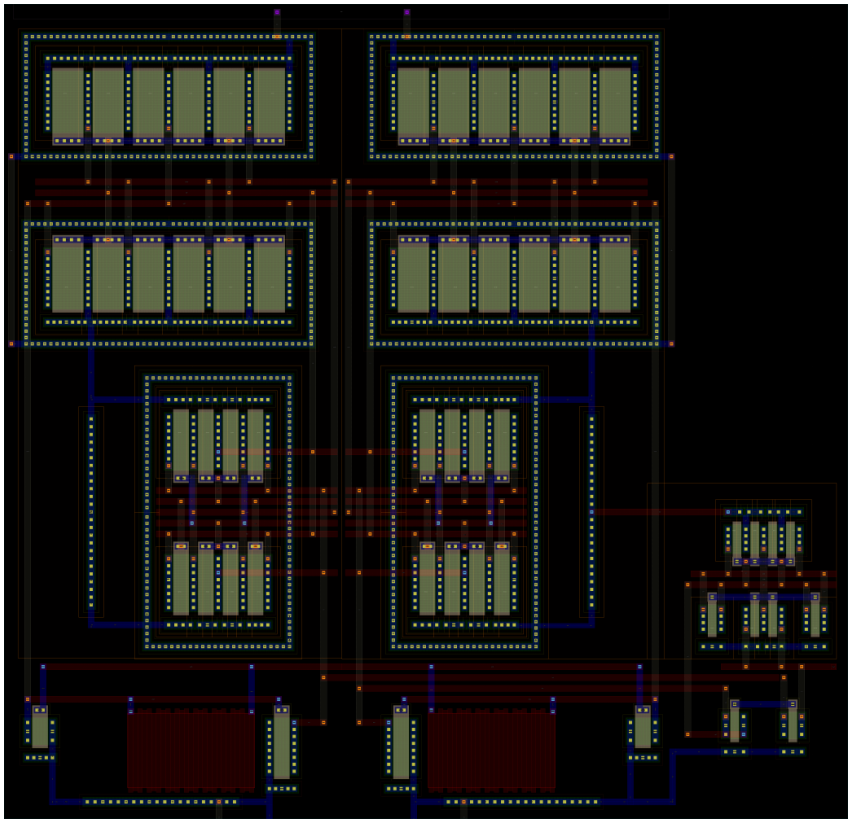

Figure 3.5: Complete layout of the LPFB FC-OTA design with metal resistor.

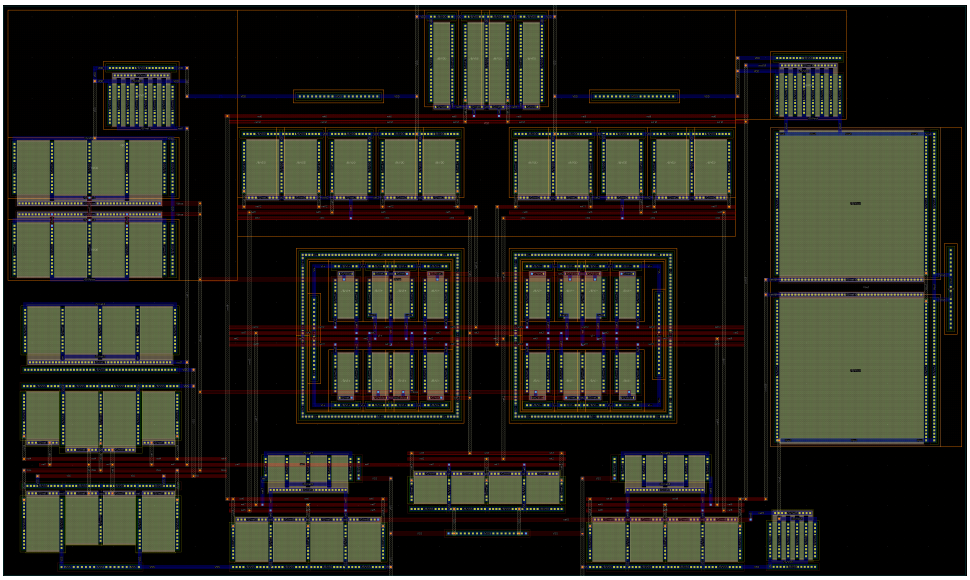

Figure 3.6: Complete layout of the IDPBD-OTA design.

# CHAPTER 4

# Sustainability Evaluation Framework

In our work, we introduce a two-part sustainability metric that quantifies the environmental impact incurred during both the fabrication and the operational phases of an integrated circuit. This metric is integrated into the PPAS framework to guide designers toward eco-friendly design choices starting from the early stages of the development cycle.

## 4.1 Embodied Carbon Footprint Metric (eCFP)

The embodied carbon footprint (eCFP) represents the total carbon emissions produced throughout the manufacturing process of integrated circuits. It encompasses all fabrication steps—including photolithography, doping, etching, and thin-film deposition—which are highly energy-intensive and significantly impact the device's environmental profile even before it is deployed. Thus, the eCFP serves as a key sustainability metric that designers can target for optimization during the IC development phase. In this work, the eCFP is defined as follows:

$$\text{eCFP} = k \times \text{Area} \times \text{Mask\_factor} \times \text{Porosity\_factor} \tag{4.1}$$

In Equation (4.1):

- $k$ represents the base energy per unit area (expressed in energy units per $\mu\text{m}^2$) as determined from a standard wafer process.
- **Area** refers to the physical layout size of the design in $\mu\text{m}^2$. A larger area directly increases the eCFP, since more material and processing energy are required.

To capture additional overhead introduced by design and process complexities, two factors are incorporated:

### Mask Overhead (Mask_factor)

The Mask Overhead accounts for the extra energy cost induced by using additional photomasks beyond a reference baseline. Additional masks may be needed for specialized components such as high-precision capacitors like mimcap or transistors with varying threshold voltages used for

comparator biasing or logic control. Moreover, when designs incorporate extra metal layers or analog-specific features, the total number of required masks increases accordingly, which in turn elevates the overall energy footprint. It is formulated as:

$$\text{Mask\_factor} = \Big( (\text{Total Masks} - \text{Standard Masks}) \times \text{Mask Factor} \Big) + 1, \tag{4.2}$$

where:

- **Total Masks** is the total number of lithographic masks used in the fabrication of the design.
- **Standard Masks** is the baseline number of masks required for a conventional process.
- **Mask Factor** is a constant (set to 0.045), indicating that each extra mask increases the energy consumption by 4.5%.

## Porosity Factor (Porosity_factor)

The porosity factor is an important metric that quantifies the efficiency of routing resource utilization within an integrated circuit (IC) layout. It reflects how much of the available routing area (e.g., metal tracks) remains unobstructed by densely packed device structures and other layout elements. A higher porosity factor indicates that a larger fraction of the routing tracks is free for signal interconnects, which can lead to lower congestion and improved design flexibility.

Efficient layouts aim for high porosity since this not only facilitates easier routing and shorter interconnect paths but also minimizes the need for additional metal layers—thereby reducing the embodied energy cost associated with extra processing steps during fabrication. In contrast, a low porosity factor signifies that many tracks are blocked by cell placement or ancillary structures. This increased congestion necessitates denser routing, may require more complex design techniques or extra metal layers, and ultimately contributes to a higher environmental cost.

The porosity factor, denoted as $P_f$, can be mathematically defined:

$$P_f = 1 - \frac{\text{Number of Blocked Tracks}}{\text{Total Number of Routing Tracks}} \tag{4.3}$$

where a lower value of $P_f$ implies that a significant portion of the available routes is blocked, leading to increased routing challenges and a potential increase in the embodied carbon footprint due to additional routing overhead during fabrication.

By integrating the porosity factor into the sustainability evaluation framework, designers can make more informed trade-offs between achieving compact layouts and maintaining suf-

ficient routing resources to lower the overall environmental impact of the chip manufacturing process.

By evaluating different designs using the eCFP metric in Equation (4.1) along with Equations (4.2) and (4.3), designers can directly compare the embodied environmental impacts of various fabrication strategies. Lower eCFP values indicate a more energy-efficient and, consequently, a more sustainable manufacturing approach[9, 10].

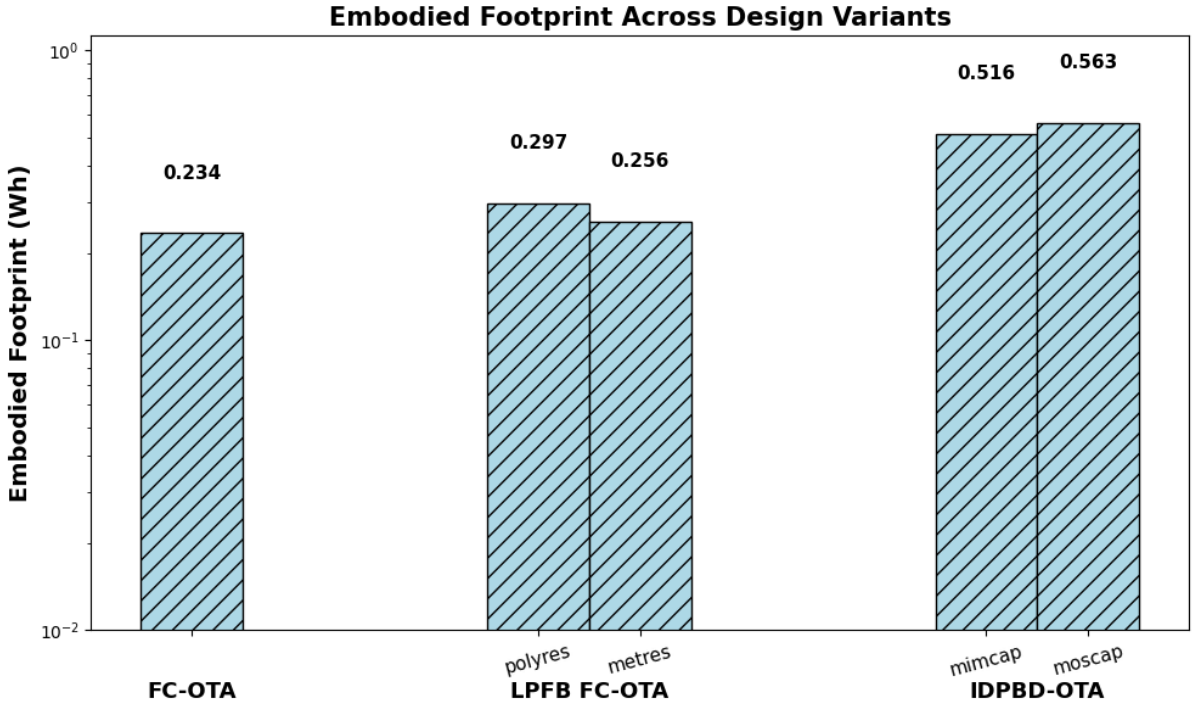


Figure 4.1: Comparative Embodied Footprint for OTA Designs

## 4.2 Operational Footprint Analysis

The operational footprint (oCFP) captures the long-term environmental impact arising from the continuous power consumption during the chip's lifetime. This metric is calculated by:

$$\text{oCFP} = \text{Total Power} \times \text{Operational Lifetime}, \tag{4.4}$$

where:

- Total Power is the power usage measured (in mW) during normal circuit operation.
- Operational Lifetime is the duration over which the circuit is expected to operate[10].

In our study, the LPFB FC-OTA design, despite its compact layout, consumes significantly more power—resulting in a substantially higher operational footprint. In contrast, the IDPBD-

OTA benefits from ultra-low power consumption, thereby minimizing its operational footprint considerably. Figure 4.2 illustrates the operational footprint obtained for each design.

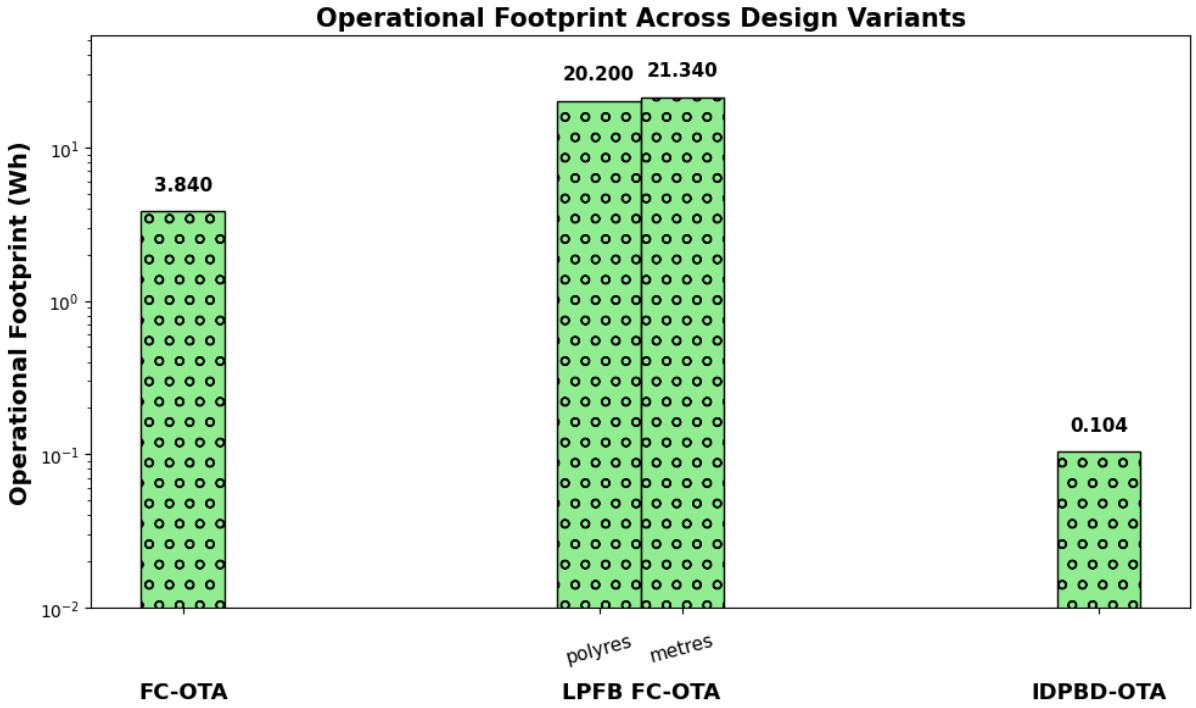


Figure 4.2: Comparative Operational Footprint for OTA Designs

## 4.3 Total Footprint and Sustainability Evaluation

The total footprint provides a comprehensive measure of the environmental impact by combining both the embodied and operational footprints:

$$\text{Total Footprint} = \text{Embodied Footprint} + \text{Operational Footprint}. \tag{4.5}$$

Even though the IDPBD-OTA incurs a higher embodied cost due to its larger layout area, its exceptionally low power consumption results in a minimal operational footprint. When these two factors are combined, the IDPBD-OTA exhibits the lowest overall total footprint, making it the most sustainable option among the three studied architectures. Figure 4.3 shows a comparative graph of the total footprints.

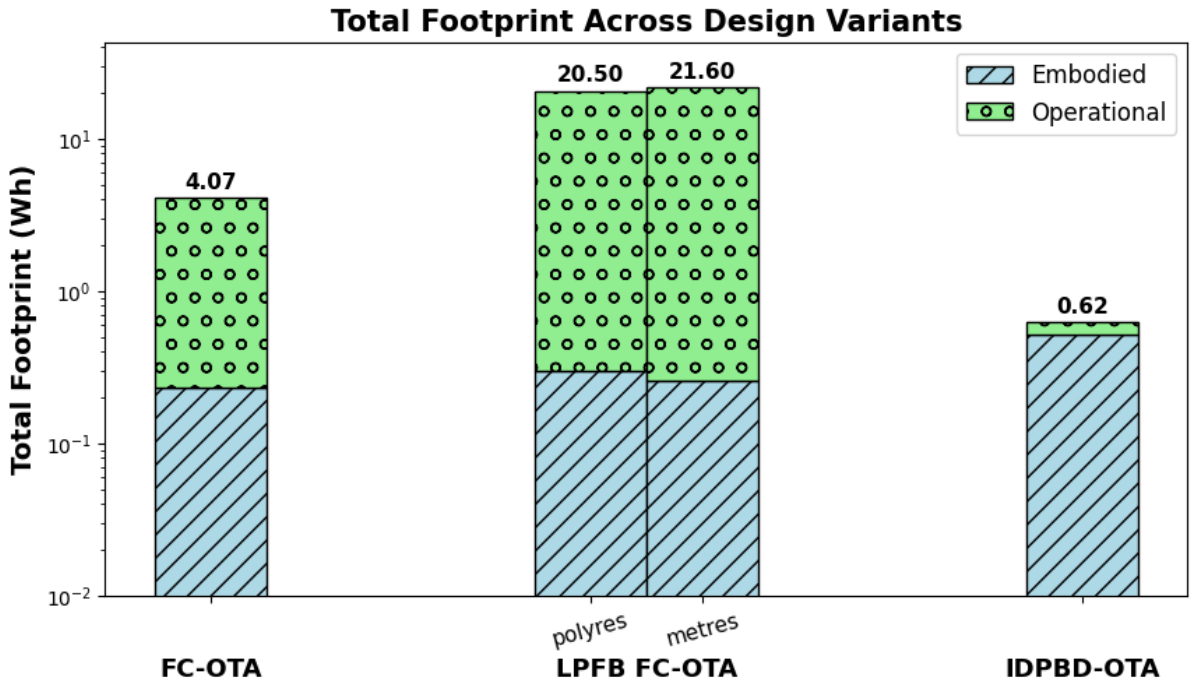


Figure 4.3: Total Footprint Comparison for OTA Designs

## Discussion

The comparative evaluations reveal a pronounced trade-off in analog circuit design when balancing electrical performance with sustainability metrics:

- **FC-OTA:** This architecture benefits from a meticulously optimized layout that minimizes its embodied footprint. However, its moderate power consumption leads to an average operational footprint—limiting the overall sustainability gains.
- **LPFB FC-OTA:** Although this design achieves enhanced gain and superior CMRR, these improvements come at the expense of increased power consumption. Notably, the metal-resistance variant exhibits a relatively low embodied carbon footprint (eCFP). Yet, its higher power draw results in a disproportionately high operational carbon footprint (oCFP) compared to the poly-resistor variant, culminating in a greater overall carbon footprint despite its lower fabrication cost.
- **IDPBD-OTA:** Despite requiring a larger chip area—which translates into higher embodied costs for both the MOSCAP and MIMCAP versions—the IDPBD-OTA leverages an ultra-low power design. Among its configurations, the MOSCAP version shows a higher eCFP than the MIMCAP version due to increased area consumption. Nonetheless, the exceptionally low power consumption drives down the operational footprint (oCFP) so significantly that the overall total carbon footprint of the IDPBD-OTA is the lowest among the evaluated architectures.

# CHAPTER 5

# Conclusions and Future Work

This thesis proposed a sustainability-aware performance assessment framework for operational transconductance amplifiers (OTAs) by extending traditional Power, Performance, and Area (PPA) metrics to include environmental impacts—namely, embodied and operational carbon footprints. Through a detailed comparative study of three OTA architectures—FC-OTA, LPFB FC-OTA, and IDPBD-OTA—using Cadence simulations and layout analysis, the work demonstrated the crucial trade-offs between performance and sustainability.

The key insight from this study is that extremely low power consumption, as seen in the IDPBD-OTA, can significantly reduce operational footprint, making it a more sustainable option overall, even when layout area (and thus embodied cost) is higher. Conversely, architectures with better electrical performance like LPFB FC-OTA may incur a heavier environmental cost due to elevated power consumption.

By integrating both performance and sustainability perspectives, this thesis advocates for a more responsible approach to analog design—one that not only meets functional requirements but also aligns with broader environmental goals.

## Future Work

Several directions can extend the scope and impact of this work:

- **Toolchain Integration:** Incorporating the sustainability framework into existing EDA tools to enable real-time carbon footprint feedback during schematic, simulation, and layout phases.
- **Component Diversity:** Expanding the analysis to include other analog building blocks like comparators, voltage references, and filters to build a generalized sustainable design methodology.
- **Lifecycle Analysis:** Including post-fabrication impacts such as packaging, deployment environment, and end-of-life disposal into the sustainability evaluation.
- **AI for Sustainable Design:** Exploring machine learning models that can predict optimal circuit configurations with minimal environmental impact.

# References


[1] Tsai-Chi Kuo, Chien-Yun Kuo, Liang-Wei Chen, "Assessing environmental impacts of nanoscale semiconductor manufacturing from the life cycle assessment perspective," *Resources, Conservation and Recycling*, vol. 182, 2022, doi:10.1016/j.resconrec.2022.106289.

[2] O. Bubnova, "The road to net-zero emissions in IC manufacturing," *Nat Rev Electr Eng*, vol. 1, pp. 214-215, 2024, doi:10.1038/s44287-024-00023-y.

[3] B. T. Krishna, "Implementation of Linear and Nonlinear circuits using Operational Transconductance Amplifier," *IJVLSID*, vol. 1, no. 2, pp. 1-4, Dec. 2023, doi:10.54105/ijvlsid.B1201.091221.

[4] H. Gupta, G. K. Mishra, N. Z. Rizvi, and S. K. Patnaik, "Design of high PSRR folded cascode operational amplifier for LDO applications," in Proc. *ICEEOT*, Chennai, India, 2016, pp. 4617-4621, doi:10.1109/ICEEOT.2016.7755591.

[5] Y. Wang, Q. Zhang, S. S. Yu, et al., "A Robust Local Positive Feedback Based Performance Enhancement Strategy for Non-Recycling Folded Cascode OTA," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 67, no. 9, pp. 2897-2908, Sept. 2020, doi:10.1109/TCSI.2020.2988310.

[6] M. Akbari, S. M. Hussein, Y. Hashim, and K.-T. Tang, "An Enhanced Input Differential Pair for Low-Voltage Bulk-Driven Amplifiers," *IEEE Trans. VLSI Syst.*, vol. 29, no. 9, pp. 1601-1611, Sept. 2021, doi:10.1109/TVLSI.2021.3084695.

[7] Analog Devices, David Guo, "Op-Amp Basics ."

[8] D. Kline et al., "Sustainable IC design and fabrication," in Proc. *Eighth International Green and Sustainable Computing Conference (IGSC)*, Orlando, FL, USA, 2017, pp. 1-8, doi:10.1109/IGCC.2017.8323572.

[9] A. Grover et al., “Sustainability Framework for Computing Element Design [9],” 2025 International Conference on ICT for Sustainability (ICT4S), Dublin, Ireland, June 2025.

[10] A. Grover et al., “Framework to Estimate and Benchmark Sustainability of Circuit Design ,” 2025 IEEE Region 10 Symposium (TENSYMP), New Zealand, July 2025.