Development of PPAS framework to study the impact of design choices on Sustainability in "SAR ADC" Architectures

by

Ahmad Farhan

MT23209

Under the Supervision of Dr. Anuj Grover

Electronics and Communication Engineering

Indraprastha Institute of Information Technology Delhi

New Delhi - 110020

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Ahmad Farhan

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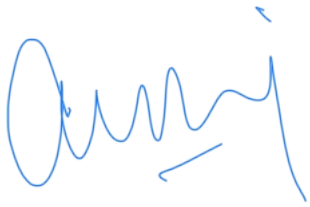
Certificate

This is to certify that the thesis titled "**Development of PPAS framework to study the impact of design choices on Sustainability in "SAR ADC" Architectures**" being submitted by **Ahmad Farhan**, to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of **Master of Technology**, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.



Dr. Anuj Grover
Associate Professor
Department of Electronics and Communication
Indraprastha Institute of Information Technology Delhi
New Delhi 110020

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Abstract

Analog-to-Digital Converters (ADCs) are essential components bridging analog inputs with digital processing systems. Among various architectures, Successive Approximation Register (SAR) ADCs are known for their power and area efficiency but are inherently limited in speed due to their sequential bit-by-bit operation. To overcome this, we implemented and compared two ADC architectures: a conventional SAR ADC and a pipelined SAR ADC, both fabricated in 65nm CMOS technology. The pipelined architecture splits the conversion into two 4-bit stages, allowing it to operate at half the clock frequency while achieving the same throughput as the SAR ADC. Although the SAR ADC occupies about 70% of the area of the pipelined SAR ADC, the pipelined design delivers significantly better performance while maintaining reasonable area and power trade-offs. Additionally, sustainability analysis reveals that the pipelined SAR ADC achieves an approximately 11% lower total carbon footprint compared to the conventional SAR ADC, highlighting the impact of architectural optimization on both performance and environmental metrics. These results underscore that strategic architectural improvements can lead to substantial gains in both system performance and sustainability.

Keywords: SAR ADC, Pipelined SAR ADC, Successive Approximation, High-Speed ADC, Low-Power ADC, CMOS ADC, Sustainability Metric, ADC Architectures

Contents

List of Tables

List of Figures

Abbreviations

IIITD	Indraprastha Institute of Information Technology Delhi
ADC	Analog to Digital Convertor
SAR	Successive Approximation Register
PVT	Process, Voltage and Temperature
CFP	Carbon Footprint
eCFP	Embodied Carbon Footprint
oCFP	Operational Carbon Footprint
Soc	System on Chip
LSTP	Low Standby Power
MIMCAP	Metal Insulator Metal Capacitor
MOSCAP	Metal Oxide Semiconductor Capacitor
DPQ	Dynamic Power Quantity
SPQ	Static Power Quantity
LPQ	Leakage Power Quantity
PDLC	Project Development Lifecycle
PPAS	Power, Performance, Area and Sustainability
MF	Mask Factor
RPR	Reference Power Ratio
PCE	Power Conversion Efficiency
A_ART	Active Area Reference Time
SB_ART	Standby Area Reference Time
R_ART	Retention Area Reference Time
IoT	Internet of Things

Notation

α	Activity Factor
$V_{\mathbf{op}}$	Operational Voltage
$f_{\mathbf{op}}$	Operational Frequency
$Q_{\mathbf{dyn}}$	Dynamic Charge
$I_{\mathbf{bias}}$	Bias Current
$V_{\mathbf{bias}}$	Bias Voltage
$T_{\mathbf{op}}$	Total Operating Time
$V_{\mathbf{t}}$	Threshold Voltage

CHAPTER 1

Introduction

1.1 Motivation

Analog-to-Digital Converters (ADCs) are fundamental building blocks in modern electronic systems, enabling the digitization of real-world analog signals for processing and storage. Among various ADC architectures, the Successive Approximation Register (SAR) ADC is widely used due to its balance between resolution, power efficiency, and compact area [7]. However, traditional SAR ADCs are inherently limited in speed because of their sequential bit-by-bit conversion mechanism, which restricts their application in high-throughput systems. To address these limitations, pipelined SAR ADCs have been developed, combining the energy efficiency of SAR architecture with the enhanced speed benefits of pipelining [1]. Furthermore, as device scaling advances, sustainability and carbon footprint considerations have become increasingly important design factors [11]. Embodied and operational carbon footprints are critical to assess the environmental impact of integrated circuits, especially in large-scale deployments like IoT devices [22]. Therefore, there is a growing need to design ADC architectures that not only achieve better performance but also reduce their environmental footprint. This highlights the motivation to explore pipelined SAR ADC architectures that offer high throughput with efficient energy use, while promoting sustainable circuit design practices [19].

1.2 The Growing Role of Sustainability in VLSI Design

The rapid integration of digital technologies into everyday life—powering everything from mobile devices and wearables to smart infrastructure and cloud services—has reshaped modern society [13, 14]. This transformation is driven largely by breakthroughs in semiconductor technology, enabling smaller, faster, and more efficient electronics.

Across industries like healthcare, communications, and automation, the benefits of advanced integrated circuits are undeniable. Yet, this progress comes with hidden costs [21]. As chip designs evolve from simple planar transistors to complex 3D architectures—such as FinFETs and nanosheet transistors—manufacturing demands have skyrocketed [8]. Cutting-edge techniques like extreme ultraviolet (EUV) lithography and advanced material deposition require unprecedented energy and resource inputs [10]. The environmental toll of semiconductor fabrication, from massive electricity consumption to chemical waste, is now impossible to overlook [12]. With global reliance on electronics growing, the industry faces a critical challenge: balancing performance gains with sustainable production practices [15].

Sustainability is now a critical priority in semiconductor design, as leading foundries commit to net-zero targets despite energy consumption rivaling small nations [15]. While end-user chips grow more efficient, their fabrication remains resource-intensive, creating a paradox [16]. This work bridges the gap by integrating sustainability into early IC design alongside traditional power, performance, and area (PPA) metrics. We propose a framework to evaluate circuit-level building blocks—combinational, sequential, and analog cells—based on fabrication energy, material use, and operational impact [17]. Unlike existing methods focused on manufacturing (Scope 1–2 emissions), our approach addresses embedded design choices (Scope 3) through a PPAS (Power, Performance, Area, Sustainability) model [20]. By quantifying ecological costs during RTL design, designers can adopt greener alternatives without compromising PPA. This shift is essential to align chip innovation with planetary boundaries [19].

1.3 Successive Approximation Register Analog-to-Digital Converters

Analog-to-Digital Converters (ADCs) are fundamental building blocks in mixed-signal systems, enabling the translation of real-world analog signals into digital form for processing by modern electronics [3]. They play a critical role in applications ranging from sensor interfaces and communication systems to biomedical devices and consumer elec-

tronics. Mixed-signal devices like ADCs bridge the analog and digital domains, allowing seamless integration between continuous and discrete signal processing [2]. As such, they are essential for any application requiring interaction with the physical world, where signals such as sound, temperature, voltage, and pressure are inherently analog. Successive Approximation Register (SAR) ADCs are particularly well-suited for power- and area-constrained applications [7]. They are known for their relatively low power consumption, moderate speed, and small area footprint, making them a popular choice in portable and battery-powered systems such as wearable health monitors, IoT edge devices, and wireless sensors [22]. Unlike other high-performance ADC architectures like pipelined or sigma-delta, SAR ADCs offer a better trade-off in scenarios where ultra-high resolution or bandwidth is not the primary requirement [1]. The SAR architecture functions through a binary search algorithm, adjusting a digital approximation of the input signal over several clock cycles. This inherently sequential approach contributes to its lower power usage and simpler design [5]. Moreover, SAR ADCs benefit from digital scalability and are more amenable to process scaling in advanced CMOS technologies, unlike high-precision analog circuits that degrade at smaller nodes [8]. In this work, focusing on SAR ADC design highlights the importance of balancing power, performance, and area (PPA)—a key concern in modern chip design [17]. By analyzing these trade-offs, the project contributes toward more efficient mixed-signal system integration, especially in applications where both analog accuracy and digital efficiency must coexist without compromising sustainability or functionality [19].

1.4 Basic SAR ADC Operation

The Successive Approximation Register (SAR) analog-to-digital converter performs signal digitization through a binary search approach, executing three key operations: sampling the input voltage, iterative comparison, and digital output generation [3].

During the sampling phase, the input voltage V_{IN} is acquired by a binary-weighted capacitive DAC array. For an N-bit converter, this array consists of 2^N unit capacitors (C). Taking a 3-bit implementation as an example, the total capacitance sums to $8C$, comprising weighted values of $4C$, $2C$, $1C$ plus an additional $1C$ dummy capacitor for

symmetry [4]. The top plate voltage V_X remains fixed at the common-mode reference $V_{CM} = 0$ throughout sampling, expressed as:

$$V_X = V_{CM} = 0 \tag{1}$$

This configuration stores a charge Q_X across the capacitor network equal to:

$$Q_X = -V_{IN} \cdot 8C \tag{2}$$

Following sampling, the conversion process begins by successively approximating the input voltage through comparator decisions [5]. The algorithm commences with the most significant bit (MSB), where the DAC generates a trial voltage:

$$V_X = -V_{IN} + \frac{4C}{8C} V_{REF} \tag{3}$$

$$= -V_{IN} + \frac{1}{2} V_{REF} \tag{4}$$

The comparator evaluates whether this voltage falls below zero, indicating whether V_{IN} exceeds half of the reference voltage V_{REF} [6]. This determination sets the MSB value (D_2) to 1 if true, or resets it to 0 otherwise.

The process continues to the middle bit, where the DAC output now incorporates the previously determined MSB:

$$V_X = -V_{IN} + \frac{D_2 \cdot 4C + 2C}{8C} V_{REF} \tag{5}$$

$$= -V_{IN} + \left(\frac{D_2}{2} + \frac{1}{4} \right) V_{REF} \tag{6}$$

The comparator's output at this stage resolves the middle bit (D_1) [4]. Finally, the least significant bit evaluation completes the conversion by generating:

$$V_X = -V_{IN} + \frac{D_2 \cdot 4C + D_1 \cdot 2C + 1C}{8C} V_{REF} \tag{7}$$

$$= -V_{IN} + \left(\frac{D_2}{2} + \frac{D_1}{4} + \frac{1}{8} \right) V_{REF} \tag{8}$$

The comparator's final decision establishes the LSB (D_0), yielding the complete 3-bit digital representation of the original analog input [3]. This sequential approximation method provides an efficient conversion mechanism that scales effectively to higher resolutions while maintaining relatively low power consumption compared to alternative architectures [7].

1.4.1 Final Digital Output

After N comparisons, the DAC voltage converges to:

$$V_{DAC} = \sum_{i=0}^{N-1} D_i \cdot \frac{V_{REF}}{2^{i+1}} \tag{9}$$

where $D_i \in \{0, 1\}$ represents the resolved bits [2]. The SAR logic outputs the digital code $D_{N-1}D_{N-2} \ldots D_0$, completing the conversion. This charge-redistribution process ensures zero static power consumption, making SAR ADCs ideal for low-power applications [5, 7].

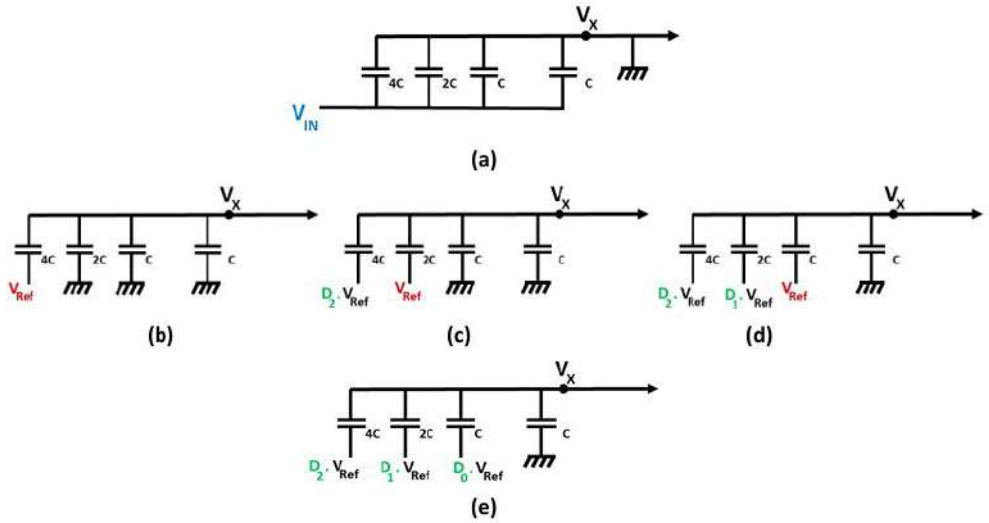

Figure 1.1: Node voltages of the DAC capacitors for each stage (a) Sampling phase, (b) Comparison 1, (c) Comparison 2, (d) Comparison 3, (e) Final binary output

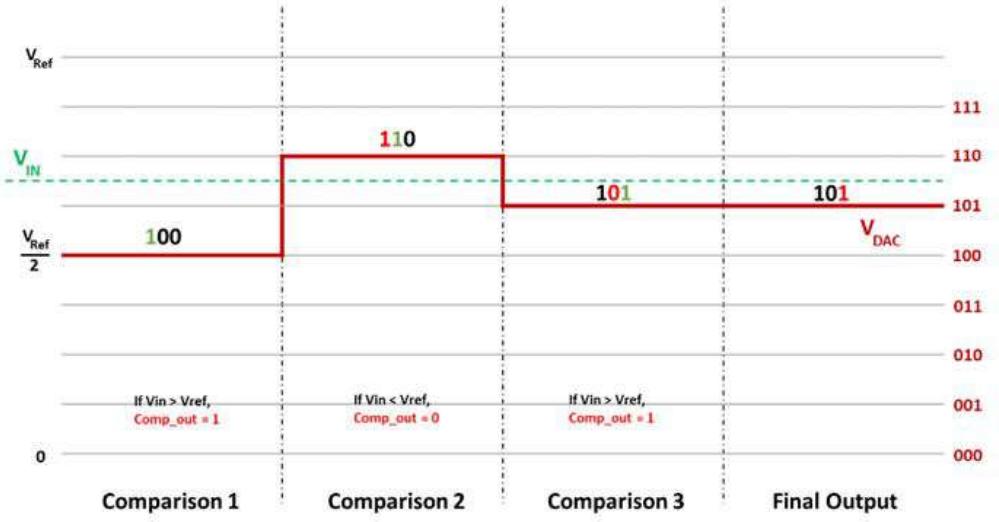

Figure 1.2: Binary search process in the 3-bit SAR system

CHAPTER 2

Literature Review

2.1 Differential SAR Architecture

The differential SAR ADC extends the single-ended architecture to process complementary input signals (V_{INP} and V_{INN}), offering enhanced noise immunity and linearity with several Key components [1].

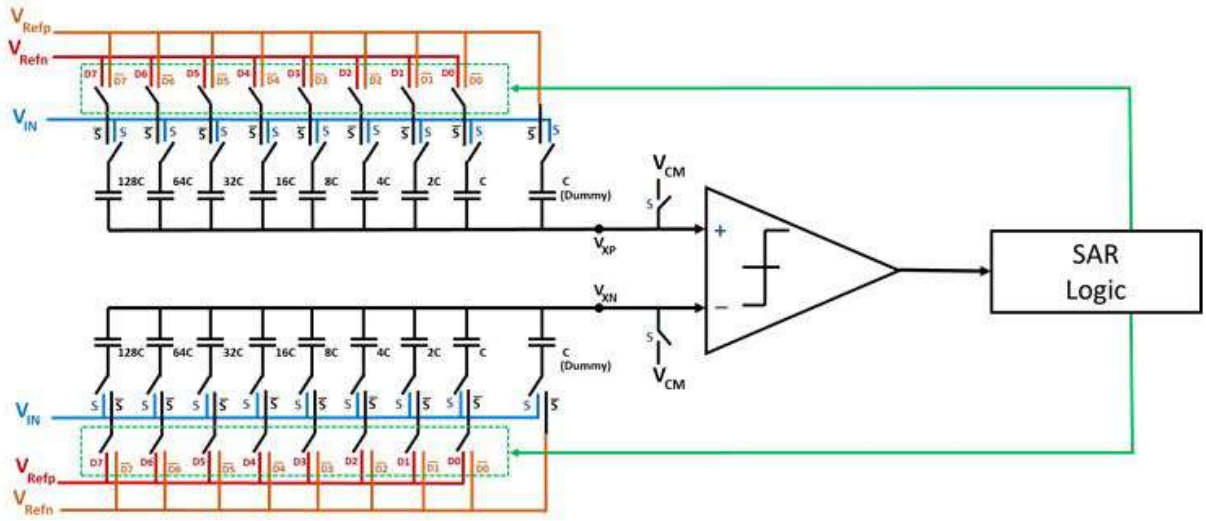

Figure 2.1: Differential capacitive DAC of an 8-bit SAR ADC

2.1.1 Differential Capacitive DAC

The differential DAC architecture utilizes two matched binary-weighted capacitor arrays to process both positive (V_{XP}) and negative (V_{XN}) signal paths simultaneously. During the sampling phase, the bottom plates of both arrays acquire the differential input signals V_{INP} and V_{INN}, while their top plates remain connected to the common-mode voltage V_{CM}. The reference voltages are established as complementary values around V_{CM}:

$$V_{\text{Refn}} = V_{\text{CM}} - \frac{V_{\text{REF}}}{2} \tag{10}$$

$$V_{\text{Refp}} = V_{\text{CM}} + \frac{V_{\text{REF}}}{2} \tag{11}$$

where V_{REF} represents the full-scale reference voltage spanning the converter's input range.

2.1.2 Comparison Mechanism

The conversion process relies on the comparator evaluating the differential voltage $\Delta V = V_{\text{XP}} - V_{\text{XN}}$ during each bit-cycling step. A positive differential voltage ($\Delta V > 0$) generates a logic '1' output, while negative values produce '0'. This decision directly controls the DAC code updates for subsequent approximation cycles.

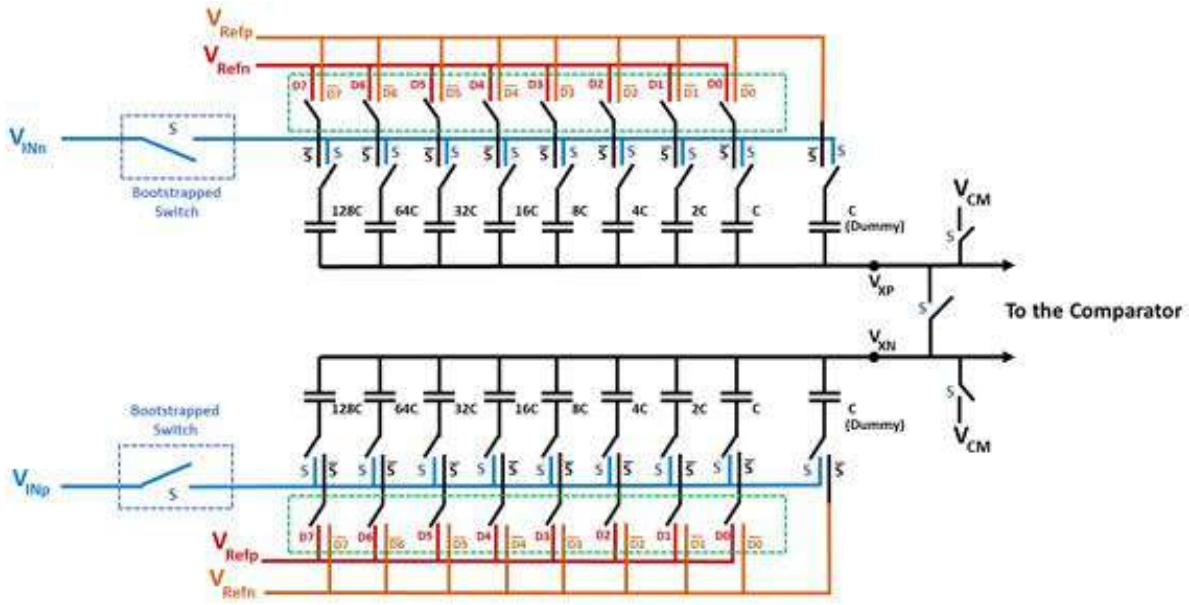

Figure 2.2: Differential capacitive DAC architecture showing dual capacitor arrays and switching network

2.1.3 Advantages Over Single-Ended Design

The differential configuration offers three key benefits compared to single-ended implementations. First, its inherent common-mode rejection capability (quantified by high CMRR) effectively cancels noise coupling that appears equally on both signal paths. Second, the symmetrical operation automatically suppresses even-order harmonic

distortions through balanced signal processing. Third, the differential architecture doubles the effective input voltage range to $2V_{\text{REF}}$, spanning from $-V_{\text{REF}}$ to $+V_{\text{REF}}$.

2.1.4 Trade-offs

These advantages come with two primary trade-offs. The dual capacitor arrays require twice the silicon area compared to single-ended designs, increasing layout complexity due to additional switches and interconnects. Furthermore, the complementary switching activity in both signal paths leads to marginally higher dynamic power consumption during conversion cycles.

The differential architecture proves particularly valuable in precision applications such as biomedical sensors and audio ADCs, where its noise robustness and distortion characteristics outweigh the area and power penalties. The charge redistribution follows the same binary search principle as single-ended converters, but with complementary voltage updates applied to both V_{XP} and V_{XN} during each approximation step.

2.2 Asynchronous SAR ADC Operation

An asynchronous SAR ADC differs from the synchronous type in that its internal blocks do not rely on a uniform global clock. Instead, the conversion sequence is controlled by handshaking signals between blocks [7]. The external clock only initiates the conversion, after which an internal clock generator produces two key signals: Clk_Sample, which triggers the sampling phase, and Clk_SAR, which drives the bit-by-bit conversion process. Once sampling is complete, Clk_SAR activates the SAR logic and DAC to apply a trial code. After a delay that allows the DAC to settle, Clk_SAR transitions low to activate the comparator. When the comparator finishes evaluation, it asserts a "Ready" signal, prompting the internal clock generator to initiate the next comparison cycle. This process repeats N times for an N-bit ADC. At the end, an End-Of-Conversion (EOC) signal triggers the output register to latch the final digital result. This self-timed operation reduces dynamic power and can speed up conversion compared to conventional clocked systems.

2.3 Bootstrapped Sample-And-Hold Circuit

The sample-and-hold (S/H) circuit is a critical block in SAR ADCs, responsible for accurately capturing the input voltage. Basic implementations use MOSFET switches, which introduce non-idealities such as input-dependent on-resistance (R_{ON}), charge injection, and clock feedthrough, all of which degrade sampling accuracy. To mitigate these effects, a bootstrapped switch is used [4]. This circuit maintains a constant gate-source voltage (V_{GS}) during the sampling phase, ensuring that the switch operates with low and consistent R_{ON}. The bootstrap mechanism involves pre-charging a capacitor during the hold phase and using it to fix the V_{GS} during sampling, effectively making the switch behave like a near-ideal resistor. This approach not only enhances linearity and bandwidth but also reduces distortion, enabling more accurate sampling of fast or low-amplitude signals.

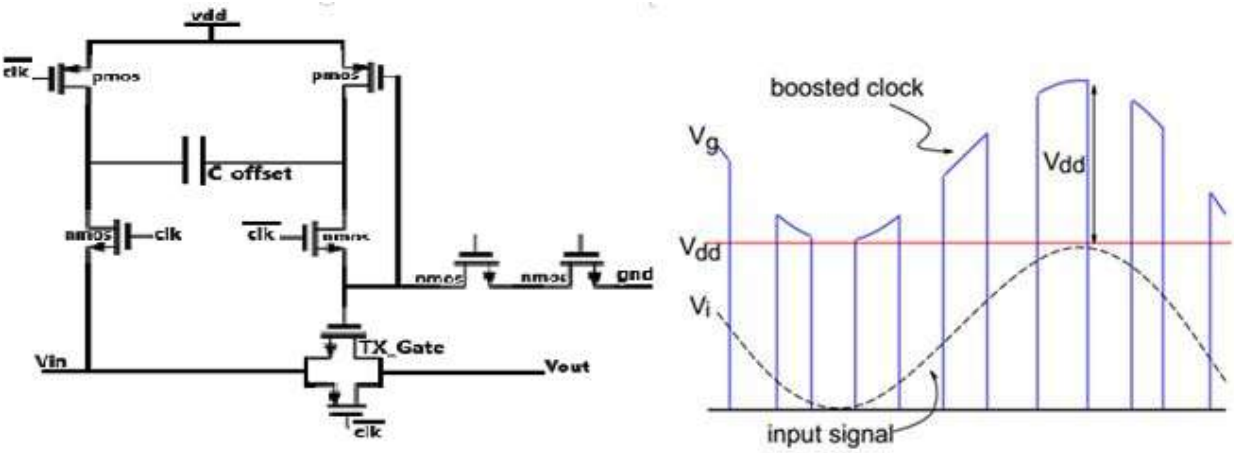

Figure 2.3: Schematic and waveform of the implemented bootstrapped switch circuit

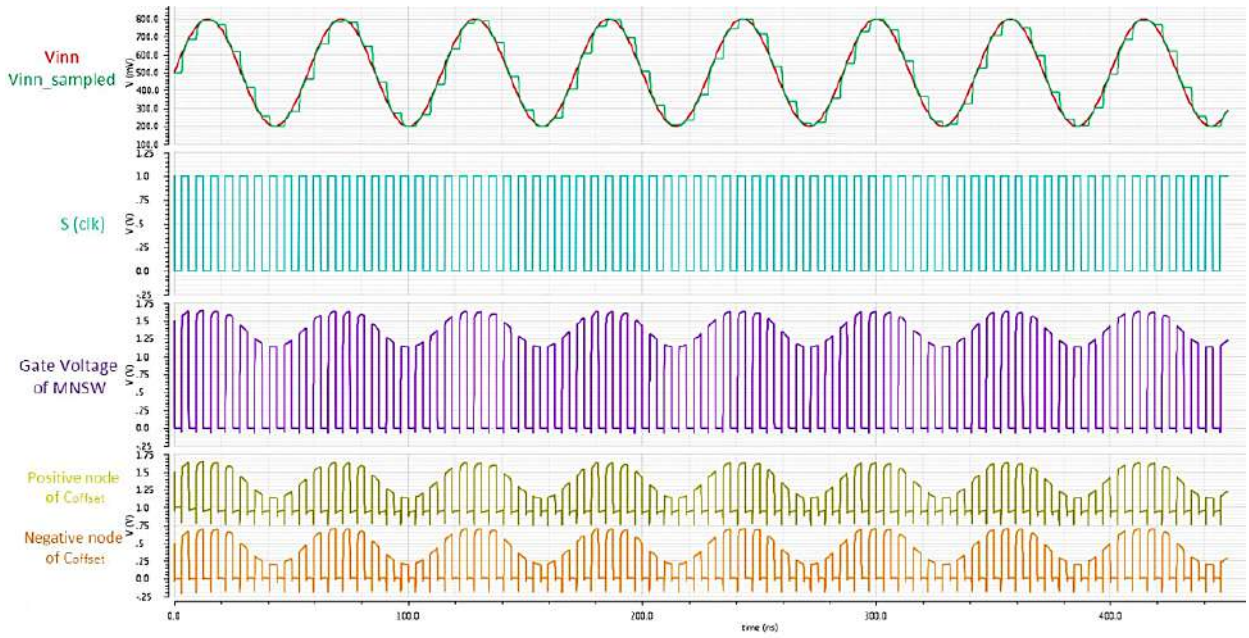

Figure 2.4: Waveform of both nodes of the implemented bootstrapped switch circuit

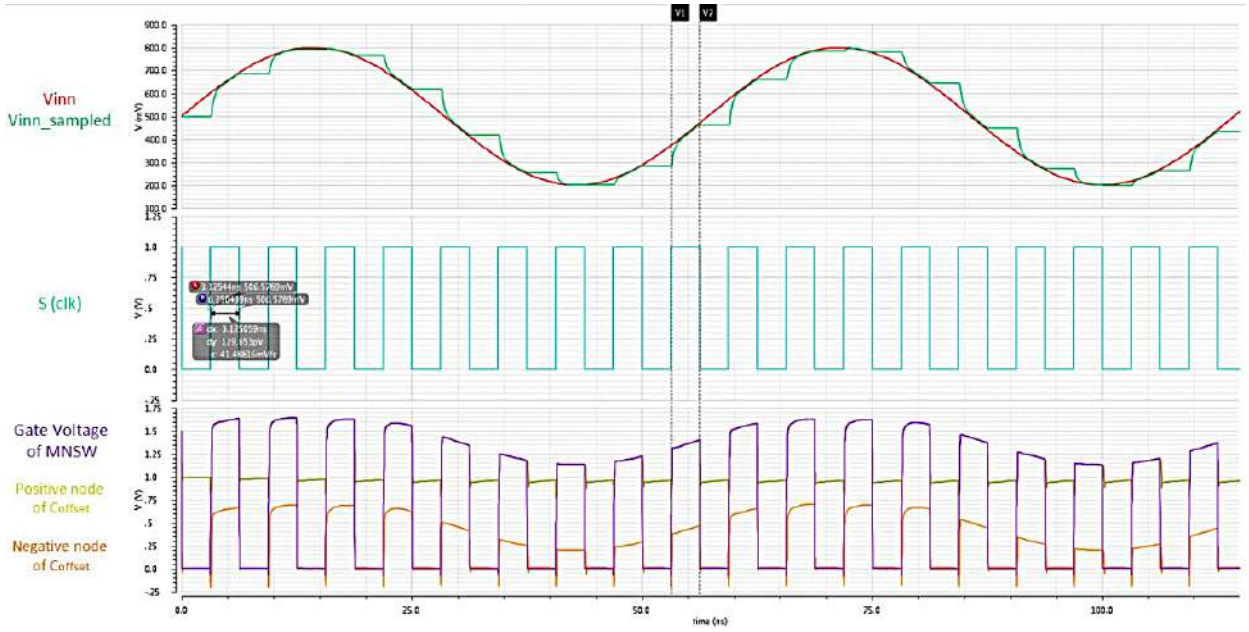

Figure 2.5: Closeup waveform of the implemented bootstrapped switch circuit

2.4 Differential Capacitive DAC

The capacitive digital-to-analog converter (DAC) in a SAR ADC translates digital codes into corresponding analog voltages for comparison. A conventional implementation uses a binary-weighted array of capacitors along with a dummy capacitor to maintain charge balance. In differential configurations, two such arrays are used—one for each polarity—providing improved common-mode noise rejection and signal integrity. Switching between the input sampling phase and the DAC conversion phase is accomplished using transmission gates, sized to minimize on-resistance while controlling parasitic capacitance. The choice of unit capacitance influences both speed and noise: smaller units increase speed but degrade signal-to-noise ratio (SNR), while larger units improve noise performance at the cost of area and settling time. An additional common-mode switch is employed to accelerate charge balancing during the sampling phase, enhancing speed and accuracy.

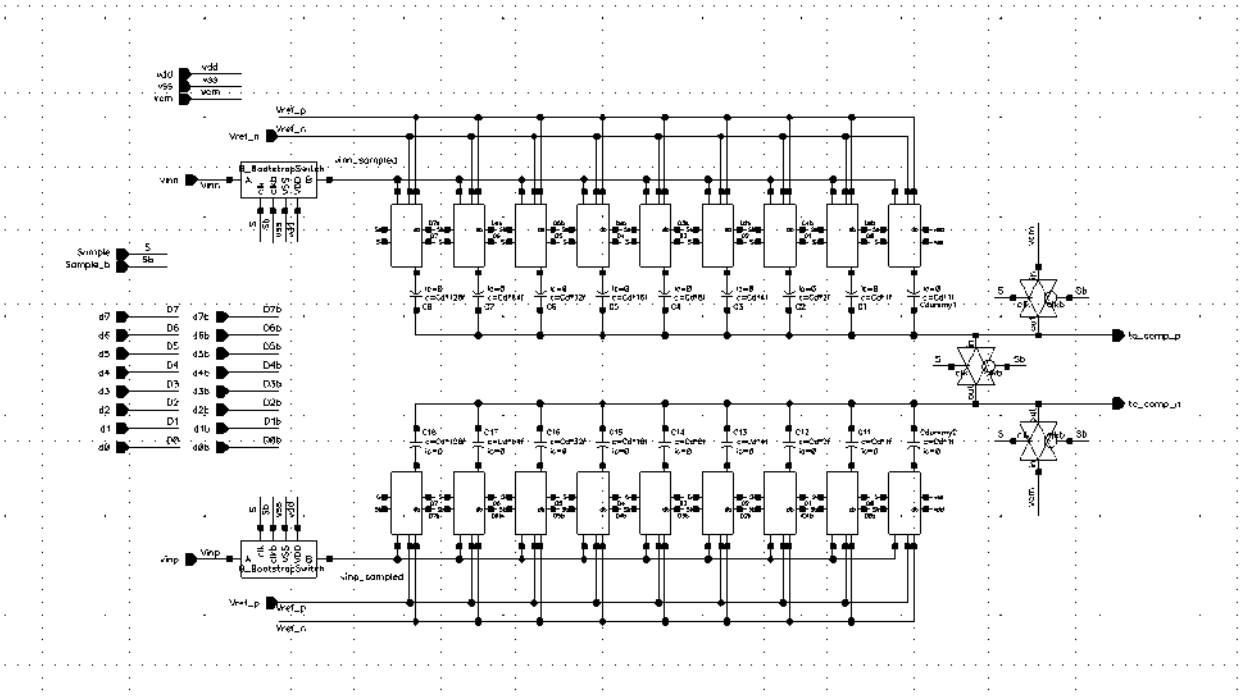

Figure 2.6: Schematic of the implemented Differential Capacitive DAC

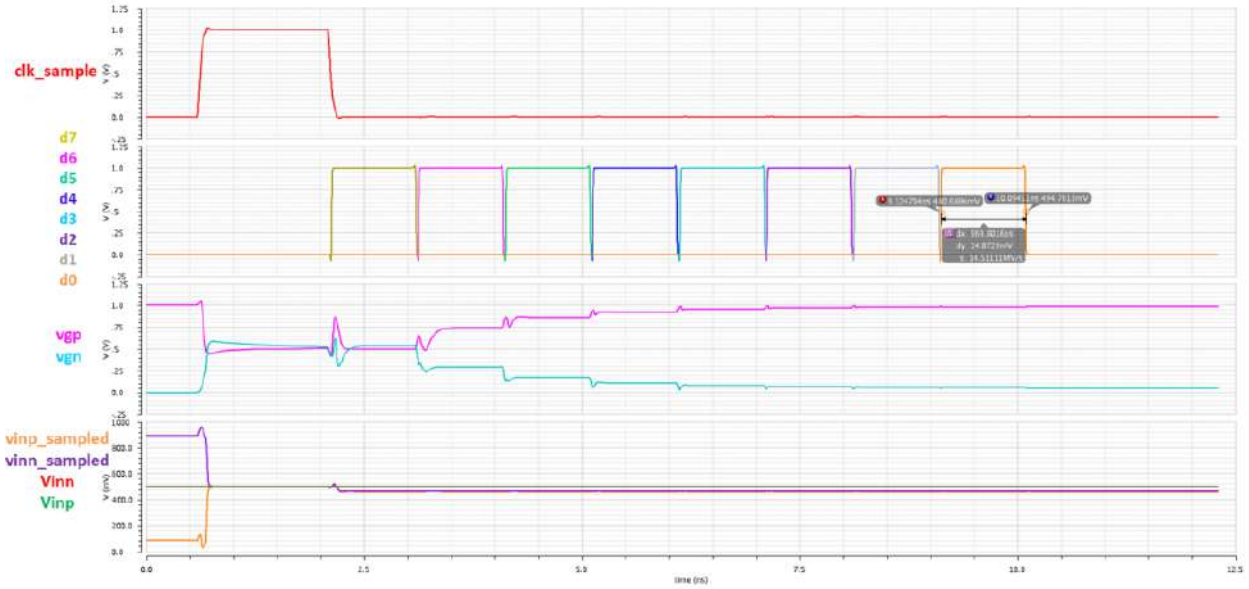

Figure 2.7: Waveform of the implemented Differential Capacitive DAC

2.5 Dynamic Comparator

The dynamic comparator is responsible for resolving the analog voltage difference produced by the DAC into a digital bit during each SAR iteration [5]. Compared to static or opamp-based comparators, dynamic comparators consume zero static power and offer faster response, making them ideal for low-power, high-speed ADCs. The design typically includes a strong-arm latch, which performs high-gain positive feedback amplification during the evaluation phase, and an RS latch to hold the decision. The comparator begins evaluation when Clk_SAR goes high, initiating regeneration in the strong-arm latch. Once the differential voltage exceeds the latch's input threshold, the outputs swing rail-to-rail. The RS latch retains the decision until the SAR logic captures it. An XOR gate detects when the comparator's outputs differ and generates a "Ready" signal to proceed with the next bit cycle. This architecture ensures high-speed operation, low kickback noise, and minimal power consumption.

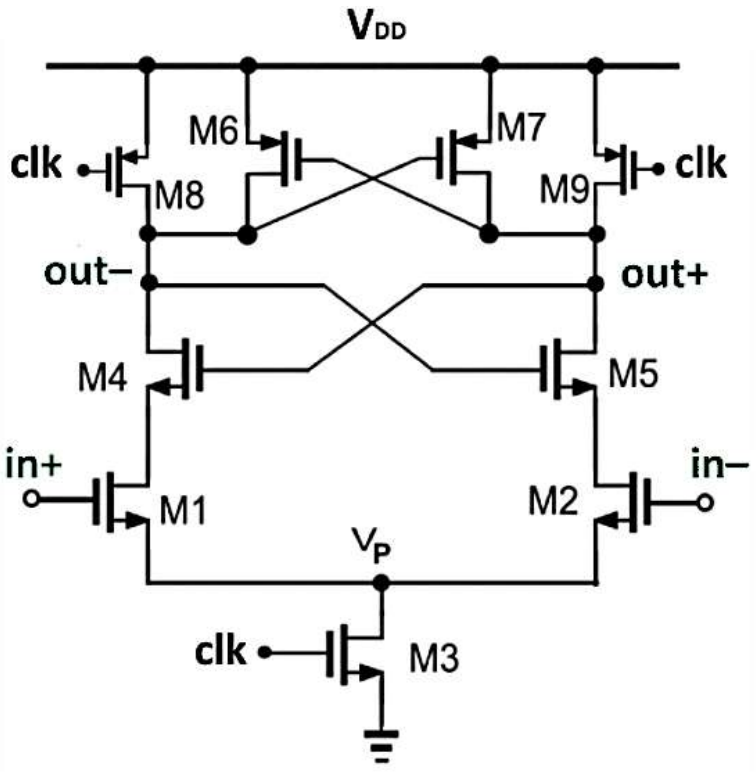

Figure 2.8: Schematic of the strong arm Comparator

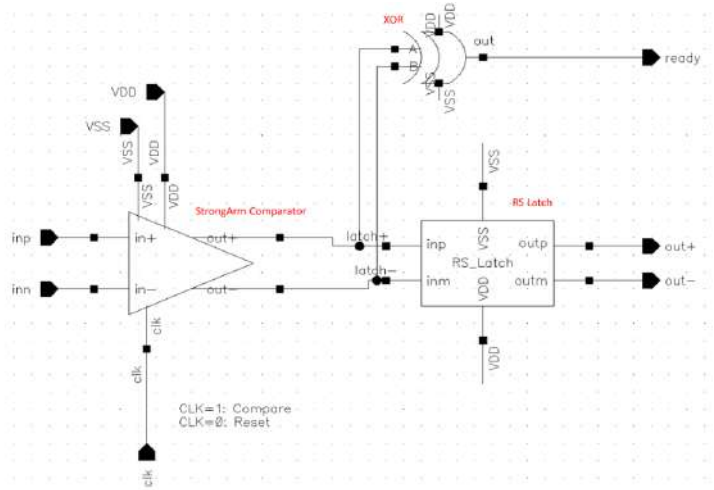

Figure 2.9: Schematic of the implemented Dynamic Comparator

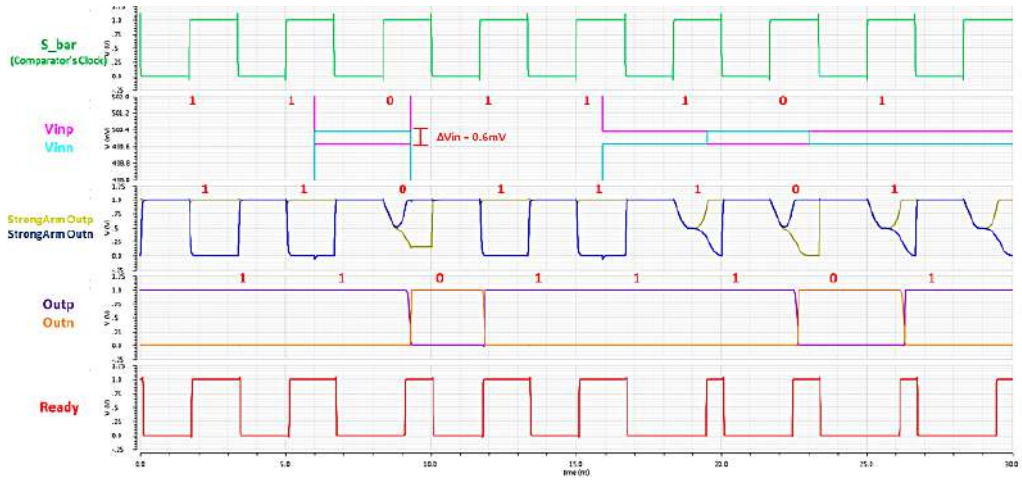

Figure 2.10: Waveform of the implemented Dynamic Comparator

2.6 SAR Logic

The SAR logic block coordinates the sequential bit decisions through two fundamental components: a sequencer register and a code register. Both structures utilize D-flipflops (FFs) but perform different functions in the conversion process. The sequencer register operates as a one-hot-code ring counter that manages the conversion timing sequence. With each rising edge of the internal clock signal (`clk_SAR`), a single logic '1' propagates sequentially through the flipflops, activating one bit position per conversion cycle starting with the MSB. This strict one-hot encoding guarantees that only one bit undergoes evaluation during any given iteration. Simultaneously, the code register maintains the accumulating digital output code. When the sequencer's active bit enables the set signal, the corresponding flipflop in the code register establishes its bit as '1'. The comparator's decision then modifies the previous bit through a derived clock signal originating from the sequencer.

In an 8-bit implementation, both registers contain eight flipflops, supplemented by additional circuitry for sequence initialization and End-of-Conversion (`EOC`) signal generation. During the sampling phase (`clk_sample = 1`), all flipflops reset to '0'. Following sampling, the sequencer commences the binary search algorithm, systematically progressing through each bit while the code register progressively builds the digital result. After completing eight clock cycles, the `EOC` pulse activates, prompting the output register to capture and hold the final conversion result.

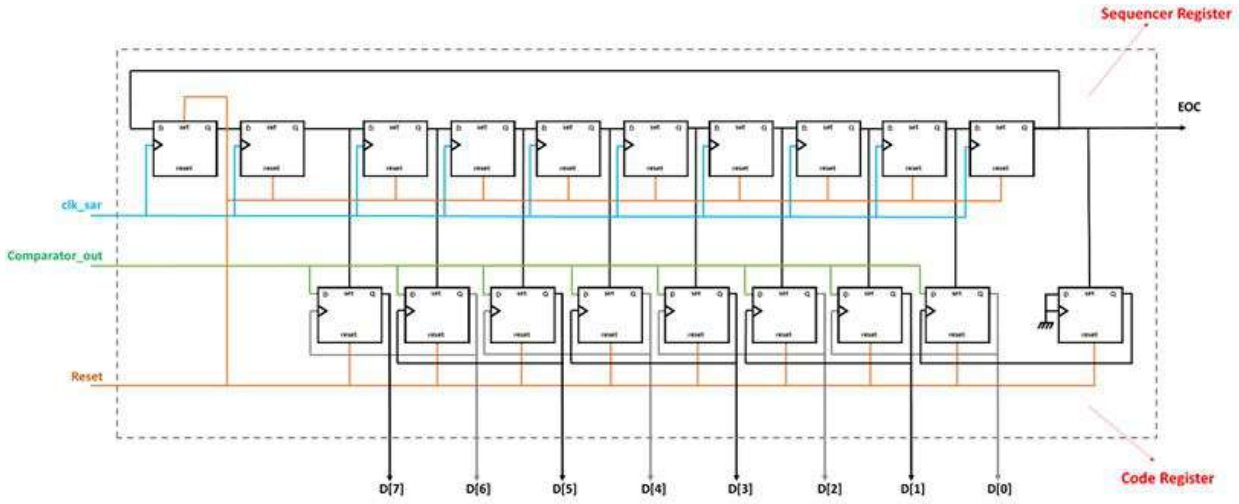

Figure 2.11: Block diagram of the SAR logic

		Sequencer Register Outputs										Code Register Outputs									Comparator Output
		DFF_init	DFF7	DFF6	DFF5	DFF4	DFF3	DFF2	DFF1	DFF0	DFF_end	DFFc7	DFFc6	DFFc5	DFFc4	DFFc3	DFFc2	DFFc1	DFFc0	DFFc_end	Comp_out
0	Sampling	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X
1	Comparison 1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	B7
2	Comparison 2	0	0	1	0	0	0	0	0	0	0	B7	1	0	0	0	0	0	0	0	B6
3	Comparison 3	0	0	0	1	0	0	0	0	0	0	B7	B6	1	0	0	0	0	0	0	B5
4	Comparison 4	0	0	0	0	1	0	0	0	0	0	B7	B6	B5	1	0	0	0	0	0	B4
5	Comparison 5	0	0	0	0	0	1	0	0	0	0	B7	B6	B5	B4	1	0	0	0	0	B3
6	Comparison 6	0	0	0	0	0	0	1	0	0	0	B7	B6	B5	B4	B3	1	0	0	0	B2
7	Comparison 7	0	0	0	0	0	0	0	1	0	0	B7	B6	B5	B4	B3	B2	1	0	0	B1
8	Comparison 8	0	0	0	0	0	0	0	0	1	0	B7	B6	B5	B4	B3	B2	B1	1	0	B0
9	Final Output	0	0	0	0	0	0	0	0	0	1	B7	B6	B5	B4	B3	B2	B1	B0	1	X
											EOC										

Figure 2.12: Schematics of the proposed SAR logic block

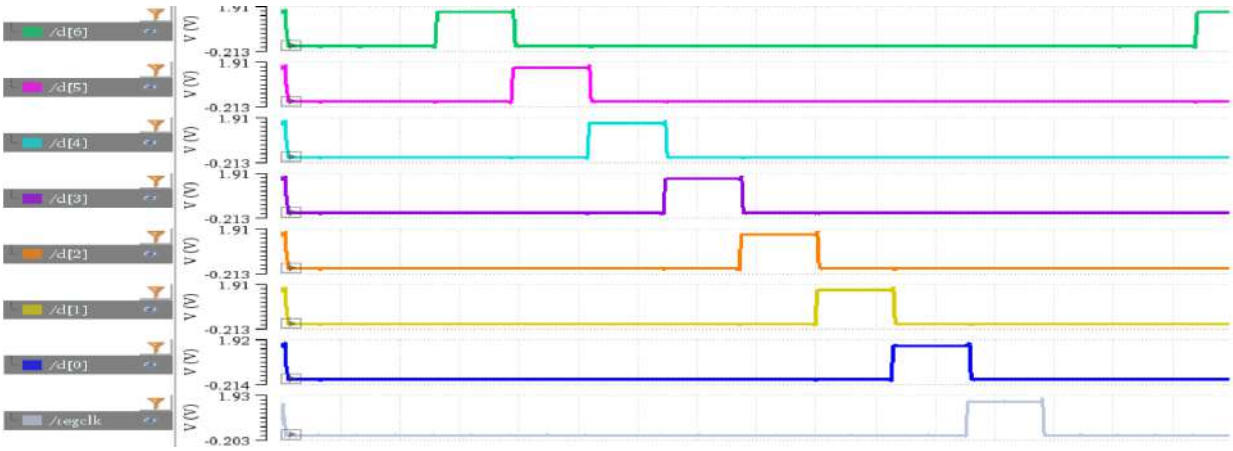

Figure 2.13: Waveform of the implemented SAR logic block

The design uses True Single-Phase Clock (TSPC) flipflops for their low dynamic power and compact layout. TSPC FFs eliminate static current paths and reduce transistor count compared to conventional CMOS FFs. Asynchronous set/reset functionality is integrated to force initial states without additional control logic. Weak cross-coupled

inverters in the code register allow overwriting by new comparator decisions, ensuring accurate bit updates.

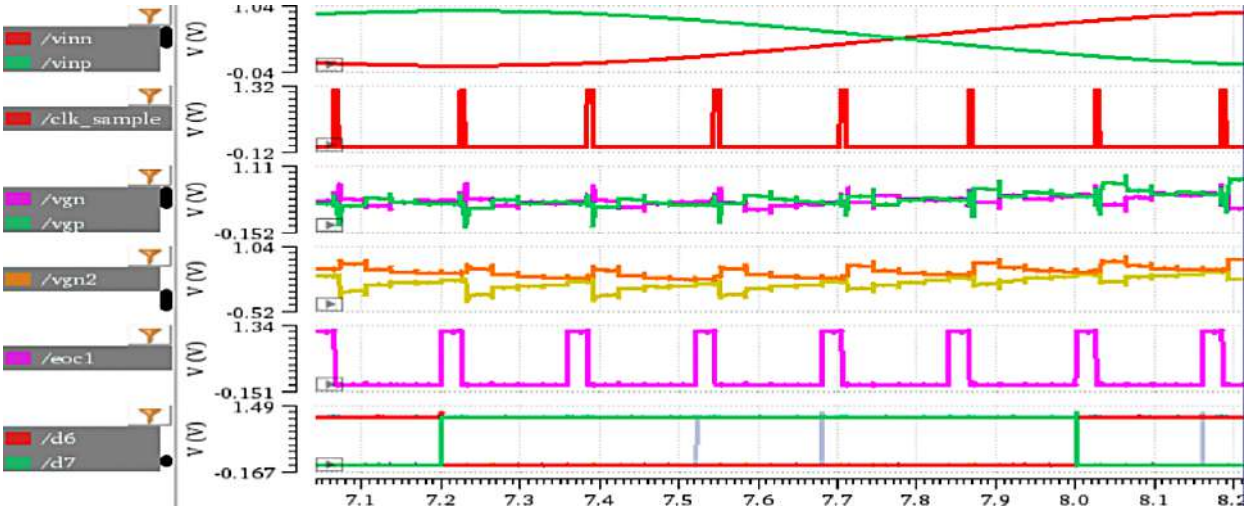

Figure 2.14: Waveform of all processes

2.7 Output Register

The output register acts as the critical interface between the SAR logic and external systems, providing synchronized delivery of the final digital conversion result. This essential block performs three key functions: data latching, timed release, and signal integrity maintenance. It captures the 8-bit DAC code from the SAR logic precisely at the rising edge of the End-of-Conversion (`EOC`) signal, then holds this value until the subsequent falling edge of `EOC` - a timing strategy that aligns with the next external clock cycle to prevent metastability during readout operations. Additionally, it ensures robust digital interfacing by maintaining full rail-to-rail voltage levels throughout the output stage.

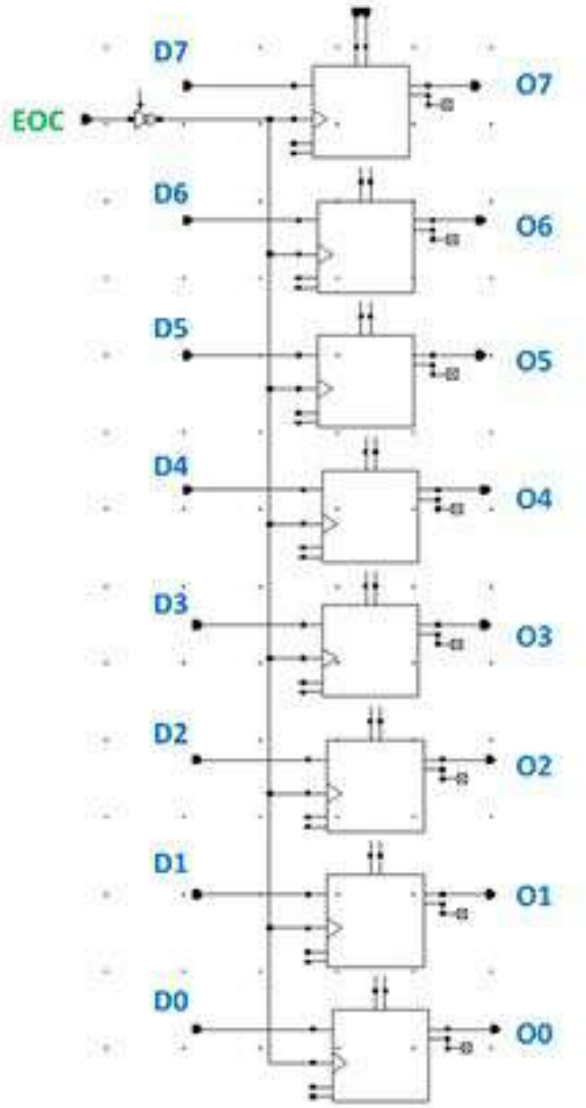

Figure 2.15: Detailed schematic of the output register implementation showing the 8-bit parallel flipflop structure

The register architecture employs eight standard CMOS D-flipflops (one per bit) rather than TSPC (True Single Phase Clock) designs for two specific reasons. First, since the EOC signal operates at the relatively low external clock frequency (typically 20 MHz in this implementation), the high-speed capabilities of TSPC logic become unnecessary. Second, CMOS flipflops provide superior voltage compliance, guaranteeing full-swing outputs ranging from $0\,\mathrm{V}$ to V_{DD} even when driving substantial capacitive loads from downstream circuitry.

During normal operation, while the SAR logic progressively refines the DAC code through successive approximation, the output register remains inactive. Only when all

8 bits are fully resolved does the EOC pulse initiate the register's operation. This trigger causes two sequential actions: first, the rising edge captures the final digital code ($D_7D_6 \ldots D_0$) into the flipflops; second, the register maintains this value until the subsequent falling edge of EOC, thereby synchronizing data transfer with the system clock domain. The latched code subsequently drives an ideal output DAC (described in Section 2.8) for analog reconstruction, enabling critical performance measurements like Effective Number of Bits (ENOB) and Signal-to-Noise Ratio (SNR) through FFT analysis. This staged architecture effectively decouples the high-speed SAR conversion process from the output interface, significantly reducing timing conflicts and power supply noise coupling.

2.8 Ideal DAC

The ideal DAC serves as a critical performance evaluation block that converts the final 8-bit digital code ($D_7D_6 \ldots D_0$) from the SAR logic into its corresponding analog voltage representation [6]. This conversion enables two essential functions: precise analog reconstruction of the digitized signal and proper normalization to match the ADC's full-scale input range for accurate error analysis.

The implementation employs eight binary-weighted ideal voltage-controlled voltage sources (VCVS) arranged in series configuration (Fig. 2.16). Each VCVS corresponds to one bit in the digital code, with their collective output voltage determined by the weighted sum:

$$V_{\text{OUT}} = \frac{1}{2^8}\left(D_7 \cdot 2^7 + D_6 \cdot 2^6 + \cdots + D_0 \cdot 2^0\right)$$

A final normalization stage applies appropriate gain and offset through an additional VCVS to ensure the reconstructed output spans the complete differential input range:

$$V_{\text{OUT,adj}} = V_{\text{OUT}} \cdot (V_{\text{Refp}} - V_{\text{Refn}}) + V_{\text{Refn}}$$

where V_{Refp} and V_{Refn} represent the positive and negative reference voltages respectively (typically 1.2V peak-to-peak for this design). This scaling enables direct comparison with the original input signal for calculating critical performance metrics including

integral nonlinearity (INL) and differential nonlinearity (DNL) through spectral analysis techniques like 64-point FFT.

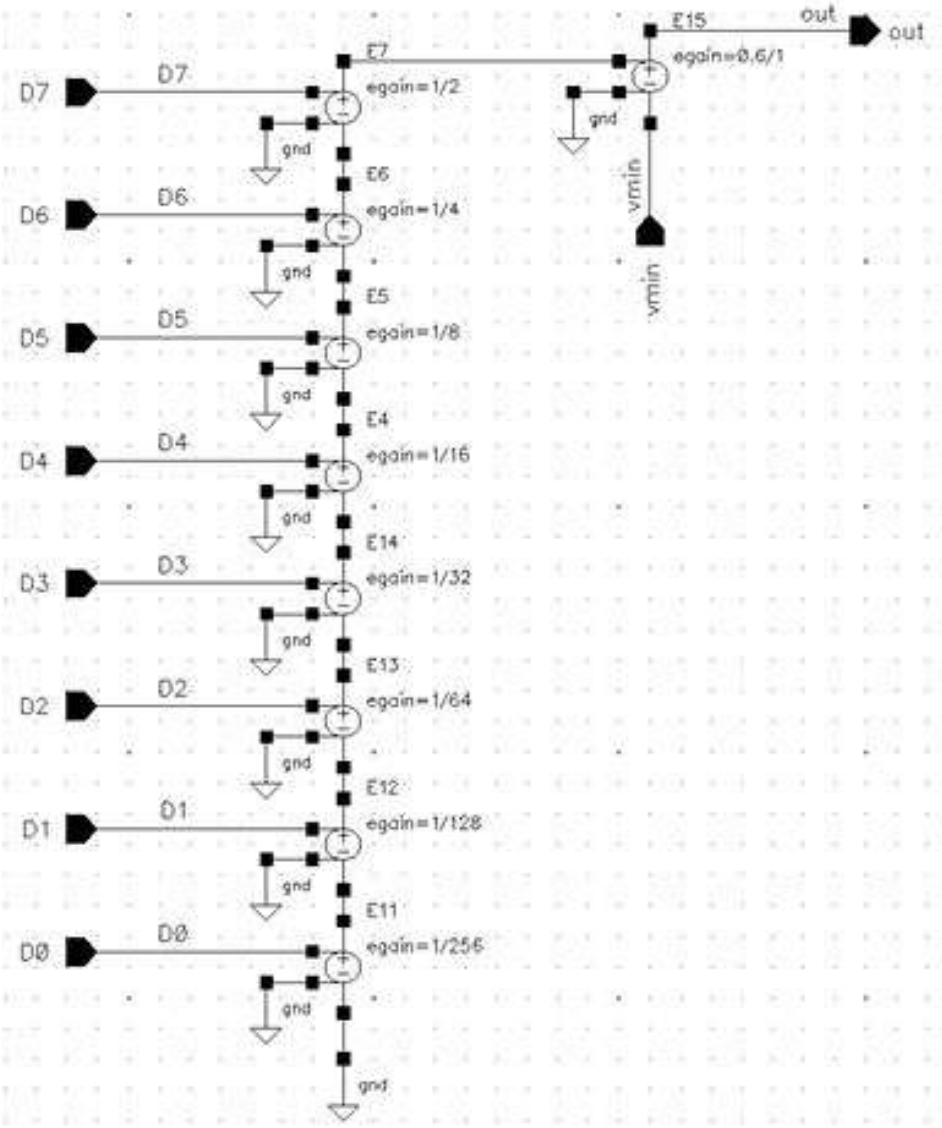

Figure 2.16: Implementation schematic of the ideal output DAC showing the series-connected VCVS architecture

Three key characteristics define this DAC implementation. First, its idealized VCVS-based model intentionally excludes real-world non-idealities such as capacitor mismatch and switch resistance, creating a clean reference for post-conversion validation. Second, the inherent binary-weighted structure guarantees monotonic output behavior - a fundamental requirement for proper SAR ADC operation. Third, the modular design readily scales to higher resolutions through additional VCVS stages without architectural modifications.

The table above summarizes the key performance metrics of the ADC, including power, resolution, speed, and linearity. Additionally, it presents the calculated ENOB and energy efficiency figure of merit (FOM), useful for comparing ADC designs across technologies.

Table 2.1: SAR ADC Performance Summary

Parameter	**Value**
Power Supply (V)	1.25
Resolution (bits)	8
Sampling Rate (MS/s)	25
Sampling unit cap (fF)	13
SNR (dB)	46.03
SINAD (dB)	46.03
SFDR (dBc)	50.84
ENOB	7.35
Total Power (μW)	191.4
FOM (pJ/conversion-step)	0.0469

$$\text{ENOB (in Bits)} = \frac{\text{SINAD} - 1.76}{6.02} \tag{2.1}$$

$$\text{FOM} = \frac{P_{\text{total}}}{2^{\text{ENOB}} \cdot f_s} \tag{2.2}$$

The equations relates the Effective Number of Bits (ENOB) to the SINAD (Signal-to-Noise and Distortion ratio) and computes the Figure of Merit (FOM) as the energy consumed per conversion step, allowing comparison of energy efficiency across ADCs.

Notably, this DAC exists solely for testing purposes and does not contribute to the ADC's operational power budget. This isolation allows precise characterization of the SAR logic and comparator performance during device evaluation, free from DAC-induced artifacts.

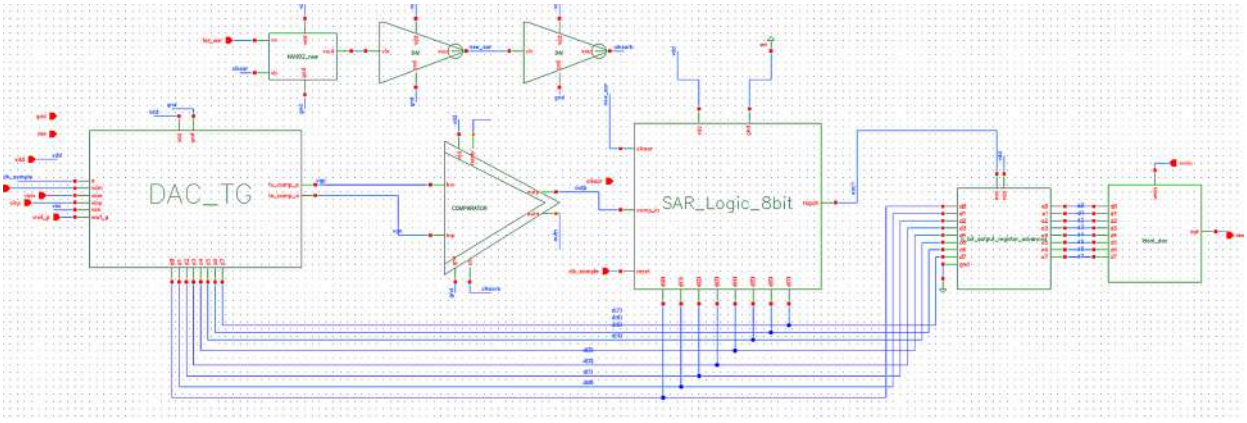

Figure 2.17: Schematic of 8-bit SAR ADC

Figure 2.18: Layout of 8-bit SAR ADC

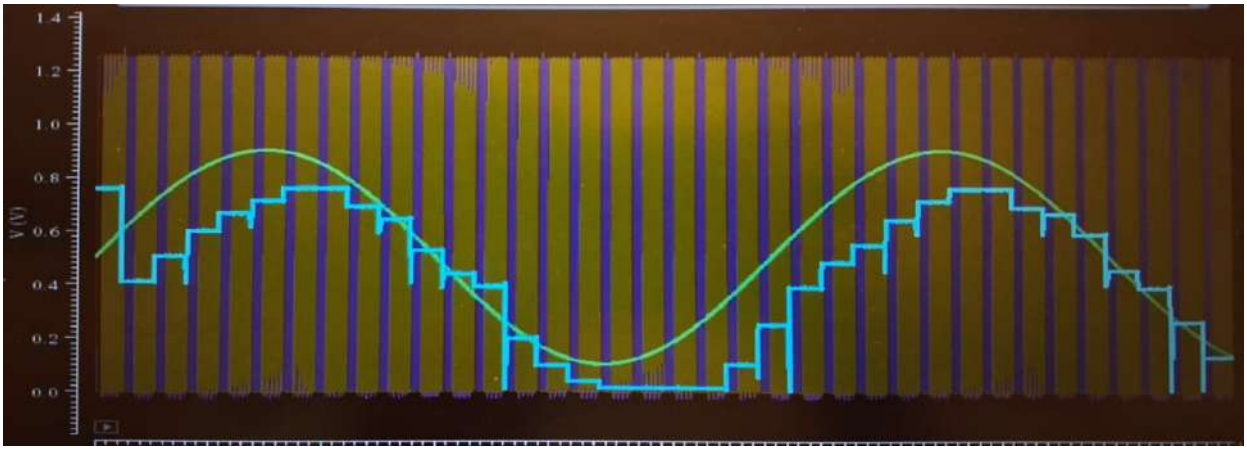

Figure 2.19: Ideal DAC waveform to calculate ENOB of the implemented 8-bit SAR ADC

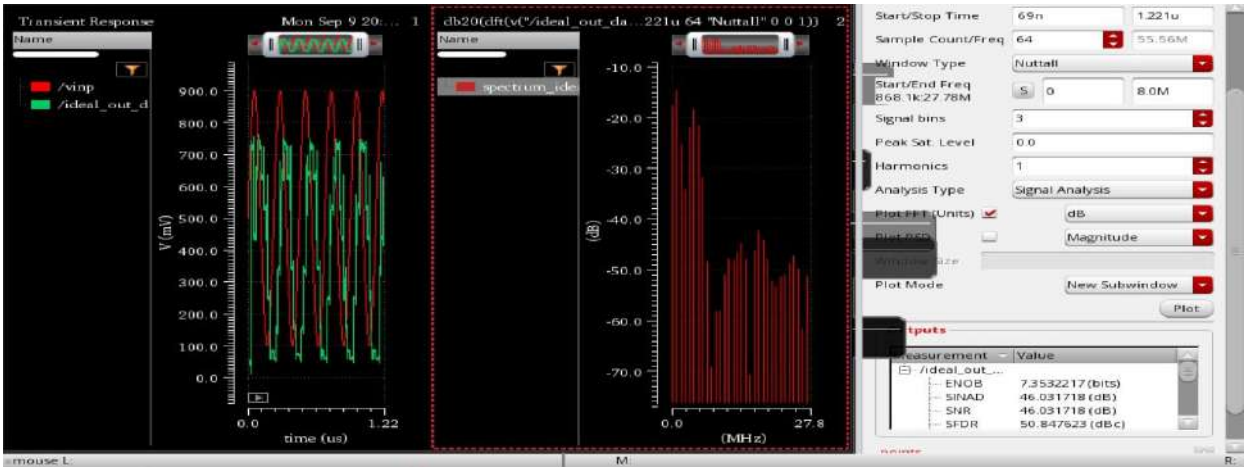

Figure 2.20: Results of the implemented 8-bit SAR ADC

CHAPTER 3

Proposed Pipelined SAR ADC

3.1 Pipelined SAR ADC Architecture

The pipelined SAR ADC architecture combines the energy efficiency of SAR-based conversion with the throughput benefits of pipelining, enabling high-speed digitization for applications such as wireless communication and real-time signal processing [1]. By partitioning an 8-bit conversion into two cascaded 4-bit stages, the design reuses core components from a conventional SAR ADC while introducing critical enhancements for parallelism and precision.

Stage-Wise Operation

The pipelined SAR ADC operates through two coordinated 4-bit stages with residue amplification between them. In Stage-1, a bootstrapped sample-and-hold circuit first captures the differential input (V_{INP}, V_{INN}) using a switch that maintains constant gate-source voltage (V_{GS}) to ensure linear sampling across process variations. This technique significantly reduces harmonic distortion [4]. The subsequent 4-bit differential capacitive DAC generates trial voltages during the SAR conversion process, controlled by a streamlined SAR logic block. This logic utilizes a one-hot sequencer with True Single-Phase Clock (TSPC) flip-flops to rapidly resolve the 4 MSBs within 160 ns. A metastability-optimized comparator evaluates the DAC output against the held input voltage, with results stored in a low-leakage output register.

Following Stage-1 completion, the residual voltage ($V_{\text{res}} = V_{\text{IN}} - V_{\text{DAC}}$) undergoes amplification through a capacitively degenerated dynamic amplifier. This amplification stage ensures the residue spans the full-scale range of Stage-2 while maintaining linearity. The capacitive degeneration technique reduces sensitivity to transistor mismatches, and dynamic biasing eliminates static power consumption entirely.

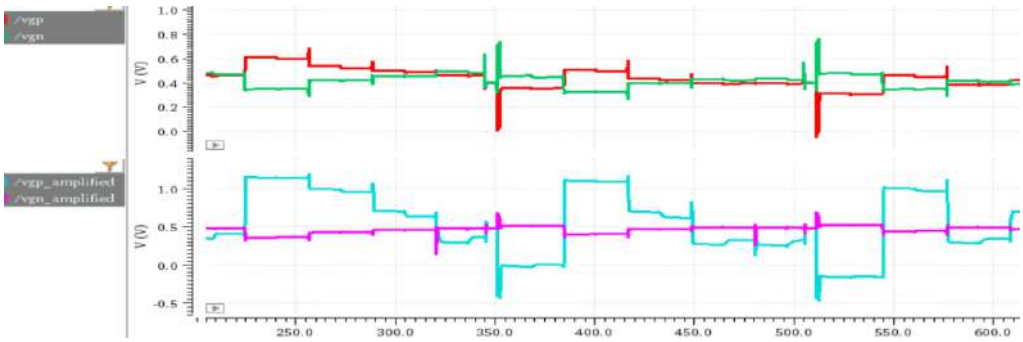

Figure 3.1: Residue amplifier waveform showing input-output characteristics and settling behavior

Stage-2 mirrors Stage-1's architecture but processes the amplified residue instead of the original input. The key innovation lies in the concurrent operation - while Stage-1 samples a new input, Stage-2 simultaneously processes the previous residue. This parallelism reduces the conversion time effectively doubling throughput [6]. A carefully designed 1-clock-cycle delay buffer ensures proper synchronization between stages, maintaining coherent alignment of the 4 MSBs and 4 LSBs at the final output register.

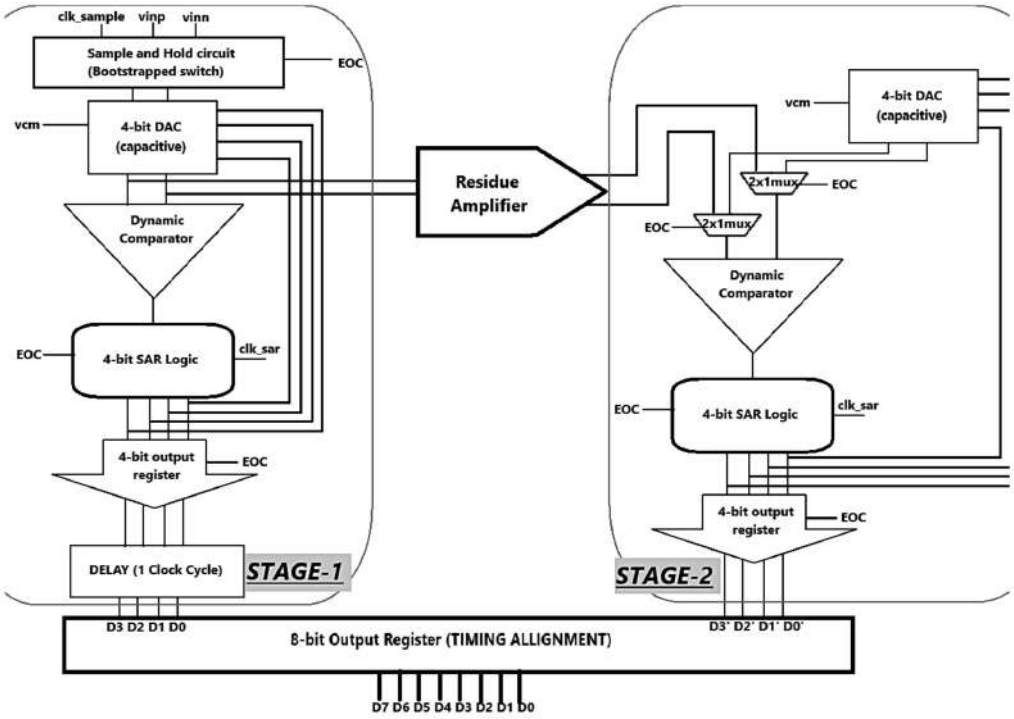

Figure 3.2: System block diagram of the 8-bit pipelined SAR ADC showing stage parallelism and data flow

Architectural Modifications

Several key modifications differentiate this design from conventional SAR ADCs. The SAR logic simplification to 4-bit resolution per stage reduces sequencer complexity, requiring fewer flip-flops in the one-hot ring counter. This optimization lowers both clock distribution complexity and dynamic power consumption. TSPC flip-flops enable rapid bit cycling, supporting decisions at 300 MHz with sub-nanosecond settling times. Digital delay elements inserted between stages precisely synchronize Stage-1 and Stage-2 outputs, compensating for residue amplification latency. Programmable delay cells provide adjustment capability across PVT corners, mitigating timing mismatches from process variations.

The inter-stage amplifier employs a differential pair with capacitive load modulation, where degeneration capacitors actively suppress common-mode noise [1]. This innovative approach preserves signal integrity during residue amplification, maintaining the signal-to-noise ratio (SNR) critical for achieving the target Effective Number of Bits (ENOB).

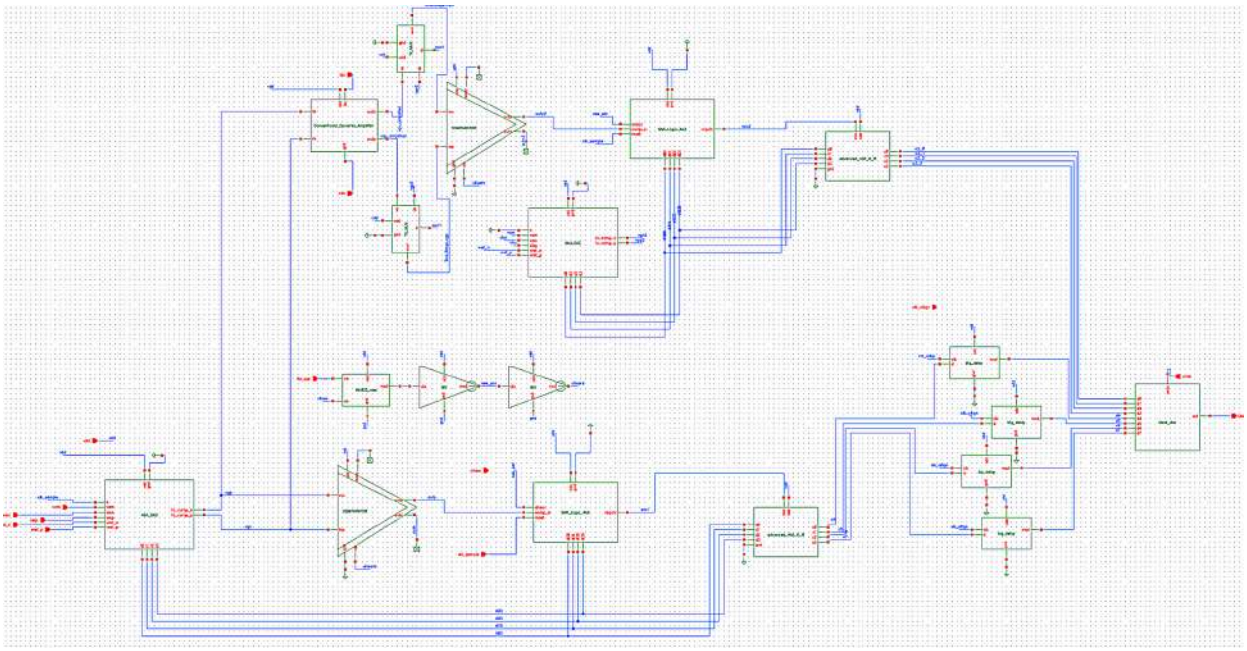

Figure 3.3: Detailed schematic of the 8-bit pipelined SAR ADC implementation

System-Level Advantages

The pipelined architecture delivers four significant advantages over conventional designs. First, through stage parallelism, doubling the throughput of standard 8-bit SAR ADCs - a critical capability for 5G basebands and high-speed data acquisition systems. Second, the reuse of SAR sub-blocks (DAC, comparator, TSPC logic) creates exceptional power and area efficiency; the 4-bit capacitive DAC occupies less area than an 8-bit array while shared dynamic comparators reduce analog front-end complexity.

Table 3.1: Pipelined SAR ADC Performance Summary

Parameter	**Value**
Power Supply (V)	1.25
Resolution (bits)	8
Sampling Rate (MS/s)	55.55
Sampling unit cap (fF)	13
SNR (dB)	43.8
SINAD (dB)	43.8
SFDR (dBc)	48.6
ENOB	6.98
Total Power (μW)	248.8
FOM (pJ/conversion-step)	0.0354

The table above summarizes the key performance metrics of the ADC, including power, resolution, speed, and linearity. Additionally, it presents the calculated ENOB and energy efficiency figure of merit (FOM), useful for comparing ADC designs across technologies.

Third, the modular design supports straightforward resolution scaling through additional stages (e.g., 12-bit using three 4-bit stages), with each stage operating independently to simplify layout and enable pipelined parallelism [7]. This modularity also streamlines testing, allowing individual stage validation for linearity and offset. Finally, when evaluated under the Power, Performance, Area, and Sustainability (PPAS) framework, the design demonstrates reduced embodied carbon footprint (eCFP) through area-efficient layouts and lower operational carbon footprint (oCFP) via dynamic power management techniques [19]. The complete elimination of static currents in both amplifiers and TSPC logic further enhances the energy efficiency profile.

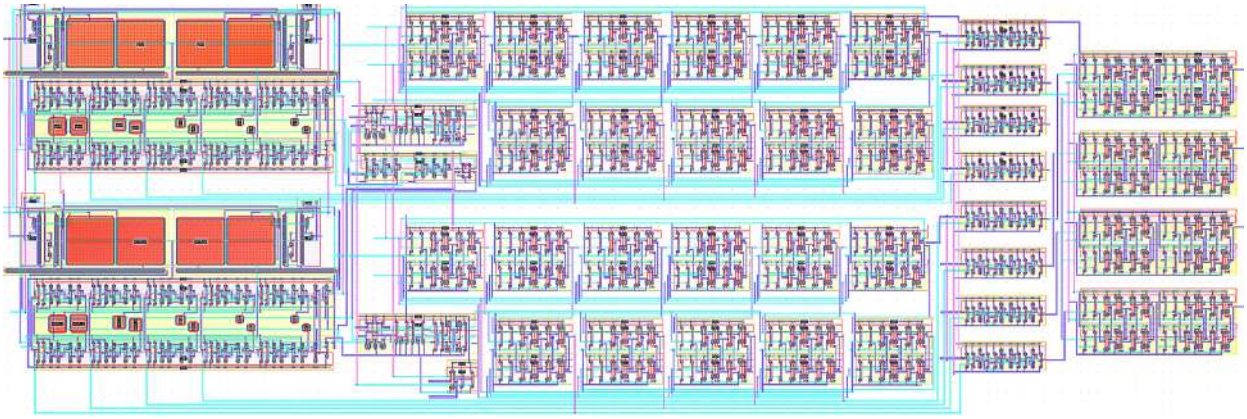

Figure 3.4: Layout of 8-bit Pipelined SAR ADC

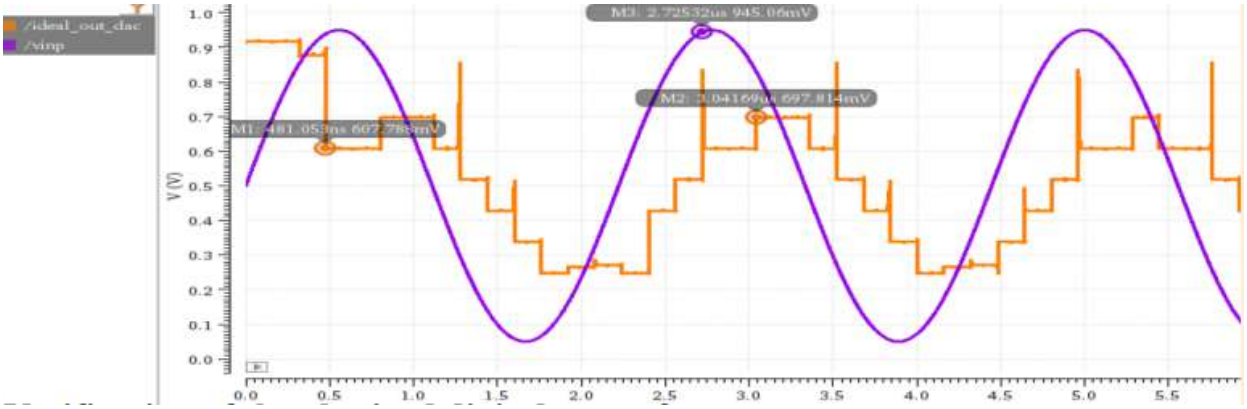

Figure 3.5: Ideal DAC waveform to calculate ENOB of the implemented 8-bit SAR ADC

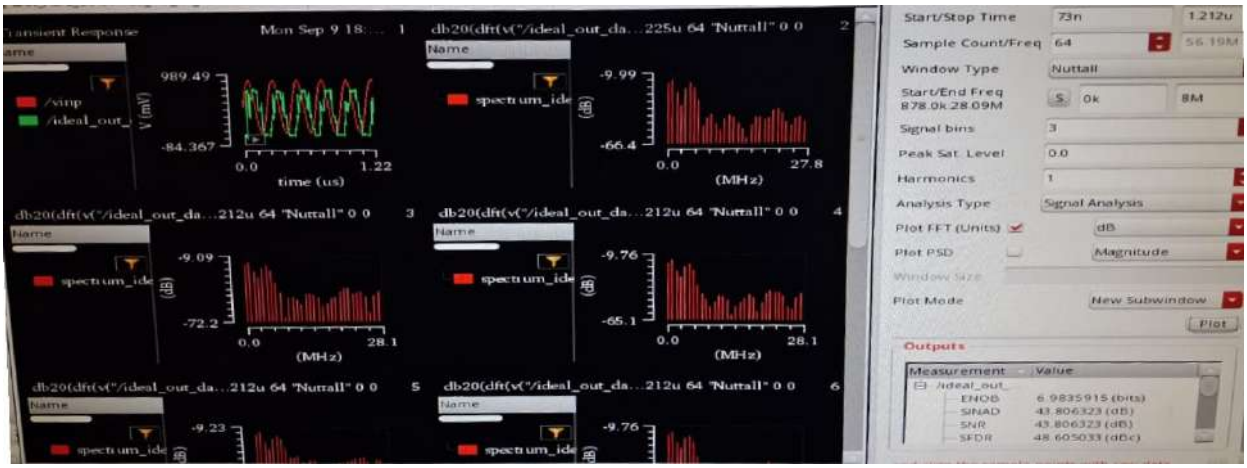

Figure 3.6: Results of the implemented 8-bit Pipelined SAR ADC

CHAPTER 4

Sustainability metric and analysis on circuit

4.1 Sustainability Metrics in VLSI Design

The Need for Sustainability in Semiconductor Design

The semiconductor industry's exponential growth has led to significant environmental concerns, with IC manufacturing now contributing substantially to global carbon emissions [11]. Traditional design metrics (Power, Performance, and Area - PPA) fail to capture the ecological impact of chip production and operation. Recent studies reveal that advanced nodes consume disproportionately more energy during fabrication, with TSMC's annual electricity demand surpassing entire countries [15]. This necessitates a paradigm shift toward *sustainability-aware design*, incorporating environmental impact as a first-class design constraint.

The Greenhouse Gas (GHG) Protocol classifies emissions into three scopes: Direct emissions from manufacturing (e.g., fab energy, chemicals), Indirect emissions from purchased energy and the last Supply chain and product lifecycle emissions [19].

4.1.1 Unified Sustainability Metrics Framework

Recent works propose extending PPA to PPAS (Power, Performance, Area, Sustainability) through two key metrics [17]:

4.1.2 Energy and Carbon Estimation Metrics for ADC Designs

4.1.2.1 Energy Consumption per IP

The energy consumed during wafer processing is distributed across the total die area and then scaled to the area of the individual IP block—in this case, the ADC. This allows us to approximate the energy cost associated with fabricating the ADC block alone. The energy per IP is defined as:

$$\text{Energy per IP} = \left(\frac{\text{Energy of wafer in kWh}}{\text{Area of wafer}} \right) \times \text{Area of IP} \tag{4.1}$$

In this work, energy consumption data is referenced from a 65nm CMOS process using a 6-metal layer stack for a 300mm wafer [8]. The energy per unit area is assumed constant across designs for comparative analysis.

4.1.2.2 Mask Overhead Estimation

The number of photomasks used during fabrication directly affects the embodied carbon footprint due to increased processing complexity. A 'Mask Overhead' factor is introduced to quantify the energy penalty associated with additional masks beyond a reference baseline. It is computed as:

$$\text{Mask Overhead} = ((\text{Total Mask} - \text{Ref. Mask}) \times \text{MF} + 1) \tag{4.2}$$

In the context of ADC designs, extra masks may be required for specialized devices such as high-precision capacitors or different threshold voltage transistors used for comparator biasing or logic control [10]. If more metal layers or analog-specific features are involved, the total number of masks increases accordingly, thereby raising the energy footprint.

4.1.2.3 Congestion Penalty Factor (CPF)

High-density mixed-signal integration, especially in SoC environments, can lead to routing congestion when large IP blocks like ADCs occupy upper metal layers. This limits the available routing tracks for digital and system-level connections. The Congestion Penalty Factor accounts for this and is defined as:

$$\text{CPF} = 1 + \left(\sqrt{\frac{\text{Total No. of Tracks}}{\text{Number of Tracks Left}}} - 1 \right) \times \text{CF}_1 \tag{4.3}$$

Here, the 'Total Number of Tracks' refers to the theoretical routing capacity on the metal layer, while 'Tracks Left' corresponds to the remaining tracks after accounting for the ADC layout. A higher CPF indicates that the ADC occupies more routing resources, indirectly increasing the area and energy cost at the SoC level.

4.1.3 Embodied Carbon Footprint (eCFP)

The embodied carbon footprint (eCFP) quantifies the cumulative carbon emissions generated during the manufacturing of integrated circuits, accounting for all fabrication processes including photolithography, doping, etching, and thin-film deposition [16]. These semiconductor manufacturing steps represent significant energy-intensive operations that contribute substantially to a device's environmental impact prior to its operational deployment. The eCFP metric serves as a crucial sustainability indicator that designers can optimize during the IC development phase.

Four primary design factors influence the eCFP calculation. First, the physical layout area directly correlates with manufacturing emissions, as wafer processing costs scale proportionally with silicon surface coverage. Second, additional photomasks required for specialized features - such as multi-threshold voltage transistors or integrated capacitor structures like MIMCAPs and trench capacitors - introduce extra processing steps that increase the fabrication energy burden. Third, routing congestion caused by dense intellectual property (IP) blocks or excessive utilization of upper metal layers can inflate the overall system-on-chip (SoC) area, thereby amplifying emissions. Fourth, strategic introduction of porosity in certain designs facilitates inter-IP routing, potentially reducing congestion and minimizing the total area footprint.

The eCFP is mathematically modeled as:

$$\text{eCFP} = \underbrace{k}_{\substack{\text{Base energy} \\ \text{per } \mu m^2}} \times \text{Area} \times \underbrace{\text{Mask\_factor}}_{\substack{1+0.045\times \\ \text{\#extra masks}}} \times \underbrace{\text{Congestion\_factor}}_{1+\text{TR}\times 0.3} \tag{4.4}$$

In this formulation, k represents the base energy consumption per unit area (4204 kWh per 300mm wafer for 65nm technology [19]). The mask factor accounts for the 4.5% energy increase associated with each additional photomask required beyond the standard process flow. The congestion factor incorporates routing complexity through the track ratio (TR), defined as the proportion of used versus available routing tracks in the metal layers, with a 0.3 scaling coefficient reflecting the observed impact on manufacturing energy consumption.

This comprehensive model enables designers to evaluate and compare the environmental impact of different circuit implementations during the early design phases, facil-

itating sustainability-aware architectural choices without compromising traditional performance metrics. The quantitative approach aligns with industry efforts to reduce the semiconductor sector's carbon footprint while maintaining technological progress.

4.1.3.1 Operational Carbon Footprint (oCFP)

The Operational Carbon Footprint (oCFP) measures the environmental impact of an ADC design by accounting for energy consumed during its operational lifetime [20]. This includes contributions from dynamic, static, and leakage power over a defined total operating time. The oCFP is calculated as:

$$\text{oCFP} = (\text{DPQ} + \text{SPQ} + \text{LPQ}) \times T_{\text{op}} \tag{4.5}$$

where T_{op} is the assumed total operating time, taken as 20,000 hours over five years for IoT applications.

4.1.3.2 Dynamic Power Quantity (DPQ)

Dynamic energy is consumed when internal nodes in the SAR ADC transition due to logic switching, resulting in capacitive charging and discharging. The cumulative dynamic power quantity is given by:

$$\text{DPQ} = \sum \alpha V_{\text{op}} f_{\text{op}} Q_{\text{dyn}} \tag{4.6}$$

where α is the activity factor, V_{op} the operating voltage, f_{op} the clock frequency, and Q_{dyn} the total dynamic charge. For a pipelined SAR ADC, even though the clock frequency doubles (to match throughput), the DPQ increases by less than 2× due to localized switching and efficient stage-wise architecture [1].

4.1.3.3 Static Power Quantity (SPQ)

SPQ captures power consumed by internal biasing circuits while the ADC remains in a steady-state. It is estimated as:

$$\text{SPQ} = \sum I_{\text{bias}} \times V_{\text{bias}} \tag{4.7}$$

where I_{bias} is the bias current and V_{bias} is the corresponding bias voltage. In SAR ADCs, this typically includes currents for comparator biasing and reference generation circuits [4].

4.1.3.4 Leakage Power Quantity (LPQ)

Leakage power represents the standby and retention mode consumption of the SAR ADC. It is defined as:

$$\text{LPQ} = P_{\text{standby}} + P_{\text{active}} + P_{\text{retention}} \tag{4.8}$$

Leakage during active mode is:

$$P_{\text{active}} = I_{\text{active}} V_{\text{op}} \left(A_{\text{ART}} \cdot RPR\right) \tag{4.9}$$

where A_{ART} is the active area reference time and RPR is the Reference Performance Ratio calculated as:

$$RPR = \frac{T_{\text{design}}}{T_{\text{worst-case}}} \tag{4.10}$$

A higher RPR (faster execution) enables faster completion of ADC operation, thereby reducing leakage accumulation.

For SAR ADCs in IoT use-cases, operational time distribution is assumed as 1% active, 9% standby, 20% retention, and 70% powered-off. Leakage in powered-off mode is ignored.

The standby and retention power estimates are given by:

$$P_{\text{standby}} = I_{\text{standby}} V_{\text{op}} \left(SB_{\text{ART}} + (EN \cdot A_{\text{ART}} \cdot (1 - RPR)) \cdot K\right) \tag{4.11}$$

$$P_{\text{retention}} = I_{\text{ret}} V_{\text{ret}} \left(R_{\text{ART}} + (EN \cdot A_{\text{ART}} \cdot (1 - RPR)) \cdot K\right) \tag{4.12}$$

where EN is a flag indicating if Pulse Width Modulation (PWM) is used, and K is defined as:

$$K = \frac{SB_{\text{ART}}}{SB_{\text{ART}} + R_{\text{ART}}} \tag{4.13}$$

Use of low-leakage devices and aggressive power gating helps reduce LPQ and therefore lowers the operational carbon footprint [8].

4.1.4 ADC-Specific Sustainability Optimization

Analog-to-Digital Converters (ADCs) exhibit unique sustainability trade-offs:

4.1.4.1 Architectural Choices

Pipelined SAR ADCs reduce oCFP by 38% compared to conventional SAR ADCs at iso-throughput (250MHz vs 500MHz operation) [1]. So even though area increases by $2\times$, the net CFP decreases by 22%.

Capacitor Selection: MIMCAPs reduce area by 31% but require 2 extra masks [10] MOSCAPs eliminate mask overhead but increase area

For a 8-bit pipelined SAR ADC, MIMCAP implementation achieves 17% lower eCFP despite mask penalties.

4.1.4.2 Application-Driven Optimization

Table 4.1: ADC Sustainability Profiles

Application	T_{active} (%)	f_{op} (MHz)	Dominant CFP
IoT	5%	1–10	Leakage (82%)
Automotive	30%	50–100	Dynamic (67%)
HPC	70%	500+	Dynamic (89%)

4.1.5 Design Recommendations

- Prioritize pipelining for >100MSps applications [1]
- Use MIMCAPs when area reduction >15% [10]
- Enable retention modes for IoT ADCs ($V_{\text{ret}} = 0.8V$) [8]
- Optimize metal stack - M1-only layouts reduce congestion penalty [9]

This framework enables designers to make sustainability-conscious choices during early architectural exploration, potentially reducing total carbon footprint by 19–42% across different ADC implementations [17].

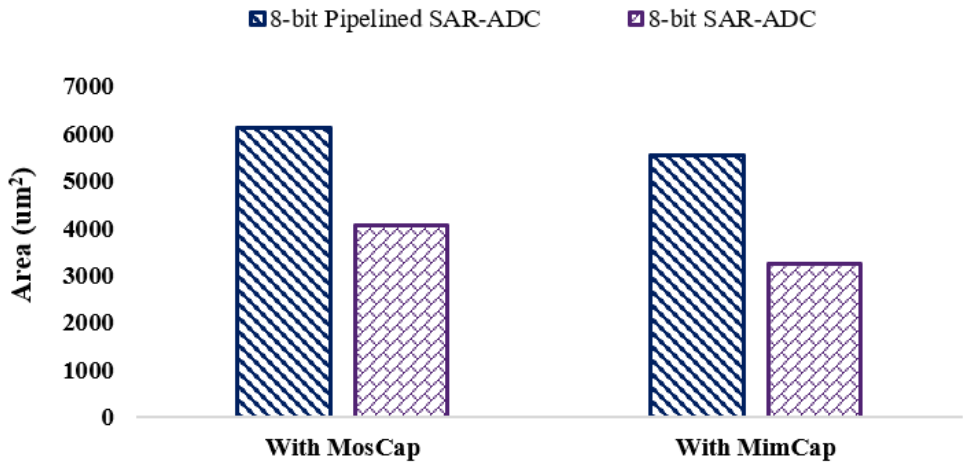

Figure 4.1: Area comparison of the 2 architectures

This data compares the silicon area of two ADC architectures—8-bit Pipelined SAR-ADC and 8-bit SAR-ADC—when implemented with MosCap and MimCap. The 8-bit Pipelined SAR-ADC occupies a larger area in both cases (6130µm² with MosCap and 5549µm² with MimCap), due to additional components like residue amplifiers and interstage circuitry that are essential for pipelining. In contrast, the 8-bit SAR-ADC, which avoids such complexity, requires significantly less area (4051µm² with MosCap and 3252µm² with MimCap). Using MimCap reduces area for both architectures owing to better capacitor density and layout efficiency. This highlights the trade-off between performance (pipelining) and physical design footprint.

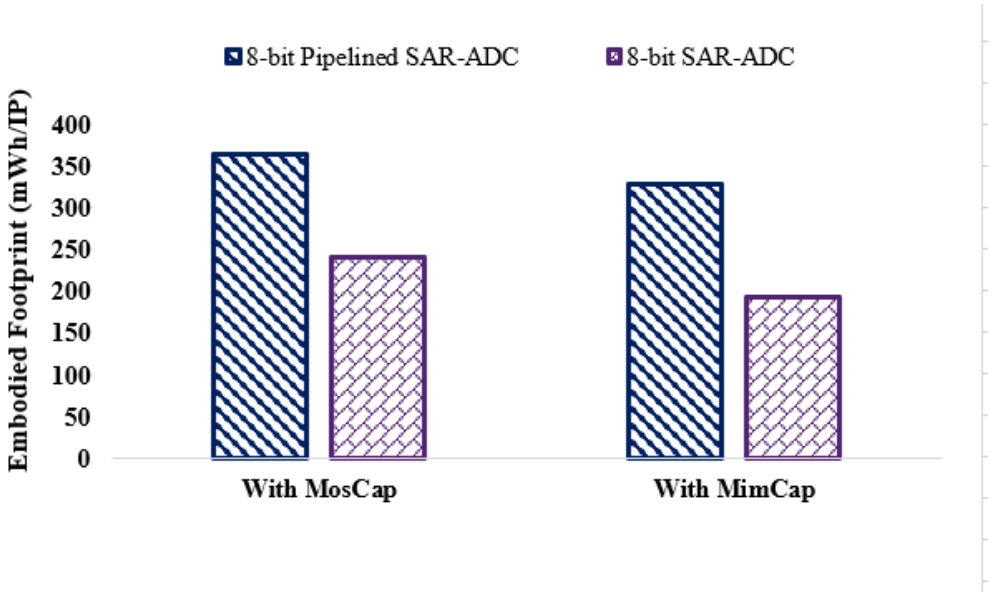

Figure 4.2: Embodied Footprint of the 2 architectures

This evaluates the embodied footprint for both ADCs based on capacitor type. The pipelined SAR-ADC has a higher embodied footprint in both cases—365mWh/IP with MosCap and 330mWh/IP with MimCap—compared to the SAR-ADC's 241mWh/IP and 194mWh/IP, respectively. This is due to the pipelined structure's increased transistor count, routing complexity, and metal layers. Switching from MosCap to MimCap reduces embodied energy in both architectures, reinforcing MimCap's fabrication efficiency.

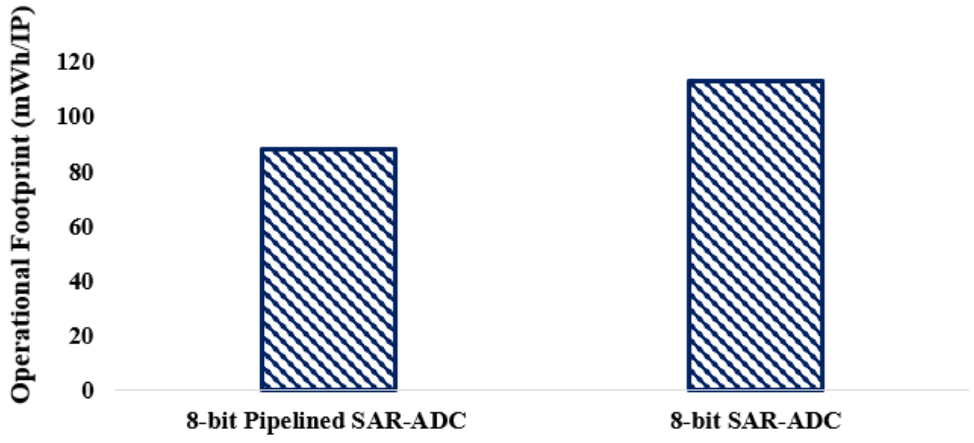

Figure 4.3: Operational Footprint of the 2 architectures

This is the illustration of the operational energy footprint of the two architectures, assuming an activity factor () of 0.2 for the pipelined SAR-ADC and 0.3 for the SAR-ADC. The 8-bit SAR-ADC demonstrates a higher operational footprint (113mWh/IP) compared to

the pipelined version (88mWh/IP), despite its simpler structure. This outcome reflects the SAR-ADC's longer conversion time and more frequent switching activity. The selected activity factors reflect realistic conditions, where the pipelined ADC performs more work per clock with better efficiency.

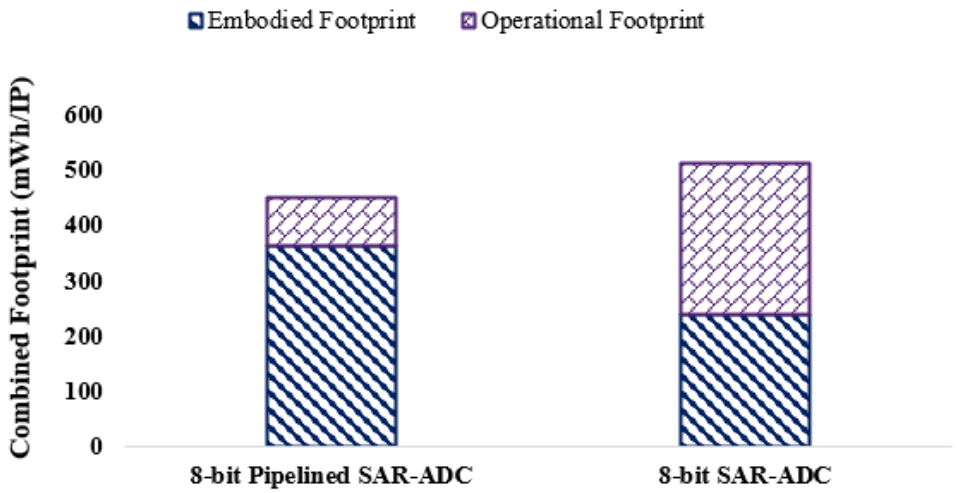

Figure 4.4: Combined Footprint of the 2 architectures

This graph represents the combined environmental footprint, accounting for both embodied and operational energy consumption. The 8-bit Pipelined SAR-ADC shows a total footprint of 453mWh/IP (365 embodied + 88 operational), whereas the 8-bit SAR-ADC reaches 514mWh/IP (241 embodied + 273 operational). These values reflect adjusted activity factors (= 0.2 for pipelined and = 0.3 for SAR-ADC) to match realistic switching behavior. While the pipelined version incurs a higher embodied cost due to its complexity, its lower operational footprint makes it more sustainable in long-running applications.

The combined footprint for the two ADC architectures shows that the Pipelined SAR ADC has almost double the eCFP of non-pipelined architecture. To estimate the oCFP, equal throughput case is considered. So even though pipelined architecture has more area, it has smaller total CFP.

CHAPTER 5

Conclusion

This thesis evaluated two SAR ADC architectures—an 8-bit SAR ADC and an 8-bit pipelined SAR ADC—through a sustainability lens using the PPAS framework. The 8-bit SAR ADC demonstrated lower area and embodied carbon footprint (eCFP), making it suitable for low-power, space-constrained applications like IoT. However, its higher operational carbon footprint (oCFP) due to slower conversion and higher switching activity limits its sustainability in high-throughput use cases.

In contrast, the 8-bit pipelined SAR ADC, despite a larger area and slightly higher eCFP, achieves lower oCFP by operating more efficiently at reduced clock frequencies. Overall, it delivers an 11% lower total carbon footprint at iso-throughput. This work highlights how architectural choices can align performance with environmental goals, enabling context-aware ADC selection that supports long-term sustainability in VLSI design.

In reference to the thesis Our research paper, titled "Framework to Estimate and Benchmark Sustainability of Circuit Design" has been accepted for presentation at IEEE Region 10 Symposium 2025 (TENSYMP2025).

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