Power Network Analysis Using Frequency Domain Approach

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STUDENT'S DECLARATION

I declare that the dissertation titled "Power Network Analysis using Frequency Domain Approach" submitted by Abhishek Jain for the partial fulfilment of the requirements for the degree of Master of Technology in VLSI and Embedded System is carried out by me under the guidance and supervision of Dr. M. S. Hashmi at Indraprastha Institute of Information Technology, Delhi and Mr Nitin Bansal at STMicroelectronics, Greater Noida. Due acknowledgements have been given in the report to all material used. This work has not been submitted anywhere else for the reward of any other degree.

..... Place and Date: .....
Abhishek Jain

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

.....
Dr. Mohammad. S. Hashmi

ABSTRACT

With reduction in size and shrinking in geometry, we have reached a point in time in which we no more can draw a direct correlation of the performance of the IC design with respect to the number of transistors on a single chip. The advancement in Electronic Design Automation and VLSI design technologies enables the circuits with increasingly higher speed to be integrated at low voltages and high densities. However this trend causes correspondingly larger voltage fluctuations in power distribution networks due to higher voltage drops such as IR-drop, L di/dt noise and LC resonance. Due to limited available silicon area and increasing clock frequencies, packaging issues and system-level performance issues such as crosstalk and Electromagnetic interference are becoming increasingly significant. Rapidly switching currents due to coupling from adjacent block's cause temporal and spatial fluctuations in the supply voltage which may cause functional failures in a design, degrading circuit performance and hence creating reliability concerns.

This dissertation addresses methodology for deciding sharing of power supplies among analog blocks (switching and non-switching blocks) taken into account the degradation of the various parameters of the s and noise due to coupling. In comparison to time domain , frequency domain characterization provides more information, simpler and are faster to perform so the analysis are done in frequency domain and results obtained are validated in time domain. Moreover a method has been proposed to predict power supply noise without actual simulation of the integrated environment by using the concept of impedance model leads to the saving of disk space and time.

ACKNOWLEDGEMENT

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1. INTRODUCTION

This dissertation deals in framing a methodology to replace the present transient analysis simulation for deciding to share a power supply among switching and non-switching analog s. It is about developing accurate, numerically robust, and computationally efficient frequency domain-based approach for computing the power supply noise (PSN). This dissertation gives the approach to predict the supply noise for a block without simulating the actual block but by utilizing the concept of Scattering(S) Parameter. This thesis discusses the concepts of propagation of noise in Power Delivery Network (PDN) such as LC resonance, Ldi/dt effect and IR drop. Transient analysis of nonlinear analog circuits is the most computationally intensive analysis and occupies the larger disk space and it needs more simulation time. The frequency domain based approach explores the concept of ohm's law in computing the noise in the supply voltage.

1.1 FREQUENCY DOMAIN

1.1.1 Frequency Domain Approach

The AC analyses are a family of frequency-domain approach that includes AC analysis, transfer function analysis, S parameter (S) analyses, and noise analysis. All of these analyses are based on the same mathematical technique of phasor analysis. Phasor analysis calculates the small signal sinusoidal steady-state response of the circuit [8]. This states that the solutions computed by the AC analysis contains only sinusoids present at the same frequency as the input signal. AC analysis is the small-signal behavior of a circuit and is computed by first linearizing the circuit about a DC operating point. Since the AC analyses operate on a linear time-invariant representation, the results computed by the AC analyses cannot include the effects normally associated with nonlinear and time-varying blocks [7]. Moreover S-parameter analysis is used to create an S-parameter model of the blocks is also based on frequency domain. This analysis is most commonly used in high-frequency (switching blocks) analog circuits.

1.1.2 Why Frequency domain?

Frequency domain is utilized in proposed approach as characterization of PDN is simpler as compare to time domain. The information from PDN impedance measurement can be easily interpreted in frequency domain. Moreover it is faster and requires lesser memory space. Another reason for using frequency-domain measurements in the characterization process instead of time domain is that external random noise can be suppressed more readily from the environment in the frequency

domain [5]. Time-domain digital instruments will have fewer bits in quantization of analog signals leading to the increase in the error and limits the achievable dynamic range in comparison to narrowband frequency domain. In order to study simultaneous switching output buffers (SSO) noise and electromagnetic interference, total PDN impedance which consisted of on-chip block PDN, package PDN, and board PDN has become more important to study from the frequency domain point of view .

The adopted approach for validating on-die PDN or power and ground network routing inadequacies using static simulations is very inefficient, as this technique only models the IR drop (DC) component of the PDN and does not capture the capacitive and inductive effects that is now increasingly dominate the noise or voltage drop seen in the chip with the increase in frequency. This noise or voltage drop comes from a combination of several factors such as simultaneous switching of several devices, Ldi/dt, chip-package resonance, and insufficient decoupling capacitance [6]. None of these effects are modeled by the DC or static simulation based approaches.

1.2 Power Supply noise

1.2.1 Need for simulating power supply noise:

Power is supplied to integrated circuits(IC’s) in chip (die) from the voltage regulator module (VRM) in the printed circuit board (PCB) through stages of the power distribution network (PDN) (or the power supply network). As the VRM is far away from the actual switching circuits, inductance provided by PDN can be large. Moreover this network is usually made up of copper as a result the PDN also has nonzero resistance. The nonzero parasites of the PDN causes the supply voltage observed at the terminals of switching circuits to be different than the voltage that was supplied by the VRM[2]. Specially, because of the PDN's nonzero resistance, the supply voltage across the circuit's supply terminals is less than what is supplied by the VRM due to IR drop and other losses. The magnitude of this difference depends directly on the resistance of the PDN. Because of the PDN's nonzero inductance, the supply voltage seen at a circuit fluctuates with time (see Figure 1). This temporal voltage fluctuation is a direct consequence of Faraday's law. The difference between the voltage supplied by the VRM and the voltage actually received by the circuits is referred to as the power-supply noise (PSN)[4]. This noise is also known as the switching noise or the simultaneous switching noise (SSN).

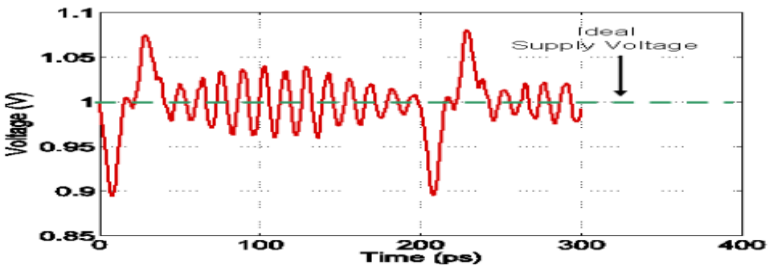


Figure 1 variation of supply voltage[2]

1.2.2 Undesirable effect of PSN:

The PSN can degrade the performance of the by affecting the timing of the clock signals or affect the functionality of the by causing logic failures [4] in switching circuits. It is estimated that a little fluctuation in the supply voltage leads to severe timing uncertainty. Since the PDN is always going to be non-ideal, PSN cannot be eliminated completely, though it can only be controlled. Unfortunately, ensuring that the PSN stays within 10% of the actual supply voltage is becoming tougher with the scaling of transistor. This means that there are going to be more circuits that are going to switch simultaneously. As the device sizes have shrunk to accommodate faster transistors, the switching speed is increasing with scaling.

To maintain a constant electric field in gates of transistors, the supply voltage is reduced. This reduction in supply voltage means that the absolute magnitude of PSN has to get smaller with scaling. It is described in [11] that with a constant field scaling, the signal to noise ratio as a result of di/dt noise scales as $1/S^4$ when scaling the process by $1/S^1$. With scaling, the total current needed also increases. As the interconnect resistance increases with scaling, the product IR drop increases with scaling[10].

1.3 MOTIVATION:

The main motivation for framing a methodology for analyzing the power supply noise is to save time, cost and area. The noise analysis tools from CWS and apache are very expensive and take several days for simulations. Noise analysis approach provided in this research will consider the effect of noise due to shared power supply on individual block. The drawbacks of individual power supplies to each block's include performance degradation due to IR-drop and L di/dt noise and larger board area. Moreover, more number of inputs output pins will be required for power supply that leads to greater parasites in a system on chip (SoC). Individual packages and pads are required for independent power supply system results in a greater area. The shared power supply system saves

on power pins at top level thus leads to reduction in area and cost. As power supply noise is aperiodic in nature FFT tool is computed to convert from time to Freq domain.

1.4 THESIS ORGANIZATION

The chapter organization of the thesis is in the following manner. Chapter 2 deals with Power Distribution Network (PDN) that provides the insight into variation in voltage supply from voltage regulator module to the actual circuit. It provides information about the signal integrity issues like crosstalk and EMI (electromagnetic interference) and various noises in PDN. Chapter 3 discusses about the various terms involved in noise analysis and provides the detailed explanation. It also deals with various power management units like Bandgap and LDO (low drop regulator) high switching blocks like ring oscillator, on which analysis are carried out. Then the organization moves to Chapter 4 that has proposed a methodology to replace the present transient analysis using frequency domain approach. Moreover it also focuses on predicting the power supply noise using a novel approach in frequency domain. The S-parameter (Z-Model) based approach has also been introduced in proposed work chapter. Chapter 5 discusses the result showing the accuracy of the proposed methodologies of supply sharing in terms of peak to peak supply variation. The approach to prediction of power supply noise has also been validated with usual practice of time domain based analysis. Finally Chapter 6 concludes the thesis and discusses the future work.

2 POWER DISTRIBUTION (DELIVERY) NETWORK (PDN)

The power supply for the individual blocks (module) is passed from the board to the die through package as shown in figure 2 of the PDN. The chip package provides a mechanical and electrical connection between the chip and a circuit board. Packages are important component of electronics systems as it connects signals and power between the chip and board with little delay or distortion and provides the physical support. Package provides means for heat removal and protects BLOCK's from thermal stress and mechanical damage. Package type includes the Dual inline package (DBLOCK), Pin grid array, Ball grid array and flip chip etc. where Ball grid array are used for high bandwidth signals. The major difference between flip chip and ball grid is that bumps are present directly on package and no wire of gold is required in flip chip, thereby reducing economic [1]. Package metrics includes cost, size, heat removal rate, number of input output, reliability and ease of testing.

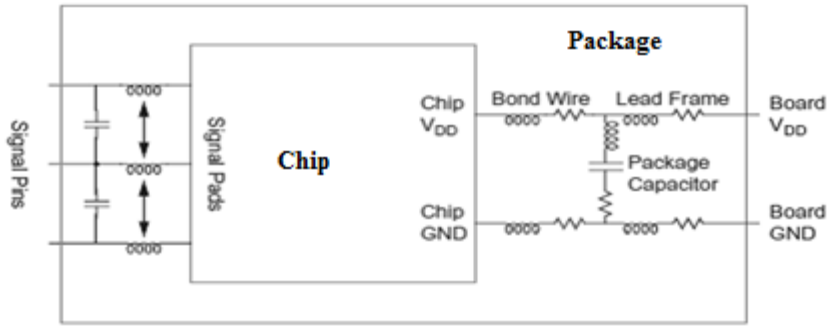


Figure 2 Package Parasitic[1]

The power distribution or delivery network (PDN) consists of all the interconnects from the voltage regulator module (VRM) to the pads on the chip and the metal on the die that distributes power and return current. It also includes bypass capacitors to supply the instantaneous current requirements of the system. The Power distribution network in a chip consists of chip level plane with thin-oxide decoupling capacitors, the package level power planes and mid frequency decoupling capacitors and board level power planes, low-frequency decoupling capacitors and voltage regulator module. The proximity of capacitor to the switching circuit determines the time required to supply the voltage. The voltage regulator main function is to produce a constant output voltage independent of the load current, though a maximum load is specified for regulator. It is modelled as an ideal voltage source in series with a small resistance and the inductance of its pins. Near the regulator is a large bulk capacitor to compensate for the variation in power supply. The external capacitors are modelled as an ideal capacitor with an effective series resistance (ESR) and

effective series inductance (ESL). The primary difference between the PDN and signal paths is that there is just one net for each voltage rail in the PDN. It can be a very large net that can physically span the entire board and have many components attached.

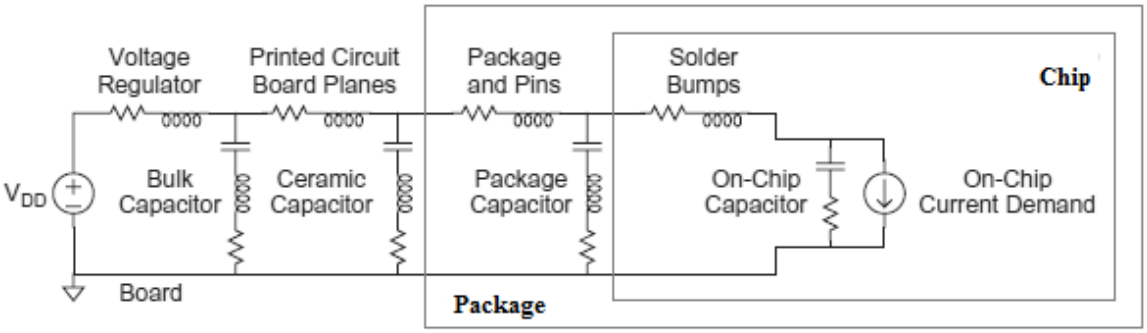


Figure 3 PDN[1]

2.1 Purpose of PDN:

The basic requirements for PDN that designers need to consider and meet, either by simulations or by measurements are:

- Deliver sufficiently clean supply voltage to the ICs;
- Provides average and peak power demands
- Provides current return paths for signals
- Avoids wear out from electromigration and self-heating
- Consumes little chip area and wiring
- Easy to lay out

The PDN of electronic circuits has to provide the chip with clean power. The switching circuitry in digital logic and the input-level and activity-dependent power in analog circuits create current transients, which across the PDN impedance generate voltage fluctuations. The voltage fluctuations (i.e. transient noise) must be kept below a predefined limit so that it does not interfere with the analog or digital signalling.

2.2 Problem due to non-ideal PDN:

First and primary objective is to keep a constant supply voltage on the pads of the chip, and keep it within a narrow tolerance band, typically on the order of 5%. This voltage has to be stable, within the voltage limits, from DC up to the bandwidth of the switching current. The main problem in designing PDN is that we have the voltage fluctuation over the range of frequency.

Secondly, in most designs, the same PDN interconnects that are used to transport the power supply are also used to carry the return currents for signal lines. These interconnects must provide a low impedance return path for the signals. The easiest way of doing this is by making the interconnects wide, so that the return currents can spread out as much as they want, and by keeping the signal traces physically separated so that the return currents do not overlap[3]. If these conditions are not met, the return currents from different signals overlap and this leads to noise at the supply voltage.

Finally, since the PDN interconnects are usually the largest conducting structures in a board, carrying the highest currents, and sometimes carry high frequency noise, they have the potential of creating the radiated emissions and causing failure of an EMC certification test. When PDN is designed effectively, the PDN interconnects can mitigate many potential EMI problems and help prevent EMC certification test failures.

2.3 CAUSES OF VARIATION:

IC's cares about the voltage on its pads. If there were no current flow in the PDN interconnects from the regulator module to the chip pads, there would be no voltage drop in this path and the constant regulator voltage (fixed DC) would appear as a constant supply voltage on the chip pads. If there were a constant DC current drawn by the chip, this DC current would cause a voltage drop in the PDN interconnects due to the series resistance of the interconnects. This is commonly referred to as the IR drop. As the current from the chip fluctuates, the voltage drop in the PDN would fluctuate and the voltage on the chip pads would fluctuate.

Consider, not just the resistive impedance of the PDN, but also the complex impedance, including the inductive and capacitive components of the PDN interconnects. The impedance of the PDN, as seen by the pads of the chip is impedance verses frequency, Z(f).

As fluctuating currents with frequency spectrum, I(f) flows through the complex impedance of the PDN, there will be a voltage drop in the PDN that is given by:

$$\boldsymbol{V(f) = I(f) * Z(f)}$$

Where:

V(f) = voltage amplitude

I(f) = current spectrum drawn by the IC

Z(f) = impedance profile of the PDN seen by the chip pads.

This voltage drop in the PDN (V_{pdn}) causes the constant voltage of the regulator as seen by the chip to be varying. In order to keep the voltage drop on the chip pads less than the tolerance noise voltage , usually referred to as the ripple(V_{ripple}), given the chip current fluctuations, the impedance of the PDN needs to be below some maximum allowable value. This is referred to as the target impedance (Z_{target})

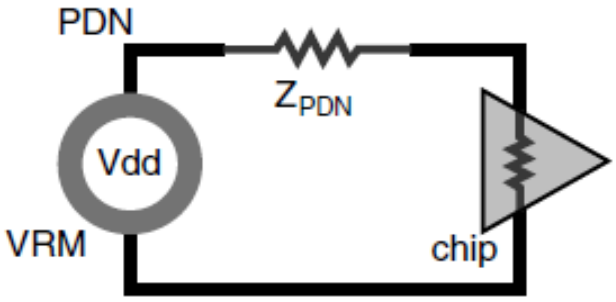


Figure 4 Connections from the VRM to chip [4]

$$\boldsymbol{Vripple > Vpdn = I(f) \times Zpdn(f)}$$

$$\boldsymbol{Ztarget = Zpdn(f) < \frac{Vripple(f)}{I(f)}}$$

Where:

V_{ripple} = tolerance noise voltage for the chip, in Volts

V_{pdn} = noise drop across the PDN interconnects, in Volts

I(f) = current spectrum drawn by the chip, in Amps

$Z_{pdn}(f)$ = impedance profile of the PDN as seen by the chip pads, in Ohms

Z_{target} = maximum allowable impedance of the PDN, in Ohms

If we want to keep the voltage stable across the pads of the chip, given the chip's current fluctuations, it means keeping the impedance of the PDN below a target value from DC to high frequency. This is the fundamental guiding principle in the design of the PDN.

2.4 Target Impedance

The most important step in designing the PDN is to establish the target impedance. This must be done separately and independently for each power supply to all the chip on the board as some designs

may use many different voltages. For each design, the target impedance may vary with frequency due to the specific current spectrum of the chip.

Consider the case when the current profile from the chip on one rail is a sine wave, with a peak to peak value of 1 A. The amplitude of the sine wave of chip current will be 0.5 A. This current from the chip is shown in both the time domain and the frequency domain in Figure5.

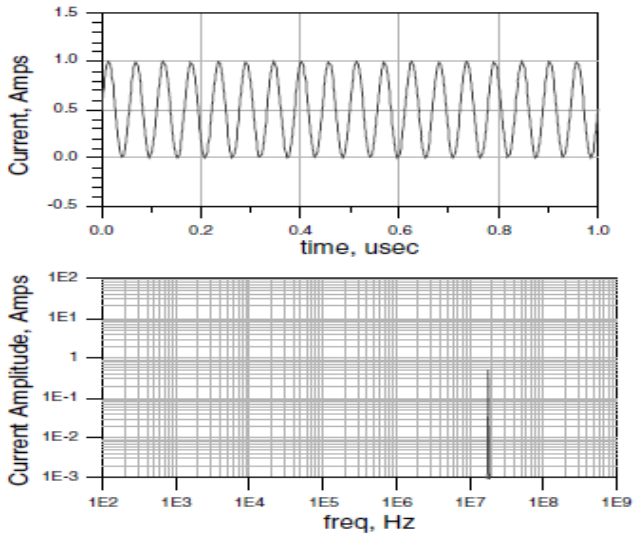


Figure 5 Chip current in Time and Freq domain[3]

When this current spectrum flows through the specific impedance profile of the PDN, a voltage noise will be generated in the PDN. An example of an impedance profile with the frequency component of the current, and the resulting time domain voltage noise across the IC has been shown in figure6. When the sine wave current passes through an impedance that is too large, the voltage generated is above the ripple voltage specification(spec), which is typically +/– 5%, shown as the reference lines. Moreover at the resonance frequency of impedance profile the voltage fluctuation is far beyond the ripple spec.

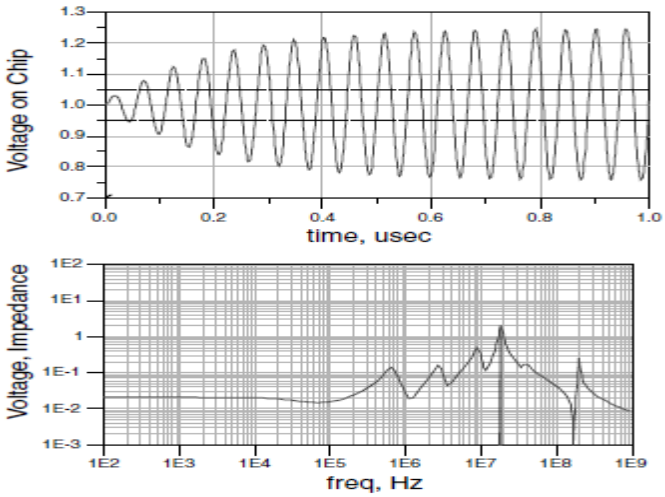


Figure 6 Impedance Profile with voltage in Time domain[3]

Generally in most cases, it is not the peak current but the maximum transient current that interacts with the higher frequencies of the PDN. If there is a steady state DC current draw from the chip, the VRM can usually compensate to keep the rail voltage close to the specified voltage value. It's when the current changes from the DC value, either increasing or decreasing, at frequencies above the response frequency of the VRM that the current will interact with the PDN impedance.

The maximum impedance for the PDN called as the target impedance, is established based on the highest impedance that will create a voltage drop still below the acceptable ripple spec. This is given by

$$Zpdn * I_{transient} = V_{noise} < Vdd * ripple\%$$

Or

$$\boldsymbol{Z_{target} < \frac{Vdd * ripple\%}{I_{transient}}}$$

Where:

Vdd = supply voltage for a specific rail

$I_{Transient}$ = worst case maximum transient current

Z_{PDN} = impedance of the PDN at some frequency

Z_{target} = target impedance, the maximum allowable impedance of the PDN

V_{noise} = worst case noise on the PDN

Ripple% = the ripple allowed, generally assumed to be +/– 10%

If the PDN impedance is kept below the target impedance at each frequency, the worst case voltage noise generated across it as the worst case, maximum transient current flows through it will be less than the ripple spec. If the PDN impedance is much below the target impedance, it suggests that the PDN was overdesigned and it will leads to unnecessary more cost. Whenever possible, the peak transient current should be used in estimating the target impedance. When the peak transient current is not available, it can be roughly estimated from the maximum current draw or from the power consumption of the chip.

2.5 NOISE IN PDN

The various noises in PDN includes IR drop, Ldi/dt and LC Resonance

2.5.1 IR Drop

The resistance of the power supply network includes the resistance of the on-chip wires, the resistance of the solder bumps to the package, the resistance of the package planes or traces, and the resistance of the printed circuit board plane. Due to resistance of the power supply network when large current flows unacceptable voltage drop occurs that causes timing uncertainty and slew rate down. As technology scales by 1/s causes chip current increases by s^3.There are 2 kinds of IR drop: Static IR drop and Dynamic IR drop. Static IR drop is the voltage drop between Vdd and ground based on the average power or current. It can be corrected by increasing the width of wires and decreasing their pitch. Dynamic IR drop refers to voltage drop due to current flowing when the circuit is switching i.e. performing some function. It is the RC transient behaviour while Static IR drop is steady state drop[20]. Dynamic IR drops are corrected by both wire sizing and inserting decaps.

2.5.2 Ldi/dt Noise

The inductance of the power supply is typically dominated by the inductance of the bond wires or solders bumps connected to the package. A sudden change of the current flowing through a wire will induce abrupt voltage changes on that wire and its neighbouring wires due to inductance. If these wires are part of the on-chip Power-Ground network, the induced voltage fluctuation is called L di/dt noise (often called Delta-I noise).

$$\frac{di}{dt} = \frac{I}{\delta} = \frac{P * f_c}{Vdd}$$

P is constantly increasing due to denser circuits, fc is increasing and Vdd is decreasing

So $\frac{di}{dt}$ is constantly increasing. $\frac{L*di}{dt}$ is present only at high frequency. It can be localized as $\frac{L*di}{dt}$can be confined in an area by inserting sufficient decoupling capacitors.

2.5.3 LC Resonance

It impacts a circuit even when operating at low frequency. As the transient oscillating term takes time to diminish, another current is injected during that duration then oscillating term takes more time to diminish[20]. When this process repeats circuit resonates at resonant frequency. It travels through the whole as LC resonance drop frequency is low, onchip decap are not effective to stop wave propagation. LC resonance can be corrected by increase in L so that resonance frequency changes. Moreover increase the damping by connecting series resistors at decap. Some advanced package technology can be used as a possible remedy for LC resonance.

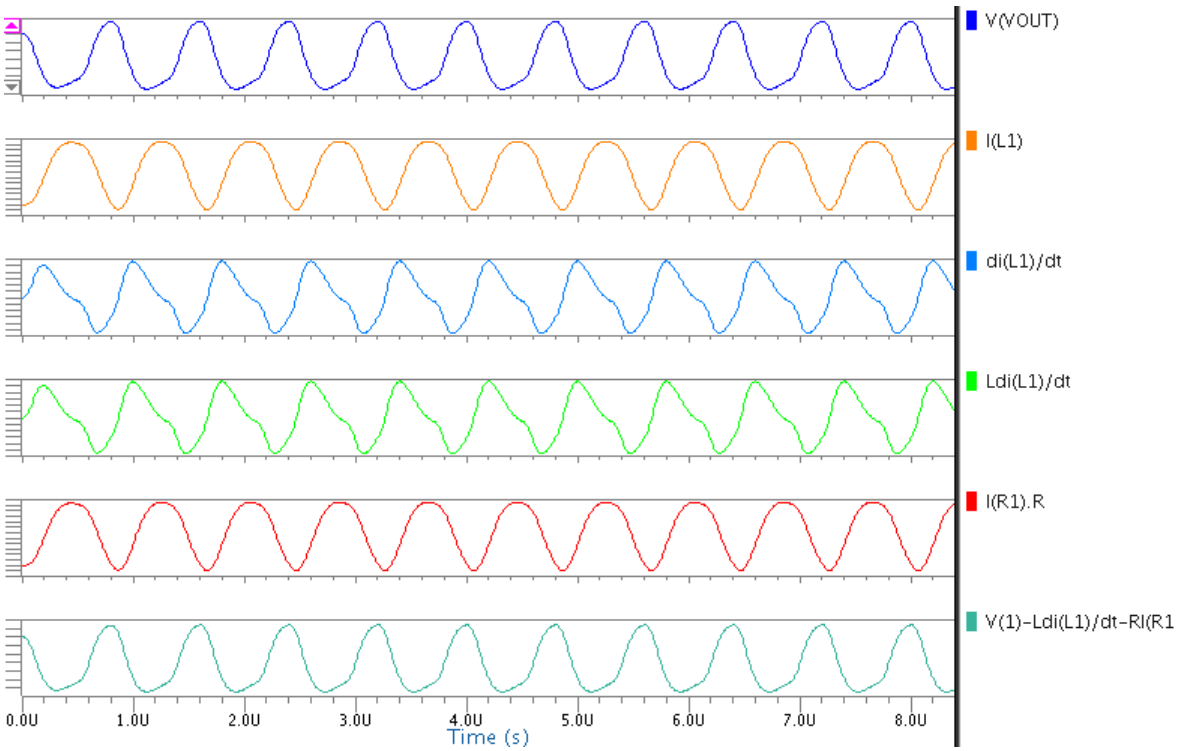


Figure 7 Showing Different Noise In PDN

3. TERMS AND S USED FOR ANALYSIS

3.1 POWER SUPPLY REJECTION RATIO:

3.1.1 Definition:

Power supply ripple rejection ratio (PSRR) is a measure of how well a circuit rejects ripple coming from the input power supply at various frequencies. The PSRR describes how a signal on the DC input voltage of the regulator system is transmitted to the regulated output. This specification is the measure of how well the regulator rejects an AC signal riding on a nominal input DC voltage. The PSRR is generally measured in dB and defined as:

$$\boldsymbol{PSRR = \frac{20Log\ Vout}{Vin}}$$

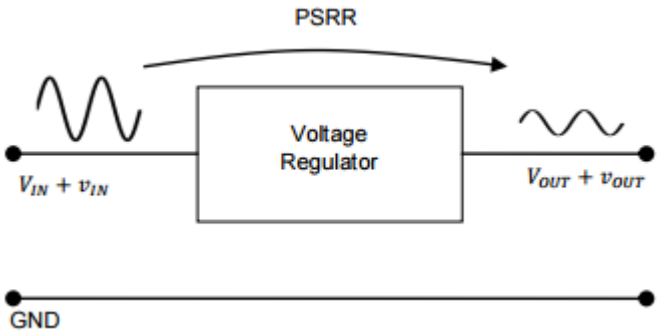


Figure 8 PSRR measurement

Depending on the definition the PSRR can be a negative or positive number. Using the above definition, the PSRR generally is a negative number. PSRR is the amount of noise from a power supply that a particular device can reject. If a supply of device changes due to noise ideally its output should be independent of variation. If a change of 'A' volts in a supply produces output voltage change of 'B' volts than the PSRR on that supply is B/A. PSRR is at a maximum at low frequencies, and begins to fall at higher frequencies depending upon the regulator design. Another parameter that is closely related to PSRR is line transient response. PSRR is specified at specific frequencies, whereas a line transient essentially contains all frequencies. However, the primary difference is that PSRR is based on small signals, whereas line transients are large signals and thus theoretically much more complicated in nature.

3.1.2 Measurement Setup of PSRR:

For PSRR simulation, superimpose an AC signal source having an amplitude of 1 on the power source (ac source in series with power source), then perform AC analysis, plot the Vout (the amplitude of the output of the device).This output in dB gives the PSRR.

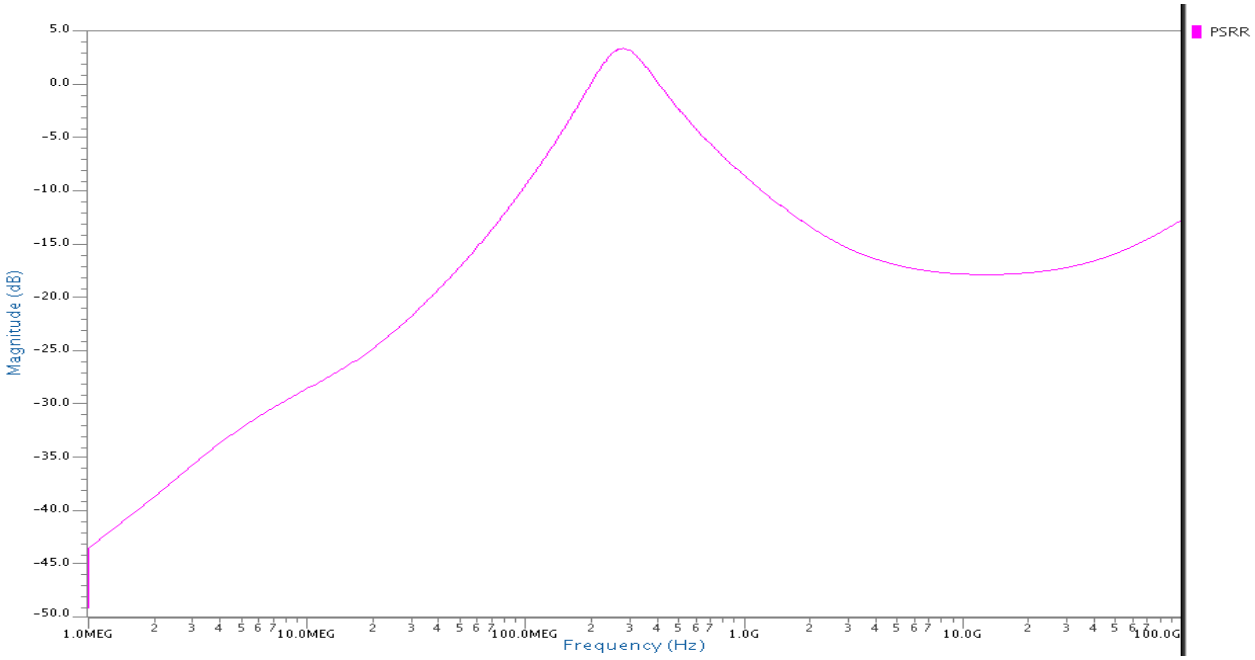


Figure 9 PSRR of LDO

3.2 Antiresonance:

It causes undesirable rise in impedance of PDN. For components of unequal values, the smooth resonance is disturbed due to existence of additional poles and zeroes. With 2 poles, 2 Resonance frequencies are obtained f1 and f2 and due to existence of zero a peak is obtained between f1 and f2.Occurenece of such peaks is called anti resonance effects. Antiresonance occurs, whenever some of the parallel connected impedance are inductive and capacitive.

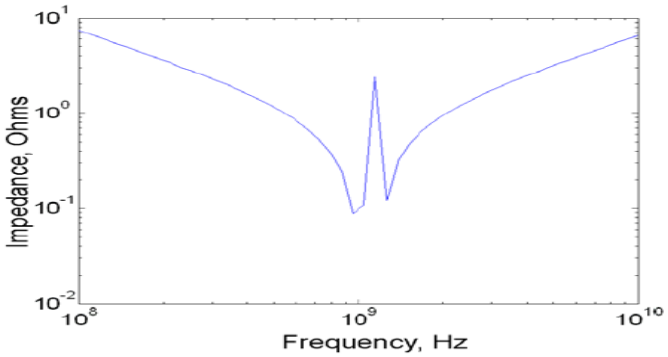


Figure 10 Antiresonance effect[13]

To cancel antiresonance effect, a small decap is placed in parallel that shifts the antiresonance spikes to a higher value. Another technique is to decrease the effective series inductance (ESL). By decreasing ESL, shifts poles to a higher frequency. By decreasing ESL, Quality factor (Q) of the system is decreased. The peaks become wider in frequency and lower in magnitude. Moreover, decrease in decap values shifts the antiresonance peak to higher frequency. Increase in effective series resistance (ESR) broadens the frequency range of anti-resonant spikes, ensuring that the amplitude of output impedance remains below the target impedance. It becomes obvious that in order to reduce the no of antiresonance peaks we need to minimize the no of different value caps used in PDN.

3.3 S-PARAMETER:

S (scattering) parameters are used to characterize electrical networks using matched impedances. S-Parameters allow a device to be treated as a "black box" with inputs and resulting outputs, making it possible to model a system without having to deal with the complex details of its actual internal structure. This property of S-Parameter has been exploited in our methodology.

As in the present world the bandwidth of operation of chip is increasing, it is important to characterize chip's performance over wide frequency ranges. Traditional low-frequency parameters such as resistance, capacitance, and gain can be dependent on frequency, and thus may not fully describe the performance of the IC at the frequency under consideration. In addition, it may not be possible to characterize every parameter of a complex IC over wide frequency range, so system-level characterization using S-parameters may provide better data. But still, to characterize a over a wide band of frequencies, we may use the impedance matrix.

3.3.1 Reasons for using Impedance Matrix (Z-Model)

The first reason for using Z-Model is that a well-designed PDN should approximate a voltage source because the noise currents should create only small voltage fluctuations on top of the dc voltage. The electronics injecting the noise at the ports can then be approximated as current sources or open terminations. The second reason is to obtain the S-matrix, we have to obtain the appropriate S-parameters by matched termination on all ports. This is not only inconvenient in case when the PDN has a large number of ports, but also creates the problem that the characterization has to be repeated each time when we change the port assignment (i.e., if we add ports or change their locations). This problem is not present in the case when we use the Z-matrix; since the Z-matrix requires open

terminations (or "nothing") at the ports, reassigning or adding ports does not require a recalculation other than obtaining the matrix elements for the newly added ports.

3.3.2 S-Parameter Definitions:

The representation of a signal wave in a two-port electrical-element is given as:

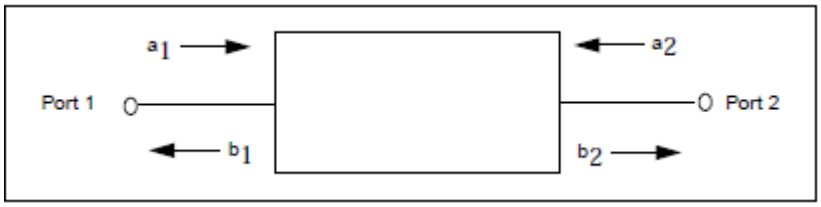


Figure 11 2 –Port Network

Where:

a_1 is the wave into port 1

b_1 is the wave out of port 1

a_2 is the wave into port 2

b_2 is the wave out of port 2

The relation between a_i and b_i (i = 1,2) can be written as a system of 2 linear equations (a_i being the independent variable, b_i the dependent variable)

$$\boldsymbol{b_1 = a_1 S_{11} + a_2 S_{12}}$$
$$\boldsymbol{b_2 = a_1 S_{21} + a_2 S_{22}}$$

Where $\boldsymbol{s_{11}}$ is the port-1 reflection coefficient*:* $s_{11} = \frac{b1}{a_1}, a_2 = 0$

$\boldsymbol{s_{22}}$ is the port-2 reflection coefficient: $s_{22} = \frac{b2}{a_2}, a_1 = 0$

$\boldsymbol{s_{21}}$ is the forward transmission coefficient: $s_{21} = \frac{b2}{a_1}, a_2 = 0$

$\boldsymbol{s_{12}}$ is the reverse transmission coefficient: $s_{12} = \frac{b1}{a_2}, a_1 = 0$

3.3.3 S-Parameter Simulation Description

S-parameters are used to represent the signal-wave response of an n-port electrical element at a given frequency. S-parameter simulation is a sort of small-signal AC phasor simulation. It is most commonly used to characterize passive RF components and establish the small-signal characteristics of a device at a specific bias voltage, time and temperature. If the circuit contains any nonlinear devices, a DC simulation is performed first and after the DC simulation; the simulator linearizes all nonlinear devices about their bias points. A linearized model is used to measure the small incremental changes of current due to small incremental changes of voltage. These are the differentials of the transistor model equations, which are evaluated at the DC bias point. Nonlinear resistors and current sources are replaced by linear resistors whose values are set by the small signal conductance dI/dV[3]. For this Methodology S-parameters are computed while considering supply source and ground as 2 ports of any switching block. The impedance of all other terminals are computed with respect to these 2 ports. Current sources that depend on voltages other than the voltage across the source are replaced by linear dependent current sources dI1/dV2. Nonlinear capacitors are replaced by linear capacitors of value dQ/dV. The linear circuit that results is analyzed as a multiport device. Each port is excited in sequence, a linear small-signal simulation is performed, and the response is measured at all ports in the circuit. That response is then converted into S-parameter data, which are in turn sent to the dataset. S-parameter simulation normally considers only the source frequency in a noise analysis.

3.4 ANALOG BLOCKS USED FOR ANALYSIS:

3.4.1 Low Drop Out (LDO) Regulators:

A LDO is a regulator circuit that provides a well specified and well defined stable DC voltage whose input to output voltage difference is low. Dropout voltage is the minimum input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage and this point occurs when the input voltage approaches the output voltage. The main features of the LDO used for satisfying the proposed approach are low power, low noise and high power supply rejection ratio (PSR) over the wide frequency spectrum.

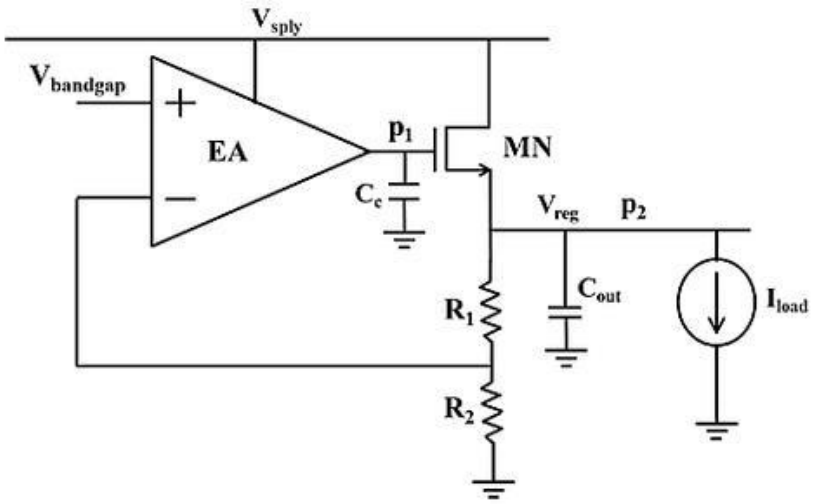


Figure 12 Basic LDO Diagram[17]

A series topology is used to regulate the supply voltage (V_{sply}), where the error amplifier is supplied by the regulated voltage using negative feedback phenomenon instead of (V_{sply}), because it provides better immunity to power supply fluctuations. The regulated voltage is then scaled, sampled and compared to a reference voltage ($V_{bandgap}$) obtained from a bandgap reference core. The error amplifier is a basic single-ended differential pair with an active load followed by the common-drain output stage for proper impedance matching and in addition it generates an output current depending on the difference between the differential inputs [16]. The negative feedback loop formed by the error amplifier and the sampling circuit (R1 and R2) ensures that the regulated voltage is maintained at the desired level. To ensure the stability of LDO, loop gain is so adjusted to maintain the negative feedback as positive feedback contributes to oscillations and thus instability.

LDO operation can be better understood using the NMOS as pass element in series (though PMOS pass element is mostly preferred). In the linear region, the series pass element acts like a series resistor. In the saturation region, mosfet becomes a voltage-controlled current source[19]. Voltage regulators usually operate in the saturation region where the series pass element acts like a constant current source as the function of gate-to-source voltage (Vgs). Under varying load conditions, Vgs controls the LDO regulator to provide the required output load.

Figure13 illustrates the LDO operation in the saturation region. When load current increases from Id2 to Id3, the operating point moves from Po to P2, and the input-to-output differential voltage, is given by Vds

$$\boldsymbol{Vds = Vi - Vo}$$

From figure13 it has been deduced that, as the input voltage decreases, the voltage regulator pushes the operating point toward P1 (toward the dropout region). As the input voltage approaches the output voltage, a critical point exists at which the voltage regulator cannot maintain a regulated output The point at which the LDO circuit begins to lose loop control is called the dropout voltage. Below the dropout voltage, the LDO regulator can no longer regulate the output.

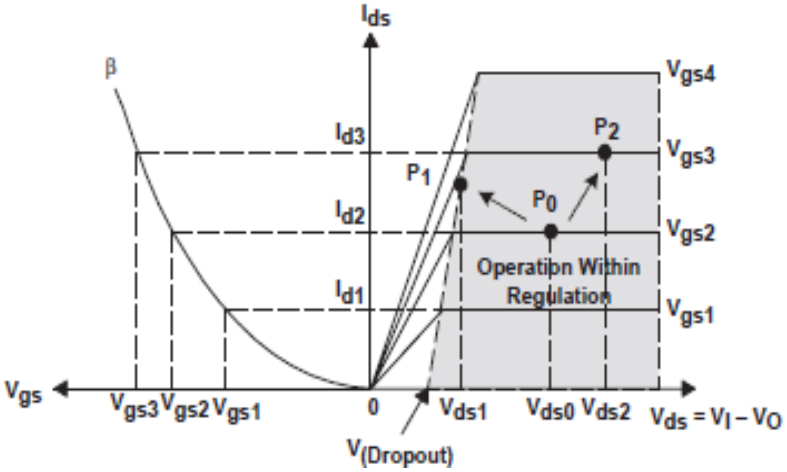


Figure 13LDO Operation[19]

When the input voltage decreases to near the output voltage, the operating point P1 moves to the operating point towards left of P1 (dropout region). Within the dropout region, gate to source voltage is no longer a function of the control loop, but of the input voltage. In other words, the regulator control loop cut off and Vgs begins to depend on the decreasing input voltage. Thus when the input voltage decreases further, the control voltage (Vgs) also decreases in proportion to the decreasing input voltage. Finally, the regulator reaches the turnoff point.

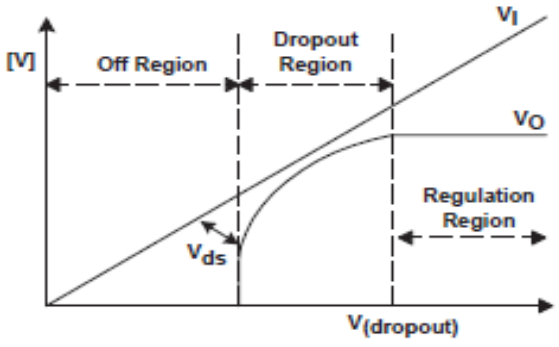


Figure 14 LDO regions of Operations[19]

Figure14 shows the dropout region in addition to the off and regulation regions. Below V(dropout) the output voltage drops with decreasing input voltage and we no longer get regulated voltage from LDO output.

3.4.1.1 LDO Topologies

The regulator circuit composed of majorly four functional circuits: the voltage reference, the pass element, sampling resistor, and the error amplifier. Linear voltage regulators can be classified based on pass element structures such as NPN-Darlington, NPN, PNP, PMOS, and NMOS regulators.

Table1 compared the different LDO topologies classified on the basis of pass element structure. The bipolar devices can deliver the higher output currents for a given supply voltage. However the MOS-based circuits offer limited drive performance with a strong dependence on aspect ratio and to voltage-gate drive[18]. On the positive side, however, the voltage-driven MOS devices minimize quiescent current flow.

PARAMETER	DARLINGTON	NPN	PNP	NMOS	PMOS
$V_{dropout}$	Vsat+2Vbe	Vsat+Vbe	Vce(sat)	Vsat+Vgs	VSD(sat)
$I_{q(Quicsent\ Current)}$	Medium	Medium	Large	Low	Low
I_{oMax}	High	High	High	High	High
Speed	Fast	Fast	Slow	Medium	Medium

Table1 Different LDO Topologies[19]

3.4.1.2 Quiescent Current

Quiescent current, or ground current, is the difference between input and output currents. Minimum quiescent current is necessary for maximum current efficiency. Quiescent current is defined by

$$I_q = I_i - I_o$$

Quiescent current consists of bias current (such as band-gap reference, sampling resistor and error amplifier) and drive current of the series pass element, which do not contribute to output power or in other words it is the current wasted. The value of quiescent current is mostly determined by the series pass element topologies, ambient temperature, etc. For current driven elements such as for bipolar devices Quiescent current value is more as compared to voltage driven devices such as mosfet. For bipolar transistors, the quiescent current increases proportionally with the output current (based on collector is directly proportional to base current) because the series pass element is a current-driven device. For MOS transistors, the quiescent current has a near constant value with respect to the load current(drain current is independent of gate current) since the device is voltage-

driven. LDO voltage regulator employing MOS transistors is essential in applications where power consumption is critical or where small bias current is needed in comparison with the output current.

3.4.1.3 Efficiency

The efficiency of a LDO regulator is limited by the quiescent current and input/output voltage as given by

$$\frac{IoVo}{Io + Iq} * 100$$

For a LDO regulator to have high efficiency drop out voltage and quiescent current must be minimized. In addition, the voltage difference between input and output must be minimized since the power dissipation of LDO regulators is a parameter for the efficiency.

$$\boldsymbol{Power\ Dissipation} = (\boldsymbol{Vi} - \boldsymbol{Vo})\boldsymbol{Io}$$

Low dropout regulators have the advantages of a quiet operation when compared to switching circuits such as a DC–DC converter, so they are mostly employed in systems that requires a low noise and highly stable power source. LDOs are also used in applications such as battery-powered systems. Power dissipation and thereby efficiency, can be improved as the dropout voltage decreases. These features of low dropout voltage and low current consumption make LDOs an efficient solution in portable and RF applications. Modern LDOs are characterized by their ability to prevent fluctuations in the regulated output voltage due to input voltage variations, output noise and quiescent current.

3.4.2 Bandgap Reference Circuit

Voltage reference bandgap circuit is the essential component of many analog circuits that has requirement of little dependence on supply and process parameters and a well-defined dependence on temperature.

Bandgap reference has a well-established reference generator technique and is most popular for both technologies CMOS and bipolar. The basic principle of the operation of bandgap circuits relies on two groups of diode-connected BJT transistors running at different emitter current densities. The negative temperature dependence of the PN junctions in one group of transistors is cancelled with the positive temperature dependence from a PTAT (proportional-to-absolute-temperature) circuit from the other group of transistors resulting in a fixed DC voltage is generated which doesn't change with temperature [22]. The resulting voltage is about 1.2–1.3 V, depending on the particular

technology, and is close to the theoretical band gap of silicon at 0°K. The components of a bandgap reference circuit consists of a supply-independent biasing circuit, a PTAT circuit, a diode connected BJT transistors generating a voltage with negative temperature coefficient and some kind of feedback mechanism to improve the performance.

3.4.2.1 Bandgap Reference:

A reference voltage is generated by addition of two voltages having opposite temperature coefficients with suitable multiplication constants leading to resulted voltage obtained which is independent of temperature. The diode voltage drop across the base-emitter junction V_{BE}, of a Bipolar Junction Transistor (BJT) changes Complementary to Absolute Temperature (CTAT**)** and for the two BJTs operating with unequal current densities, the difference in the base emitter voltages, ΔV_{BE} of the transistors is found to be Proportional to Absolute Temperature (PTAT). The PTAT voltage may be added to the CTAT voltage with suitable weighting constants to obtain a constant reference voltage.

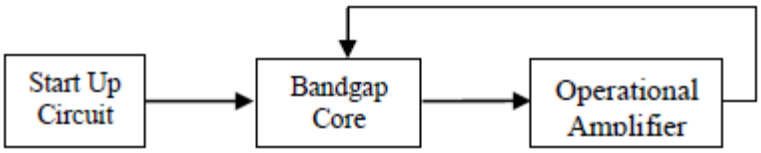


Figure 15 Basic Bandgap circuit[23]

3.4.2.2 Bandgap core:

It is the most important part of reference circuit that produces the reference voltage. Node A and Node B are actually input to the operational amplifier. So the voltage of these two nodes is equal. IREF is a reference current source and is obtained from the output of operational amplifier. R1, R2 and R3 are the resistances responsible for generating constant voltage independent of variation. Two transistors (q1 and q2) are actually vertical inherent BJTs of CMOS process. From the schematic in figure16 it can be found that there are two branches in this core circuit. Initially current in branch1 (branch having R1 and R3) is higher than that of branch2 (branch having R2). At steady state, current through both branches becomes equal. Therefore voltage of node A and node B becomes equal. Since voltages of node A and node B are equal, therefore the voltage across the resistor R2 is given by

$$\boldsymbol{V_{R2} = I_2 R_2}$$

$$= \frac{V_{BE2} - V_{BE1}}{R_3} * R_2$$

$$= \frac{V_T \ln(4)}{R_3} * R_2$$

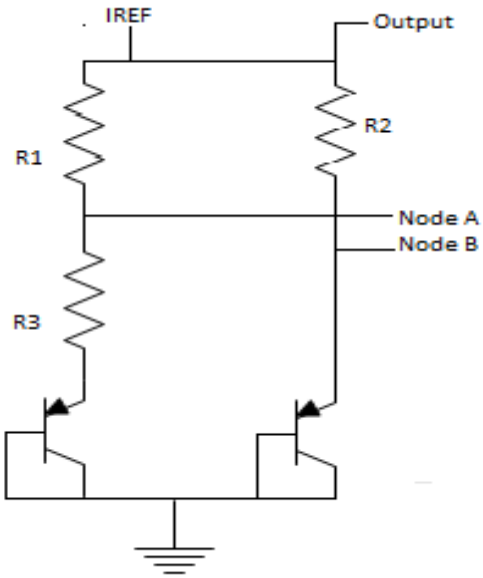


Figure 16 Bandgap Core[22]

V_T is thermal voltage, which is given as, $V_T = KT/q$ .So V_T is directly proportional to absolute temperature (T). V_{R2} is a positive temperature constant voltage. And it is known from the theory of BJT that base emitter voltage of a BJT is conversely proportional to temperature. So output voltage is given as

$$Vout = V_{R2} + V_{BE2}$$

$$\frac{V_T \ln(4)}{R_3} * R_2 + V_{BE2}$$

Thus output voltage is actually summation of a positive TC and a negative TC voltage. By choosing the proper value of resistors, output reference voltage is made constant with respect to temperatures (Zero TC)[23].

3.4.2.3 Startup Circuit

When the supply is turned on, if all of the transistors carry zero current they may remain off indefinitely because the loop can support a zero current in both branches in the bandgap reference circuit. So for the proper operation of bandgap it is required to inject current in the bandgap core and startup circuit does this job. This circuit also turns off when steady state is reached.

3.4.2.4 Operational Amplifier:

Operational Amplifier (Opamp) used for the bandgap circuit is basically a two stage differential amplifier. As difference in input voltage of the operational amplifier is very small, small gain in amplifier will not produce enough current to drive the bandgap core. Moreover MOSFET doesn't have high Transconductance. So for proper function of bandgap core it is needed to increase the gain of the circuit. This is the reason of using a two stage operational amplifier in bandgap circuit.

The main purpose of the operational amplifier is to drive the bandgap core. Operational Amplifier is designed in such a way that its output is independent to variation in supply. This helps to establish a reference voltage which is insensitive to supply. Ideally this Opamp should have infinite gain for proper function of bandgap core as output current of operational amplifier drives the bandgap core. Opamp can produce a current which is insensitive to variation of VDD (supply voltage) by driving the amplifier with its own output current. This is done by mirroring. This makes the output current of operational amplifier almost constant with respect to variation in supply voltage.

3.4.2.5 Variation of Reference Voltage with supply noise

Here it has been assumed that noise voltage is a sine voltage having amplitude of 1V, frequency of 1Mega Hz. Initially there is oscillation in reference voltage, but eventually reference voltage settles to steady state value.

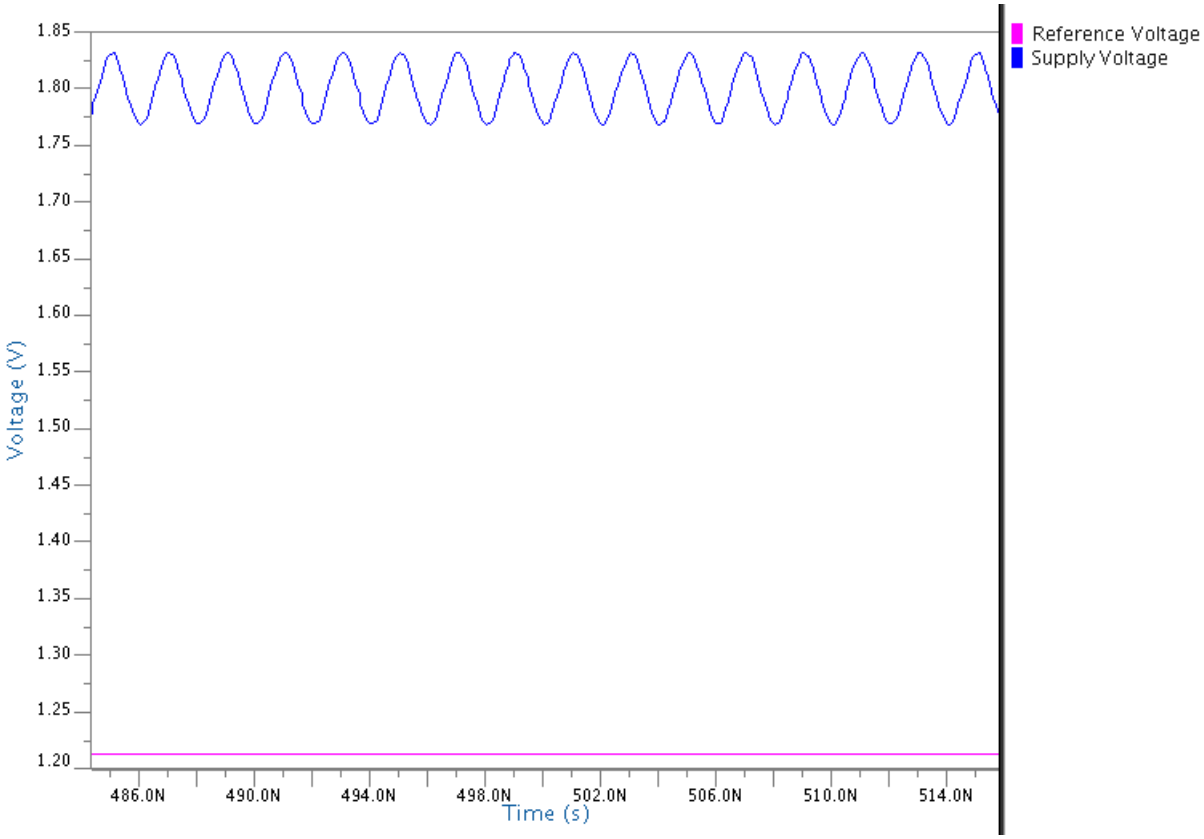


Figure 17 Bandgap Output and supply voltage

3.4.3 Ring Oscillator

Ring oscillator is cascaded combination of delay stages, connected in a close loop chain. A ring oscillator is a free running oscillator comprised of an odd number of open-loop inverting amplifiers in a feedback loop. The ring oscillators designed with a cascaded connections of inverters and capacitors are connected in between to provide stability and delay[24].

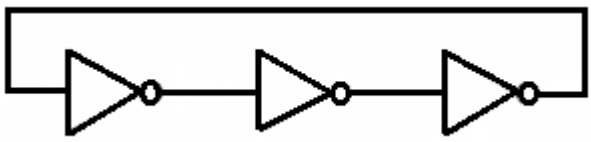


Figure 18 Ring Oscillator[24]

The attractive features of ring oscillators includes, it can achieve oscillations at low voltage. Moreover it can be designed with the complimentary logic design (CMOS, BiCMOS). It can provide high frequency of oscillations while dissipating low power and can be tuned electrically. It can provide wide tuning range and multiphase outputs because of their basic structure. These outputs can be logically combined to realize multiphase clock signals, which have considerable use in a number of applications in communication systems.

3.4.3.1 Frequency of Oscillation

The oscillation frequency of a ring oscillator depends on the propagation delay (td) per stage and the number of stages used in the ring structure. To achieve self-sustained oscillation, the ring must provide a phase shift of 2Π and have unity voltage gain at the frequency of oscillation. In an *m*-stage ring oscillator, each stage provides a phase shift of Π /*m* and dc inversion provides the remaining phase shift of Π. Therefore, the oscillating signal must go through each of the *m* delay stages once to provide the first Π shift in a time of m td and it must go each stage a second time to obtain the remaining phase shift in a time period of 2*m* t*d*. Thus the frequency of oscillation is given by[25]:

$$f_o = \frac{1}{2m\tau d}$$

The oscillation frequency of an RO may be determined from the expression of t*d* which depends on the circuit parameters. But the main difficulty in obtaining the expression of td arises due to the nonlinearities and parasites of the circuits.

3.4.3.2 Effect of supply integration on phase noise and jitter

Phase Noise and jitter are both ways of describing the stability of an oscillator. Phase Noise describes the stability in frequency domain while timing jitter is considered in time domain. The domain to consider for predicting oscillator stability is application dependent. RF engineers working in communication filed are interested in phase noise as poor phase noise performance measurement leads to improper up and down conversions and inaccurate channel spacing. However digital engineers working in time division multiplexing (TDM) are concerned with timing jitter as poor jitter performance leads to network excessive resending of traffic [26].

Phase noise is defined with respect to the noise power in a 1-Hz bandwidth as a function of frequency. Phase noise is defined as the ratio of the noise in a 1-Hz bandwidth at a specified frequency offset (f_m), to the oscillator signal amplitude at frequency (f_o) and is expressed in dbc/hz. Period jitter (J_{PER}) is the time difference between a measured cycle period and the ideal cycle period. Due to its random nature, this jitter can be measured peak-to-peak or by root of mean square (RMS).

It has been shown in figure19 that on integration of power supply to the two ring oscillators there is an increase in phase noise of the oscillators. The PDN are designed in such a manner to minimize the phase noise on supply integration.

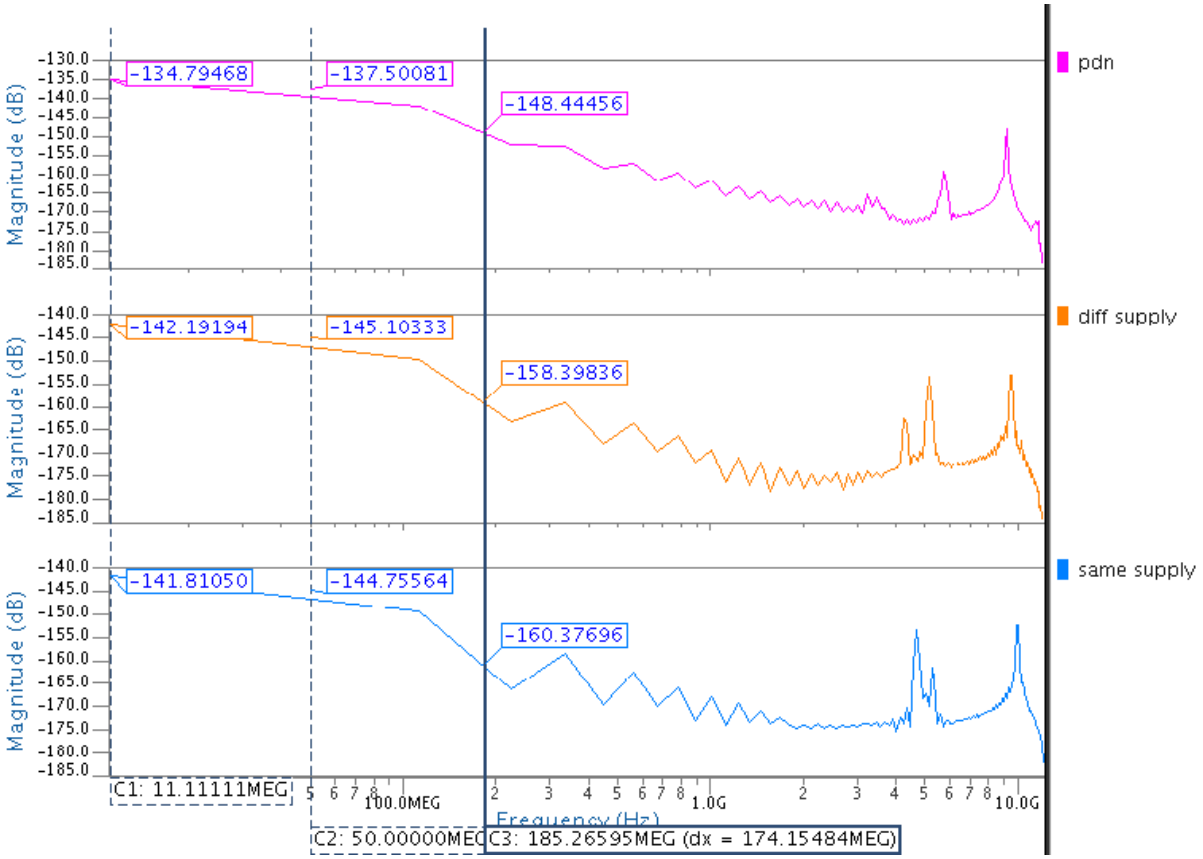


Figure 19 Phase noise with supply integration

4. PROPOSED WORK

To overcome the drawbacks of time domain analysis a memory efficient, faster and easier frequency domain approach has been proposed to predict the power supply noise and whether supply sharing is feasible among analog and mixed signal s such as Bandgap reference , LDO and ring oscillators.

4.1 BASIC IDEA FOR PROPOSED METHODOLOGY

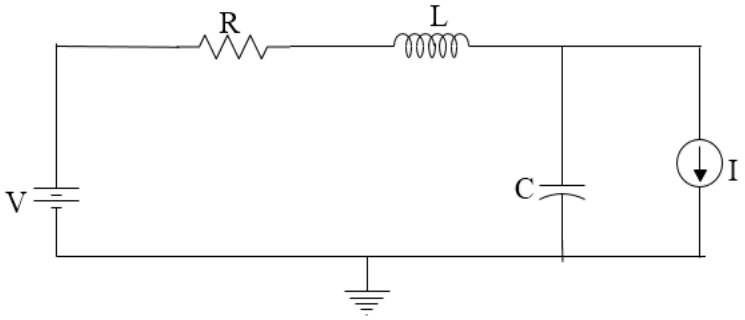


Figure 20 Idea behind Proposed Method

- Disturbance incorporated due to I(load) are analysed in Frequency domain using AC analysis
- Stimuli is applied at input terminal(V) and output is taken across Capacitor
- Approach followed is calculating the Impedance(Z) seen from the current source and observe

$$\boldsymbol{V(f) = FFT(I) * Z}$$

- Observing behaviour before and after settling time
- IFFT{V(f)} is then validated against the Tran analysis.

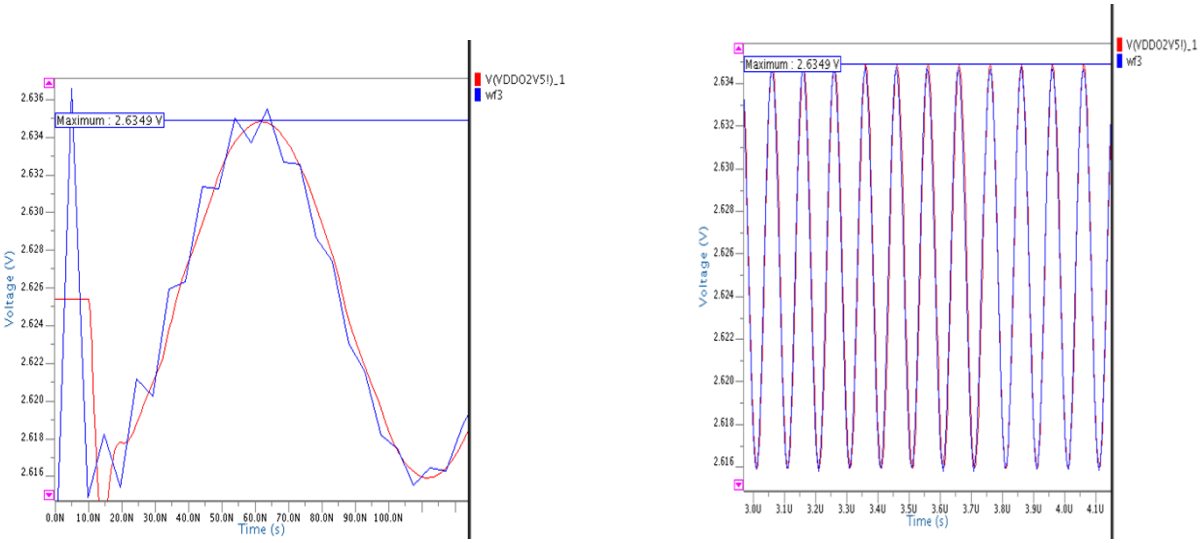


Figure 21 Initial mismatch before settling time in tran and ac analysis

Proposed Approach to Counter Problem

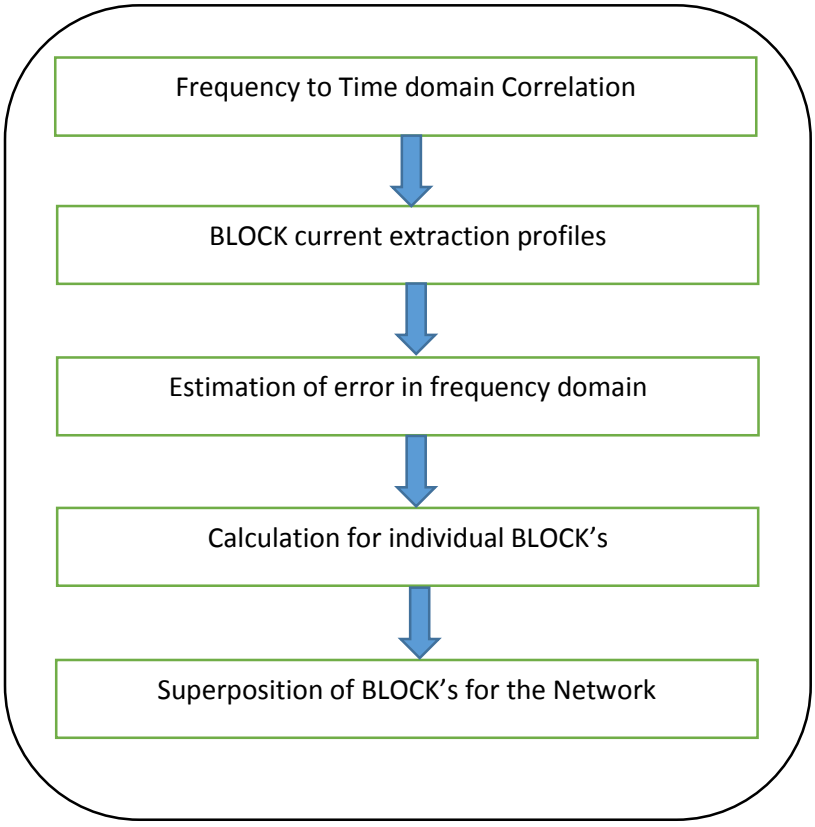


Figure 22 Flow chart to cater Problem

4.2 Methodology for non-switching BLOCKs

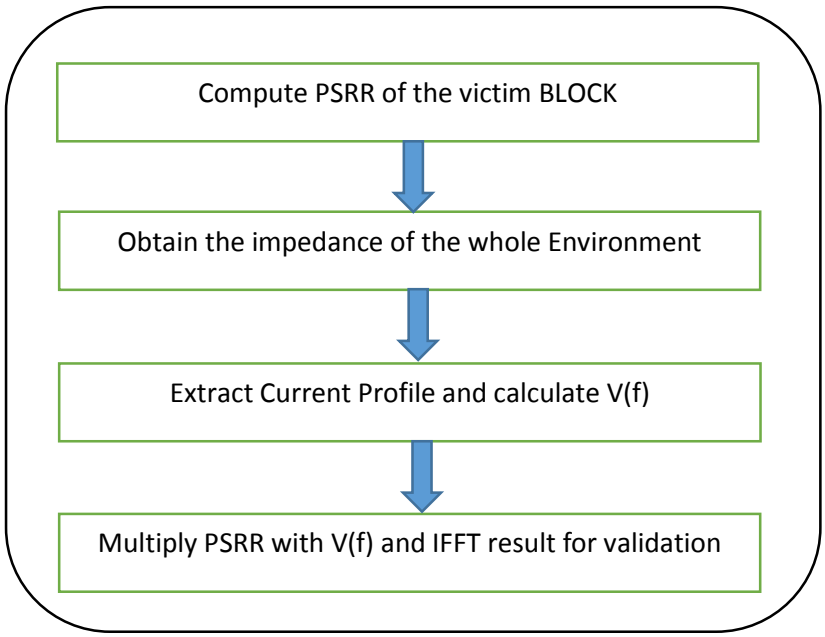


Figure 23 Methodology non switching blocks

1) Compute the PSRR of the BLOCK by superimposing the ac input source of amplitude one on the DC power supply and observing the output of the using AC analysis.

2) Obtain the impedance(Z) of the circuit using Norton theorem method by looking inwards from the supply rail

3) Compute Fourier Transform of the current profile and perform $\boldsymbol{V(f) = FFT(I) * Z}$ using waveform calculator

4) Multiply the Vdd(f) with PSRR obtained in step 1 to get $\boldsymbol{Vout(f)}$ and validate $\boldsymbol{IFFT\{Vout(f)\}}$ with Tran analysis

4.2.1 Setup for individual BLOCK's

The following PDN's are used with C_{vary} has values of 1nf,100p, 10p and 1 pf

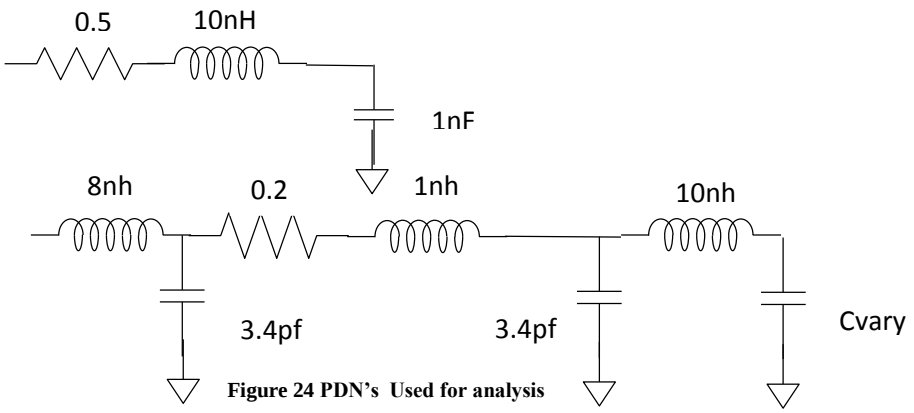


Figure 24 PDN's Used for analysis

Considering non switching s such as Differential (Diff) amplifier based Buffer, Bandgap reference circuit and LDO

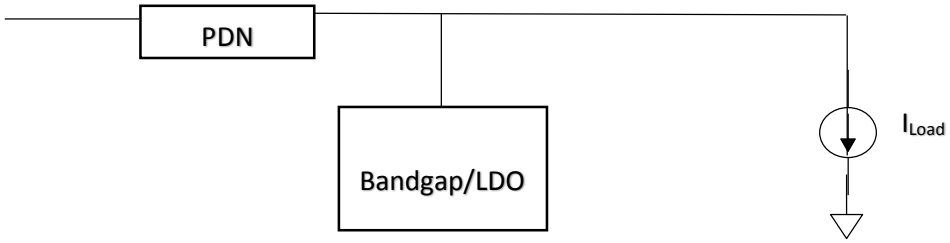


Figure 25 Setup for individual BLOCK's

4.2.2Setup Integrated Environment

When multiple are connected to a single power supply passing through PDN, one whose output to be computed acts as a Victim and remaining s acts as noise source for the victim in an integrated environment. Here the effect of noise coupled from one to other has to be taken into consideration.

Integrated LDO and Bandgap circuits (non switching blocks)

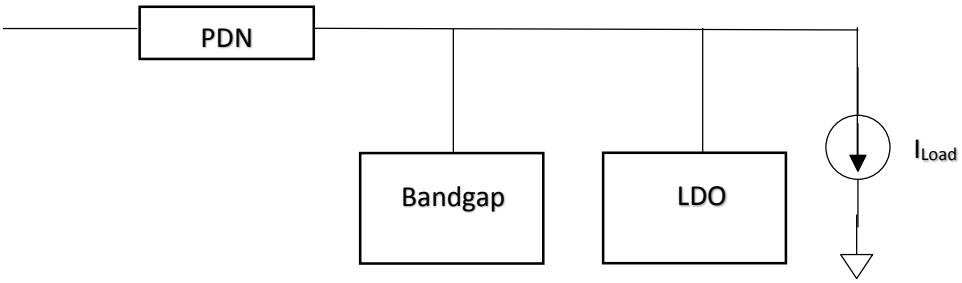


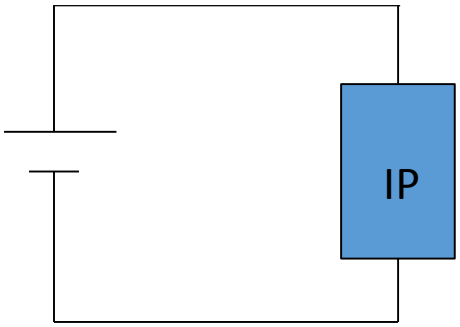
Figure 26 Setup for integrated BLOCK's

4.3 Analysis using S-Parameter

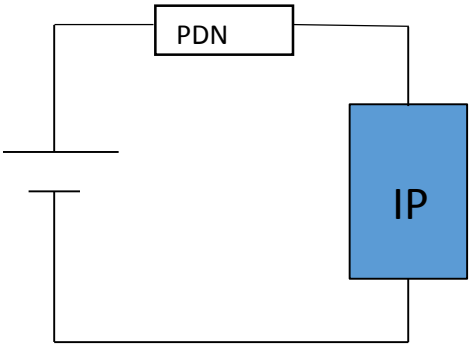
4.3.1 Approach followed:

- First current profile and S parameters are measured by connecting individual BLOCK's with Ideal clean supply.
- S parameter is used to model internal impedance of BLOCK (Bandgap and LDO). Z impedance are measured considering supply node and ground as the 2 ports and measuring impedance of all the nodes with respect to these 2 ports.
- The same setup is run with BLOCK's replace by internal Z impedance(S parameter) & a current source in parallel calculated from ideal supply.

- Tran analysis is done to compare supply voltage for the 2 setup's one with an actual BLOCK'S and other with S parameter and extracted current profile of BLOCK in parallel



Spice simulation to obtain I(Ideal Supply)



Spice simulation with sample PDN(Normal Tran Analysis)

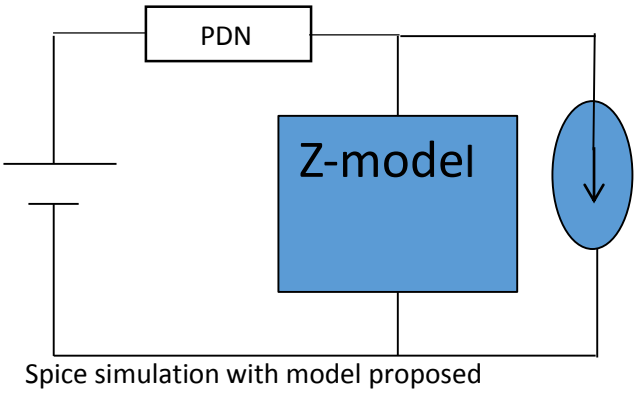


Figure 27 S-Parameter Model Proposed

4.3.2 Methodology for Switching blocks (Using Z-Model)

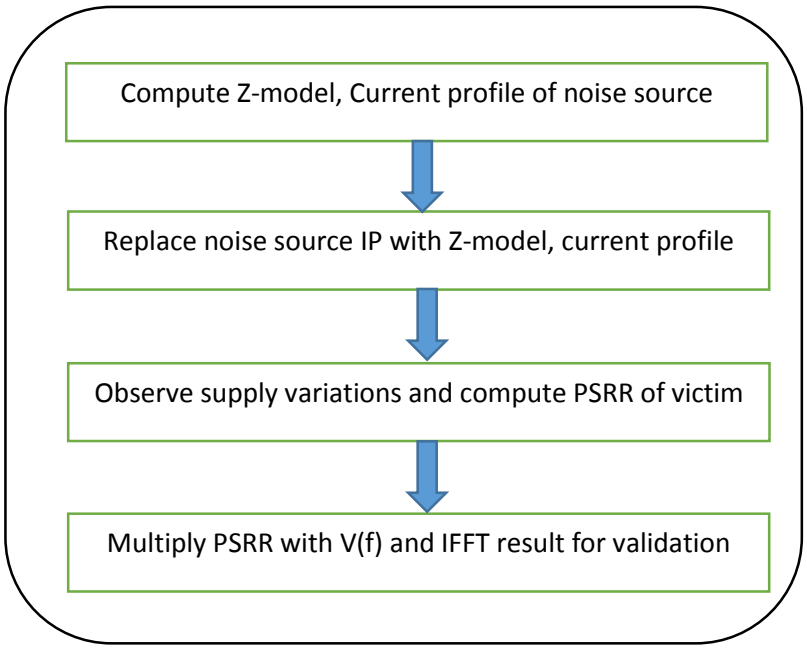


Figure 28 Methodology Switching blocks

1) Compute the S parameter and extract the current profile of the BLOCK acting as noise source.

2) Observe the variation in supply rail(Vdde) after replacing noise source BLOCK with its S-Parameter.

3)Calculate the PSRR of the source BLOCK(victim) and compute $\boldsymbol{PSRR * FFT(vdde)}$ to obtain V_{out} and validate $\boldsymbol{IFFT(Vout)}$ against tran analysis.

4.3.3 Setup for the Circuit

Ring Oscillator has been used as a switching block as it consumes current on switching from logic high to logic low and vice versa. The switching block (ring oscillator) has been used as a noise source that has been shared with a LDO. The Z-model analysis has been done to compute the impedance of Ring Oscillator.

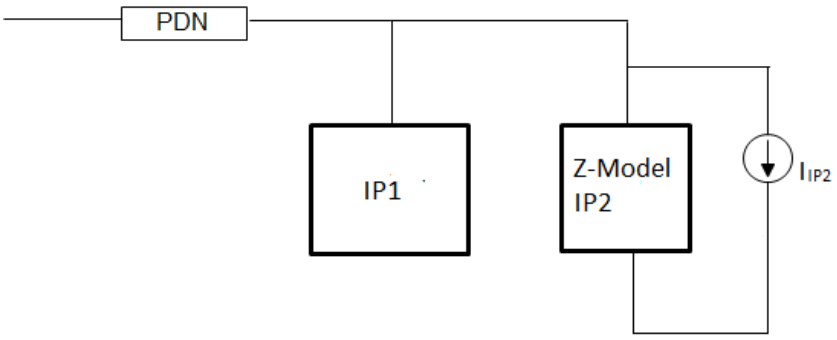


Figure 29 Setup circuit for switching/Non Switching Block

4.4 Proposed Method for predicting Power Supply Noise

The regulated power supply from LDO regualtor are being integrated to BLOCK's after passing through PDN.The power supply noise can be predicted by employing the concept of ohm's law(V=I*Z) for the integrated BLOCK's without actually simulating the enviornment

4.4.1 Methology for predicting power supply noise:

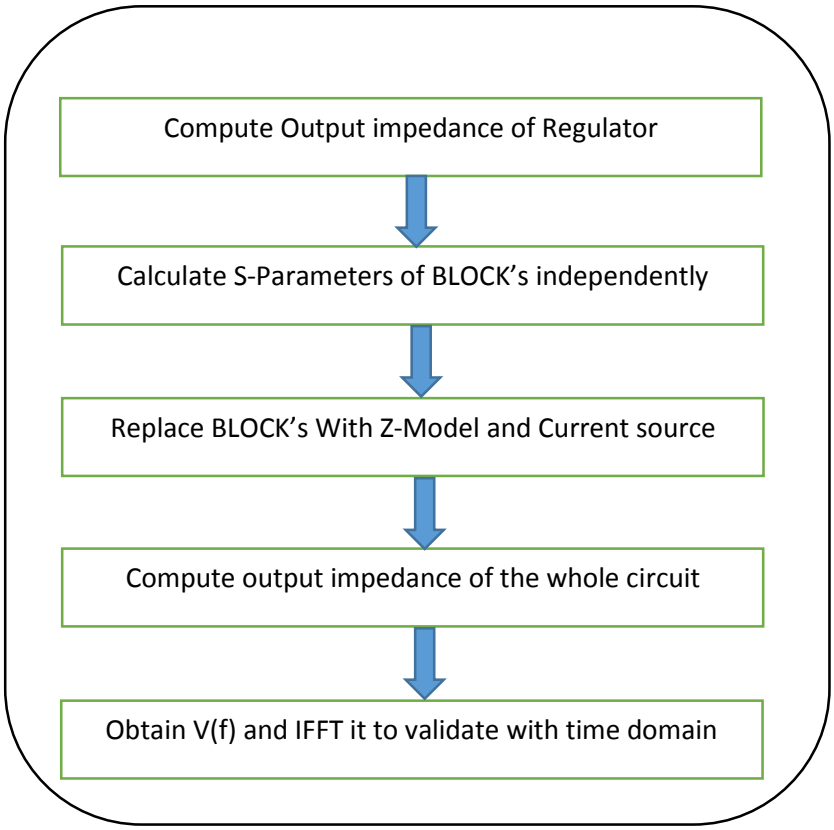


Figure 30 Predicting Power Supply Noise

1)Compute the output impedance of the LDO regulator seeing into the Output node using the concept of Norton Equivalent.

2)Calculate the S-parameters and extract the switching current of BLOCK's as connected independently to an ideal supply.

3)Replace the actual BLOCK's with its Z-Model and the extracted current in parallel.

4) Calculate the output impedance from the node of point of computation of power supply noise with LDO regulator replaced with its output impedance and integrated BLOCK's with its Z model and current source in parallel.

5)Calculate V(f)=FFT{extracted current of BLOCK whose supply noise is to be calculated} * Z(impedance computed in above step. Inverse Fourier Transform V(f) to obtain supply noise characterstic in time domain and validate it against the results obtained using actual integrated enviornment.

4.4.2 Series Connection:

Two or more BLOCK's that are integrated to a regulated supply from LDO regulator in a series manner.Supply noise are variation in voltage at nodes A and B.

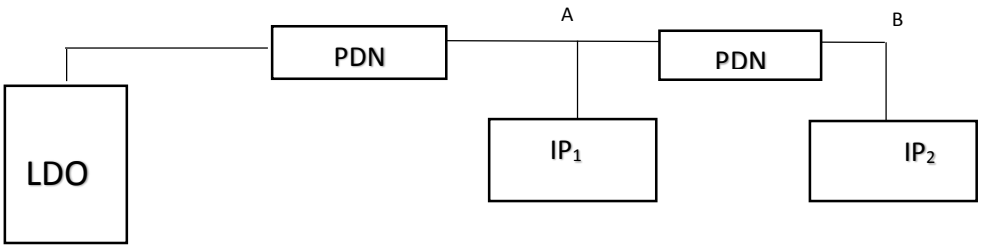


Figure 31 Normal Method of Power Supply Analysis for BLOCK1 and BLOCK2(Tran Analysis)

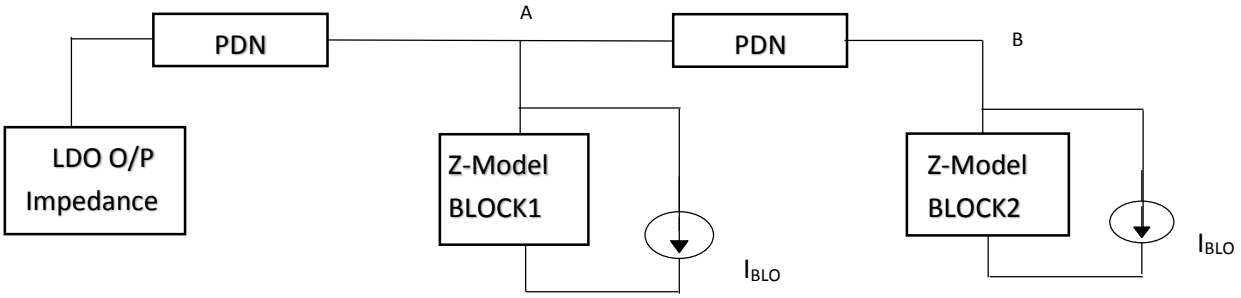


Figure 32 Proposed Method of Predicting Power Supply Noise for BLOCK1 and BLOCK2

4.4.3 Star Connection:

The proposed Methodology for prediction of power supply noise has been validated for the star topology in which regulated voltage from voltage regulator has been shared by two switching BLOCK's.

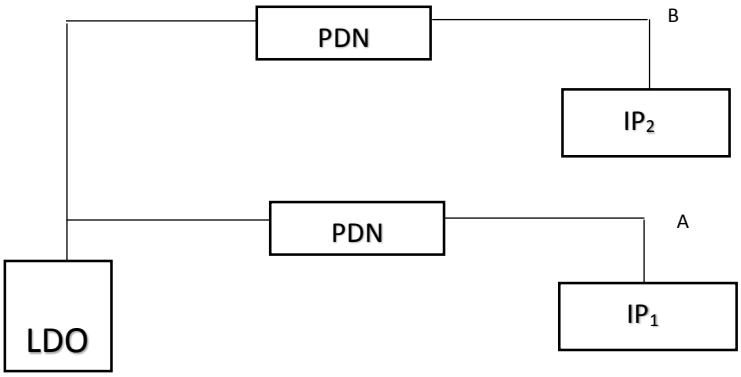


Figure 33 Normal Method of Power Supply Analysis for BLOCK1 and BLOCK2(Tran Analysis)

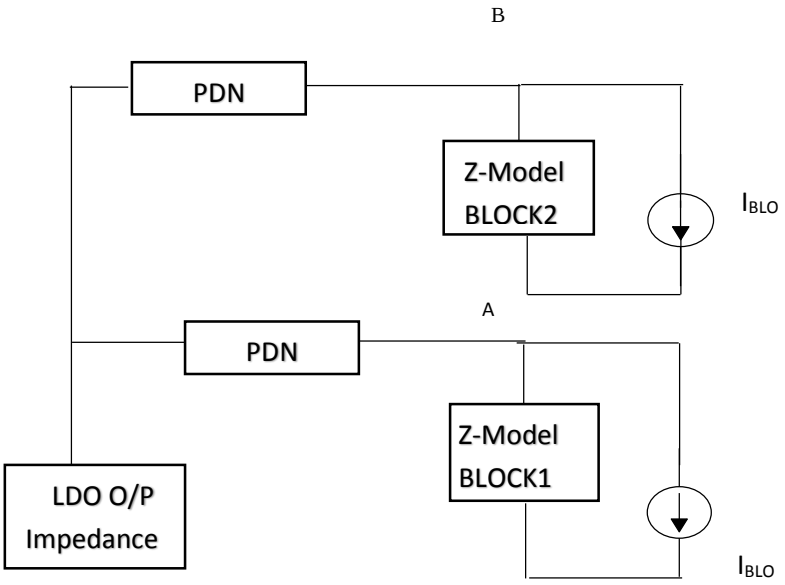


Figure 34 Proposed Method of Predicting Power Supply Noise for BLOCK1 and BLOCK2

5. RESULTS

The proposed approach for the frequency domain analysis has been validated first for the individual non switching BLOCK's such as LDO and Bandgap.

5.1 INDIVIDUAL S

The results in figure 35 and 36 shows a proper match between tran analysis and AC analysis using framed methodology for LDO and Bandgap circuits

5.1.1 LDO Circuit

The analysis is done for C=100pf,1nf and I_{load} Frequency=1,10MHz and all these values confirmed the proper match between Tran and Freq domain methodology.

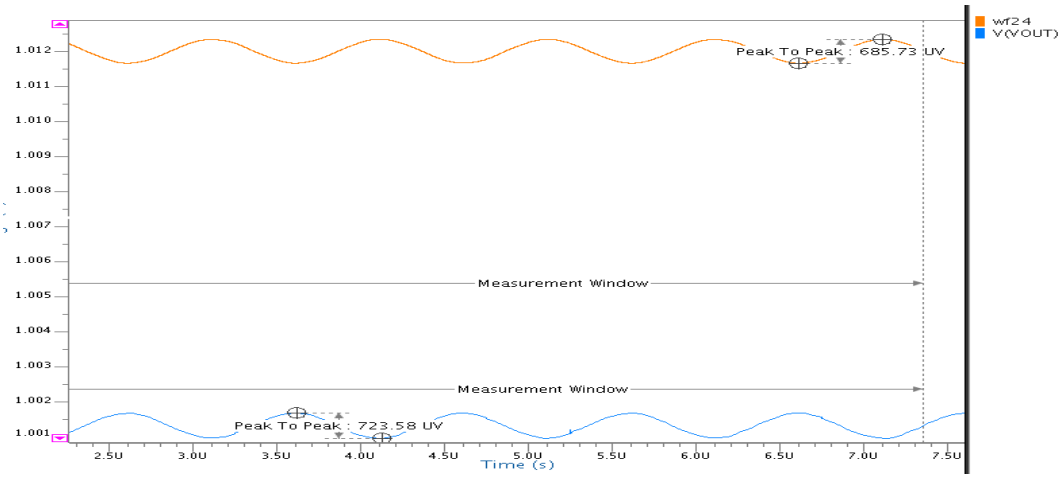


Figure 35 Peak to Peak Match between tran and proposed approach for LDO

5.1.2 Bandgap Circuit

The analysis is done for C=100pf,1nf and I_{load} Frequency=1,10MHz and all these values confirmed the proper match between Tran and Freq domain methodology

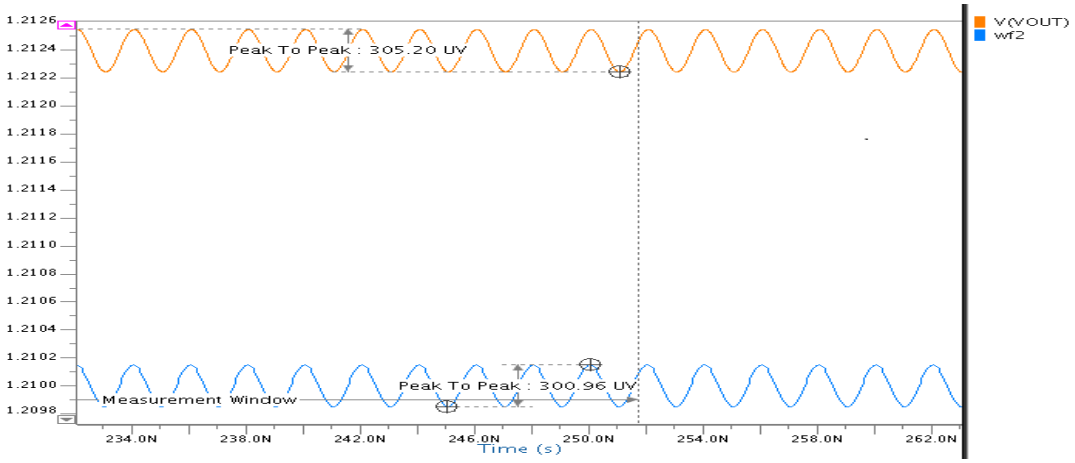


Figure 36 Peak to Peak Match between tran and proposed approach for Bandgap

5.2 INTEGRATED ENVIRONMENT:

The non-switching blocks are connected to the shared power supply.

5.2.1 LDO as Noise source and Bandgap as Victim

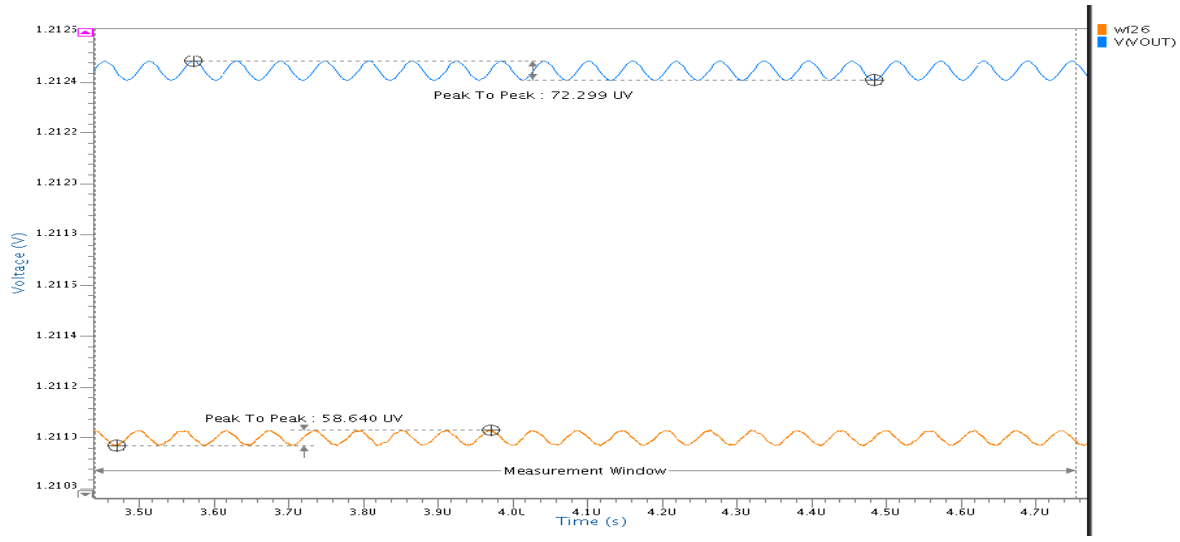


Figure 37 Peak to peak match between proposed approach and tran analysis when LDO as noise source in integrated environment

5.2.2 LDO as Victim and Bandgap as Noise Source

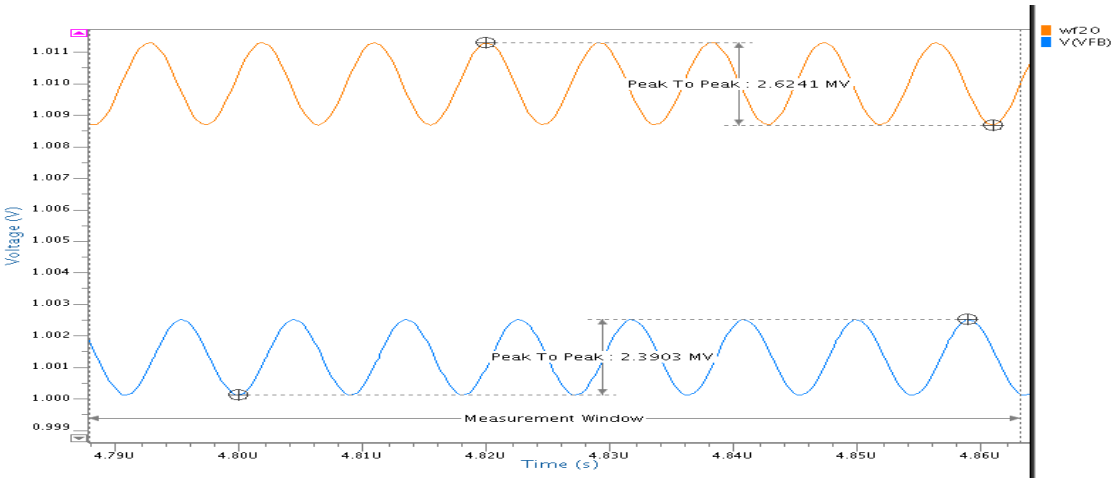


Figure 38 Peak to peak match between proposed approach and tran analysis when Bandgap as noise source in integrated environment

Result obtained verifies that ac analysis using this methodology can replace the usual Tran analysis practice as results are within 5% range

5.3 Analysis using S-Parameter(Z-Model)

The proposed approach that states that replacing BLOCK with its S-Parameter and current profile has no effects in its power supply fluctuation.

5.3.1 Individual Blocks :

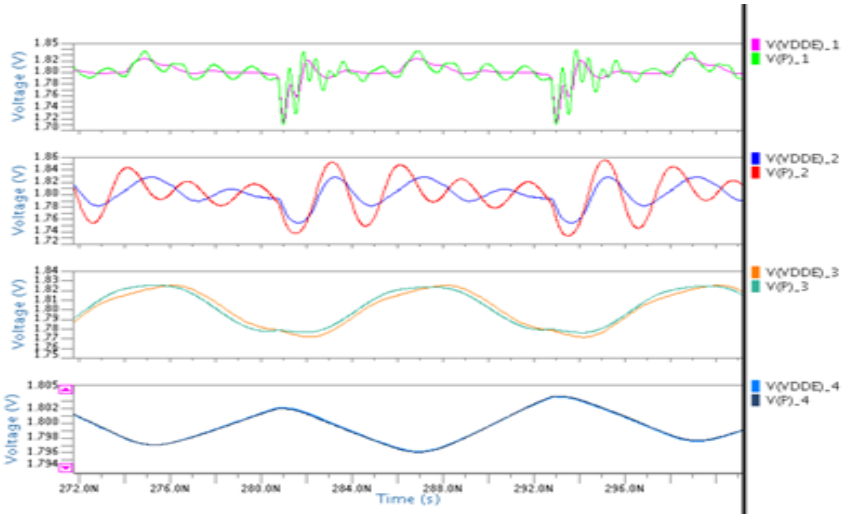


Figure 39 Comparison between BLOCK Simulation and BLOCK replaced by S-parameter and Current Profile for LDO

For the LDO BLOCK it has been shown that we can replace BLOCK with S parameter and Current source Open Question arises when the C_{vary} (decap) in pdn are used of 10pf and 1pf or of lower values then V(P) and V(VDDE) shows some mismatch For higher C_{vary} (decap) values it shows perfect match .Square pulse PULSE (0 2m 4n 2ns 2ns 4ns 12ns) is applied at output of LDO Tran analysis are done for both the cases.

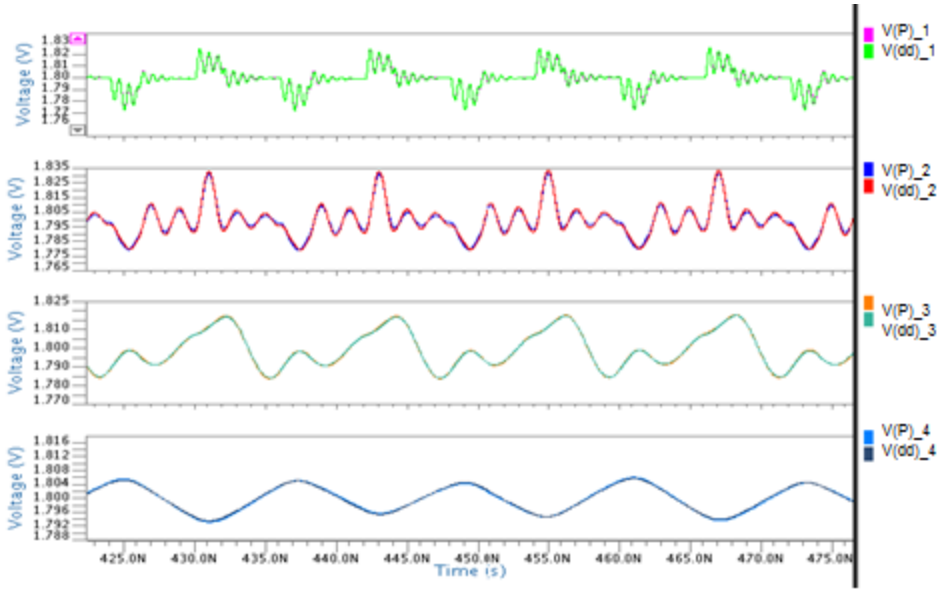


Figure 40 Comparison between BLOCK Simulation and BLOCK replaced by S-parameter and Current Profile for Bandgap

For the Bandgap BLOCK it has been shown that we can replace BLOCK with S parameter and Current source. Open Question arises when the C_{vary} (decap) in pdn are used of 10pf and 1pf or of lower values then V(P) and V(VDDE) shows some mismatch .For higher C_{vary} (decap) values it shows perfect match .Square pulse PULSE (0 2m 4n 2ns 2ns 4ns 12ns) is applied at output of Bandgap.Tran analysis are done for both the cases

5.3.2 Integrated Circuits

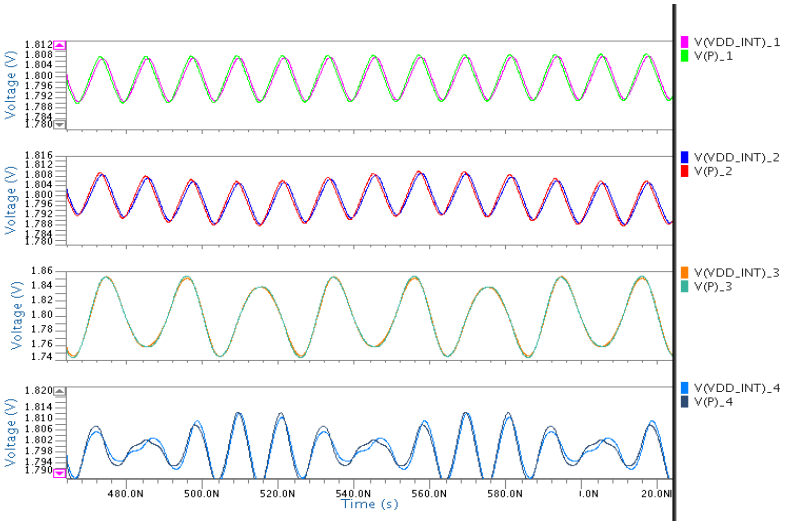


Figure 41 Match for Sinewave as Load of LDO in Integrated Enviornment

Iload used are sine wave with varying frequency. Sine wave used of 1,10,50 and 100 Mhz. At all frequencies of sine wave as load it has been shown that V(P) and V(VDDE) shows perfect match. C_{vary} (Decap) used of 1nf for all the frequencies.

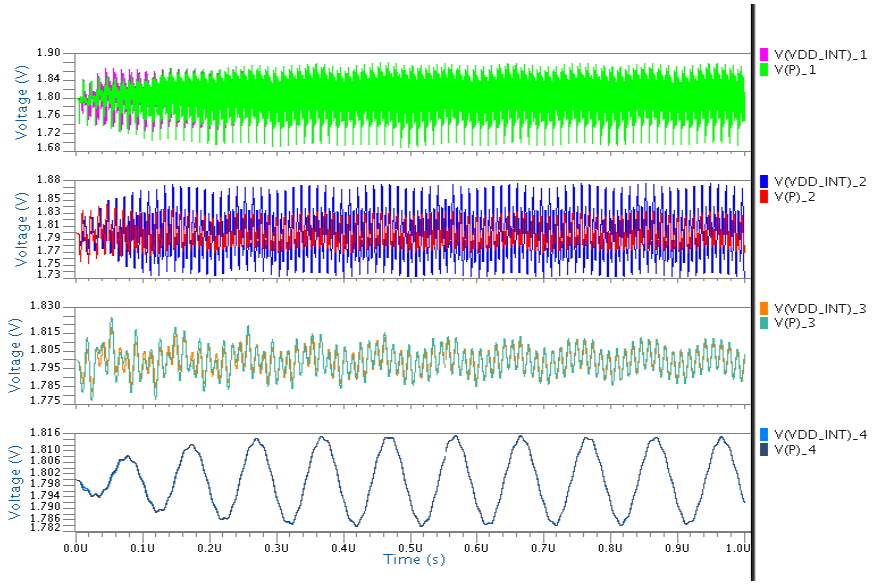


Figure 41 Comparison between BLOCK Simulation and BLOCK replaced by S-parameter and Current Profile for LDO and Bandgap Integrated

For integrated Bandgap and LDO BLOCK's it has been shown that we can replace BLOCK with S parameter and Current source .Open Question arises when the C_{vary} (decap) in PDN are used of 10pf and 1pf or of lower values then V(P) and V(VDDE) shows some mismatch .For higher C_{vary} (decap) values it shows perfect match. Square pulse PULSE (0 2m 4n 2ns 2ns 4ns 12ns) is applied at output of LDO and Bandgap .Tran analysis are done for both the cases

5.3.3 Switching circuit replaced with S-parameter

The result obtained from the proposed methodology that utilizes the concept of S-parameter has been validated after inverse transform in time domain. The switching block acting as noise source has been replaced with S-parameter.

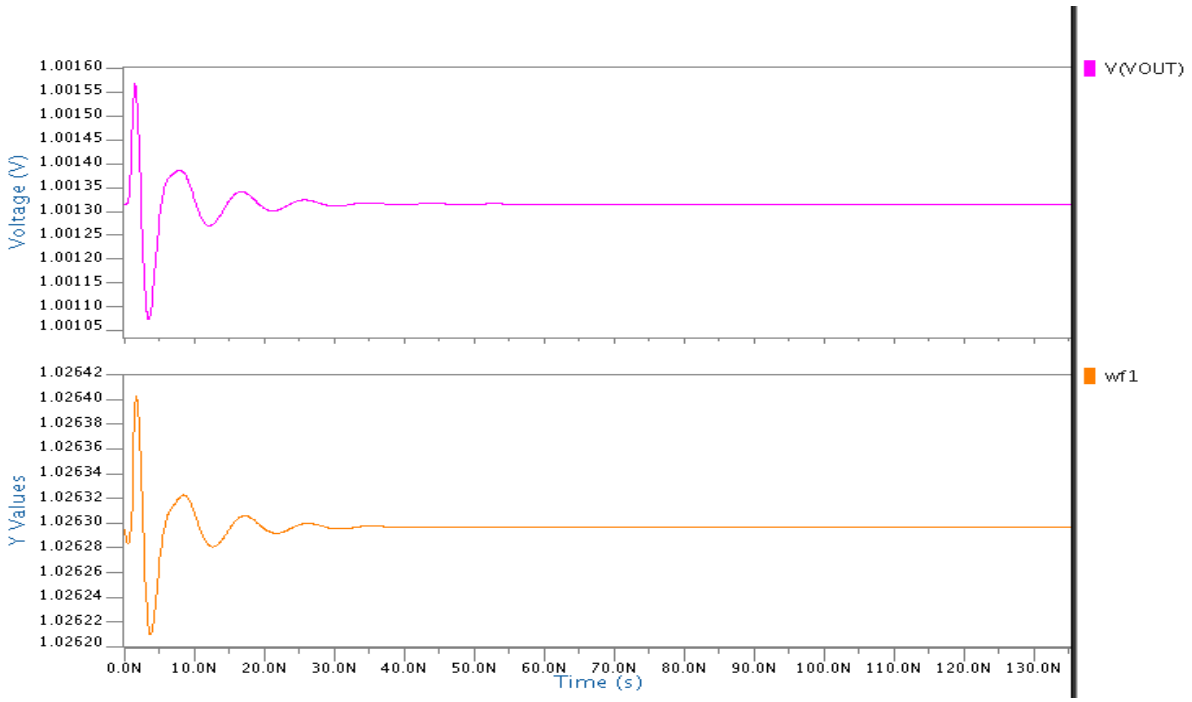


Figure 43 Comparison of Output obtained using Tran analysis and Proposed Methodology for S-parameter

5.4 PREDICTING POWER SUPPLY NOISE:

The proposed approach for the power supply noise has been verified on node A and B. The figure44 and 45 shows the comparison of power supply noise for series connection at node A and node B respectively with the results obtained using the normal Tran analysis for the series connection.

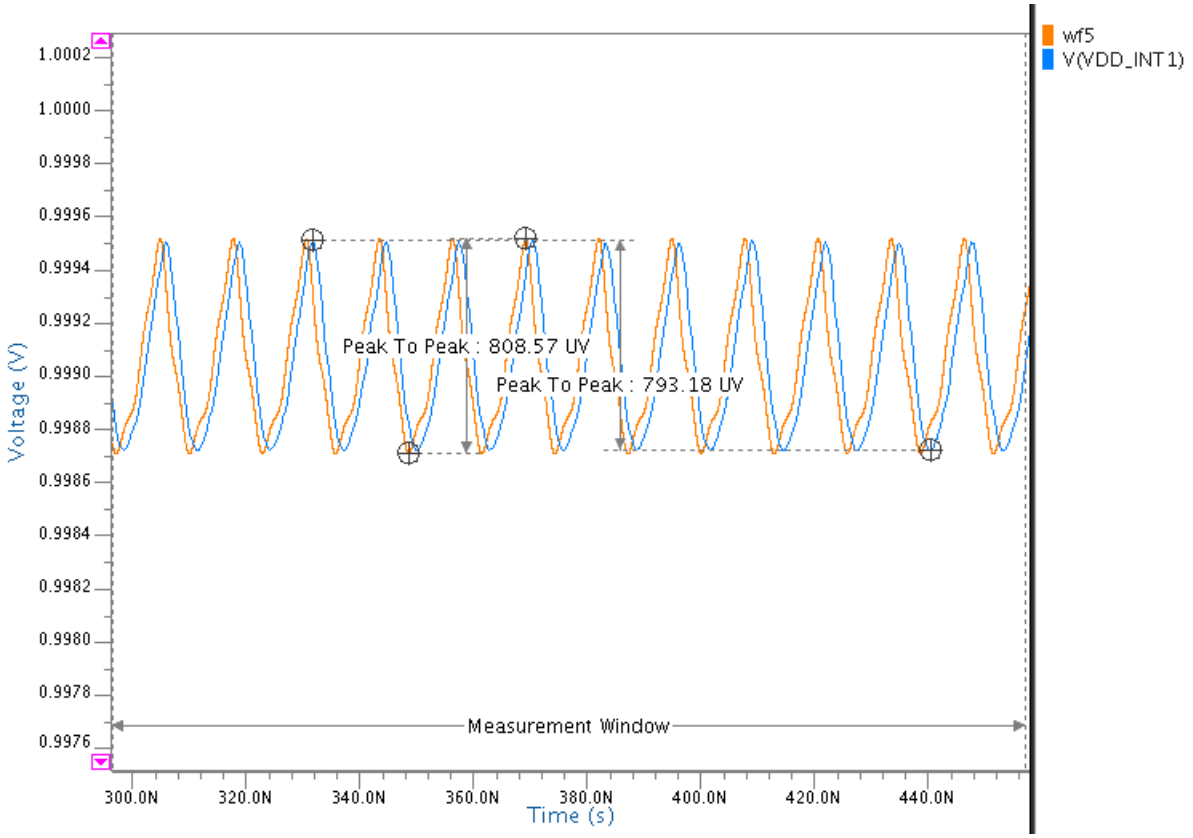


Figure 42 Comparison of PSN at Node A for normal and proposed method for series connection

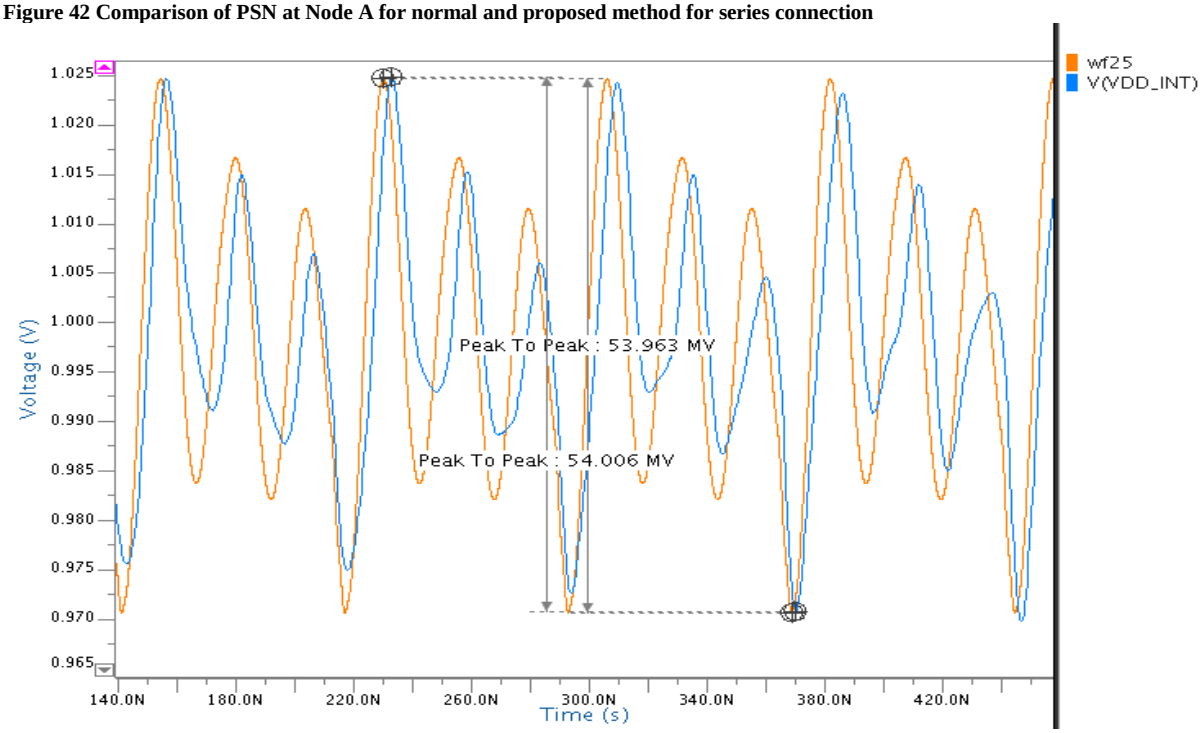


Figure 43 Comparison of PSN at Node B for normal and proposed method for series connection

The comparison of the normal method and the proposed method of power supply noise for the Star topology has been shown in figure46

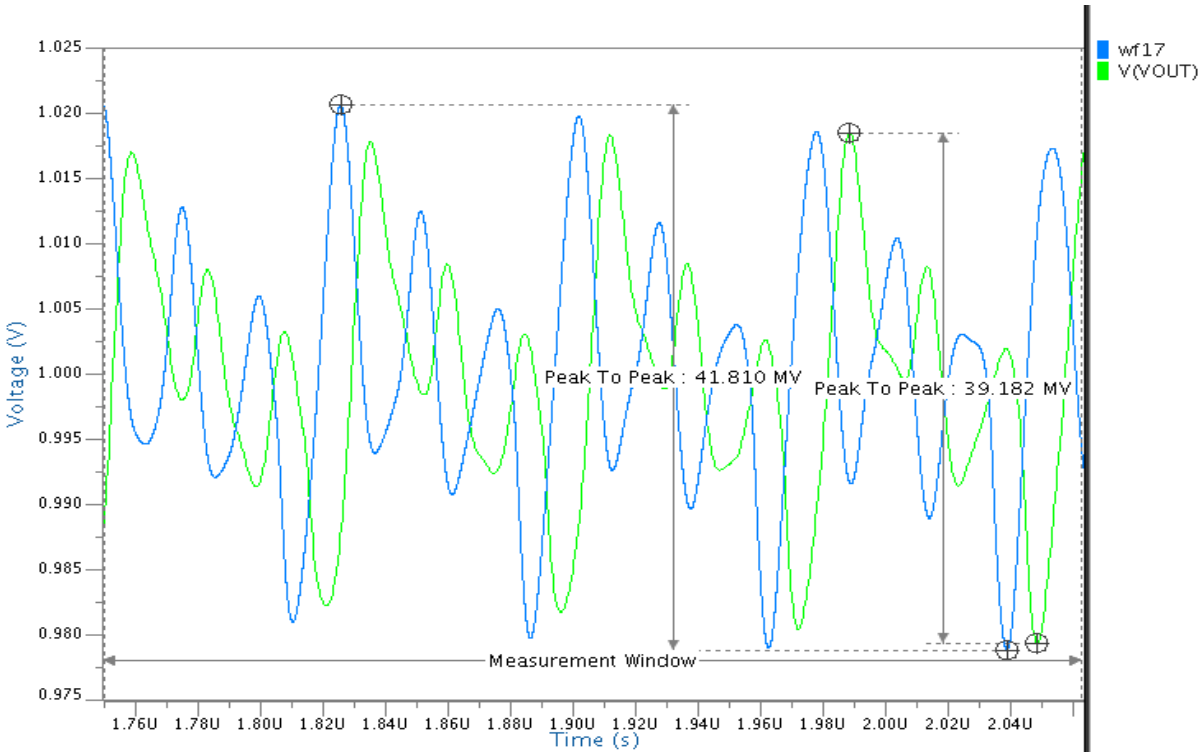


Figure 44 Comparison of PSN at Node B for normal and proposed method for star connection

6. CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSION

As can be implied from the results, the proposed methodology of frequency domain approach for non-switching s for individual as well as integrated environment can replace the normal Tran analysis as peak to peak mismatch are within the 10 % tolerable limit. The proposed approach can replace the normal analysis for predicting the feasibility of supply sharing for non-switching s. Moreover it has been observed that for certain low voltage range (few mv) there exists a correlation between linear and nonlinear analysis. The mismatch during transient remains an open question while after settling time frequency and time domain shows good matching. Analysing simplest PDN shows the effect of LC resonance apart from IR drop and Ldi/dt noise. It can be concluded that the S-parameter based Analysis for integration of power supply can replace the normal analysis procedure for switching and non-switching linear time invariant s. The work done in this dissertation has given an accurate, numerically robust, and computationally efficient frequency domain-based approach for computing the power supply noise (PSN). Moreover the approach has been framed to predict the supply noise for a block without simulating the actual block but by utilizing the concept of Scattering(S) Parameter and the output impedance.

6.2 FUTURE WORK:

The methodology is limited to the switching and non-switching analog blocks. There is a scope to extend the proposed approach for the mixed signal as well as digital s, thereby making it more generic. Moreover the cause of mismatch during initial time before settling period needs to be resolved.

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