Current Feedback Based Voltage Regulator For Non-Volatile Memories

by

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CERTIFICATE

This is to certify that the thesis titled ‘‘Current Feedback Based Voltage Regulator for Non-Volatile memories’’ being submitted by Bhawana Singh Nirwan (Roll No. - MT 13152) to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original work carried out by her under my supervision. In my opinion, thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in the thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

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ABSTRACT

Non-volatile memories have continued to retrieve their stronghold presence in the electronic industry wherever memory intensive applications are required. The present technologies like Flash have dominated the industry for so long. However there is a continuous shrinking of the technology nodes and now reaching the edge. This shrinking leads to challenging design of the floating gate devices used in Flash memories. The number of electrons stored in the floating gate decreases. As a result, there is a continuous focus on emerging trends and solutions to replace the existing technologies.

Phase change memories (PCM) have shown a growing trend in the recent years. It exploits the concept of the phase transition of a chalcogenide material from amorphous to crystalline. PCM characteristics approximate those of DRAM and Flash memories, making it their strong competitor. Its main advantages are large cycling endurance, fast program and access time and extended scalability.

In this dissertation, a voltage regulator has been developed in 110nm BCD9s technology for high voltage management with reference to phase change memory system. The error amplifier of the regulator is a three-stage operational amplifier designed to achieve a high gain with a sufficient phase margin. The voltage regulator is capable of regulating a wide voltage range, which is made possible by using a current based feedback system for the regulator. The varying current feedback enables to vary the feedback to the op-amp, providing a variable regulation scheme. The regulator provides a minimum granularity of 100 mV starting from 1.2 V onwards. The feedback current has a minimum granularity of 1 µA supporting the 100 mV step of the regulator.

PUBLICATION

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1. INTRODUCTION

1.1 INTRODUCTION TO PHASE CHANGE MEMORIES

Phase change memories (PCM) are being considered as a strong candidate in competition to the existing flash memories in the non-volatile memory solutions. All this is possible due to its fast read and write times, high write endurance of about 10^{12} cycles and higher retention time. It also offers the advantage of bit-by-bit data write to the memory.

1.1.1 PCM CELL STRUCTURE AND ITS OPERATION

The PCM cell comprises of a resistor (heater) and a selector transistor. The resistor is essentially made of a phase-change chalcogenide material present in two different phases, namely amorphous and crystalline. A large difference in resistivity exists between the two states, easily differentiating them. These two states are referred as SET (crystalline) and RESET (amorphous) states of the cell. Figure 1 shows the two states of the material. It shows the profile of two memory cells, one with the irregular amorphous state and the other with crystalline state. Figure 2(a) shows the transistor level representation of the memory element. M1 is the selector transistor to select the corresponding cell in the array [1]. WL and BL represent the wordline and the bitline of the array respectively. Figure 2(b) shows the current profile for the SET and RESET operations of the memory cell. Figure 2(c) depicts the structure of the crystalline and amorphous states of the memory cell. A memory cell is selected by driving the wordline and the bitline with voltage levels corresponding to the operation to be performed on the memory cell.

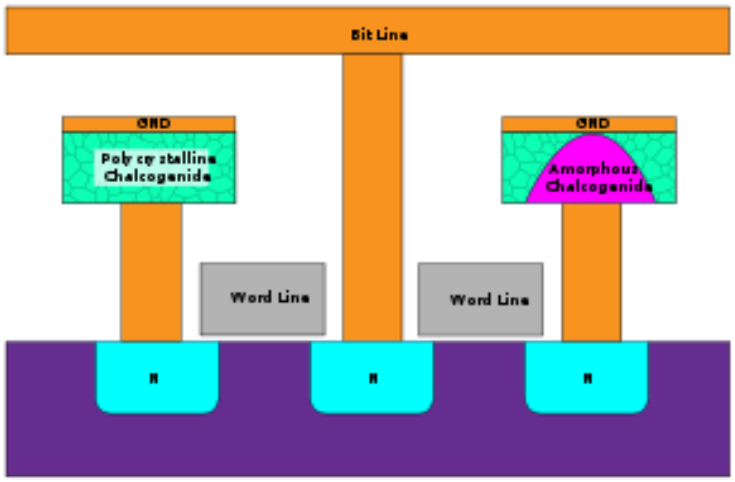
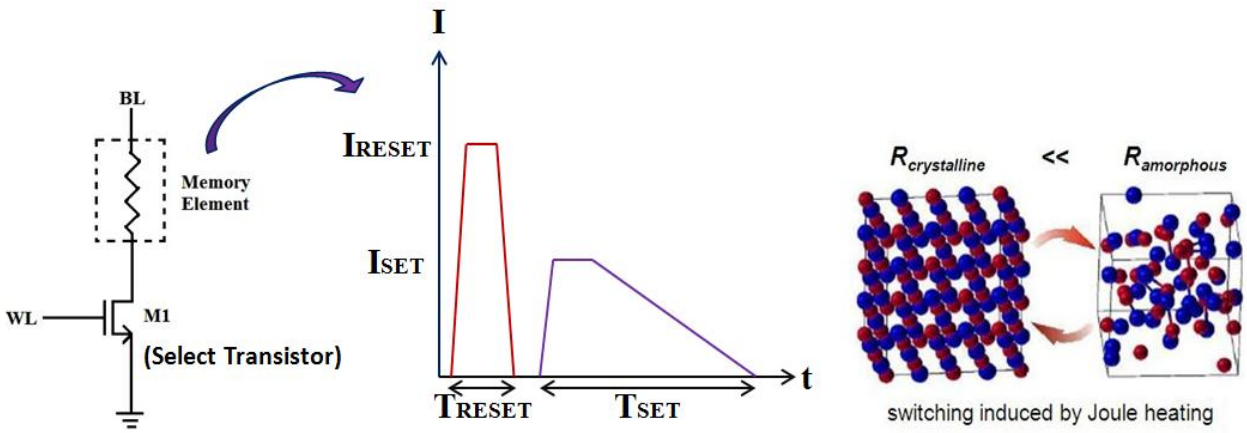


Fig. 1 PCM cell structure [https://en.wikipedia.org/wiki/Phase-change_memory]



(a) (b) (c)

Fig. 2 (a) PCM memory cell schematic (b) Current profile for the memory cell (c) Switching profile of memory cell between amorphous and crystalline

Programming is done by passing a high magnitude current pulse of the order of 700 μA for a duration of 50 to 100ns, followed by a sharp falling edge of the pulse. This process causes a Joule heating effect in the chalcogenide material, increasing its resistance and changing its state from crystalline to amorphous. The resistance of the two states ranges from kΩ to MΩ. Figure 3 depicts the temperature behavior of the PCM cell corresponding to the SET and RESET pulses [2].

Reading operation is done by biasing the cell at a lower read voltage and measuring the current through the memory cell against a reference current.

1.1.2 VOLTAGE REGULATION IN PCM

To achieve proper device operation, the memory cells require very accurate and stable biasing voltages. This is done by on-chip voltage regulators.
During the write operation, a PCM cell draws a huge current to change the phase of the chalcogenide material. If the cells are directly biased by charge pump, it may lead to an instability in the charge pump due to the sudden current drawn by the cells. It is of more concern when the cell stores multiple bits, as the currents injected into the memory element should be precise enough to achieve different resistance levels. This also justifies the presence of on-chip voltage regulator for the memory. The regulator should be efficient enough to provide the required cell current. Also, the sudden surge of current by the cell causes a drop in the regulated voltage. It must be ensured that the recovery time of the regulator is fast enough to prevent memory access time degradation.

Also during read operation, any biasing voltage fluctuations for the memory cell may result in an incorrect read, since the cell current is compared to the fixed reference current. The same biasing conditions should be ensured for both reference and the memory cells.

The word lines are biased at 1.8 V and 2.5 V during read and write respectively [3]. So the voltage regulator should be able to regulate these voltages. Also the circuit providing current for memory write operation runs on a higher regulated voltage supply [4]. This regulated voltage also has to support the bit line biasing voltage which goes up to 2.8 V during programming [3]. The voltage supporting the write operation may go up to 5.0 V depending on the memory architecture.

The specifications for the voltage regulator designed in the thesis work are listed in Table I.

Table I. Specifications of the regulator

Input Reference Voltage	1.2 V
Output Voltage	1.2 – 5.0 V
Output load	10 pF
Supply	1.8 V, 5.0 V

2. FUNDAMENTALS OF REGULATORS

2.1 TYPES OF VOLTAGE REGULATORS

A typical on-chip voltage regulator can be designed using two architectures as briefed below.

2.1.1 RESISTIVE LADDER BASED FEEDBACK

This variant uses a resistive divider based feedback to the regulator as depicted in Figure 3. The feedback network senses the output voltage and delivers a fraction of it to the input of the error amplifier through the resistive divider feedback network.

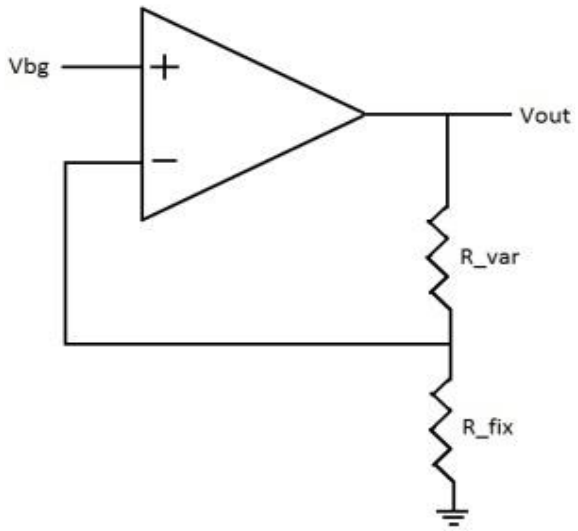


Fig. 3 Resistive ladder feedback based voltage regulator

The output voltage is realized by the reference voltage and the ratio of the resistors in the feedback network.

$$Vout = Vbg\ (\ 1 + \frac{R_{\_var}}{R_{\_fix}}) \quad (1)$$

Here, Vbg is the band-gap voltage used as a reference voltage for the error amplifier and $R_{\_var}$ and $R_{\_fix}$ are the voltage sensing resistors for the feedback network.
This design offers less flexibility to achieve variability in the regulated voltage. The resistor values once fixed by the designers cannot be further changed.Also resistors add to chip area and suffer from significant mismatch problem (due to process and temperature variations). The mismatch in the absolute value may be as high as +/- 25% [5]-[6]. Hence layout becomes challenging to achieve matching between resistors.

2.1.2 CURRENT DAC BASED FEEDBACK

The current DAC based voltage regulator uses a digital to analog converter that offers the flexibility of generating various levels of regulated voltages needed in the memory operations [7]. A desired feedback is given to the error amplifier based on the current generated by the DAC block (I_VAR) as shown in Figure 4.

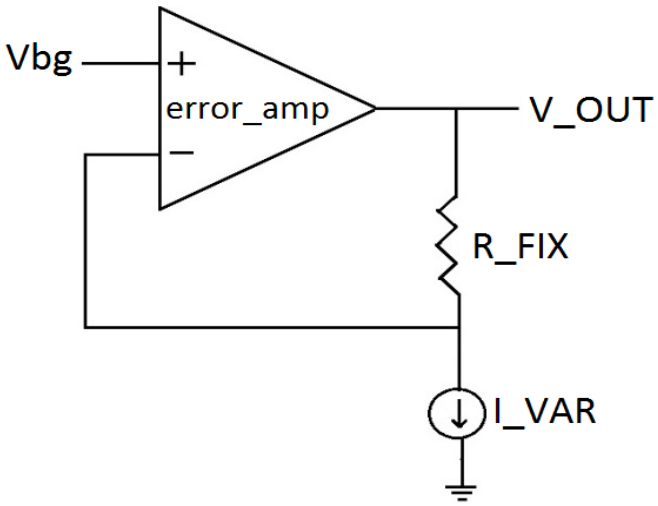


Fig. 4 Current DAC based voltage regulator

The output voltage of the regulator is given as :

$$Vout = Vbg + (R_{\_fix} * I_{\_var}) \quad (2)$$

Here, *Vbg* is the band-gap voltage used as a reference voltage for the error amplifier and $R_{_fix}$is the voltage sensing resistor for the feedback network. *I_var*is the DAC current whose value can be varied as per the requirements of the regulated voltage.

This work uses the current DAC based approach to design the voltage regulator. The error amplifier is realized using a three stage operational amplifier.

2.2 PARAMETERS OF VOLTAGE REGULATOR

2.2.1 LINE REGULATION

It is the ability of the regulator to maintain the output volatge at a specific level irrespective of any variations in the input volatge. Line regulation is expressed as the change in output voltage with respect to input voltage changes.

$$Line\ Regulation = \frac{\Delta V_{out}}{\Delta V_{in}} \quad (3)$$

Line regulation is a steady-state parameter and improves on inceasing the loop gain of the circuit.

2.2.2 LOAD REGULATION

Load regulation is the ability of the circuit to maintain the specified output voltage with varying load conditions. It is defined as :

$$Load\ Regulation = \frac{\Delta V_{out}}{\Delta I_{out}} \quad (4)$$

Output voltage variations occur when the load current drawn from the regulation transitions from zero to maximum allowable value or vice versa. An output voltage dip occurs at this sudden variation of the load current.

2.2.3 POWER SUPPLY REJECTION RATIO (PSRR)

Power supply rejection ratio is also termed as ripple rejection. PSRR is a measure of the regulator's ability to prevent the output voltage fluctuations caused due to supply voltage variations. PSRR is valid for the entire frequency spectrum of operation of the regulator. Hence it is sometimes also measured as a function of frequency.

2.2.4 EFFICIENCY

Regulator efficiency is a measure of its power transfer ability from the input to the output. Generally the regulator is designed to have minimum power dissipation. This results in maximum transfer of the power to the output.

$$\eta = \frac{P_o}{P_{in}} \tag{5}$$

Here P_o (V_o*I_o)is the output power delivered by the regulator and P_{in} (V_{in}*I_{in}) is the regulator input power.

3. LITERATURE SURVEY

3.1 VOLTAGE REGULATORS IN NON-VOLATILE MEMORIES

A lot of literature work is avaliable for voltage regulators. Regulators have been designed for a fixed voltage regulation as well as for variable voltage regulation. Regulator design depends on the loading seen by the regulator, i.e. current load or capacitive load. In both cases the output stage of the regulator differs due to the loading conditions. A regulator supporting current load has to ensure that the output stage is able to provide the necessary load current. If it fails to do so, then the regulator output voltage drops hence failing it purpose. In the case of capacitive load, the regulator should ensure that the settling time is not very long due to the loading. Long recovery or settling time may affect the critical circuits of the memory.

Regulators delivering a fixed regulated voltage have a fixed feedback circuit, generally a fixed resistive devider network. To support a range of regulated voltages, the resistive devider network in the feedback stage incorporates a variable resistor as discussed in section 2.1.1. As per the discussion, resistors occupy significant area of the design. Layout matching of the resistors becomes critical to avoid any mismatches in the feedback network, otherwise these mismatches in the feedback factor affect the gain of the error amplifier.

In order to lessen the above listed effects to a certain extent, one way is to use minimal resistors on the circuit so as to gain in terms of area. Also an alternate technique to vary the feedback factor can be adopted to have a more precise regulated voltage. So the current DAC based approach can be used to vary the feedback factor to achieve variable regulation. An on-chip precise reference current is already available in the designs. This current can be used in the DAC as the base current and then mirrored accordingly.

3.2 THREE-STAGE OPERATIONAL AMPLIFIER

A number of three-stage operational amplifiers have been presented in the literature. Some of the existing architectures are discussed further.

A three-stage amplifier with positive feedback compensation scheme is discussed in [8]. It is a low voltage op-amp working at a supply of 1.5 V and achieving a gain bandwidth of 2.7 MHz. It uses a feed-forward transconductance approach from first stage to the third stage. It provides a direct path from to the output at higher frequencies, boosting the bandwidth of the amplifier. It also uses a positive feedback around the second stage to control the damping factor of complex poles. The capacitor realizing this effect is such as to not limit the slew of the first stage. The transconductance of the third stage and feedforward-stage are set equal.

A three-stage amplifier with reverse-nested miller compensation technique is discussed in [9]. The design has been optimized to achieve an optimum setlling time for the amplifier. It also uses a feedforward transconductance stage to improve the transient response of the amplifier. Compensation capacitors from first stage to second and third stages have been used. A nulling resistor is used in order to eliminate the right-hand plane zero occuring in the design. This design also works on a low supply voltage of 1 V.

Both these architectures studied have been developed for low voltage applications. Also, keeping equal transconductance for the feed-forward stage and third stage does hamper the transient performance of the amplifier. This is due to the fact that these stages are driven by different signals and hence their transconductances should be adjusted so as to have optimum symmetry in the amplifier response.

3.3 OUTPUT AMPLIFIER

Output amplifiers are designed to efficiently drive proper signals to the load circuit. The performance of output amplifiers can be measured based on parameters like ac output resistance, output swing and the load capacitance. The output load may be resistive or capacitive in nature. To drive a low-resistive load, the output resistance of the amplifier should be lower than or equal to that of the load. In case of capacitive loading, the amplifier should have the ability to sink or source the required load current, while maintaining its performance. Some of the output stages studied are discussed further.

3.3.1 CLASS-A AMPLIFIERS

Class A amplifier can be realized essentially as a CMOS inverter with a current source load [10].The figure below shows the schematic of class A amplifier. The output current will be limited by the maximum sourcing current of the PMOS device. The output current is also limited by the slew rate performance of the load capacitor.

$$|I_{out}| = C_L \, (dv_{out}/dt) \tag{6}$$

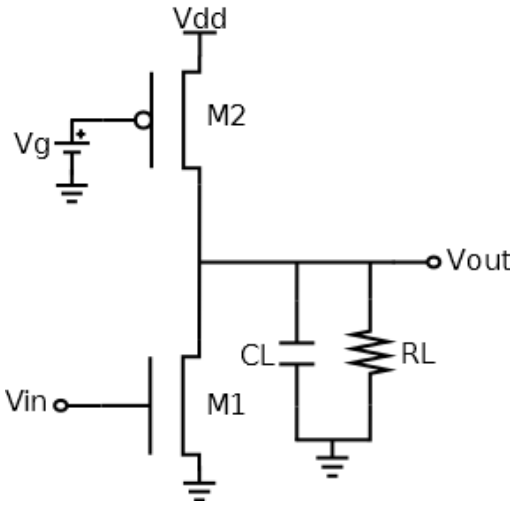


Fig. 5 Class A amplifier circuit diagram

Where, (dv_{out}/dt) is the slew rate. Also, if the load resistance R_L is low enough, it steals a portion of the charging current from the capacitor, affecting the performance. The maximum efficiency offered by class A amplifier is 25%.

3.3.2 SOURCE FOLLOWER

The source follower or the common drain configuration offers significant current gain and low output resistance [10]. It can be used to implement an output amplifier. Figure 6 shows the two variants in which source follower topology can be implemented. However it has certain limitations like the prominance of body effect which modifies the output voltage, making it lower than the supply (Vdd). Here, the maximum output-current sourcin gis

determined by M1 and V_{in} whereas current sinking is determined by M2. Its efficiency is similar to that of class A amplifier.

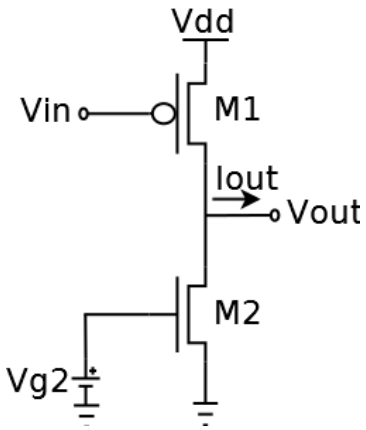


Fig. 6 Source follower with a current sink load

3.3.3 PUSH-PULL COMMON SOURCE AMPLIFIER

The push-pull topology offers better efficiency as compared to the two topologies discussed above [10]. Figure 7 shows the push-pull topology design. The input signal is common to both the pull-up and pull-down transistors. The entire current of the output stage is stirred completely in one direction, from supply to load or from the load to the ground. No current is wasted as only one device is active at a time, either pull-up or pull-down. It also offers a symmetric output voltage curve, hence improving the performance of the output stage.

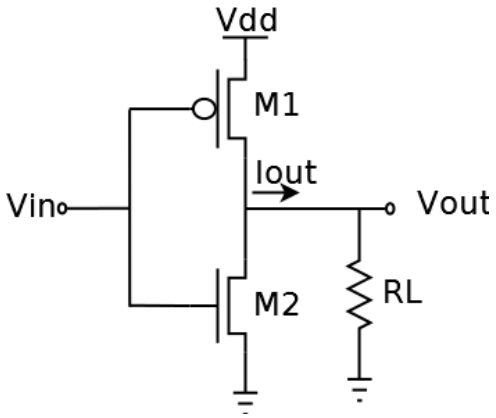


Fig. 7 Push-pull source follower circuit

4. DESIGNING OF REGULATOR

The regulator is designed and simulated using 110nm BCD9s process. The building blocks of the regulator include the error amplifier, current DAC and the feedback resistance. A three-stage operational amplifier topology has been chosen for the regulator design to meet the high gain and swing requirements.

4.1 ERROR AMPLIFIER DESIGN

The error amplifier is designed using a three-stage operational amplifier. The idea here is to achieve maximum gain from the first stage and then do a low to high voltage conversion using the second stage. The final stage of the amplifier provides the desired swing.

4.1.1 FIRST STAGE: FOLDED CASCODE

The first stage of the op-amp is realized using a folded cascode topology. It gives the advantage of a good input common mode range and a higher gain, comparable to the gain of a conventional two-stage operational amplifier. A cascode current mirror is used at the output stage for a higher gain [10]-[11]. The transistor level implementation of the design is depicted in Figure 8. Transistors M3 and M4 are the current sources supplying currents I1, I2 and I3, I4 respectively. The currents are decided such that the dc current in the cascode mirror is never zero so as to avoid the delay for the mirror to turn on again. These current values decide the biasing voltage for the pmos current sources. The biasing voltage (V_{bn}) of the cascode current mirror should ensure that both M8 and M10 transistors remain in saturation. The minimum biasing voltage for this cascode is:

$$V_{bn} = V_{GS8} + (V_{GS10} - V_{TH10}) \quad (7)$$

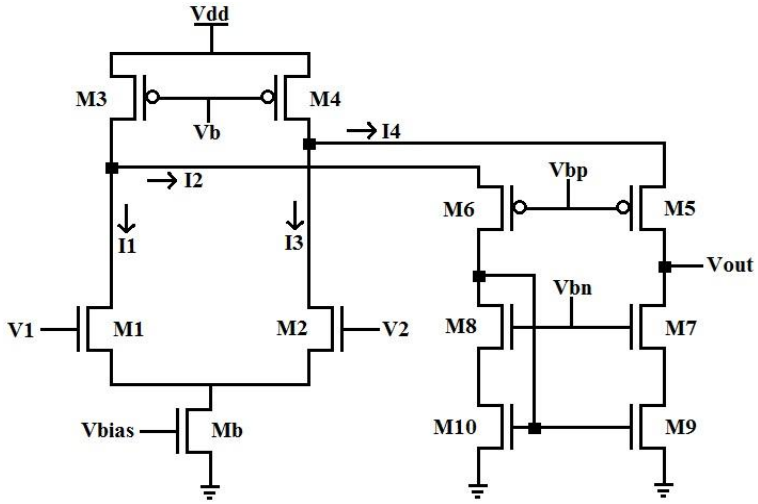


Fig. 8 First stage folded cascode schematic design

The small signal current through cascode current mirror is given by:

$$i_{10} = -g_{m1}\,(r_{ds1} || r_{ds3})v_{in}/2[R_A + (r_{ds1} || r_{ds3})] \tag{8}$$

$$i_{10} \approx -g_{m1}v_{in}/2 \tag{9}$$

Where, R_A is the resistance looking into the source of M6. The current through M5 is given by:

$$i_5 = \frac{g_{m2}(r_{ds2} || r_{ds4})v_{in}}{2[(R_7/g_{m5}r_{ds5}) + (r_{ds2} || r_{ds4})]} \tag{10}$$

$$i_5 = \frac{g_{m2}v_{in}}{2[1+(R_7(g_{ds2}+g_{ds4})/g_{m5}r_{ds5})]} \tag{11}$$

$$i_5 = \frac{g_{m2}v_{in}}{2(1+k)} \tag{12}$$

Where, k is known as a low frequency unbalance factor given by:

$$k = \frac{R_7(g_{ds2} + g_{ds4})}{g_{m5} r_{ds5}} \tag{13}$$

Hence the gain of this folded cascode op-amp is given as the total current flowing through the output resistance R_{out} .

$$\frac{v_{out}}{v_{in}} = [(g_{m1}/2) + (g_{m2}/2(1+k))]R_{out} \tag{14}$$

$$A_v = [(2+k)/(2+2k)]\, g_{m1} R_{out} \tag{15}$$

The output resistance, R_{out} , is given by:

$$R_{out} \approx g_{m7} r_{ds7} r_{ds9} || [g_{m5} r_{ds5} (r_{ds2} || r_{ds4})] \tag{16}$$

As can be deduced from the gain equation of the folded cascode op-amp, significant gain is achievable, provided that the biasing currents and bias voltages are proper.

4.1.2 SECOND STAGE: COMMON SOURCE

The second stage of the design is the common source topology of nmos input type. The small signal first stage perturbations are fed through a current mirror to the second stage which is then being amplified. This stage is driven by a 5V supply. A single level of cascoding is used at this stage to prevent safe operating area (SOA) violations of the transistors.

4.1.3 THIRD STAGE: CLASS AB OUTPUT STAGE (PUSH-PULL)

The output stage for the three stage op-amp is symmetric push-pull class-AB stage [12]. The pull down transistor of this stage is driven by the output of the first stage introducing a feed-forward transconductance stage [8]. Conventionally, the pull-up and pull-down transistors have the aspect ratio such that their transconductance is equal to achieve symmetric operation. However this result in an asymmetry in the positive/negative op-amp step response

as the driving signals for both pull-up and pull-down are different [12]. Therefore the aspect ratio has to be increased further in order to achieve symmetric response and compensate for the difference in the driving signals for the duo, along with carrier mobility.

Figure 9 shows the final block diagram of the voltage regulator. It includes the error amplifier, the feedback resistance and the current feedback mechanism using a current DAC (digital to analog). The error amplifier is driven by two supplies, 1.8 V and 5.0 V.

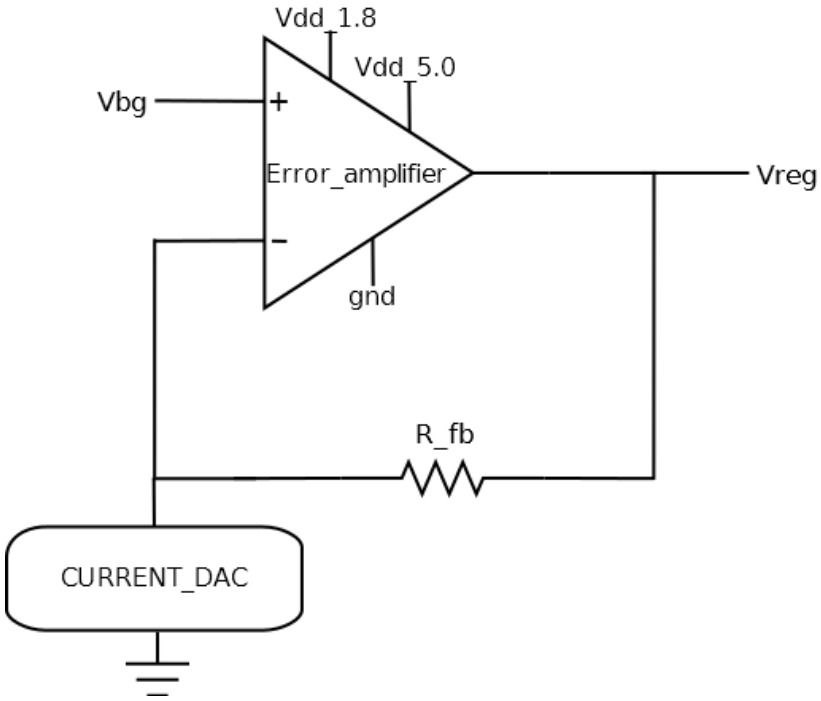


Fig. 9 Block level diagram of proposed regulator showing the operating supply voltages

4.1.4 FREQUENCY COMPENSATION

Figure 10 shows the transistor level circuit of the three-stage operational amplifier used as an error amplifier. Poles are to be identified which affect the frequency response of the op-amp. Nodes A and B offer non-dominant poles. The poles at node Vout, Vo1 and node D significantly affect the frequency response. Considering along with the load of the circuit, the output nodes contributes a dominant pole. The value of this dominant pole is given as below:

$$P_1 = \frac{1}{R_{load} * C_{load}} \tag{17}$$

Where R_{load} and C_{load} are the load resistance and load capacitance (total parasitic and load capacitance of output stage) of the circuit respectively. The load resistance can be calculated as given below:

$$R_{load} = r_{ds15} \,||\, r_{ds16} \tag{18}$$

The uncompensated AC and transient responses of the op-amp are shown in figures below. Figure 11 shows the AC response. The presence of three poles in the system can be easily inferred from the phase response of the op-amp. As mentioned above, the poles at output node, Vo1 node and node D affect the frequency response. Also, the transient behavior shown in figure 12, suffers from ringing significantly. The overshoot goes as high as 160 mV. Similarly the undershoot goes as low as 210 mV below the desired response. The ringing in the circuit can be prevented by shifting the poles beyond

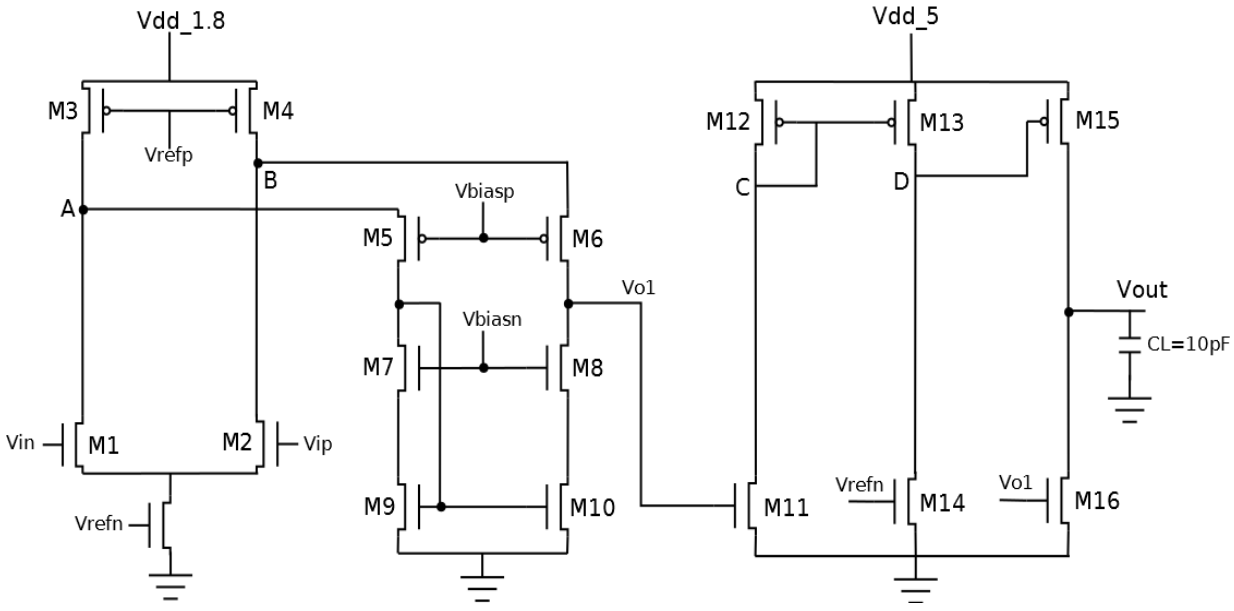


Fig. 10 Proposed circuit of uncompensated three-stage op-amp with load

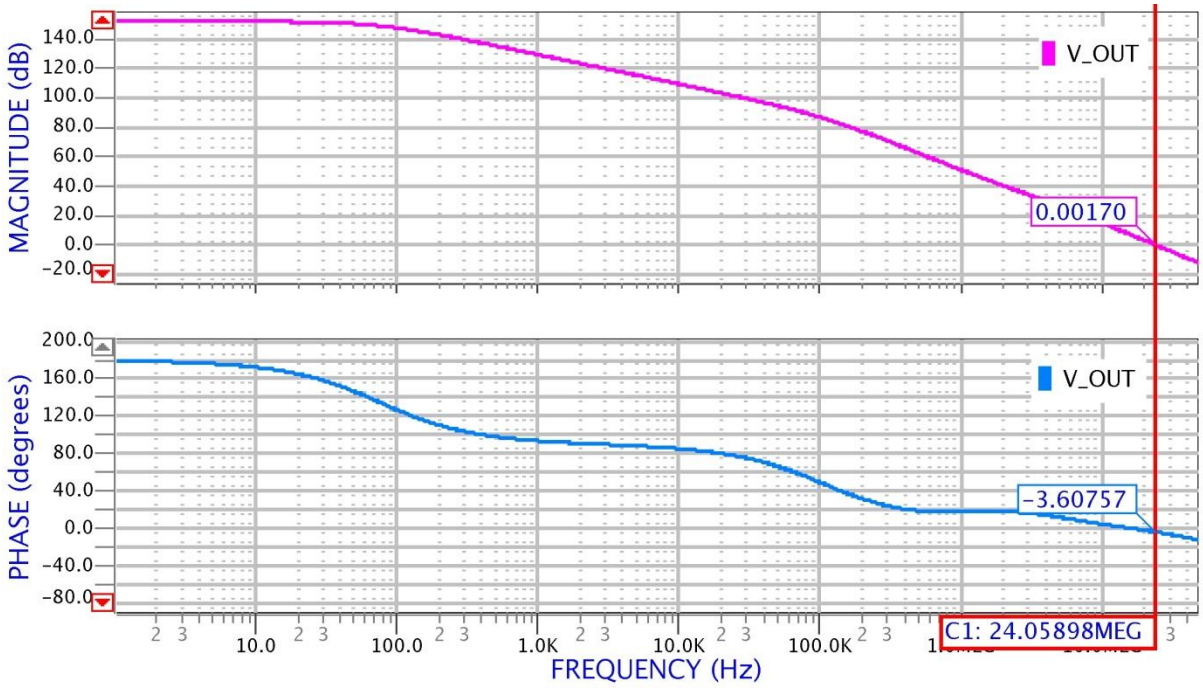


Fig. 11 AC response of the proposed uncompensated three-stage op-amp

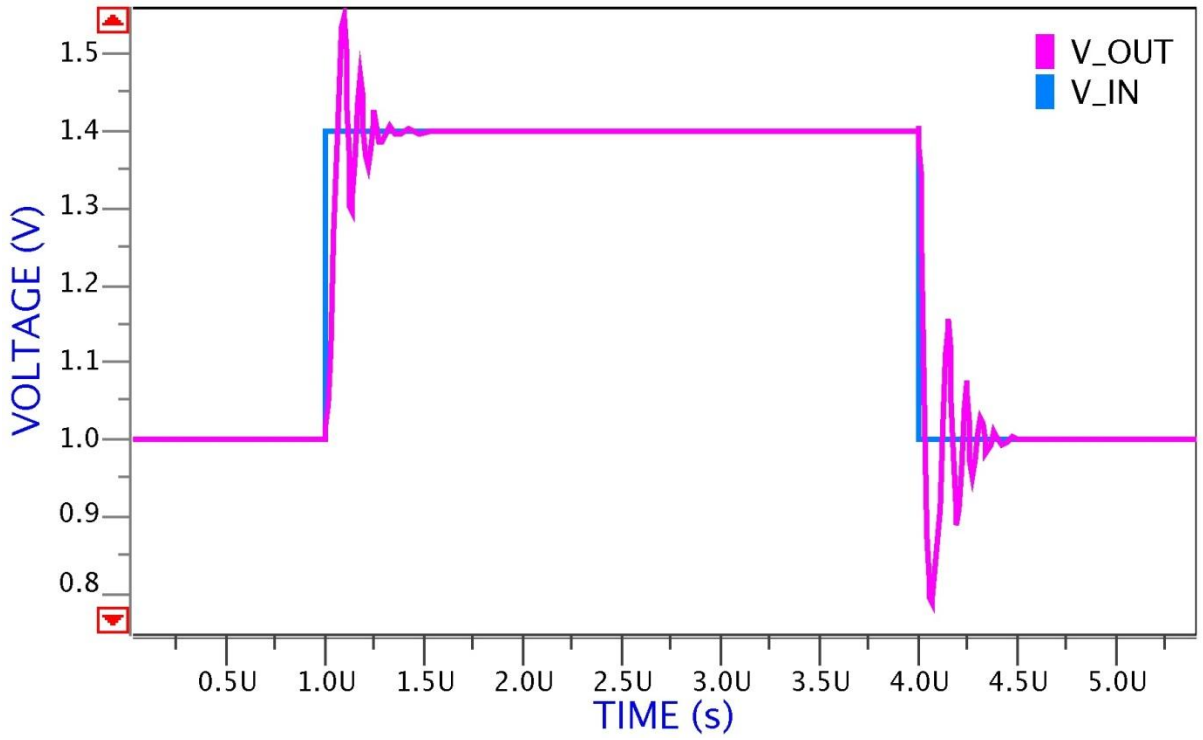


Fig. 12 Transient response of the proposed uncompensated three-stage op-amp

the unity gain frequency, so as to have only one pole inside the unity gain bandwidth. This idea can be also be used to achieve proper phase margin, making the system sufficiently stable. Nested miller compensation technique is used here to compensate the frequency response [13].The use of compensation capacitor for the feedback path also tends to introduce parasitic zero in the right half plane (RHP) which degrades the phase margin of the response [14]. This right hand plane zero can be eliminated by introducing a nulling resistor connected in series with the compensation capacitor. The value of this nulling resistor is calculated as below:

$$R_z = \frac{1}{g_m} \tag{19}$$

Where, g_m represents the transconductance of the gain stage across which the resistor is to be connected in series with the compensation capacitor C_c.

The compensation capacitors (C_{c1} and C_{c2}) are connected from output of stage one and stage two to the final output node of the op-amp. The compensated response is discussed in the results section.

4.2 REFERENCE CURRENT GENERATION CIRCUIT

A constant current reference circuit has been designed to supply the internal biasing currents of the three-stage op-amp. The reference generation circuit uses the combination of proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) circuits [15]. The reference current (I_{ref}) is the sum of PTAT and CTAT currents. The circuit offers almost zero temperature coefficient. The schematic of the reference circuit is shown in figure 13.

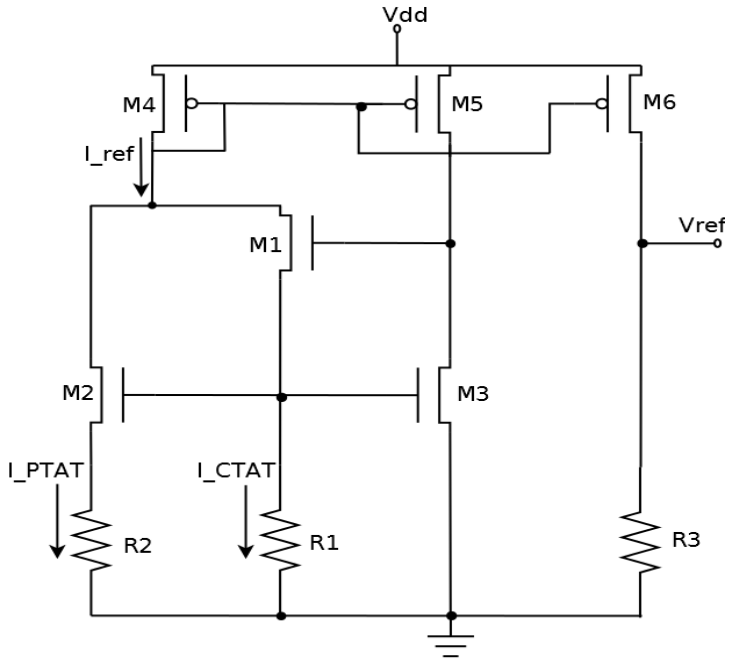


Fig. 13 Voltage reference circuit

In this circuit, transistors M1, M3 and R1 generate the I_{CTAT} current whereas transistor M2 and R2 generate the I_{PTAT} current. Transistor M4 sums the I_{CTAT} and I_{PTAT} currents to generate the reference current. This reference current is further mirrored to transistor M6 to generate a reference voltage across the resistor R3. The value of R3 can be chosen to get a desirable reference voltage from the circuit.

Here, the transistors M3 and M2 operate in weak inversion region to realize the exponential current behavior. The gate-source voltage of transistor M3 can be calculated using the current equation in weak inversion region, given as below:

$$V_{gs_{M3}} = nV_T \, ln\,(I_{ds3}.L_3/I_t.W_3) + V_{th} \tag{20}$$

Here,I_{ds3} is the drain current of M3, L_3 and W_3 are channel length and width of the transistor respectively,$I_t$is the MOSFET saturation current and V_{th} is the threshold voltage. $V_T$is the thermal voltage given by the equation:

$$V_T = \frac{kT}{q} \tag{21}$$

Here k is defined as the Boltzmann's constant, q is the electric charge and T is the absolute temperature.

The reference current is expressed as:

$$I_{ref} = \frac{Vgs_{M3}}{R1} + \frac{nV_T}{R2} \ln m \tag{22}$$

Here, n is the slope factor of the transistor, V_T is the thermal voltage as mentioned above, R1 and R2 are the resistors as mentioned above and m is the aspect ratio of transistors M2 and M3.

This reference current is mirrored through transistors M5 and M6. The reference voltage is the product of current given by transistor M6 and the resistance R3, obtained as follows:

$$V_{ref} = I_{ref} * R3 \tag{23}$$

In this design, a reference current of 1µA is generated. The transistor M6 gives a reference current of 1 µA which is then mirrored (5 µA) to the biasing transistors of the op-amp.

5. RESULTS AND DISCUSSION

The proposed circuits in this work have been designed in BCD9s technology using Cadence schematic editor tool and simulated using ELDO spice circuit simulator. Two voltage supplies have been used. The second and final stage of the error amplifier are driven by 5 V supply. Rest all circuits are driven by 1.8 V supply. The design has been evaluated across five process corners (slow-slow, fast-fast, slow-fast, fast-slow and typical for n-p devices) at three temperature levels of -40 °C, 25 °C and 150 °C. The nominal simulation setup includes typical process corner for both nmos and pmos transistors, at 25 °C temperature.

The following sections include the simulation results of the error amplifier (three-stage operational amplifier) including its various performance parameter measurements, biasing circuit and the final voltage regulator.

5.1 THREE STAGE OP-AMP PARAMETERS

The three-stage op-amp designed and discussed earlier has been evaluated for its various performance parameters. The results are shown below.

5.1.1 AC ANALYSIS

The ac analysis of the op-amp is done with the op-amp in unity feed-back configuration. The gain and phase margin of the op-amp versus frequency are evaluated and depicted in figure 14. Table II summarizes the gain, phase margin and unity gain bandwidth (UGB) details of the op-amp across process variations at nominal temperature of 25 °C.

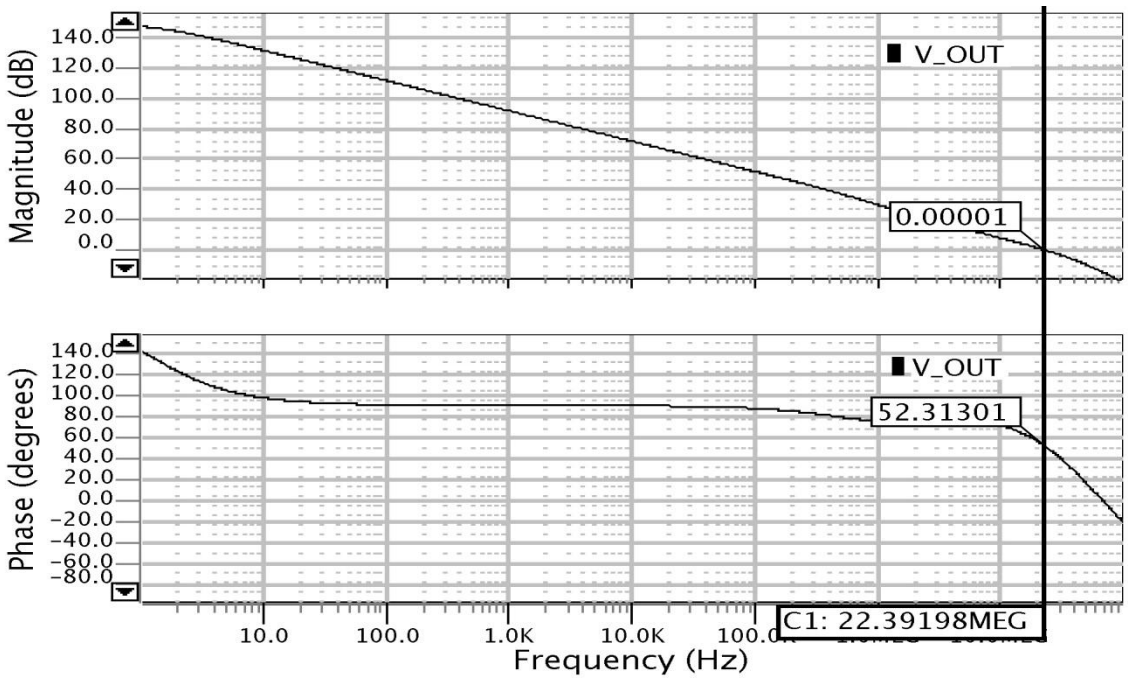


Fig. 14 Phase and magnitude plots for the compensated three-stage op-amp

TABLE II Gain, phase margin and UGB across process variations

CORNER	GAIN (dB)	PHASE MARGIN (°)	UGB
TYP	147.43	52.37	22.35
MIN	141.65	52.28	19.71
MAX	145.69	52.44	24.43
SFA	142.81	54.19	21.11
FSA	144.31	51.44	22.34

5.1.2 INPUT COMMON MODE RANGE (ICMR)

The ICMR measurement is done by applying variable DC voltage at the input of op-amp. The op-amp is used in unity gain closed loop configuration. The ICMR plot is shown in Figure 15, with ICMR of 2.105V ranging from 0.260V (ICMR min) to 2.365V (ICMR max). Input voltage applied beyond this range leads the op-amp out of saturation resulting in an undesirable performance.

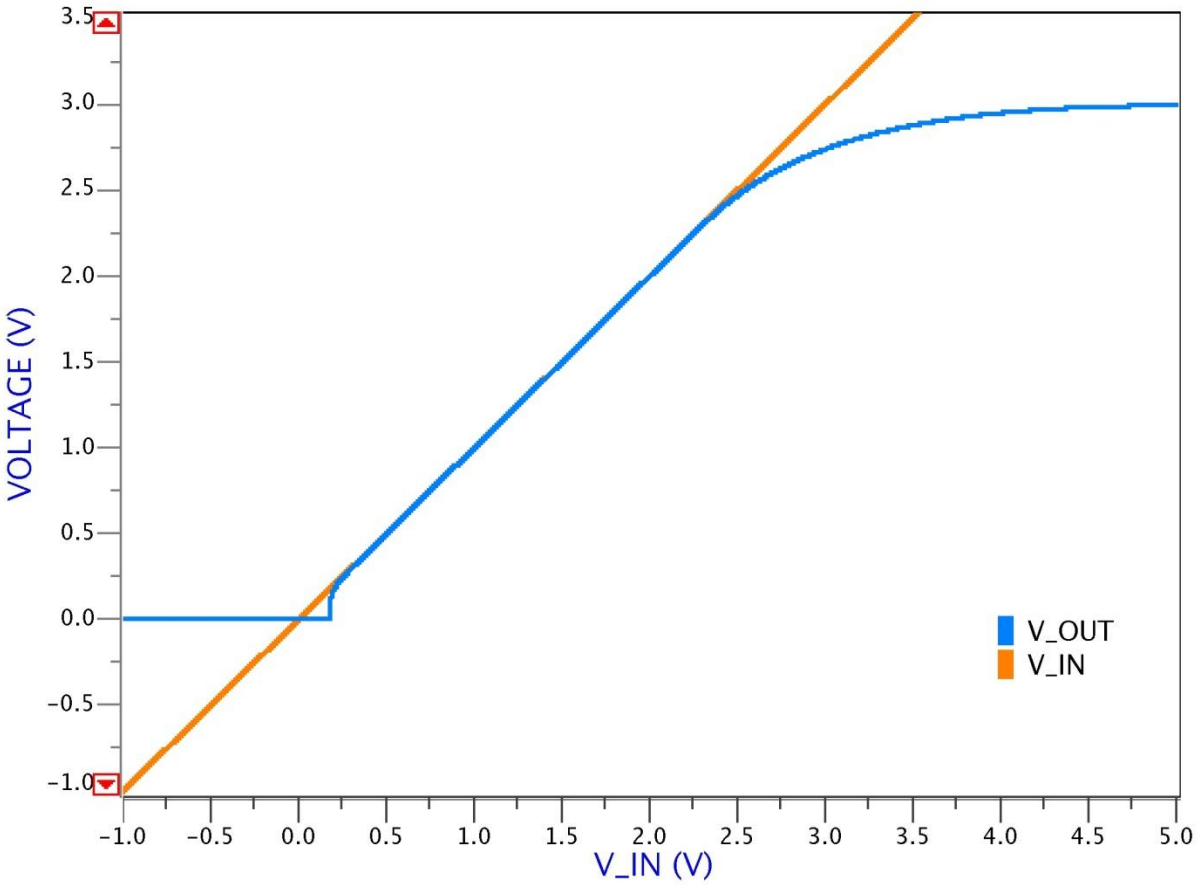


Fig. 15 Linear operating range of proposed three-stage op-amp

5.1.3 OUTPUT VOLTAGE SWING

The output voltage swing of the amplifier corresponds to the linear part of the transfer curve when the op-amp is used in the high gain configuration. This corresponds to the maximum range in which the output voltage can vary keeping the op-amp in saturation. The figure below depicts the output voltage swing of the designed op-amp. It corresponds to an output swing of 4.996V.

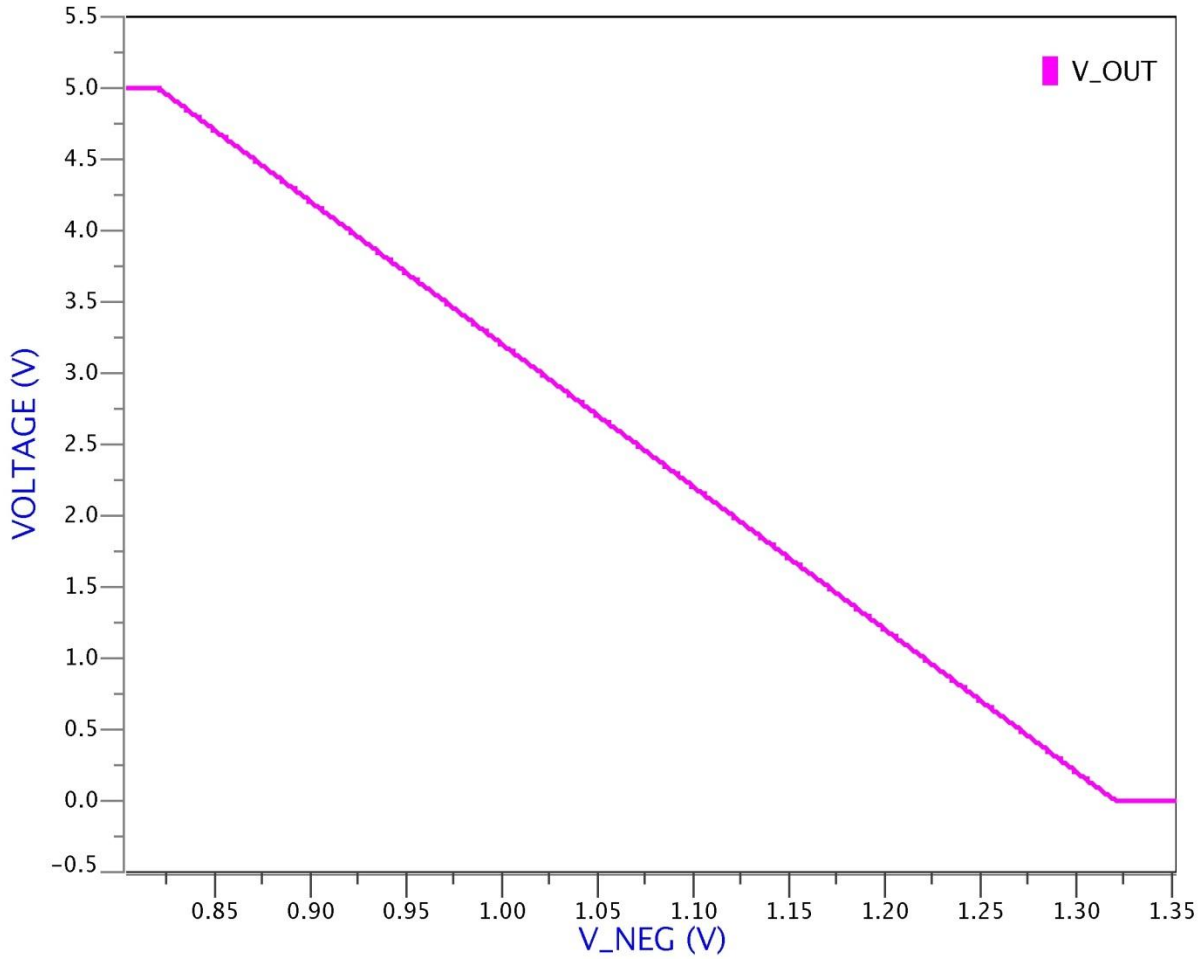


Fig. 16 Output voltage range of the three-stage op-amp

5.1.4 TRANSIENT ANALYSIS

Transient analysis helps to evaluate the actual performance of the op-amp. Parameters like settling time and slew rate are calculated using the transient response of the op-amp. Transient response is observed by applying an input step signal. The design is evaluated in the presence of output loading of 10 pF for the op-amp. Figure 17 shows the transient behavior of the op-amp.

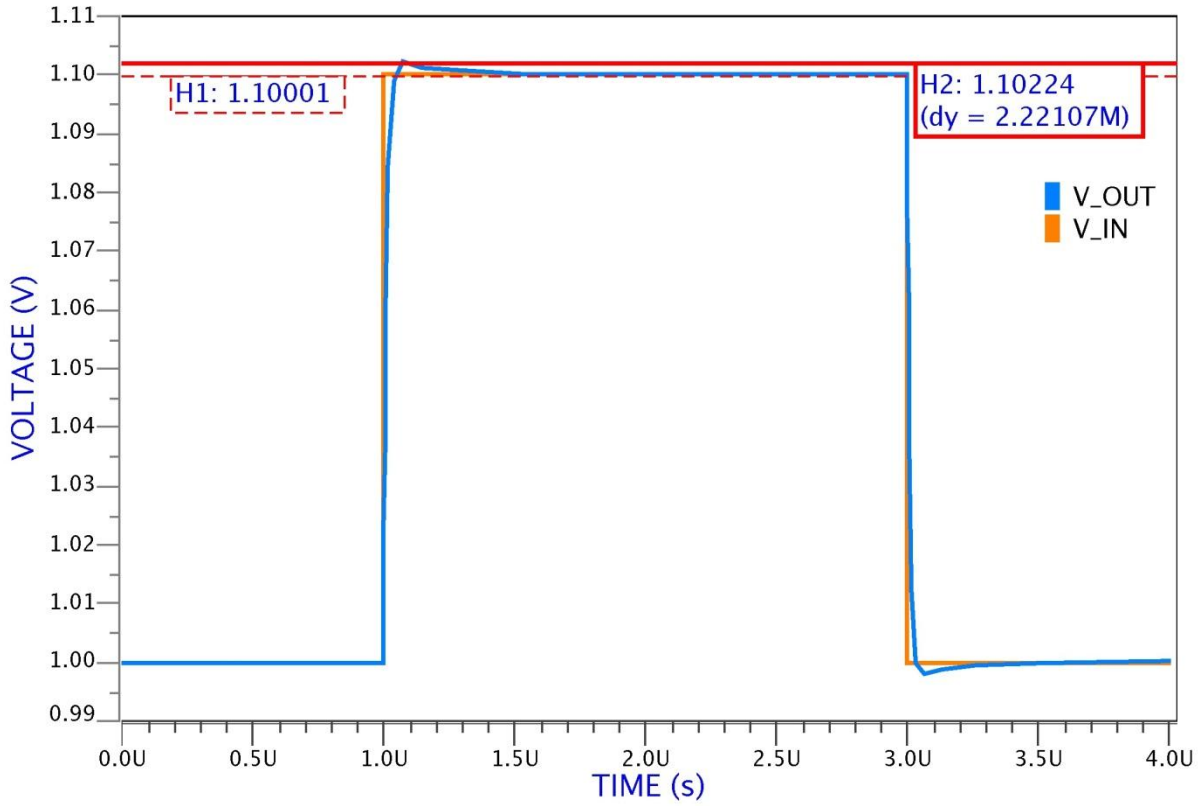


Fig. 17 Transient response of three-stage op-amp with step input

Here, the settling time for the considered input step of 100 mV is 87 ns. The op-amp achieves a settling time of 240 ns for larger step inputs. The positive slew rate comes out to be 4.56 V/µs and negative slew rate is 9.15 V/µs.

5.1.5 DC OFFSET

For a perfectly symmetric design and differential input of the op-amp, V_{in} = 0, the observed V_{out} = 0. But due to mismatches, the circuit offers a dc offset, which is the output value observed with zero differential input. A dc offset may limit the performance of the op-amp, reducing the precision of measurement. This may significantly affect the circuits like comparators which are used to compare the reference voltage and the input voltage and accordingly generate an output signal. Figure 18 depicts the input offset voltage of the proposed op-amp with zero differential input voltage at nominal condition. It can be inferred that the offset of the op-amp is approximately 408 nV. Figures 19-20 depict the Monte-Carlo analysis for offset measurement. Monte-Carlo analysis is done for 10000 runs across statistical corners for the design. It can be inferred that as opposed to 1.2 V, the output flips at

somewhat higher voltage than 1.2 V. The difference between the two is termed as the DC offset of the design as can be inferred from Figure 20. The mean DC offset is of 31.39 µV.

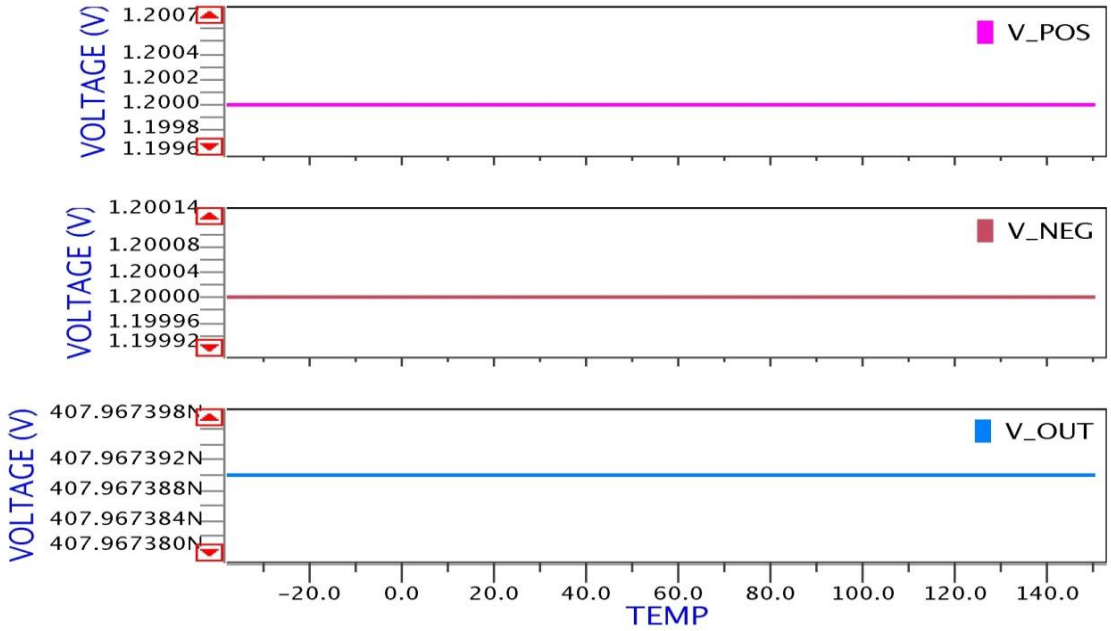


Fig. 18 Input offset measured at nominal condition (typical process corner and 25 °C temperature)

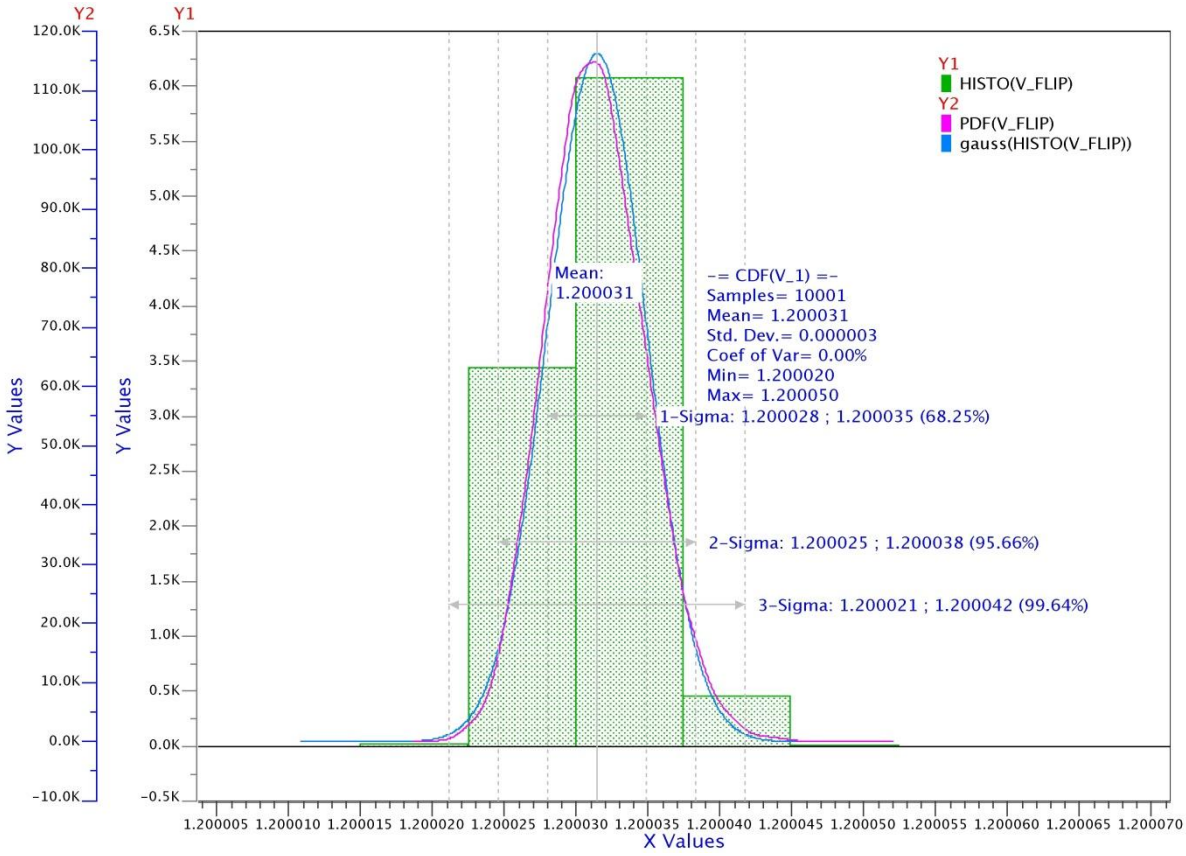


Fig. 19 Monte-Carlo analysis depicting input voltage at which output flips its polarity

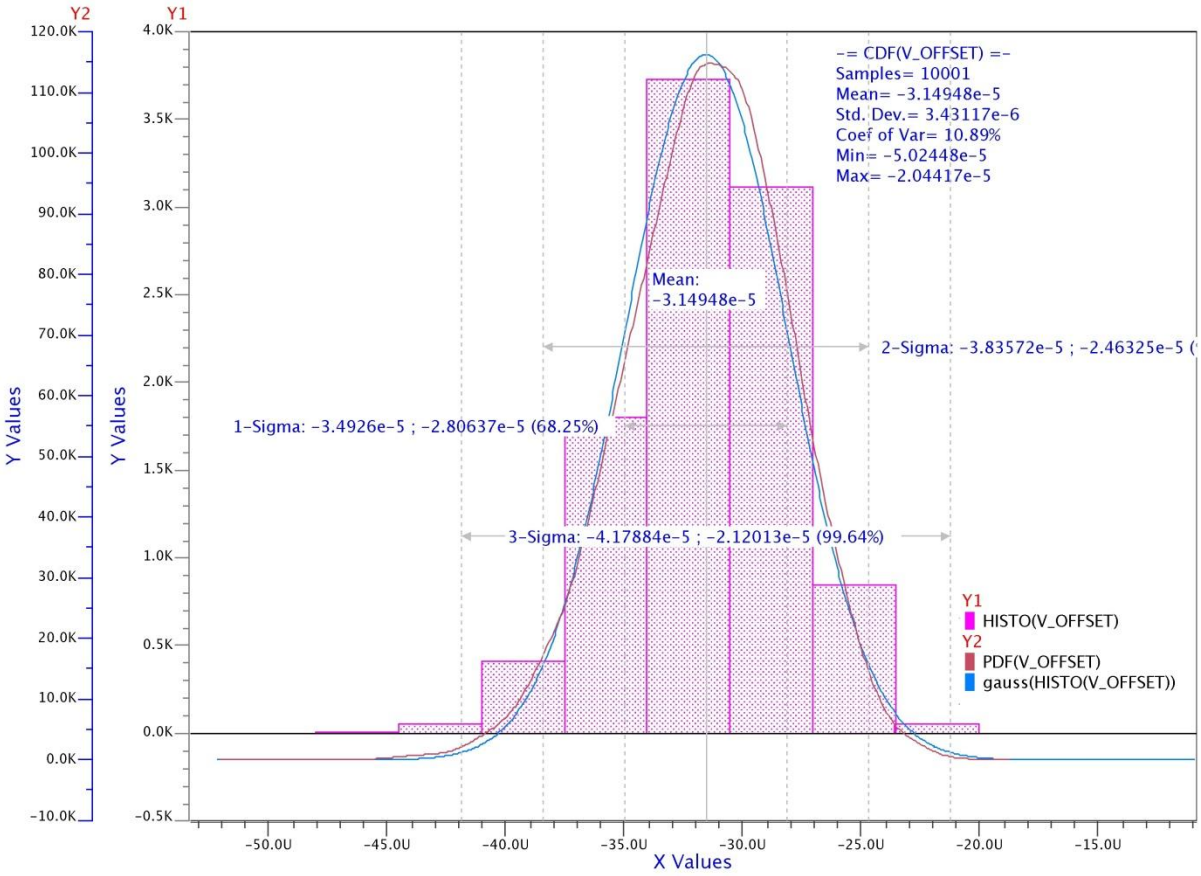


Fig. 20 Monte-Carlo analysis of the DC offset of the op-amp

Finally the performance parameters of the proposed three-stage operational amplifier are summarized in Table III. The listed parameters are measured at nominal simulation setup, i.e. typical process corner, 25 °C temperature, Vdd1v8 = 1.8 V and Vdd5 = 5.0 V.

TABLE III Measured performance parameters of proposed op-amp

Parameter	**Value**
Gain	147.43 dB
Phase margin	52.37°
UGB	22.35
Settling time	87 ns
Slew rate	9.15 V/µs
Load cap.	10 pF
Avg. current consumption	64.825 µA

5.1.6 BIASING CIRCUIT

The biasing circuit is designed to obtain a constant biasing current of 1µA independent of temperature under temperature variations from -40 °C to 150 °C. Current mirrors are further used to bias the op-amp stages. Figure 21 shows the currents with positive and negative temperature coefficients, I_{PTAT} and I_{CTAT} respectively. Both currents are summed up to produce the reference current I_{ref} as depicted in Figure 22. The reference current flows through the load resistor to give the reference voltage V_{ref}. Temperature independent reference voltage is shown in Figure 23. The design achieves a variation of +/- 2 mV for a reference voltage generation of 500 mV across the considered temperature range.

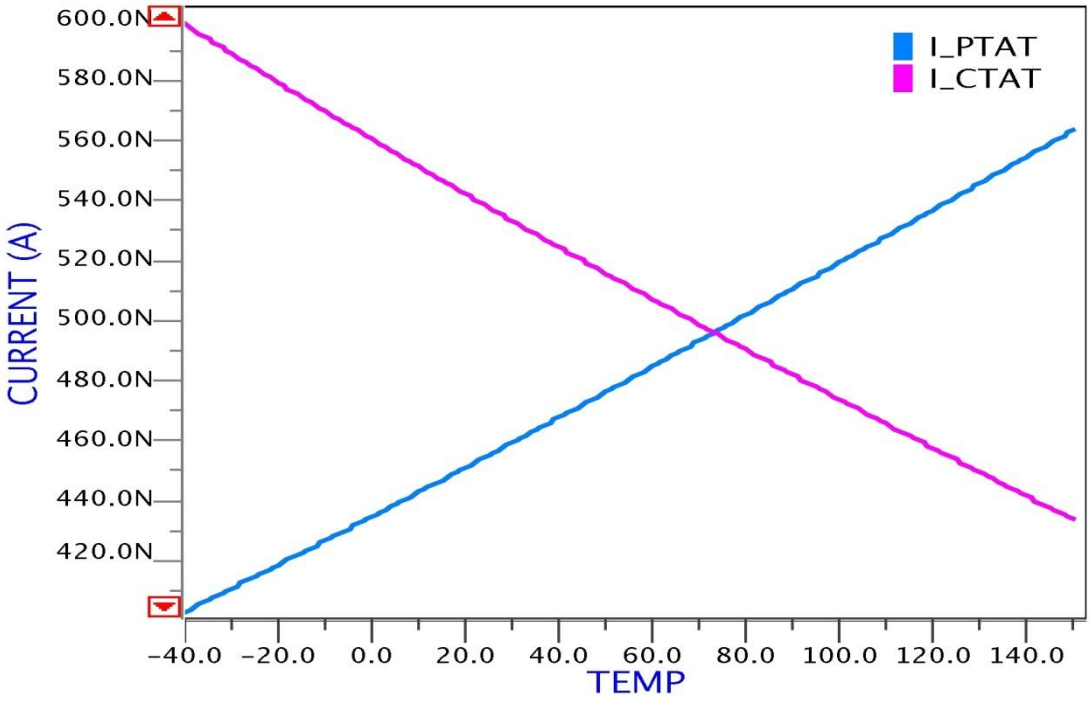


Fig 21 PTAT and CTAT currents as a function of temperature

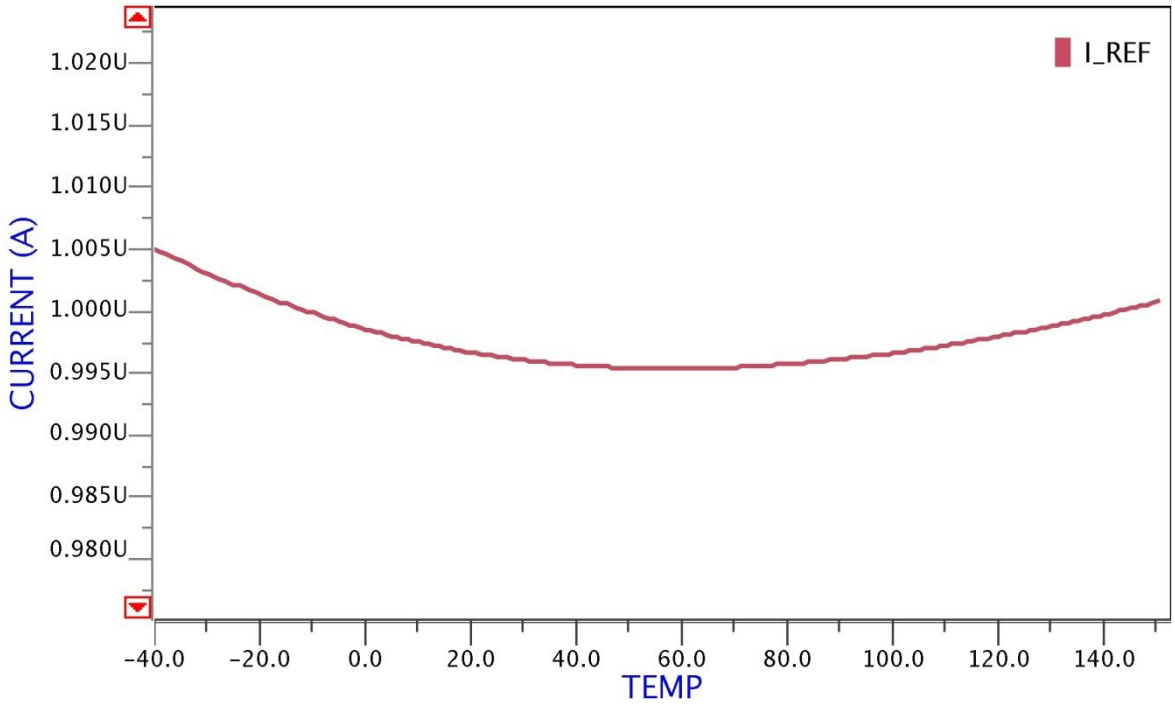


Fig. 22 Reference current as a function of temperature

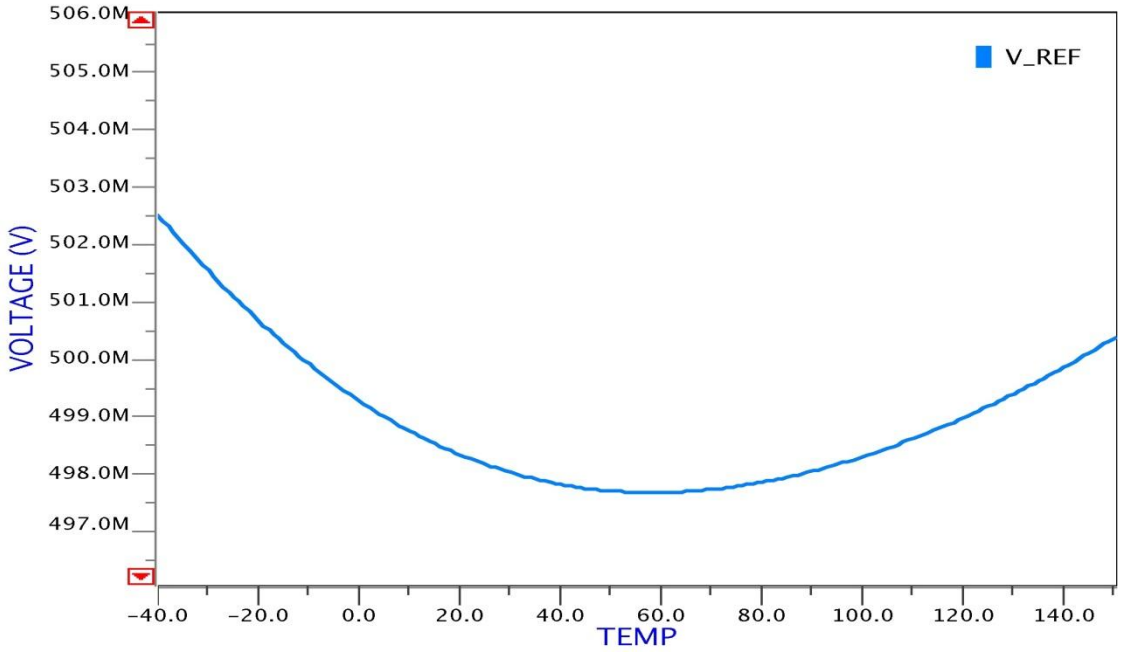


Fig. 23 Reference voltage as a function of temperature

Figure 24 shows the reference voltage as a function of the supply voltage. It can be inferred that the biasing circuit can be successfully operated for a supply voltage range from 1.5 V to 2.8 V. The upper limit of the supply voltage is set by the safe operating area (SOA) violation of the transistors which is 2.8 V for low voltage transistors in the used technology.

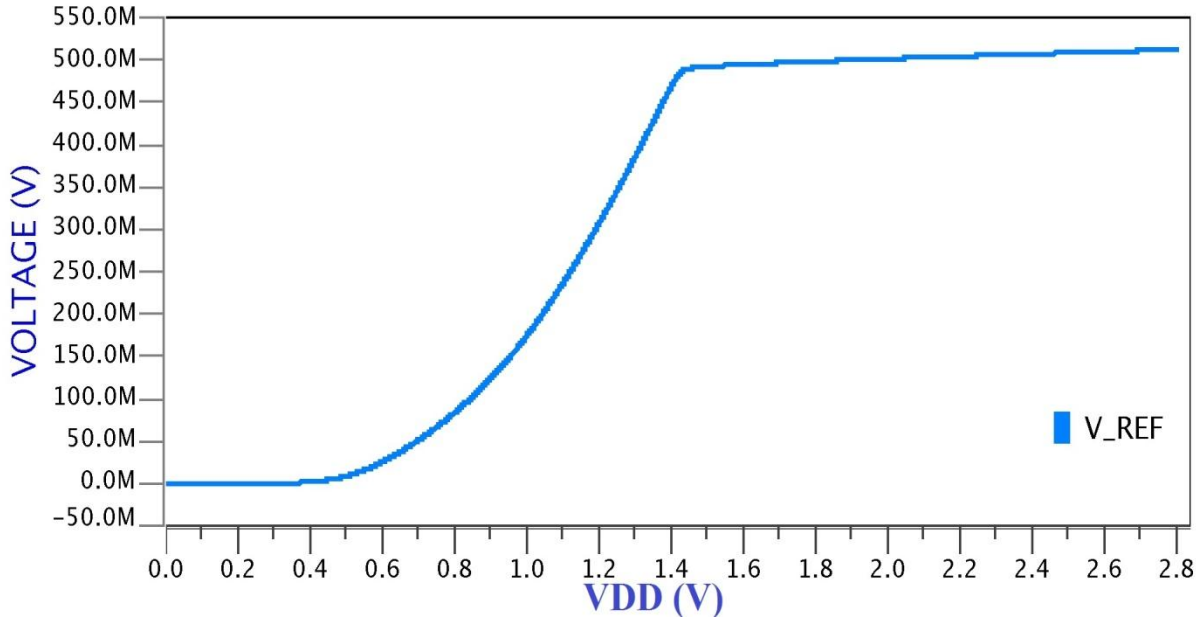


Fig. 24 Reference voltage as a function of supply voltage

5.2 VOLTAGE REGULATOR

This section includes the final results of the voltage regulator. The DAC current for the regulator is varied with a step of 1 µA. The feedback resistor has a value of 100 kΩ. Hence each step increase in the feedback current (DAC current) increases the regulated output voltage by 100 mV. Figure 25 shows an increase of 100 mV in the regulated voltage with increase of DAC current by 1 µA. It also depicts the maximum range of the regulated voltage that can be achieved. The upper limit on the output voltage is also put by the maximum supply voltage available to drive the circuit.

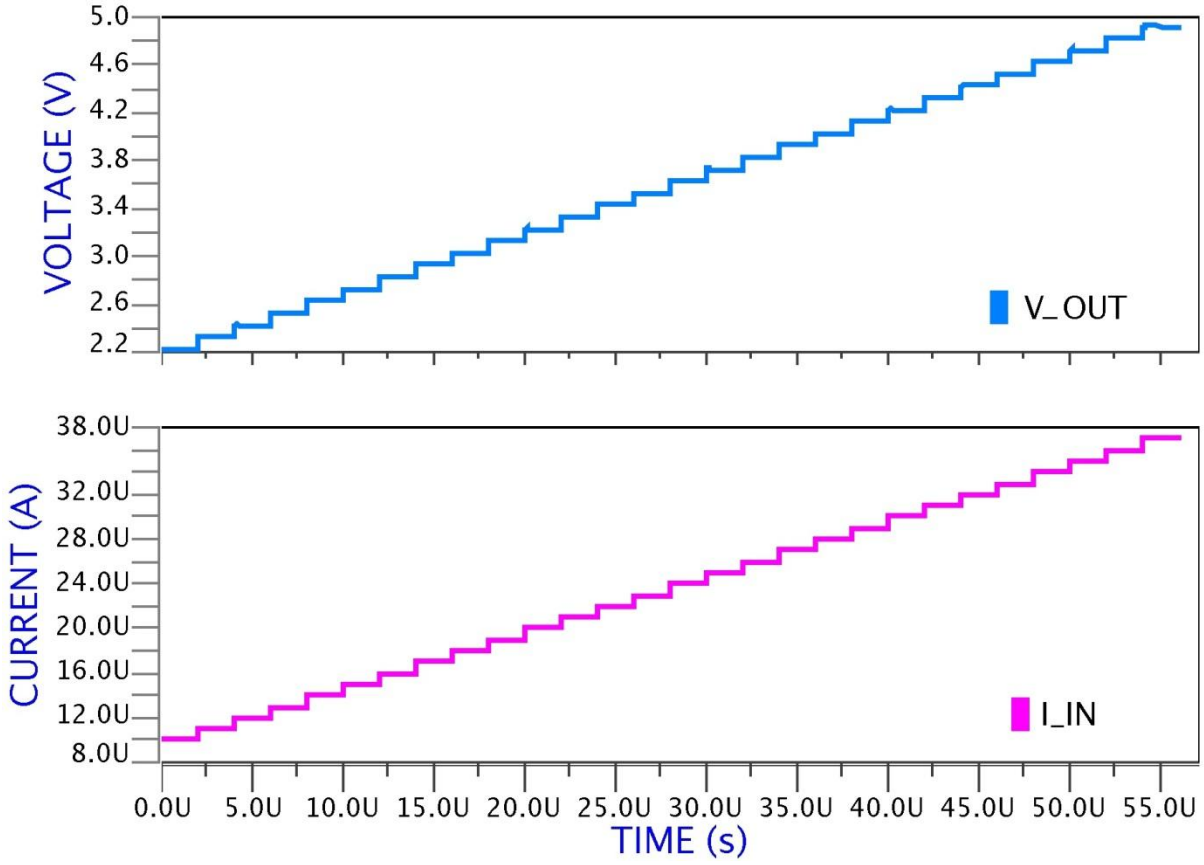


Fig. 25 Maximum regulated voltage that can be achieved for the proposed regulator

6. CONCLUSION

6.1 SUMMARY

In this work, voltage regulator architecture has been designed to have different levels of regulated voltages according to the type of operation to be performed on the memory. The design is done with reference to phase change memories (PCM), a growing technology for non-volatile storage. The design uses a current DAC based feedback architecture unlike the conventional resistive ladder based feedback, to achieve different modularity of the regulated voltage. The error amplifier is realized using a three-stage operational amplifier topology with nested miller compensation technique. A reference circuit has been designed to generate reference current for biasing the three-stage op-amp. The designs have been validated and simulated for variations across process and temperature. The proposed regulator offers a wide swing for the regulated voltage.

6.2 FUTURE WORK

This work focused on the design of the error amplifier and the biasing network. However, this work can be further extended by working on the design of current DAC block. In this work, an external current DAC was used for the validation of the regulator design.

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