# Identification of Weak Bits in SRAM

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For the degree of M.Tech in Electronics and Communication Engineering

# Student's Declaration

I declare that the dissertation titled "Identification of Weak Bits in SRAM" submitted by Gundu Anil Kumar for the partial fulfilment of the requirements for the degree of Master of Technology in Electronics and Communication Engineering is carried out by me under the guidance and supervision of Dr. M. S. Hashmi at Indraprastha Institute of Information Technology, Delhi and Mr. Anuj Grover at STMicroelectronics, Greater Noida. Due acknowledgements have been given in the report to all material used. This work has not been submitted anywhere else for the reward of any other degree.

..... Place and Date: …….....
G Anil Kumar

# CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

…….. ……
Dr. Mohammad. S. Hashmi Mr. Anuj Grover

# ABSTRACT

Up to 70% of Systems on a Chip (SoC) area are occupied by embedded memories. In order to achieve higher robustness, embedded SRAMs (eSRAM) are often used in SOC applications. However, due to advancement in technology it is nearly impossible to guarantee the first silicon success in an IC. Furthermore in high density devices like SRAMs, device variations are very common because of continuous scaling down of length, width and threshold voltage of the transistor devices. In these variations, if the variations occurring in the devices are random then it becomes a very tedious job to achieve silicon success. For example, random variations like number and location of dopant atoms in the channel will cause asymmetric variations and degrades the performance of the devices. It is therefore becoming a growing need to validate the silicon to detect and fix bugs in an IC after the design process. Thereby, it is largely viewed as an art with very few systematic solutions. As a result, post-silicon validation is becoming an emerging research topic for major innovations in electronic design automation.

In this work, we conducted a comprehensive analysis for detecting the memory cells which exhibits weak Static Noise Margin (SNM), write time, write margin and identified the factors causing these cells to exhibit weak properties. In this work the term ‘weak’ is qualified as the cells exhibiting weak SNM, cell current, write margin and write time. Based on these characteristics, two methods are proposed for identifying the weak bits. For verification of these methodologies in SRAM, a single port high density STM critical path was considered in 28nm technology.

# ACKNOWLEDGEMENTS

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*"Arise, awake, and stop not till the goal is reached" – Swami Vivekananda from Katha Upanishad.*

## PUBLICATIONS:

1. "*Statistical Analysis and Parametric Yield Estimation of Standard 6T SRAM Cell for Different Capacities*", 28th IEEE System on Chip Conference (SOCC), Beijing, China (Accepted for publication)

2. "*A Regression Based Methodology to Estimate SNM for Improving Yield of 6T SRAM*", Submitted to 24th IEEE Asian Test Symposium (ATS), Mumbai

3. "*A Modified Latch type Sense Amplifier with Improved Offset Voltage and Sensing Delay for SRAM*" Submitted to 24th IEEE Asian Test Symposium (ATS), Mumbai

4. "*Identification of Weak bits in SRAMs with respect to Write times*", (Under Preparation)

5. *"Assessing the Methodology for Weak bit Detection in SRAMs by Lowering the Bit line Voltage"*, IEEE VLSI Design 2016 (Under Review)

# LIST OF FIGURES

CONTENTS

# 1 INTRODUCTION

## 1.1 SRAM OVERVIEW

Today, the driving factors in the development of efficient and high density static random access memories (SRAMs) memory has been the driving force behind the rapid development of CMOS technology we have been witnessing in the past few decades. Starting from the first 1Kb DRAM chip developed by Intel in the seventies, nowadays DRAM capacities have reached beyond 1Gb. The advent of the virtual memory in personal computers contributed to the hierarchical structure of various kinds of memory ranging from the small capacity, fast but more costly cache memories to large capacity, slower but more affordable magnetic and optical storage. The pyramid-like hierarchy of memory types in a personal computer, shown in Figure 1, reflects the growing speed and cost/bit as we move from the bottom Level 5 (L5) remote secondary storage to the topmost register Level (L0). The introduction of memory hierarchy is a fundamental consequence of maintaining the random access memory abstraction and practical limits on cost and power consumption. The growing gap between the Micro Processor Unit (MPU) cycle time and DRAM access time necessitated the introduction of several levels of caching in modern data processors. In personal computer MPUs such levels are often represented by L1 and L2 on-chip embedded SRAM cache memories. As the speed gap between MPU, memory and mass storage continues to widen, deeper memory hierarchies have been introduced in high-end server microprocessors. Depending on the amount of L2 cache, ITRS distinguishes the Cost-Performance MPU which is optimized for maximum performance, and the lowest cost by limiting the amount of on-chip SRAM Level-2 (L2) cache and the high-performance MPU optimized for maximum system performance by combining a single or multiple CPU cores with a large L2, and recently, L3 on-chip SRAM cache [1]. Logic functionality and L2 cache capacity typically doubles every technology generation by doubling the number of on-chip CPU cores and associated memory.

One of the ways to increase the on-chip cache sizes is to use the high-density dynamic RAM. An SoC with embedded DRAMs implemented in the standard logic process can benefit from fast low- $V_{TH}$ transistors. However, the inherently high sub threshold leakage current complicates

implementation of a 1T DRAM cell. Replacing 1T DRAM cells with alternative DRAM cell designs having a larger number of transistors results in an area penalty and undermines the cell area advantage that embedded DRAMs normally have over embedded SRAM. Embedded SRAMs have been used to accelerate the performance of high-end micro-processors, network routers and switches. They use the regular fast logic process and do not require additional mask steps.

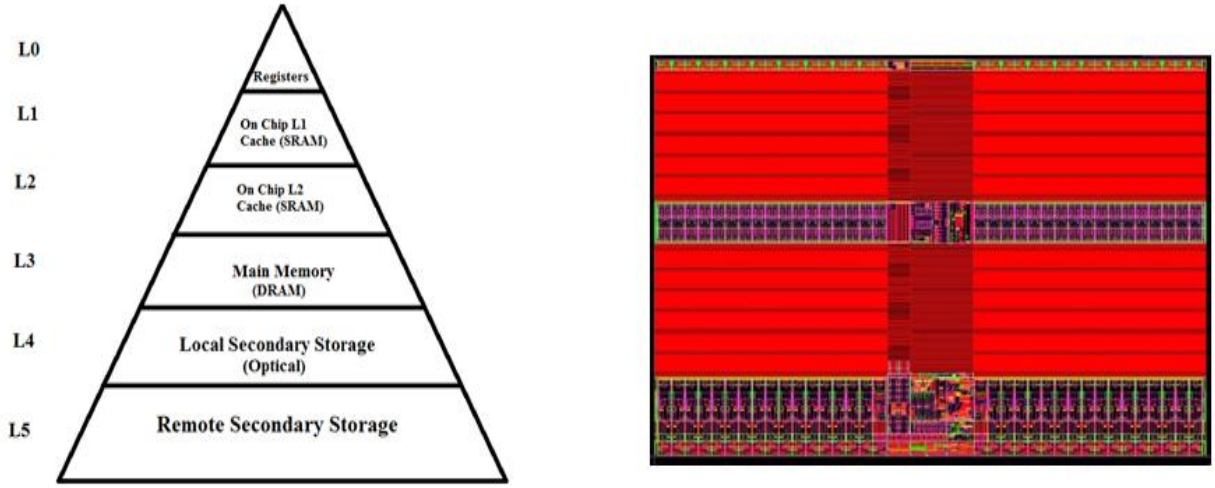



FIGURE 1 Memory Pyramid (LEFT) and High Density SRAM IC (RIGHT)

In order to double on-chip functionality every two years according to Moore's Law, technology-node scaling of 0.7 in linear size and 0.5 in area has to be carried out every three years; as well as an additional device/process design improvement of 0.8/(2 years) must be achieved. The advancement rate through the technology nodes determined by the ability to economically manufacture a chip based upon the best available leading-edge design and manufacturing process. The typical high-performance ASIC design is assumed to have the same average transistor density as high-performance MPUs, which mostly consist of SRAM transistors [2]. Every technology node the transistor density gap between the regular logic and embedded SRAMs is predicted to grow from approximately x5 in 2005 and to around x6 by 2018. At the same time, the six-transistor SRAM cell area now constitutes only 36% of the typical four-transistor logic gate area and is projected to further reduce to become 35% in year 2018. As a rule, SRAM cell size continues to scale≈0.5x/generation driven by the need for high-performance processors.

### 1.1.1 MEMORY CELL DESIGN AND ITS OPERATION

A typical 6T SRAM cell consists of cross coupled inverter which forms a latch with two access transistors for accessing the data which is stored in the memory cell or to write data into the memory cell. The design of the SRAM cell should be done in such a way that it should provide a non destructive read operation at the same time with good write margin.

1.1.1a Read Operation:

The read operation is performed by precharging the BLT and BLF to $V_{DD}$ and enabling the word line (WL).Upon read access, the bit line voltage VBLF remains at the precharge level equal $V_{DD}$. The complementary bit line voltage VBLT is discharged through transistors Q1 and Q5 connected in series (Figure2). Effectively, transistors Q1 and Q5 form a voltage divider whose output is connected to the input of inverter Q2−Q4 in Figure 3. Sizing of Q1 and Q5 such that the bump occurs at node BLTI should not be more than the trip voltage of the inverter Q2−Q4.

$$\Delta V = \frac{V_{DSATn} + CR(V_{DD} - V_{THn}) - \sqrt{V_{DSATn}^2(1+CR) + CR^2(V_{DD} - V_{THn})^2}}{CR}$$

$$CR = \frac{W_1/L_1}{W_5/L_5}$$

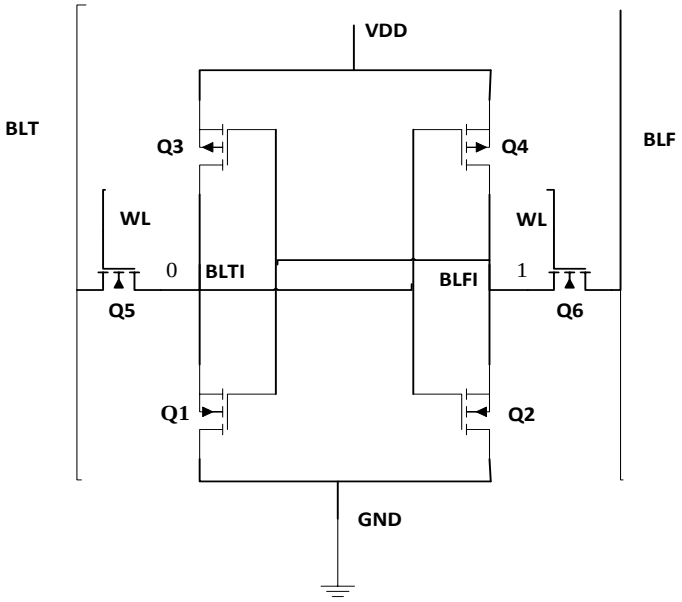



FIGURE 2 Standard 6T SRAM Cell

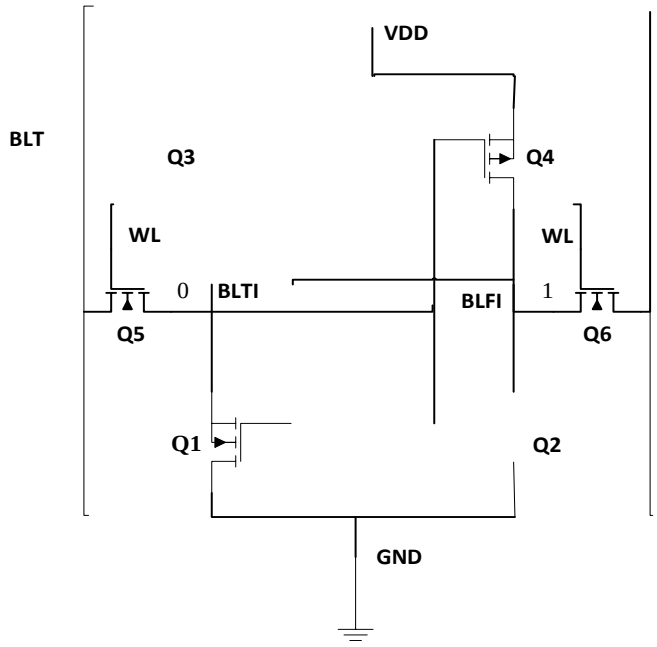



FIGURE 3 6t SRAM Cell in Read Operation

1.1.1b Write Operation:

Consider the write '0' operation assuming that logic '1' is stored in the SRAM cell initially. Figure 2 shows the voltage levels in the CMOS SRAM cell at the beginning of the data write operation. The transistors Q3 and Q2 are turned off, while Q1 and Q4 are operating in the linear mode. Now while writing into the cell both the bit lines BLT and BLF should be precharged and the bit line BLF should be discharged to zero such that the internal node BLFI discharges and hence positive feedback action starts causing flipping of data. Here, the strength of the access transistor should be greater than the strength of the pull down as shown in the equations. Typically the ratio of W/L of the pull up transistor should be 3-4 times lesser than W/L of the pull down transistor. Normally, to minimize the cell area and hence, increase the packing density, the sizes of the pull-up and access transistors are chosen to be minimal and approximately the same. However, stronger access transistors and/or weaker pull-up transistors may be needed to ensure a robust write operation under the worst process conditions e.g., in the fast PMOS and slow NMOS corner.

$$V_{"1"} = V_{DD} - V_{THn} - \sqrt{(V_{DD} - V_{THn})^2 - 2\frac{\mu_p}{\mu_n} PR\left(\left(V_{DD} - V_{tp}\right)V_{Dsat} - \frac{V_{Dsat}^2}{2}\right)}$$

Pull up ratio is given by,

$$PR = \frac{W_4/L_4}{W_6/L_6}$$

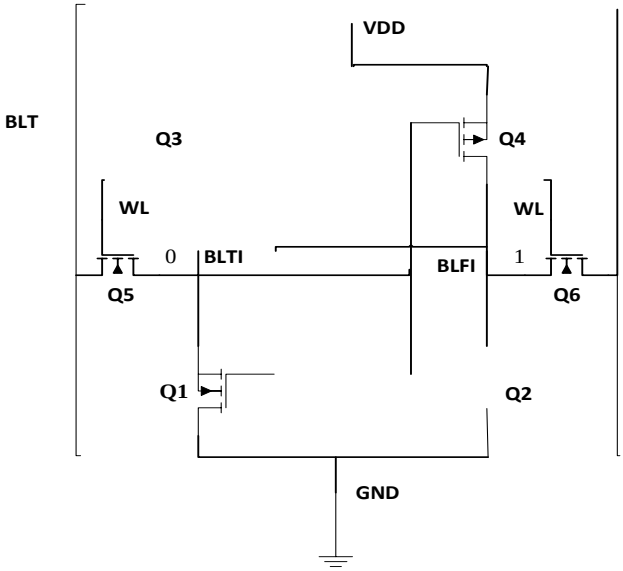



Figure 4 6T SRAM during Write Operation

### 1.1.2 MEMORY TEST BASICS

An efficient and economical memory test should provide the best defect coverage in the shortest time. Besides fault detection, a manufacturing memory test must also include diagnostic capability that allows identifying and possibly repairing defective locations by applying redundant elements. In addition, the diagnostic capability can be instrumental if the manufacturing yield ramp-up by providing feedback to designers and process engineers. A number of weak bit cell tests are proposed and given at [3-12]. A flavour on few of them are given below

#### 1.1.2a. MARCH TEST

March tests can be classified as functional test techniques for testing SRAMs. These kind of tests verify the circuit functionality by conducting read and write operations on each memory location of the array. A March test includes a finite sequence of March elements, which in turn consist of the sequence of operations applied to every cell before proceeding to the next cell. In simple terms it can be explained as writing data into the memory location and reading which in turn should yield the same data which was written before. If reading doesn't yield the same data, then

it can be deemed as a fault cell. These kinds of tests are often targets certain kind of faults such as stuck at, address, coupling etc...

#### 1.1.2b DATA RETENTION TEST:

A typical Data Retention Test (DRT) is implemented as a pause of an order of 100ms between the March elements. DRT can detect a complete open in the pull-up path of an SRAM cell. In case of a symmetric defect, where the pull-up paths in both the inverters are open, the detection is not dependent on the data value stored in the cell. However, if a cell has an asymmetric defect, where only one of the inverters has an open in the pull-up path, the DRT will only detect an open in the pull-up path of the node storing a "1" [13]. This property of the DRT requires to run it for each of the two opposite backgrounds to cover both the asymmetric faults in the pull-up path of the cell. Since running the DRT for each of the data backgrounds takes 100-200ms [14], applying the DRT will result in each chip spending an extra 200-400ms on the tester

### 1.1.2 WEAK BIT TEST ECONOMICS

Memory array organization becomes more and more complex as the demand of high density SRAM memories is increasing day by day. As, the device density becomes higher and the operating voltage is decreasing over the decades, it results in yield loss and parametric failures. The increasing transistor/pin ratio which is projected to exceed 2.3 million/pin by 2016 [15] is limiting the controllability from the primary inputs and the observability of the faulty behaviour at the primary outputs in embedded memories [16]. Moreover, striving to keep up with the increasing clock speeds of SoCs increases the cost of Automatic Test Equipment (ATE) so that the at-speed test of high-performance chips becomes problematic. The fastest available ATE is always slower than the chips it will test. As multi-million-dollar ATEs become commonplace, the cost of the tester time spent on every chip directly impacts the total cost of the chip.

A customer regards a product to be of high quality if the product is meeting their requirements at the lowest possible cost. Memory tests check conformance to the requirements, while the cost is reduced by improving the process yield. Exhaustive functional memory test is economically unfeasible. For instance, exhaustive test of a 1Kb SRAM array will take $2^{1024}$ combinations to complete a full functional test. Such a test of an SRAM with the access time of 10ns will conclude in more than 10290 years! Attention was given to the fault modelling, structural testing

and DFT techniques to ensure and maintain test cost effectiveness and low defect levels. The test cost per chip, which can run up to a half of the product cost and is directly related to the test time, cannot increase significantly.

However, the number of bits/chip is exponentially growing and fault sensitivity is increasing. Maintaining an acceptable defect level in the upcoming scaled down generations will likely require more complicated and lengthy tests. An ideal test algorithm(s) should have maximum fault coverage with minimum complexity, which is proportional to the test time and test cost. However, real test algorithms have limited fault coverage. To improve the fault coverage, several tests may have to be employed. Therefore, a test engineer faces a difficult choice between balancing the test cost and the defect level.

## 1.2 MOTIVATION AND AIM OF THE RESEARCH

Up to 70% of Systems on a Chip (SoC) area are occupied by embedded memories. In order to achieve higher robustness, embedded SRAMs (eSRAM) are often used in SOC applications. However, due to advancement in technology it is nearly impossible to guarantee the first silicon success in an IC. Furthermore in high density devices like SRAMs, device variations are very common because of continuous scaling down of length, width and threshold voltage of the transistor devices. In these variations, if the variations occurring in the devices are random then it becomes a very tedious job to achieve silicon success. For example, random variations like number and location of dopant atoms in the channel will cause asymmetric variations and degrades the performance of the devices. It is therefore becoming a growing need to validate the silicon to detect and fix bugs in an IC after the design process. Thereby, it is largely viewed as an art with very few systematic solutions. As a result, post-silicon validation is becoming an emerging research topic for major innovations in electronic design automation.

In this work, we conducted a comprehensive analysis for detecting the memory cells which exhibits weak Static Noise Margin (SNM), write time, write margin and identified the factors causing these cells to exhibit weak properties. In this work we qualified the term ‘weak’ as the cells exhibits weak SNM, cell current, write margin and write time. Based on the above mentioned characteristics, we proposed two methods for identifying the weak bits. For

verification of these methodologies in SRAM, a single port high density STM critical path was considered in 28nm technology.

## 1.3 THESIS ORGANIZATION

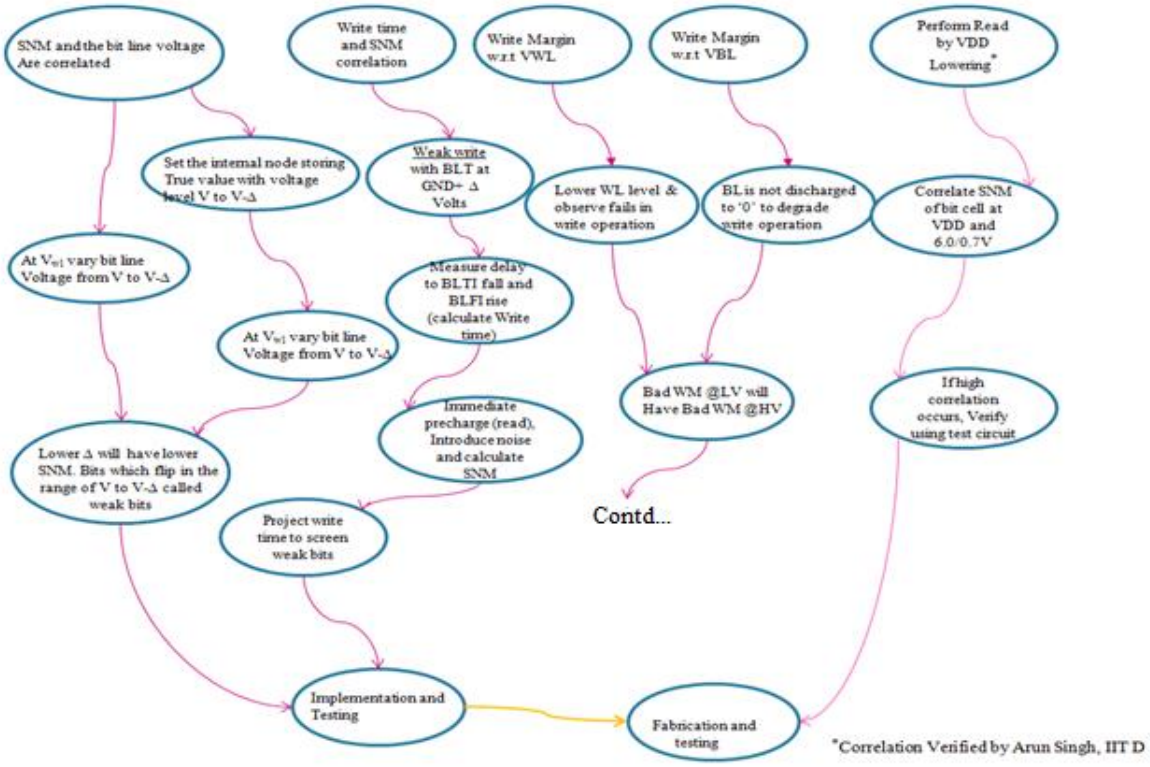
The thesis is organized as follows. Chapter 2 describes a methodology for detecting the weak bits with respect to write margins. It also includes a discussion on the correlation between Static Noise Margin and write time of memory cell. A discussion on circuitry required for performing the weak bit test is presented. Finally chapter concludes with result discussion.

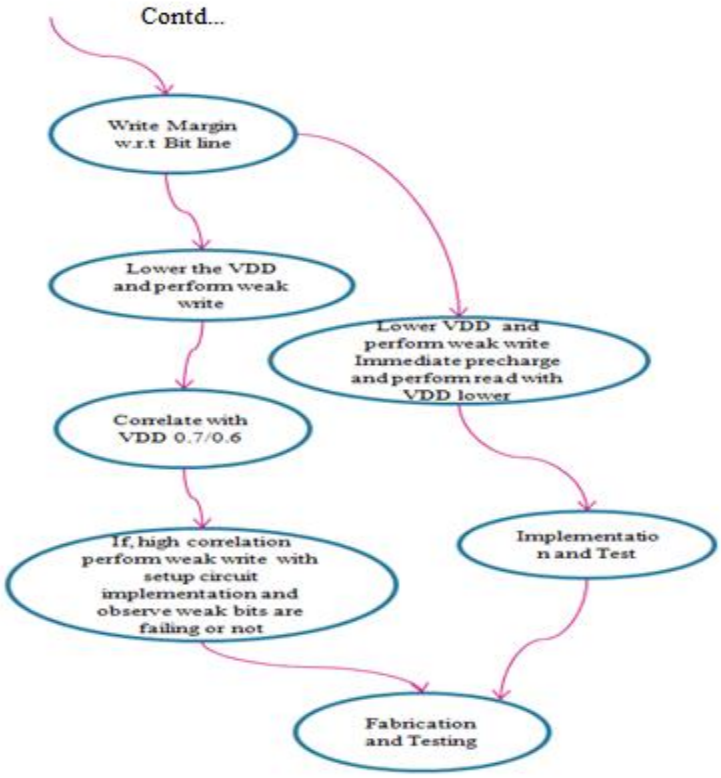
Chapter 3 presents a methodology for detecting the cells which are exhibiting low static noise margin. A detailed discussion on stability of SRAM cell is presented. Section 3.2.2 presents correlation methodology for the proposed test method. Several setup circuits and their drawbacks are also discussed in this chapter.

An alternate approach for detecting the weak bits by reducing the bit line voltages is presented in Chapter 4. Correlations of SNM of memory cell at normal conditions for different bit line voltages and for worst case conditions are presented in this chapter. An important discussion on why this methodology fails in detecting weak bits also presented

The direction of future work and methodology of improving the write margin and disturbing the write operation is presented and discussed its effectiveness over directly disturbing the write operation in chapter and conclusion follows.

Test methods for detecting weak bits in SRAM at a glance are shown in the next page.


SNM and the bit line voltage Are correlated
Write time and SNM correlation
Write Margin w.r.t VWL
Write Margin w.r.t VBL
Perform Read by VDD Lowering*
Set the internal node storing True value with voltage level V to V-Δ
Weak write with BLT at GND+ Δ Volts
Lower WL level & observe fails in write operation
BL is not discharged to '0' to degrade write operation
Correlate SNM of bit cell at VDD and 6.0/0.7V
At Vwl vary bit line Voltage from V to V-Δ
Measure delay to BLTI fall and BLFI rise (calculate Write time)
At Vwl vary bit line Voltage from V to V-Δ
Bad WM @LV will Have Bad WM @HV
If high correlation occurs, Verify using test circuit
Immediate precharge (read), Introduce noise and calculate SNM
Lower Δ will have lower SNM. Bits which flip in the range of V to V-Δ called weak bits
Contd...
Project write time to screen weak bits
Implementation and Testing
Fabrication and testing
*Correlation Verified by Arun Singh, IIT D


Contd...
Write Margin w.r.t Bit line
Lower the VDD and perform weak write
Lower VDD and perform weak write Immediate precharge and perform read with VDD lower
Correlate with VDD 0.7/0.6
Implementation and Test
If, high correlation perform weak write with setup circuit implementation and observe weak bits are failing or not
Fabrication and Testing

# 2 SRAM CELL WEAK WRITE DETECTION

*This chapter is dedicated to identification of Weak cell with respect to write operation and modeling of setup circuitry for detection of the cell. Section 2.1 gives a generic introduction of weak bits of SRAM*

## 2.1 INTRODUCTION

Up to 70% of Systems on a Chip (SOC) area is occupied by embedded memories [17][18]. In order to achieve higher robustness embedded SRAMs (eSRAM) are often used in SOC applications. However, because of high density, the consequences are memory devices are more likely to be effected by manufacturing losses results in the overall drop of Yield (Y).With scaling of device dimensions, random variations like number and location of dopant atoms in the channel limits the variations in terms of electrical characteristics of the devices, these microscopic random variations affects are more common in minimum geometry MOSFETs which are majorly used in area constrained devices called SRAMs[19][20]. Since these random variations are independent on the location of transistor on the chip, the mismatch caused between the neighbouring transistors due to these random variations on the chip makes memory cells 'weak'. The definition weak cell doesn't replicate any Fault in the cell. Weak cell failures are random in nature as the cells are not entirely damaged and the state flipping may occur only under certain operating conditions. For instance, a weak SRAM cell can fail under stressed Process (P), Voltage (V) and Temperature (T) while at other combination of PVT might still have been operating. The cell weakness is typically a result of resistive defects, excessive process shifts, transistor mismatch, IR drops, Coupling etc. The state flipping of a weak cell may occur due to any electrical disturbance such as power supply noise, read/write cell disturbs, etc. during the normal operation of the SRAM. These adverse conditions, especially combined, can cause a weak cell. As the applications demands, bit cells with lower operating and retention voltages which results in reduction of SNM. SNM reduction of the SRAM cell puts limit on Yield in SoC. As a guideline, [21] suggests that $\mu - 6\sigma$ of SNM is required to exceed nearly 4% of $V_{DD}$ to reach a 90% yield on 1Mb SRAM. Thus it suggests that for an SRAM cell to be stable, it should have an SNM above some threshold SNM at typical conditions else the cells may escape the traditional tests and fail in the field. The main reason for the unstable behaviour of an SRAM cell could be weak property or poor nature of the pull up PMOS transistors (Fig.5) ($Q_3$,

$Q_4$). If $I_{leak\_Q2} \geq I_{Q4} + I_{leak\_Q6}$ then the capacitance at the node A will get discharged after a time proportional to

$$\frac{CV}{(I_{leak_{Q2}} - (I_{Q4} + I_{leak_{Q6}}))}$$

Where, C is the capacitance seen between node A and ground.

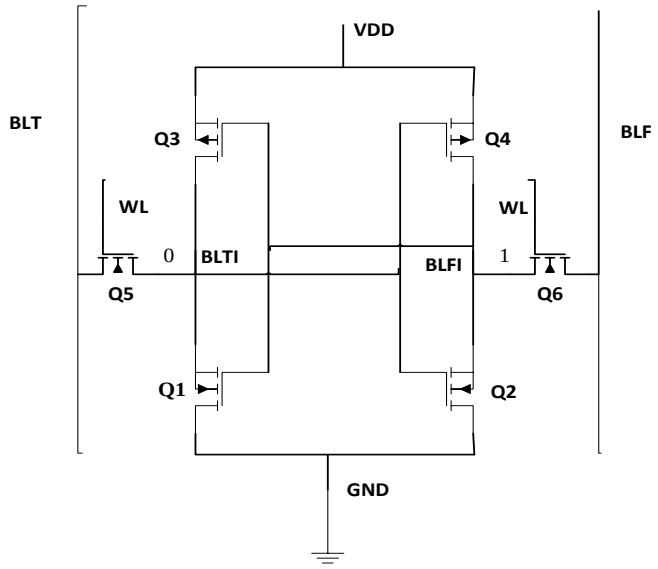



Figure 5 Standard 6T SRAM Cell

This indicates that the memory cell cannot store the data beyond this time, hence causes unstable. In order to detect this category of weak cells, a simple methodology is reading the cells after a certain delay mentioned above and compare the data with previously written data. This test known as Data Retention Test (DRT) can detect weak PMOS transistors ($Q_3$, $Q_4$). However, this test needs significant test times and elevated temperature range as the leakage currents has positive temperature dependencies. On the other hand significant test time and elevated temperatures degrades the economics of the test. This chapter discusses with detection methodology that depends in the write times of memory cell. In context with Write Time, the *weak cells* are defined as the cells with large write time which makes the cell to write weak 1 or weak 0.

### 2.1.1 PERFORM READ AFTER WRITE (PRW) TEST CONCEPT

Figure 1 illustrates the schematic of well-known 6T SRAM memory cell. Node Q is the true node whereas QB is the complement of Q. The minimum geometry, random variations and the

high density of these cells on the silicon makes more prone to defects which makes the restoring feedback in the cell weak consequently prone to write and/or read fails. While performing weak write into the cell, if the internal nodes storing 0V takes large time to charge 1V and we introduce noise after immediately precharging the bit lines, the weak cells will flip for less noise which means the cells which are weak will have less SNM. So, write time is inversely proportional to SNM (When write is being disturbed). The related figure is shown in the next page (Fig.6)

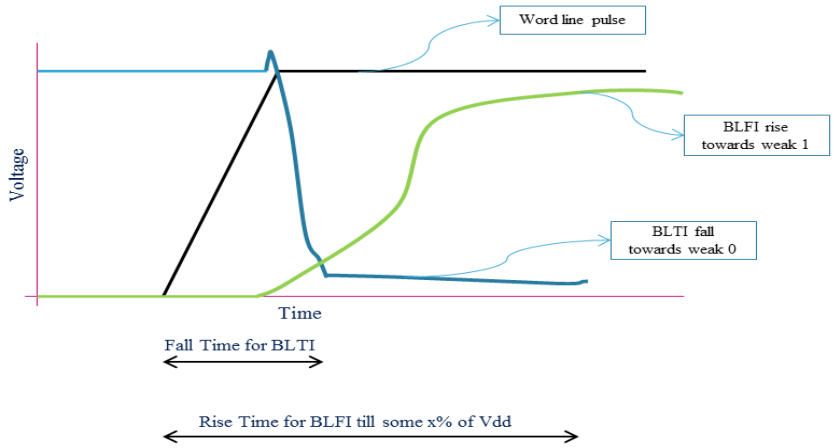



Figure 6: Model for Detecting Weak Bits

Assume that the memory cell is storing 1 and 0 on its internal node QB and Q. Introduce threshold voltage ($V_t$) variations in the cell by DoE method and launch the word line pulse by maintaining BLB at 0V and BL at 1V and measure the delay to QB fall and Q rise. It is clear that the discharging rate of the node QB is faster than the charging rate of node Q. From this step, the write times of the memory cell can be observed for different Vt variations. After some amount of write time's, precharge the bit lines to VDD and introduce some noise to calculate the SNM of the cell. Suppose if the cell is weak, upon application of write disturbance the cell will flip its state else retains its previous state. This situation is essentially nothing but projecting an immediate read signal after a specific amount of write time while writing a data into the memory cell. In order to project read signal after appropriate write time, it is essential to calculate the weak write time of the cell. This can be done by introducing Vt variations in the cell by DoE method and calculating the weak write time for screening the weak bit.

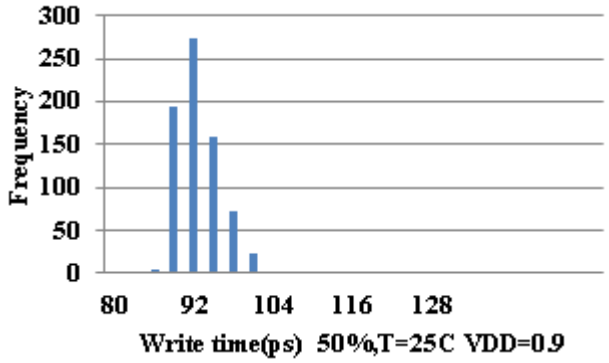



FIGURE 7: Histogram of 50% Write Times for $V_T$ Variations

It can be observed from figure.7 and 8 that the VT conditions VDD=0.9V and T=25$^{o}$C are not stressing the weak bits and hence the distribution of the write time is very narrow which results is not allowing to identify the write time for screening the weak bits. On the other hand, it can be observed that for the worst case voltage (V) and temperature (T) conditions VDD=0.7V and T=-40$^{o}$C are stressing the bits which are weak and hence the distribution of write time is very wide. The related plots can be observed below.

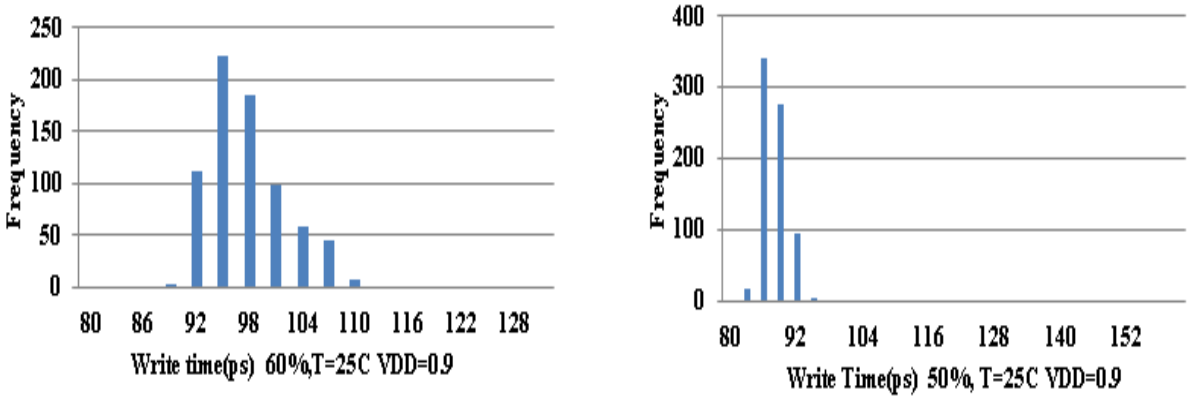



FIGURE 8: Histogram of Write Times

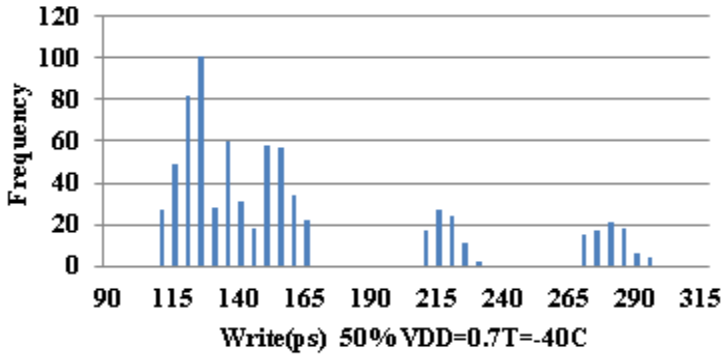



FIGURE 9 Write Time Histogram at 0.7V supply

But performing the test at elevated temperatures or reduced temperatures is not recommended for weak bit tests. In order to screen the weak bits at normal operating voltages and temperatures with respect to write times, the voltage level for BLB is to be maintained at 0+ΔV and the write disturb is to be applied . This situation is similar to weak writing into the cell and reading by disturbing write operation. In order to verify the voltage which is required for detecting the weak bits, simulations are again performed by maintaining bit line voltage at 0+ΔV for the side storing 1V.

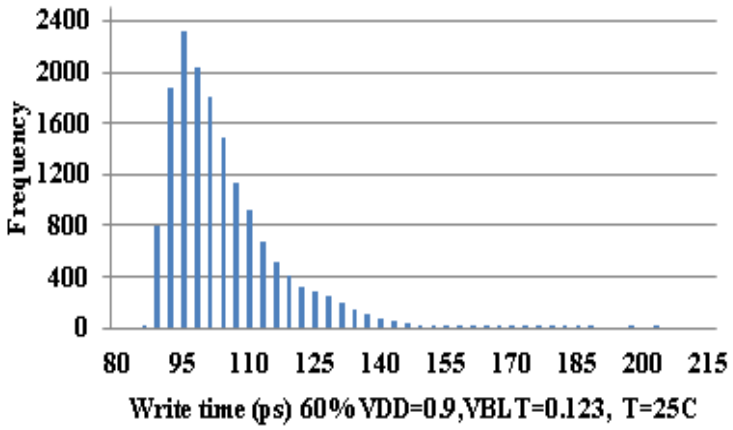



FIGURE 10 Write Time Histogram For VBLT=0.123v

Fig.10 presents a wide distribution of 60% write times for a bit line voltage of 0.123V instead of 0V at MAXMIN lot at 0.9V, 150$^{o}$C which indicates that a memory cell undergoes stress when it is subjected to these mentioned conditions. It can be observed from Fig.10 that the density of memory cell having write times of greater than 140ps are very less which essentially suggests that these cells could be a weak cells w.r.t the write times. Fig.11 depicts the distribution of 60% write time for bit line voltages of 0.25V and 0.27V respectively at 0.9V supply Voltage and 25$^{0}$C for MAXMIN corner. From Fig.11 the weak write time can be found to be as 140 ps, that means at 140ps the read pulse must be activates to disturb write operation. In order to verify the hypothesis, SNM of the cell is calculated after launching read pulse at 140ps and the relation between SNM and write time is verified

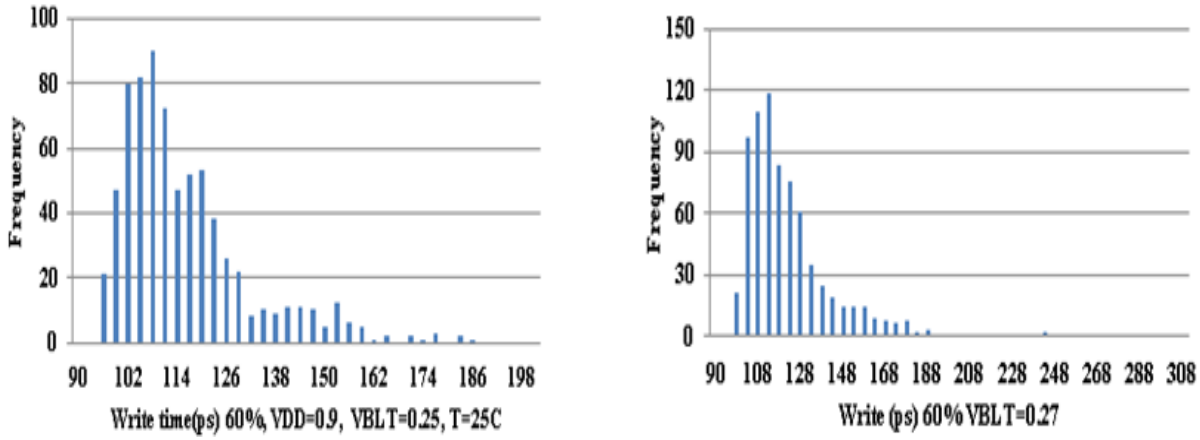



Figure 11: Write Time Histogram

### 2.1.2 VERIFICATION OF PROPOSED METHOD

This section deals with verifying the dependency of static noise margin (SNM) with write times of memory cell. It should be noted that, noise should be incorporated only when the bit lines are precharged high. In order to verify how the SNM of memory cell is dependent on write time of SRAM cell, a standalone circuit for a load of 512 rows is considered with a pulse width duration of 2ps at $V_{DD}$=0.9 and temperature $25^0$C. The considered circuit is simulated in ELDO 13.2b simulator. It can be observed from Fig.12 that the SNM and write time follows nearly inverse relation. It can be justified theoretically as when a bit cell has weak write time, internal node takes large time to charge which .So, these bits can easily flip their states whenever an immediate read is performed as the SNM of the cell drops down for weak writing cells.

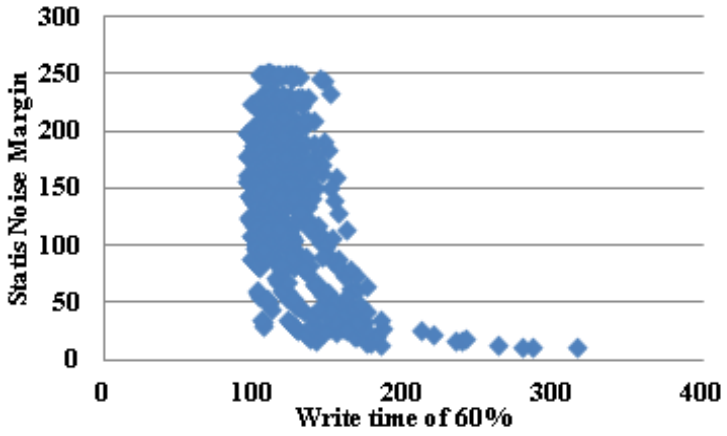



Figure 12 SNM and Write Time Correlation

## 2.2 EXPERIMENTAL SETUP-CHARGE SHARING TECHNIQUE

The proposed active programmable charge sharing technique for generating any test voltage $V_{BL\_TEST}$ considers a group of bit lines in an SRAM chip. Let N be the number of bit lines considered for generating required test voltage $V_{BL\_TEST}$ in an SRAM array. Initially BLT and BLF are precharged to $V_{DD}$ and the other (N-1) cells are driven to 0V. By shorting all the N bit lines once after the bit lines BLT/BLF are charged to $V_{DD}$, because of charge sharing action of the bit line capacitances, after steady state all the N bit lines will settle to a voltage equals to $V_{DD}/N$ if all the bit lines exhibits equal capacitances. For example, if we consider the numbers of bit lines are to be 8, then after the events charging/discharging and shorting the bit line all the bit lines settle to a steady state value 1/8 which is equal to 0.125V. If we repeat the same procedure for different number of bit lines we can generate $V_{BL\_TEST}$ as desired. To verify the proposed charge sharing technique, an SRAM test chip is considered with N equals to 5 bit lines and the number of rows equal to 256 on 28 nm technology. Fig. below depicts the output voltage when 5 bit lines are shorted (0.125V). The test sequence starts with driving the bit line voltage BLT to the test voltage $V_{BL\_TEST}$ followed by writing data into the cell and then immediately precharging the bit lines to disturb the write operation and the subsequent read operation detects whether the SRAM cell is weak or good.

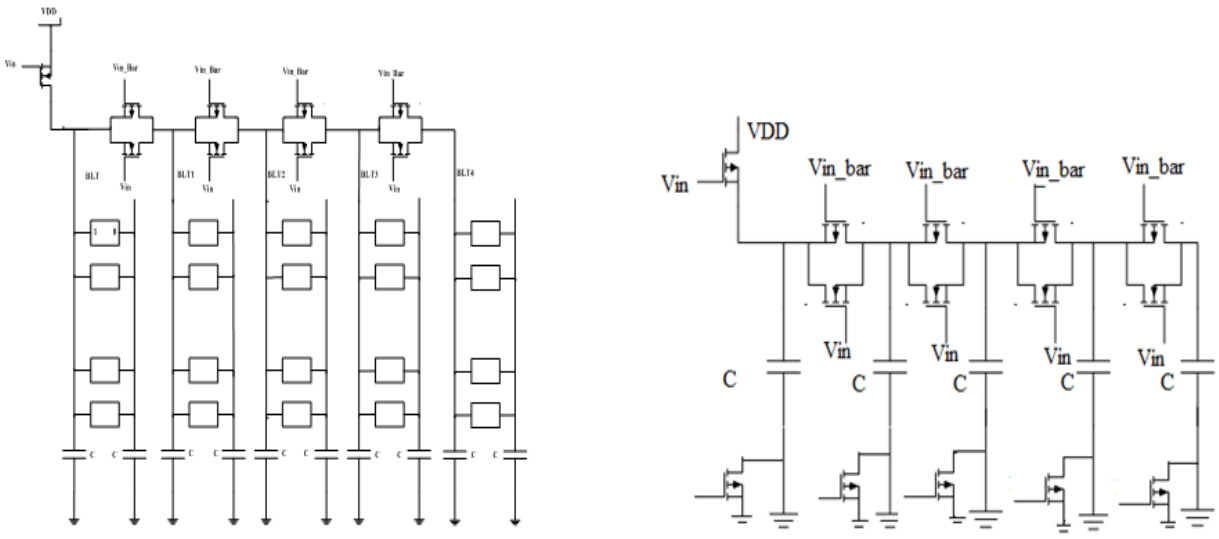



FIGURE 13 Charge Sharing Technique (Left) and its Equivalent (Right)

The above circuit is simulated in ELDO 13.2b simulator in 28nm technology environment. The memory cell is initialized with data 1 which means, the node storing BLTI holds 1V and the other node BLFI is at 0V. The equivalent circuit is shown in figure 13 (right) with its discharging

driver transistors. The pass gates which are present between the capacitors are used to short bit lines electrically. Initially the first bit line shown in fig 13 is charged through a PMOS, after charging the bit line, all the five bit lines are shorted through transmission gates. The related outputs can be observed from fig 13 that all the bit lines are settling to a value of 0.125V.

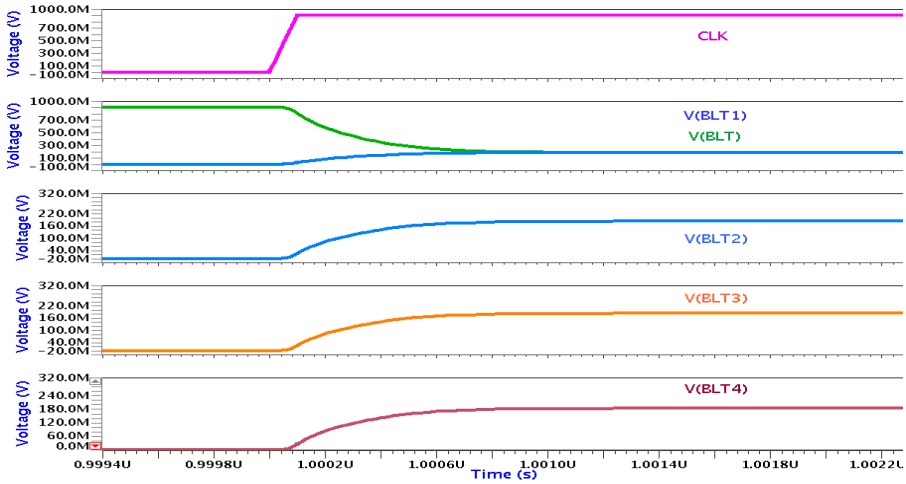



FIGURE 14 Transient Responses for the Circuit Shown in Fig 13

### 2.2.1 SETUP CIRCUITRY IN MEMORY

The muxing technique 8X1 which is used in single port high density SRAM memory is implemented by two 4X1 mux's. The resultant figure in terms of black box is as shown in Fig.15.

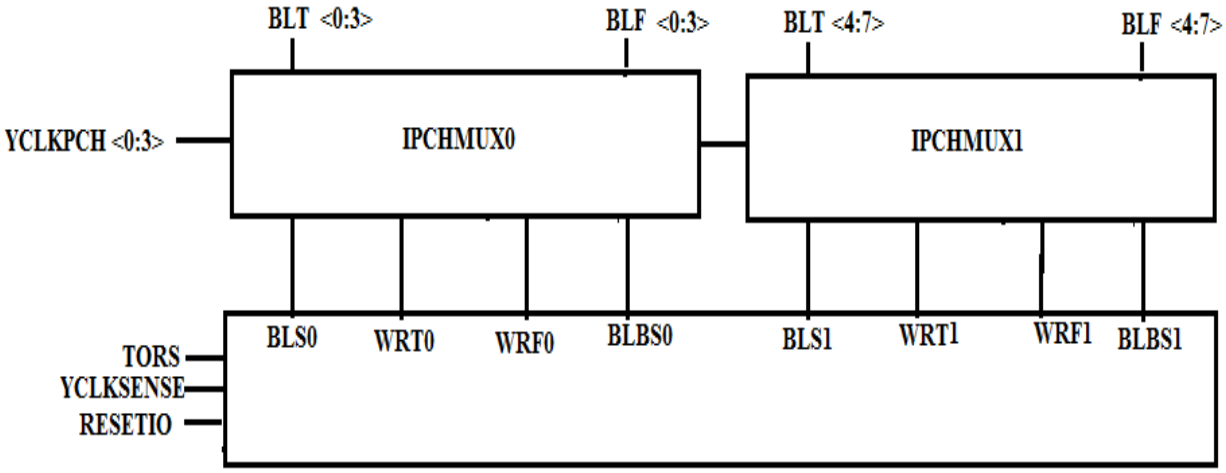



Figure 15 Realization 0f MUX 8X1 with two 4X1

The driver transistors which are to be used for setting up the initial node voltage should not be excited with WRF which is called as write driver signal or precharge signal (YCLKPCH) signal

as it will affect the data of the memory cell in previous read signal if any. A new circuitry should be designed for the discharge of the bit lines. YCLKPCH<0>, YCLKPCH<1> … starts first than any of the signal shown in the Fig.16. It is not possible directly to preset the other columns of the SRAM without having any signal which starts before YCLKPCH's. Solution is to use an even number of Inverter chain and delay the YCLKPCH signal which goes to the PCH and generate new signal for discharge of the columns with YCLKPCH and delayed version of YCLKPCH. Number of inverters between YCLKPCH< > and YCLKPCH_delayed should be an even number. In first simulation used 14 inverters and YCLKPCH_delayed is named as YCLKPB11 (delay of 120 ps). In order to decouple the memory from write drivers the circuit as shown inFig.18 is being used.

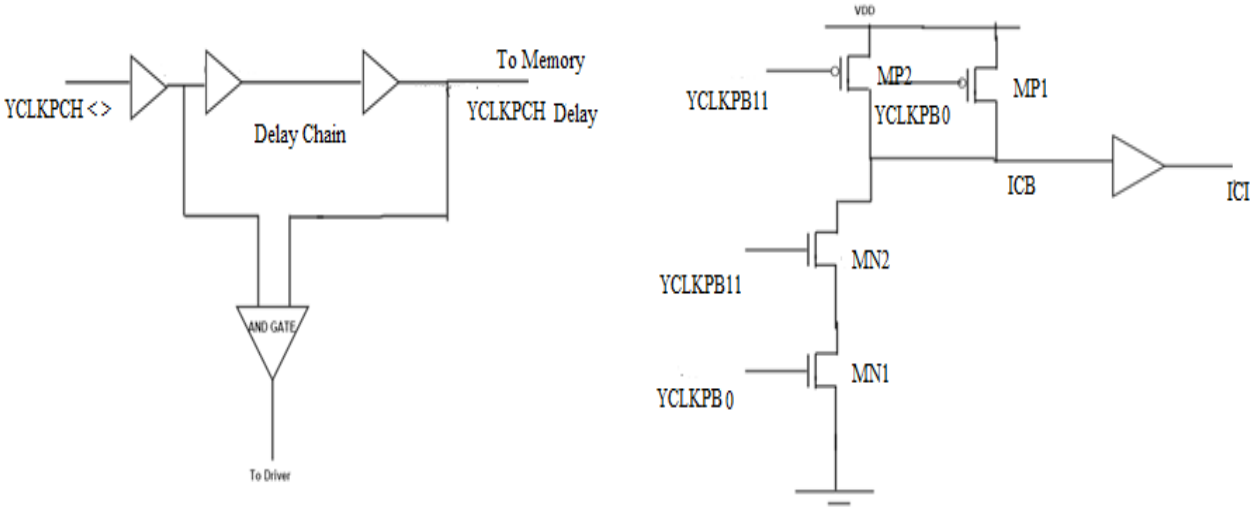



FIGURE 16 Setup Circuits for Precharging bit lines (Left) and Initializing bit lines (Right)

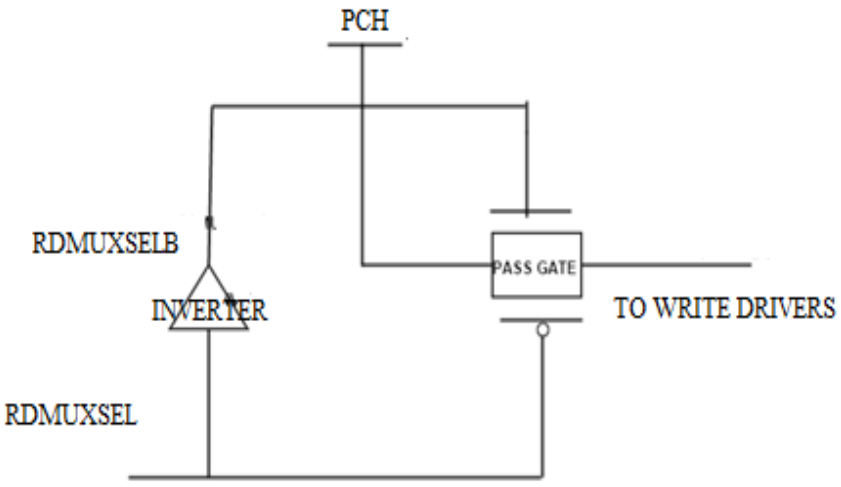



FIGURE 17: Circuit for Decoupling the Write Drivers

### 2.2.2 RESULTS

This section presents how the weak bits are identified and detected from an array of memory. From the above sections it is clear that, the bits which exhibit either large write time or less SNM can be qualified as the weak bits .It is again obvious that if a memory cell exhibits even both weak SNM and write time also qualified as weak cell. In this methodology, we have combined four bit lines of SRAM core that means four columns are considered while testing the chip and used intrinsic capacitance effect to generate the required voltage for testing. As the testing method suggests, weak write operation should be performed followed by immediate read operation

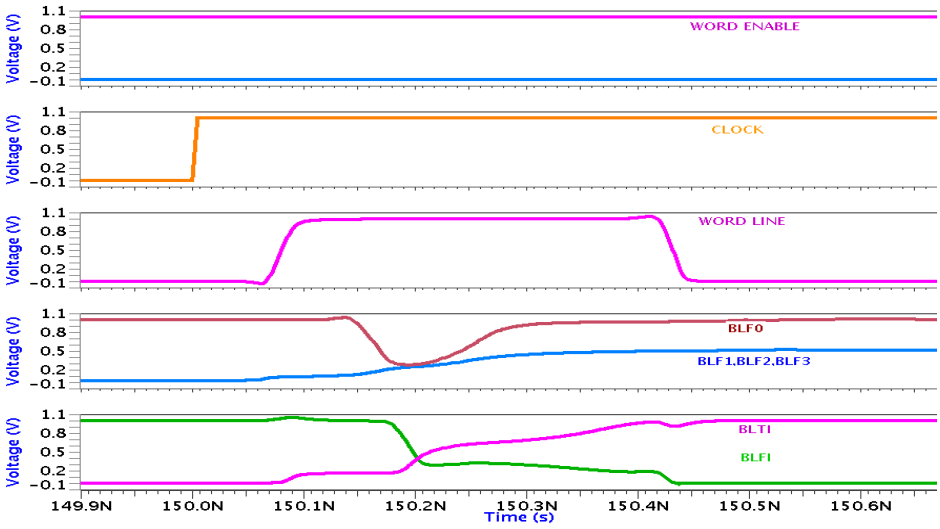



FIGURE 18 Transient Response of the Memory Cell with Setup Circuit

While incorporating the setup circuit for identifying the weak bits the good cells shouldn't be disturbed. The same can be observed as the setup circuit is not disturbing the write operation of the normal cell (BLTI and BLFI) when no variations were introduced in the devices of SRAM cell. Initially the test setup is incorporated in standalone mode and the correlation between write time and the SNM is taken for different variations of all six devices in SRAM cell using Design of Experiments (DoE) method.

Now the test setup circuit is incorporated in the complete SRAM system for 2048 words and again the same variations are incorporated using DoE method and observed the variations for which the cell is not writing. The variations for which the memory cell cannot able to write in

complete SRAM cell are mapped with the variations from the stand alone experiment and observed the outputs.

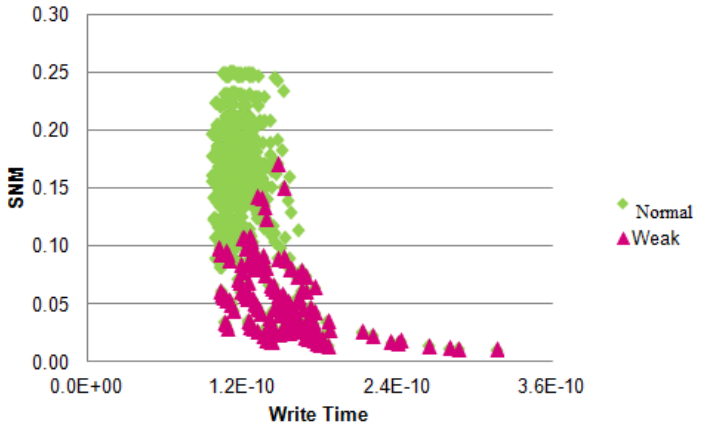



FIGURE 19 Plot representing Normal bits (Green) Weak Bits w. r. t Write Time (Pink)

In the above figure 19, the portion of bits with pink colour is weak bits and the portions of bits with represented in green colour are normal bits. It can be observed that the bits which are weak with respect to write operation have either weak write time or less SNM or both.

# 3 SUPPLY VOLTAGE LOWERING FOR WEAK BIT DETECTION

*In chapter 2, a method for detecting the weak bits with respect to write time is discussed. This chapter is dedicated for another approach for detecting weak bits by lowering the supply voltage. This chapter starts with verifying the hypothesis made for detecting weak bits at different voltages, processes and temperatures. A comprehensive SNM sensitive test at lower voltages is conducted for 28nm SRAM cell. The latter part of the chapter deals with designing the setup circuit for the verification of the test method followed by testing the memory.*

## 3.1 INTRODUCTION:

The technology from semiconductor industry is being constantly pushed to improve the performance of SRAMs. As it is being discussed in the previous chapters, one solution is to scale down the physical dimensions of the circuit components. It is to be noted that that the Constant-voltage scaling (CVS) in the VLSI designs are being dominated at lower physical dimensions. As the length of the channels are scaling down, the velocity saturation due to the increasing electric field in short-channel transistors created a situation where even after further voltage scaling did not give a performance advantage over the constant- field scaling [22]. In other words, since the drain current in short-channel transistors is no longer a quadratic function of drain voltage (Reference, Waterloo Thesis), the gain of an increased drain current has become less important than the penalty of a higher voltage causing the increased power dissipation. Constant Field Scaling requires, decrease of supply voltage which in turn results in decrease in Noise Margins of SRAMs. On the other hand random distribution of the dopant atoms in the channel makes the behaviour of the transistor uncertain and leads to decrease of noise margins.

## 3.2 NOISE MARGIN & SNM DEFINITIONS:

The noise margin can be defined using the input voltage to output voltage transfer characteristic, a.k.a. Voltage Transfer Characteristic (VTC). In general, the Noise Margin (NM) is the maximum spurious signal that can be accepted by the device when used in a system while still maintaining the correct operation [23-25]. If the consequences of the noise applied to a circuit node are not latched, such noise will not affect the correct operation of the system and can thus be deemed tolerable.

### 3.2.1 STATIC NOISE MARGIN OF 6T SRAM FOR READ CASE:

Static Noise Margin (SNM) is the most prominent stability metrics and was introduced more than 40 years ago [15]. With this metric , it can be easily estimated how much the SRAM cell is tolerable towards noise, in other words estimated how much voltage room for static noise, i.e. DC voltage, is left until the cell will flip. Therefore, both inverters (Cross coupled inverters from SRAM circuit) are first scanned independently to get the transfer curves, also known as voltage transfer characteristics VTC. Then, curves are plotted into one diagram, while one transfer curve is mirrored. This results in 2 called overlaying curves, better known as 'butterfly curve'. The eye opening of the biggest inbuilt square is a measure for how much static noise is needed to reach the trigger level of the opposite inverter under read conditions.

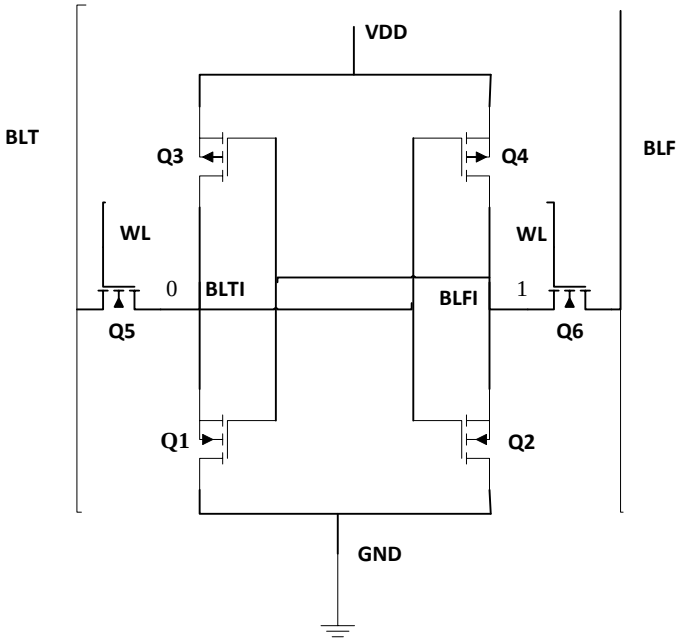



FIGURE 20: Standard 6T SRAM Cell

For the above 6T SRAM cell shown in Figure 30, the SNM is calculated in 28nm technology and observed as 230mV at no device variations. The resultant butterfly plot is shown in the below figure at typ-typ corner. The figure shown in the right side represents the read failure of the memory cell due to stability failure.

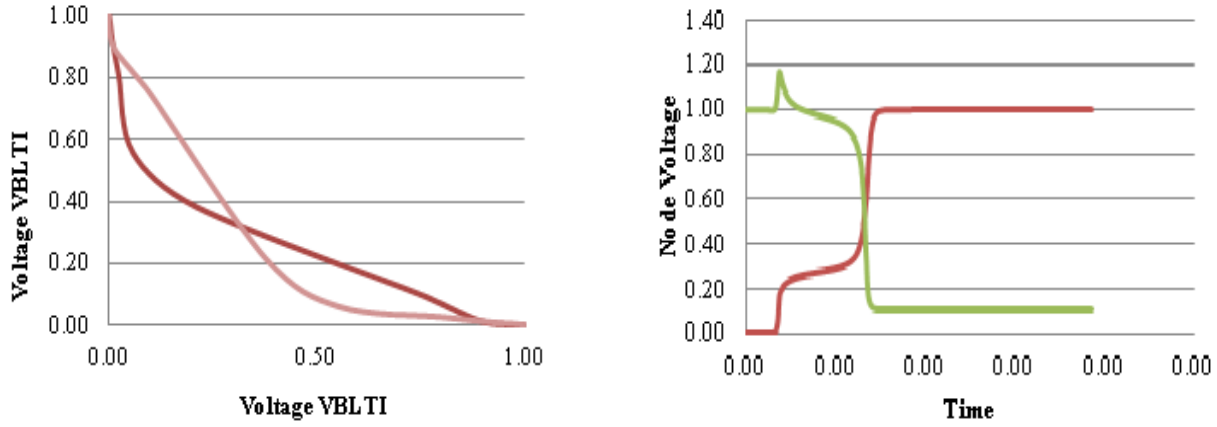



FIGURE 21 SNM plot and Read Failure

### 3.2.2 CORRELATION METHODOLOGY:

In order to test the memory cell to detect the weak bits, correlation methodology is used. The required test voltage can be found by correlating the SNM at reduced VDD voltage with the worst case conditions such as supply voltage of 0.7/0.6V and temperature of -40$^{o}$C and 125$^{o}$C at all corners. Initially a standalone memory cell with its equivalent load of 512 rows and a read pulse width of 2ps is considered and variations in all the devices are introduced using Design of Experiments (DoE) method and simulate in ELDI 13.2b simulator.

The supply voltage must be selected in such a way that the correlation between normal conditions with reduced supply SNM and the worst condition (0.6/0.7V and 150/-25$^{0}$C) should yield high correlation.

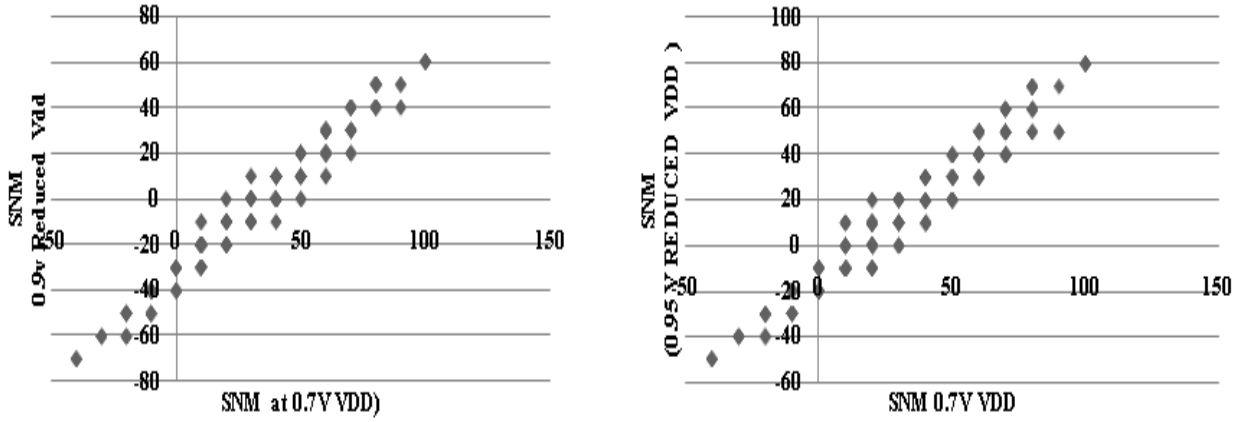



FIGURE 22 MaxMin

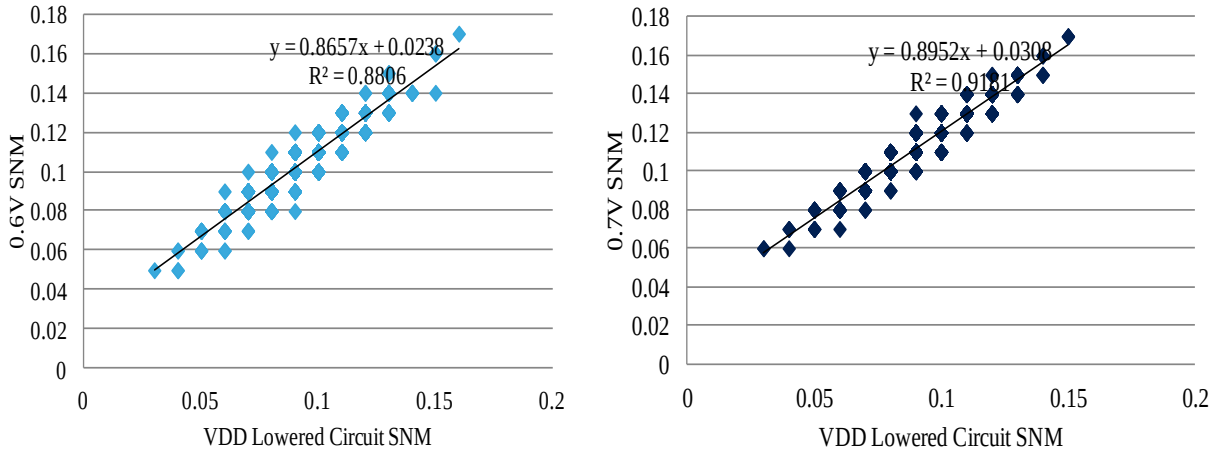



FIGURE 23 MaxMax & MaxMin

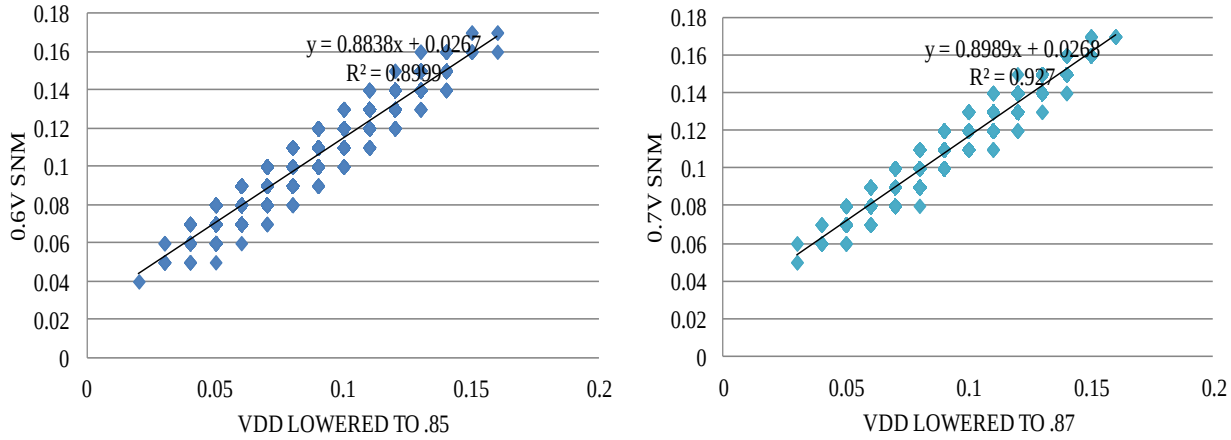



FIGURE 24 MaxMax & MaxMin

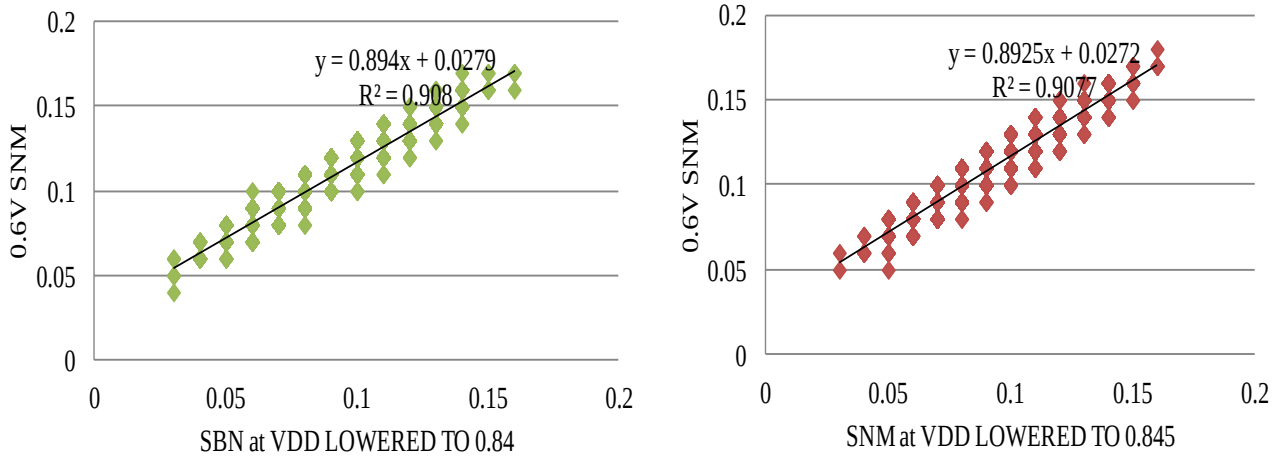



FIGURE 25 TypTyp & MaxMax

TABLE 1 Test Voltages for different Corners

| LOT | MAXMAX | MAXMIN | MINMAX | MINMIN | TYPTYP |
|---|---|---|---|---|---|
| Maximum SNM Correlation at VDD | 0.85V | 0.87V | 0.84V | 0.84V | 0.85V |

### 3.2.1 SETUP CIRCUIT FOR VDD LOWERING

This section deals with explanation and identification of setup circuit for lowering the $V_{DD}$ to be used for identification of weak bits with respect to Static Noise Margin. For achieving the circuit different methods like diode connector circuit and switching capacitor circuits were considered. Due to their constraints in incorporating the above circuitry, a simple resistor divider circuit is taken. To verify the response of the circuit a total of 512 rows of SRAM cell load is considered in the standalone mode.

### 3.2.2 RESISTOR DIVIDER-DIODE CONNECTOR

Initially a simple resistor divider is considered with all the resistors are realized with diode connector circuit. The advantage of this circuit is, area occupied by resistors when realized with diode connector MOSFET is less. On the other hand, this circuit cannot generate a required voltage greater than $V_{DD}$-$V_T$ and less than $V_T$ because of swing constraints of the devices, as they are in saturation.

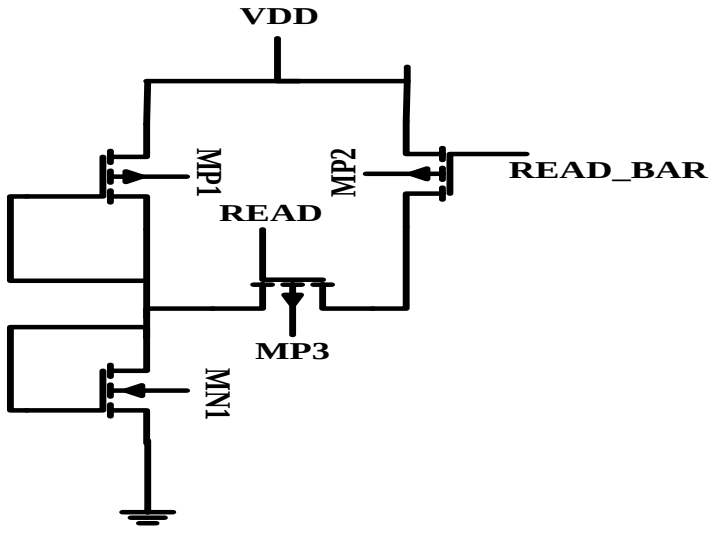



FIGURE 26: Diode Connector Voltage Divider

The related circuitry consisting of MOSFET for resistive divider with diode connector is shown in Fig.3.7.READ and READ_BAR signals are complement to each other. During READ signal, the circuit shown in Fig.3.4 acts like a voltage divider and passes reduced voltage to the circuit. During the duration of READ_BAR, full $V_{DD}$ supply will be passed to the memory cell.

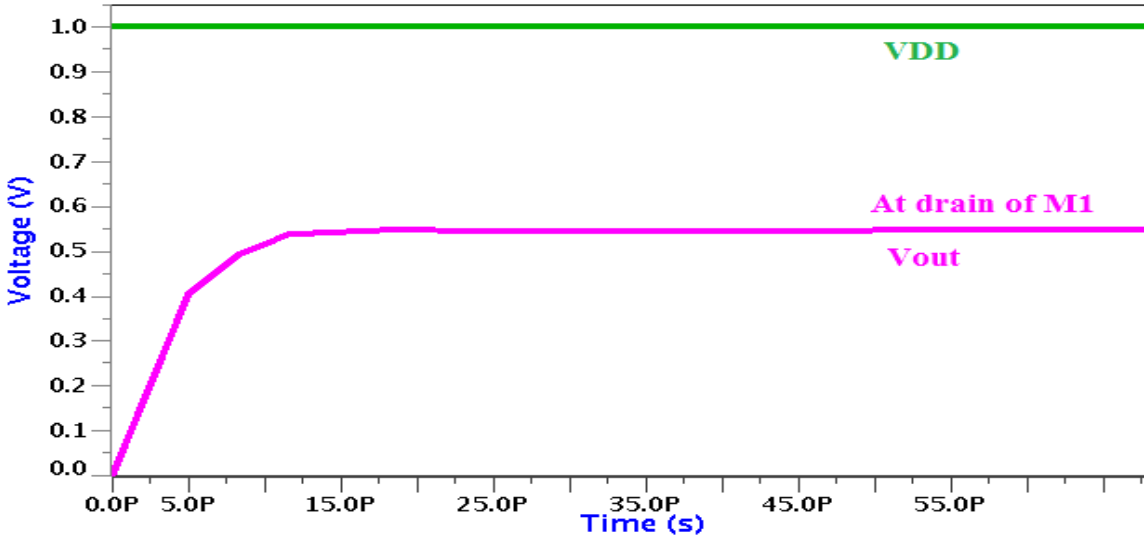



FIGURE 27: Transient Response for the Fig.26

### 3.2.3 RESISTOR DIVIDER-SWITCHING CAPACITOR

It is discussed in the previous section that the circuit realized with diode connector has limitation on swing voltages. In order to realize the resistor with capacitor, another alternative approach is proposed with switching capacitor. A simple sampling circuit consists of a switch and a capacitor. A MOS transistor can serve as a switch because (a) it can be ON while carrying zero current, and (b) its source and drain voltages are not "pinned" to the gate voltage, i.e., if the gate voltage varies, the source or drain voltage need not follow that variation. By contrast, bipolar transistors lack both of these properties, typically necessitating complex circuits to perform sampling. Transistor shown in Fig.3.8 is a PMOS, if NMOS is used in the below circuit then it will not pass strong $V_{IN}$ to the capacitor $C_H$.

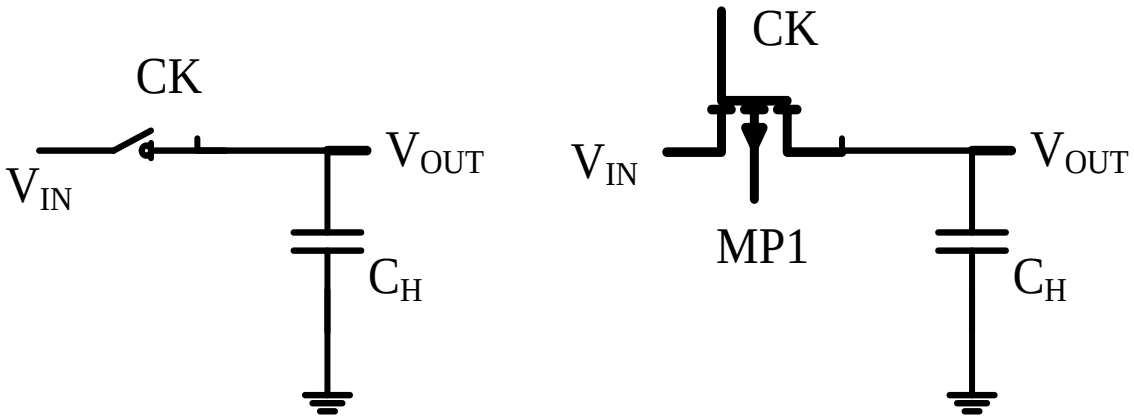



FIGURE 28: Switch and Capacitor with PMOS

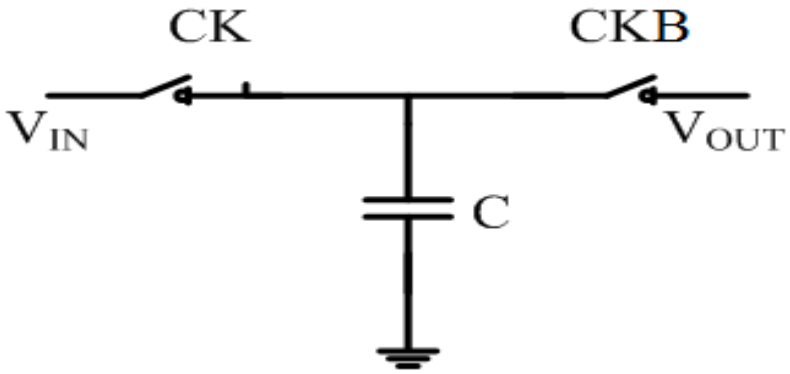



FIGURE 29: Switching Capacitor-Resistor

It can be observed from Fig.30 that a resistor is realized using switching capacitor circuit. CK and CKB are two non overlapping clock pulses. For a switching capacitor to act like a resistor, a very high speed switching clock is necessary. The transient response of the nodes Vc and Vout can be observed from Fig 31 and Fig 32. It can be seen from Figure 31 that the voltage across the resistor R is increasing, this is because the voltage which the capacitor charged in the period of CK will now gets discharges. It can also infer from the same figure, there is a voltage spike at voltage $V_{out}$.

Realization of resistor with switching capacitor demands a very high clock frequency, thus the idea of switching capacitor has dropped for the initial testing.

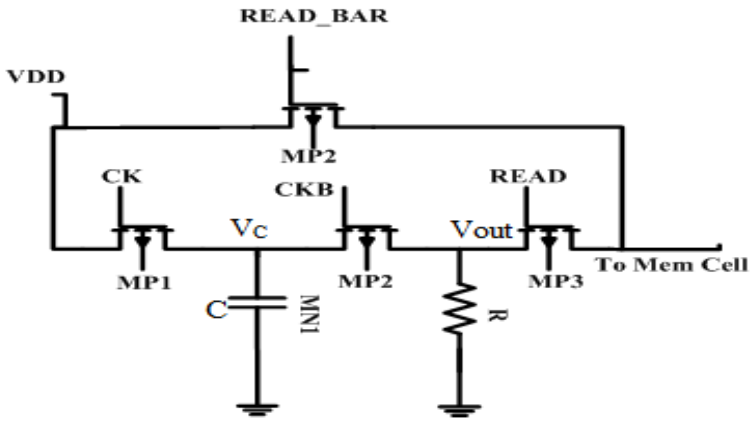



FIGURE 30: Switch and Capacitor with PMOS

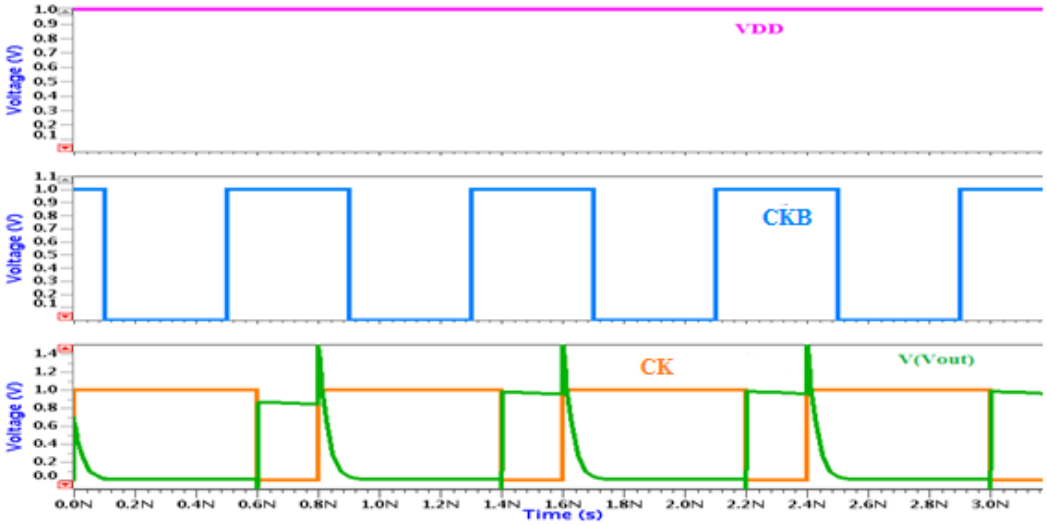



FIGURE 31 Transient Response of Fig.30

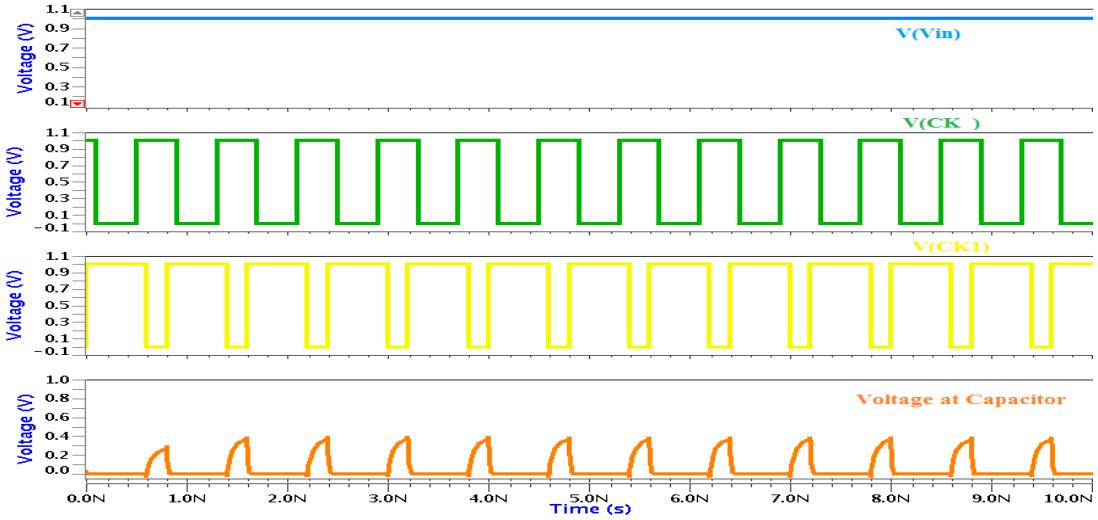



FIGURE 32: Transient Voltage $V_c$ Of Fig.30

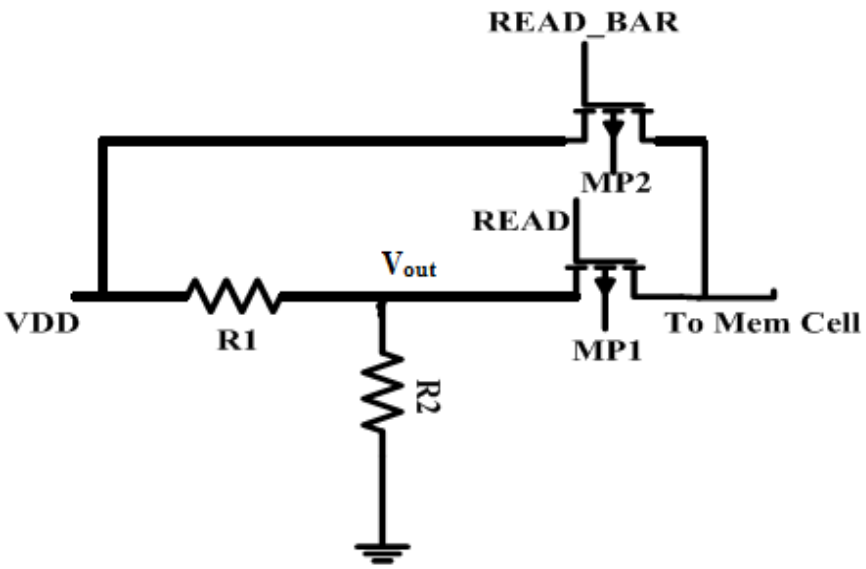



FIGURE 33: Voltage divider circuit

### 3.2.4 RESULTS

The resistive divider circuit shown in Fig.33 is used for testing the proposed methodology. During read cycle, the signal READ will be activated and the voltage occurred at node $V_{out}$ will be passes through PMOS MP1. During normal operation the supply voltage $V_{DD}$ will be passed through MP2 by activating READ_BAR signal.

Simulations are done for different resistance values R1 and R2. For a particular value of resistance, the variations of all the devices are represented with respect to the static noise margin (SNM) equation using linear regression.

TABLE 2 COEFFICIENTS CORRESPONDING TO SNM FOR ALL CELLS

| Coefficient | PDT | PDF | WLT | WLF | PUF | PUT | Constant | Correlation ($R^2$) |
|---|---|---|---|---|---|---|---|---|
| Value | -0.00705 | 0.013768 | 0.009082 | -0.00014 | 0.004119 | 0.0000918 | 0.208364 | 99.4 |

TABLE 3 : COEFFICIENTS CORRESPONDING TO SNM FOR WEAK CELLS

| Coefficient | PDT | PDF | WLT | WLF | PUF | PUT | Constant | Correlation ($R^2$) |
|---|---|---|---|---|---|---|---|---|
| Value | 0 | 0 | 0 | $-2.6X10^{-5}$ | 0.003035 | $5.84X10^{-6}$ | 0.0803 | 99.3 |

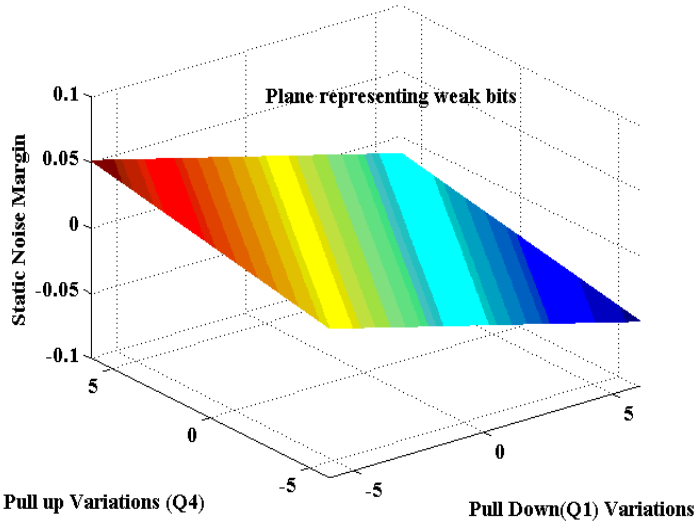



FIGURE 34 Linear Regression of the Weak Bit Plane

Above Fig.34 shows the plane of weak bits with respect to the Static Noise Margin after performing regression. The related coefficients/weights of all the devices are shown in Table 2.

# 4 BIT LINE VOLTAGE LOWERING

*This chapter is dedicated to identification of Weak cell with respect to Static Noise Margin. A hypothesis is proposed and the verification of the hypothesis and its incapability in detecting weak bits is discussed. A brief discussion on outputs is also presented for different process corners.*

## 4.1 INTRODUCTION:

The technology from semiconductor industry is being constantly pushed to improve the performance of SRAMs. As it is being discussed in the previous chapters, one solution is to scale down the physical dimensions of the circuit components. It is to be noted that that the Constant-voltage scaling (CVS) in the VLSI designs are being dominated at lower physical dimensions. As the length of the channels are scaling down, the velocity saturation due to the increasing electric field in short-channel transistors created a situation where even after further voltage scaling did not give a performance advantage over the constant- field scaling [3]. In other words, since the drain current in short-channel transistors is no longer a quadratic function of drain voltage (Reference, Waterloo Thesis), the gain of an increased drain current has become less important than the penalty of a higher voltage causing the increased power dissipation. Constant Field Scaling requires, decrease of supply voltage which in turn results in decrease in Noise Margins of SRAMs. On the other hand random distribution of the dopant atoms in the channel makes the behaviour of the transistor uncertain and leads to decrease of noise margins. It can be referred from chapter 3 that how the $V_{DD}$ lowering will affect the SNM and could able to detect the weak cell w.r.t less Static Noise Margin.

## 4.2 BIT LINE VOLTAGE LOWERING - SNM CORRELATION:

This section discusses about variation of Static Noise Margin (SNM) with lowering of bit line voltages while reading the memory cell. $V_T$ variations in all the devices of 6T SRAM cell shown in Fig.4.1 (right) are introduced using Design of Experiments (DoE) in 28nm environment. A standalone circuit with a load of 512 rows and pulse duration of 1.5ps is considered for read operation and simulated in ELDO Spice 13.2b for different corners for observing the correlation between SNM of the memory cell at normal conditions and SNM of the cell at reduced bit line voltages.

In order to illustrate the method for identifying the weak bit in SRAM w.r.t stability consider the transfer curve shown in figure 4.1. Figure 4.1 represents the transfer curve of two inverters connected back to back, in which the curve represented in green is SNM of weak and the curve presented in blue represents SNM of a good SRAM cell. M1 and M2 represent the Meta stable points of good cell and weak cell respectively. Assume that node A of an SRAM cell has state "1" and that the bit lines are pre-charged to a known value.

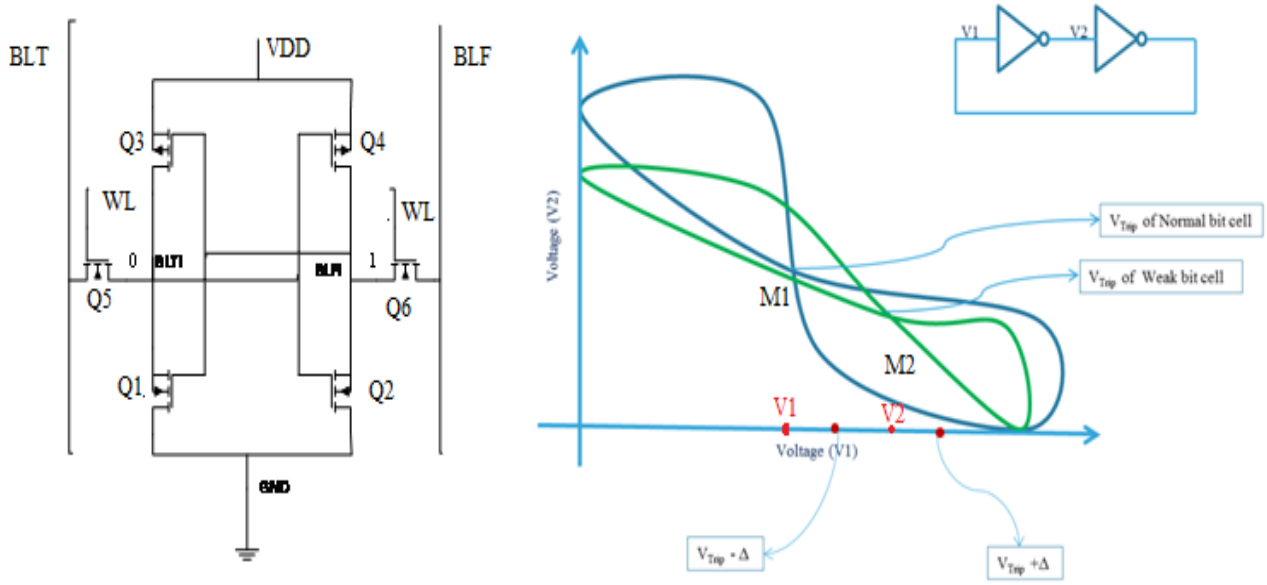



FIGURE 35 Standard 6t SRAM Cell (Left) SNM Curves (Right)

Assume that node BLFI of an SRAM cell has state "1" and that the bit lines are pre-charged to a known value. Now assume that by certain manipulation, the Voltage of node BLFI is reduced from a stable state to a certain voltage. It can be observed that the trip voltages of the strong and weak bit are $V_{trip}$ and $V_{trip1}$. Now consider that the SRAM array have some weak bits. The bits which are weak will have a deviation of the trip point to left or right from the strong cell trip point. This method includes varying of the bit line voltage (test voltage) of memory cell from Vtrip and $V_{trip+\Delta.}$

By varying the bit line voltage it can detect the weak bits as follow. From the above figure we can conclude that the weak bit will have less SNM and thus it is very prone to change its state. So it can be deduced from above figure4.1 when the voltage is raised from $V_{trip}$ and $V_{trip+\Delta}$ strong bit will not change its state but if that bit is weak bit means it will change its state and thus allows detecting the weak bits.

## 4.2 STANDALONE SIMULATIONS:

According to the hypothesis, we have to compare the SNM at 0.9V with of nominal temperature $25^0$C with the SNM at 0.7 and worst case temperature. These two should correlate according to the hypothesis. As we know that the SNM at 0.7V should be lesser than the SNM of bit cell at 0.9V, the correlation graph should be more or less like a straight line. Since the data flips at lower SNM so we are not really interested in the higher SNM value because data wouldn't flip at higher SNM. So we consider the sample points which are nearly about origin.

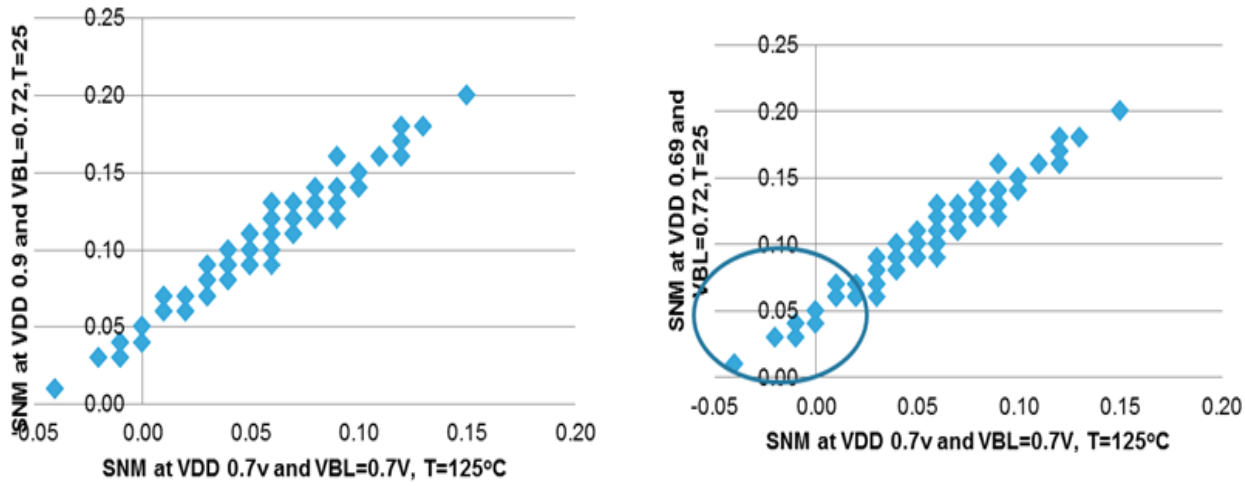



FIGURE 36 : MaxMin Variation

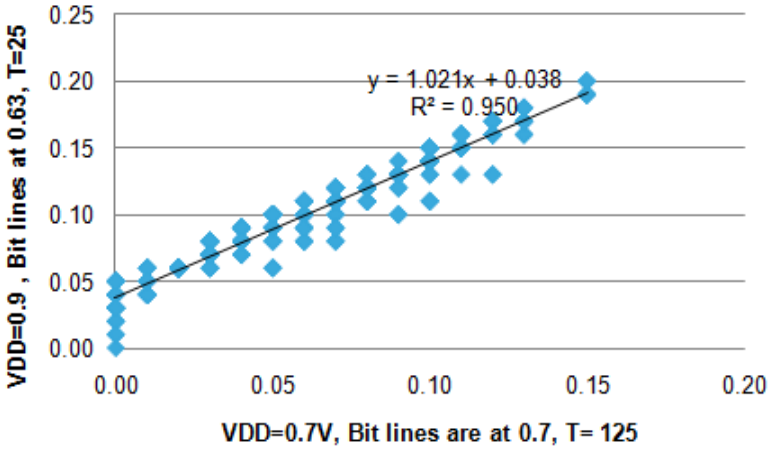



FIGURE 37 MaxMin Variation

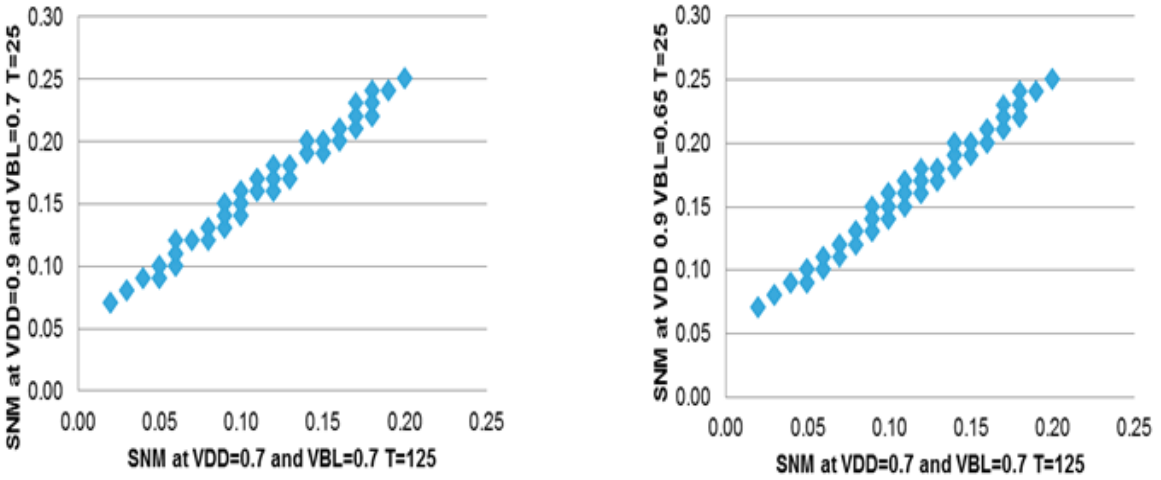



FIGURE 38 : TypTyp Variation

| MAXMIN | |
|---|---|
| Bit line Voltage | Correlation |
| 0.63V | 95.5 |
| 0.64V | 96.3 |
| 0.65V | 95.2 |
| 0.7V | 94.4 |

| TYPTYP | |
|---|---|
| Bit line Voltage | Correlation |
| 0.63V | 94.3 |
| 0.64V | 97.3 |
| 0.65V | 98.2 |
| 0.7V | 98.1 |

## 4.1 RESULT DISCUSSION

From the above Figs 36-38 and tables it can be observed that maximum correlation of about 95 to 96% has occurred when the bit line voltage range of about 0.63 to 0.73V, but there are few samples (observe the area which was highlighted with a circle) where the SNM at 0.7V is deviating very largely when compared with SNM at 0.9V. This means there are few samples which this test method is cannot able to identify as weak bits. This test when performed on silicon could give some weird results.

## 4.2 RESULTS AT OTHER CORNERS

In order to observe the effectiveness of the method, correlation is seen at other process corners Min-Min and Max-Max also between normal conditions and the worst case conditions.

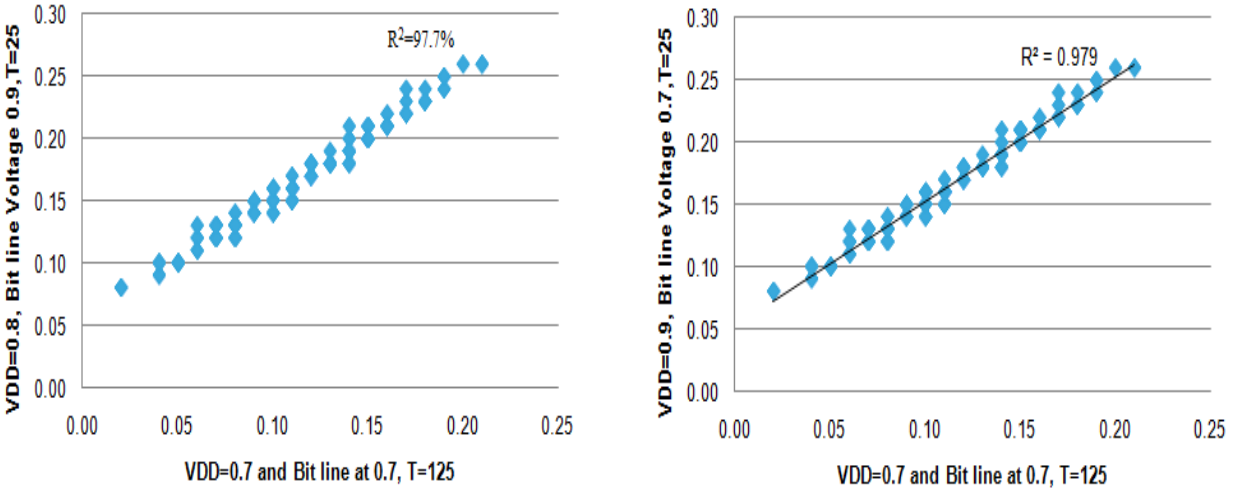



FIGURE 39 MinMin Corner

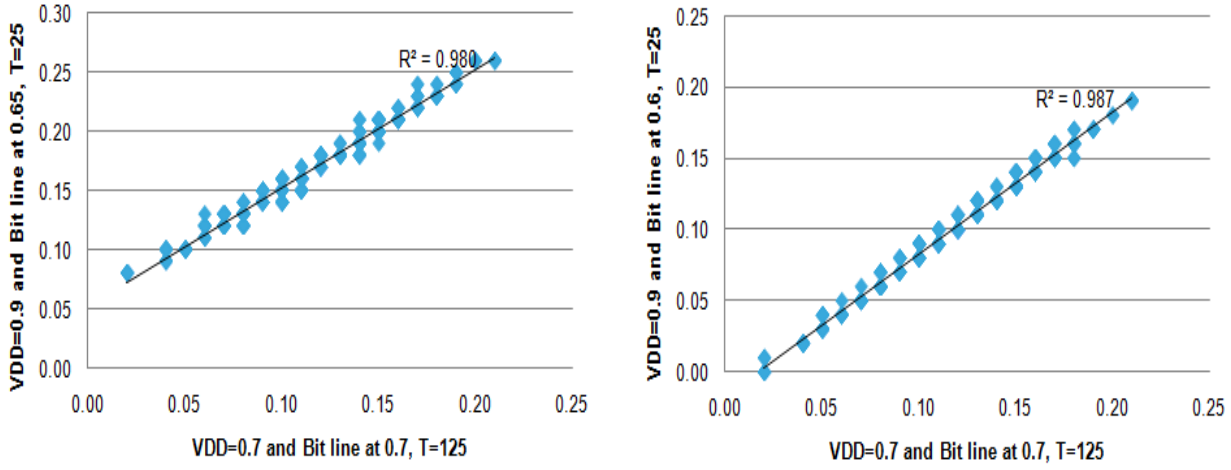



FIGURE 40 MinMin Corner

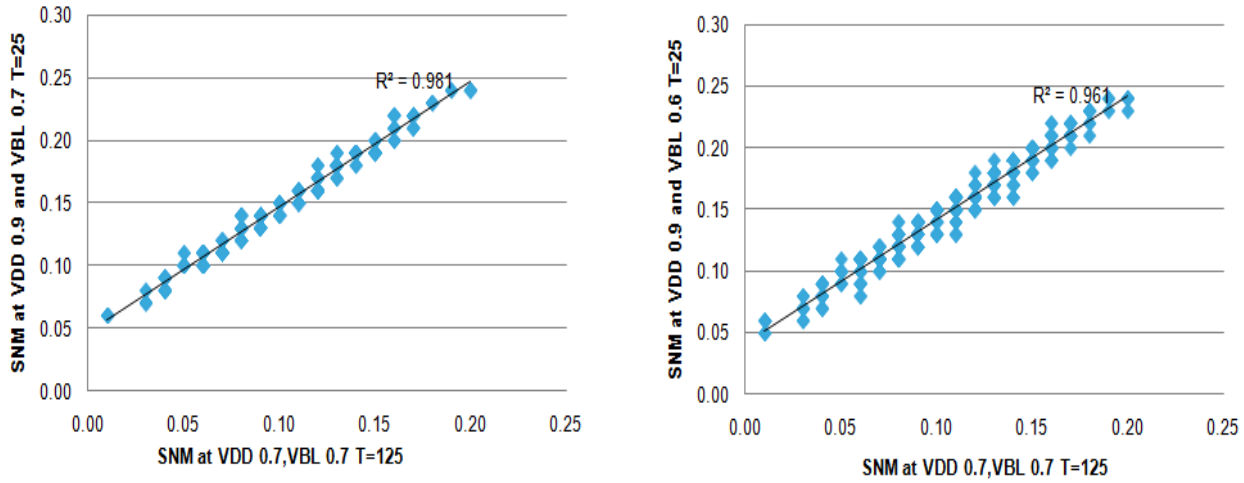



FIGURE 41 MaxMax Corner

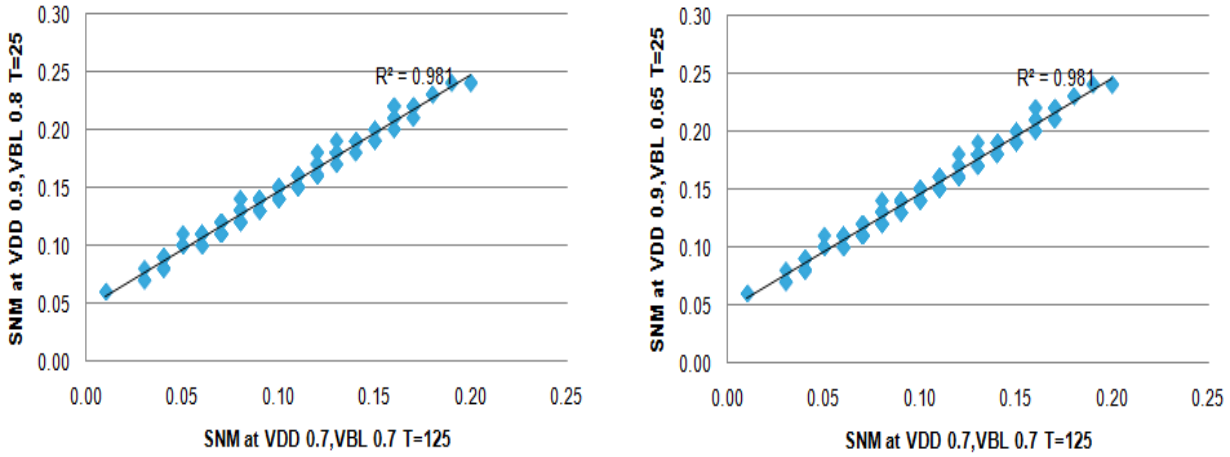



FIGURE 42 MaxMax Corner

# 5 FUTURE WORK & CONCLUSION

*This chapter discusses about a methodology for detecting with respect to write margin. All the analysis was carried out in standalone mode. Further Conclusion of this dissertation follows.*

## 5.1 WEAK BIT DETECTION-WRITE MARGIN

In this section, a methodology for detecting the weak bits in SRAM with respect to bit line write margin is discussed. In [26], it has been discussed an approach to detect weak bits, a weak write is performed on the memory cell instead of performing strong write. An alternative approach verified in this dissertation for the detection of weak bits in standalone mode. However, verification of the proposed method in not validated by using critical path.

The methodology can be explained as, "Improvise the write operation and perform a destructive read operation". Write margin of the cell can be improved by lowering $V_{DD}$, a write operation can be made destructive by increasing the bit line voltage. Fig.41 depicts the steps of proposed and discussed [26] methodologies.

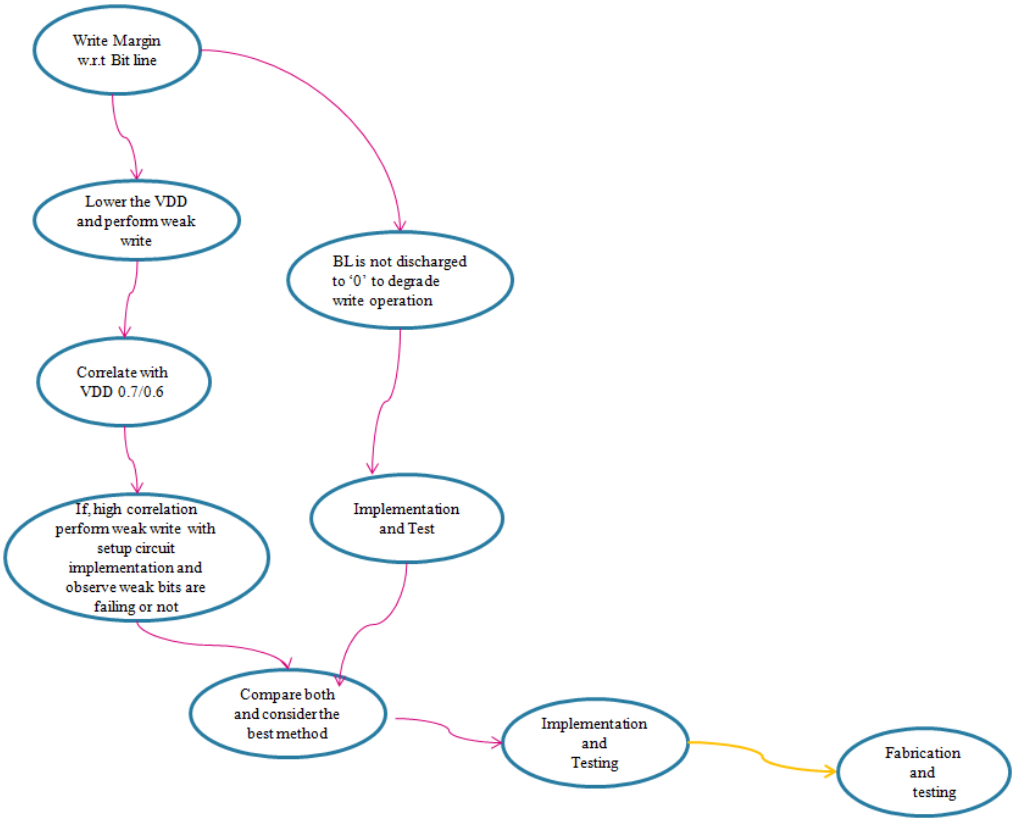



FIGURE 43 $V_{dd}$ Lower with Bit Line high (Left Branch) and Bit line voltage high (Right Branch)

Correlation of above proposed method is verified on a memory cell for a load of 512 rows and pulse duration of 2ps in ELDO 13.2b in standalone operation.

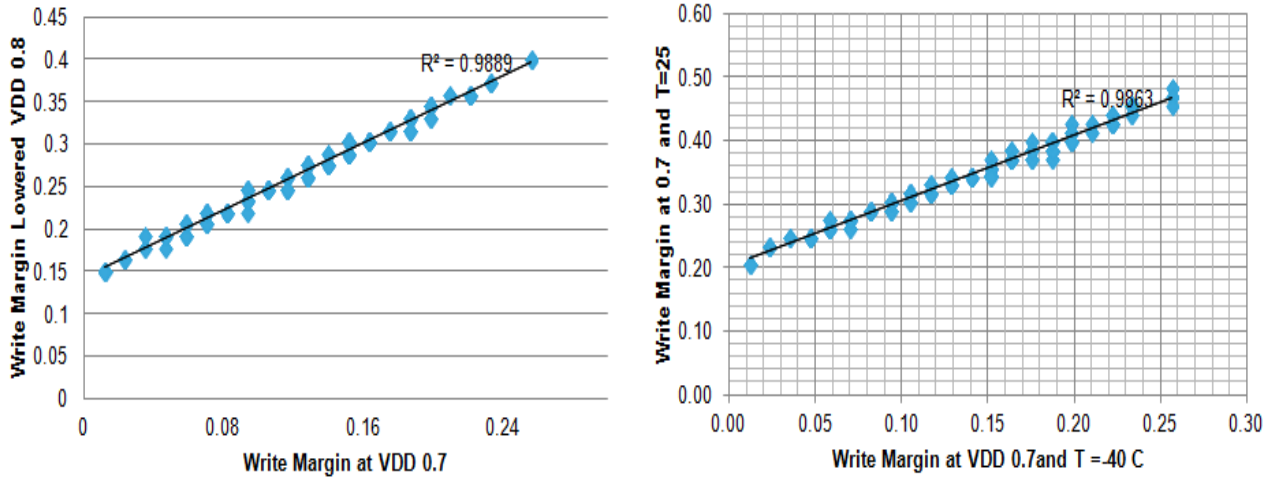



FIGURE 44: MinMin Correlation

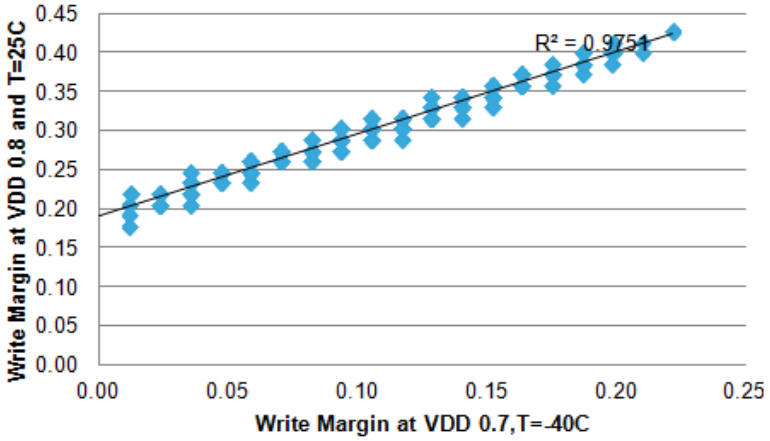



Figure 45: MaxMax Correlation

Simulations are carried out at Maxmax and Minmin corner because, leakages are more at Maxmax and leakages will be less at Minmin corners. It can be observed from above Figs 44-45 that there is a very high correlation between write margins between normal conditions (VDD=0.9V and T=25C) and the worst conditions (VDD=0.7 and T=-40C)

It can be noted that the write time and the write margin of a memory cell follows almost nearly inverse relation. In order see the advantage of the proposed methodology, correlation between the write times and write margin is observed for different voltages. A scattered of weak and normal bits are plotted. It can be observed from fig.46 (right) that, the test which is proposed in [26] is very aggressive for small changes in bit line voltages. That means for a small variation of

the voltages, there is a chance of disturbing a huge number of normal cells. As a result normal cells will be caught as weak cells. Stability comparison w.r.t number of bits failing for variable bit line voltage can be observed in Fig.47

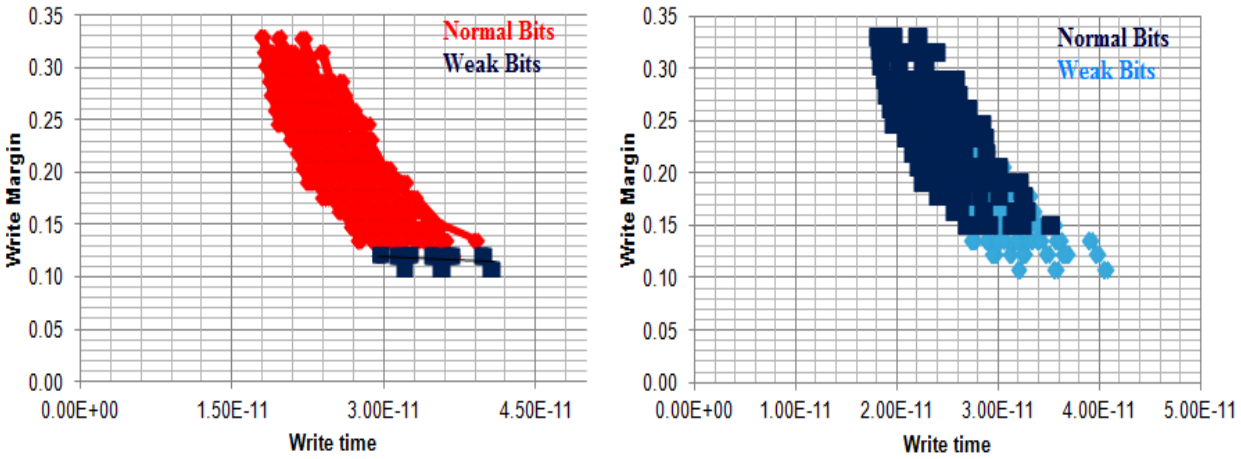



FIGURE 46 Stability Comparison of $V_{dd}$ Lower with Write Disturb (Right) and Write Disturb (Right) Tests

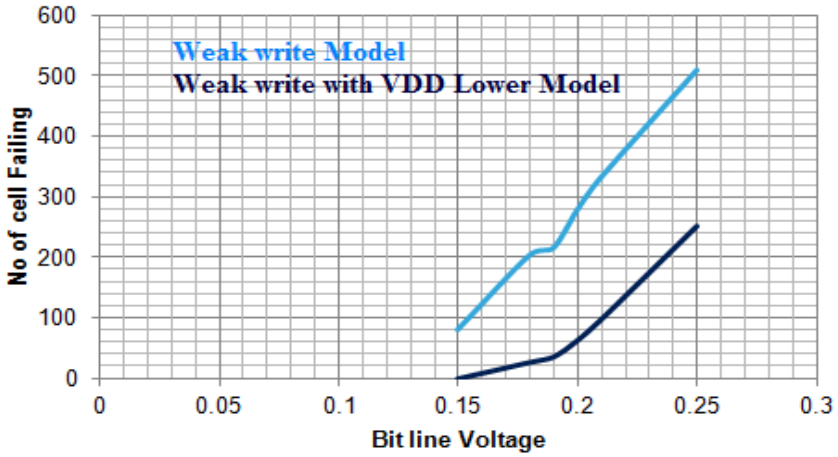



FIGURE 47: Stability Comparison of Both Models

## 5.2 FUTURE WORK

In this work we have shown how to detect sequence sensitizing fault such as a quick read-after-write operation. Layout design of an SRAM cell plays a major role in ensuring cell stability yield maximization. Proximity effects on the critical diffusion, poly, contact etc… can degrade the SNM and hence the performance of SRAM cell. Layout-dependent capacitance on the critical nodes and their collection efficiency affect the soft error immunity. Maximizing the SNM by

increasing the driver transistor size makes a cell faster but the packing density is reduced. A co-optimization study of SNM, soft-error immunity, speed and packing density for various bit cell architectures is an interesting topic for future work. New methods such as enhancing the characteristics of memory cell and then degrading the performance can be an interesting topic for extending the work.

## 5.3 CONCLUSION

In this dissertation, we have discussed different methodologies for detecting weak bits in SRAM cell with respect to write time, Static Noise Margin, Write margin. We also have presented a new method for realizing setup circuits based on charge sharing techniques and resistor divides. Challenges and limitations of other circuits were also presented in this work. In chapter 5, a thorough discussion on the stability of write margin method is presented followed by conclusion.

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