Exploration of Test Methodologies to Detect Weak Bits in SRAMs

by

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Certificate

This is to certify that the thesis titled "**Exploration of Test Methodologies to Detect Weak Bits in SRAMs"** being submitted by Nidhi Batra to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original research work carried out by her under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

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Acknowledgements

Abstract

Embedded memories will continue to dominate the System-on-Chip (SoC) area in subsequent years. SRAMs are designed to exploit the technology limits to achieve highest storage capacity, minimum access times and operating voltages. Consequently SRAMs are prone to manufacturing losses. In advanced technology nodes, process limitations and device variations limit the SRAM performance and yield. Intra-die mismatches, process shifts, random variations in device parameters such as Threshold Voltage (V_t) and effective channel length and other defects are inevitable. The increased process spreads of modern scaled down technologies can compromise the stability of SRAM cells. All these result in the increase in probability of SRAM cells becoming weak for such highly dense memories. The performance parameters, majorly cell stability, and other Figures of Merit (FOMs) of a weak cell get deteriorated which lead to reliability issues in the SRAM. A weak cell might accidentally flip its contents during some worst case operating conditions.

However, memories designed in state-of-the-art technologies like Fully Depleted Silicon on Insulator (FDSOI) possess several performance benefits due to dopant free channel, but the impact of process variations, resistive defects, transistor mismatches, IR drops and coupling still exist in SRAM core causing cell weakness. To ensure reliability of SRAMs, it is important to identify such weak cells post silicon. In this work, a comprehensive analysis on the weak cells and their effect on various FOMs have been conducted. Based on the limitations of the existing stability fault detection techniques, techniques for the identification of weak cells in SRAMs have been explored. Here, correlation based test methodologies for the efficient detection of weak bits in SRAMs have been proposed. The proposed methodology targets high speed testing at lower test costs. It enables to perform the test at nominal operating voltage and room temperature. For verification of the test methodologies, case study is conducted for a single port SRAM instance in 28nm FDSOI technology. The work presented in this thesis is carried out at ST Microelectronics.

Publications

1. "Static Noise Margin based Yield Modelling of 6T SRAM for Area and Minimum Operating Voltage Improvement using Recovery Techniques", 26th IEEE Great Lakes Symposium on VLSI (GLSVLSI) 2016, Boston, USA.

2. "An Effective Test Methodology Enabling Detection of Weak bits in SRAMs: Case Study in 28nm FDSOI", 20th IEEE International Symposium on VLSI Design and Test (VDAT) 2016, IIT Guwahati, India.

3. "A Method to Estimate Effectiveness of Weak Bit Test: Comparison of Weak pMOS and WL Boost based Test - 28nm FDSOI Implementation", (Submitted to IEEE SOCC 2016).

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Chapter 1

Introduction

This chapter provides a background of the SRAMs and their position in memory hierarchy. It also highlights the motivation for carrying out this work. Section 1.1 gives the overview of memories in SoCs. Section 1.2 describes the SRAM cell design and its operation. Section 1.3 presents the basic architecture of SRAMs adopted in present day technology. Section 1.4 introduces about the SRAMs designed in FDSOI. Section 1.5 highlights the motivation for carrying out this work. Section 1.6 presents the related work. Section 1.7 describes the chapter break-down of the thesis.

1.1   Memory Overview

Memories play a vital role in the rapid growth of the Complementary Metal Oxide Semiconductor (CMOS) technology and the semiconductor industry products. With the advancement in process technology, memory capacities have been drastically increased. The diverse use of memory in processor and its applications has led to a memory hierarchy, ranging from small capacity cache to large capacity external storages. Figure 1.1 shows a typical memory hierarchy in any advanced processing unit or a computer. It reflects the growing cost and speed moving from high capacity secondary storage to small capacity Central Processing Unit (CPU) registers. The need of several levels of cache aroused in order to meet the increasing processor speeds. The processor cycle time is rapidly reducing and the performance gap between processor and memory access is increasing. This has led to the introduction of high speed caches in the memory hierarchy.

On-chip L1 and L2 caches are comprised of Static Random Access Memory (SRAM). The amount of on-chip caches and number of processor cores in a system trades-off the performance and cost of the chip. To increase the on-chip cache capacities, for enhancing system performance, high density embedded SRAMs are used. The reduced supply voltages of the new technology nodes pose a higher risk of soft errors that can be even more problematic for the scaled down embedded Dynamic Random Access Memories (DRAMs). Due to the reduced charge stored on the DRAM capacitor and the absence of latching feedback mechanism as in SRAMs, embedded DRAMs can be more susceptible to α-particles and cosmic rays.

Now-a-days, almost all the electronic equipments comprise of embedded SRAMs within the chip. Many of the applications of embedded SRAMs include:
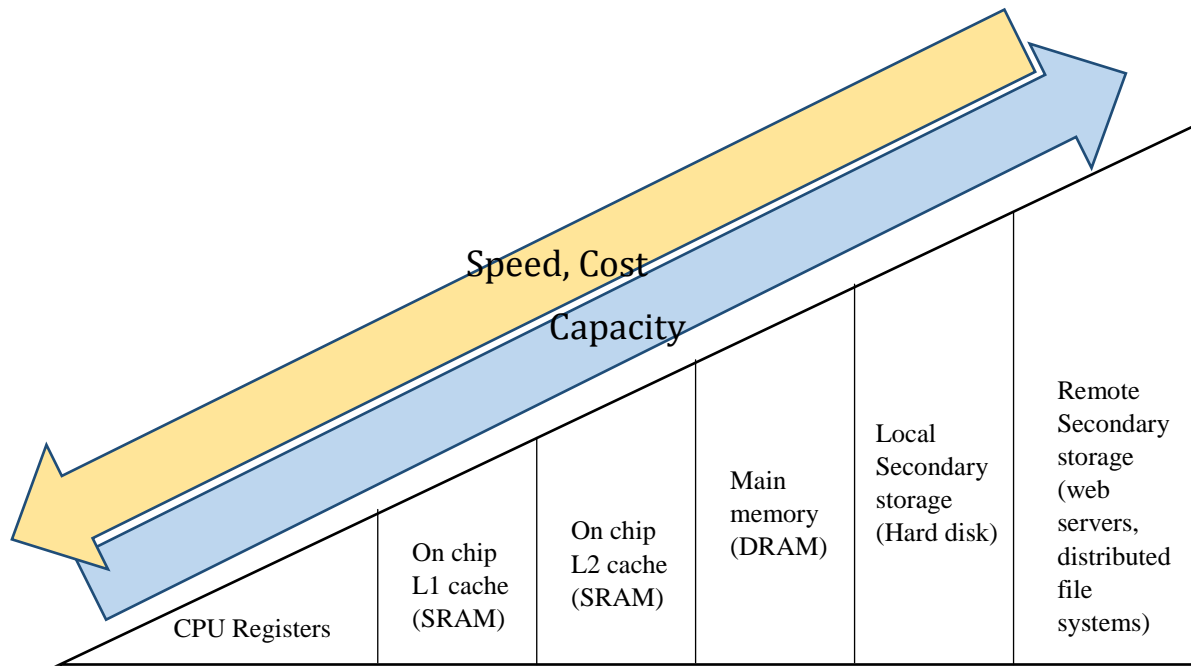
Figure 1.1   Memory hierarchy in advanced processing system / computer

- High performance computing,

- Wearable electronics,

- Medical and Automotive electronics,

- Mobile phones and Tablets,

- Smart homes and many more.

As a result, SRAM cell size continues to scale down, driven by the need of high-performance processor with large caches. SRAM cell area hence becomes a key determinant of the product cost and one of the foremost Figure of Merit (FOM) of the cell. According to Moore's Law, in order to double the on-chip functionality every two years, technology-node scaling of 0.7 in linear size and 0.5 in area has to be carried out every three years; as well as an additional device/process design improvement of 0.8/(2 years) must be achieved. A typical ASIC design is assumed to have same transistor density as high performance MPUs, which mostly consist of SRAM transistors [1].

SRAM memory cell design involves lot of optimization, owing to the above reasons, to achieve the required performance with high target chip density. In order to achieve this, certain design measures are adopted. Transistor count for a cell is reduced, transistors sizes are reduced as far as possible, SRAM architecture is optimized in banks and cell arrays, and layouts as well are optimized.

1.2   SRAM Cell Design and Operation

The simplest design of the SRAM array is shown in Figure 1.2. The array is divided into rows and columns. Every cell stores one bit information. SRAM architectures generally follow 2-dimensional addressing scheme, row and column addressing. Row decoder decodes the row address and activates one of the wordlines, to select a row. A particular cell in a row is further selected by the column decoder. Hierarchically, memory cells are arranged in cores, which can be further divided into blocks and arrays depending on the system speed and power requirements.
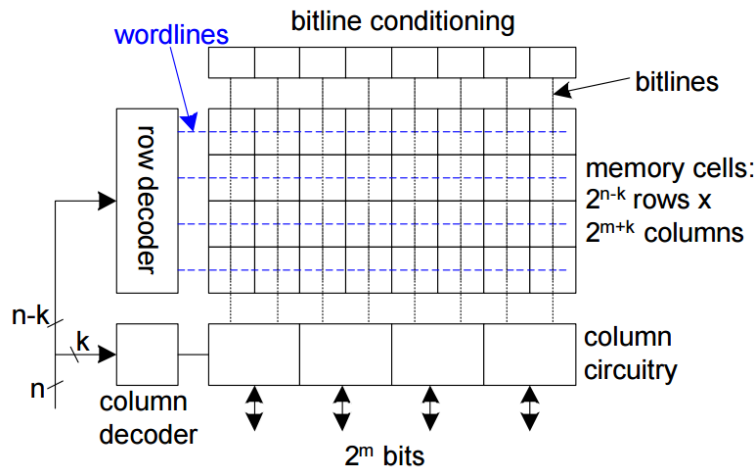
Figure 1.2   Simplified view of a SRAM array

1.2.1   6-T SRAM Cell

Memory cells are the key components of any SRAM serving for storage of binary information. A typical SRAM cell is comprised of two cross-coupled inverters forming a latch and access transistors. Access transistors enable the read and write access in the cell for the selected cell and provide isolation during the non-accessed state of the cell. An SRAM cell has to provide non-destructive read access, write capability and infinite storage (or data retention) time, till the power is supplied to the memory.

The 6-T cell design considerations represent a trade-off between cell area, robustness, speed and power. Cell size minimization is one of the most important design objectives. A smaller cell allows the number of bits per area to be increased and hence decreases cost per bit. Reduced cell size can indirectly improve the speed and power consumption due to the reduction in the associated capacitances. However, the cell area might have to be traded-off for high performance or low power or some other special functionality requirements.

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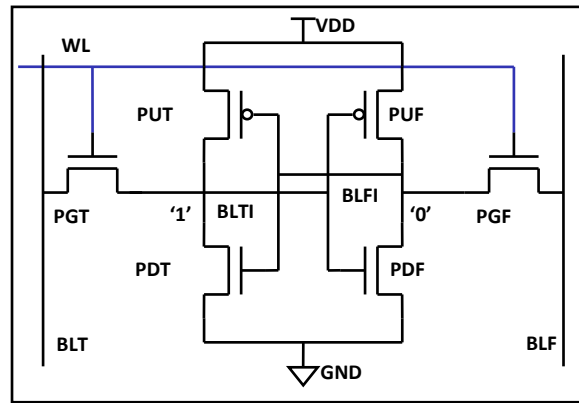
Figure 1.3   Schematic of standard 6T SRAM cell

A typical 6-T CMOS SRAM cell is shown in Figure 1.3. It consists of 6 transistors and is similar to one of the implementations of an SR latch. Transistors PDT (pull-down true side), PUT (pull-up true side), PDF (pull-down false side) and PUF (pull-up false side) comprise the two cross coupled inverters and the access transistors PGT (pass gate true side) and PGF (pass gate false side) provide the read and write access to the cell. The positive feedback of the cross coupled inverters corrects the disturbances caused by noise or leakage. Upon the activation of the word line (WL), the access transistors connect the two internal nodes (BLTI and BLFI) of the cell to the true (BLT) and complementary (BLF) bitlines.

The central challenges in SRAM design are minimizing its size and ensuring that the circuitry holding the state is weak enough to be overpowered during a write, yet strong enough not to be disturbed during a read.

1.2.2   Cell Read Operation

The cell read operation starts by pre-charging both the bitlines to the supply voltage. Then the WL is asserted for the cell which is to be read. This connects the pre-charged bitlines, BLT and BLF, to the internal nodes through pass gates.

When the word line is raised, BLF is discharged through pass gate (PGF) and pull down (PDF) transistors, while BLT retains its high level. So there is a potential difference which is created between the two bitlines. This difference is further detected by a sense amplifier to finish the cell read operation.

Transistors PGF and PDF form a voltage divider. While the BLF is discharging through PGF and PDF transistors, the voltage of the node BLFI rises slightly. This operation is illustrated is Figure 1.4. To ensure the non-destructive read operation, the ratio of the pass gate and pull down sizes needs to be optimized. This is because if the voltage bump created at

the internal node, BLFI is large enough to exceed the threshold of the other inverter, then the cell contents might flip. This will affect read stability of the memory cell. The ratio of the transistor widths of pull down to pass gate is generally defined as the cell ratio. The SRAM cell needs to be designed such that the cell ratio is greater than 1 to maintain cell stability.

The bump voltage which the cell can tolerate without flipping the cell contents is defined as Static Noise Margin (SNM) of the cell. SNM is very critical FOM of an SRAM cell. It is decisive of the cell stability and is dependent on various factors. It is one of the key inputs which is taken care of during thr SRAM cell design.
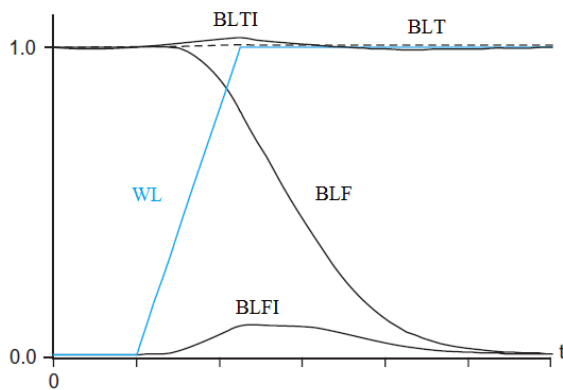
Figure 1.4   Read operation of 6T SRAM cell   Figure 1.5   Write operation of 6T SRAM cell
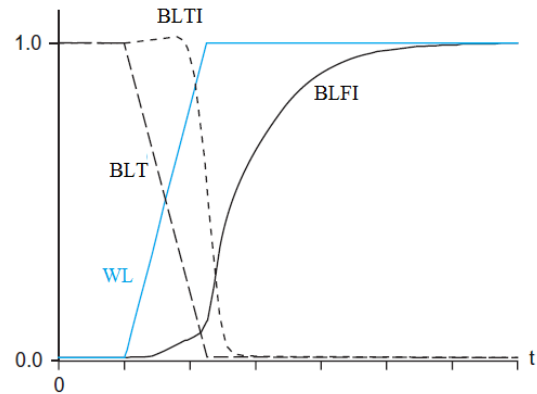
1.2.3   Cell Write Operation

Figure 1.5 shows the SRAM cell being written. BLFI and BLTI are initially storing '0' and '1' respectively. In order to write the opposite cell content to the memory, the bitline BLT is driven to the ground potential with the help of a write driver circuitary. And the other bitline, BLF is normally kept precharged to the supply. The read stability ensures that the precharged BLT will not flip the stored '0' at BLFI to '1'. But, to write the cell, the node, BLTI will discharge through the pass gate PGT. This will further force the node BLFI to flip to logic '1' through the inverter action. And hence, the cell will be overwritten to its new value.

In order to ensure that the node BLTI is overwritten, the strength of pull up transistor (PUT) plays a critical role, as it tries to supply the logic high at the node BLTI. This opposes the overwriting to '0' at that node. Hence, the sizing of pull up transistors needs to be done carefully. To ensure writability, pull up transistor should be weaker than the pass gate. The ratio of the sizes of pull up to pass gate transistors defines the pull up ratio and it is also a design parameter.

Conclusively, for a SRAM cell design, to ensure both read stability and writability, the nMOS pull down transistors must be strongest. The access transistors should be of intermediate strength and the pull up transistors must be weakest.

1.3   SRAM Basic Architecture
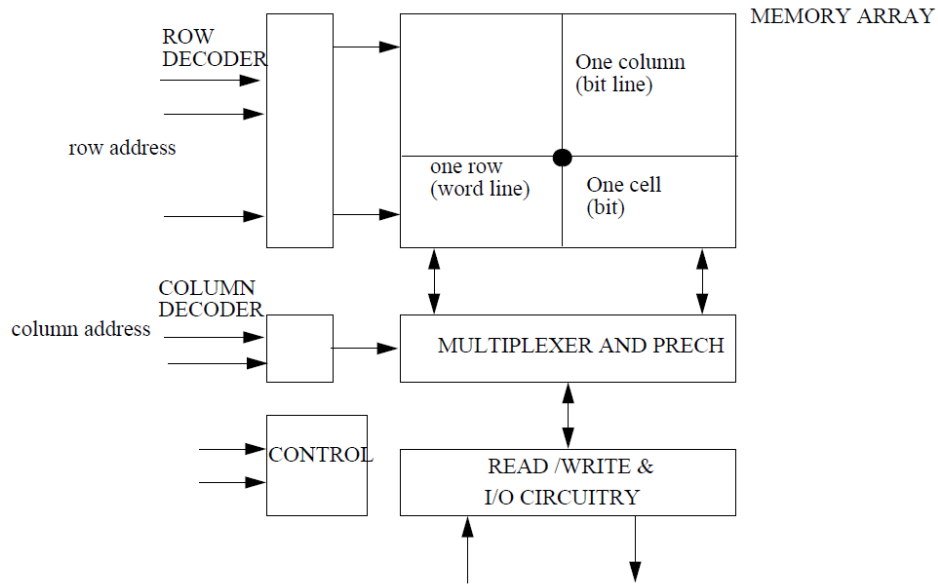
Figure 1.6   Basic architecture of a SRAM

SRAMs achieve higher density by not only using dense storage element, but also by organizing them in a structured manner. SRAM cells are organized into rows and columns to achieve a desired capacity (words x bits). Input addresses are decoded in decoders to select the desired word. Generally, 2-dimensional decoding includes row and column decoding. Several decoding schemes are used for different applications in order to optimize SRAM area, power and yield. Many words share the output circuits to minimize the area and power requirements. Figure 1.6 depicts one of the basic architectures of a SRAM. Apart from the core design, the periphery circuits also play a crucial role in the overall SRAM design. These circuits are decisive of the SRAM operation and performance. Other than address decoders which enable the core access, SRAM architecture also constitutes circuitry to aid the read and write operation such as sense amplifiers, write drivers, and precharge circuits.

In addition to decoders and multiplexers and I/O buffers, modern SRAMs include many more circuits to enhance its functionality – for example, power switches, different levels of address decoding to improve speed and area, input latches to minimize signal hold time requirements, and so on. These additional circuits and functionality require management of a complex state machine and is a part of 'control' region of the SRAM. The array region

includes the basic storage elements, the SRAM cells. Decoder region includes address decode circuits to select desired rows. I/Os include column decoders and input/ output circuits in addition to circuits required to access the information in SRAM cells. Control region houses the state machine of the SRAM.

Other than the basic architecture depicted in Figure 1.6, current state-of-the-art architectures include complex circuits governing the timing of the SRAMs, to enable faster memory access. One such architecture is Self-timed architecture, which is also referred in this work.

1.3.1   Self-timed SRAM architecture

Figure 1.7 shows one of the ways of achieving a self timing in SRAMs. It includes dummy cells, dummy rows and columns. The dummy region of the SRAM is responsible for controlling the timing of the read and write operations in the memory. For instance, during the read operation, the difference created in the bitlines' voltages is detected by the sense amplifier. The sense amplifier needs to be triggered at the correct time when sufficient voltage difference has been created. The dummy setup in the SRAM array follows the actual intended read/write timing in the memory. It has the similar charge/discharge times for the internal capacitances. The dummy sense amplifier (DSA) controls the triggering of the sense amplifier for the SRAM array.
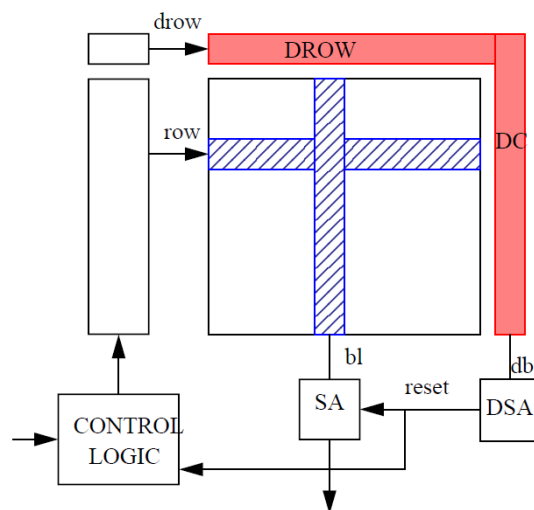
Figure 1.7   Self-timed architecture of SRAM

There may be other similar architectures for controlling the SRAM read/write timing in an efficient and fast manner, driven by specific application demands.

1.4   SRAMs in FDSOI

Technology scaling and high density in memories leads to increased leakage and power dissipation. The device scaling and lower voltage operation results in process variations and random dopant fluctuations which degrades the performance of SRAMs. This arises the need of new technologies and memory design techniques to reduce leakage, power dissipation, and device variations (number of dopant atoms in the channel). For technology nodes of 28nm and lower feature size, traditional CMOS using silicon base is not fully capable of meeting the future demands considering the p-n substrate leakages, carrier tunneling, variability issues, short channel effects etc are growing concerns when technology scales. Bulk technology faces challenges such as scaling challenges for performance, power and area; low power and high speed requirements; and process complexities.

Silicon on Insulator (SOI) technology is one of the new, state-of the-art technologies which offer some solutions to the discussed problems [2]. Some of the feautures include:

- It reduces drain-source coupling and hence reduces short channel effects.
- Experiences lesser leakage because of elimination of parasitic diodes to the bulk.
- Lowers Soft error rate.
- No latch up, (parasitic BJT).
- Fully depleted SOI (FDSOI) offers excellent electrostatic control of the transistor, acts as a performance booster, enables lower VDD, and hence lowers power consumption, while reaching remarkable performance.

The above features make FDOSI an excellent candidate for the design of SRAMs, offering several performance benefits. [3,4].

1.5   Motivation

Embedded memories will continue to dominate the System-on-Chip (SoC) area in subsequent years [5, 6]. SRAMs are designed to exploit the technology limits to achieve highest storage capacity, minimum access times and operating voltages. Consequently, SRAMs are prone to manufacturing losses, which govern the SoC Yield (Y). To ensure reliability, the cell stability is of prime concern. In present scaled down technologies, intra-die mismatches, process shifts, random variations in device parameters such as Threshold Voltage (V_t) and effective channel length and other defects are inevitable. This results in the increase in probability of SRAM cells becoming weak for such highly dense memories. The performance parameters, majorly cell stability, and other Figures of Merit (FOMs) of a weak cell get deteriorated which lead to

reliability issues in the SRAM. However, memories designed in state-of-the-art technologies like Fully Depleted Silicon on Insulator (FDSOI) possess several performance benefits due to dopant free channel [3][4], but the impact of process variations, resistive defects, transistor mismatches, IR drops and coupling still exist in SRAM core causing cell weakness.

The definition weak cell doesn't replicate any Fault in the cell. A weak cell does not fail at nominal operating conditions, but it might flip at some other PVT. Any disruption in the normal memory operation such as supply voltage fluctuation, coupling noise, read/write cell disturbs, excessive temperature variations etc. might force a weak cell to flip its state. Owing to the specified reasons, the weak cells may fail at any time but generally pass the traditional SRAM functional tests. Therefore, it is essential to explore the techniques which allow the detection of such kind of weak cells present in SRAMs, in order to minimize the test escapees and ensure reliability.

None of the existing stability fault detection tests correlate the impact of test stress with the tested FOM. In this work, we propose correlation based test methodologies to detect weak cells w.r.t Static Noise Margin (SNM) in SRAM. Though a weak cell may possess weak SNM, weak write time, weak write margin or bad retention, but we address cell stability here as it is most crucial and yield limiter in nanoscale technologies including FDSOI. In context with SNM, the *weak cells* are defined as the cells with degraded or insufficient SNM which might force the cell to flip its state during read operation. As a guideline, [7] suggests that $\mu - 6\sigma$ of SNM is required to exceed nearly 4% of V_{DD} to reach a 90% yield on 1Mb SRAM. This suggests that for an SRAM cell to be stable, it should have an SNM above some threshold SNM else it may escape the traditional tests and fail in the field. Detection of such cells requires low voltages and elevated temperatures, which essentially adds to test cost. Also, testing at low voltage results in lower speed of testing. The proposed methodology aims to detect the weak cells at nominal operating voltage and room temperature itself by correlating the SNM. This facilitates in high speed testing at minimal cost of test in terms of voltages and temperatures.

1.6   Related Work

An efficient and economical memory test should provide the best defect coverage in the shortest time. Memory array organization becomes more and more complex as the demand of high density SRAM memories is increasing day by day. As, the device density becomes higher and the operating voltage is decreasing over the decades, it results in yield loss and

parametric failures. The increasing transistor/pin ratio which is projected to exceed 2.3 million/pin by 2016 [8] is limiting the controllability from the primary inputs and the observability of the faulty behaviour at the primary outputs in embedded memories [9]. Moreover, striving to keep up with the increasing clock speeds of SoCs increases the cost of Automatic Test Equipment (ATE) so that the at-speed test of high-performance chips becomes problematic. The fastest available ATE is always slower than the chips it will test. As multi-million-dollar ATEs become commonplace, the cost of the tester time spent on every chip directly impacts the total cost of the chip. A customer regards a product to be of high quality if the product is meeting their requirements at the lowest possible cost. Attention was given to the fault modelling, structural testing and DFT techniques to ensure and maintain test cost effectiveness and low defect levels. Some of these techniques are presented here.

Traditional Design For Test (DFT) methods include March Tests and Data Retention Tests. These are the functional test techniques for testing SRAMs. These tests need significant test times and elevated temperature which adds to testing cost. Moreover, they have very limited fault coverage [10, 11].

Literature presents some DFT techniques for stability fault detection [11-22]. The well-known techniques include Weak Write Test Mode (WWTM) [11], which applies a weak overwrite stress to detect defective cells. Other method in [12] suggests lowering the array supply voltage in isolation to the periphery. Due to poor tracking of process changes, these techniques may require multiple design iterations for adjusting the test stress to achieve acceptable test quality. Also, having separate pads for several memory instances as required in [12] is not advisable. Two programmable cell stability tests and debug techniques that use partially discharged floating bit lines to apply weak overwrite stress on the memory cell are described in [13]. The test involves activation of multiple word lines (WLs) at a time and the contents of the selected cells in a column generate the required test stress on the bit lines. The techniques are effective in detecting the unstable cells but involve significant circuit complexity in terms of modification in the row decoder architecture. Also, these require a considerable test time in order to initialize and generate the test stress. In addition, some modifications of the internal timing structure are required to allow the selection of multiple core-cells of a column at a time. None of the above mentioned tests correlate the impact of test stress with the tested FOM. In this work, we propose a correlation based methodology to detect weak cells w.r.t Static Noise Margin (SNM) in SRAMs.

1.7   Thesis Organisation

The thesis is organized as follows. Chapter 2 introduces the weak bits and the factors causing them. Subsequent sections define the weak bits and propose the correlation methodology to detect the weak bits in SRAMs. Later the flow of work is presented.

Chapter 3 presents a weak bit detection technique by boosting the wordline voltage of the cell. It describes the impact of boosting the wordline voltage on SNM of the SRAM cell. Subsequently, the correlation methodology is presented for the described test technique. Test setup and implementation of the WL boost technique is also discussed in the later sections. Finally a case study is presented for the proposed technique on a 28nm FDSOI SRAM.

Chapter 4 presents another technique for detecting the weak bits in SRAMs. It introduces the concept of array supply lowering and its possible impact. Then the SNM correlation of the test with the worst case conditions is verified and discussed. Finally it presents the possible implementations for generating test stress and discusses the results.

Chapter 5 explores a technique of raising the ground potential and its ineffectiveness for the detection of weak bits is discussed. Chapter introduces the ground raise concept. It presents the hypothesis about the possibility of weak bit detection by ground raise technique. Finally the chapter reveals the correlation results of the technique and concludes the experiment.

Chapter 6 concludes this thesis work and presents the possible future work which can be carried forward to this work.

Chapter 2

Proposed Weak Bit Detection Flow

This chapter discusses about the weak bits and the factors causing them. It describes about the direction of flow for the detection of weak bits. Section 2.1 introduces the definition of weak bits in SRAMs. Section 2.2 presents the correlation methodology proposed for the weak bits identification. Finally, the flow of exploration and verification of test methods is presented in Section 2.3.

2.1   What are Weak Bits?

In the present day advanced technology nodes, due to process limitations and scaled device dimensions, SRAMs experience random variations. These variations degrade the characteristics of the SRAM cells and impose weakness in the cell. There are several FOMs which characterize a 6T SRAM cell. Process variations may affect any of the FOMs associated with the cells. The definition weak cell doesn't replicate any Fault in the cell. A weak cell does not fail at nominal operating conditions, but it might flip at some other PVT. Any disruption in the normal memory operation such as supply voltage fluctuation, coupling noise, read/write cell disturbs, excessive temperature variations etc. might force a weak cell to flip its state. Owing to the specified reasons, the weak cells may fail at any time but generally pass the traditional SRAM functional tests.

A weak cell may possess weak SNM, weak write time, weak write margin or bad retention, but we address cell stability here as it is most crucial and yield limiter in nanoscale technologies including FDSOI. In context with SNM, the *weak cells* are defined as the cells with degraded or insufficient SNM which might force the cell to flip its state during read operation under certain conditions. The cell weakness is typically a result of resistive defects, excessive process shifts, transistor mismatch, IR drops, Coupling etc. Since the weak bits can escape through the functionality tests. Therefore, it is essential to explore the techniques which allow the detection of such kind of weak cells present in SRAMs, in order to minimize the test escapees and ensure reliability.

In the subsequent section, we have proposed a correlation based methodology which enables the detection of weak bits.

2.2   Proposed Correlation Methodology

For the identification of weak cells, we apply a test stress to the SRAM cells under investigation. The application of test stress to the cells affects the characteristics of the cell such as stability, write time, write margin etc. If a cell is weak, it will fail in its operation under the applied test stress. The correlation methodology analyses the effectiveness of the test for the weak bit detection. It is necessary to find the amount of stress that is required to push only weak cells towards the failure region which essentially means that the stress should be capable of degrading the stability of cell equivalent to the effect caused at abnormal operating conditions. In order to estimate sufficient stress, initially we perform SNM sensitivity analysis to find out the SNM sensitive devices. Thereafter, inducing various stress levels at nominal conditions and correlates the SNMs with worst case conditions, which are considered to be at lowered V_{dd} and extreme temperatures for different set of device V_t variations in SRAM cell. We decide the stress level by observing the plots which have high correlation coefficient (R^2) and the low intercept of the linear curve fitted line obtained from scatter plot. Trend lines having high R^2 values and intercepts approaching to zero indicates the corresponding voltage stress levels which are enough to detect the weak cells. Hence stress levels corresponding to trend lines with either less R^2 value or non zero intercept must be ignored. Varying the stress level at nominal conditions and correlating with worst PVT conditions must be repeated till this process yields high R^2 and intercept tending to zero for finding test voltage. Suitable test setup must be implemented such that the value of correlation coefficient (R^2) must not get affected with the chosen setup circuit since the devices used in the setup circuit plays a significant role in affecting the overall correlation. Hence it is essential to confirm the validity of R^2 with setup circuit also. The entire flow of the algorithm is shown in Figure 2.1. Observing the correlations on CAD before testing on silicon enables to effectively design the test setup and enables to find the desired condition for precisely detecting weak bits.

```
┌─────────────────────────────┐
│ Identify the test stress to detect │
│ weak SNM cells              │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│ Do Sensitivity analysis for SNM by │
│ applying 6σ Vₜ variations on │
│ devices Independently       │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│ Estimate SNM with elevated stress │
│ @ Nominal operating Conditions │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│ Correlate SNM @ stressed    │
│ conditions with worst PVT   │
│ condition                   │
└─────────────────────────────┘
```

Identify the test stress to detect weak SNM cells

Do Sensitivity analysis for SNM by applying 6σ V_t variations on devices Independently

Estimate SNM with elevated stress @ Nominal operating Conditions

Correlate SNM @ stressed conditions with worst PVT condition

Modify test conditions @ nominal conditions

High Correlation (R^2)

No

Yes

Intercept tending to zero

No

Yes

Design and Implement test circuit

Confirm validity by checking R^2 with set up

No

Yes

Observe cell failures to capture weak bits

Figure 2.1   Flowchart of proposed correlation methodology

2.3   Direction of Work

Figure 2.2 shows the flow of techniques which can be used to detect the weak bits in SRAMs. The depicted flow is followed in this work.

Figure 2.2   Flow of Weak Bit detection in SRAMs

Chapter 3

Weak Bit Detection by Boosting WL

This chapter presents the weak bit detection technique by boosting the wordline voltage of a cell. Section 3.1 introduces the test concept. Section 3.2 discusses the impact of boosting the wordline voltage on SNM of the SRAM cell. Section 3.3 presents the SNM correlation for the WL boost technique. Section 3.4 describes the implementation of generating the required boosted WL voltage and the test setup. Finally, Section 3.5 presents a case study for the described technique on a 28nm FDSOI SRAM.

3.1   Introduction

This test is based on the concept of applying stress on the core cell by slightly raising the Word Line (WL) voltage during read operation while retaining bit lines and other voltages as normal. By doing this, the SRAM cell experiences a read stress and if it possesses a lower stability then the cell gets flipped during read. This identifies a particular cell is weak.

3.2   Impact of WL Boost on Core Cell and SNM

Figure 3.1 depicts the standard 6T SRAM cell. During read operation, WL is asserted (at VDD) and the false side bit line (BLF) discharges through pass gate (PGF) and pull down (PDF), creating a small voltage bump at the internal node which depends on the resistive ratio of PGF and PDF. Raising the WL voltage disturbs this normal ratio of a designed cell, making PG stronger. This might lead to an increase in bump and might cause a weak cell to flip. [21] explains that a cell possessing a low SNM might flip its content when an elevated WL voltage is applied to it. In other words, raising the WL above normal tends to disturb the cell stability and lowers the SNM of the cell. Hence, we utilize this to create the test stress for the weak bit screening. Figure 3.2 illustrates the SNM trends when the WL voltage is raised, for an SRAM FDSOI cell. It is clear that the cell stability decreases with the increase in the WL voltage due to increase in the pass gate strength.
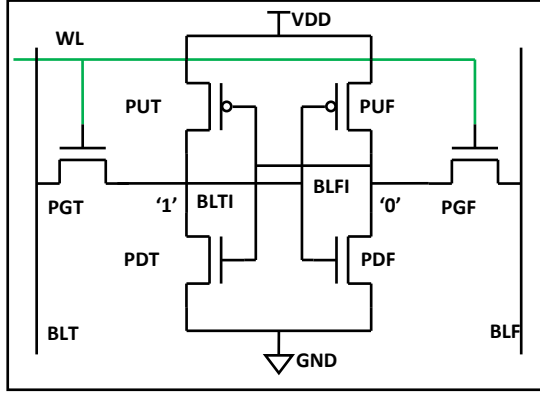
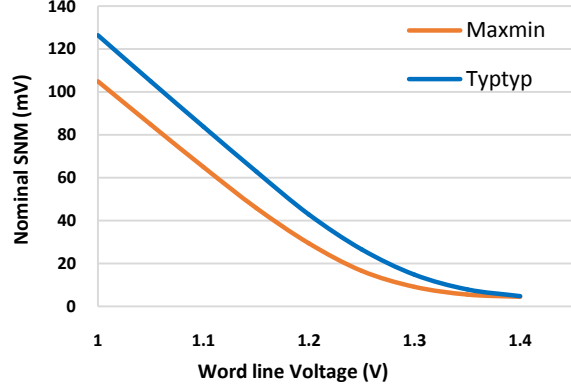**Figure 3.1 Schematic of standard 6T SRAM cell**

Figure 3.2 SNM variation with WL

3.2.1 Read Stress

In order to detect the memory bits which have a tendency to flip at in-field worst case conditions for cell stability, i.e. low voltage and extreme temperatures, we induce a stress during read cycle by boosting the word line (WL) voltage of the selected row of memory cells in test mode. The array and periphery excluding WL is supplied with nominal supply voltage in the test mode. Cells of selected row experience a read stress and if a cell is weak with respect to SNM, it will flip. Figure 3.3 shows such a weak cell flipping under stress of boosted WL. To ensure that the amount of induced read stress imposes the similar impact on the cell's stability as the worst operating conditions do, we propose correlation methodology.
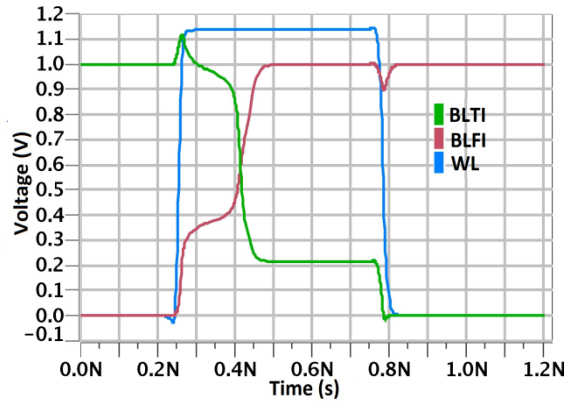
Figure 3.3 Read failure of a weak cell subjected to WL Boost

3.3 SNM correlation for WL Boost Stress

The correlation methodology analyses the effectiveness of the test for the weak bit detection. We correlate the impact of the test for the different set of variations in the SRAM cell. The affected cells should be stressed in such a way that it causes consistent effect across variations in the cell. Also, we need to ensure that stress effect is equivalent to that of the worst

27

operating conditions. Observing the correlations on CAD before testing on Silicon enables designers to effectively design the tests.

It is necessary to find the amount of read stress that is required to push the weak cells towards instability, which essentially means that the test stress should be capable of degrading the stability of the cells equivalent to the effect caused by abnormal operating conditions. At the same time, test stress should not be excessive which may force the strong cells to flip. In order to estimate the required voltage stress, we correlate SNM of the core cell for various boosted WL voltages, at normal operating conditions (1V, 25°C) with the worst case conditions such as, supply voltage of 0.7/0.6V and temperature ranging from 120°C-150°C, for different process corners. To obtain the correlation between the SNM of the cell for the two scenarios mentioned, we have introduced threshold voltage (V_t) variations in all the devices of memory cell using the method of Design of Experiments (DoE) [23] with a load of 64 rows and simulated in ELDO for 28nm FDSOI technology. The benefit of using DOE for variation is to allow covering a large sigma space even with lesser number of samples. Figure 3.4 depicts the maximum SNM correlation plots obtained for different corners at corresponding boosted WL voltage, T=25°C with respect to the SNM at worst case conditions.

The correlation methodology validates the effectiveness of the test for the detection of weak bits. It is evident from the plots that the bits which are actually weak, indicated by very low SNM values (even negative) at worst case possess nearly equal SNM for boosted WL subject to application of sufficient stress. This ensures that the bits having tendency to fail infield due to undesirable variation in process, voltage, temperature shall also fail under the applied stress and hence can be detected. Figure 3.5 shows the correlation trends across various process corners with respect to the extent of WL boost. For a range of WL voltage, we can observe sufficiently good correlation. In addition to correlation coefficient value, intercept of the trendline is also significant. Trendline intercept should approach to zero as it indicates the corresponding voltage stress is enough to detect the weak cells. Small negative intercept is acceptable but positive intercept is not appreciated, to ensure complete weak bit detection. To ensure effective weak bit detection, the low SNM bits at worst case should map to low SNM bits under stress. SNM under stress should be equal or slightly less than SNM at worst case. Hence, the maximum correlation stress is determined for the test by considering the above criteria.
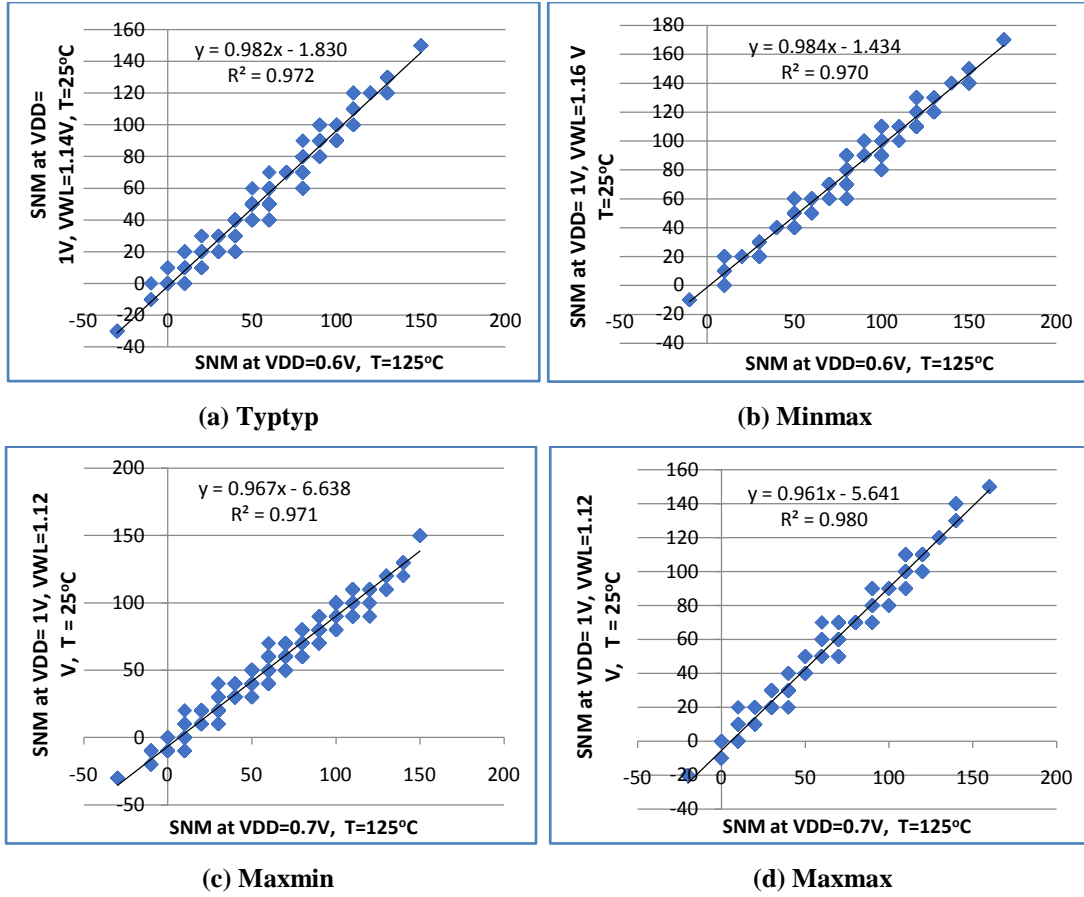
(a) Typtyp

(b) Minmax

(c) Maxmin

(d) Maxmax

Figure 3.4   Correlation plots of SNM for WL boost at nominal and worst case operating conditions
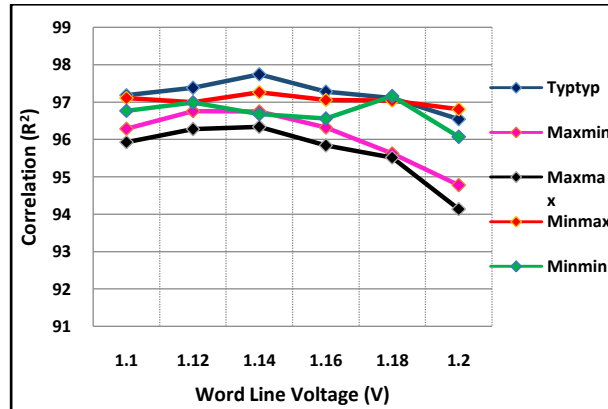

Figure 3.5   SNM Correlation for WL Voltages across corners

3.4   Test Setup and Implementation

It is evident from previous section that to perform the test, appropriate boosted WL voltage must be applied to SRAM array for effective weak bits detection. Several WL boosting techniques based on charge pumps and capacitive coupling exist [24, 25], which are traditionally used as write assist schemes [26]. In order to generate the required boosted WL voltage during the test mode, we propose a test setup, shown in Figure 3.6. Boosted WL voltage is achieved by using the principle of capacitive coupling.
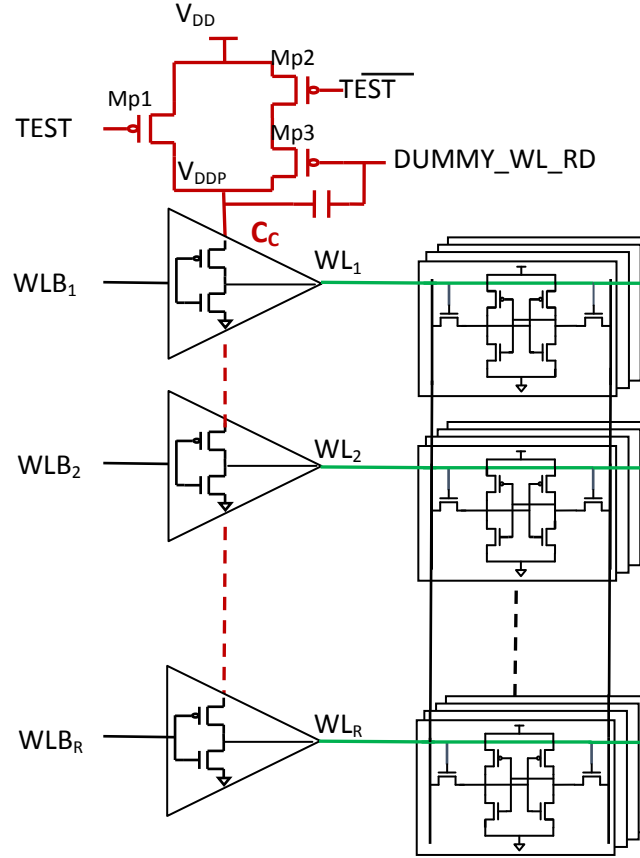
Figure 3.6 Illustration of proposed setup for word line boost

According to the normal SRAM read/write operation, for a selected row, WL driver asserts the word line, when the corresponding WLB signal is activated by the row decoder. During the test mode, we modulate the supply of this WL driver with the help of the booster circuit depicted in the schematic (Figure 3.6). In the normal mode of operation, test signal is low, supplying V_{DD} to WL drivers normally. However, during the test mode, other parallel path (Mp2-Mp3) directs the supply. For the self-timed SRAM architectures, during read operation, dummy word line read signal (Dummy_WL_RD) tracks the WL. Hence we utilize this signal for generating boosted voltage through capacitive coupling between C_C and the intrinsic capacitance at the supply node (V_{DDP}) of WL drivers. Initially the supply node is at V_{DD}. When Dummy_WL_RD makes a transition from low to high, MP3 is turned off, and voltage at V_{DDP} rises due to coupling. The amount of rise depends on the ratio of C_C and the intrinsic capacitance. Consequently, the raised potential at the supply of WL driver drives a boosted WL signal during read, in test mode, providing the read stress to the cells of selected row. This operation is illustrated in Figure 3.7 which depicts the transient response of the proposed setup when simulated for core array of 64 columns with a load of 64 rows using silicon extracted spice models. It can be inferred from Figure 3.7 that whenever both the

TEST mode is enabled and the read pulse is active, the word line (WL) voltage is boosted to higher voltage because of transition of Dummy_WL_RD from low to high. Moreover, the voltage rise may also be slightly modulated by controlling the rise/fall time of the read pulse, as shown in Figure 3.8.
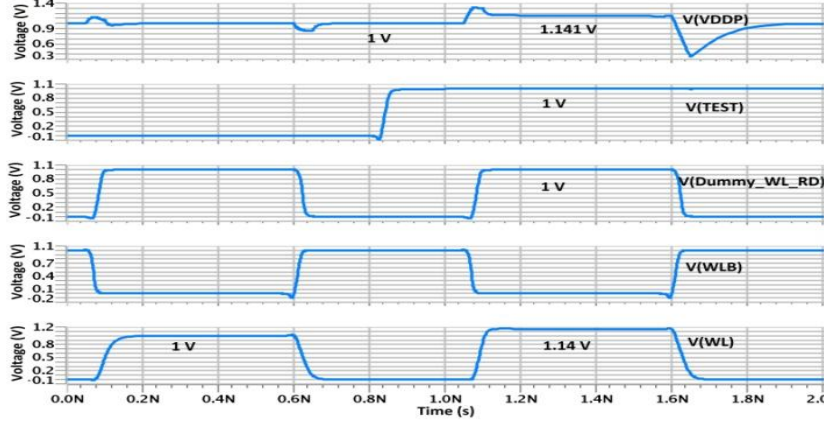

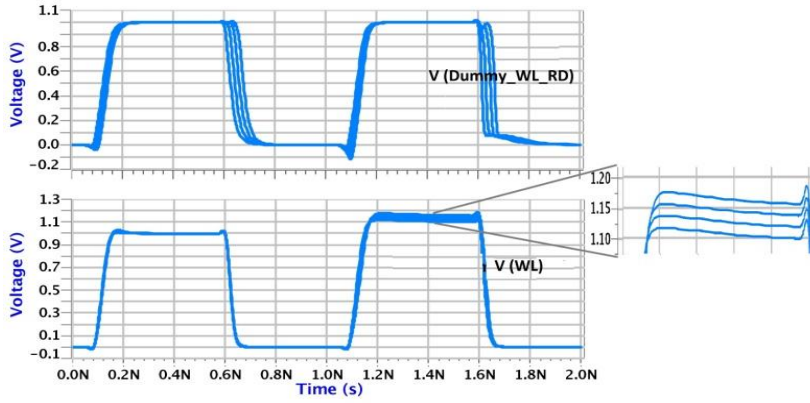**Figure 3.7   Transient response of setup with WL boosted in Test mode**

Figure 3.8   Illustration of WL boost with respect to rise/fall time of the Dummy_WL_RD pulse

## 3.5   Case Study on 28nm FDSOI SRAM: Results and Findings

The proposed weak bit detection methodology with the test setup is implemented and tested on an SRAM in 28nm FDSOI. We present a case study for a characterization of 64x64 memory array to demonstrate the effectiveness of the proposed technique. All the simulations are carried out using silicon extracted spice models.

Prior to the application of read stress, we observe the SNM correlation for varied amount of WL boost stress. As a result, we can determine the appropriate amount of stress which correlates to the effect of worst case operating conditions for stability. The correlation trends are analyzed across different process corners and the corresponding correlation coefficient values are shown in Table 3.1.

Table 3.1   SNM correlation across various corners for WL voltages

WL (V)	Typtyp	Maxmin	Maxmax	Minmax	Minmin
1.1	97.19	96.29	95.93	97.11	96.77
1.12	97.38	96.76	96.28	97	96.99
1.14	97.74	96.75	96.34	97.26	96.68
1.16	97.28	96.32	95.84	97.06	96.98
1.18	97.11	95.63	95.52	97.01	96.77
1.2	96.54	94.78	94.14	96.81	96.07

It can be observed that, WL voltage ranging from 1.12V to 1.16V results in good correlation values consistently for all corners, which is also clearly depicted in Figure 3.5. With this correlation analysis, we deduce the most appropriate WL voltage for performing the test across the process by considering both the correlation coefficient as well as the trend line intercept. The maximum correlation and sufficient stress WL voltages deduced for weak bits detection throughout different process corners is depicted in Figure 3.9. We observe that there is a slight variation in the most suited stress value across the corners. As an illustration, for Minmax, slightly higher stress is required since this corner severely degrades the cell stability.
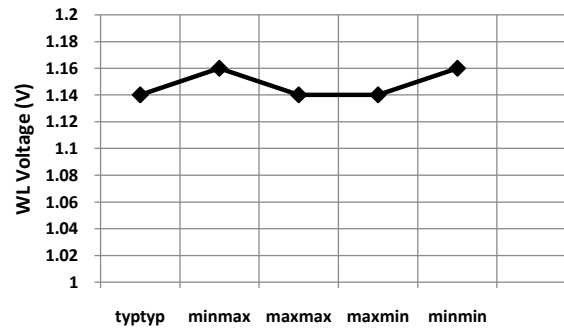

Figure 3.9   WL stress voltage for performing weak bit test across corners

Subsequently, the test is performed on the SRAM with the setup described in earlier section. We introduced V_t variations in the devices of a memory cell using DOE, covering a large sigma range from both sides of the mean. Initially, to observe the pass/fail trend of the SRAM cells under stress we introduced V_t variations in the devices which majorly govern SNM. It is intuitive and also verified that the devices PDT, PDF and PGF of 6T cell (Figure 3.1) severely affect its SNM. Figure 3.10 shows the impact of the applied read stress with respect to the V_t variations in the specified devices. Red color indicates the detected weak bits which flipped during the test whereas the green color region shows the normal bits which passed the test. Figure 3.10(b) represents the boundary demarcating the weak bits and normal bits for the estimated WL stress voltage. Figure 3.10(c), (d) shows the trend of failing bits for the Maxmin and Minmax process corner respectively. We observed that the number of bits

failing in the Maxmin corner is greater compared to others, which is inline with our expectation, as it is worst process corner with respect to SNM. It can also be verified from Figure 3.10 that more number of cells fail when the false side pass gate is made strong and pull down weak. Also, with the increase in strength of true side pull down, the cells flip easily, which is clearly depicted in the figure.

Thereafter, V_t is varied for all the six devices of the SRAM cell and the threshold SNM is obtained for the different process corners. Figure 3.11 illustrates the transient response of internal nodes of SRAM cell under the WL boost stress with the V_t variations in all the devices. Weak cells are flipping and normal cells are not flipping. Figure 3.12, 3.13 and 3.14 depict the histogram of weak bits (Red) and normal bits (Green) at their estimated best suited WL stress voltages for TYPTYP, MAXMIN and MINMAX corners respectively. It is clear that the cells having very low SNM are detected as the weak bits by the application of the test. The threshold SNM value can also be observed from the figures. Figure 3.15 shows this value for different process corners. For the specified memory specifications and WL voltages, the test is able to detect weak cells having SNM upto 50-60mV.
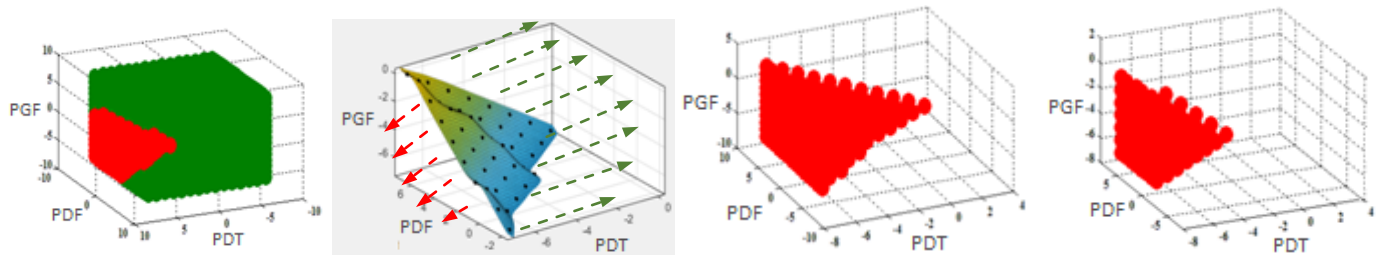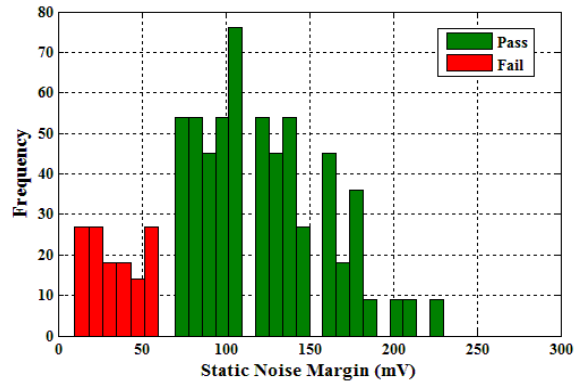

Figure 3.10   Depicting Weak/Normal cells (a) Pass-Fail region for Typtyp corner (b) Boundary separating weak-normal cells (c) Fail region for MaxMin corner (d) Fail region for Minmax corner
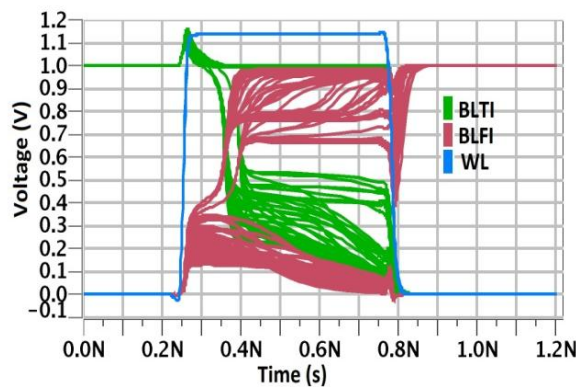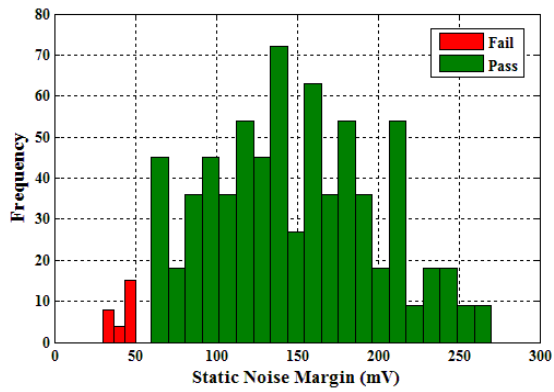

Figure 3.11   Read success and failure of cells for V_t variations (Typtyp)
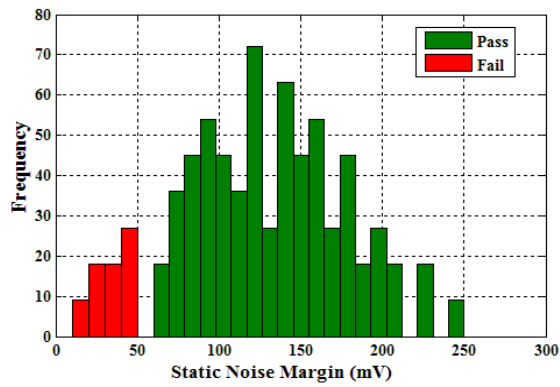
Figure 3.12   Histogram depicting weak cells (Red) which failed the test and normal cells (Green) which passed the test (Typtyp corner)
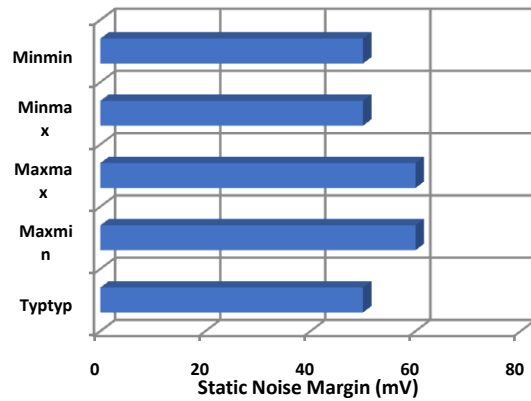

Figure 3.13   Histogram depicting weak cells (Red) which failed the test and normal cells (Green) which passed the test for (Maxmin corner)

Figure 3.14   Histogram depicting weak cells (Red) which failed the test and normal cells (Green) which passed the test for Minmax corner

Figure 3.15   Detectable weak Static Noise Margin across the corners

Chapter 4

Lowering Memory Core Supply Voltage for Weak Bit Detection

This chapter presents another technique for detecting the weak bits in SRAMs. Section 4.1 introduces the concept of array supply lowering and its possible impact. Section 4.2 discusses about the SNM of SRAM cell and how the test produces stress on SNM. Section 4.3 verifies the SNM correlation of the test with the worst case. Section 4.4 presents the possible implementations for generating test stress and discusses the results.

4.1   Introduction

This test is based on the concept of applying stress on the SRAM cell by slightly lowering the supply voltage of the memory array, but keeping the voltage of periphery unchanged. This means all the other voltage levels including those of bitlines, wordlines, drivers and other peripheral circuitry are not altered. The SRAM cells are applied read pulses under the mentioned condition. The reduced supply of the array imposes stress on the SRAM cells. And this effectively reduces the SNM of the cells. If a cell is weak, it will flip its contents when a read operation is performed with all other levels unaltered.

4.2   SNM for Supply Voltage Variation

Voltage Transfer Characteristic curve (VTC) of a 6T SRAM cell simulated for a specific threshold voltage (Vt) variation is depicted in Figure 4.1. In ideal scenario, the VTC of both halves of the Static Noise Curves (SNM) curve will be perfectly matched. However in reality, the process spreads, resistive defects, coupling effects etc would deform the symmetry of VTC plot. The term SNM can be defined as the side of the smaller of the two squares that can be fit in the eyes of the VTC curves, as shown in Figure 4.1. In general, the Noise Margin (NM) is the maximum spurious signal that can be accepted by the device when used in a system while still maintaining the correct operation [27-29]. If the consequences of the noise applied to a circuit node are not latched, such noise will not affect the correct operation of the system and can thus be deemed tolerable.

Static Noise Margin (SNM) is the most prominent stability metric. With this metric, it can be easily estimated that how much the SRAM cell is tolerable towards noise. In other words it can be estimated that how much voltage room for static noise, i.e. DC voltage, is left until the cell will flip. There are several ways in which the SNM of a SRAM cell can be measured.

With the reduction in the supply voltage, the SNM of SRAM cell decreases. Reducing the array supply while maintaining the periphery level introduces a stress in the normal SRAM cell. This degrades the SNM of the cell. In this work, this is utilized as a test stress to identify the weak bits in SRAM.
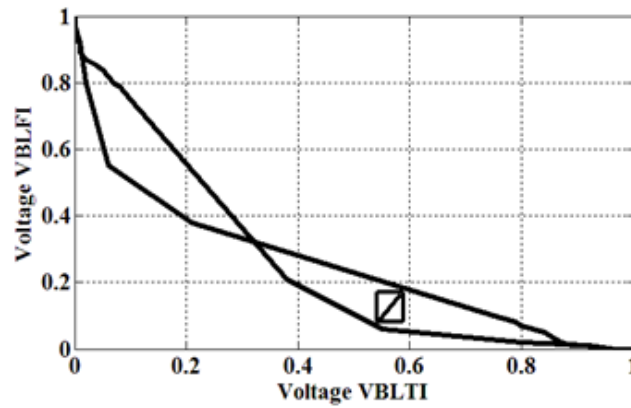

Figure 4.1   Voltage transfer characteristics (VTC) Curve

4.2.1   Array Supply Lowering Test Stress

In order to detect the bits having a tendency to flip at worst case conditions for cell stability, i.e. low voltage and extreme temperatures, we induce the read stress. While testing the weak bits in memory array during the cell read cycle, the array is supplied with slightly lowered voltage while the periphery including the bit lines and the word line is maintained at normal operating voltage. With this methodology, the cell under test experiences a read stress and if the cell is weak with respect to SNM, it will flip. To ensure that the induced read stress imposes the similar impact on the cell's stability as the worst operating conditions do, we have used the method of correlation.

We have investigated the the SNM dependency with respect to the variations of array supply voltage (VDD) (but not word line (WL)) for different threshold voltage (V_t) variations. In order to investigate the SNM dependency, a memory cell which is designed for faithful operation at 1V supply room temperature is considered with a load of 2048 rows with an appropriate read pulse. The dependency is investigated by correlating the SNM of the memory cell at VDD=0.9V, word line (WL) and bitlines voltage of 1V at nominal temperature of 25^oC with the SNM of the memory cell at operating voltage of 0.7V at an extreme temperature 125^oC where it is the worst case for SNM. It can be observed from Figure 4.2 that the SNM of the memory cell is highly sensitive to the cell or array supply voltage (V_{DD}) lowering. Hence, the method of reducing the array supply voltage of the memory cell can be applied for screening weak bit during read operation as SNM is highly sensitive to the variation of array

supply voltage. It can be understood that in order to perform the test at nominal environment, an appropriate array test supply voltage must be selected which can be done by observing the supply voltage at which maximum correlation is achieved when the SNM at normal condition (with some stress) and the worst case conditions are compared.
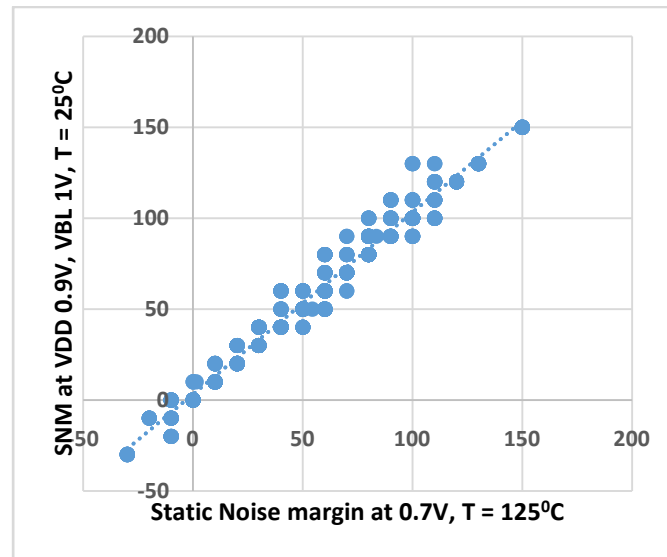
Figure 4.2   Scatter Plot of SNM with reduced operating voltage at nominal environment to the worst case environment for Maxmin Corner

4.3   SNM Correlation

It is required to find the extent of read stress sufficient to push the cell towards instability which is equivalent to the effect caused at abnormal operating conditions. The required voltage stress can be found by correlating the SNM at reduced array supply voltage and nominal temperature with the worst case conditions that may appear, such as supply voltage of 0.7/0.6V and temperature ranging from $120^{o}C$-$150^{o}C$ at all corners. For this, Figure 4.2 depicts the correlation of SNM at reduced array supply of 0.9V but periphery supply voltage of 1V at T=$25^{o}C$ with the complete cell operating at worst a supply voltage of 0.7V at T= $125^{o}C$.

To obtain the correlation between the SNM of the cell for the two cases mentioned above, a memory cell with its equivalent load of 2048 rows are considered. Threshold voltage (Vt) variations are introduced in all the devices using the method of Design of Experiments (DoE) and simulated in ELDO simulator. In order to achieve this test voltage for different corners, simulations are performed at different reduced array voltages for various process corners. Figure 4.3 and 4.4 show the flavour of analysis at different corners, with different amount of test stress. It can observed from the plots that the bits which are having tendency to fail, i.e. having lower stability at the worst conditions will also fail during testing at nominal

conditions for the applied voltage stress. The optimum reduced voltage values observed for all the different corners are observed to be in range of 0.84-0.9V.
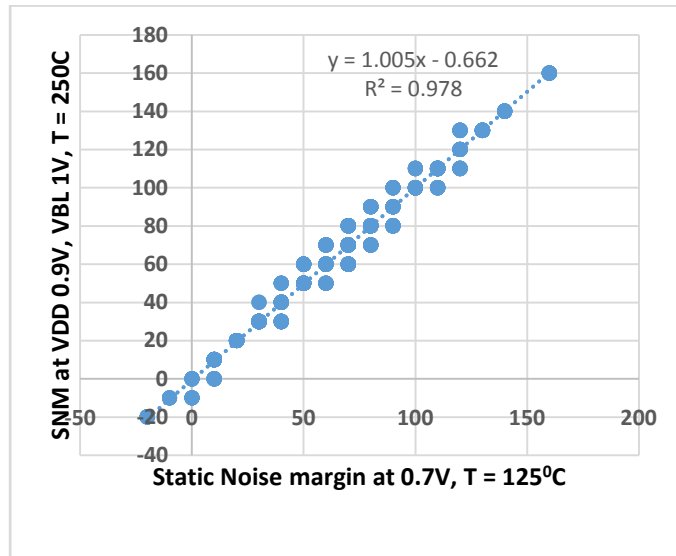

Figure 4.3   Static Noise Margin correlation plot at Typtyp corner for 0.1V lowering
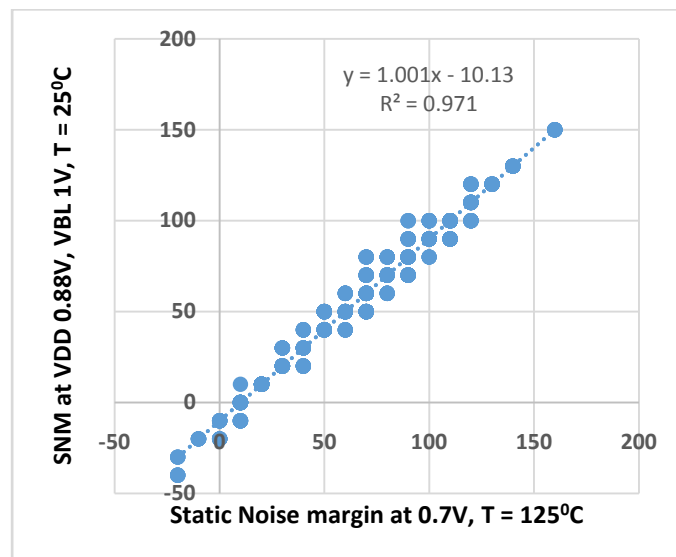

Figure 4.4   Static Noise Margin correlation plot at Typtyp corner for 0.12V lowering

4.4   Test Setup and Implementation

It can be deduced from the previous section that for performing the test, an appropriate reduced supply voltage must be applied to the array for the detection of the weak bits. For achieving the circuit different potential divider circuits can be considered. In this work, the following two implementations have been considered.
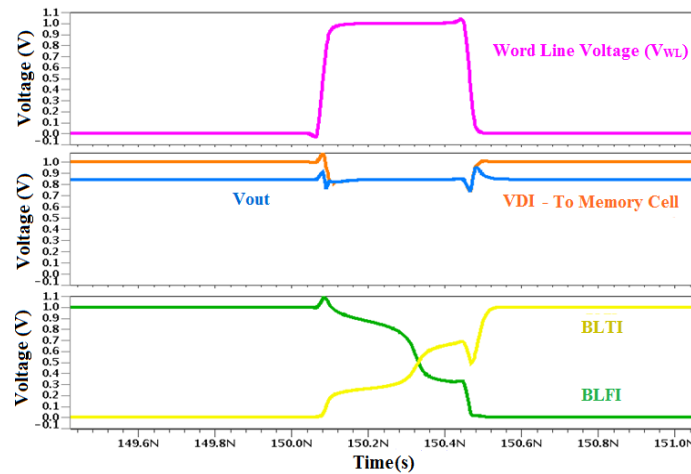
4.4.1 Implementation 1
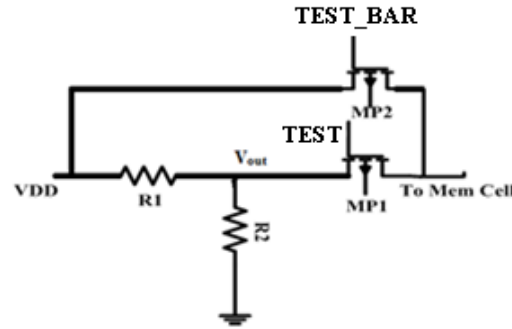
Figure 4.5 Resistor divider implementation for generating lower VDD

A potential divider circuit shown in Figure 4.5 is implemented to generate the reduced supply voltage for the array. During normal operation of the memory, nominal supply voltage V_{DD} (1V in our setup) passes to the memory cell as well as periphery through MP2. On the other hand, while testing the memory for weak cells, the reduced voltage, V_{out} passes to the memory cells through MP1. But the periphery is supplied with the nominal voltage V_{DD} for all the times.

Figure 4.6 shows various signals and waveforms captured while simulating the above implementation. It depicts the flipping of a weak cell during the stressed read cycle, in TEST mode. It can be seen from the figure that during the TEST read operation, indicated by the activation of wordline in the figure, the memory cell receives a reduced supply. For the other times, during the normal operation it receives normal V_{DD}.


Figure 4.6 Simulation waveforms of a weak cell flip under Vdd lowering stress

4.4.2 Implementation 2

The potential divider can be realized using the implementation similar to as shown in Figure 4.7. Present day memories are provided with the embedded switch in SRAM architectures

which is designed usually for power gating. That can be utilized to generate a potential divider which can supply a lower V_{DD} to the array in the test mode.

When the test signal is not asserted, the nMOS is turned off and the memory gets the usual supply. During the test mode, nMOS turns ON and the potential divider is activated. Now the core array receives the lower supply voltage.
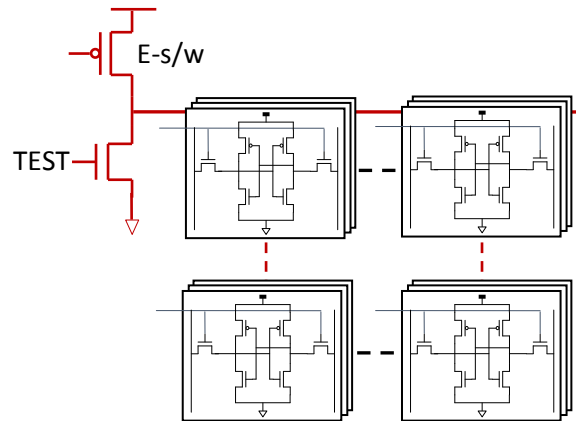
Figure 4.7 Setup for generating a reduced voltage at memory array

4.4.3   Results

The proposed weak bit detection scheme is implemented and tested on a memory cut of 64 words. It is characterized using STM critical path in 28nm FDSOI technology. The memory instance is then simulated with the incorporated test described setup of potential divider for V_{DD}=1V, T=25°C at different process corners. The memory is initialized with the data '1' or '0' and is subjected to random variations in order to drive the memory cell weak for certain cases of variations. The weak bit screen test is applied by asserting the TEST signal. We observe whether the memory cell is flipping its state or not for different set of variations.

Figure 4.8 shows the plot of the frequency of cells failing/passing under the applied stress and their corresponding SNM values under nominal operating conditions. The failing cells are the weak cells. We have observed that the cells having the SNM less that 99.27mV flipped their state because of the applied read stress. This indicates that these weak cells may fail and flip their state in presence of infield variation in PVT, due to their lesser SNM/stability. The ones in green do not flip their state, implying these are the stable cells which can sustain the infield variations.

Hence, we can infer that the proposed scheme of applying the read stress successfully facilitates the screening of weak bits by testing at the nominal conditions. Figure 4.9 depicts the boundary for which the cells are detected as weak cells for various process corners. For

the MaxMin corner, the cells which possess SNM less than 104.32mV are detected as weak. And 98.11mV is the minimum margin for the cells in MinMin corner to retain their state.
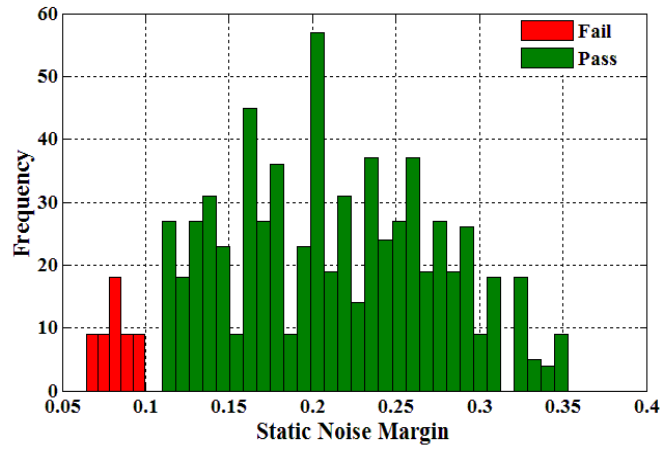

Figure 4.8   Histogram depicting pass/fail cells under the applied stress
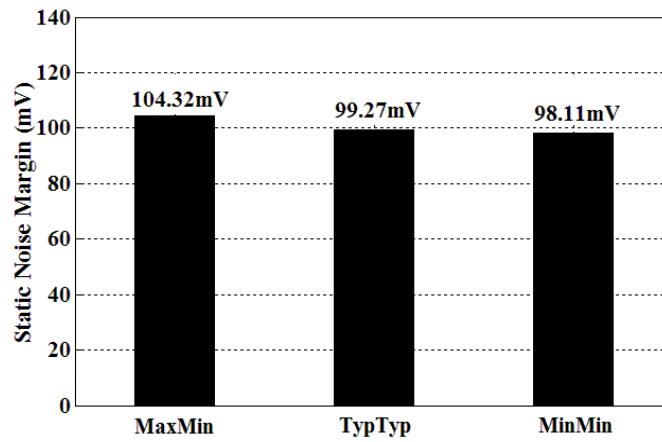

Figure 4.9   SNM boundary for weak cells at different corners

Chapter 5

Ground Raise Experiment

This chapter explores a technique of raising the ground potential and its ineffectiveness for the detection of weak bits is discussed. Section 5.1 introduces the ground raise concept. Section 5.2 presents the hypothesis about the possibility of weak bit detection by ground raise technique. Section 5.3 reveals the correlation results of the technique and concludes the chapter.

5.1   Introduction

This experiment is based on the concept of applying stress on the SRAM cell by slightly raising the ground supply voltage of the memory array. Considering the cell stability as the key Figure of Merit of the SRAM cells, the technique is explored which can stress the stability of the SRAM cells and might be used as a test technique to identify the weak cells.

As mentioned previously, SNM is considered as a measure of the cell stability. In order to test for the lower SNM cells, methods need to be explored which can stress the SNM of the cell, in other words, can affect the cell stability.

5.2   Hypothesis
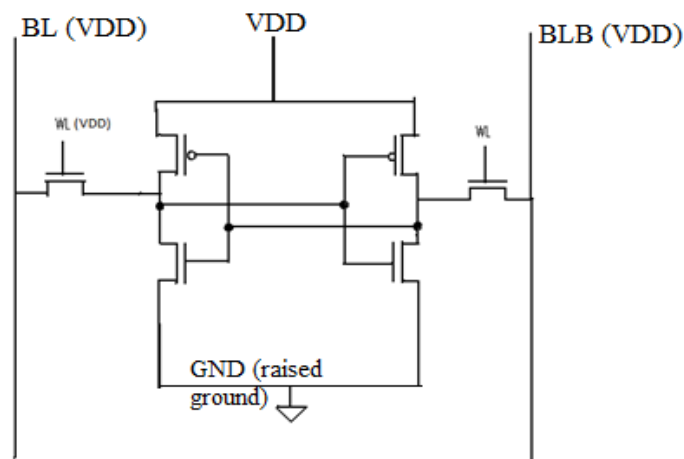
Figure 5.1   A 6T SRAM cell with raised ground voltage

Raising the ground voltage of the SRAM call may be considered as a stress for the SNM of the cell. If the ground potential is raised, the pull down transistor strength reduces. Consider the read operation of a SRAM cell. When the word line is asserted, the bitline near node storing logic '0', discharges through the pass gate and the pull down transistors. During the read operation, a small voltage bump is created at the node storing '0'.

Now raising the ground potential results in the decrease in strength of the pull down transistor, this in turn results in a larger voltage bump at the internal node. So, the SNM of the cell reduces under the given condition. Figure 5.1 depicts the SRAM cell with the raised ground node.

If there is a weak cell already possessing a low SNM, then raising the ground potential and reading the cell may cause it to flip its contents. In order to verify this hypothesis correlation of the SNM with ground raised is obtained with the SNM under worst case conditions.

5.3   Ground Raise Correlation

To verify the above hypothesis that raising the ground voltage can be used as a test stress for detecting the weak cells, correlation of SNM with ground raised is computed with the SNM at the worst case conditions. This is done to validate that the test stress would produce similar impact on the SRAM cells as the worst operating conditions do. SRAM cell with a load of 64 rows is considered and simulated in ELDO in FDSOI technology. Further, read pulse is applied on a memory cell with the ground raised and SNM is computed. This SNM is plotted against the SNM at the worst cell stability conditions.

5.3.1   Result and Conclusion

Figure 5.2 and 5.3 depicts the correlation plots obtained from the SNM simulations. It can be observed that the test is not able to produce enough stability stress as the worst operating conditions impose. Very high values of raised ground voltage are required in order to produce more stress on the SRAM cells. Doing so is not suggestible. Also, it degrades the correlation at higher voltage values.
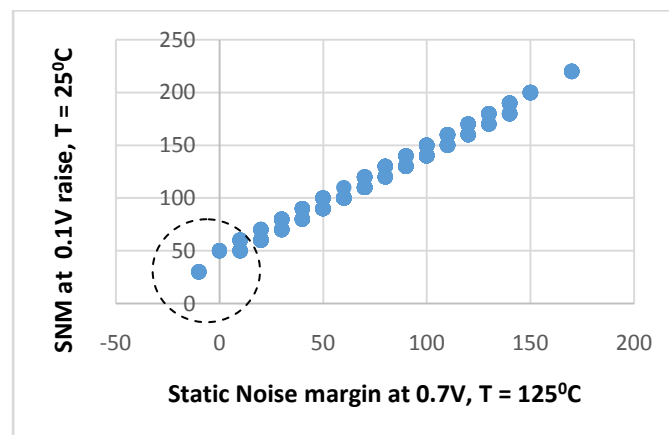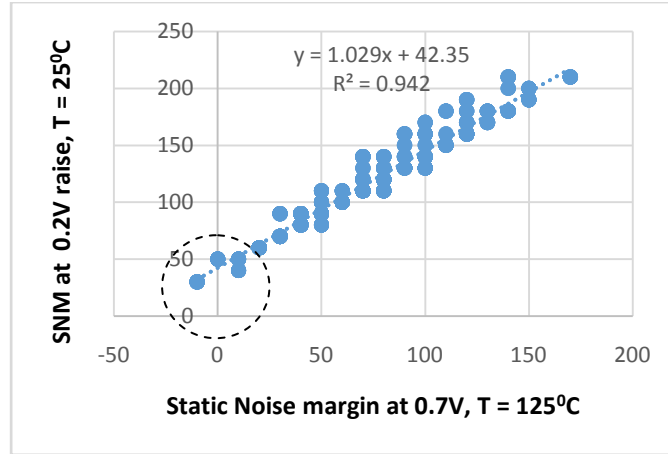

Figure 5.2   SNM Correlation plot with GND raise of 0.1V

Figure 5.3   SNM Correlation plot with GND raise of 0.2V

The observed deficiency of the test stress imposed in this experiment can be justified as the pull down transistor of the other side, i.e., the node storing logic '1' may require a higher Vgs to flip its contents. Since the ground raise affects the strength of other side pull down transistor also.

Hence, this experiment suggests that the discussed experiment of raising the ground voltage to detect the weak bits of SRAM is not advisable to perform as a test. As, the test when performed on silicon might not give desired results.

Chapter 6

Conclusion and Future Work

This chapter concludes this thesis work and presents the possible future work which can be carried forward to this work.

6.1 Conclusion

In this work, we proposed correlation based test methodologies to screen the weak bits, possessing a tendency to fail in field in presence of adverse PVT conditions. This ensures good yields and reliability during SRAM field operation. The proposed test methods are verified with an appropriate test setup of STM critical path for SRAM core array in 28nm FDSOI technology. It is evident that discussed techniques can be effectively used as the read stress for performing the Weak bit detection test.

The implementation of the techniques is also discussed in the work. Previous chapter discusses about a theoretical hypothesis which was later realized to be not efficient for the weak bit detection. The test stress can be computed by using correlation methodology. Sufficiently good correlation trends show that the test methods can be used to estimate the amount of stress required which permits the testing at nominal voltage and room temperature, hence saving test cost and time.

The pass/fail trends for the applied tests at different corners are inline with expectations across the process corners. The case study is also conducted to estimate the margin SNM which qualifies the test for a particular stress applied.

6.2 Future Work

In this work, the cell stability or SNM is considered as the criteria for detecting the presence of weakness in the cell. This is known that the device variations and process limitations affect other FOMs of the SRAM cell also.

The test techniques considering the other SRAM cell FOMs such as write time, write margin etc may also be explored. A SRAM cell may possess sufficient cell stability but weaker writability (write time or write margin). That can also be set as criteria for detection of weak bits according to application demands.

Figure 6.1 shows a flowchart depicting some other test techniques which can be explored. These are based on theoretical understanding and analysis. All such techniques may be explored and verified for their efficiency.
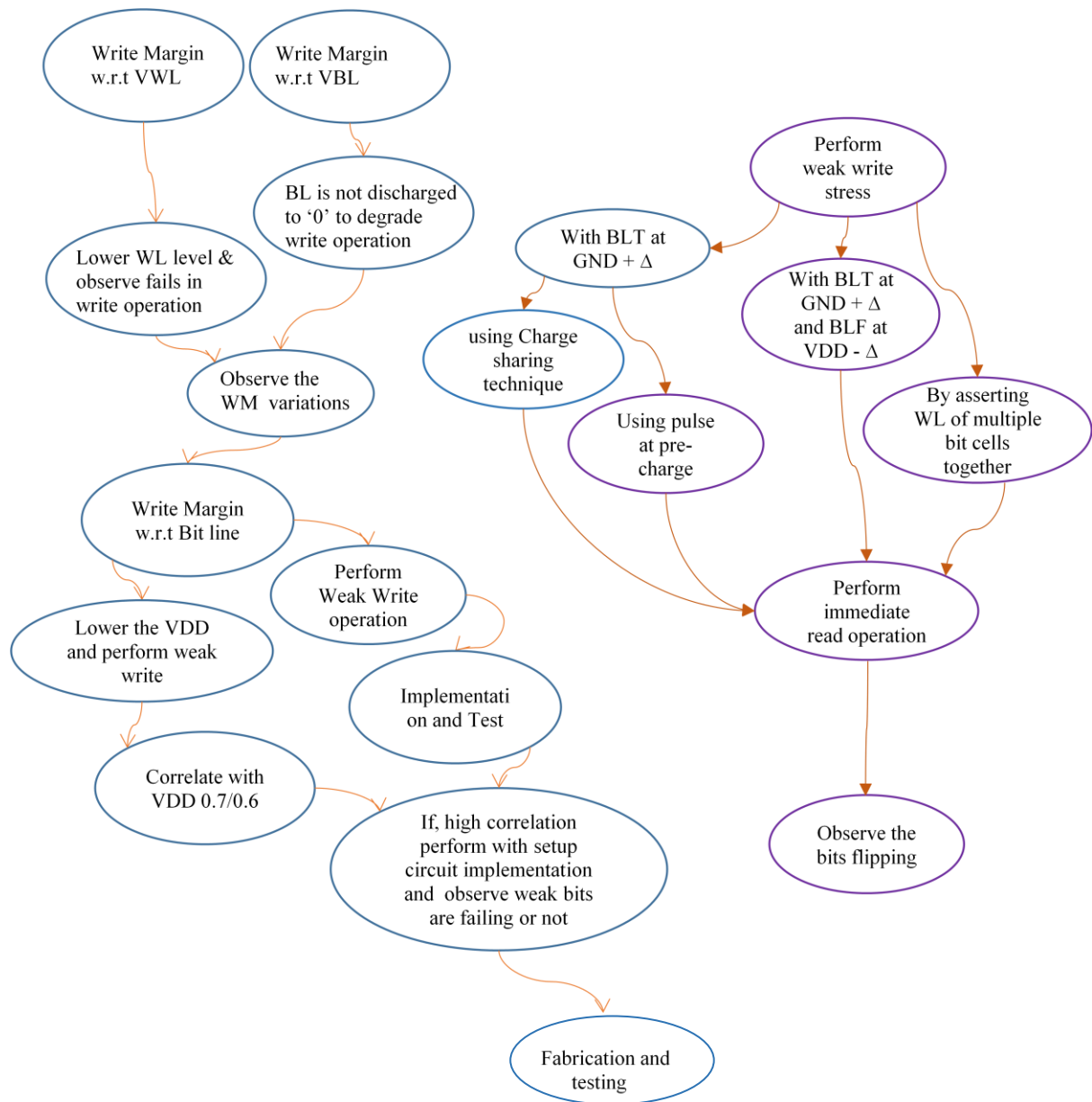
Figure 6.1   Flowchart of theoretical explorations on writability based test techniques

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