Wide bandgap HEMT Device (GaN) Characterization and Modeling for High Power Amplifier Design.

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with specialization in VLSI and Embedded Systems

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Certificate

This is to certify that the thesis titled **"Wide bandgap HEMT Device (GaN) Characterization and Modeling for High Power Amplifier Design."** submitted by **Shashwat** for the partial fulfillment of the requirements for the degree of *Master of Technology* in *VLSI & Embedded Systems* is a record of the bonafide work carried out by him under my guidance and supervision in the Security and Privacy group at Indraprastha Institute of Information Technology, Delhi. This work has not been submitted anywhere else for the reward of any other degree.

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Abstract

To serve large geographical area, there is need to drive antenna with high power. It necessitates the requirement of high power amplifier (PA) for delivering large RF output power. Alongside power added efficiency (PAE) and linearity should be optimized to meet the requirements of the high capacity and high quality services of next generation communication systems. RFPA capability is highly dependent on the transistor material quality. It is known that a high terminal voltage is required for achieving high output power from a transistor device. In this context, a device possessing large bandgap so that it can be operated at high terminal voltages is required. AlGaN/GaN HEMT technology is becoming an interesting candidate for the PA design as GaN is a wide band gap material. In addition, it can be operated at high operating frequency owing to its high saturation velocity. The efficient and cost effective RFPA design flow requires identification of optimal circuit configuration on computer added design (CAD) tools prior to fabrication. This necessitates accurate transistor model to simulate its real time behavior. In the case of GaN HEMTs, modeling attains significant importance considering the device complexity and not a well-developed fabrication process. It is envisaged that the systematic modeling strategy can facilitate its fabrication process to a significant extent. This thesis presents the study and implementation of small-signal modeling technique and device capability based on measured data.

The final outcome is presented in the form of an equivalent electric circuit that can be represented as a device in CAD.

Acknowledgments

I wish to express my special gratitude to my research advisor Prof. Dr. M S Hashmi, head of the Department of ECE, IIITD , for giving me the chance to work in different research projects in the past two years. I am very grateful for his continuous support and encouragement in the course of this work. I would like to thanks to our industry research partner for their cooperation by providing device's measured data. My thanks also goes to Pulkit Sharma, Nidhi Gupta, Shipra Batra, Pankhuri Singh, Ankush Singh, Deepayan Banerjee and Protim Bhattacharya for their help to improve representation of this dissertation.

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Chapter 1

Introduction

In today's world telecommunication plays a vital role in almost every technology and forms the backbone of knowledge dissemination in various forms. It has had a significant impact in the modernization of the quality of human life and has played a major role in strengthening the defense system of various nations. Military communication has been an important part in the advancement of the intelligence and security. Space missions have also incorporated several telecommunication principles for collecting huge amounts of data from the depths of universe. Figure 1.1 shows a block diagram comprising the main components of a communication system. The main function of antenna is to sense or transmit the radio signals which are processed by the receiver. The DSP unit processes information to and from the base transceiver stations (BTS) controller. The power amplifier (PA) is an integral part of the transmitter which aims at amplifying the power of the transmitted signal.

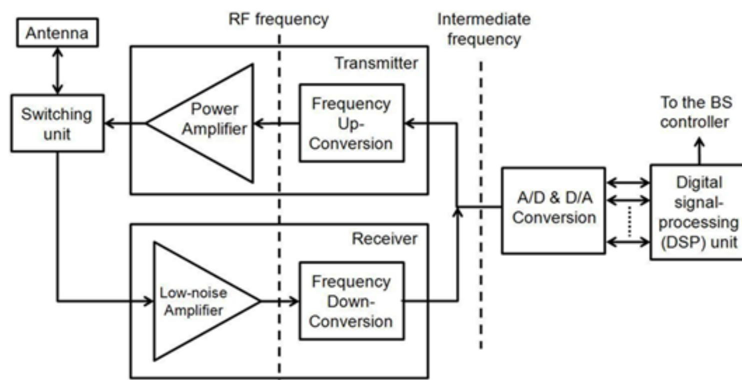

Figure 1.1: Basic component of a communication system

PAs at RF, microwave and millimeter-wave frequencies find diverse applications including cellular handsets, WLAN, wireless broadband satellite, military, and avionics. Predominantly, the rapid growth of wireless communication necessitated power amplifiers in 1 GHz and 2 GHz range for mobile handsets and BTS.

In order to provide sufficient quality of service for large user capacity, one will need highly linear PAs with high power efficiency [5, 6]. Linearity and efficiency have strong trade-offs to improve one without compromising the other. There are two options available for improvement of both linearity and efficiency. One is to improve PAs linearity by adding external circuits, simply by improving those designs without affecting efficiency or by improving the quality of the power transistor(s) active device, which is a key component of PA. However, the first technique involves several drawbacks like increased cost and size, reduced effective bandwidth and difficulty in adjustment of figures of merit (FoM). Consequently, there is a growing interest in direct optimization of the actual PA linearity in terms of the employed active device [7]. Hence, the availability of power transistors with high output power and other important FoMs (linearity, gain, efficiency, large input and output impedances), is a qualification for designing efficient and linear PAs.

The power transistors technologies which are currently in use for PA design, like Si-LDMOS, are attaining their limits [8]. The main limitation in them is their operating frequency range which is limited to about 4 GHz. As a result, intensive research in recent years has made it possible to develop new device process technologies using new wide band-gap materials. The excellent contender of these wide band gap materials is AlGaN/GaN High Electron Mobility Transistors (HEMTs). They have a record of achieving power densities up to 30 W/mm on SiC substrates [9], 9.4 W/mm on GaN substrates [10], 12 W/mm on silicon substrates [11] and 12W/mm on sapphire substrates [12]. Also, [8] shows improved FoMs of PA, in which they are designed using two 48 mm AlGaN/GaN HEMTs on semi-insulating SiC substrates and producing a saturated output power of 370W (drain bias of 45V) with a linear gain of 11.2 dB at 2.14 GHz excited with W-CDMA input signal. Though, these reported works are typically for small-size devices and usual power densities are 2 to 5 W/mm for larger devices.

AlGaN/GaN HEMT has high sheet carrier density and high saturation electron velocity, which is responsible for high output power and also it has high electron mobility, which leads to low on-resistance, and therefore, high power added efficiency. Due to consequence of its wideband material, it can achieve very high breakdown voltage, very high current density, and sustain very high operating temperature. The input and output impedances of these devices are also large because of their high power densities. Ultimately all these parameters indirectly improve the linearity of the AlGaN/GaN HEMT [13]. The superior efficiency and linearity figures indicate how AlGaN/GaN HEMTs have profoundly changed the outcome of microwave PA design.

However, the technology of processing AlGaN/GaN HEMTs is still not mature and some technological issues such as drain current collapse, reliability and appropriate packaging for thermal management remain to be solved consistently. So to solve these problems, initial stage is to start with appropriate small signal modeling strategy.

1.1 Transistor modeling for Power Amplifier Design

The simulation of various circuit designs in computer-assisted design (CAD) environment is highly dependent on the ease of availability of the model files of the circuit components. Hence, the modeling of power amplifier components like transistors will reduce the complexity involved in simulating the design. An accurate model of transistors will result in the minimization of the differential error in the simulated and the fabricated design parameters.

The design of power amplifier improves using models in CAD environment because models allow to iterative simulation for performance improvements of the circuit variants. Therefore, the designer can find an efficient circuit version before fabrication, which ultimately minimizes the iterations of fabrication and reduces the cost. Figure 1.2 and 1.3 shows the design process without model and with model respectively.

Modeling of transistor can help to evaluate and improve the fabrication process of device. So the model parameters must maintain a correlation with physical meaning of device. Small-signal models are the initial approach to transistor modeling and consist of linearization around an operating point of the nonlinear device. However, accurate description of key nonlinear effects of modern transistors requires more complete models, known as large-signal models. But this thesis focuses mainly on small-signal model.

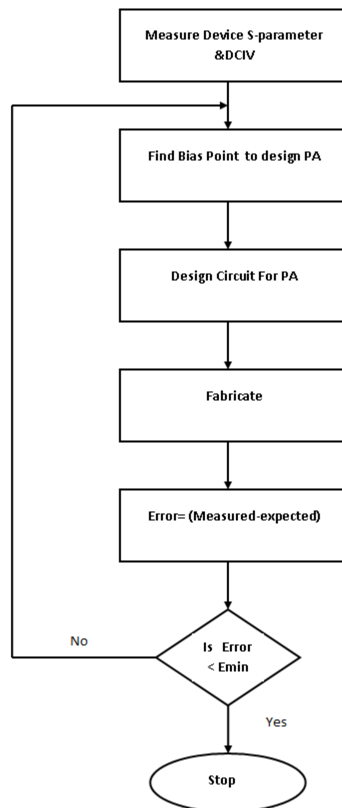

Figure 1.2: Flow Chart for circuit design without using models and CAD

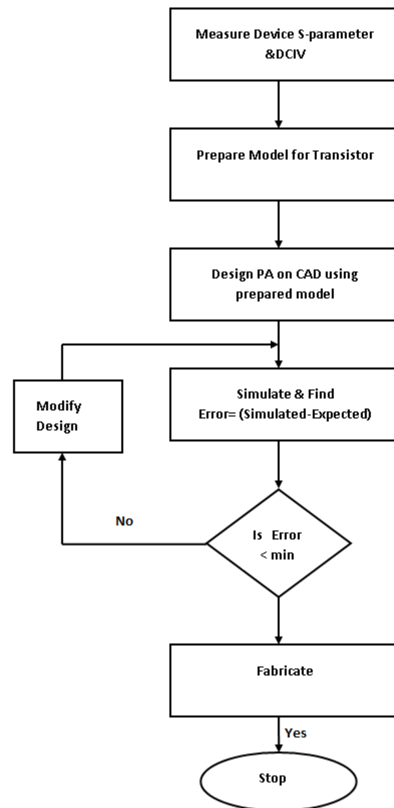

Figure 1.3: Flow Chart for circuit design with using models and CAD

1.1.1 Fundamental type of Modeling

Fundamentally there are two types of modeling.

- Physical Modeling This modeling methodology involves the analysis and the understanding of the physical parameters of the device like its dimensions, geometries, free charge carriers transport properties and the properties of the material used [13]. It involves solving complex non-linear differential equations, which is a time consuming process and took larger memory storage. So it is not very efficient for circuit designer.

- Empirical Modeling This modeling methodology is based on the measurement of electrical parameter like current and voltage. These measured parameters are further used to develop an equivalent electrical circuit. One of the approaches for empirical modeling is to construct an analytical equation to relate electrical parameters, known as "analytical models" [14]. Another method which is widely used is 'tabular method', where a list of independent variable is maintained and used with interpolation technique. Commonly it is termed as "table- used models" [15]. Analytical method has its own limitation like limited accuracy, technology dependency and non-physical meaning of fitting parameters. Tabular method

is having better accuracy and reliability. Unlike using mathematical equation, here we use multidimensional Spline curve fitting between extracted/measured data. So I am going to follow this method in my thesis.

1.1.2 Challenges of Modeling Advanced Transistors for High-Power Amplifiers

Due to the complex parasitic and nonlinear dependency, modeling GaN devices with equivalent circuits needs more comprehensive electrical networks with more number of parameters. As the model parameters grow, it leads to an increase in complexity of extraction and it also needs to apply optimization algorithm to find more accurate parameters. Mathematical optimization has its own drawbacks of emphasizing local-minima problems and concealing the physical interpretation of the parameters.

1.2 Main Objectives of the Research Work

The main agenda of this thesis is to develop a small-signal model of GaN HEMTs for the design of PAs. It contains the modeling approach to represent the complex physical effects of GaN HEMTs such that it should maintain the physical meaning of the model-parameters as close as possible. The extraction of model parameters depends on measurements of S-parameter for various bias points. Model approach involves taking standard number of measurements while maintaining a concise database and a user friendly model in CAD software.

1.3 Outline of the Thesis

Chapter 1 introduces the reader into the research field, providing a bird view to the general problematic of the thesis, from the topic of telecommunications into the specific aspects of transistor modeling for power amplifiers and also, stating the main objectives of the research work.

Chapter 2 discusses about basic HEMTs physics and need of wide-bandgap semiconductors to be used in the fabrication of transistors. It also talks about comparison of GaN with currently-used materials. That chapter also presents the GaN HEMTs DC and RF performance used for modeling in this thesis.

Chapter 3 deals with the initial subtask of the small signal modeling strategy and the key results for model verification.

Chapter 2

AlGaN/GaN HEMTs

Semiconductor devices were first introduced as a replacement for vacuum tube devices and once a field dominated by Silicon and Germanium, has seen the introduction of many alloy type semiconductor material and in particular Gallium Arsenide (GaAs). With theses advancement the frequency performance improved but the power delivering capability was still limited. Limit of the power delivering capability for solid devices depends on the DC voltage across its terminal. Each device has its own internal breakdown field limitation that ultimately limits DC voltage, which means that high RF power operation can only be achieved with large DC and RF currents, which need large area devices. However large area means high capacitance and low impedance. Finally it restricts the operating frequency.

The DC and RF performance capability of semiconductor devices is basically dependent upon the electronic, thermal, and mechanical properties of the materials from which the devices are fabricated. In this chapter an overview of materials properties and their significance is discussed along with the fundamentals of physics and operation of AlGaN/GaN HEMT. It also includes basics of the structure, and performance.

Table 2.1 lists values (collected from references [16–18]) of these properties for bulk materials like, Si, SiC, diamond, GaAs, and GaN.

Material properties include a large energy gap, Eg (eV), high charge carrier mobility μ_n(cm$^2/V.s$)

Table 2.1: Comparison of value of material propertied for different semiconductors

Property of bulk material [unit]	**GaN**	**4H-SiC**	**Diamond**	**GaAs**	**Si**
Bandgap [eV]	3.4	3.2	5.5	1.4	1.1
Electron mobility at 300 K [cm$^2/V.s$]	440	700	1900	4000	1500
Electron saturation velocity [$10^7 cm/s$]	2.5	2.0	2.7	1.0	1.0
Breakdown field [MV/s]	3.3	3.0	5.6	0.4	0.3
Thermal conductivity [W/cm.K]	1.3	3.7	20	0.5	1.5
Relative dielectric constant [-]	9.0	10.0	5.5	12.8	11.8

and saturation velocity, a low value of dielectric constant, ϵ_r, high thermal conductivity, κ (W/K-cm), and high critical electric field for breakdownE_c (V/cm).

Wide bandgap energy shows material capability to withstand high internal electric fields before electronic breakdown happens.

The dielectric constant gives an indication of the capacitive loading of a device and affects the terminal impedance. A low value for the semiconductor dielectric constant may reduce the capacitive loading and allows larger area devices to be fabricated for specified impedance. Increased area permits larger RF currents and higher RF power to be generated [1].

The thermal conductance needs to be as high as possible in order to extract heat from the device efficiently. Diamond and SiC are excellent thermal conductors and have been used as substrates for GaN HEMTs [1].

Finally, the critical electric field for electronic breakdown should be high. This parameter is an indication of the strength of the electric fields that can be supported internally by the device before breakdown occurs. High electric fields permit large RF voltages to be supported, and hence high RF power to be generated. One of the attractive features of the wide bandgap materials is a high value for the critical field for breakdown, which is typically an order of magnitude greater than that of conventional semiconductors.

2.1 v-E Characteristics

A current is defined as the movement of charge and expressed as the product between the charge density and transport velocity. Therefore, the DC and RF currents that flow through a device are directly dependent upon the charge carrier velocity versus electric field transport characteristics of the semiconductor material. Generally, for high currents and high frequency, high charge carrier mobility and high saturation velocity are desirable. A comparison of the electron velocity-electric field v-E characteristics for several semiconductors is shown in Figure 2.1 [1].

The v-E characteristic is described in terms of charge carrier mobility μ_n $(cm^2/V.s)$, defined from the slope of the v-E characteristic at low electric field, and the saturated velocity vs (units of cm/sec), defined when the carrier velocity obtains a constant, field-independent magnitude, generally at high electric field. The high value for electron mobility of GaAs (typically, μ_n 5000 cm$^2/V.s)$ is the main reason that FETs fabricated from this material have such excellent low noise and high-frequency performance [1].

In general, both high mobility and high saturation velocity are desirable for high RF current. Si and GaAs have electron saturation velocities that are limited to about $v_s = 10^7 cm/s$, and this limits both the power that can be generated and the frequency response of the device. Wide

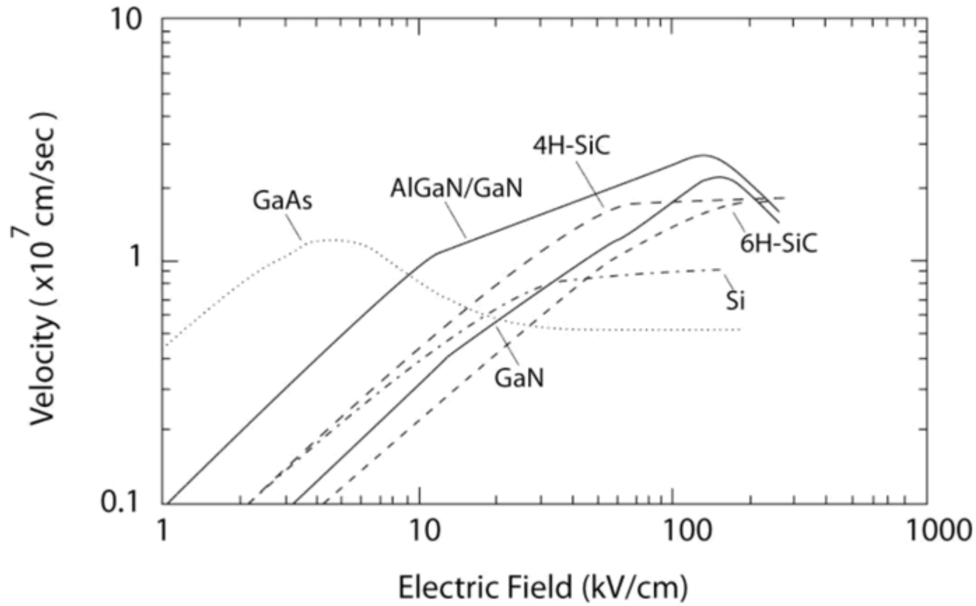

Figure 2.1: Electron velocity vs. electric field characteristic for several semiconductors (Nd = 10^{17} cm^{-3}) [1]

bandgap semiconductors have electron saturation velocities that are a factor of two higher. The combination of high current and high voltage capability make wide bandgap semiconductors very attractive candidate for fabrication of high-power and high-performance electronic devices [15].

The relationship among material properties, device FoMs and overall system performance is summarized in table 2.2.

Table 2.2: Device and system level performance advantages of using wide bandgap materials for power transistors (adopted from [4]

Material Property	**Device Operates**	**Improved Device Figure of Merit**	**System Advantage**
High breakdown field	High voltage operation High doping	Power density Power Gain Efficiency Output Impedance IMD	Increased BW Smaller number of die per system Efficiency
High Thermal Coductivity & Wide Bandgap	High temperature	Smaller die size More power/die	Smaller and cheaper package
High Electron Velocity	High Frequency	High fr and fmax	High System Frequency

2.2 Basic HEMT definition

The desired properties of a semiconductor are that it should have high electron mobility and abundant carrier concentration. To increase the carriers in a semiconductor material, it needs to use higher dopants and because of introduction of more dopants, the presence of immobile ions increase. Due to high electric field interaction, the carriers start scattering and results to effective mobility degradation. So aim is now to have high carrier density without affecting mobility degradation, without directly introducing the dopants in material. So researchers find a way to supply charge carriers to material when it is required. It leads to concept of HEMTs. The high electron mobility transistor (HEMT) is a key component for today's high-performance microwave devices. It is a heterostructure field effect transistor, which has advantage of high transport properties of abundant carrier present in potential well. A heterostructure consist of at least two layers of different semiconducting materials with distinct bandgaps. The interface between two of these layers is called hetrojunction [19].

For the basic understanding of hetrojunction, a simplified band diagram of HEMTs device is shown in fig 2.2. In Fig 2.2 consist two distinct bandgap material with doped/supply layer (here for e.g, it is n-type doped AlGaAs) and other is undoped/buffer (GaAs) layer. Initially when materials are kept apart the Fermi level of n-type doped material is closer to conduction band edge and undoped material Fermi level is at middle of bands. When these two materials placed closer then electrons must be transferred from the supply layer into the undoped layer to align the Fermi level. Another way to see this is that the conduction band on the AlGaAs side lies energetically higher than that on the GaAs side, results into the energy of the electrons in the conduction band of the AlGaAs layer is higher than that of the GaAs layer. Because electrons tend to occupy the lowest allowed energy state, they are encouraged to move from AlGaAs to GaAs. This leads to a sizable increase in the electron concentration within the GaAs layer even without the introduction of ionized donor impurities.

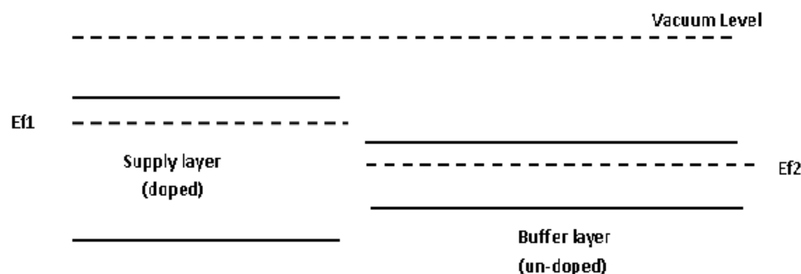

Figure 2.2: Energy band diagrams of the AlGaAs and GaAs layers when apart and in equilibrium [18]

Figure 2.3 shows a sharp dip of the band edge occurs at the doped/undoped interface. It results

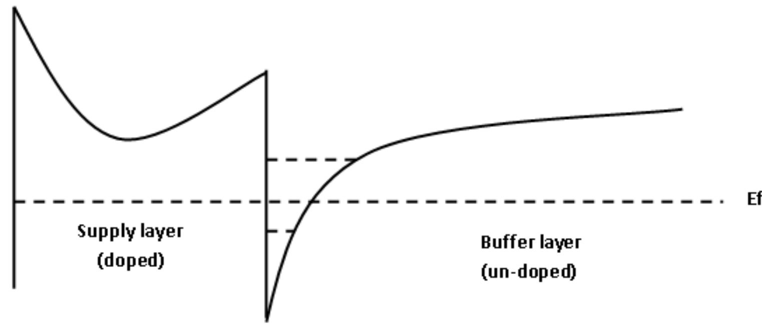

Figure 2.3: Energy band diagram of the heterostructure. The two dashed horizontal lines at the heterointerface in the GaAs layer represent energy subbands arising from spatial quantization effects [2]

in high carrier concentration in a narrow region (a quantum well). The spread of electrons in the quantum well is essentially two-dimensional. Therefore the charge density is termed a two-dimensional electron gas (2DEG) and quantified in terms of sheet carrier density.

2.3 AlGaN/GaN strcture and its band diagram

AlGaN/GaN HEMT has been fabricated in a similar way using doped or undoped AlGaN layer as shown in Figure 2.4. It has been observed that a 2DEG is formed in the AlGaN/GaN interface even when there is no intentional doping of AlGaN layer. So the reason to form 2DEG here is due to presence of a strong polarization field across the AlGaN/GaN heterojunction. A 2DEG with the sheet carrier density up to $10^{13} cm^{-2}$ can be achieved without any doping [20]. The basic layered structure shown in Figure 2.4 and band diagram of the structure is illustrated in Figure 2.5. Here band diagram include complete source to drain region and showing the flow of charge carrier with an appropriate potential difference.

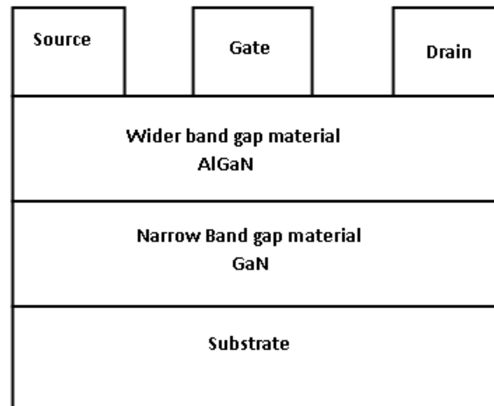

Figure 2.4: Simplified AlGaN/GaN HEMT structure

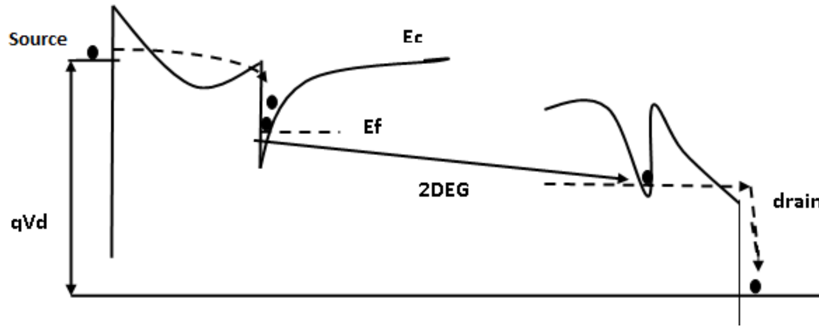

Figure 2.5: HEMT structure and energy bands at source and drain contacts [3]

2.4 AlGaN/GaN HEMT Performance

2.4.1 IV Characteristics

DC IV characteristics for 4x100 μm gate width AlGaN/GaN HEMT are shown in Figure 2.6. The maximum zero gate voltage current (I_{DSO}) is equal to $205mA$ and the drain knee voltage ($V_{DS,Knee}$) is approximately 5V. The extracted maximum extrinsic transconductance ($G_{m,max}$)

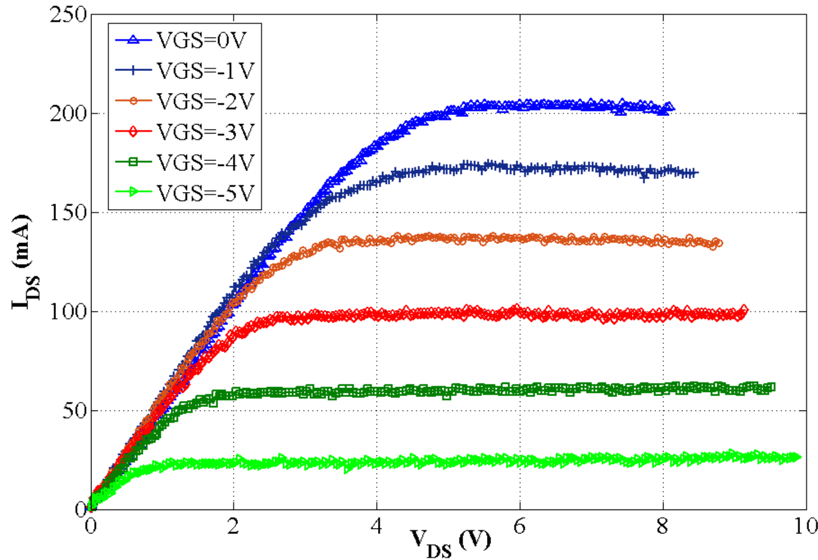

Figure 2.6: DC IV Characteristics for 4x100 μm device

is equal to $96mS$. With increasing V_{GS} the knee voltage is shifting right and the breakdown voltage is shifting left. So the power delivering region is becoming narrower. Max power that can be delivered by this device is given by equation 2.1. This device is capable of delivering 615 mW power.

$$P_{out} = \frac{1}{8}(I_{max} - I_{min})(BV_{gd} - V_{knee}) \tag{2.1}$$

2.4.2 RF Characteristics

The unity current gain frequency (f_t) and the maximum oscillation frequency (f_{max}) are useful figures of merit for understanding of the frequency response performance of any transistors. f_t is the frequency at which the short circuit current gain, h_{21}, is unity. f_t can be extracted from S-parameter measurements by transforming S-parameters into H-parameters and then h_{21} is plotted (in dB) versus frequency using the equation 2.2.

$$h_{21}(dB) = 20log(\frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}) \tag{2.2}$$

We can obtain f_t , from the linear fitting extrapolation of the h_{21} curve with the frequency axis. Normally, f_t is a good indication of the maximum achievable gain-bandwidth for resistively terminated device. f_{max} is the frequency at which maximum unilateral gain (MUG) is unity. It is obtained with the condition of conjugate matched input and output of the device (max power transfer) and eliminating the feedback gate-drain impedance. This frequency is the maximum possible frequency to achieve power amplification using the device. f_{max} can be extracted from the S-parameter measurements utilizing the following expression

$$\text{MUG (dB)} = 10 \text{ log } (\frac{1}{(1-|S_{11}|^2)} \mid S_{21} \mid^2 \frac{1}{(1-|S_{22}|^2)}) \tag{2.3}$$

And again like f_t , it is also obtained by extrapolating the curve of MUG versus frequency. The values of f_t and f_{max}, at certain bias condition are function of the structure of the device, which provides the values of the intrinsic parameters and the parasitic elements. Figure 2.7 and 2.8 shows the extracted value of f_t and f_max at different bias points for a 2x200 μm gate width AlGaN/GaN HEMT respectively. As shown in the figure, the maximum value of f_t for class A and AB operated device is approximately 18 GHz, while the maximum value of f_{max} is approximately 30 GHz.

At lower voltages or at lower drain current, f_t increases with an increase of V_{GS} voltages due to an increase of the transconductance. The decrease of f_t value at high voltages or at high drain current is due to the self-heating effect, and it reduces the value of electron velocity, leads to the smaller transconductance. f_{max} has the same trend as f_t because they are correlated. It can also be conclude that the value of f_t and f_{max} increases with drain voltage. This increase is mainly

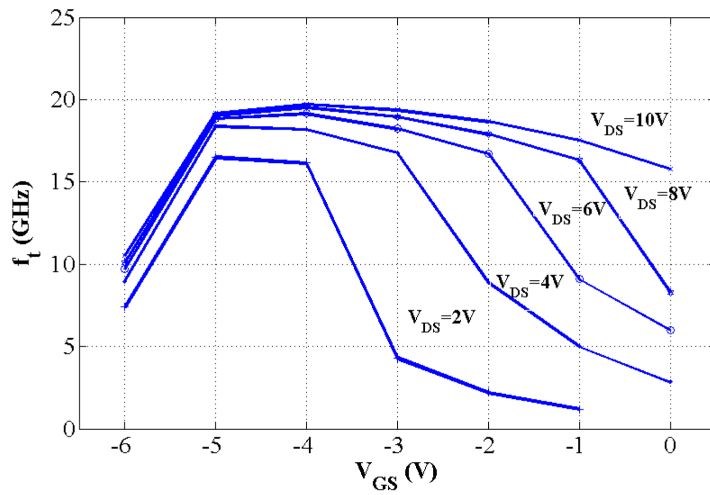

Figure 2.7: Measured unity gain frequency (f_t) for 2x200 μm gate width vs gate voltage

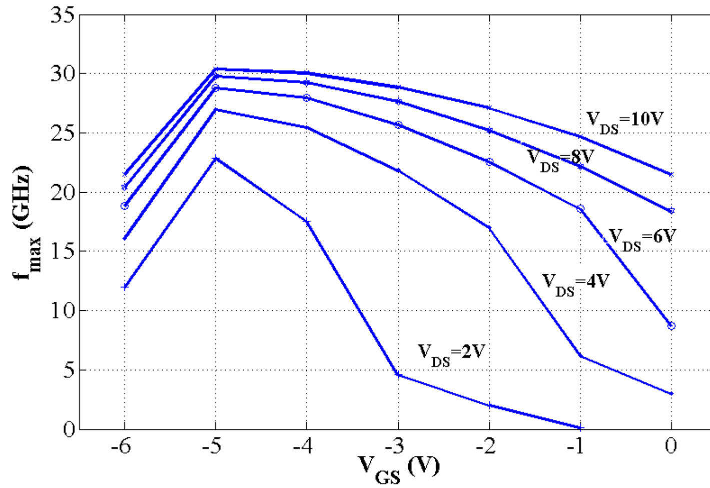

Figure 2.8: Measured max oscillation frequency (f_{max}) for 2x200 μm gate width vs gate voltage

because of the decrease of gate-drain intrinsic capacitance with increasing the drain voltage [21].

Chapter 3

Bias-Dependent Linear AlGaN/GaN HEMTs Model

Small signal models and extraction technique of parameters of FETs are being used by researchers since decades, but continuous revision is needed as the new device technologies evolve. The small-signal equivalent circuit model of a FET is the representation of the linear electrical behavior of the device over a frequency range and at a specific operating bias point. The parameters of the equivalent circuit are usually lumped elements. Each element in the equivalent circuit is used to approximate some aspects of the device physics.

In deriving the small-signal model of a FET, S-parameter data under different bias conditions are used. However, basic device physical layout and geometry data are also useful inputs in estimating model parameters.

The number of elements required in the equivalent circuit, the topology of the network and the model parameters extraction procedures that are necessary to provide a good match to the measured S-parameters over wide frequency range have been intensively studied. There are a number of factors that increase the complexity of the required small-signal equivalent circuit model. Among these are the complexities of the device layout, immature device processing technology, conductive substrate, and breakdown and leakage currents. In this case, a sample representative device can be used to make the necessary measurements and thereby derive the model.

The linear model of FET is useful in the design of active linear circuit design. It may also be the basis for deriving some of the nonlinear large-signal model elements of the device. The large-signal charge models are derived from the bias dependent capacitances of the small-signal model. Other benefits of using small-signal equivalent circuit are model scaling and data size reduction. Since the electrical equivalent circuit model elements are frequency independent, there is data size reduction as compared to using the S-parameter directly in a circuit design. The small-signal

equivalent circuit elements may be scaled with gate width and number of gate fingers thereby enabling the designer to predict the S-parameters of different device sizes. Theoretically, it can also be used to extrapolate device performance beyond the original measurement data range.

This procedure of extracting model parameters from measured S-parameters can be basically repeated to a range of bias points. The small-signal equivalent circuit element values for each bias point can be extracted from the corresponding S-parameters measured at that particular bias point. The variation of each model element as function of the bias (gate- and drain-voltages) can then be determined. Hence, the result is a bias-dependent small-signal model that can be used for linear circuit design for bias ranges considered. Usually there are no good analytical functions that can fit to most of these bias dependent equivalent circuit elements. Consequently, look-up table based models that use spline or other interpolation and extrapolation techniques are better alternatives.

In this chapter, the determination of the extrinsic and bias dependent intrinsic elements of the small-signal model of AlGaN/GaN HEMTs is discussed.

3.1 Electrical Equivalent Circuit Model

Small-signal model derivation procedure starts by defining electrical equivalent circuit (EEC). The EEC definition needs a watchful examination of the layout of the FET structure to identify relevant parasitic elements. Figure 3.1 shows a general small-signal EEC model.

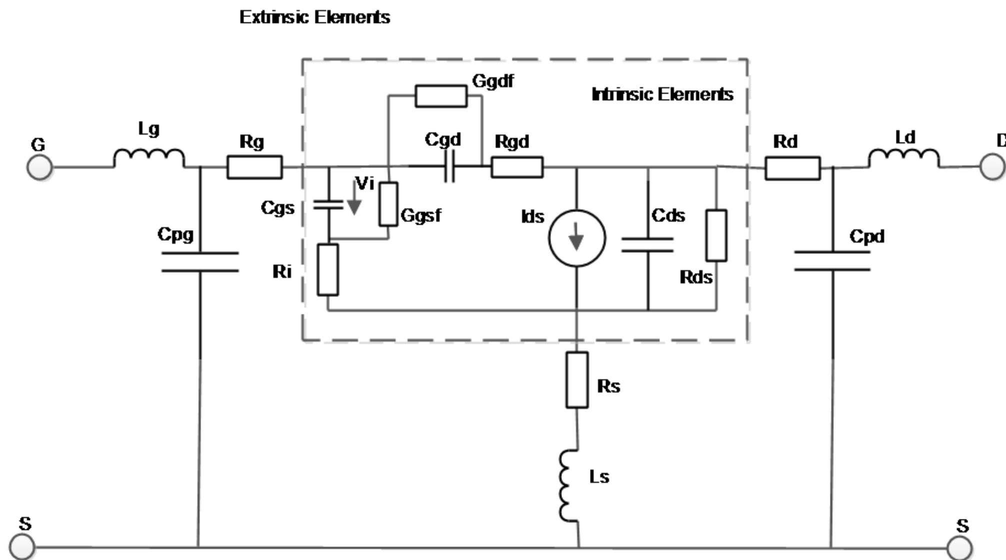

Figure 3.1: Typical small-signal equivalent circuit of a FET

The equivalent circuit model contains linear bias independent extrinsic parameters covering the

device parasitic and the nonlinear bias dependent intrinsic elements that model the active region under the gate. The extrinsic part models the RF contact pads and gate, drain, and source metallization effect.

The parameters G_{gdf} and G_{gsf} represents forward conductances of the gate-drain and gate-source regions. It is related to effects of gate-current leakage, which are normal to appear when the diode-like effects of those regions are forward biased. The intrinsic capacitance parameters C_{gs} and C_{gd} represent charge-storage effects in the gate-source and gate-drain regions between the gate electrode and the 2DEG. The capacitances C_{gs} and C_{gd} require finite times to charge, which are represented by the time constants R_iC_{gs} and $R_{gd}C_{gd}$. That is the physical interpretation of the intrinsic resistance parameters R_i and R_{gd}. In this equivalent circuit, R_i and R_{gd} are cascaded to their corresponding capacitance and the conductance parameters, in contrast with other typical models that set them in series only with Cgs and Cgd, as presented in [22].

The current flow in the 2DEG is described in the EEC with the parameters I_{ds} and R_{ds}. The current source is controlled by the input voltage V_i (voltage across C_{gs}) and the current is proportional to the controlling voltage by a factor that is the device transconductance G_m and it is delayed from the input voltage by the parameter τ which describes the propagation time of electrons in the 2DEG from drain to the source. The R_{ds} parameter (or its equivalent reciprocal $G_{ds} = 1/R_{ds}$) approximates the sheet resistance appearing around the 2DEG space, whereas C_{ds} describes the geometric capacitance related to this region.

The distributed inductive and resistive effects due to the electrodes behaving as transmission lines are represented by L_g, L_d and L_s, and R_g, R_d and R_s, for the gate, drain and source, respectively. C_{pg} and C_{pd} are the parasitic capacitances includes the effect due to pads and inter-electrodes and due to fingers air bridge.

3.1.1 Extrinsic Parameters

The procedure for the extraction of the extrinsic parameters is based on two S-parameter datasets. Both datasets are obtained with the device drain bias voltage set to zero ($V_{DS} = 0$ V) also referred as "cold-FET" conditions. Under this bias condition, the voltage controlled drain-source current can be removed from the equivalent circuit model and the FET is placed in passive condition and the intrinsic FET equivalent circuit can be simplified considerably. In fact, two cases of the simplified equivalent circuit, corresponding two gate-bias conditions, are used to determine the extrinsic parameters. These are the gate-forward ($V_{GS} \geq 0$) and a gate-reverse voltage lower than the pinch-off voltage ($V_{GS} \leq V_P$) of a FET.

The agenda is to extract the parasitic capacitances from the gate bias below pinch-off ($V_{GS} \leq V_P$) while the series parasitic resistances and inductances are determined from gate forward ($V_{GS} \geq 0$) bias conditions of measured S-parameters keeping drain voltage to zero ($V_{DS} = 0$ V).

In the following section, the main steps used to extract these parasitics parameters for 2 x 200 μm AlGaN/GaN HEMT. The procedure has also been applied to 4 x 100 μm devices but the mostly results presented here are mainly for the 2 x 200 μm device in order to avoid repetitions of procedure descriptions. But where it is needed, both device parameter data are presented.

3.1.2 Parasitic Capacitances

Simplifications to the cold-FET equivalent circuit can be assumed at gate bias voltages lower than pinch off. Under these bias conditions, the small-signal equivalent circuit of the cold-FET simplifies to the one shown in Fig. 3.2 [23]. The depletion region under the gate is described by three identical capacitors C_b, which are associated with gate, source, and drain symmetrically [23].

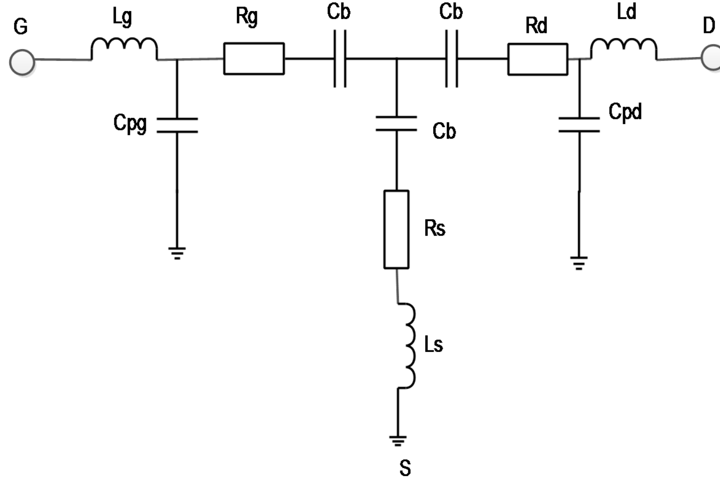

Figure 3.2: Simplified small-signal equivalent circuit at cold-pinch off bias [23].

Depending on this equivalent circuit, the gate and drain parasitic capacitances, C_{pg} and C_{pd}, can be estimated from cold pinch-off S-parameters data. The inductances can be neglected at low frequencies and the simplified expressions can be deduce using T to π converted equivalent circuit (shown in figure 3.3) for the imaginary parts of the Y-parameters of this circuit are

$$Im(Y_{11}) = j\omega(C_{pg} + \frac{2}{3}C_b) \tag{3.1}$$

$$-Im(Y_{12}) = \text{-Im}(Y_{12}) = \text{j}\omega\tfrac{C_b}{3} \tag{3.2}$$

$$Im(Y_{22}) = j\omega(C_{pd} + \frac{2}{3}C_b) \tag{3.3}$$

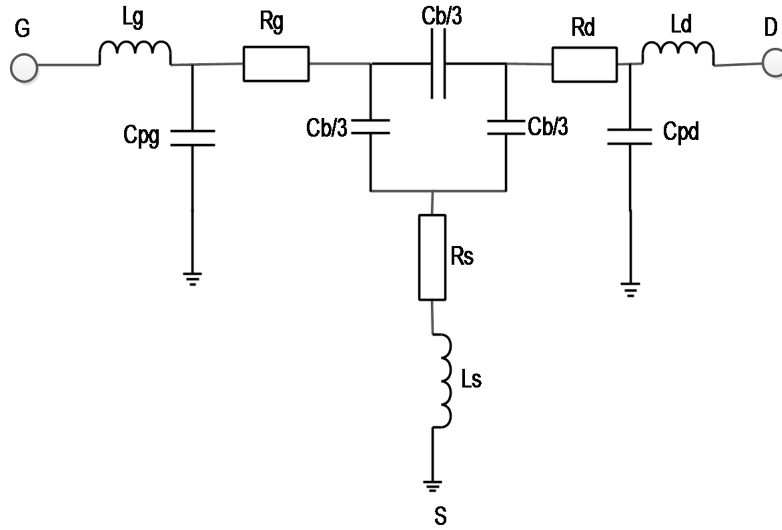

Figure 3.3: π equivalent for Figure 3.1

The equivalent circuit shown in Figure 3.3 gives better parasitic capacitances for FETs having gate and drain bond pads similar in shape and size. This can be observed for the 2 x 100 μm GaN HEMT [Fig. 3.4] where its parasitic capacitance is dominated by the bond pads and $\text{Im}(Y_{11}) \approx \text{Im}(Y_{22})$. But for the 4 x 100 μm GaN HEMT, gate-source capacitances contribute to substantially to $\text{Im}(Y_{11})$. This significant contributation is mainly due to the dimensions of the gate and drain electrode and their distance to the source air-bridge interconnect. $\text{Im}(Y_{22})$ is almost similar but with small increment due to same reason. Multiples of air-bridge sources interconnects makes the geometry more complex than the 2-finger HEMT so $\text{Im}(Y_{11})$ and $\text{Im}(Y_{22})$ are not necessarily comparable [Fig.3.5] even though the gate and drain pads have similar size and shape.

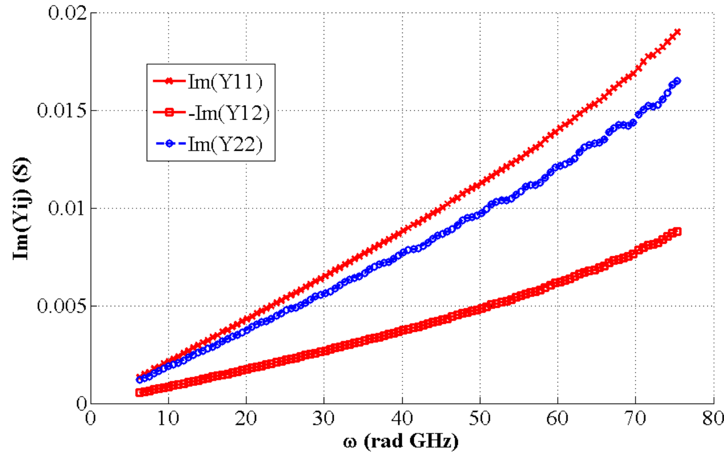

Figure 3.4: $\text{Im}(Y_{ij})$ parameters of GaN HEMTs at $V_{DS} = 0$ V and gate bias voltage below pinch-off for 2 x 200 μm device

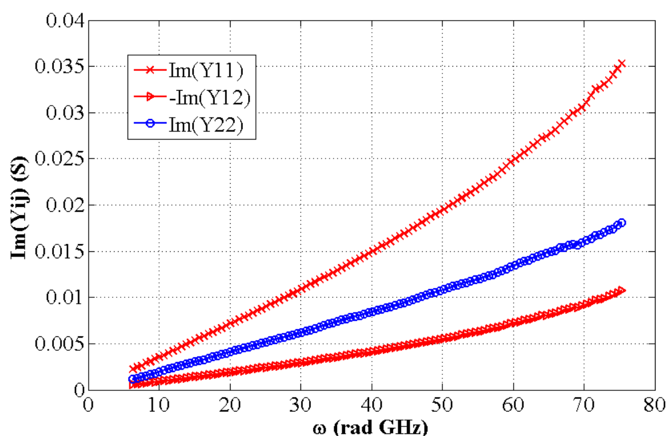

Figure 3.5: Im(Y_{ij}) parameters of GaN HEMTs at $V_{DS} = 0$ V and gate bias voltage below pinch-off for 4 x 100 μm device

From the slope of the Im(Y_{11}), Im(Y_{12}) and Im(Y_{22}) versus ω plots in Fig. 3.4, the total gate-source, gate-drain and drain-source capacitances are 126.4 fF, 85.6 fF and 98.8 fF respectively for the 2 x 200 μm GaN HEMT. With help of equation (3.1) - (3.3), one gets $C_{pg} = 43.8$ fF , $C_{gd} = 85.6$ fF and $C_{pd} = 15.6$ fF. A similar analysis of Fig. 3.5 for the 4 x 100 μm GaN HEMT gives $C_{pg} = 170$ fF , $C_{gd} = 91.1$ fF and $C_{pd} = 18$ fF. It is evident that due to more number of fingers gate pad capacitance is more, and it is because of more inter-electrode capacitance with source air bridge.

3.1.3 Parasitic Resistances and Inductances

Traditionally, S-parameters measured under gate-forward condition of the cold-FET were used to determine parasitic resistances and inductances. The Schottky barrier under the gate is modeled by distributed RC network [24]. But this old procedure cannot be directly used for HEMTs. Because first, the gate-to-channel contact for HEMTs is not only Schottky barrier as in MESFETs but a Schottky contact in series with a heterojunction and second, the high gate forward bias is not a typical operating condition of a FET and such measurement may also damage the device. This procedure may also result in overestimated source and drain resistances [25].

Researchers have used S-parameter of "Unbiased FET" [25, 26] which is biasing the transistor at $V_{GS} = V_{DS} = 0$ V instead of gate-forward bias condition to extract the parasitic inductances and resistances. This procedure will be followed here. The equivalent circuit as shown in Fig. 3.7 is used for the unbiased-FET [25] where r_g and C_g represent the differential resistance and capacitance of the Schottky barrier respectively.

The choice of bias condition for inductance extraction can be observed in Figure 3.5, which shows the evolution of S_{11} with increasing gate voltage for the 2 x 200 μm GaN HEMT, the inductive behavior is also increasing.

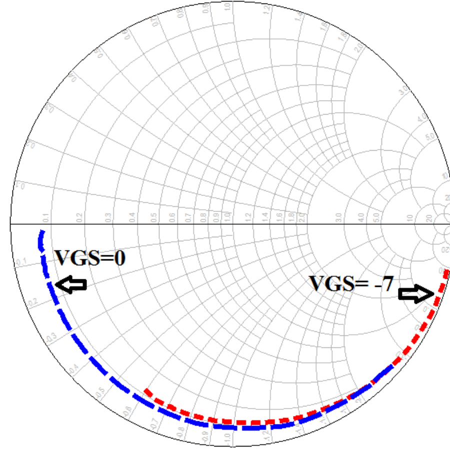

Figure 3.6: Evolution of S11 for cold- pinch off FET and unbiased FET of 2 x 200 μm AlGaN/GaN HEMT

After de-embedding C_{pg} and C_{pd} the parasitic inductances can be readily identified from the imaginary parts of the Z-parameters. The Z parameters for circuit in fig 3.7 are

$$Z_{11} = R_g + R_s + \frac{R_c}{2} + \frac{r_g}{D} + j\omega(L_g + L_s - \frac{C_g r_g^2}{D}) \tag{3.4}$$

$$Z_{12}{=}Z_{21}{=}R_s + \tfrac{R_c}{2} + j\omega L_s \tag{3.5}$$

$$Z_{22} = R_d + R_s + R_c + j\omega(L_d + L_s) \tag{3.6}$$

where R_c is the channel resistance, r_g and C_g are the differential resistance and capacitance, respectively. $D = 1 + (\omega C_g r_g)^2$. And now define branch impedances Z_g , Z_s and Z_d for gate, source and drain respectively as

$$Z_g = Z_{11} - Z_{12} \tag{3.7}$$

$$Z_s{=}Z_{12}{=}Z_{21} \tag{3.8}$$

$$Z_d = Z_{22} - Z_{12} \tag{3.9}$$

The use of the equivalent circuit shown in Fig. 3.7 is also justified, by observing the shapes of

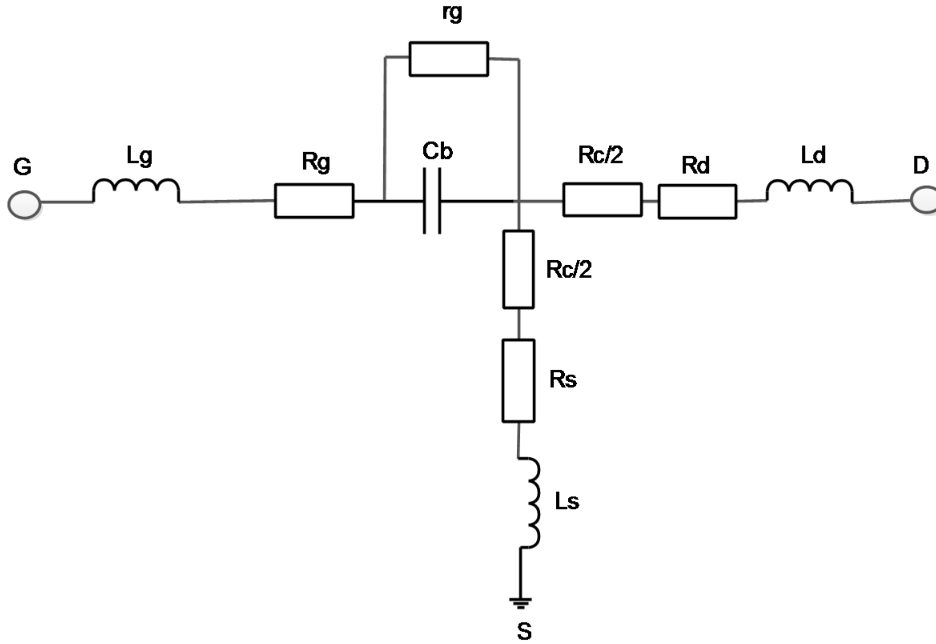

Figure 3.7: Simplified small-signal equivalent of unbiased FET (VGS = 0 V ,VDS = 0 V) [25].

real (Fig. 3.11 3.12) and imaginary (Fig. 3.10) parts of the gate branch impedance, Z_g as given in equation (3.11). The shape of $Re(Z_g)$ versus ω plot in fig 3.11 and 3.12 illustrates the decreasing r_g/D part with increasing frequency. Similarly, $\omega.\ Im(Z_g)$ versus ω^2 plot should be a straight line at high frequency with slope L_g and the y-intercept of this line gives the capacitance C_g. Both L_s and L_d are readily obtained from Im(Z_s) and Im(Z_d) versus ω plots respectively as shown in Fig. 3.8 for 2 x 200 μm and fig 3.9 for 4 x 100 μm. It is evident from fig 3.8 and 3.9 L_s inductance are very small and for 2 x 200 μm device, it is appearing negative; the reason could be dominance of capacitance.

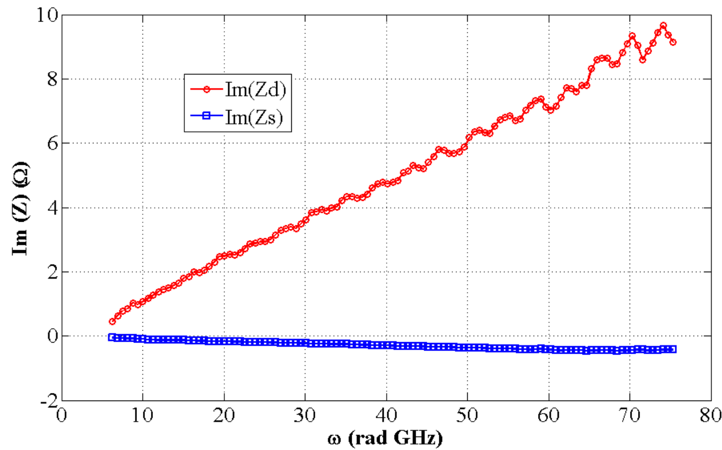

Figure 3.8: Measured imaginary parts of the drain and source branch impedances of unbiased 2 x 200 μm GaN HEMT

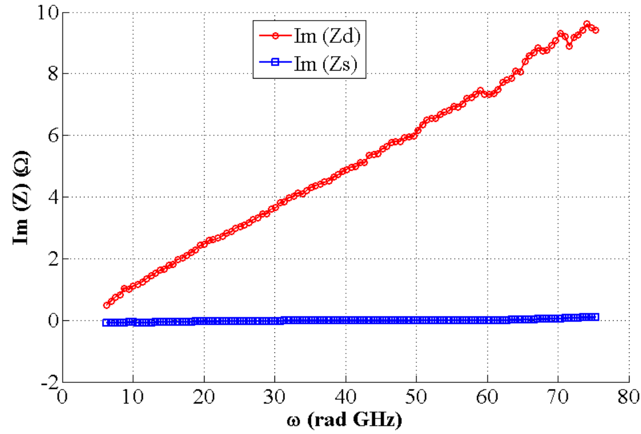

Figure 3.9: Measured imaginary parts of the drain and source branch impedances of unbiased 4 x 100 μm GaN HEMT

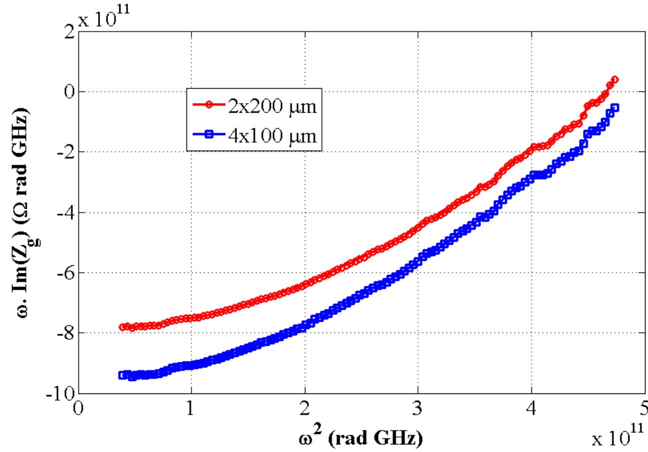

Figure 3.10: Measured imaginary parts of the gate branch impedances of unbiased 2 x 200 μm and 4 x 100 μm GaN HEMT

Now consider the real parts of the branch impedances of the above equation set and the plots in fig. 3.11 and 3.12. One notes that R_g can be obtained from the horizontal asymptote of Re(Z_g) plot where r_g/D becomes negligible. The resistance $R_s + \frac{R_c}{2}$ and $R_d + \frac{R_c}{2}$ are also identified from Re(Z_s) and Re(Z_d) plots, respectively. And following a method described in [26], the sum $R_s + R_d$can be determined from Re(Z_{22}) of pinch-off data and hence one can then calculate R_s , R_c and R_d in that order. The extrinsic parameters determined are summarized in table 3.1 and 3.1 for both devices.

Table 3.1: Parasitic resistances from unbiased cold-FET conditions of 2 x 200 μm and 4 x 100 μm GaN HEMTs

Unbiased HEMT	**2x200 μm**	**4x100 μm**
R_g**[ohm]**	4.55	2.395
$R_s + R_c/2$ **[ohm]**	2.690	2.923
$R_d + R_c/2$ **[ohm]**	3.469	3.097

Table 3.2: Extrinsic parameters of 2 x 200 μm and 4 x 100 μm GaN HEMT based on small-signal EEC model in fig. 3.1

GaN HEMT	C_{pg} **[fF]**	C_{pd} **[fF]**	R_g **[ohm]**	R_s **[ohm]**	R_d **[ohm]**	L_g **[pH]**	L_s **[pH]**	L_d **[pH]**
2 x 200 μm	44	15.6	4.55	0.801	1.58	138.34	0.009	123.2
4 x 100 μm	170	18	2.395	1.1035	1.2725	138.34	1.93	123.2

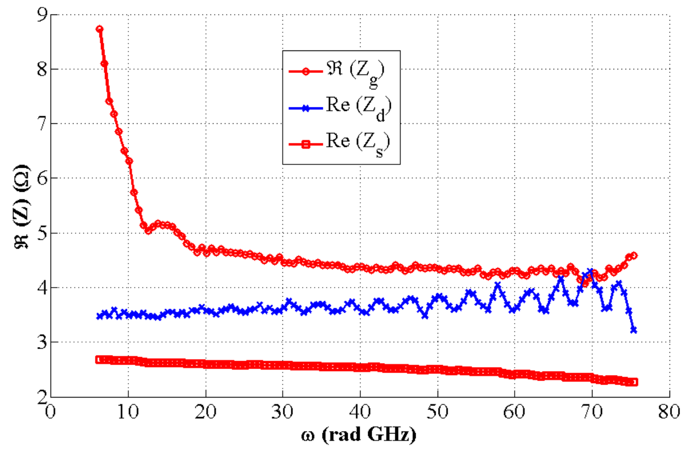

Figure 3.11: Measured real parts of the Z-parameters of the branch impedances of unbiased 2 x 200 μm GaN HEMT

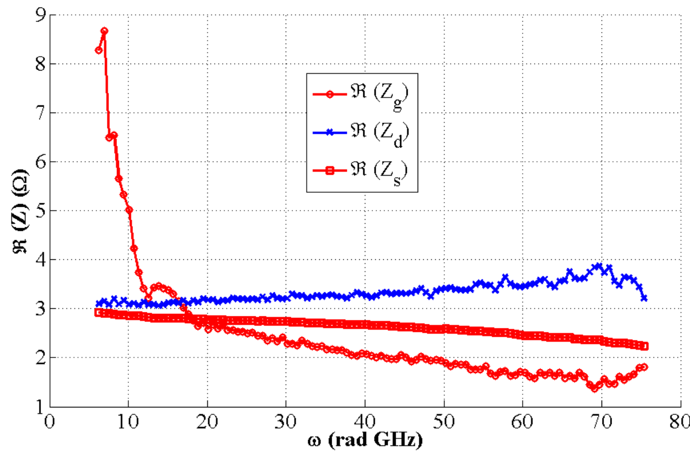

Figure 3.12: Measured real parts of the Z-parameters of the branch impedances of unbiased 4 x 100 μm GaN HEMT

3.1.4 Intrinsic Parameter Extraction

After calculating the extrinsic parameter values, their effects are subtracted from S-parameters measurements at each bias point of interest, to obtain the Y-parameters matrix of the intrinsic transistor. The intrinsic transistor is formulated as four branch admittances: Y_{gs}, Y_{gd}, Y_{gm} and Y_{ds}, with the electric circuit shown in Figure 3.13. The admittance of the intrinsic gate-source

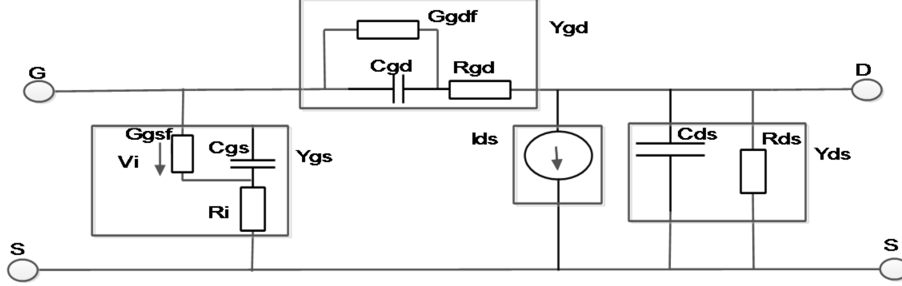

Figure 3.13: Intrinsic transistor equivalent circuit formulated with admittance branches

branch Y_{gs} is given by

$$Y_{gs} = Y_{11} + Y_{12} = \frac{G_{gsf} + j\omega C_{gs}}{1 + R_i G_{gsf} + j\omega R_i C_{gs}} \tag{3.10}$$

By defining a new variable D as

$$D = \frac{\mid Y_{gs} \mid^2}{Im[Y_{gs}]} = \frac{\mid G_{gsf} \mid^2}{\omega C_{gs}} + \omega C_{gs} \tag{3.11}$$

C_{gs} can be determined from the slope of the curve for ω D versus ω ^{2} by linear fitting, where ω is the angular frequency. Again by redefining D as

$$D = \frac{Y_{gs}}{Im[Y_{gs}]} = \frac{G_{gsf}(1 + R_i G_{gsf})}{\omega C_{gs}} + \omega R_i C_{gs} - j \tag{3.12}$$

R_i can be determined from the plot of the real part of ω D versus ω ^{2} by linear fitting. G_{gsf} can be determined from the real part of Y_{gs} at low frequencies. The admittance for the intrinsic gate-drain branch Y_{gd} is given by

$$Y_{gd} = -Y_{12} = \frac{G_{gdf} + j\omega C_{gd}}{1 + R_{gd} G_{gdf} + j\omega R_{gd} C_{gd}} \tag{3.13}$$

The same procedure, given in (4.35) and (4.36), can be used for extracting C_{gd}, R_{gd}, and G_{gdf}.

The admittance of the intrinsic transconductance branch Y_{gm} can be expressed as

$$Y_{gm} = Y_{21} - Y_{12} = \frac{G_m e^{j\omega\tau}}{1 + R_i G_{gsf} + j\omega C_{gs}} \tag{3.14}$$

By redefining D as

$$D = (G_{gsf} + j\omega C_{gs}) \frac{Y_{gm}}{Y_{gs}} = G_m e^{-j\omega\tau} \tag{3.15}$$

G_m and τ can be determined from above equation (3.15) using magnitude and phase plot with respect to ω with linear curve fitting. The admittance of intrinsic drain-source branch Y_{ds} can be expressed as

$$Y_{ds} = Y_{22} + Y_{12} = G_{ds} + j\omega C_{ds} \tag{3.16}$$

It is clear that from equation (3.16) that real part give G_{ds} and C_{ds} can be calculated from imaginary part.

Figures 4.12, 4.13, and 4.14 present the extracted intrinsic parameters versus the extrinsic bias voltages. The extraction results show the typical expected characteristics of the AlGaN/GaN HEMT.

The intrinsic parameters C_{gd} and C_{gs} appears as a parallel-plat capacitance whose two plates are formed by the gate metal and the 2DEG channel charge [27]. For a constant V_{DS} and V_{GS} decreasing from 0V towards the pinch-off region, negative charges at the gate due to the increasingly negative V_{GS} reduce the charge storage in the gate-drain and gate-source regions. The corresponding reductions of C_{gd} and C_{gs} are observed in the extracted values shown in Figure 3.14. It can also observed that with $V_{DS} = 0$V and V_{GS} increasing from pinch-off towards 0V, C_{gs} increase to a maximum value, which occurs around the V_{GS} value that corresponds to the maximum transconductance G_m. After that maximum point, C_{gs} will show again a notable decrease. With a fixed V_{GS}, increasing V_{DS} from 0V presents positive charges in the drain that hinder the capacitive effects of the gate-drain region, leaving the gate-source region unaffected. Thus, effects denoted by C_{gd} decrease, whereas those denoted by C_{gs} remain roughly constant. But it can be noted that gradual increase for C_{gs} with increasing the drain voltage is observed around the grounded gate voltage ($V_{GS} = 0$V). This reduction is due to decrement in depletion layer depth and it is because of the lateral electric field established by the drain voltage, accelerates charge carriers in the channel to scatter into the barrier layers and reduces effective amount of available carriers.

G_m is defined as the rate of change of the drain current with respect to the gate voltage. Then, its bias dependency can be inferred from the DC IV transfer characteristic. With $V_{DS} = 0$V or

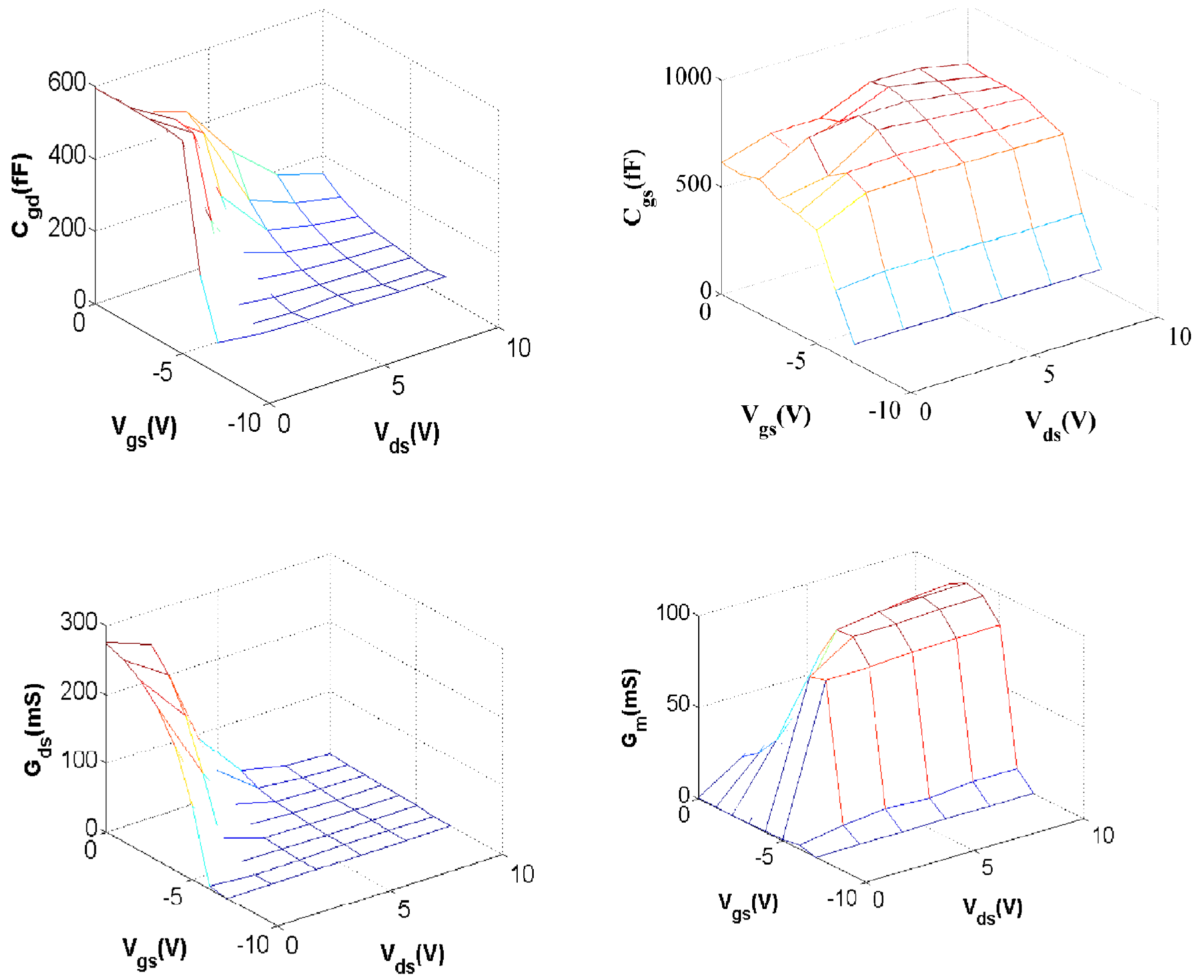

Figure 3.14: Extracted C_{gd}, C_{gs}, G_m, and G_{ds} as a function of bias voltages for a 2x100 μm gate width AlGaN/GaN HEMT

with V_{GS} near pinch-off or more negative, the values of G_m are expected to be low. It increases rapidly in the low V_{DS} range when V_{GS} increase from the pinch-off. For large V_{DS} values G_m is expected to show a saturated behavior that allow high drain currents.It can also inferred from that due to high electric field condition electron velocity saturates. With V_{DS} above 0V, it is a known characteristic of GaN HEMTs that the transconductance has a non-symmetrical bell-shape with respect toV_{GS}, with an increase from pinch-off than gradual decrease after the peak value. These properties of the transconductance are well represented by the extracted G_m as presented in Figure 3.14.

G_{ds} models the change of the drain current with the drain voltage. Thus, small values forG_{ds} in the saturation region can be clearly visible in Figure 3.14. Increasing the gate voltage increases G_{ds} because it increase the channel charge density and thus the drain current. This increase becomes observable in the ohmic region due the reduction of the depletion layer.

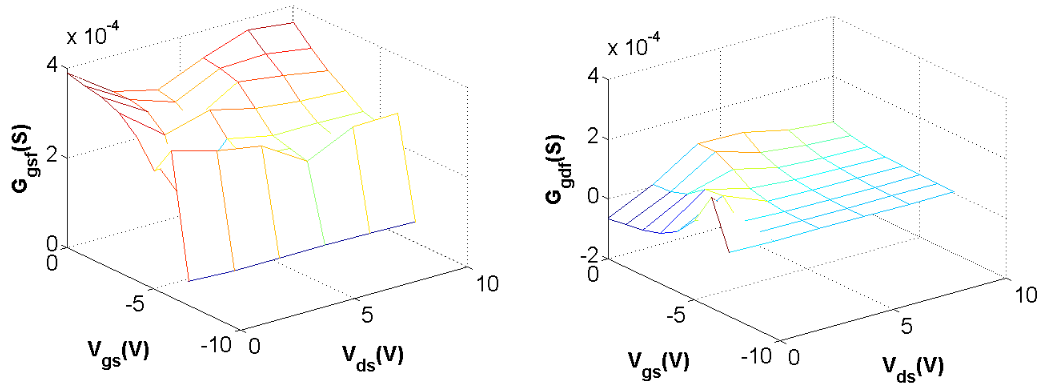

Figure 3.15: Extracted G_{gsf}, and G_{gdf} as a function of bias voltages for a 2x100 μm gate width AlGaN/GaN HEMT

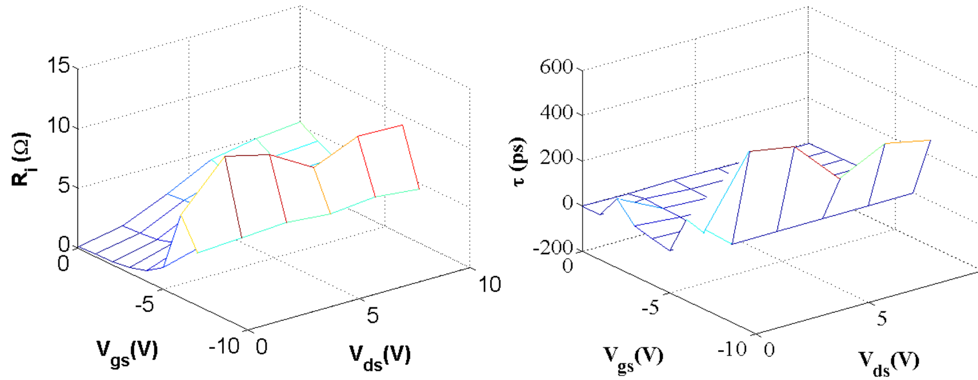

Figure 3.16: Extracted R_i, and τ as a function of bias voltages for a 2x100 μm gate width AlGaN/GaN HEMT

G_{gsf} and G_{gsf} represent the conduction current through the gate diodes. Therefore, they have large values only when the gate voltage is increasing towards more forward bias and it can be seen in Figure 3.15.

R_i models the undepleted part of the channel under the gate, and represent spatial delays in the setup of the charge storage effects related to gate-source capacitance. The value of R_i is equal to the ratio of the potential drop in this channel part and the channel current, which is approximately equal to the drain current [28]. Therefore, it is expected that the value of R_i should be high in the low drain-current region as shown in Figure 3.16. The parameter τ represents the time delay due to the drift of electrons along the 2DEG. It increases strongly as the gate voltage approaches the pinch-off region and as the drain voltage approaches 0V. This is correctly shown by the extracted values of this parameter in Figure 3.16.

R_{gd} have same physical definition as R_i and it also represent spatial delays in the setup of the charge storage effects related to gate-drain capacitance, as shown in Figure 3.17. The physical

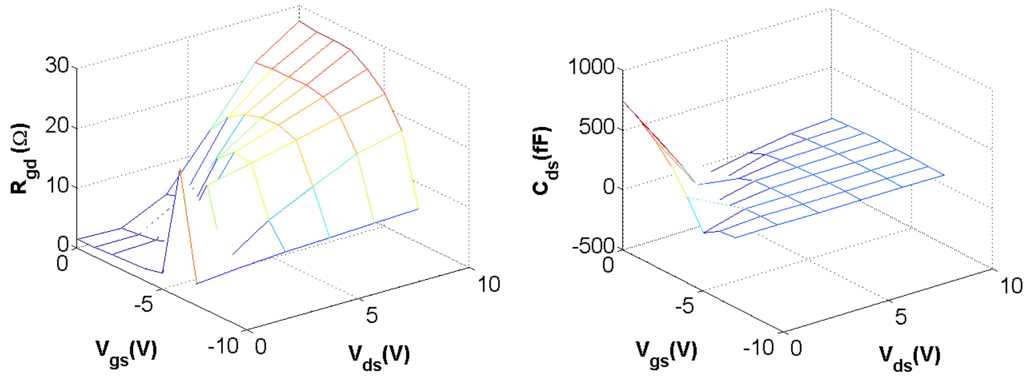

Figure 3.17: Extracted R_{gd}, and G_{ds} as a function of bias voltages for a 2x100 μm gate width AlGaN/GaN HEMT

origin of C_{ds} is the geometrical capacitance between drain and source. C_{ds} values decrease as V_{GS} increase and allows the 2DEG formation. The emergence of significant effects related to C_{ds} around V_{DS} = 0V and V_{GS} = 0V has been reported in [29, 30]. The sudden negative value of C_{ds} in the ohmic region (at low V_{DS}) is known in small-signal model parameters extraction procedures of FETs [31]. It is explained that the negative capacitance observed is as inductive effect of a resonant circuit below its resonance frequency. This leads to that an RLC circuit is required in the drain-source circuit. But we have already used an RLC model. So in this case, C_{pd} or L_s may have been underestimated. The result is shown in Figure 3.17.

3.2 Small- Signal Model Verification

The small-signal modeling is verified through the simulation of the S-parameter for the 2 x 200 μm device. Figure 3.18 and 3.19 shows the results of S-parameter simulation at two different bias points, in pinch off and saturation regions, over a wide frequency range from 1 GHz to 10 GHz. Very good agreement is achieved between measurements and simulations at shown bias points $V_{GS} = -7V \;\; V_{DS} = 0V$ and $V_{GS} = -3V \;\; V_{DS} = 8V$, with relative error of 2% and 4% respectively. The relative error distribution at different bias point is presented in Figure 3.20. Average error across given bias points is 7.33%. The relative error is defined here as

$$RelativeError = \frac{1}{N}\sum_{N}\frac{1}{4}\sum_{ij}\frac{\mid S_{ij}^{mes} - S_{ij}^{sim} \mid}{\mid Sij \mid}. \tag{3.17}$$

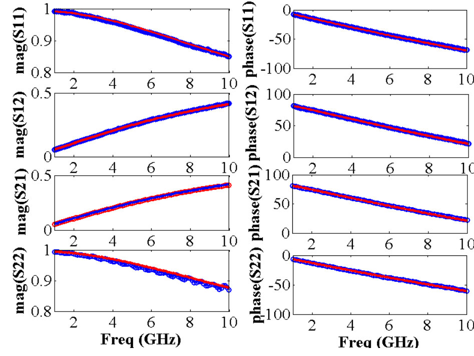

Figure 3.18: S-parameter Comparison of measured (shown in red) and simulated (shown in blue) at bias voltage $V_{GS} = -7V \quad V_{DS} = 0V$ for a 2x100 μm gate width AlGaN/GaN HEMT

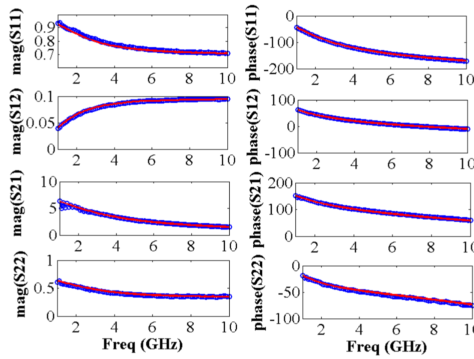

Figure 3.19: S-parameter Comparison of measured (shown in red) and simulated (shown in blue) at bias voltage $V_{GS} = -3V \quad V_{DS} = 8V$ for a 2x100 μm gate width AlGaN/GaN HEMT

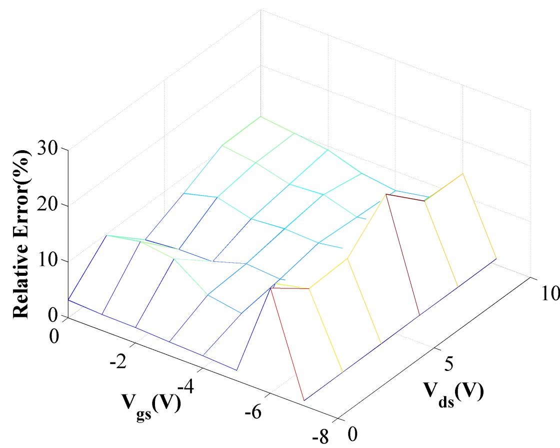

Figure 3.20: Relative Error for a 2x100 μm gate width AlGaN/GaN HEMT

Chapter 4

Conclusion and Future Work

4.1 Conclusion

In this dissertation, AlGaN/GaN HEMT small-signal model has been shown and its equivalent circuit modal parameter is extracted. After modeling for simulation the table based approach has been followed. Finally a complete flow chart is shown in Figure 3.20 and 3.21 of the complete extraction process. And the flow chart also include the optimization processes to enhance result of some modal parameter showing unexpected behavior like C_{ds} and L_g. After iteration of process we reach an effective model parameter value by minimizing relative errors. Results has not be shown here because that have almost similar trend as we discussed above.

The small-signal modeling process is completed in ADS circuit simulator. Where deembedding process is done using in-built function. DAC data management block is to store modal parameter in table format and used for simulation at different bias.

4.2 Future work

Here a small signal model is prepared. But for PA, large signal model is more close to real scenario because it can depict the linearity for non-linear PA design.

GaN HEMTs fabrication process is still in immature stage. So, this device have huge problem with trapping of carriers and self heating. So these effects are also need to be modeled and for that pulsed IV measurement is needed.

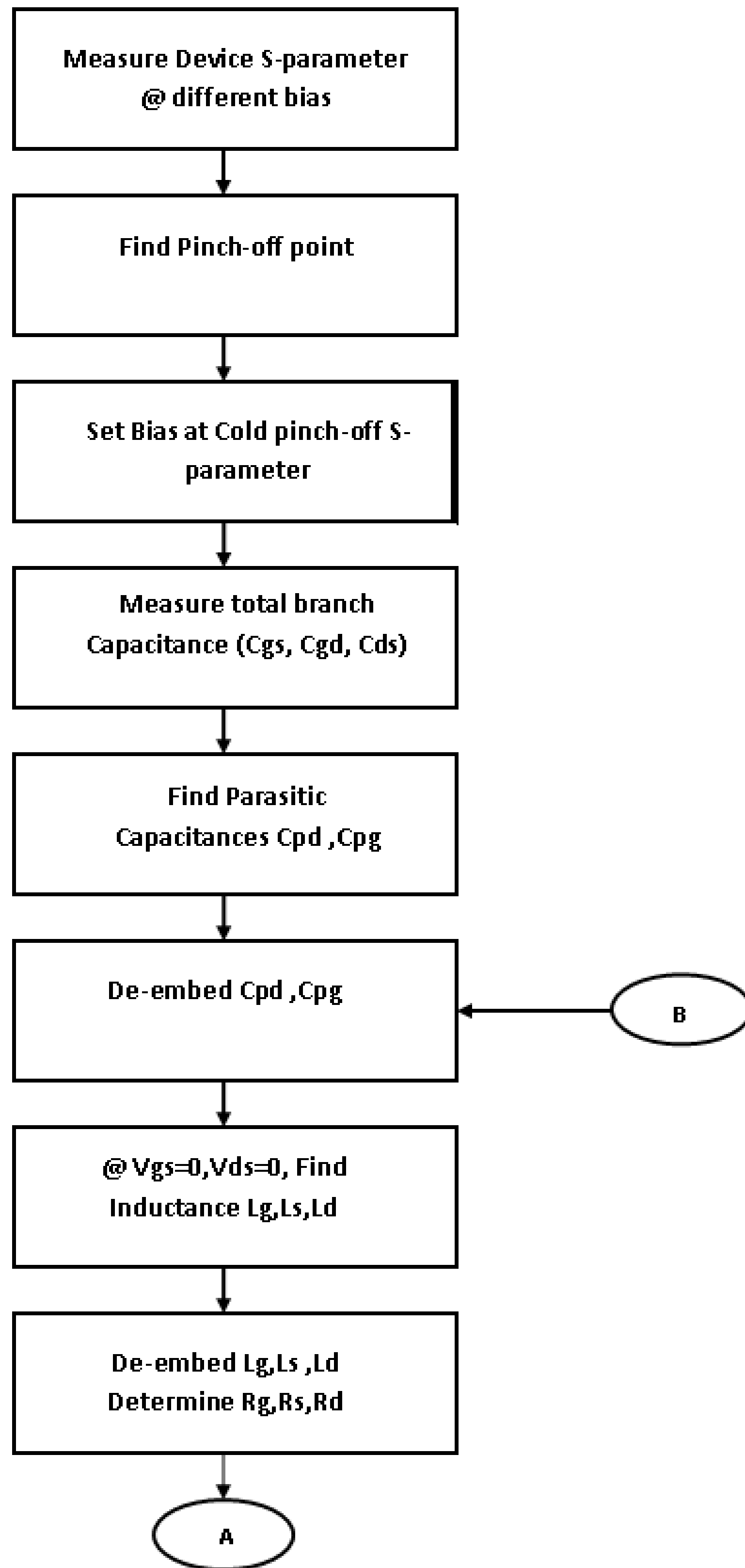

Figure 4.1: Complete flow chart of extraction process part-I

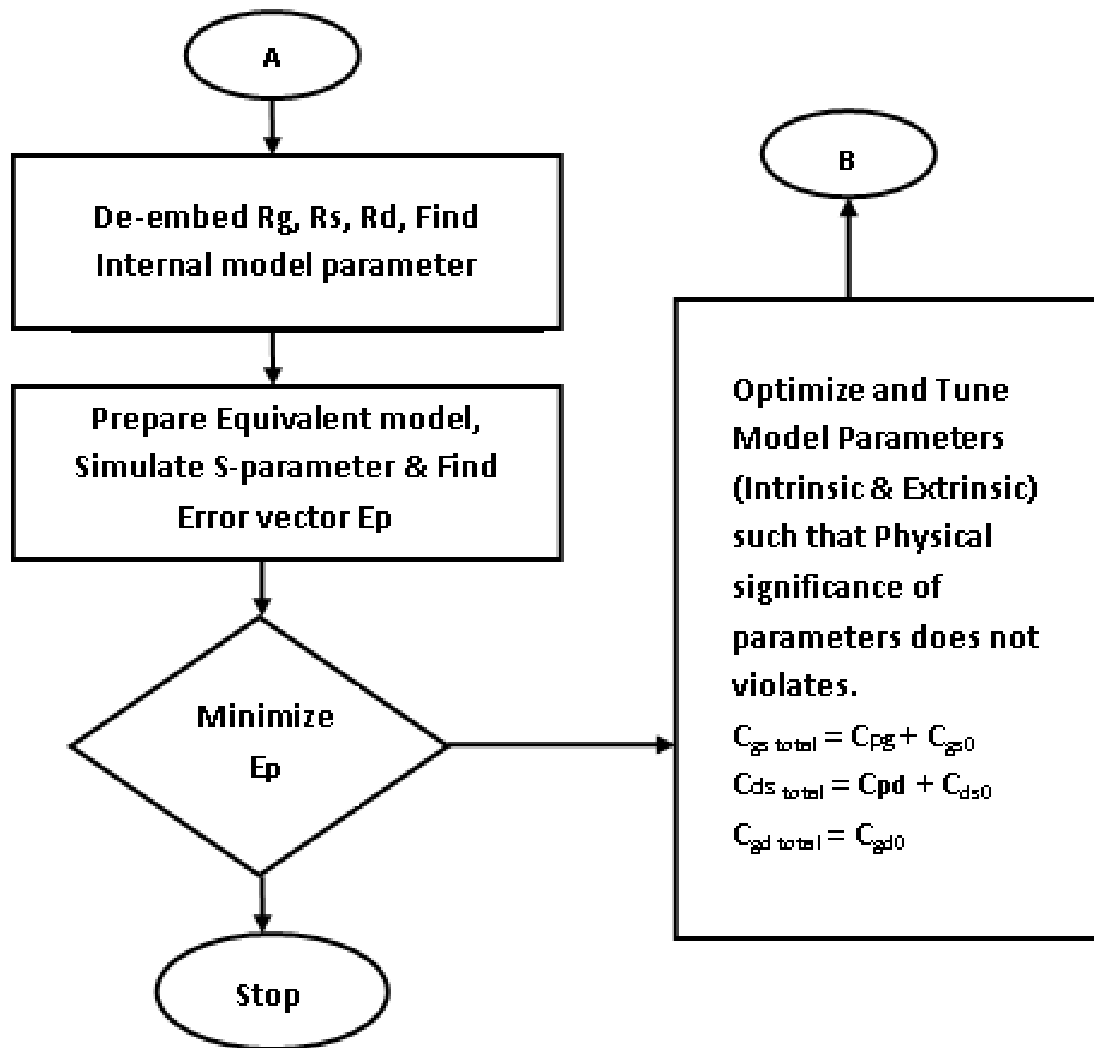

Figure 4.2: Complete flow chart of extraction process part-II

Bibliography

[1] R. J. Trew, "High-frequency solid-state electronic devices," *IEEE transactions on electron devices*, vol. 52, no. 5, pp. 638–649, 2005.

[2] K. F. Brennan and A. S. Brown, *Theory of modern electronic semiconductor devices.* John Wiley, 2002.

[3] D. Sima, "Understanding semiconductor devices," ISBN 0-19-513186-X.–New York: Oxford University Press, 2000.–574 P, Tech. Rep., 2000.

[4] M. Golio, *RF and microwave semiconductor device handbook.* CRC press, 2002.

[5] H. Ku and J. S. Kenney, "Behavioral modeling of nonlinear rf power amplifiers considering memory effects," *IEEE transactions on microwave theory and techniques*, vol. 51, no. 12, pp. 2495–2504, 2003.

[6] R. Raich and G. T. Zhou, "On the modeling of memory nonlinear effects of power amplifiers for communication applications," in *Digital Signal Processing Workshop, 2002 and the 2nd Signal Processing Education Workshop. Proceedings of 2002 IEEE 10th*, Oct 2002, pp. 7–10.

[7] P. M. Cabral, N. Borges Carvalho, and J. C. Pedro, "An integrated view of nonlinear distortion phenomena in various power amplifier technologies," 2003.

[8] W. Nagy, J. Brown, R. Borges, and S. Singhal, "Linearity characteristics of microwave-power gan hemts," *IEEE transactions on microwave theory and techniques*, vol. 51, no. 2, pp. 660–664, 2003.

[9] Y.-F. Wu, A. Saxler, M. Moore, R. Smith, S. Sheppard, P. Chavarkar, T. Wisleder, U. Mishra, and P. Parikh, "30-w/mm gan hemts by field plate optimization," *IEEE Electron Device Letters*, vol. 25, no. 3, pp. 117–119, 2004.

[10] K. Chu, P. Chao, M. Pizzella, R. Actis, D. Meharry, K. Nichols, R. Vaudo, X. Xu, J. Flynn, J. Dion *et al.*, "9.4-w/mm power density algan-gan hemts on free-standing gan substrates," *IEEE Electron Device Letters*, vol. 25, no. 9, pp. 596–598, 2004.

[11] J. Johnson, E. Piner, A. Vescan, R. Therrien, P. Rajagopal, J. Roberts, J. Brown, S. Singhal, and K. Linthicum, “12 w/mm algan-gan hfets on silicon substrates,” *IEEE Electron Device Letters*, vol. 25, no. 7, pp. 459–461, 2004.

[12] A. Chini, D. Buttari, R. Coffie, S. Heikman, S. Keller, and U. Mishra, “12w/mm power density algan/gan hemts on sapphire substrate,” *Electronics Letters*, vol. 40, no. 1, p. 1, 2004.

[13] A. Kranti, S. Haldar, M. Gupta, R. Gupta *et al.*, “Comprehensive analysis of small-signal parameters of fully strained and partially relaxed high al-content lattice mismatched al m ga 1-m n/gan hemts,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 2, pp. 607–617, 2003.

[14] W. R. Curtice, “A mesfet model for use in the design of gaas integrated circuits,” *IEEE Transactions On Microwave Theory Techniques*, vol. 28, pp. 448–456, 1980.

[15] D. Root, S. Fan, and J. Meyer, “Technology-independent large-signal fet models: A measurement-based approach to active device modeling,” in *Proc. 15th ARMMS conf*, 1991, pp. 1–21.

[16] R. Trew, “Wide bandgap semiconductor transistors for microwave power amplifiers,” *IEEE Microwave magazine*, vol. 1, no. 1, pp. 46–54, 2000.

[17] L. F. Eastman and U. K. Mishra, “The toughest transistor yet [gan transistors],” *IEEE spectrum*, vol. 39, no. 5, pp. 28–33, 2002.

[18] B. Ozpineci and L. Tolbert, *Comparison of wide-bandgap semiconductors for power electronics applications.* United States. Department of Energy, 2004.

[19] F. Schwierz and J. J. Liou, *Modern microwave transistors: theory, design, and performance.* Wiley-Interscience, 2003.

[20] O. Ambacher, B. Foutz, J. Smart, J. Shealy, N. Weimann, K. Chu, M. Murphy, A. Sierakowski, W. Schaff, L. Eastman *et al.*, “Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped algan/gan heterostructures,” *Journal of applied physics*, vol. 87, no. 1, pp. 334–344, 2000.

[21] Y. Okamoto, Y. Ando, T. Nakayama, K. Hataya, H. Miyamoto, T. Inoue, M. Senda, K. Hirata, M. Kosaki, N. Shibata *et al.*, “High-power recessed-gate algan-gan hfet with a field-modulating plate,” *IEEE Transactions on Electron Devices*, vol. 51, no. 12, pp. 2217–2222, 2004.

[22] E. Chigaeva, W. Walthes, D. Wiegner, M. Grozing, F. Schaich, N. Wieser, M. Berroth, O. Breitschadel, L. Kley, B. Kuhn *et al.*, “Determination of small-signal parameters of

gan-based hemts," in *High Performance Devices, 2000. Proceedings. 2000 IEEE/Cornell Conference on.* IEEE, 2000, pp. 115–122.

[23] P. M. White and R. M. Healy, "Improved equivalent circuit for determination of mesfet and hemt parasitic capacitances from" coldfet" measurements," *IEEE microwave and guided wave letters*, vol. 3, no. 12, pp. 453–454, 1993.

[24] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the fet small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151–1159, 1988.

[25] J. Wood and D. E. Root, "Bias-dependent linear scalable millimeter-wave fet model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2352–2360, 2000.

[26] R. Tayrani, J. E. Gerber, T. Daniel, R. S. Pengelly, and U. L. Rohde, "A new and reliable direct parasitic extraction method for mesfets and hemts," in *Microwave Conference, 1993. 23rd European.* IEEE, 1993, pp. 451–453.

[27] H. Rohdin, A. Nagy, V. Robbins, C. Y. Su, A. S. Wakita, J. Seeger, T. Hwang, P. Chye, P. E. Gregory, S. R. Bahl *et al.*, "0.1 μm gate length alinas/gainas/gaas modfet mmic process for applications in high speed wireless communications," *Hewlett-Packard Journal Online*, 1997.

[28] P. H. Ladbrooke and M. Design, "Gaas fets and hemts, artech house," *Inc., Norwood, Massachusetts*, 1989.

[29] R. G. Brady, C. H. Oxley, and T. J. Brazil, "An improved small-signal parameter-extraction algorithm for gan hemt devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 7, pp. 1535–1544, 2008.

[30] G. Crupi, D. Xiao, D.-P. Schreurs, E. Limiti, A. Caddemi, W. De Raedt, and M. Germain, "Accurate multibias equivalent-circuit extraction for gan hemts," *IEEE transactions on microwave theory and techniques*, vol. 54, no. 10, pp. 3616–3622, 2006.

[31] C. Camacho-Peñalosa, J. Esteban, T. Martín-Guerrero, and B. Castillo-Vázquez, "On negative drain-to-source capacitances in microwave fet-type devices," in *Proceedings of the International Symposium on Microwave and Optical Technologies (ISMOT'01)*, 2001, pp. 115–118.