DESIGN OF HIGH GAIN AND LOW NOISE FIGURE ON-CHIP LNA FOR Ku BAND APPLICATION

By

VIJAY SHARMA

Under the Supervision of **Dr. M.S.HASHMI**

Indraprastha Institute of Information Technology Delhi

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Under the Supervision of **Dr. M.S.HASHMI**

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Communication.

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CERTIFICATE

This is to certify that the thesis titled "**DESIGN OF HIGH GAIN AND LOW NOISE FIGURE ON-CHIP LNA FOR Ku-BAND APPLICATION**" being submitted by **VIJAY SHARMA** to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

Sep, 2016

Dr. M.S.HASHMI
Department of Electronics and Communication Engineering
Indraprastha Institute of Information Technology Delhi
New Delhi 110 020

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ABSTRACT

Low Noise Amplifiers (LNA) are key components in the receiving end of nearly every communication system. Primary purpose of the LNA is to amplify the received signal while at the same time adding as little additional noise as possible. Its performance greatly affects the overall receiver performance. This thesis discusses design of narrow band low noise amplifiers for Ku band applications. The target of this thesis is to design a LNA at 17 GHz for Ku Band. It also addresses some of the main aspects of microwave LNA design for use in the Ku frequency band. Through evaluation of the published literature on the LNA designing, a circuit topology has been selected, explored and redesigned. The tradeoffs related to input and output mis-match, bandwidth and gain has been explored and discussed. Finally, LNA has been designed in 0.09 um CMOS process using Agilent's ADS having off-chip and on-chip inductors.

On-chip inductor technique reduces the contribution of spectral noise current due to inductor series resistance and provides a good matching at the LNA input and output. After resonance frequency inductor starts behaving like a capacitor. By the help of on-chip inductor, resonance frequency can be controlled. As this design includes on-chip rectangular spiral inductors, the design, and modeling of on-chip inductors have been discussed briefly.

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1. INTRODUCTION

1.1 Background

The first active amplification component of a receiver is a Low Noise Amplifier (LNA). The main function of LNA is to amplify the signal to suppress the noise of subsequent stages while adding as little noise as possible. The performance of RF receiver is significantly influenced by the LNA. Operating frequency also depends on the RF filter used in front of LNA.

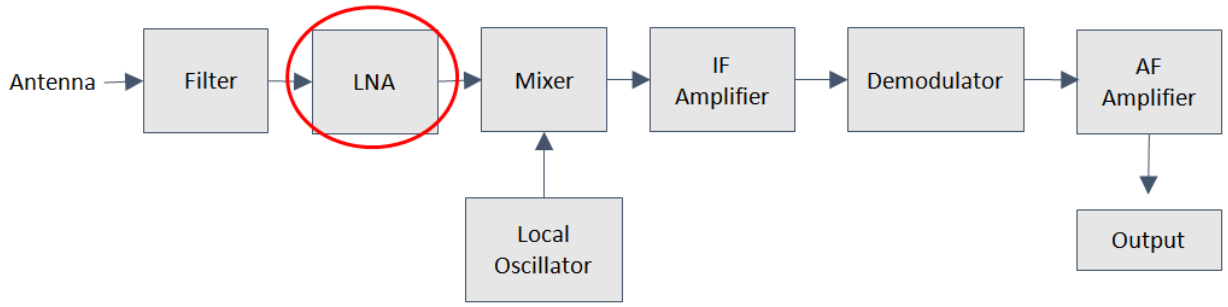

Figure 1.1: RF Receiver

Bipolar and GaAs used in earlier time for designing of LNA. They offer a good gain and low noise figure, But they are expensive and cannot be integrated easily. As the new technology evolved, we successfully researched the feasibility of the new CMOS technologies in RF circuit designs. CMOS devices translated into low noise figure and higher gain. Latest CMOS technologies showed to be a strong not only in terms of cost and integration, but also in terms of high performance.

Inductive source generated low noise amplifier provide best noise performance and gain. However, they operate in a narrow band of frequency. Inductive source degenerated low noise amplifier has been presented in this thesis which can be tuned to the required frequency of interest.

1.2 Objective

The objective of this thesis is to explain the concept of a Low Noise Amplifier (LNA) design for the use of the K_u Band. In this thesis, LNA is proposed for the 17 GHz in Ku-band. The LNA was optimized for low NF and high gain. The thesis consists of LNA design for reconfigurability in 0.09 um CMOS process.

Table 1.1: LNA Design Parameter and Specification

Parameter	Specification
Operating frequency	17 GHz (Ku-Band)
Gain	>20 dB
Noise Figure	<3dB
Input Matching 50 ohms	<-25 dB
Stability Factor	Should be unconditionally stable

1.3 Ku-Band and Its Application

Ku-band is the 12-18 GHz portion in the microwave range of frequencies. This symbol means K-under (originally German: *Kurz-unter*), this band directly below the K-band. It ranges from 12-18GHz according to the formal definition of radar frequency band nomenclature in IEEE Standard 521-2002.[1] Ku-band is not restricted in power to avoid interference with terrestrial microwave systems as compared to C-band. The power of uplink and downlink can be increased.

K_u band is generally used for satellite communication in fixed and broadcast services. It also used in NASA's tracking Data Relay Satellite used for both space shuttle and international space station communication.

1.4 On-Chip Inductor

On-chip inductor technique reduces the contribution of spectral noise current due to inductor series resistance and provides a good matching at the LNA input and output. It enhances the reliability and efficiency of silicon integrated RF cells. It also helps in reducing the effect of the parasitic capacitance at the input of the LNA due to MOSFET used in design. In this thesis inductive source degeneration inductor and series inductor was replaced by on-chip inductor technique.

1.5 Outline of the thesis

Chapter 1 is the background of the thesis. It also contains thesis problem and related factors to the thesis problem. **Chapter 2** contains LNA characterizations. It has a short description of different factors of LNA. On the basis of these factors we can judge the performance of the LNA. **Chapter 3** describe about different topology of the LNA. In this chapter all the topologies compared to each other on the basis of some parameters. **Chapter 4** has circuit implementations with off-chip and On-chip inductors. It contains the result of different parameters like input matching, gain, output matching, stability etc. at 17 GHz. **Chapter 5** has future implementations and conclusion of the thesis. In the next section it has the references used in this thesis.

1.6 TERMINOLOGY

IC	Integrated circuits
RF	Radio frequency
LNA	Low noise amplifier
IIP3	Input referred third order intermodulation intercept point
OIP3	Output referred third order intermodulation intercept point
CMOS	Complementary metal oxide semiconductor
RFIC	Radio frequency integrated circuits
ESD	Electrostatic discharge
f_T	Unity gain frequency
MIM	Metal-insulator-metal
IF	Intermediate Frequency
LPF	Low pass filter
SDF	Spectral Density Function
BPF	Band Pass Filter

2. LOW NOISE AMPLIFIER CHARACTERIZATION

2.1 Sensitivity

The sensitivity of an RF receiver is the minimum magnitude of input signal required to get a specified output signal having a specified SNR. In the other terms sensitivity represents as responsivity. Receiver sensitivity indicates that how faint an input signal can be to be successfully received by the receiver, so lower power level will be better. Sensitivity of the receiver is mainly determined by the LNA noise figure and power gain.

2.2 Noise Figure

The Noise performance of an RF amplifier is represented by its noise figure. The Noise figure is a measurement of the noise performance of a circuit. It is expressed in decibels.

$$NF = 10 \log_{10} F \quad (2.1)$$

$$F = (SNR_{in}/SNR_{out}) \quad (2.2)$$

Figure 2.1: Noise Figure of a System

Where SNR_{in} and SNR_{out} are the SNRs at the input and output of the amplifier respectively.

2.1.1 Noise Figure of Cascaded Stages

Noise figure for more than one stage shown in figure 2.2.

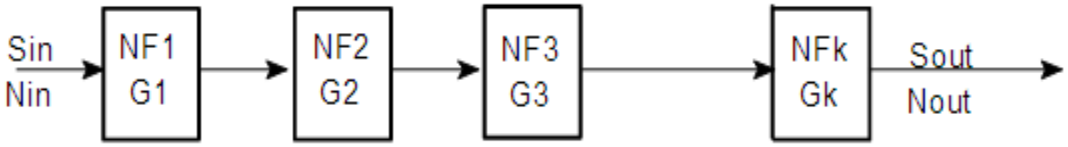

Figure 2.2: Cascaded Noisy Stages

For a cascade system of N stages, the overall noise factor can be obtained in terms of the noise factor and gain in each stage. Total noise factor for cascaded stages is given by Friis's formula.

$$F_{total} = F1 + \frac{F2-1}{G1} + \frac{F3-1}{G1G2} + \frac{F4-1}{G1G2G3} + \ldots\ldots + \frac{Fn-1}{G1G2\ldots.Gn-1} + \quad (2.3)$$

Where Fi and Gi are the noise factor and available power gain, respectively, of the i-th stage and n is the number of the stages.

2.3 S-Parameters

There are many ways to represent the behavior of a two-port network. At low frequency generally Z, Y, H and ABCD parameters are used. S-parameters play an important role in RF systems. Z-parameter and h-parameter is difficult to use in the RF-system. Short circuit and open circuit do not behave the same at radio frequencies because of inductance and capacitance present in a transmission line. S-parameters are the best way to measure incident and reflected wave power in a two-port network for RF block.

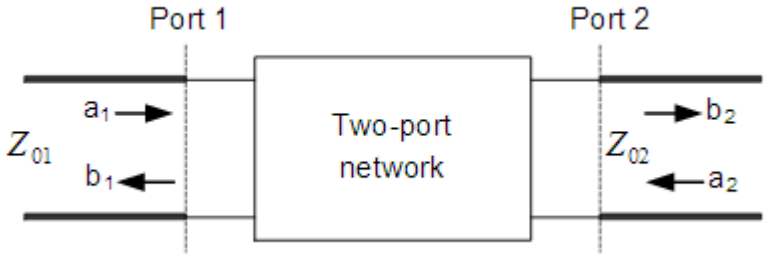

Figure 2.3: A two-port network

$S_{11} = \frac{b1}{a1}\Big|_{a2=0}$ = Input reflection coefficient with matched output port

$S_{12} = \frac{b1}{a2}\Big|_{a1=0}$ = Reverse transmission coefficient with matched input port

$S_{21} = \frac{b2}{a1}\Big|_{a2=0}$ = Forward transmission coefficient with matched output port

$S_{22} = \frac{b2}{a2}\Big|_{a1=0}$ = Output reflection coefficient with matched input port

For the LNA amplifier from design point of view, S_{11} and S_{22} denote the input and output impedances matching. S_{21} measures the amplification gain of the amplifier and S_{12} represents the isolation between input and output ports.

2.4 Stability

Stability is a major concern in RF amplifiers. It is obvious that an LNA may become an oscillator if it is unstable in the circuit performance. After circuit designing its stability should be examined by the designer. The degree of an amplifier's stability can be quantified by a so-called stability factor. The stability of a circuit is characterized by the stern stability factor given in equation 2.4 [4]

$$K = \frac{1 + |\Delta|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{11}||s_{22}|} \tag{2.4}$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \tag{2.5}$$

Other method to represent the stability factor is given by equation 2.6

$$B_{if} = 1 + |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2 \tag{2.6}$$

A circuit is unconditionally stable if K>1 anf B_{if} >0

The conditions for unconditionally stability for all the reflections coefficient are

$$|\Gamma_s| < 1$$

$$|\Gamma_L| < 1$$

$$|\Gamma_{in}| < 1$$

$$|\Gamma_{out}| < 1$$

In the recent year K and Δ repleced by μ factor which is defined by equation

$$\mu = \frac{1 - \text{Squareof}\,|S11|}{|S22 - \Delta\text{Conj}(S11)| + |S21 * S12|} \qquad (2.7)$$

2.5 Input and Output Impedance Matching

Impedance matching is an important aspect in RF circuits designing. Performance of RF circuits depends on the input and output matching. In order to maximize power transfer from source to load, matching impedances is required. If the load impedance is Z_L, then for maximum power transfer source impedance Z_S is equal to a conjugate of load impedance.

$$Z_S = Z_L^* \qquad (2.8)$$

The reflection coefficient Γ is a normalized measure of the relationship between source impedance and load impedance. Input and output impedance matching is given by the input and output return loss. Return loss (RL) is the relationship between the reflected power wave at a port to incident power wave at the same port and it's defined in equation 2.9,2.10 and 2.11. A perfect match will have no reflection and an SWR of 1.

$$\Gamma = \frac{Zl - Zo}{Zl + Zo} \qquad (2.9)$$

$$20 \log \Gamma_{in} = 20 \log |S_{11}| \quad (2.10)$$

$$20 \log \Gamma_{out} = 20 \log |S_{22}| \quad (2.11)$$

2.6 Quality factor

Quality factor (Q) is a parameter of the rate of energy loss in complete network or in individual inductor or capacitor. We can define the quality factor on the basis of two factors. One is damping performance of the circuit; means of Q become larger, the resonator becomes less damped. Other one depends on the ratio of frequency to the bandwidth of the resonator.

$$Q=\frac{fr}{\Delta f} \quad (2.12)$$

Where fr is the resonant frequency and Δf is the bandwidth.

Other Common definition of Q is given in equation 2.13

$$Q=2\pi*\frac{Energy\ stored}{Energy\ dissipated\ per\ cycle} \quad (2.13)$$

$$Q_L=\frac{Xl}{R}=\frac{wL}{R} \quad (2.14)$$

$$Q_c=\frac{Xc}{R}=\frac{1}{WRC} \quad (2.15)$$

2.7 Linearity

Linearity is most important design point along with noise, gain and impedance matching. Active RF devices can be nonlinear in operation, due to nonlinearities, intermodulation distortion, desensitization, blocking and cross modulation occur in the system. The output of the nonlinear system contains several harmonics of the input signal which are integral multiple of input frequency.[2]

Input is given in equation 2.16

$$x(t)=A\sin\omega t \tag{2.16}$$

If x(t) applied to nonlinear system then output in given in equation 2.17

$$y(t)= \beta_1 A\sin\omega t+ \beta_2 A^2 \sin^2\omega t+ \beta_3 A^3 \sin^3\omega t+.... \tag{2.17}$$

The term with the input frequency is called fundamental component and the higher terms called harmonics components in the output.

There are two important factors to measure the linearity in RF circuit design.

2.7.1 1-DB Compression point

Gain reduction due to the nonlinearity of the transfer function of the amplifying device is called gain compression. The 1-dB compression point is the one of the technique to measure gain compression. It is defined as the input signal level for which the gain of the amplifier drops by 1-dB. By the help of 1-dB compression point we can calculate the maximum input range of our design.[4]

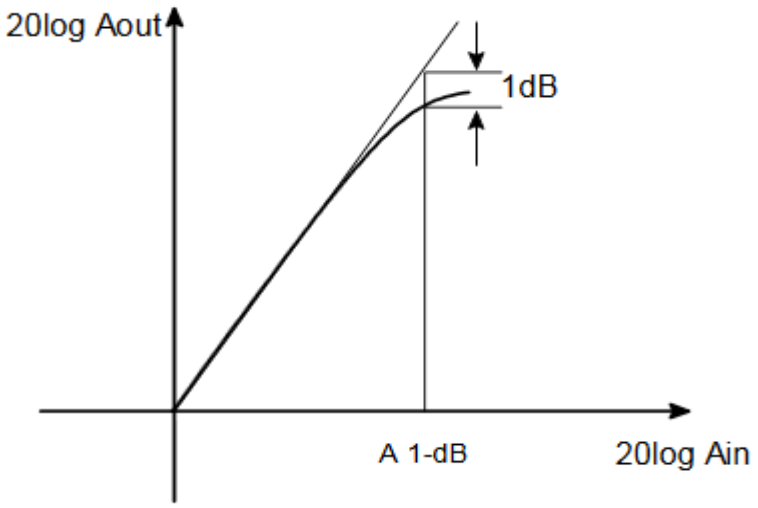

Figure 2.4: 1-dB Compression Point

2.7.2 Third Order Intercept Point

The Third order intercept point is the measure for nonlinear system. It indicates that how well a receiver performs with the distortion. It's based on nonlinearity which derived from Taylor series expansion. It relates to the third order nonlinear term generated to the linear amplified signal. The intersection of the line of the fundamental first order output and 3rd order intermodulation product is called the third intercept point.[3]

$$\frac{A(1-dB)}{A(IP3)} \cong 9.6 \text{ dB} \qquad (2.18)$$

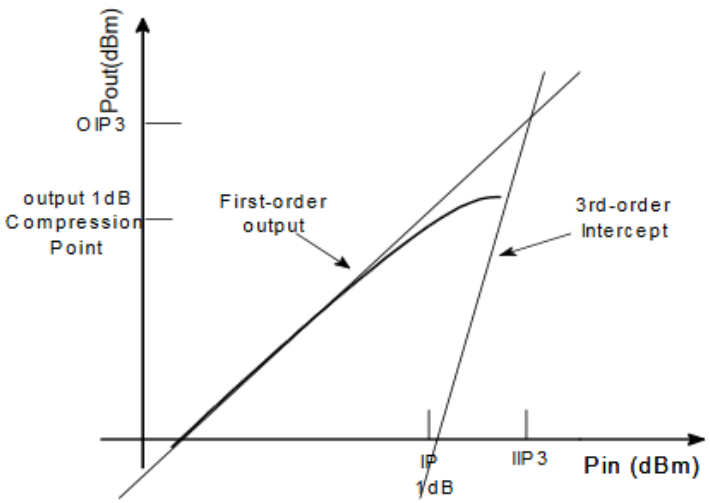

Figure 2.5: Third Order Intercept Point

3. LNA DESIGN

3.1 Popular LNA topologies in CMOS technology

In the LNA designs usually involves one or two transistors so that we can achieve low noise at the output. CMOS technologies are the best way to design LNA. They provide high speed operation, simplicity in fabrication and also low power consumption. Frequency of operation depends on different parameters like size of the transistors, impedance values connected to the transistors, etc. Operating frequency also depends on the filter connected to the input of the LNA.

The most important parameter in the designing of the LNA is impedance matching technique. Different LNA structures have different methods to achieve impedance matching.

The structure shown in Figure 3.1 gets input impedance by directly putting a 50 Ω resistor (Rs) in parallel with the gate of transistor M1. In this case noise figure will be very high. The minimum noise figure for this structure given in equation 3.1 [9]

$$F >= 2 + (4\gamma/\alpha g_m R_s) \quad (3.1)$$

Where α is the drain source conductance and γ is a constant value of 0.66. After these values noise figure is readily larger than 6 dB In this topology main contribution of noise is termination resistor Rs. Because of the high noise figure, this topology is rarely used. [9]

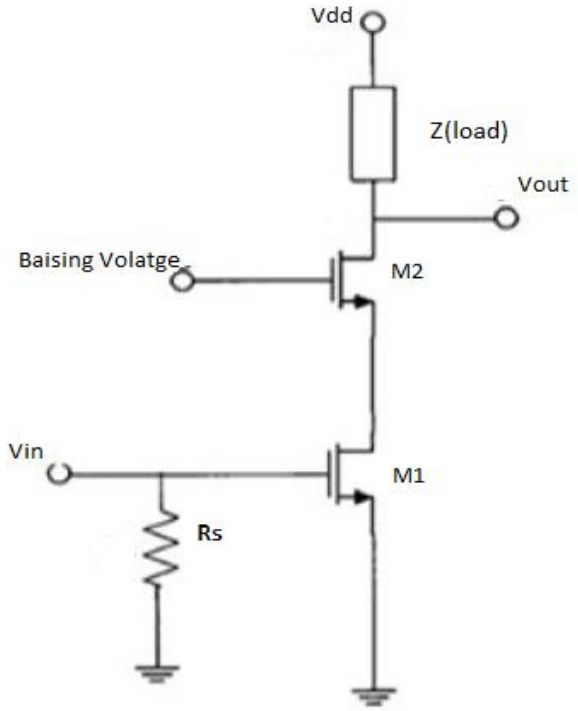

Figure 3.1: Resistive terminated LNA

In Figure 3.2, common gate amplifier structure has better input impedance as compared to the common source structure. Due to this high input impedance input matching will be easier in this topology. Noise factor F>=1+γ/α . The minimum noise factor for this device is 5 dB. The primary reason for the high noise factor is gate current. [9]

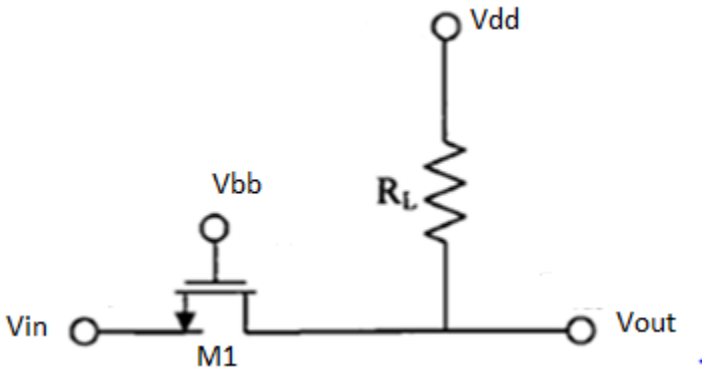

Figure 3.2: Common Gate LNA

In figure 3.3, LNA uses negative shunt feedback to modify the input impedance of a common source stage. Due to this property we can get matching in large range. Its input impedance depends on the voltage gain of the amplifier given in the equation 3.2 [9]

$$Z_{in} = R_F/(1+A) \quad (3.2)$$

Where A is the voltage gain which is approximately equal to R_l/R_1. And RF is the feedback resistor.

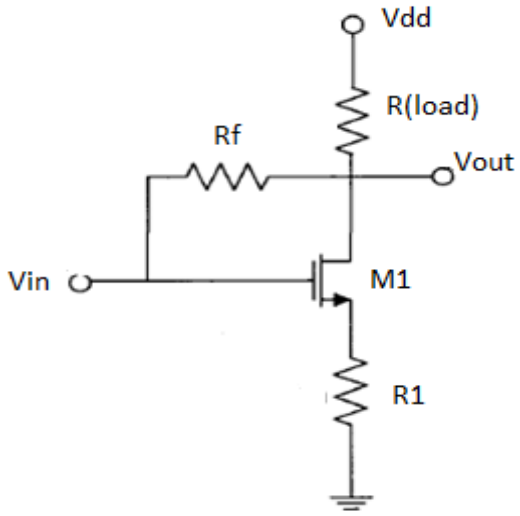

Figure 3.3: Shunt series feedback LNA

The Noise figure for shunt series LNA topology is better than as compare to above topologies. But because of feedback stability issues occurs in this topology. This type of LNA used in wide band receiver. Noise occurs in this topology because of gate current.[9]

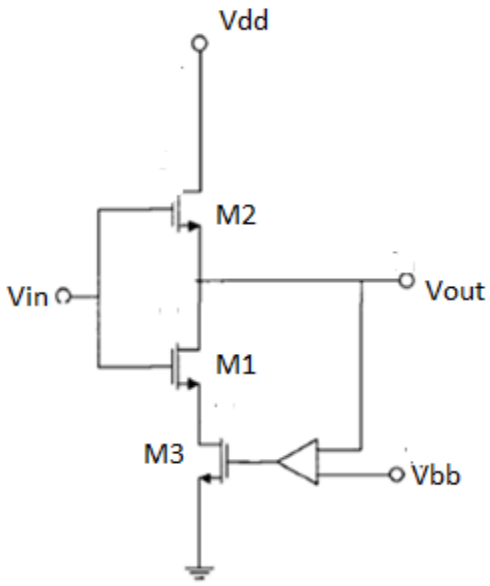

Figure 3.4: Current Reuse LNA

Generally CMOS transistors have low transconductance because of this design have low gain. So by the use of current reuse we increase the transconductance. Figure 3.4 shows a current reuse LNA. Effective transconductance in this topology is gm1+gm2. Gain of the system directly proportional to transconductance of the CMOS transistors. The Gain of this topology is better than as compare to other topologies. But major disadvantage of this topology is its high input and output impedance. So this requiring external impedance matching circuit to get the impedance matching. In this topology, two identical stages are cascaded to improve the reverse isolation.[9]

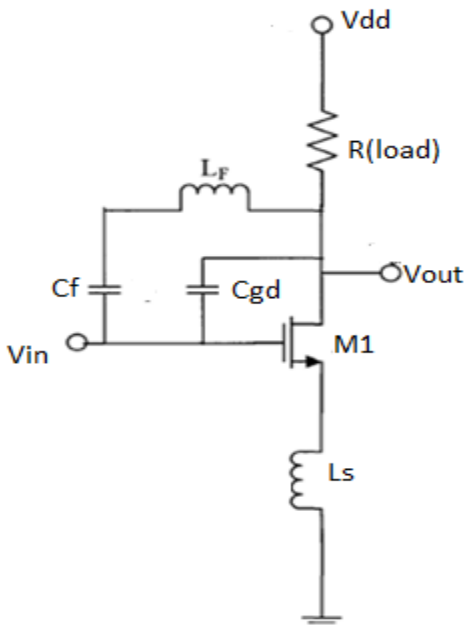

Figure 3.5: Inductor Neutralization LNA

By the help of LNA neutralization technique, we can improve reverse isolation of LNA. An inductor Lf is added in parallel with this capacitor to provide a different feedback polarity to cancel the effect of C_{gd}. This will provide good reverse isolation at the output. But because of this C_{gd}, stability issue occurs in this LNA design. The LNA neutralization technique shown in figure 3.5. Because of these extra components (inductors and capacitors) added in this design, area is larger as compare to the other topologies. [9]

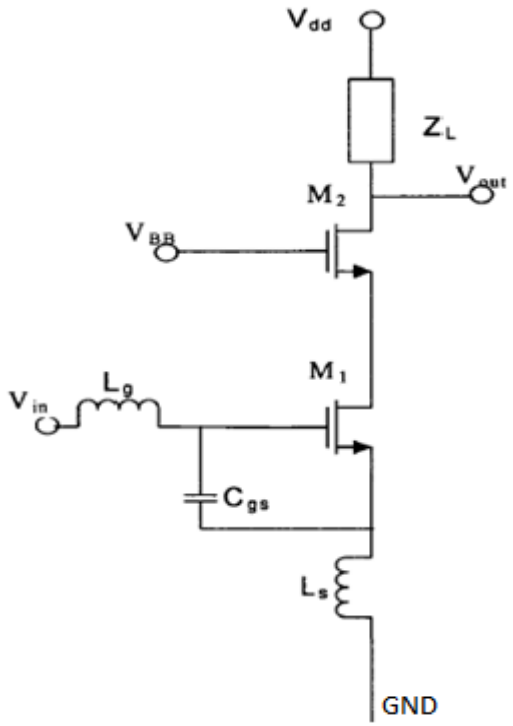

Figure 3.6: Inductive Source degeneration LNA

Inductive source degeneration LNA technique used in this thesis for LNA designing. There are two transistors used in this topology, one is M1, is in the common source mode and M2 is in the common gate mode. By the help of cascade technique, topology gets high input impedance. Inductor L_s provides negative feedback to the amplifier and because of this negative feedback gain is stabilized. By the help of cascade technique, we can get a narrow band match. Inductive source degeneration LNA has a low noise figure. But because of extra components (inductors and capacitors) used in this LNA, area will be more on this topology.[4]

Table 3.1 compares all the topologies discussed above [9]. It contains, plus and minus point of all the topologies discussed before.

Table 3.1: Comparison between different topologies

Topology	Advantages	Disadvantages
Resistive termination	Good input match	Large NF
Common gate	Better input match	High NF
Series shunt feedback	Broad band i/o match	Not stable
Inductive degeneration	Good matching in narrowband	Large area
Current reuse	High gain	External matching required
Inductor neutralization	Good output matching	Stability issue

4. CIRCUIT IMPLEMENTATION

4.1 Previous Work

The first transmission and reception of electromagnetic waves was conducted by Henrich Hertz in 1887. The K_u frequency band (12GHz to 18 GHz) is widely being used in radar systems. This standard is the most used standards in modern communication systems and there is a great need for transceivers capable of working with this frequency standard. CMOS and Silicon Germanium are the main processes to implement RF circuits. Low power consumption and easy availability were the main reasons to choose the CMOS process for this thesis. The low noise amplifier is designed in 0.35um thick metal CMOS process by austria microsystems (C35B4M3). In this thesis we will discuss some previously designed LNAs and then the new design strategy for tunable LNA will be presented. BSIM 0.09 um CMOS technology was selected to design the LNA. BSIM 0.09 um CMOS technology consists of 6 metal layers and 1 poly-silicon layer which is designed for high speed low voltage applications. Metal 6 is the outer most of all the layers, and it is used for laying out the inductors.

4.2 Inductive Source Degeneration LNA Design with Filter

Inductive Source Degeneration LNA schematic shown in figure 4.1. Ku band limit is from 12 to 18 GHz. For this we have to design our filter in this range. A Chebyshev filter is used to achieve this range of frequencies. The Chebyshev filter contains L_1, C_1, L_2, and C2. The values of these are selected correctly so that it achieves resonance in K_u Band.

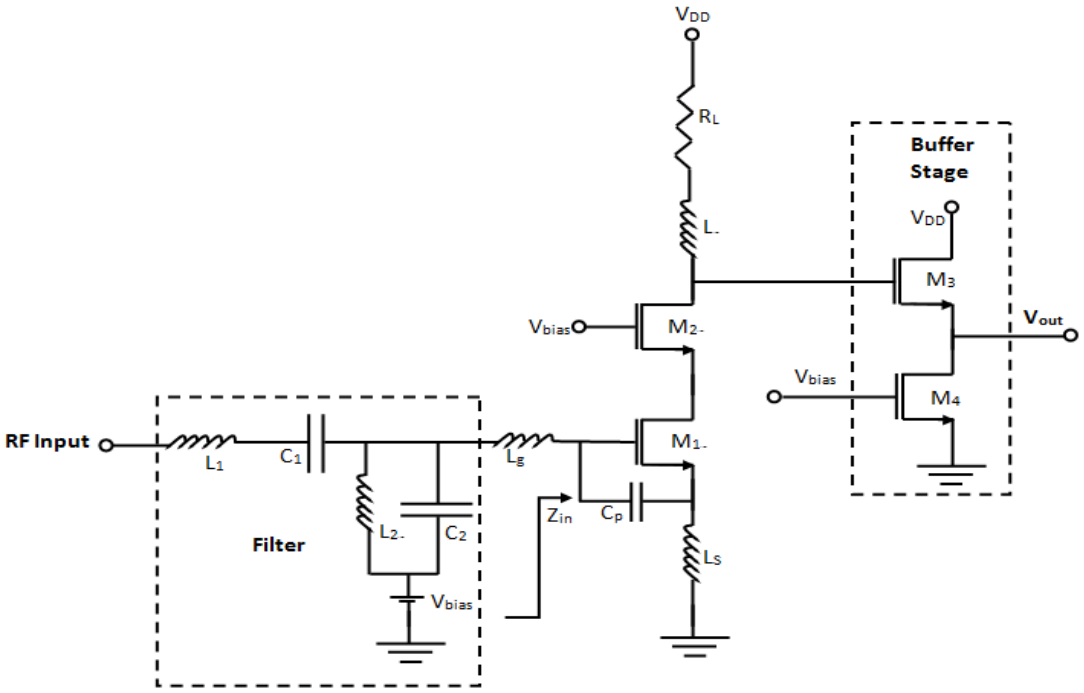

Figure 4.1: Inductive source degeneration LNA

The basic structure of a cascaded input transistor shown in figure 4.1. Where Transistor M1 acts as input transistor and M2 is the cascade transistor. The Cascade transistor is added for the isolation purpose. Cascade transistor reduces the effect of the drain- gate capacitance of the input transistor, which acts as a miller capacitance. Inductor L_s behaves like a bond wire as an on-chip ground line and off chip ground plate. Other two inductors used to tune the frequency of LNA. C_{gs} represents the parasitic gate source capacitance of transistor M_1. For the matching, source impedance should be equal to the input impedance of the design.

The CB or CG configuration of the second stage guarantees isolation between input and output. In a cascade amplifier, input stage amplified the current, and voltage is amplified in the cascade stage. Consequently, the voltage and power of the signal can be magnified, Therefore, satisfying both digital and RF circuit designer.

4.2.1 Input Match Analysis

Impedance matching is a core technology in RF circuit design. As seen in the figure 4.2, the input impedance of transistor M1 is a series with an LC circuit given by equation 4.1. The noise performance of the design sample is good after impedance matching is done.[6]

$$Z_{in} = \frac{V}{I}$$

$$Z_{in} = j(\omega(Ls+Lg) - \frac{1}{wCgs}) + \frac{gmLs}{Cgs} \quad (4.1)$$

$$\omega_T = \frac{gm}{Cgs} \quad (4.2)$$

Where ω_T is a unity current gain magnitude frequency. The value of ω_T should be high so that system has good gain and low noise figure. ω_T increases with the increase in current through the circuit. Imaginary part of impedance cancels at resonance frequency and by the help of real part of impedance function; input matching is achieved.

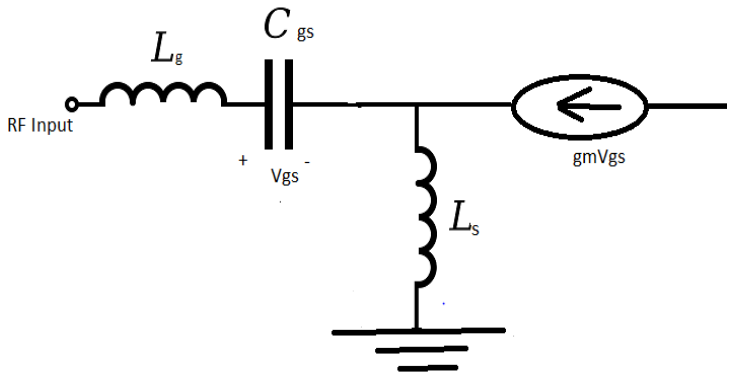

Figure 4.2 : Input equivalent of a modified raw device

By equating imaginary part of Z_{in} to zero at resonance frequency, we get the equation 4.3

$$\text{Img}(Z_{in}) = (\omega(Ls+Lg) - \frac{1}{wCgs})$$

$$\omega_{op} = \frac{1}{\sqrt{((Ls+Lg)Cgs)}} \quad (4.3)$$

Real part of Zin is equal to source impedance (generally it is equal to 50Ω)

$$\text{Real } (Z_{in}) = \text{Source Impedance} = \frac{gmLs}{Cgs} \quad (4.4)$$

4.2.2 Gain

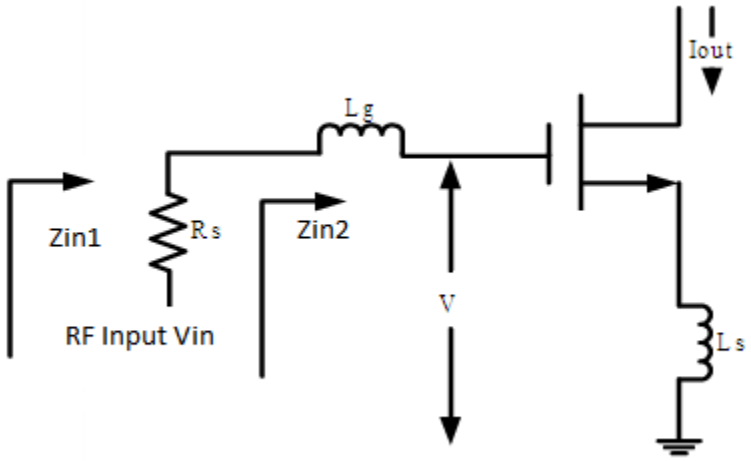

Figure 4.3: Inductive Degeneration LNA Gain Stage

Inductive Degeneration LNA Gain Stage is shown in figure 4.3.

$$V = V_{gs} + g_m * Vgs * s * Ls \quad (4.5)$$

$$Vgs = \frac{V}{1 + gm * s * Ls} \quad (4.6)$$

$$V = \frac{Zin2}{Zin1} * V_{in} \quad (4.7)$$

Where $Z_{in}2$ is defined in equation 4.1.

$$Z_{in}1 = Rs + Z_{in}2 \quad (4.8)$$

Output current is defined in equation 4.9 and 4.10. [4]

$$I_{out} = g_m * V_{gs} \quad (4.9)$$

$$I_{out} = \frac{gm}{1 + gm * s * Ls} * V \quad (4.10)$$

After putting value of V, Zin1 and Zin2 in equation 4.10 and solving for the stage transconductance gain gives

$$G_m = \frac{Iout}{Vin} \quad (4.11)$$

$$G_m = \frac{wt}{2 * s * Rs} \quad (4.12)$$

Transconductance gain of the stage is not dependent on g_m of input transistor. It depends on the unity current gain frequency f_t.

4.2.3 Noise Figure

There are two noise sources in the input, tunable inductor and input transistor. The noise of the inductor can be reduced by improving Q of the inductor. Off chip inductor (Lg) have high Q as compared to the on-chip inductor (Ls). Ls add significant noise figure in the design. Input transistor has thermal noise of its drain and gate. Mathematical formula of noise figure is defined in equation 4.13[10]

$$F=1+\frac{2w\,Ls}{3*Q*Rs}+\frac{1}{15*gm*Rs}*\left(1+\frac{1}{Square\ of\ Q}\right) \quad (4.13)$$

Where Q is defined in equation 4.14

$$Q=\frac{1}{gm1*w*Ls} \quad (4.14)$$

4.3 Band Pass Filter for Ku band

Chebyshev filter is used for realizing band pass filter in K_u band. Impedance of the filter should be match to the source impedance.

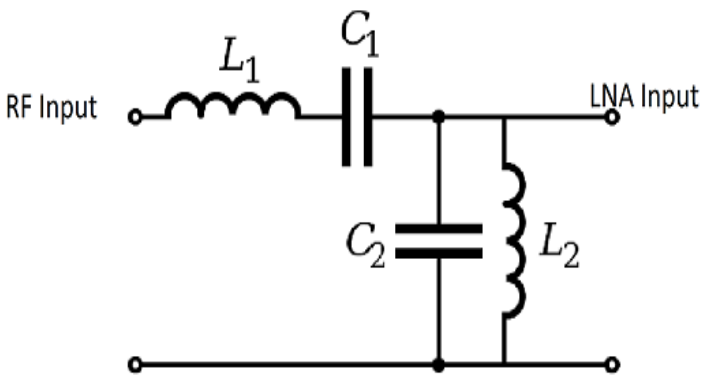

Figure 4.4: Chebyshev Band-Pass Filter

Table 4.1 Values of components of Band pass filter

Component	Value
L1	1.34 nH
C1	69.5 fF
L2	0.92 nH
C2	113.6 fF

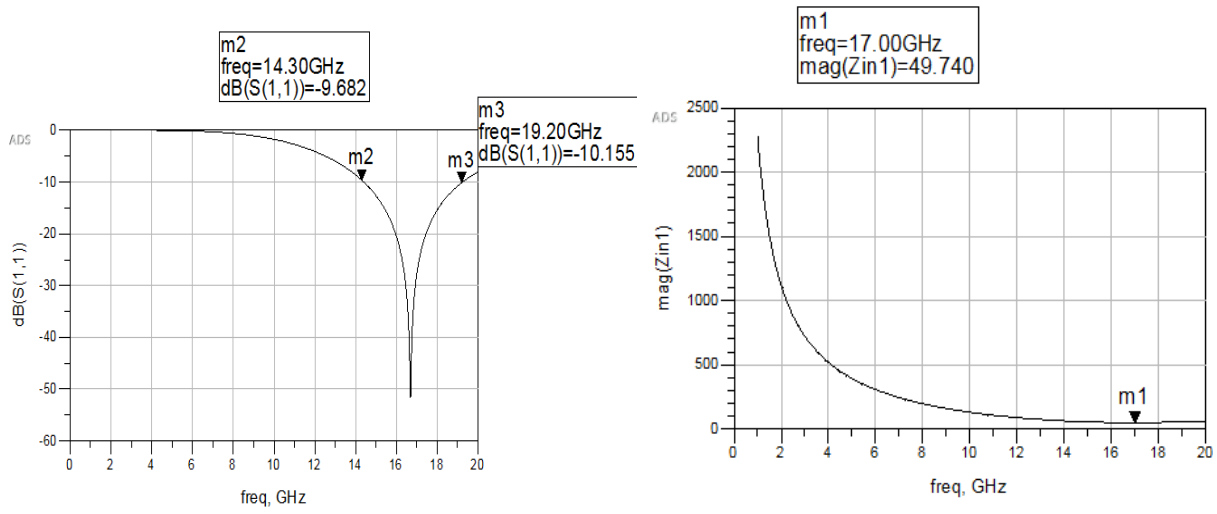

Figure 4.5 : Bandwidth and Impedance of band pass filter in Ku Band

Bandwidth of band-pass filter is around 5GHz (from 14.30 GHz to 19.30 GHz) in K_u band. Chebyshev filters minimize the error between the idealized and actual filter characteristic over the range of the filter. Chebyshev filters are sharper than the other filters. They show fewer ripples over the bandwidth.

4.4 LNA Implementation with Off-Chip (General) Inductor at 17 GHz

In this thesis LNA implemented at 17 GHz (K_u Band) using the ADS software. 17 GHz is the design frequency for this thesis. The Chebyshev band-pass filter used in this design has pass-band from 14 GHz to 19 GHz. The circuit implemented in ADS shown in figure 4.6. Buffer stage use of the output of cascade amplifier, So that the design has good output matching. Components values used for this design in table 4.2.

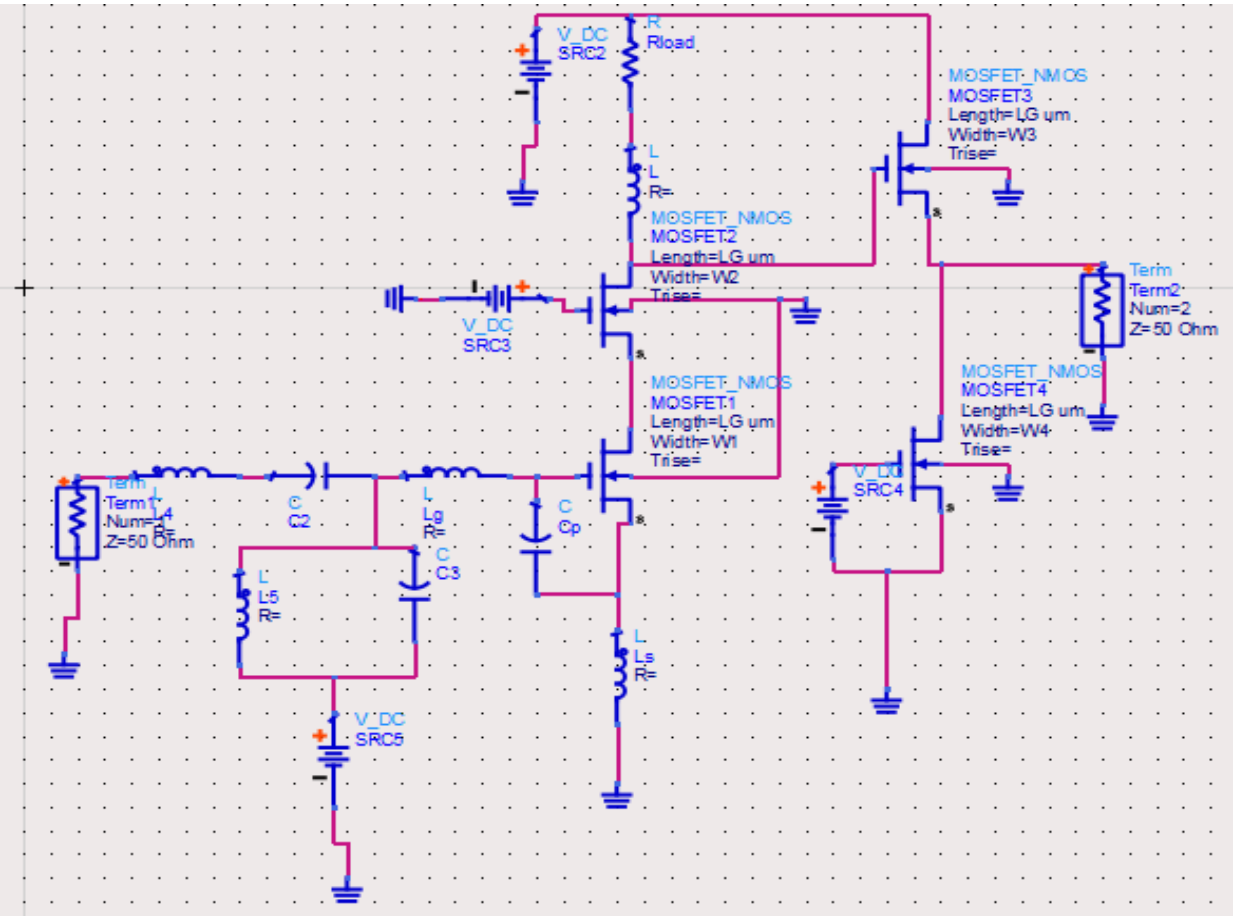

Figure 4.6: Inductive Source Degeneration LNA ADS Schematic for 17 GHz

ADS Software has the tuning property. After calculation from equations mentioned before, and using the property of tuner in ADS we get the values mentioned in table 4.2.

Table 4.2 Values of components for LNA at 17 GHz

Component	Value
Lg	864 pH
Ls	12 pH
Cp	30.98 fF
L1,L2,L3,L4	0.09 um
W1	80.16 um
W2	52.31um
W3	28.23um
W4	57.95 um
L	614.66 pH
R_L	6 Ω
V_{dd}	2.2 V
Vbias(Input Transistor)	816.5 mV
Vbias(Cascade Transistor)	1.1 V
Vbias(Buffer Stage)	545.23 mV

4.4.1 Results

Result of input matching is shown in the figure 4.7. At 17 GHz, the value of S_{11} is equal to 47.25 dB. Bandwidth is nearly equal to 1GHz. The quality factor is equal to 17 (as given in equation 2.12) so that this design comes from the narrow band region. The gain of the circuit is equal to 19.4 dB at the operating frequency. Noise Figure of the system is 2.7 dB at 17 GHz.

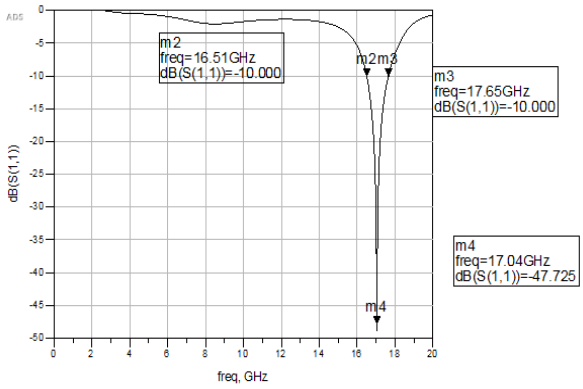

Figure 4.7: Input Matching of the LNA

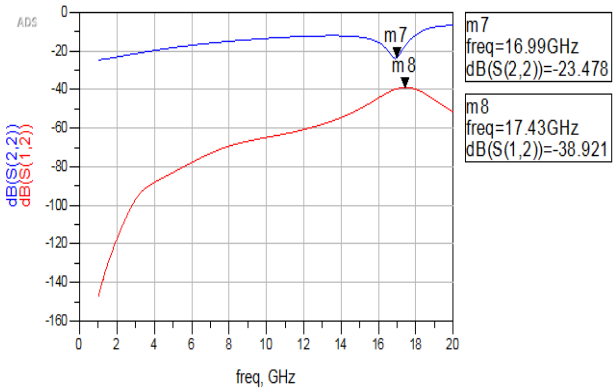

Figure 4.8: Reverse Isolation and Output Matching of the LNA

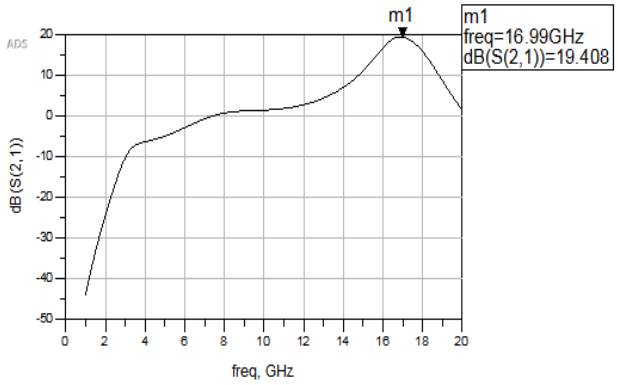

Figure 4.9: Gain of the LNA

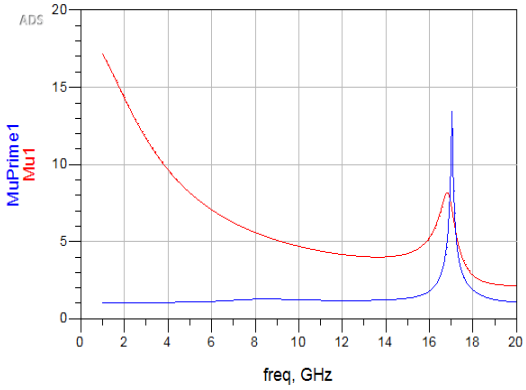

Figure 4.10: μ Factor (Stability Factor) for Load and Source

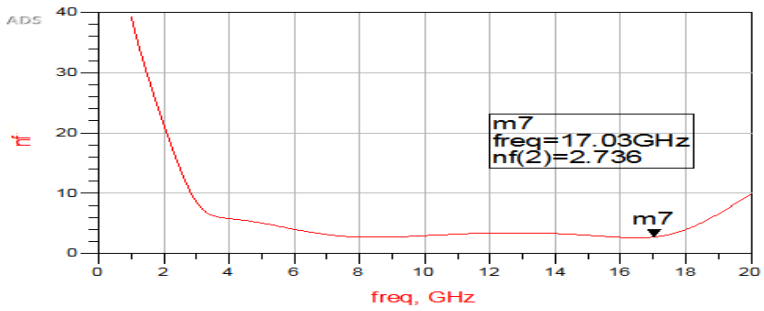

Figure 4.11: Noise Figure of the system at 17 GHz

4.5 On-Chip Inductor

In ADS On-Chip inductor is made with the micro-strip line. Parameters used in the on-chip inductor given in table 4.3. For designing the inductor, first of all, the resonant frequency is decided. The resonant frequency of the inductor is dependent on the value of inductor, f_t(unity gain bandwidth) of the system. General inductor impedance characteristic shown in figure 4.12. Figure 4.12 shows that over 31 GHz (resonate frequency), Impedance will be negative. Inductor starts behaving like a capacitor.

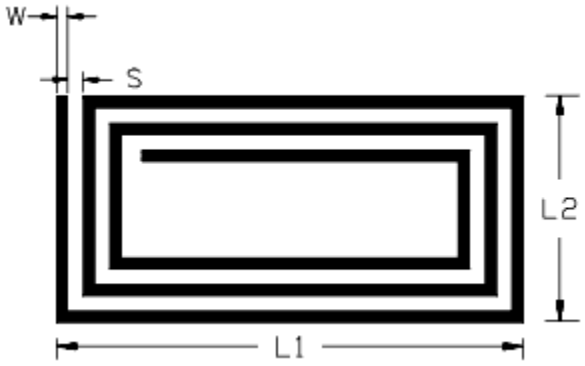

Figure 4.12: On-Chip Inductor

Table 4.3: Parameters of On-Chip Inductor

Name	Description
Subst	Substrate instance name
N	Number of turn
L1=dout	Length of second outer most segment
L2=din	Length of outmost segment
W	Conductor Width
S	Conductor spacing

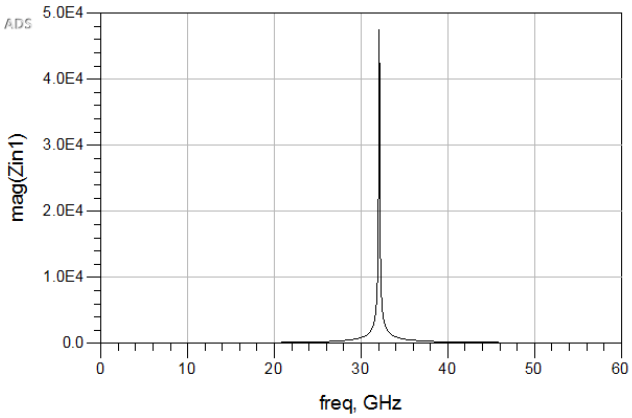

Figure 4.13: Inductor Properties over Frequency

$$L=0.5*\mu o*n^2*d_{avg}*C_1*[\ln(C1/\rho)+C_2+C_4\rho^2] \quad (4.15)$$

Where μo is the permeability of air, n is the number of turns, d_{avg} is the average diameters of outer (d_{out}) and inner turns(d_{in}) , p is the fill factor defined as p= (d_{out}-d_{in})/ (d_{out}+ d_{in}). The coefficients C_1, C_2, C_3 and C4 are given as 1.27, 2.07, 0.18, 0.13 respectively for the square spiral inductor.[5]

The design procedure is: [5]

- Find the value of L use in the design
- Choose a value for p <1
- Calculate the d_{avg} using equation
- Determine d_{out} and d_{in}
- Choose a constant value for s.

4.6 LNA Implementation with On-Chip Inductor at 17 GHz

The inductor present in the previous design is replaced by the on-chip inductor. Inductor is made from rectangular spiral microstrip transmission line. Each segment of the spiral is modeled as a lumped C-L-C π-section with mutual inductive coupling to all other parallel segments including those of an image spiral. The image spiral accounts for the effects of the microstrip ground plane. The inductive calculations include the end-effects and differing lengths of coupled segments. The capacitive components account for capacitance to ground, coupling to the parallel adjacent segments, and the coupling to the next parallel segments beyond the adjacent on both sides. [7]

The frequency dependence of the skin effect is included in the conductor loss calculation. A smooth transition is provided from dc resistance to resistance due to skin effect at high frequencies. Dielectric loss is also included in the loss calculation. In layout, the number of turns is rounded to the nearest quarter-turn.[8] The connection will align at the inside edge at pin 1 and the outside edge at pin 2, unless W1 (width of the line that connects to pin 1) < W or WB (width of the line that connects to pin 2) > W, in which case the conductors are centered.

As the value of inductor increases, L1 and L2 increase for constant no of turns. The width of the all the transistor doesn't not change in this design as compared to the designed before. Parameters of on-chip inductors are decided by equation 4.15. On the time of calculating the values of parameters of on-chip inductor, we should care about minimum PCB fabrication parameters.

Inductive source degeneration LNA schematic shown in figure 4.14. It replaces the inductive source degeneration inductor, series inductor and load inductor with the on-chip inductor. The resonance frequency of the on-chip inductor is decide as according to the value of the general inductor in this location.

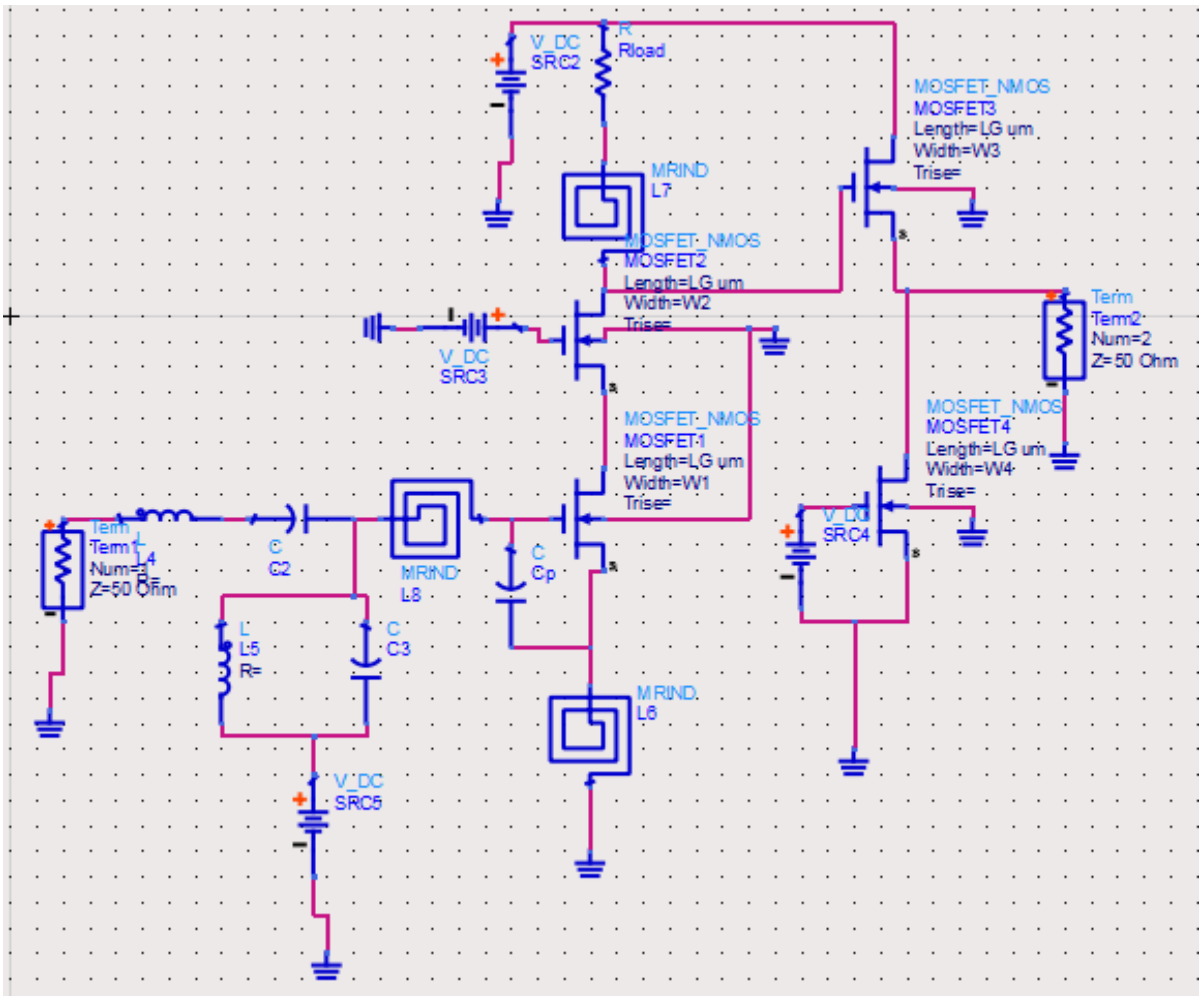

Figure 4.14: Inductive Source Degeneration LNA ADS Schematic with on-Chip inductor for 17 GHz

Table 4-4: Value of On Chip Inductor Parameters

L_6 (L_s)

Parameter	Value
N	2
L1	0.98 mm
L2	0.94 mm
W	0.14 mm
S	0.08 mm

L_7 (L_{load})

Parameter	Value
N	2
L1	0.84 mm
L2	0.76 mm
W	0.16 mm
S	0.08 mm

L_8 (L_g)

Parameter	Value
N	2
L1	0.80 mm
L2	0.76 mm
W	0.15 mm
S	0.08 mm

Quality factor of inductor is given in equation 2.14. The quality factor of inductor Lg is 15, Inductor Lg is 190 and load inductor is 130. No of turns for the on-chip inductors is taken as constant 2

4.6.1 Results

Input matching, gain, noise figure, output matching and stability results for the design given above are shown in figure 4.15 to 4.19. As seen in figure 4.15 to 4.19, the results of all these parameters are improved using on-chip inductors. The value of S_{11} is -51 dB. Output matching and reverse isolation also improve using on-chip inductors. Gain of LNA increases by 2 dB and it becomes 21 dB. The noise figure of the LNA also improved and it becomes 2.6 dB. Unity gain bandwidth of the LNA is around 21 GHz.

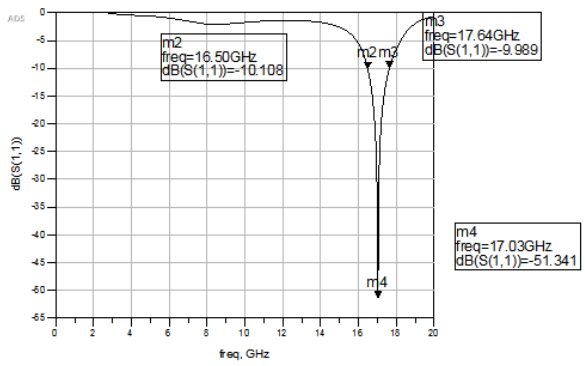

Figure 4.15: Input Matching of the LNA

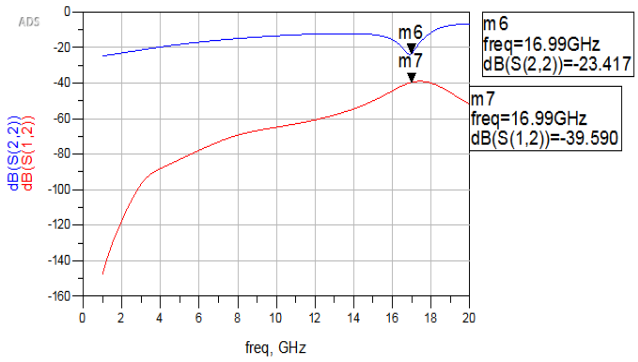

Figure 4.16: Reverse Isolation and Output Matching of the LNA

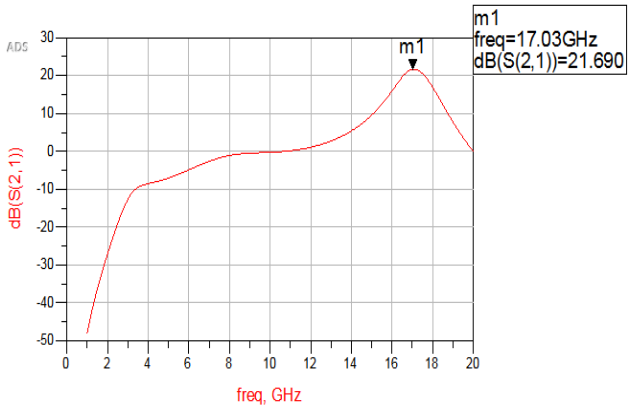

Figure 4.17: Gain of the LNA

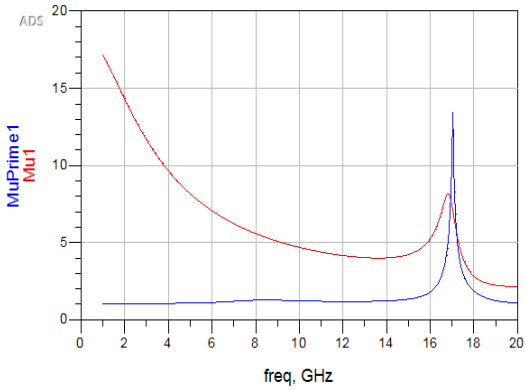

Figure 4.18: μ Factor (Stability Factor) for Load and Source

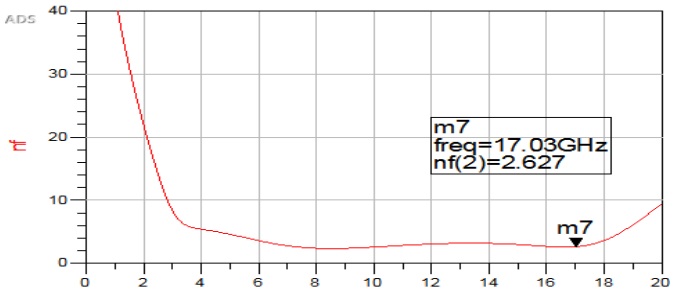

Figure 4.19: Noise Figure of the system at 17 GHz

5. FUTURE AND CONCULSION

Due to the high potential of this work, here we propose several future works to be done. Firstly, while we have covered and explored deeply on the topic of LNA, other important blocks such as filter, on-chip inductor. In the future, significantly power consumption can be saved by further exploring the performance trade-offs in K_u Band. Secondly, while bringing in benefit such as higher level of integration and higher, technology scaling also creates many issues for RFIC designer. In this thesis a new input matching topology for tunable narrowband LNAs has been discussed and a fully differential tunable LNA has been designed in 0.09um technology. The design has been validated through ADS RF simulation tool. The simulations show good results for the frequency 17 GHz. The tunability to frequencies in between 14 GHz and 19 GHz is limited due to sharp change in varactor capacitance from the accumulation to depletion mode.

However at 17 GHz the LNA provides stable operation with varactors operating fully in accumulation and depletion modes respectively. At low supply voltage, it is very challenging for critical blocks such as mixer and baseband circuits to achieve sufficient linearity. Since narrowband LNAs are suitable for low Q inductors, custom made inductor like on-chip inductor models should be explored. By reducing the area occupied by the inductors, we can increase the number of on-chip inductors without increasing the size of the implemented circuit. With custom made inductor models we can investigate other architectures, like the distributed amplifier and expand input matching networks for improved match, solutions which were turned down in this project.

6. REFERENCES

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