High Efficiency Fully Integrated PLL based Low-Dropout Voltage Regulator

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Certificate

This is to certify that the thesis titled **"High Efficiency fully-integrated PLL-based Low-Dropout voltage regulator."** submitted by **Ankush Singh** for the partial fulfillment of the requirements for the degree of *Master of Technology* in *VLSI & Embedded Systems* is a record of the bonafide work carried out by him under my guidance and supervision in the Security and Privacy group at Indraprastha Institute of Information Technology, Delhi. This work has not been submitted anywhere else for the reward of any other degree.

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Abstract

Low Dropout Regulators (LDOs) are extensively used in many applications ranging from high power system to the portable application like mobile phones, PDAs and notebooks. These portable applications demand high power efficiency and low output voltage ripple which is responsible for long battery life. The output voltage of a conventional DC/DC converter (generally switched mode) has considerable ripple which feeds as input to these LDOs. And the challenge is to suppress these ripples for wide range of frequencies (for radio units) to provide clean supply. These low dropout regulators (LDOs) typically requires output capacitors ranging from 1μF to 10μF. The necessity of output capacitors occupies valuable board space and can add additional integrated circuit (IC) pin count. A high IC pin count can restrict LDOs for system-on-chip (SoC) solutions.

Several topologies are presented in order to compose a capacitor-less LDO regulator. In this thesis a new capacitor-less LDO which has integrator based architecture with digitally controlled loop is proposed which regulates the voltage on the principle of PLL. This PLL based voltage regulator is fully integrated on-chip and is stabilized under different load conditions which gives the user an option with regard to the external capacitor. Hence, the LDO presented here is ideal for any application, whether it be for a SoC solution or stand-alone LDO. The proposed capacitor-less fully integrated LDO is designed using 28nm FDSOI technology.

The integrator based LDO architecture based on the phase locked loop principle provide a stable output response from 0μA to 20mA with output capacitors in the range of 0 – 1 μF.This architecture provides higher efficiency, better load and line regulation at very low input voltage than the conventional op-amp based architecture. A 1V, 20mA fully integrated on chip LDO consumes 80μA of quiescent current with a dropout voltage of 200mV. This architecture appears to be robust to the process variations and the load conditions. Experimental results confirm a load regulation of 36uV/mA. Therefore, the proposed LDO is ideal for any application with a maximum supply rail of 1.2V and requiring the load current up to 20mA. The load transients show transient glitches at the output which are less than 300 mV independent of output capacitance.Thus, the presented PLL-based LDO voltage regulator is designed for system-on-chip (SoC) solutions.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

In the recent years, the world has seen a huge boom in portable electronic products like cell phones, tablets, etc. This evolution is especially noticed in mobile devices like cellular phones, PDAs, MP3 players, GPS etc. Evolution of the technology in terms of miniaturization and increase in the complexity of circuits bring a new challenge of the autonomy of the gadget. As a result, lots of recent researches have been researched across the world in battery's power supply noise management field to improve power consumption and also to reduce the cost of integrated chips. In these handheld devices, the battery supplies to the switching converter such as a buck converter that steps down the battery supply voltage to wanted lower output voltage with small ripples at its switching frequency. The ripples affects critical performance factor on the application hence voltage supply free of noise is required to power up the internal blocks of each device, many of them noise-sensitive, and to provide increased processing power and functionality for a longer period of time. [7] Therefore, a linear regulator is added right before the load block to remove the ripples as shown in Fig1.1.The most common way to isolate the ripples in the voltage supply is by the use of several independent linear regulators.

Voltage regulators are electronic circuits capable of maintaining a steady voltage at their terminals despite battery, temperature and load conditions. Although there are several voltage regulators available in the industry, the focus of this work will be in PLL based high efficiency Low Dropout regulator which is fully integrated with SoC as it does not require any external capacitor. Conventional op-amp based voltage regulator is sensi-

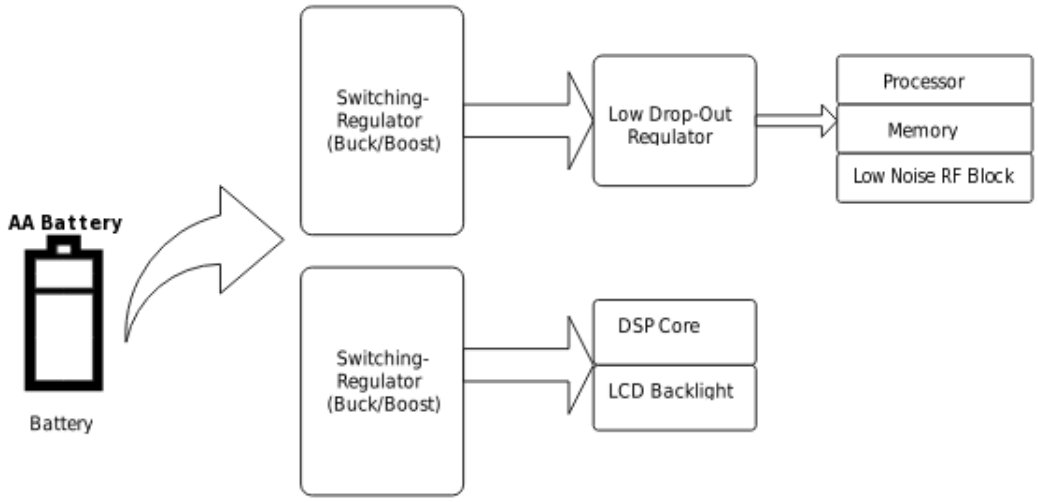

Figure 1.1: Flow of power supply in SoC

tive to the process, voltage and temperature variation as well as it is very sensitive to noise. Proposed voltage regulation technique using digitally controlled loop gives us the advantage over above mentioned problems faced by the conventional op-amp based voltage regulator. Several other architecture have been proposed for the improvements in the LDO regulation characteristic are mostly based on the opamp which have the finite DC gain. This integrator based LDO provides high performance because it can provide the infinite DC gain leads to zero steady state error.

1.2 Organization

The present thesis is organized as follows: In Chapter 2 characterization of conventional LDO regulator, its performance parameter in each analysis is discussed.Also,the fundamental properties of LDO regulators, design parameters and challenges faced in designing are discussed in this chapter.In Chapter 3 the theoretical macro-model of the design is presented as a starting point. Detailed analysis of topologies for each block and various other design constraints for realization of LDO are examined in the Chapter 3.Chapter 4 describes the circuit level designing and implementation of each component in the design. Chapter 5 presents the performance evaluation of the final design based on simulations. Both Transistor level Simulation result from cadence as well as behavioral simulation

from MATLAB is analyzed. Chapter 6 summarizes all the work done, comparison with the previous work with all the options taken into account. The main features of the design are also presented. Finally, for future works, a brief reference to relevant research is presented.

Chapter 2

Low Dropout Regulator

2.1 Conventional LDO Topology

LDO voltage regulators fall into the class of linear voltage regulators. The operation and objectives of this class remain the same, so LDOs, like any other voltage regulator, must provide a steady and clean voltage at their terminals independently of external variations. There are two different linear regulator topologies: a conventional linear regulator and a low dropout (LDO) linear regulator. The main difference in these linear regulator topologies is the configuration of the pass transistor. The pass transistor in the conventional linear regulator is in a source-follower or emitter-follower configuration. The conventional LDO topology is shown in Figure 2.1. [1].

The main blocks of the conventional LDO topology are the error amplifier, the pass device and the linear feedback network (R1 and R2). To operate, the LDO also needs a voltage reference. This reference is established by an electric circuit known as Band Gap. The difference between LDOs and Band Gaps, since both provide a steady voltage, is that an LDO must be able to provide current and voltage to any indefinite number of load blocks. Band Gaps, on the other hand, must provide a steady voltage to a single block with constant input capacitance, which is usually a voltage regulator like an LDO. Some of the older linear voltage regulators mainly used NPN or PNP bipolar junction transistor as a pass element, but with higher demand for lower supply voltages and lower quiescent current, they have been replaced by MOSFETs. Main disadvantage of BJT transistors is

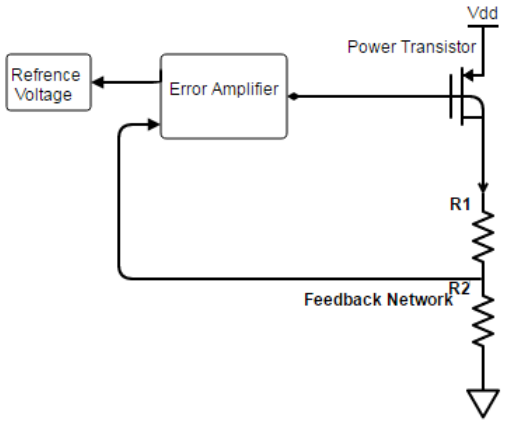

Figure 2.1: Conventional LDO topology [1]

that their base current is proportional to the load current according to given equation:

$$I_b = I_{load}/\beta \tag{2.1}$$

This current can be reduced by cascading BJT transistors at the expense of increased dropout voltage. Compared to base current of BJT transistor, the gate current of MOSFET is negligible and is not dependent on the load current, because the transistor is controlled by voltage.

LDOs can also be classified based on the compensation mechanism used for their open loop stability. Conventional designs use huge off-chip capacitor at the output to create a dominant pole and hence increases cost of the LDO. And in some cases it utilizes the Electrical Series Resistance (ESR) of such capacitors for pole-zero cancellation. Stability achieved by this manner heavily depends on ESR value which changes with temperature. An internal zero can be generated to help compensation without the dependency on ESR and output capacitor. Using such a huge off-chip capacitor poses several integration issues. A simple Miller compensation guarantees stability in a capacitor-free fashion. This saves cost and lot of board area and makes the LDO suitable for SOC design. But this kind of internal compensation has poor load transient and PSR performances compared to the conventional one.

2.2 LDO Performance Parameter:

2.2.1 Input/output Voltage Range

An LDO is first characterized by the operation range. A wide range of operation is desired for different load conditions. For different applications, the range can be widely different. Most analog environments require output to be greater than 1 V while in submicron digital, output voltage can be as low as 0.5 V.

2.2.2 Maximum/Minimum Load Current

Maximum load current indicates the maximum power available from an LDO and minimum load current is the point where LDO can operate before going into unstable. LDO can source up to maximum current specified before the pass transistor leaves its saturation state.

2.2.3 Dropout Voltage

Dropout voltage represents the differential voltage between input and output node of the voltage regulator at which the circuit ceases to regulate against further decrease of the input voltage. This tells the user what the minimum input voltage is for a particular output voltage which is typically specified at maximum load current. The voltage drop across the pass transistor is $V_{in} - V_{ref}$ and the wasted power is therefore;

$$P_{wasted} = (V_{in} - V_{ref}) * I_L \tag{2.2}$$

We thus define the dropout voltage as for power efficiency as we want as low $V_{dropout}$ as possible. This derives the fact that voltage drop over a power switch is lower than the voltage drop over a series power transistor. However, certain voltage headroom is required to maintain the pass transistor in saturation for reasonable power supply rejection ratio (PSRR).

2.2.4 Quiescent Current

There is a small amount of current consumed by the controlling circuit to make the LDO work properly, which is defined as quiescent current I_Q.This is the current when the device is enabled and no load current is supplied whereas shutdown current ($I_{shutdown}$) is calculated when the device is disabled and there is zero output voltage.

2.2.5 Efficiency

The LDO regulator efficiency is determined by three parameters: quiescent current, load current, and pass transistor voltage drop. The total no-load quiescent current consumption for the entire LDO regulator circuitry is also known as the ground current. Efficiency in terms of I_{gnd}, I_{load} and $V_{dropout}$:

$$Efficiency = \frac{(V_{out} * I_{load})}{(V_{in} * (I_{gnd} + I_{load}))} \tag{2.3}$$

When the dropout voltage of the LDO is at minimum and it supplies a large current to the load, the effect of the quiescent current is negligible and the efficiency approaches that of a switching regulator. However, when the load current is small, the maximum efficiency is limited by the quiescent current. Therefore, in order to minimize battery consumption during standby, the current efficiency of the LDO should be high. The longevity of battery life for low current applications can be significantly increased by reducing the quiescent ground current. At the other extreme, for very large load currents, the power efficiency is solely dependent on the pass transistor voltage drop, shown in equation 2.3. The efficiency of the linear regulator approaches 100% as the output voltage approaches the input voltage. This scenario, however, requires a large pass transistor and would result in a large gate capacitance. Clearly, there is a tradeoff between consumption and speed of the LDO regulator.

2.2.6 Regulation

Regulation performance in LDOs is determined by line and load regulation. Load regulation is a defined as the capability of the regulator to maintain output voltage with varying

DC changes in load current as given in equation:

$$LoadRegulation = \frac{\delta V_{out}}{\delta I_{load}} \tag{2.4}$$

where $\delta\ V_{out}$ and $\delta\ I_{load}$ are the changes in output voltage and load current. Load regulation performance is determined by the loop gain of the system.Line regulation, like load regulation, is a DC parameter which refers to the capability of the regulator to maintain V_{out} with variations in V_{in} in a DC sense.

$$LineRegulation = \frac{\delta V_{out}}{\delta V_{in}} \tag{2.5}$$

where$\delta\ V_{in}$ and $\delta\ V_{out}$ are the changes in input voltage and output voltage respectively. The line regulation is approximately the ratio of the pass device gain to the loop gain.

2.2.7 Transient Response

Transient response measures the settling time of the output when there is a step change in the output current. There are two types of transients; load and line. Load transients occur when the output current rapidly changes levels, such as a 1mA to 20mA step in load current. Line transients are when the input voltage rapidly changes levels, such as a 1V to 1.2V step. The maximum tolerance for the output voltage fluctuation varies between applications; analog electronics are quite stringent for the operating voltage while digital circuits are far less sensitive to variations in the supply voltage. For both load and line transients, important specifications are overshoot, undershoot, and response time and are usually shown as a plot with a particular output capacitor.
At the moment when the load current suddenly increases, the output voltage decreases until the control loop is able to respond to the change. The time required for the control loop depends ideally on closed-loop bandwidth as shown in equation:

$$t_{rise-time} = 0.35/Bandwidth \tag{2.6}$$

but in practice it depends on closed loop bandwidth, capacitance at the gate terminal and the slew rate of the signal. Responding to a current pulse with a rise time of a few nanoseconds requires a very large bandwidth from the regulator which is impossible to achieve with low power consumption requirements. Therefore, the current pulses are

outside of the loop bandwidth and the regulator cannot react to the load change. In this case, all of the required current is provided by the output capacitor.

2.2.8 Loop Stability

Since the entire regulative functionality of a linear regulator is based on negative feedback, correct frequency behavior of a LDO is crucial. Loop stability directly indicates the functionality of an LDO i.e. a working LDO must be stable. Further, the phase margin should be good enough such that the transient response is reasonable. To analyze the loop gain characteristic, a small signal model is drawn. Obviously, there are two poles in the system at DC and a zero is required before the unity gain bandwidth. The third pole due to low pass filter and parasitic of pass transistor at gate terminal creates the instability of loop so to maximize phase margin of loop, zero is placed appropriately before the unity gain bandwidth. Usually when the LDO is designed to support a big output current, the size of the pass device will be extremely big, making C_{gd} big. As we can see, the closed-loop gain is constant and starts to fall when open-loop gain reaches zero decibels. The open loop gain equals to 1 at the unity-gain frequency $f_0$db for this single pole system. Closed-loop gain pole is higher than the open-loop gain and loop gain magnitude is $1/\beta_f$ lower than the magnitude of open loop gain [8]. β_f is usually lower or equal to 1 and it states how "strong" feedback is applied.

2.3 Overview of proposed PLL-based LDO regulator

As previously discussed PLL based voltage regulation is suitable in low voltage digital circuits. This LDO is fully integrated in a single chip hence the output capacitor is not desired for its stability. This LDO provides high performance operation due to its integrator based architecture. In the conventional topologies which are based on op-amp as error amplifier, there is constant error at the steady state due to the limited DC gain of operational amplifier. But on the other hand, the proposed integrator based architecture performs the time integration of voltage which gives infinite DC gain which leads to zero error at steady state. [9] Below figure compares the bode plots of an integrator and op-amp:

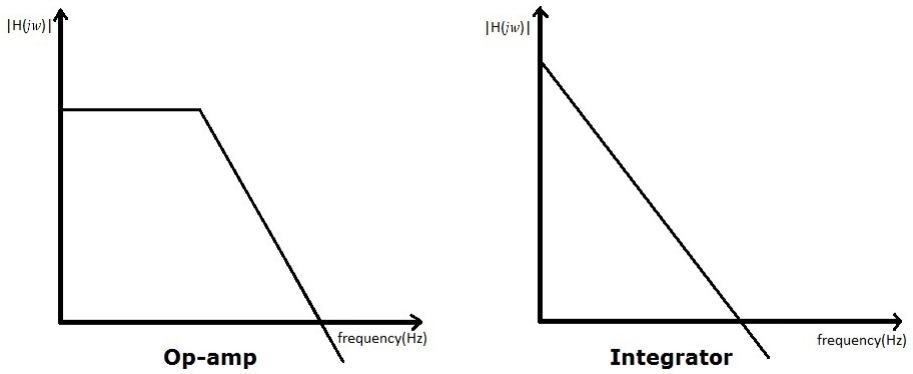

Figure 2.2: Bode Plot of Op-amp and Integrator

The proposed LDO regulates the voltages through digitally controlled loop which gives the advantage of low power consumption, low variation of temperature and process as well as less second order effects. Therefore it is suited for all compact and portable products, such as cellular phones, pagers, camera records, notebook, etc. In this architecture voltage controlled oscillator integrates the input voltage to output the phase which is fed to phase frequency detector. This phase frequency detector compares the two input phase where one is reference phase other is feedback phase from the output. Charge pump converts this phase into voltage by supplying the current through the impedance of low pass filter. High load regulation performance and low power consumption is achieved due to its integrator based architecture which also support digital controlled loop. This LDO is also stable even without output capacitor.

Chapter 3

FDSOI process specification

The proposed LDO is designed in 28nm FDSOI (Fully depleted silicon on insulator) technology. In FDSOI there are two primary modifications with respect to CMOS bulk technology. First, there is ultra thin layer of insulator called buried oxide at the top of base silicon and other is the thin silicon film which implements the transistor channel and because of its thin structure there is no need of to dope the channel thus named as fully depleted transistor. Due to this construction of transistor we are able to get much better transistor electrostatic characteristics than conventional bulk technology. In a fully depleted SOI (FDSOI) device, most of the field lines propagate through the buried oxide (BOX) before reaching the channel region. This buried oxide lowers the parasitic capacitance between drain and source terminal. Short-channel effects can be reduced in FDSOI MOSFETs by using this thin buried oxide and an underlying ground plane. FDSOI devices also have much better performance in terms of reduced leakage current [10].
To properly design circuits in FDSOI technology the designer has to be aware of the relationships between various parameters of the MOS transistors and its electrical characteristics. In this chapter various simulations of used MOSFET transistors will be presented together with basic theory of operation. All these simulations were done using ELDO circuit simulator of mentor graphics.

3.1 $I_d - V_{ds}$ Relation

We can generate a set of i_d vs V_{ds} curve for MOSFET by setting V_{gs} and varying V_{ds}. This can be shown in fig 3.1.

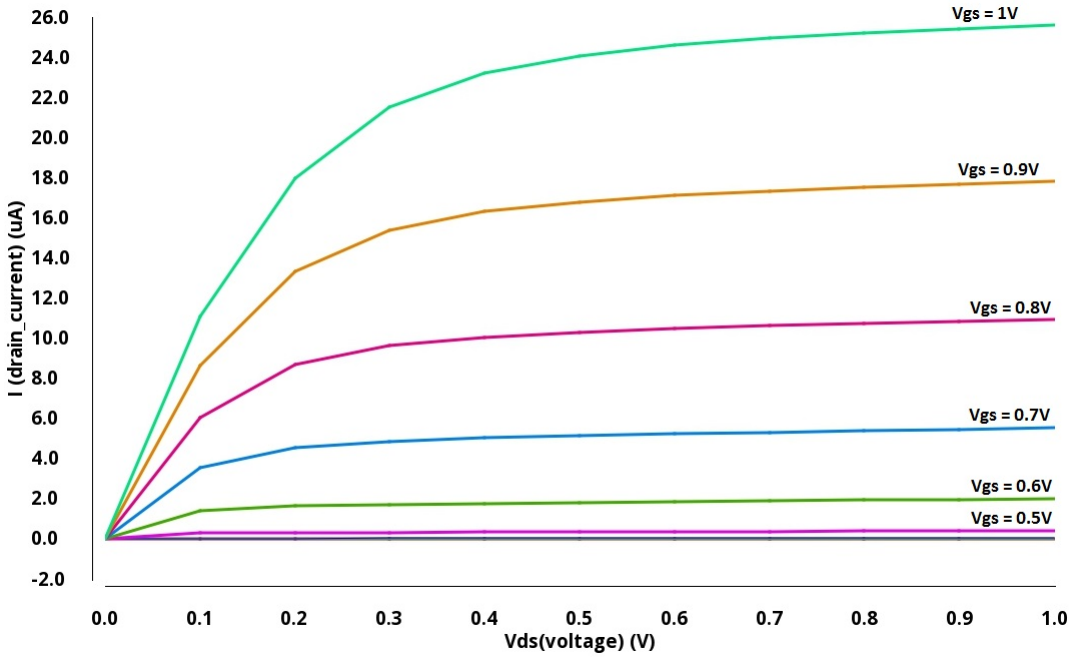

Figure 3.1: Id-Vds Characteristic

There are three region of MOSFET. First, Cut-off region where gate to source voltage is less than V_{th} .In this region dependence of current on gate voltage is exponential but the magnitude is negligible as the channel is not present. Conduction happening in this region is known as sub-threshold conduction. Second, Linear region where gate voltage increases beyond threshold voltage and channel is formed between source and drain terminals. In this region current increases linearly with increasing drain voltage till a particular drain voltage determined by the following relations -

$$V_{gs} > V_{th} \tag{3.1}$$

$$V_{ds} < V_{gs} - V_{th} \tag{3.2}$$

The linear model of FET is useful in the design of active linear circuit design. It may also be the basis for deriving some of the nonlinear large-signal model elements of the device. The large-signal charge models are derived from the bias dependent capacitance

of the small-signal model. Other benefits of using small-signal equivalent circuit are model scaling and data size reduction. Since the electrical equivalent circuit model elements are frequency independent, there is data size reduction as compared to using the S-parameter directly in a circuit design. The small-signal equivalent circuit elements may be scaled with gate width and number of gate fingers thereby enabling the designer to predict the S-parameters of different device sizes. Theoretically, it can also be used to extrapolate device performance beyond the original measurement data range.
Saturation region is the third region where the effect of drain voltage on current is negligible. MOSFET in saturation act as a current source. That is regardless of the voltage across V_{ds} the current through the device will be constant.

3.1.1 Channel Length modulation

In the saturation region actual channel length is modulated by drain to source voltage. An increase of drain to source voltage causes more depletion region at the drain junction and the effective channel length gets reduced. Channel length modulation is modelled by the parameter lambda which is inversely proportional to the effective channel length i.e.

$$\lambda = \frac{\delta L}{V_A L} \tag{3.3}$$

where V_A is fitting parameter.Channel length modulation is significant in case of short channel. The output resistance is inversely proportional to the channel length modulation factor. Higher the modulation, lower the effective output resistance. In FDSOI devices, the change in channel potential with the increase of drain to source voltage is negligible hence the second order effect of channel length modulation on FDSOI devices is far less than CMOS bulk technology.

3.2 Threshold Voltage

Minimum Voltage required making the transistor in ON state. It affects both the overdrive and current of the transistor hence an important parameter for design. Variation of threshold voltage with other parameter should be studied while designing the circuit. We can see that V_{th} increases at shorter channel lengths. This is called reverse short

channel effect which is a result of non-uniform channel doping. Channels are more doped near the drain and source terminals which reduce the size of depletion region near these junctions. At shorter channel length the doping of the source overlaps the doping of the drain, which increases the average channel doping concentration and this translates into increase of threshold voltage. Also the effect of process and temperature on threshold voltage should be studied because process parameters can be the same roughly but it varies with die.

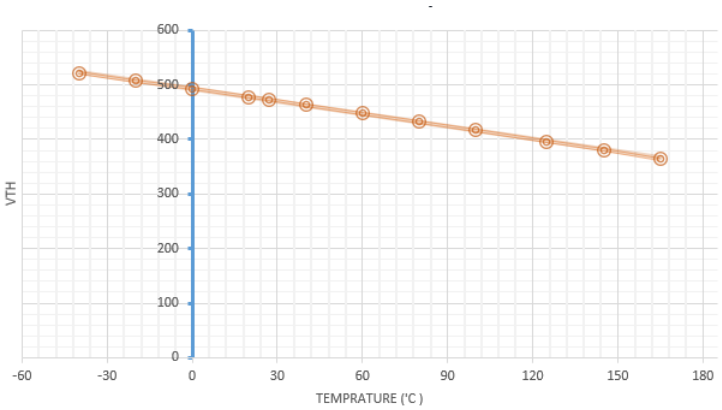

Figure 3.2: Threshold Voltage Vs Temperature

3.2.1 Body Effect

Threshold voltage of the transistor varies with source to bulk voltage according to the below equation. This is known as body effect

$$V_{th} = V_{t0} + \gamma * \sqrt{|V_{sb} + 2\phi_F|} - \sqrt{|2 * \phi_F|} \tag{3.4}$$

Where γ is junction depletion region coefficient and depends on the used technology but is not voltage dependent. ϕ is Fermi potential. This body effect can be avoided by connecting bulk to source of the transistor, but that is not always possible, since it depends on the technology.

On the other hand, FDSOI technology has the advantage to efficiently control the threshold voltage. In FDSOI devices we control the variation of parameter values and the transistor behaviour not only through gate terminal but also by giving the voltage in bulk terminal under the buried oxide [2]. In CMOS bulk technology there is parasitic

leakage current due to body biasing hence this technique is not implementable on this technology. But in FDSOI devices due to the buried thin film oxide layer, body biasing is efficiently used to control the transistor behaviour.It can be observed that the gate terminal is actually controlling the current whereas the body terminal is controlling the gate terminal hence it acts like a back gate. Hence the presence of the buried oxide allows the application of higher biasing voltages, resulting in dynamic control of the transistor. FDSOI devices also give the advantage of forward body biasing. This (Forward Body Biasing) FBB is an extremely powerful technique to optimize performance and power consumption. This technique is easy to implement, as FBB can be modulated dynamically during the transistor operation, bringing a great flexibility for designers. Forward body bias improves switching speed at the expense of leakage. However, the designer has

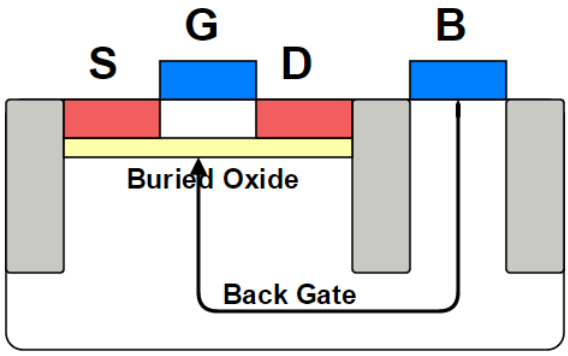

Figure 3.3: Forward Body Bias [2]

to select whether performance or leakage is more important for the particular transistors.

3.3 DTMOS Configuration

Dynamic threshold MOS (DTMOS) techniques are used to reduce the threshold voltage of the MOS transistor. Biasing the body terminal is to control the threshold voltage of FDSOI devices and decrease its sensitivity over t_{ox} i.e. thickness of the metal oxide. From the layout point of view, implementation of triple-well technique is needed for the CMOS transistors while implementing DTMOS technique but there is no such restriction in FDSOI devices because the body terminal is insulated by thin buried oxide layer. Dynamic threshold voltage MOSFET (DTMOS) technique is very effective in terms of

controlling threshold voltage dynamically by biasing the body terminal, which requires ultra-low supply voltage (below 0.6V) [3].

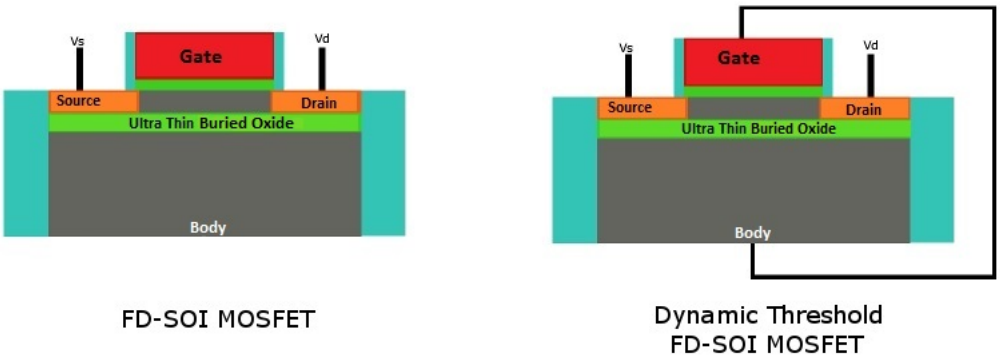

Figure 3.4: DTMOS configuration [3]

3.4 Technology Parameter

Below are the technology parameters of 28nm FDSOI which are important to keep in mind while designing the circuits:

Parameter	**NMOS**	**PMOS**
Supply	1.8V	1.8V
Max.Width(W)	35u	35u
Min. Width(W)	160n	160n
Max.Length(L)	10u	1.104u
Min.Length(L)	150n	150n
Vt (saturation)	518mv	481mV
Vt (linear)	517mV	540mV
Leakage	1pA	2.6pA
Gate Oxide	150	150

Table 3.1: FDSOI technology parameter

Chapter 4

Design of PLL-Based Low Dropout Voltage Regulator

4.1 Proposed LDO Architecture

Figure 4.1 illustrates the functional block diagram of the proposed PLL-based voltage regulator. It consist of phase-frequency detector (PFD) followed by a difference detector circuit, charge pump filter, two current controlled oscillators, low to full swing amplifier and a power transistor. LDO output voltage is fed to the differential voltage controlled oscillator (VCO's) which converts the output voltage into frequency .Similarly, the reference voltage is converted into frequency with differential voltage-controlled oscillators. Here, in order to obtain high PSRR, fully differential 3-stage ring oscillator is implemented. The output signal of the VCO passes through a low-to-full swing (L-F) amplifier. The frequency output from both voltage-controlled oscillator is compared by the phase-frequency detector. PFD generate the pulse width which is proportional to phase difference of the two wave generated by the voltage-controlled oscillator [7]. The PFD is followed by the charge pump and a low pass filter which produces the control voltage at the gate of common-source power transistor which provides the load current and does the voltage regulation at the output.

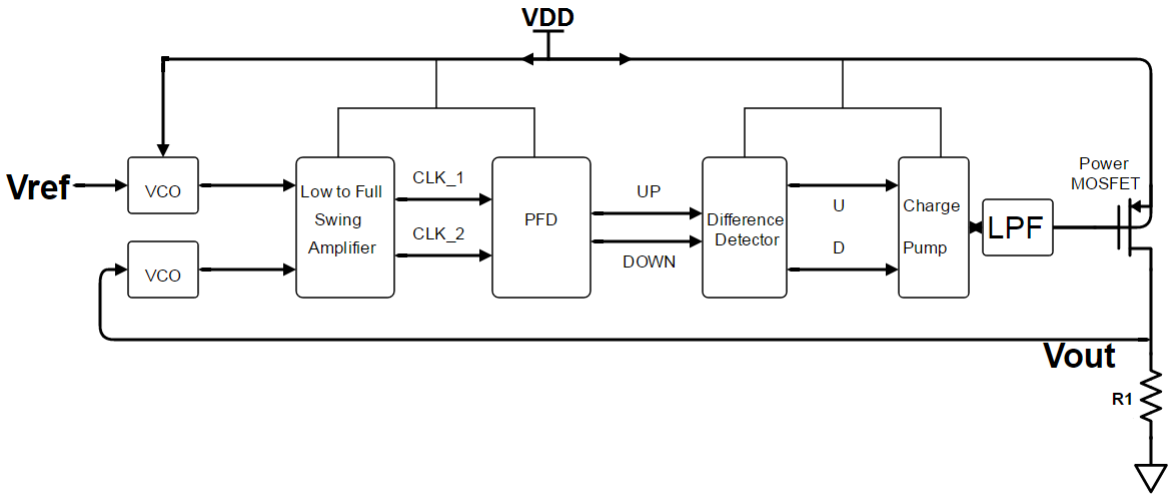

Figure 4.1: Functional block Diagram Of Proposed LDO

The design challenges for the proposed PLL-based voltage regulator are 1.) High unity gain bandwidth 2.) Good Phase Margin 3) to achieve high supply noise rejection for each block in the system. 4.) Low power and low quiescent current. 5.) Low operating Voltage

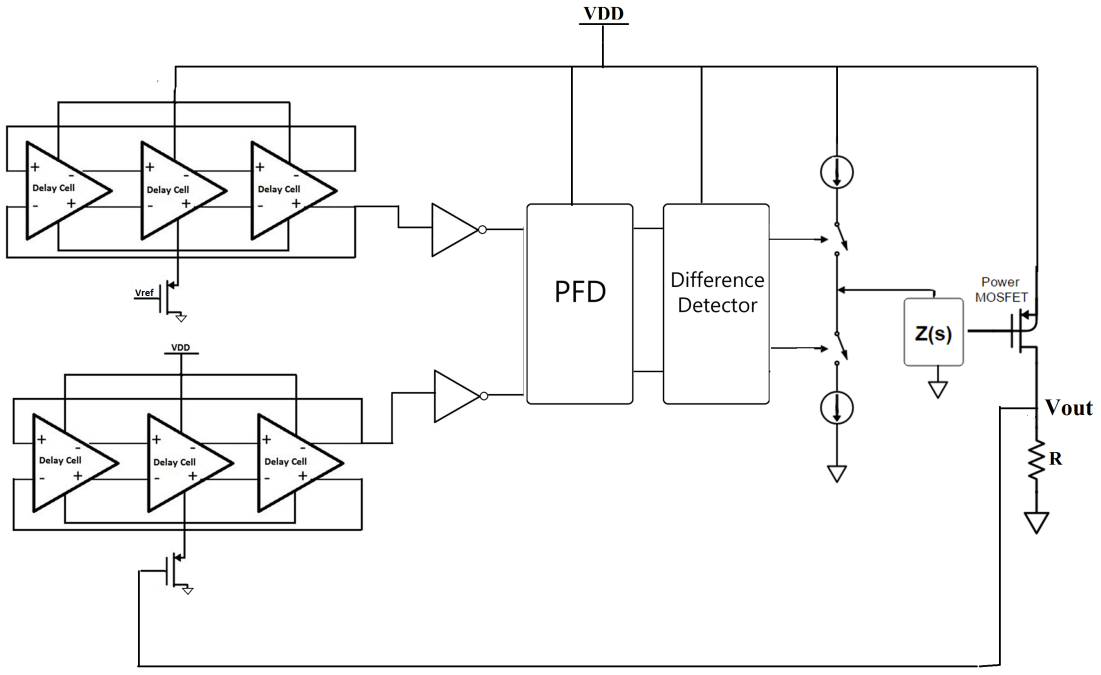

Figure 4.2: Circuit Diagram Of Proposed LDO

4.2 Design of LDO components

4.2.1 Voltage Controlled Oscillator

VCO composed of voltage to current converter and differential current controlled oscillator. It converts the voltage into frequency while providing the gain K_{vco}. Architecture of the oscillator is based on the ring oscillator with differential delay cells. Among all blocks in the system, the design of a low-jitter VCO is the most critical one because any noise coupled into the control input voltage is directly translated to the change in the oscillation frequency. This change in frequency appears is basically phase error which is persistent for the time equal to the time constant of the loop. The jitter accumulation issue becomes more sever for lower loop bandwidths or higher time constant. To avoid the problem, design of a VCO with high supply noise rejection is required. A differential delay stage is employed in order to achieve good power supply noise rejection [11].

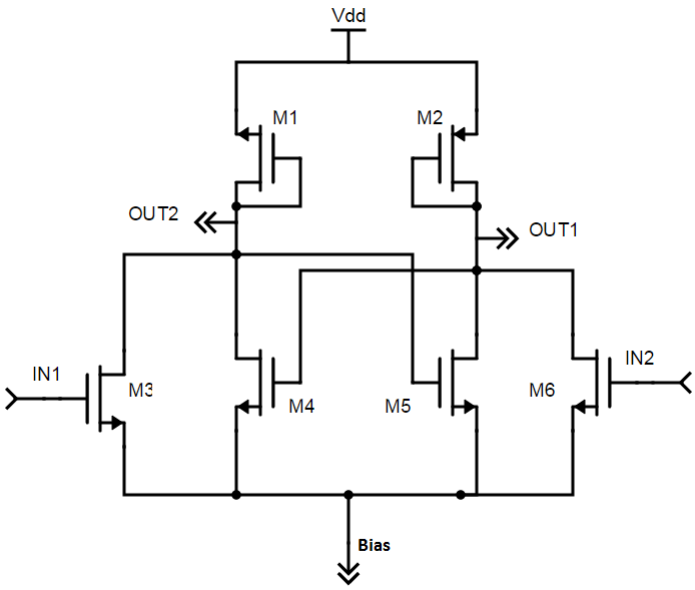

Figure 4.3: Delay cell of VCO

Figure 4.2 shows a saturated delay stage with cross-coupled PMOS load. The regenerative PMOS transistors provide rail-to-rail output signals via the full switching of the FETs. The latch circuitry reduces the delay of the stage, allowing higher frequency of operation.

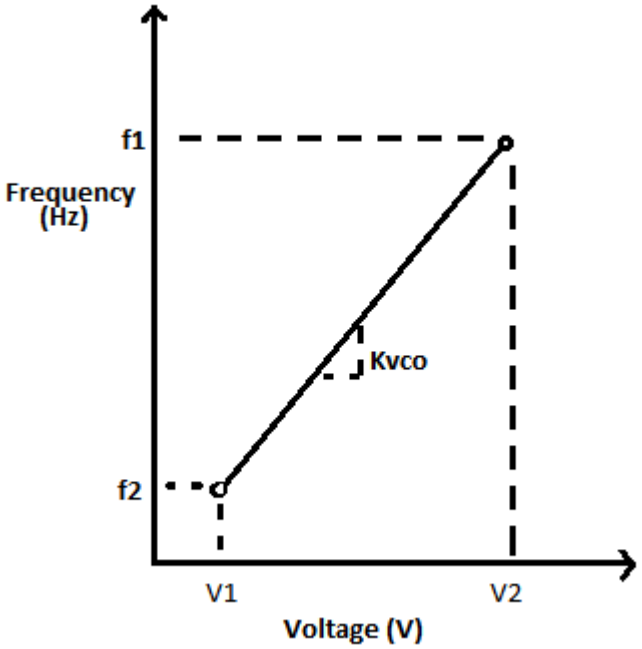

Figure 4.4: Voltage vs frequency curve of VCO

The full switching of the transistors also reduces the flicker noise. Number of delay cell used in design is 3. We can see the delay control option is given by controlling the tail current source as shown. This design limits the voltage swing at the output. Main focus for the design is to make the voltage controlled oscillator as much linear as possible. It is important to note that this oscillator has a single ended control; however it is constructed by differential delay elements. Implementing the differential stages yield 50% duty cycle, thus improving the spectral purity of the output frequency. Voltage versus frequency curve is plotted for the designed VCO in Figure 4.3. where K_{vco} is the slop of the graph between voltage and frequency. Transfer function of the VCO is given as:

$$H(s) = \frac{K_{vco}}{s} \tag{4.1}$$

VCO performs an integration of the control voltage and thus provides a factor of 1/s in the loop transfer function.Hence, PLL is always first order feedback system.

4.2.2 Low to Full Swing Amplifier

As discussed, delay cell of the VCO has the differential architecture and this design limits the voltage swing at the output of voltage-controlled oscillator. A low to full swing amplifier is designed which maintains the full swing at the output of VCO which is feeds back to PFD. Low to full swing amplifier is the skewed buffer placed just after the VCO. It is designed such that it has minimum delay.

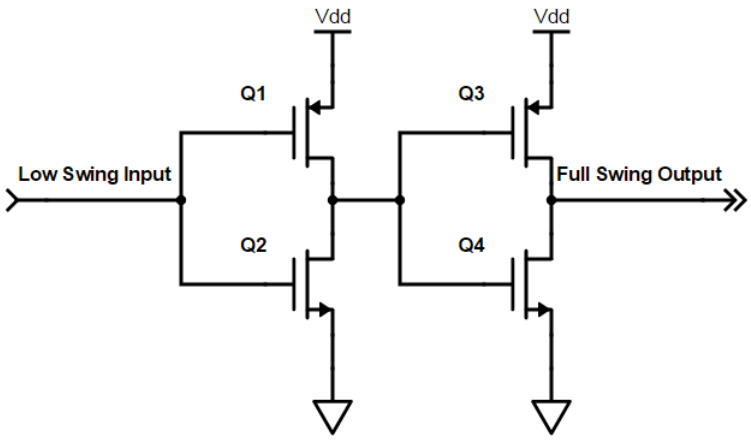

Figure 4.5: Low to Full Swing Amplifier

4.2.3 Phase Frequency Detector (PFD)

A conventional architecture for clock generation uses a phase-frequency detector (PFD) for simultaneous phase and frequency acquisition. Figure 4.5 illustrates a common linear PFD architecture using re-settable D-flip flops (DFFs) [4]. The DFFs are triggered by the inputs of the PFD. Initially, both outputs are low. When one of the PFD inputs rises, the corresponding output becomes HIGH. The state of FSM moves from an initial state to an Up or Down state. The state is held until the second input goes high which in turn resets the circuit and returns the FSM to the initial state. The PFD's characteristic is ideally linear for the entire range of input phase differences from -2π to 2π. As explained, PFD compares the two input clock and output the pulse which is modulated by the phase difference between the two clocks. PFD have the unique ability to detect the frequency with the phase detection hence PFD is preferred over PD. Also Phase Detector which is

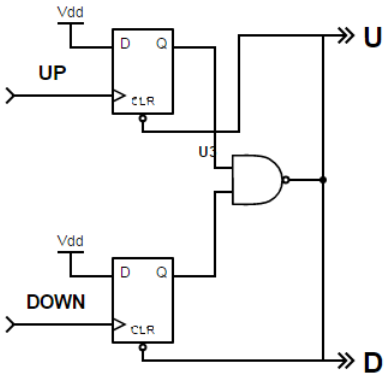

Figure 4.6: Phase Frequency Detector [4]

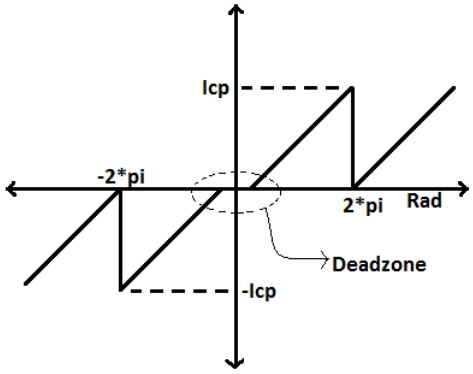

Figure 4.7: Transfer Curve Of PFD

usually XOR gate have finite input range however it is not so in Phase frequency detector. Transfer Curve of the PFD is shown.in Fig 4.6

PFD have the problem of deadzone. Deadzone is the case when phase error is small and short output pulses produced by PFD cannot effectively propagate to switch charge pump results in the phase detector dead zone which causes low loop gain and increased jitter. Given that the worst case turn-on time for the charge pump switches was found through simulation to be 0.1ns, the propagation delay of the PFD was set to be such that any deadzone of operation could be safely avoided. Transfer function of PFD that relates the average on time with phase error is:

$$H(s) = \frac{1}{2\pi} \tag{4.2}$$

4.2.4 Difference Detector

In the conventional Phase Frequency Detector, large jitter is produced in the loop when it is locked state. This jitter is produced due to large deadzone in phase characteristic of PFD. A dead-zone occurs when the loop is in a lock mode and the output of the charge pump does not change for small changes in the input signals at the PFD. This may cause many problems. Conventional PFD architecture have four states among which the state when UP and DOWN signal rise to high at the same time creates phase error and jitter problem. Actually for this state, charging and discharging current should be same in charge pump to maintain the locked state but due to the non-ideal effects of transistor there is mismatch in these two currents which will cause jitter problem. Difference detector is implemented to decrease the phase error in the loop due to above discussed problem. It output the pulse of same width as of intermediate signal such that of phase and frequency of two signal is same it will generate all-zero output. Difference detector converts the four state property of conventional PFD into three state property i.e. it avoids the case of UP and DOWN signal both high at the same time. Hence, this circuit improves the phase stability when the loop is in locked state [5].

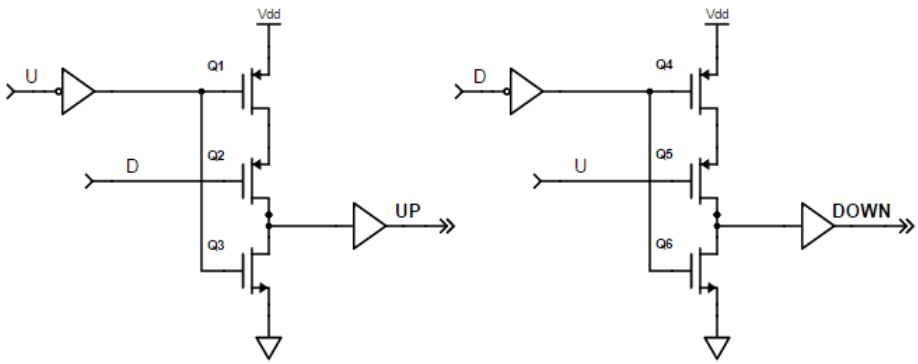

Figure 4.8: Difference Detector [5]

4.2.5 Charge Pump

Figure 4.8 shows the implementation of charge pump for the PLL based voltage regulator. Charge pump is used to source and sink the current into loop-filter according to the output of PFD. Charge pump transfers the phase difference into current. The charge-

pump converts the up and down pulses into current pulses and these current pulses change voltage across the loop-filter impedance which is actually the control voltage. The charge-pump circuit needs to be carefully designed because it is the main contributor to low-frequency PLL noise.

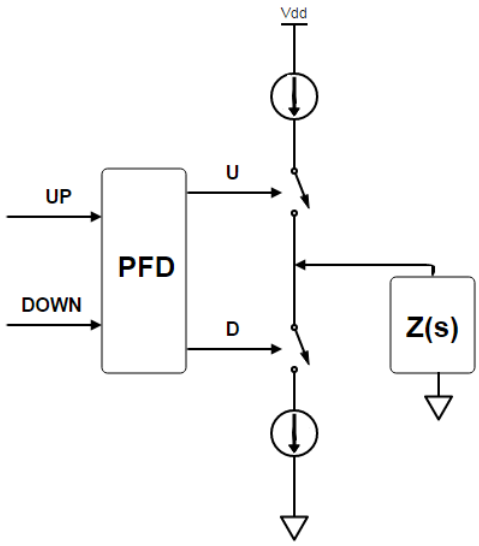

Figure 4.9: Charge Pump

Problems in designing charge pump are current mismatch, charge sharing and charge injection noise which contributes to the low frequency noise. Charge sharing is mostly caused by the position of two switches placed in the charge pump. When the charge pump is drain switched, charge is shared between the capacitance at the source node and the output capacitor. Mainly, unity gain amplifier is used to reduce the charge sharing but due to its large power consumption this design is not used in the present circuit . Other implementation of charge pump are source switched and gate switched which has many other disadvantages.

Charge injection is another consideration when designing a good Charge pump. Whenever any switch is ON, there are charges under the gate of the transistor and these charges under the gate in the OFF state will be injected to the drain and the source of the transistor. If the switch is next to the output pin, the injected charge will cause ripple at the output which is undesirable.Charge injection can also be through clock feed through mechanism which is due to the coupling capacitance from the gate to both the source and drain due to which a portion of the clock signal appears across load capacitor. One of the way to reduce the charge injection is by the use of dummy switch [6].

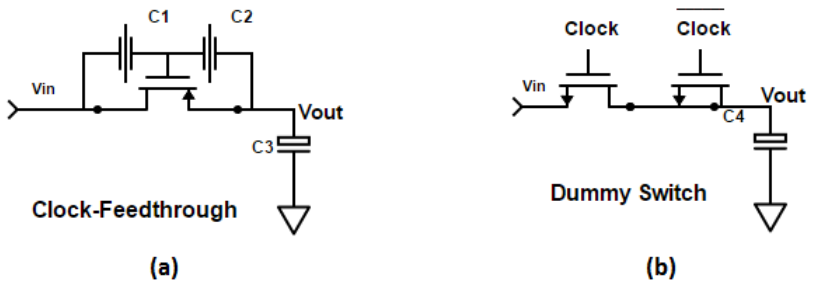

Figure 4.10: a)Clock-Feedthrough b)Use of dummy switch [6]

Dummy switch is the MOS device with its drain and source shorted and placed in series with the desired switch with its control signal being the inverted signal of that main switch. So charge injected by main switch is essentially matched by that which is induced by dummy switch hence overall charge injection is canceled .Therefore this charge will not affect the value of the control voltage.

The current mismatch in the charge-pump,one of the main design problem, also leads to static-phase offset and causes ripples in the control voltage, thereby creating a 'jittery' output. Thus, it is important to design a CP circuit that has equivalent pull-up and pull down currents and equal on-time for the PMOS/NMOS switches. The classical method of reducing the current mismatch of the charge pump is to either increase the output resistance of the pump or to use a compensation method. The output resistance of the charge pump can be increased by either using a cascode or a gain–boosting topology. This will however reduce the output dynamic range and prevent the use of the pump for low voltage operations. The compensation method is implemented by the use of operational amplifier.The op–amp enables the pump currents to track each other and then compensate for any mismatch. This will however result in higher power consumption and an area overhead due to the addition of the op–amp.The transfer function of charge pump is :

$$H(s) = I_{cp} \tag{4.3}$$

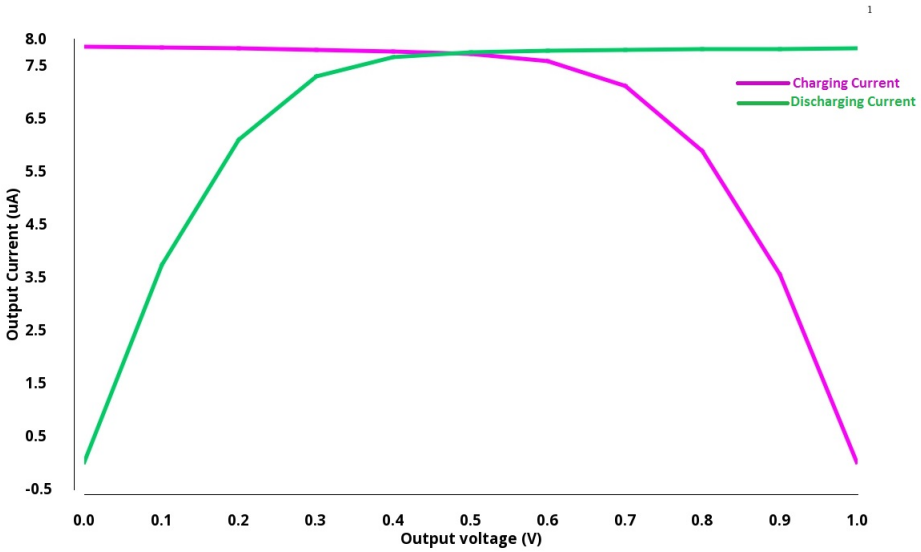

Figure 4.11: Current matching characteristic of charge pump

4.2.6 Low Pass Filter

The function of the low pass filter (LPF) is to convert the charge pump current into control voltage. Low pass filter charges or discharges the capacitor according the phase detector output. Basically, Loop filter composes of a capacitor, C1,where the charge pump injects the charge into or out of it. This capacitor contributes a DC pole which leads to instability. As the VCO is already an integrator, and other components will add a bit more phase shift, a simple second integrator (low pass filter) in the loop would guarantee instability by giving 180 degrees plus a bit of phase shift. For the stability of loop a zero should be introduced by adding a resistor, Rz, in series with the loop filter capacitor. This resulting low pass filter is termed as first-order passive lag-lead filter. Component value of this filter should be wisely chosen such that there is enough phase margin and good settling time.

The function of the LPF is also to remove the high frequency components in the output of the phase detector and to remove the high frequency noise. High frequency noise leads to spurs at the VCO output which can be damned down by placing a second capacitor in parallel to C_1. Thus, for the ripple suppression and reduction of spur a capacitor in parallel is placed. This forms a second order low pass filter which have better performance than simple low pass filter.

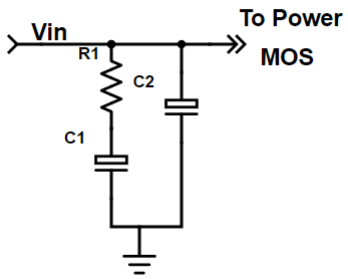

Figure 4.12: Low Pass Filter

Each component value of low pass filter should have optimum value as it plays the critical role in generating smooth and ripple free control voltage. For the better ripple suppression we need high C2 value whereas for good phase margin the value should be less than C1 comparatively. Hence there is trade-off between phase margin and ripple suppression factor. Hence, the ratio C2/C1 is normally taken around 10. While designing the cut off frequency of low pass filter, we should know that if filter has a very low cut-off frequency then the changes in tune voltage will only take place slowly and the VCO will not be able to change its frequency as fast but if a filter has a higher cut-off frequency it will pass the unwanted frequencies resulting in spurious signals at control voltage. Transfer function of Low Pass Filter :

$$H(s) = \frac{s(sR_zC_1 + 1)}{s^2C_1C_2R_z + sC_1} \tag{4.4}$$

4.2.7 Pass Device

Power transistor should be sized for the dropout voltage such that it can source the maximum current maintaining its state to be in saturation. We have two choices of pass device NMOS and PMOS. For the NMOS we need the charge pump to raise the gate voltage such that transistor is properly biased. This will need more complex circuitry. Hence, PMOS is best choice because of its low drop out voltage. Now after deciding PMOS device as power transistor we need to consider the maximum load current and low dropout voltage. We need to design pass device such that it can deliver maximum drain current forcing the dimension of pass device for the desired low dropout regulator. We need to keep the dimension (W/L) in limit because the larger dimension will have larger capacitance which will decrease the phase margin and reduce the bandwidth of loop.

So, there is trade off between gate capacitance and transconductance of pass transistor. This pass device can be modelled as gm with output resistance and a gate capacitor. As discussed, pass device in this work is used in DTMOS configuration which gives large transconductance value for the same aspect ratio.

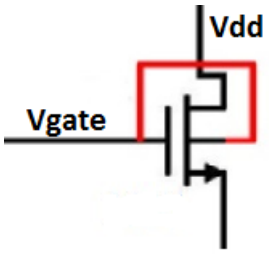

Figure 4.13: Power Transistor

Chapter 5

Simulation Results

5.1 Behavioural Modelling and Simulation Results

To minimize the fabrication cost, we need a way to predict the specification before fabricating the design. Simulation is obvious solution but it takes much larger computing time to run simulation for the evaluating full design. Therefore, behavioural model of each block is modelled in MATLAB and simulated. Simulation using these models is much faster than circuit level simulation. We can complete many simulations in a day, implementing different ideas for each functional block. Behavioural model for each block is created with a simple Transfer function block. Model of the proposed LDO is shown in the fig 5.1.

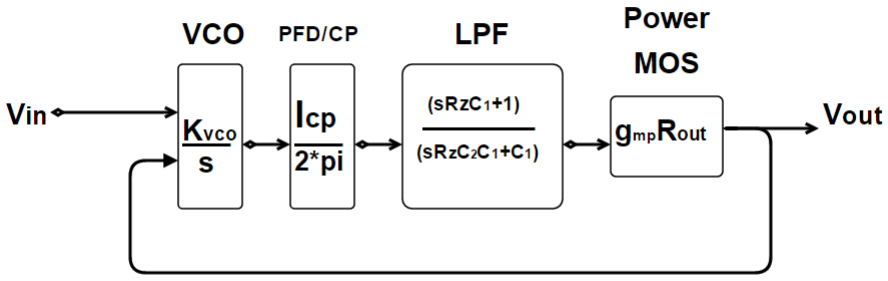

Figure 5.1: Linear model of proposed LDO

Transfer function of each block is discussed before in chapter 4. Power transistor here is modelled as $g_{mp} * r_{out}$ where g_{mp} is the transconductance of power transistor. The open loop transfer function of proposed LDO is shown in equation below :

$$\frac{V_{out}}{V_{in}} = \frac{K_{vco}}{s} * \frac{I_p}{2\pi} * \frac{s(sR_zC_1 + 1)}{s^2C_1C_2R_z + sC_1} * g_{mp}R_{out} \tag{5.1}$$

This closed loop system has three poles and a zero. VCO integrator contributes a pole at 0rad/s and two remaining pole is due to low pass filter. This system has closed loop zero due to resistance placed in low pass filter which stabilize the loop. We need to place third pole such that maxima of phase plot occurs at the unity gain frequency.This condition maximizes the phase margin for the required W_u. Hence, at unity gain frequency the derivative of the phase w.r.t frequency at W_u is calculated and kept equal to zero i.e.

$$\frac{\delta\phi_m}{\delta W_u} = 0 \tag{5.2}$$

We get the relation between W_z , W_{p3} and W_u as shown in equation 5.3. so, the desired parameter are W_u as well as phase margin and requirement is optimal phase margin.

$$W_u = \sqrt{W_uW_z} \tag{5.3}$$

Using this relation, we can write W_u in terms of C_1 , C_2, W_z and W_{p3}. Phase margin at this W_u is derived using the above relation.

$$P.M = \arctan\sqrt{1 + \frac{C_1}{C_2}} - \arctan\sqrt{\frac{1}{1 + \frac{C_1}{C_2}}} \tag{5.4}$$

For the required unity gain-bandwidth and phase margin we can calculate the value of $\frac{C_1}{C_2}$, W_z and W_{p3} using the equation 5.4. There is always a concern for the area of capacitor i.e. for large phase margin we may need a capacitor of the value in the range of uF which consume larger area. Hence there is always a trade off between phase margin and value of capacitor. Choice on the value of R_z is done according to the noise analysis. Since we know the value W_z which is equal to $\frac{1}{RC_1}$, we calculate the absolute value of C_1 and then C_2. At the unity-bandwidth frequency, magnitude of the open loop transfer function is 1. Using this condition we find out the value of I_{cp} [12].

But the value of $\frac{C_1}{C_2}$ is not only decided by the phase margin because the location of third pole W_{p3} also decides the suppression of the ripple at the output. Hence ratio $\frac{C_1}{C_2}$ is kept around 10 for both condition to satisfy. Also absolute value of C_1 and C_2 is chosen such that there is trade off between the unity-bandwidth frequency and cut-off frequency of low pass filter. The Open loop transfer function is simulated in MATLAB to calculate the bandwidth and phase margin of the loop. Optimum parameter value is selected according to the bandwidth and phase margin of the system.For the different load condition bode plot of loop transfer function is plotted:

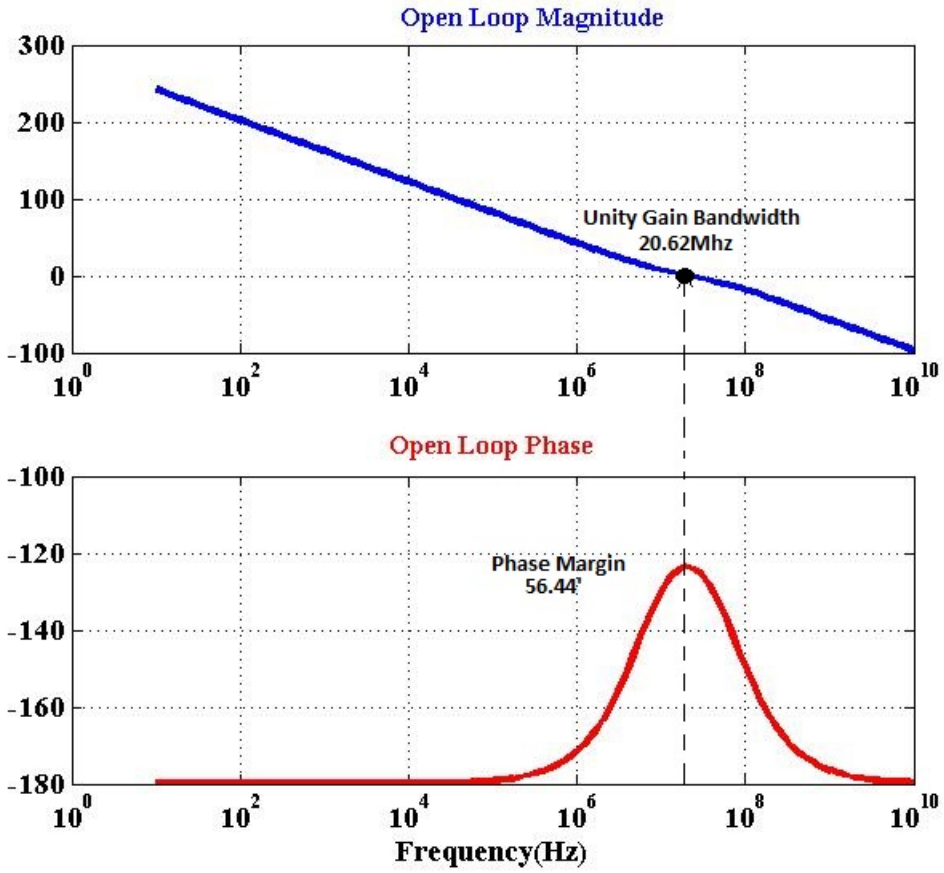

Figure 5.2: Magnitude and Phase plot of PLL-based LDO

5.2 Transistor Level Simulation Results

This chapter presents the simulated results that characterize the LDO. All simulations are done for the minimum dropout voltage of 200mV; input voltage of 1V and regulated output voltage of 800mV. The proposed LDO is stable without output capacitor. This LDO can source the load current up to 20mA. The proposed LDO with digital controlled loop is designed in 28nm FDSOI technology. Simulations are performed at room temperature using Mentor Graphics' ELDO simulator.

5.2.1 Start-Up Simulation

Start-up response and power-down response of the proposed LDO is described in this section. When power down signal is HIGH, circuit is in power down mode. Circuitry only starts up when the power down signal is LOW and regulation takes place. This simulation is done with input voltage of 1 V for both light and heavy load conditions, 0 µA and 20 mA respectively. The start-up response of the circuitry is shown in Figure 5.3.
Start-up response show that for the given load condition, the regulator stabilizes the output voltage within settling time 1.6µs. We can observe that regulator settle to desired output voltage in very less time for heavy load condition giving better performance at high load currents. At power down mode, current consumption by the voltage regulator is in order of picoampere as all the blocks in the regulator is in OFF state. On the other hand, when power down signal is LOW the regulator start up and consumes quiescent current which is in order of microampere.

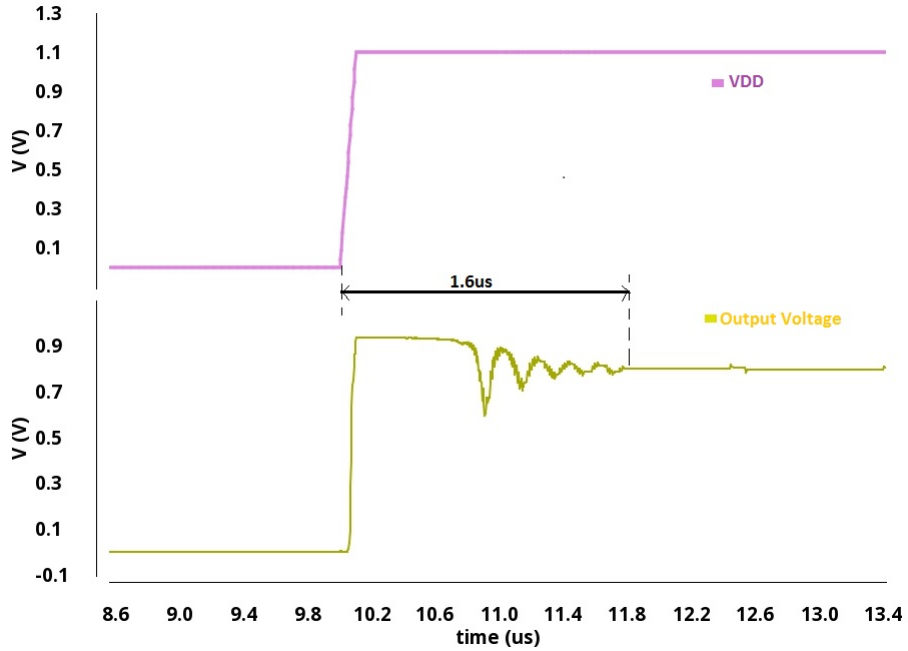

Figure 5.3: Start-Up simulation

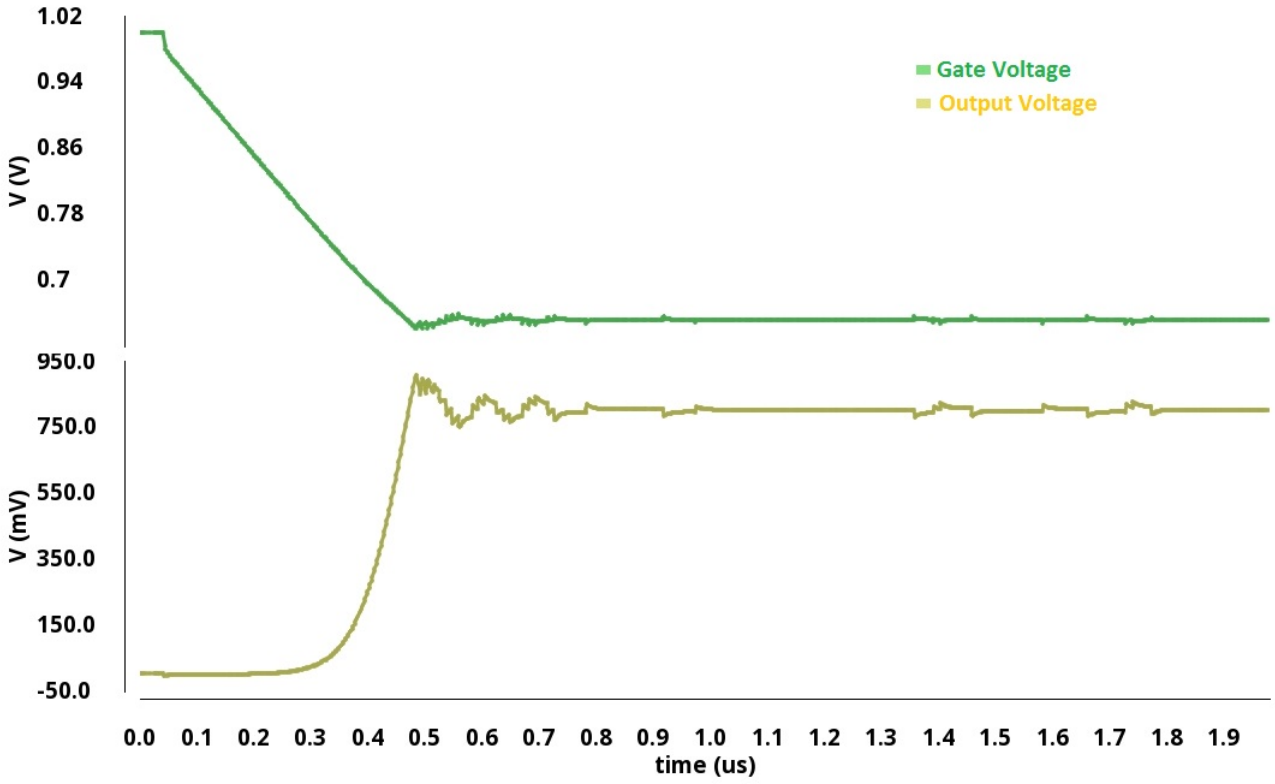

Figure 5.4: Start-Up simulation at light load condition

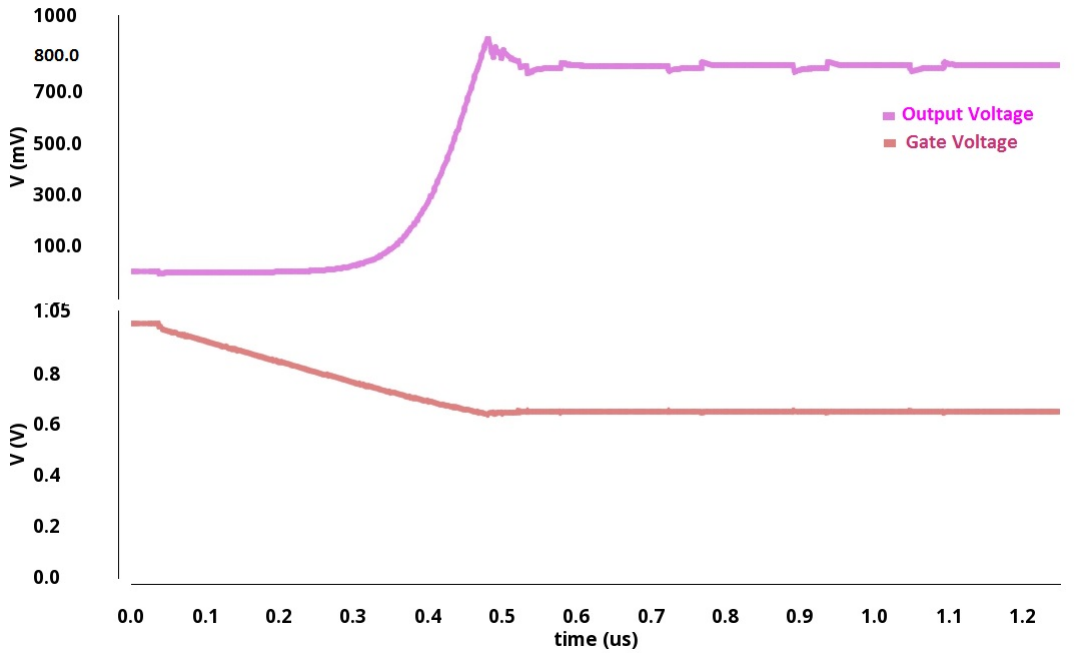

Figure 5.5: Start-Up simulation at heavy load condition

5.2.2 Steady State Behaviour

This simulation is performed to analyze the steady state behaviour of the proposed LDO. Stability of the loop, output voltage ripple and the constant phase offset when the voltage regulator is in steady state is studied. The simulation is performed at different load condition with multiple input voltages. Steady state phase offset and output voltage ripple under different load condition are shown below figure. The static phase offset is 0.381% and the output voltage ripple is 13.23uV peak to peak.

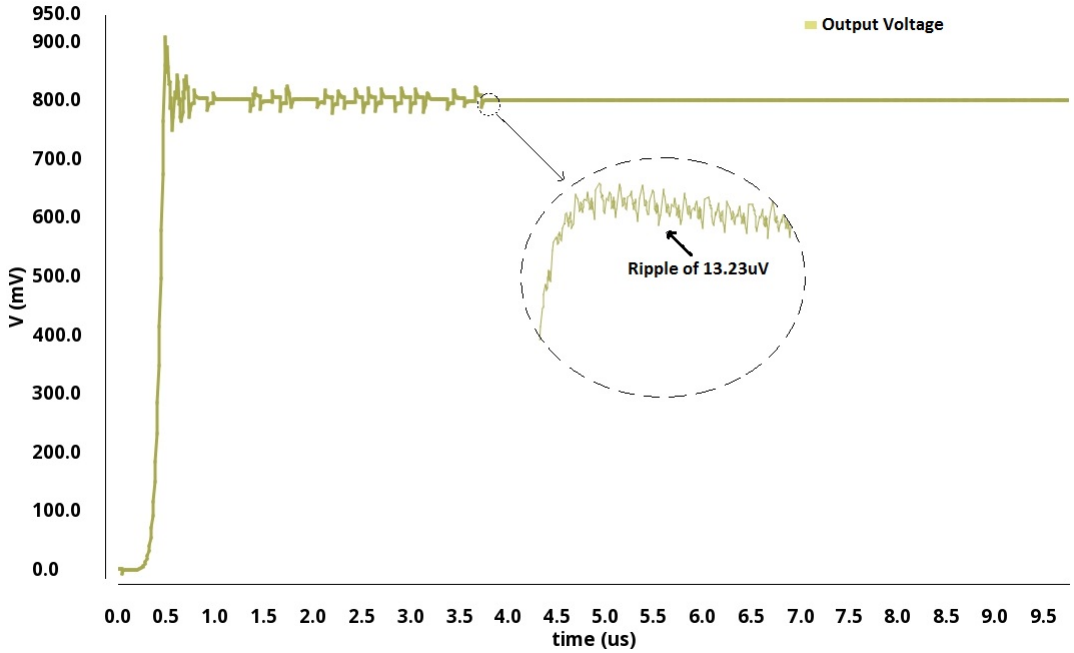

Figure 5.6: Output voltage ripple at steady state

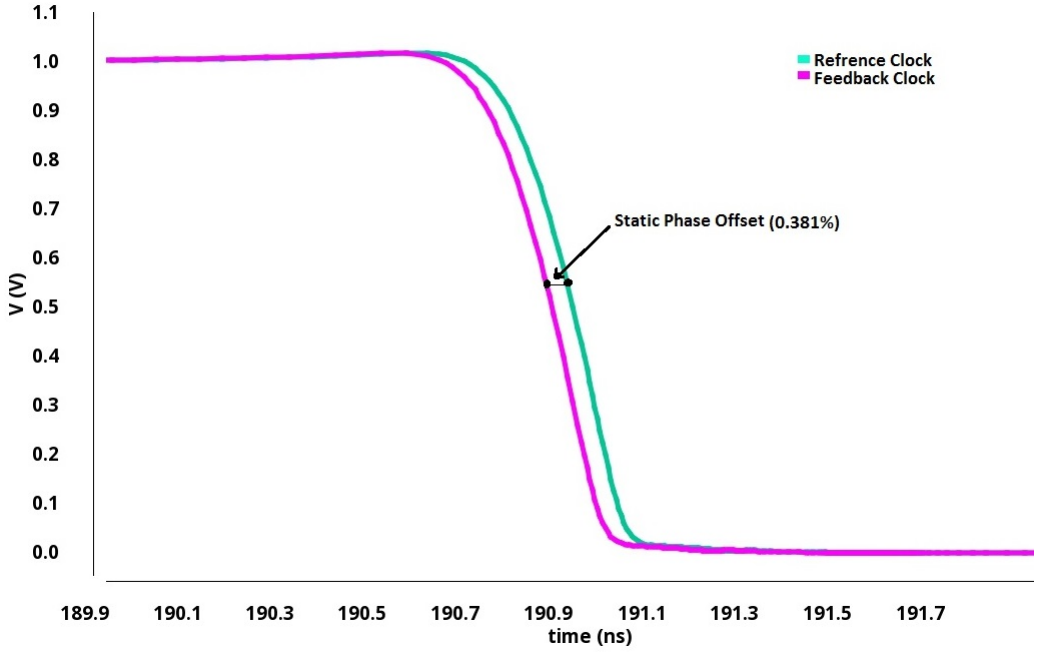

Figure 5.7: Static Phase Offset at steady state

5.2.3 Transient Response

Most important analysis is transient simulation, because it test how the circuit behaves in real time with varying large signal transients. Load and Line Transient responses are the two most important parameters in transient analysis of LDO regulator. If we simulated correctly and the circuit is stable, we should not see any oscillations or ringing during the step responses. In load transient analysis output current is varied using a current source at the output of the LDO, between 0µA to 20mA (no load situation and full load situation respectively) with a rise time and a fall time of 3µs.

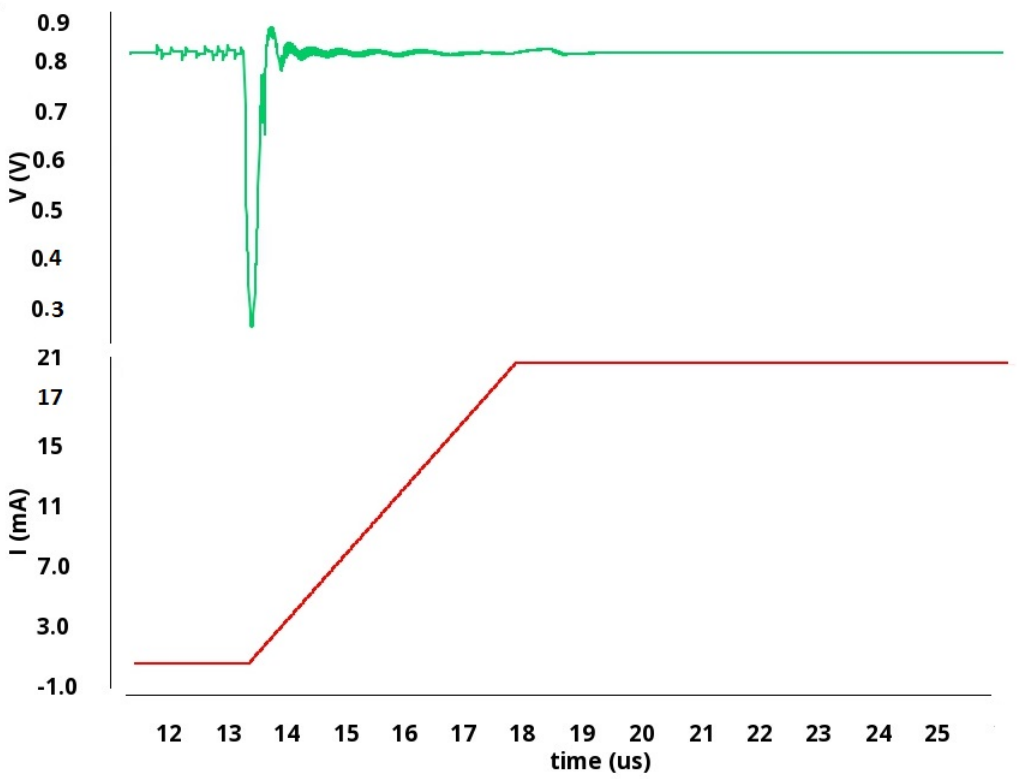

Figure 5.8: Load transient Behavior (from no load to full load)

As shown in above waveform, the LDO is stable with no output cap. With no output cap, the settling time is roughly 3.6µs and 3.8µs for the both the load steps. When the rise of the load current is very fast i.e. frequency is above the bandwidth of the system, the regulator does not have time to react and it just oscillates which never settle.

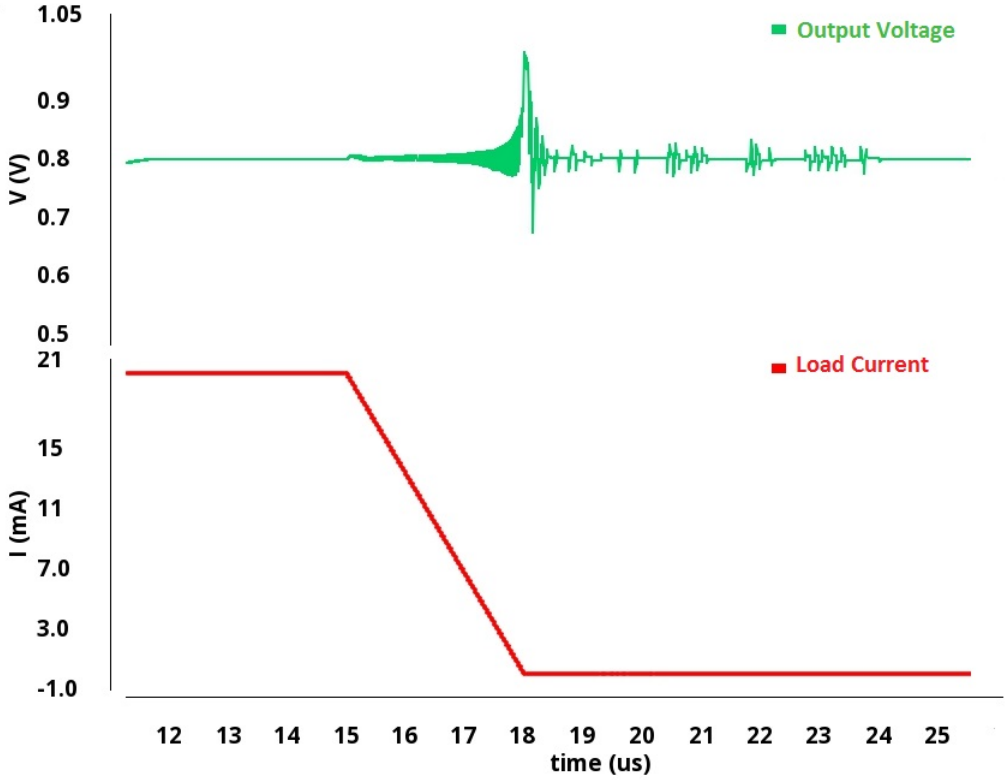

Figure 5.9: Load transient Behavior (from full load to no load)

In the line transient simulation, the input voltage was quickly changed from the 940mV to 1.04V or 1.1V to 1.2V.This LDO is stable if the power supply has the step response as shown in Fig 5.10. Line transient response is different from power-supply rejection ratio (PSRR). PSRR is a DC measurement, while a line transient is a step function containing the Fourier components of the step input voltage.

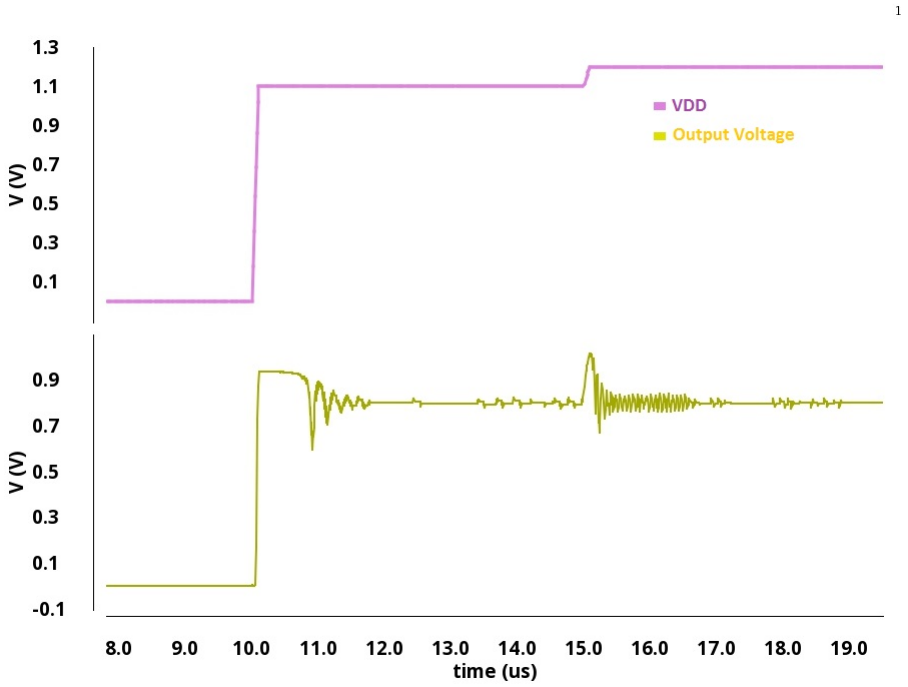

Figure 5.10: Line-transient Behavior of the proposed LDO

5.2.4 Power Consumption

Power consumption of the proposed LDO is shown in table. For both the cases when power down signal is LOW/HIGH, power consumption from each block is shown. As discussed, when the regulator is in power down mode LDO consumes the current in range of picoampere which increases to microampere range when power down signal is low.

Block	**Regulation Mode**	**Power Down Mode**
Oscillator	7.956uA	4.05pA
L-F Amplifier	3.39pA	3.39pA
PFD	12pA	12pA
Difference Detector	9.126pA	9.126pA
Charge Pump	10uA	10uA
Power MOS	70uA	949.739pA

Table 5.1: Power Consumption

Chapter 6

Conclusion

6.1 Summary and Conclusions

The objective of this thesis was to design high performance fully-integrated PLL-based low dropout voltage regulator. This design is implemented on 28nm FDSOI technology. The proposed LDO has been able to regulate the output at 800mV with the dropout voltage of 200mV.This LDO can source the maximum current of 20mA. Load regulation of 8uV/mA is achieved due to its integrator based architecture which is much better than traditional opamp based on voltage regulator. Due to digitally controlled loop the power consumption is very low which is very important for the battery in portable electronics. This novel LDO design allows a wide range of output capacitors to be used. This allows the LDO to be fully integrated in system-on-chip with no off-chip capacitor needed. In this thesis, initially we discussed the conventional LDO architecture and its performance parameters. After that, how these parameters are analyzed and measured for any voltage regulator is studied. Detailed description of FDSOI technology parameter is analyzed before designing the proposed circuitry. Advantages of FDSOI technology over CMOS bulk technology were studied and are taken into consideration while designing the circuit. In Chapter 5, we dealt with the detailed design analysis of each block in the circuit. Using behavioural modelling and simulation, we calculated the optimum component value for each block. Transistor level simulation results shows that the specifications have been met and regulator is stable under all process and parameter corners at no/full load condition. .The final characteristics of the LDO designed are presented in Table 6.1

Table 6.1: Final characteristic of the LDO

Parameter	**Measurement**
Technology	28nm FDSOI
Input Voltage	1V
Dropout Voltage	200mV
Output Voltage	800mV
Max Output Current	20mA
Startup Time	1.6us
Settling time	3.8us

6.2 Future Work

This work is based on schematic simulation. But the performance of the LDO can be varied from the schematic simulation results due to parasitic and signal routing. Thus, to evaluate the effects of parasitics and to gain a higher degree of confidence it is important to do the layout and run post-layout simulations. There are other design aspects also that future work should focus on in order to achieve a good performance, low power consumption and less area.

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