Design of GaN HEMT Broadband Power Amplifiers

by

Deepayan Banerjee

Under the Supervision of Dr. Mohammad S. Hashmi

Indraprastha Institute of Information Technology Delhi

March, 2017

Indraprastha Institute of Information Technology (IIITD), New Delhi 2017

Design of GaN HEMT Broadband Power Amplifiers

by

Deepayan Banerjee

Submitted

in partial fulfillment of the requirements for the degree of

Master of Technology

to

Indraprastha Institute of Information Technology Delhi

March, 2017

Certificate

This is to certify that the thesis titled **"Design of GaN HEMT Broadband Power Amplifiers"** being submitted by ***Deepayan Banerjee*** to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

March, 2017

Supervisor Name
Department of _____
Indraprastha Institute of Information Technology Delhi
New Delhi 110 020

Acknowledgements

This Master's Thesis has been prepared by Deepayan Banerjee at Indraprastha Institute of Information Technology, Delhi, during August, 2016 – March, 2017. I would like to thank my thesis supervisor Prof. Dr. Mohammad S. Hashmi for providing me valuable advice and help during the entire period of work. This work would not have been complete without his support. I thank Dr. Mohammad Ayatullah Maktoomi for providing me deeper insights of basic PA design, conventional techniques and references. I would also like to thank Mr. Rahul Gupta for his support in the labs. Thanks to all the authors of the papers I have referred, to the people whose webinars and lectures have helped me develop this work.

Lastly, I would like to thank my parents who have always kept enormous faith in me, have been by my side every minute of my life and blessed me with immense love. A "thanks" would not be enough!

Abstract

Power Amplifiers are undoubtedly one of the most important blocks in any transmitter system. Long range communication requires a massive boost-up of the power to be delivered, before it can be launched in the channel. This makes Power Amplifier (PA) design to be a challenging task. Recently, a lot of work regarding Gallium Nitride (GaN) PAs is going on around the globe and have drawn the researcher's interests. This Master's thesis presents a simulation based design of a 10W broadband PA, operating at the WiFi frequency of 2.4GHz. The amplifier was designed using the large signal model (CGH400010F) from Cree Incorp. Advanced Design Systems (ADS) from Keysight Technologies has been used for simulations. The designed amplifier shows a Power Added Efficiency (PAE) of 70% and delivers 38dBm (P_{del}) of power at the design frequency. The gain is measured to be above 9.5dB over the operating band.

Contents

List of figures

Abbreviations

ADS: Advanced Design System

GaN: Gallium Nitride

HEMT: High Electron Mobility Transistor

FET: Field Effect Transistor

PA: Power Amplifier

LNA: Low Noise Amplifier

NF: Noise Figure

PAE: Power Added Efficiency

P_{del}: Power delivered

RF: Radio Frequency

SDR: Software Defined Radio

CCA: Current Conduction Angle

ZVS: Zero Voltage Switching

ZVDS: Zero Voltage Differential Switching

SMT: Surface Mount Thin-film

SMD: Surface Mount Device

LPF: Low Pass Filter

HPF: High Pass Filter

IMN: Input Matching Network

OMN: Output Matching Network

ACPR: Adjacent Channel Power Ratio

EVM: Error Vector Magnitude

Motivation and Introduction

Power Amplifiers are an indispensable unit in any transmitter architecture. In any situation where power has to be transmitted over a channel to long distances, or a case which needs a boost in the operating power level, a power amplifier is absolutely necessary. Recent technological advancements, which include Software Defined Radios (SDR) to Drone Swarms, Air Traffic Control to Air Surveillance Radars, crave for a good amount of power that has to be transmitted from the transmitter to remote locations/areas of operation. Power Amplifiers boost up the feeble power levels that contain the intelligence (information of interest) before it can be transmitted through a terminal antenna. An efficient design of a PA can prove its worth in defense, communication and other related industries where efficiency needs to be achieved in hand with reliability.

Emerging transistor technologies have speeded up the development of high performance PAs. The capability to handle high power at RF and Microwave frequencies require a semiconductor material to possess the properties of large breakdown voltage and high electron velocity. Emerging technologies such as the SiC MESFETs, GaAs HBTs, GaAs MESFETs and GaN HEMTs prove to be ideal for power amplification at high frequencies.

In this thesis, the PA design is made using ADS from Keysight. GaN HEMT large signal model was obtained from Cree Incorp. The work is structured in a way that it starts with the basics of power amplifiers, transistor characteristics and types, delves deep into the required theory and finally elaborates on the simulation based design procedure. Simulation results, discussion and conclusion have also been provided at the end of the thesis.

Background and related work

The history of Power Amplifiers date back to the time between the World Wars, when there was an urgent need for Trans-Atlantic communication. Wireless communication had grown enough and all that was needed was to broaden the extent upto which messages could be sent on air. The first research paper, *"Power Amplifiers in Trans-Atlantic Radio Telephony"*, by Oswald and Schelleng [1] was presented in May 7, 1924 before the Institute of Radio Engineers, New York. Following that, *"Design of Non-Distorting Power Amplifier"*, by Kellog [2] was presented at the Midwinter Convention of the A.I.E.E, New York, on February 1925.

Designs of various Power Amplifiers came up in the early '30s depending upon their performance efficiencies and mode of operation. They were broadly classified into classes- A, B and AB. Later a new type of architecture came into existence which suggested that power amplification can also be obtained if the operating transistor can be made to behave as a switch. In fact, it would account for highly enhanced efficiency as well. Research has been going on ever since, to design PAs that serve specific purpose in a communication system.

This thesis focuses on an enhanced efficiency based PA, operating over a large bandwidth. This would find application mainly in SDRs [3], WiFi and Drone Swarms in defense equipment. Some recent works include Class-F PA design using mode transferring techniques [4], Harmonic tuned PAs [5], Class-J high efficiency PA [6] and more [7] – [12].

3. Theory

This section provides the basics of RF PAs. Their development, operating principle, characterizing parameters and limitations.

3.1. Power Amplifier- Basics:

A Power Amplifier is the last stage of a transmitter system. It is present just before the antenna (Fig. 1) to boost up the power levels of the signal before radiating it into space, and hence, PAs play a crucial role in any transmitter system. An RF power amplifiers is essentially much different from ordinary audio power amplifiers, though architectural similarity is quite obvious. The device operates at the RF or Microwave region of the spectrum and hence requires additional measures that can be neglected at audio frequencies. An RF PA basically consists of four elements (or networks, more suitably)-the transistor, the bias network, the input and the output matching networks. Added are some safety circuitry that helps preventing the device to get into regions of instability. Each of the components would be discussed in detail in the upcoming sections. Fig. 2 depicts the general architecture of a PA.

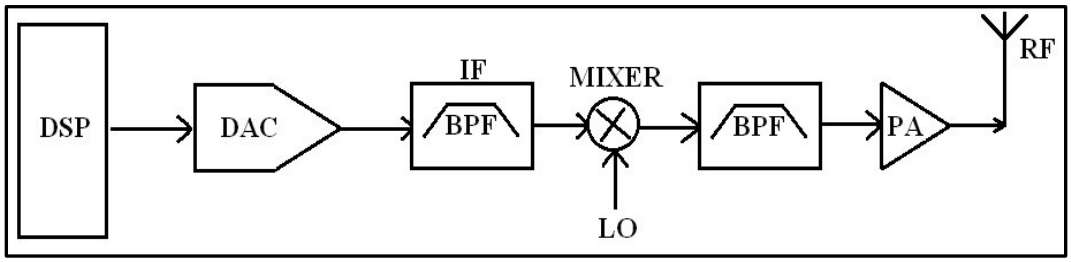


Fig. 1. Transmitter architecture

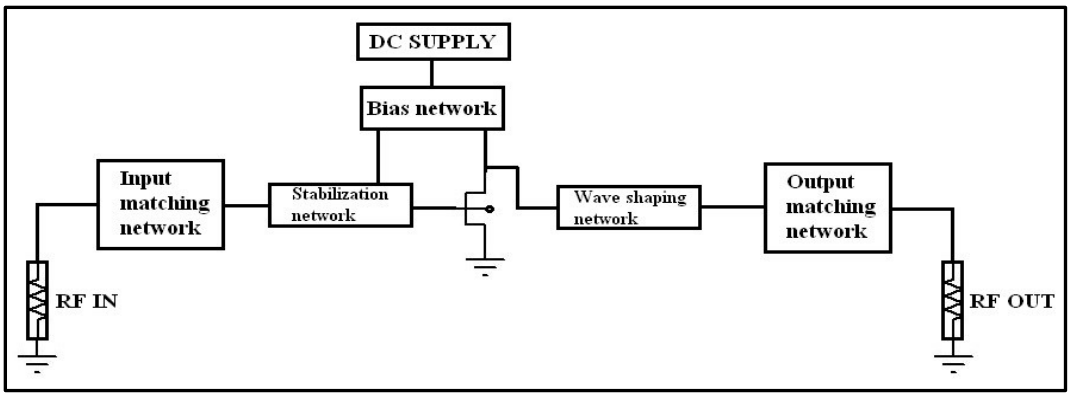


Fig. 2. General PA architecture

3.1.1. The transistor:

The heart of a Power Amplifier is a transistor that does the basic job of amplification. Depending on the purpose and utility, we choose various transistor that meet the needs. In this work, we have chosen a GaN HEMT [13] (Gallium Nitride High Electron Mobility Transistor) as the basic unit of amplification. The important properties of high power active devices are [14]:

1. High electron mobility
2. High energy band-gap
3. High thermal conductivity

Electron mobility is the criterion used to estimate the high frequency applicability of the active device. Devices with higher electron mobility provide higher gain and a good frequency response. Electron mobility in GaN depends on the condition of heterojunction formation. The metal-semiconductor heterojunction enables the formation of a quantum well where there happens to be a lot of free electrons. When these localized free electrons are set a potential, they can easily flow, thus forming a current. As these electrons are free, they can respond almost instantaneously to the high frequency of the input signal. Despite the advantages, the late emerging of GaN devices are due to the lack of a suitable substrate for GaN growth. Recently the technology for epitaxial growth of GaN on SiC has shown significant advances. Mobility of GaN is not much superior to that of Si (1600cm^2/V-s, compared to 1350cm^2/V-s for Si), but still it is used due to the fact that we can make a maximum utilization of its mobility. By employing HEMT structure, maximum mobility can be obtained because that mobility can be obtained in the absence of impurities.

The higher the thermal conductivity, the greater is the advantage in heat dissipation, and thus the device is capable to have a high-power consumption capability.

The energy band-gap is closely related to the breakdown voltage of the active device. The larger the band-gap, the higher is the breakdown voltage. Some important properties of GaN are listed below:

- Band-gap: 3.4eV (compared to 1.1eV for Si)
- Breakdown voltage: 3.5 x 10^6 V (compared to 6 x 10^5 V for Si)
- Electron mobility: 1600cm^2/V-s (compared to 1350cm^2/V-s for Si)

3.1.2. Biasing network and bias stability:

The transistor, discussed in the previous section, needs to be biased at a particular operating point for operating as an amplifier. Selecting a proper bias point is a major aspect in PA design [15] – [19]. Not only does the DC bias network determine the PAE (Power Added Efficiency), but also it defines the PA performance over temperature.

Stabilization of the DC bias network requires that the amplifier would remain within limits of its operating point, over the entire frequency range of operation. If the device fails to do so, this would disrupt the amplification resulting in unbound oscillations, degraded linearity and ultimately distorted output. The stabilization network basically prevents the PA from entering into oscillations. Oscillations are a result of an effective negative impedance at the input or output port of the PA. Generally, oscillations occur around the lower frequency side of the operating spectrum and can be avoided by decreasing the gain at that particular region.

3.1.3. Matching networks:

Matching networks are basically transformation networks that transform impedances between the transistor and the typical 50Ω input/output. These matching networks are essential for transferring maximum power from the source to the load of the amplifier. They can be designed using lumped components as well as microstrip lines (although the latter is advisable for high frequencies). The input side matching is done based on maximum power transfer which derives from the concept of conjugate matching, and accounts for low return loss [15]. It's quite evident that half of the power is lost on conjugate matching and thus very high efficiency cannot be ensured practically. The matching on the output side is done according to the needs, i.e. the class of PA designed. It may consist of harmonic peaking networks [4], [5], wave traps or some other architecture depending upon the type of the output waveforms required.

3.1.4. PA design and characterization parameters:

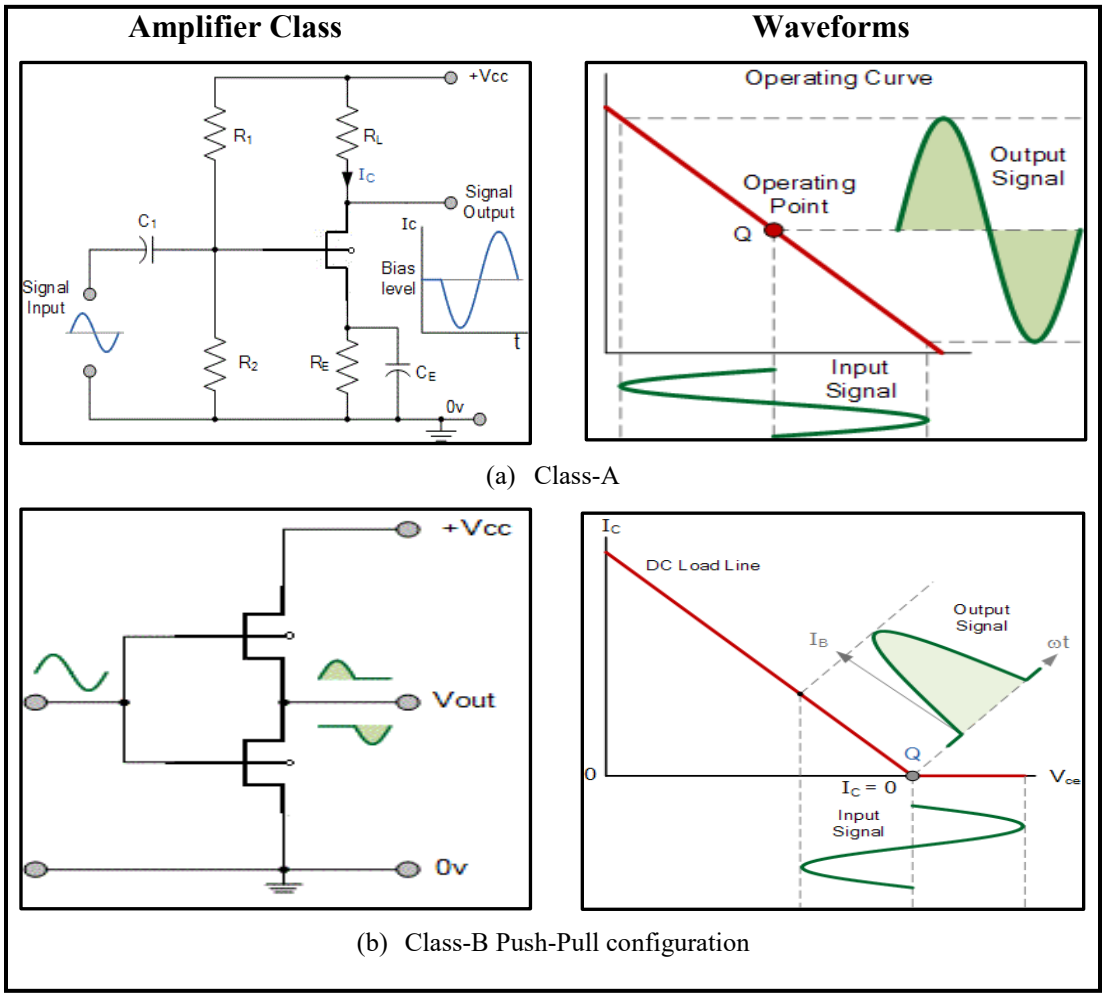
PA architectures can vary widely depending upon the application. There are a few parameters that are used to characterize the PA performance. Based on these parameters do the design procedure depend, i.e. they form the target specification for any design architecture. Efficiency is an important parameter to describe the amplifier performance. However, this metric finds use in low power, and hence, small signal amplifiers. Efficiency is defined to be the ratio of the output RF power to the input DC power ($\eta = P_{RF_{out}}/P_{DC}$). In other words, it can be stated as how much DC power the amplifier is able to convert to RF power (This is also called the Drain Efficiency of the PA). Focus has always been to improve the efficiency of any amplifier because an improved efficiency device requires less DC power to be supplied into it and hence extends the battery life.

The problem of the above definition of efficiency comes into picture when the input signal is not small anymore. For large signals, a better defining metric, Power Added Efficiency (PAE) is used. PAE = $\frac{P_{RF_{out}} - P_{RF_{in}}}{P_{DC}}$ takes the input RF power into account and can be described as, how efficiently the amplifier is able to convert DC power to RF power. This is the main reason why PAE forms the most important describing parameter for RF PAs, and would be discussed in detail in this thesis. PAE also tells us about the gain that can be provided by the PA. Higher value of PAE signifies higher gain. With the DC power (P_{DC}) remaining constant, an increase in PAE increases ($P_{RF_{out}} - P_{RF_{in}}$), and hence the gain.

Another important metric in defining PA performance is the 1dB compression point. When the input power level of the amplifier is low, the gain is constant and has a linear behavior, but as the input power level becomes high, the output signal saturates and no longer varies linearly with the input signal. In other words, the linearity behavior fails to take a stand. The input power level at which the amplifier shows 1dB lesser linear gain than usual, due to saturation, is called 1dB compression point and is a very important metric in defining linearity of a PA.

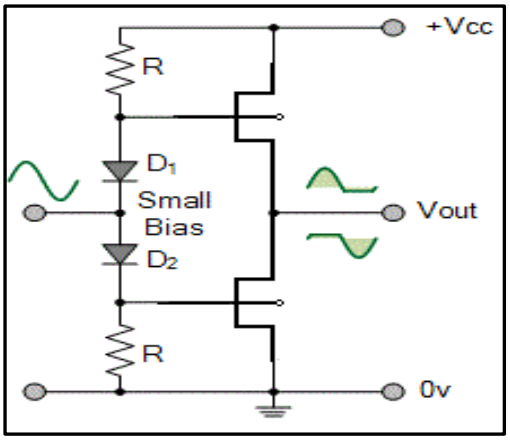
3.2 Power Amplifiers- types and classification:

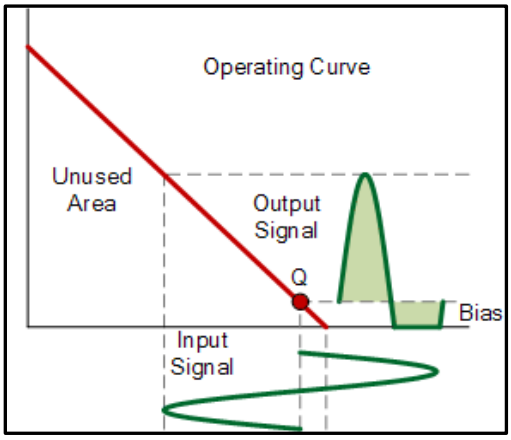
Power Amplifiers are broadly classified into two types- linear and non-linear PAs [20]. Linear PAs produce output power which is proportional to the input power and generates a negligible amount of harmonic power. On the other hand, non-linear PAs have their output signal not in proportion to the input signal and generates a considerable amount of harmonic power besides the fundamental signal. Furthermore, these can be combined in two categories- the bias class PAs and the switching class PAs. The bias class PAs operate on the active region, has a defined bias point and a good linearity, whereas switching class PAs operate at the edge of cut-off, produces a lot of harmonics and hence, fall in the class of non-linear amplifiers. Further based on the current conduction angle (CCA), bias class amplifiers are classified into Class-A, Class-B, Class-AB and Class-C amplifiers.



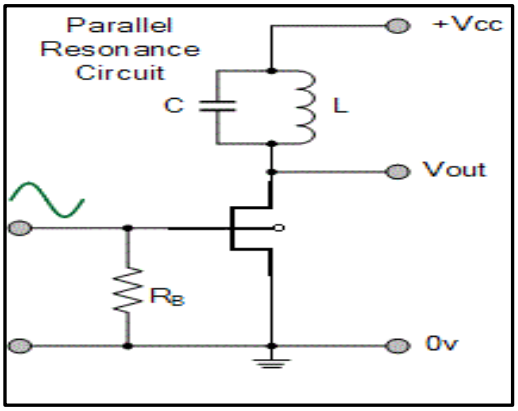
(a) Class-A

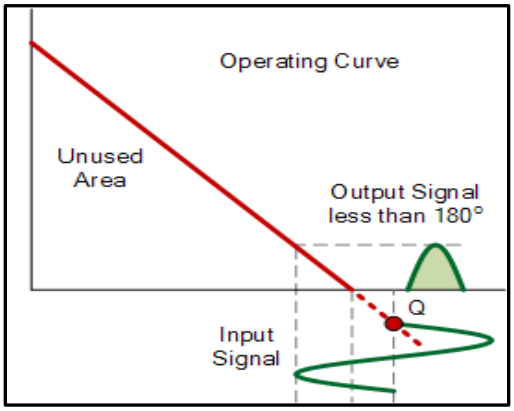
(b) Class-B Push-Pull configuration



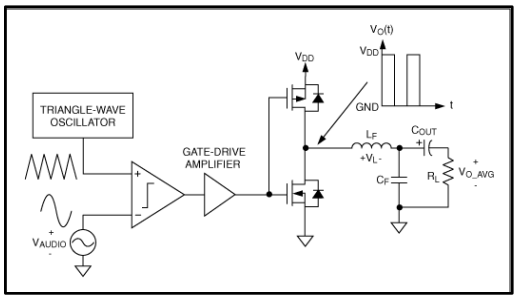


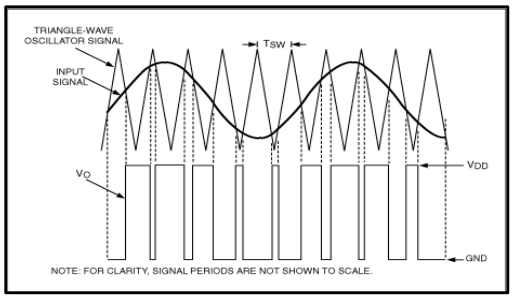
(c) Class-AB Push-Pull configuration



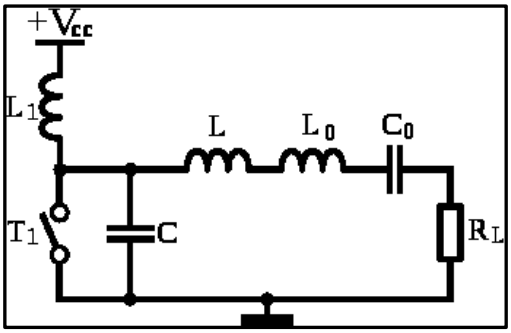


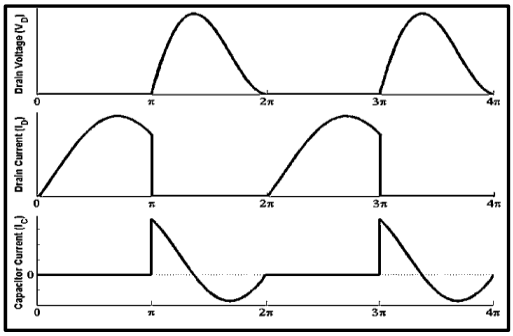
(d) Class-C



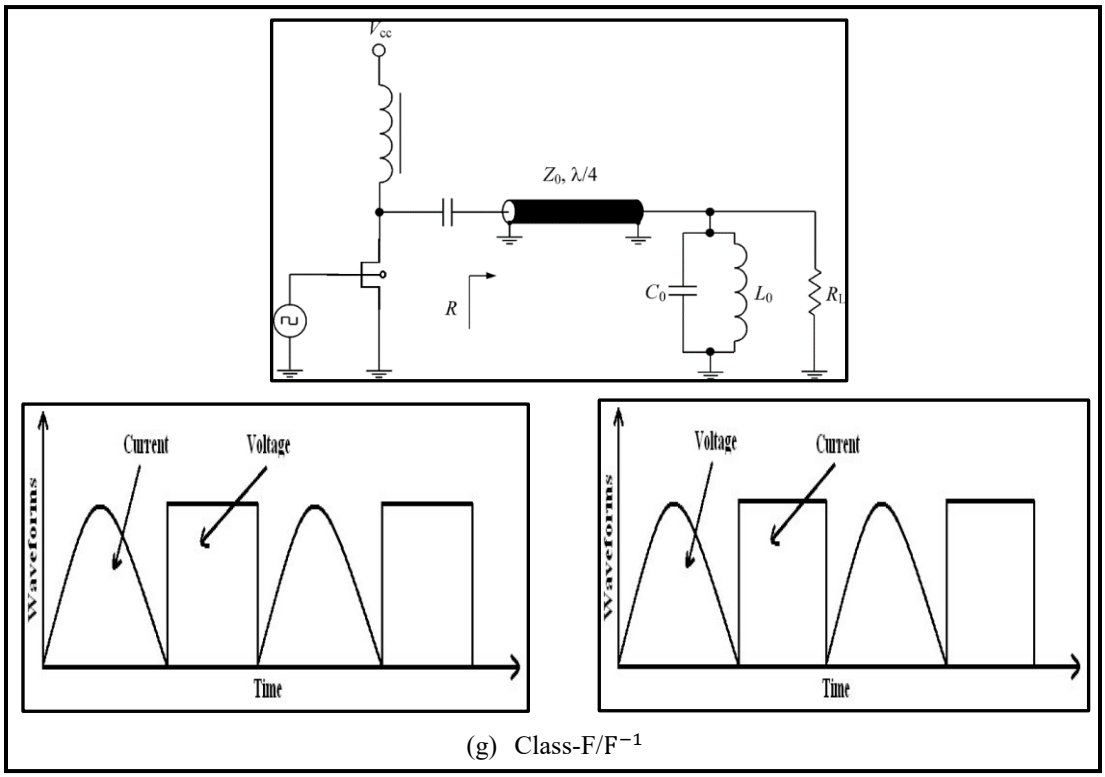


(e) Class-D





(f) Class-E



(g) Class-F/F^{-1}

Fig. 3. Classes of Power Amplifiers- circuits and waveforms [35]

3.2.1. Biasing class amplifiers:

As it's quite evident from the title, these classes of amplifiers operate on a particular bias point. The transistor conducts for the entire cycle (or most of it) of the input wave and thus they are always ON (or OFF for only a short time). The further classification of this class is done based on how much time the transistor is remaining in the conductive state (in other words, the conduction angle). They are discussed in the forthcoming sections.

3.2.1.1. Class-A amplifiers:

In Class-A, the transistor is biased exactly at the middle of the load line so that the device conducts for the entire cycle of the input signal (current at the output flows for the entire cycle of the input signal). Thus, the conduction angle happens to be 360°. As the bias point is exactly at the middle, there is no question of the transistor switching OFF any time during operation. So, linearity is maximum in this class. Owing to the property of always being ON, amplifiers of this class consumes a large amount of DC power. Fig. 3(a) shows a class-A amplifier circuit along with its output waveform. Though class-A amplifiers have a very good high frequency response, but they are not one of the good choices due to its lowered efficiency. The theoretical values of efficiency limits to 50%, the practical being much less. Power dissipation in the form of heat also happens to be a major drawback of this class as bulky heat sinks should be used. Thus, although having a good linearity and simple architecture, this class is avoided while designing a high-performance PA.

3.2.1.2. Class-B amplifiers:

These classes of amplifiers also operate on a fixed bias level which is lower than that of class-A, near the deep cut-off region. In this biasing scenario, the transistor conducts only on the half-cycle of the input drive signal. This accounts for a current conduction angle (CCA) of 180°, and a better efficiency than its class-A counterpart [22]. As the transistor conducts only for one cycle, thus we get abrupt termination in waveforms, and hence generation of higher order harmonics. This degrades the linearity performance of the class-B amplifiers. The poor linearity of this class can be improved by using two transistors in the push-pull configuration- each of them switches ON at alternate cycles thus contributing to the full cycle. However, one disadvantage of the push-pull configuration is that for a very small time, both of the transistors remain cut-off. This leads to a condition called cross-over distortion which again deteriorates the linearity of this class. Anyway, the reduction of conduction angle by lowering the bias point elevates the theoretical efficiency of this class to be 78.5%. Fig. 3(b) depicts a class-B PA.

3.2.1.3. Class-AB amplifiers:

This class can be considered as a compromise between classes-A and B in terms of linearity and efficiency- something in between [22]. As shown in Fig. 3(c), the bias point lies in between the bias points of class-A and B, i.e. somewhere between the middle of the load line and the deep cut-off region. This improves the efficiency of this class as the conduction angle is reduced, but still it is lower than 78.5%, as the CCA is between 180° and 360°. In class-AB amplifiers, the cross-over distortion is reduced and hence there is an improvement in linearity [23]. In many push-pull configurations, both the transistors are applied a gate bias such that they don't go to cut-off at the time of half-cycle switch-over. This avoids cross-over distortion. For the same saturation distortion, the maximum output power is somewhat less for class-A than for class-AB, but for class-A, it is not possible to get as high linearity as one wants by reducing the maximum used output power, which is not possible for a realistic class-AB amplifier. However, it is more linear than class-B.

3.2.2. Switching class amplifiers:

Unlike the bias class amplifiers, the switching class amplifiers are not based on any bias point. All of them operate at the cut-off region and hence are inherently in the OFF state. This happens to be a big advantage as idle-state power consumption reduces to a great extent. Depending upon the cycles they conduct and the time for which the conduction takes place, they can be further branched into class- C, D, E, F and F^{-1}. They are discussed in further sections.

3.2.2.1. Class-C amplifiers:

This is another modification of amplifier biasing where the bias point is kept below the pinch-off. Thus, the transistor, by nature, remains OFF and thus consumes very little power ideally. It conducts less than 50% of the time and correspond to a

CCA < 180°. It has a higher efficiency than classes-A, B and AB amplifiers but shows the worst linearity amongst them. Fig. 3(d) shows a class-C PA.

3.2.2.2. Class-D amplifiers:

Mostly used in audio amplification, class-D amplifiers can be considered as a high-power signal generator, which uses switching to get high efficiency. The input signal consists of constant amplitude pulse train that switches the transistor ON and OFF between conductive and non-conductive states. The input signal to be amplified is converted into a series of pulses by Pulse Width Modulation (PWM) or other techniques, as shown in Fig. 3(e). Post-amplification signal reconstruction is done using low-pass filtration.

3.2.2.3. Class-E amplifiers:

These classes, mainly E and F, have their operation depending on the configuration of the networks connected at their input and outputs. They are mainly based on the concept of wave shaping [24], [25]. The active device, i.e. the transistor simply acts as a switch that turns ON and OFF with a duty cycle of 50%. In this aspect, the concepts of Zero Voltage Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS) should be well understood. In amplifiers, power loss occurs only when both the current and the voltage waveforms overlap each other. The amount of power dissipated is in proportion with the area of total overlap. ZVS accounts for zero voltage when the transistor is switched ON and ZVDS can be defined as the condition of 'zero overlap' or no overlap between the current and voltage waveforms, so that no loss occurs. For implementing these conditions, reactive components are utilized in the output network. Fig. 4 below shows the operation of a class-E amplifier. The transistor, denoted as the active device, acts as a switch. C_p is the shunt capacitor that models the transistor intrinsic parasitic capacitance and the capacitance of the circuit. A series resonator is realized by C_s and L_s that resonates at the fundamental frequency. The series resonator allows only the fundamental signal to the load. At the ON state of the transistor, capacitor C_p will be charged. As it turns OFF, L_s and C_s, in series with R functions as a damped oscillating circuit, and C_p is discharged through the resistive load R [25]. Fig. 3(f) shows the voltage and current waveforms of the class-E amplifier. The current and the voltage waveforms are present alternately at the OFF and ON periods and thus theoretically there is no overlap. This accounts for 100% efficiency ideally.

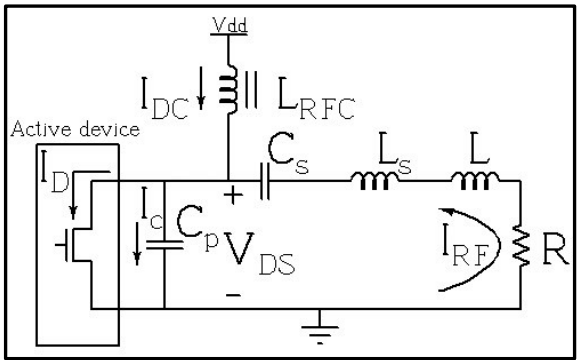


Fig. 4. Class-E operation

The efficiency of class-E amplifiers being 100%, it is quite alluring to design these and put to use. But there are some disadvantages associated with class-E operation. Firstly, design at high frequency is a big concern as the shunt capacitance C_p assumes a very high value. This limits the operating frequency and the ability to deliver high output power at elevated frequencies. Secondly, the knee voltage required to turn on the active GaN device is relatively high as compared to the ON state current (V_{knee} is approximately 5V for GaN transistors). As both voltage and current waveforms are present during switching, the ZVS assumption described earlier, cannot be implemented successfully for class-E amplifiers. To attain ZVDS, these amplifiers require a fast input switching drive signal, which indeed increases stress for the transistor [25]. These limitations are not present in class-F or F^{-1} amplifiers and hence draws the attention of PA designers.

3.2.2.4. Class-F/F^{-1} amplifiers:

Class-F amplifiers are considered to be the most effective of them all. They use the concept of ZVS and ZVDS to control the output current and voltage waveform overlap by designing harmonic terminations in the output network. By this process, the harmonic powers are reflected back and directed toward the fundamental tone thereby increasing the level of the output power delivered (and thereby increasing the efficiency). Theoretically, these classes of amplifiers are able to perform at an efficiency of 100%, but that is not possible in practice because for that, an infinite number of harmonics need to be controlled, which is physically not feasible. Circuits can be designed that control upto 3rd harmonic, and moreover going higher up makes little difference as those higher harmonics contain very less amount of power. The criteria for zero waveform overlap (and hence zero power dissipation) is that the drain voltage should be a perfect square wave and the drain current should be a 180° shifted half-sine wave [26]. Fig. 3(g) shows the output waveforms of the class-F amplifier.

Research till date has mostly been done on the design of the output network of class-F amplifiers. Focus has not been given toward the input network. The input is not that critical in PAs because they are the last component in any transmitter block. As a matter of fact, (following the Friis equation, App. D), the PA has to have a very good output matching and that is the main reason why a lot of attention has been given there. But recent research studies show that there has been substantial improvement in the PA performance with an input 2nd harmonic peaking network. The drain voltage and current waveform equations are given below as [15]:

$$V(t) = V_{dd} + V_1 \cos(\omega_0 t + \phi_1) + V_2 \cos(2\omega_0 t + \phi_2) + V_3 \cos(3\omega_0 t + \phi_3) + \cdots$$
$$I(t) = I_{dd} + I_1 \cos(\omega_0 t + \phi_1) + I_2 \cos(2\omega_0 t + \phi_2) + I_3 \cos(3\omega_0 t + \phi_3) + \cdots$$

Fourier analysis of drain current and voltage waveforms:

The drain current has to be a truncated half-sine wave in order to attain the property of zero overlap. The Fourier coefficients are listed below as:

$$a_0 = \frac{1}{\pi}$$

$$a_n = \frac{2}{\pi}\frac{(-1)^{\frac{n}{2}+1}}{n^2-1}$$

$$b_n = 0$$

As discussed earlier, the drain voltage should be a perfect square wave, and for that to be true, following are the Fourier coefficients:

$$a_0 = \frac{1}{\pi}$$

$$a_n = 0$$

$$b_n = \frac{2}{\pi}\frac{(-1)^{\frac{n}{2}+1}}{n}$$

Where, a_0 is the DC term, a_n and b_n are the even and odd harmonics respectively. As evident from the above formulations, for the drain current, all odd harmonics should be eliminated in order to have a truncated half-sine wave with only even harmonics. On the other hand, to have a perfect square wave, all the even harmonics should be removed. Fig. 5 depicts the case of an ideal class-F output waveform in comparison to a case in which the 2nd harmonic has been controlled. Needless to say, the more the harmonics are controlled, the more the waveforms would tend to the ideal case of a square voltage and a truncated half-sine drain current.

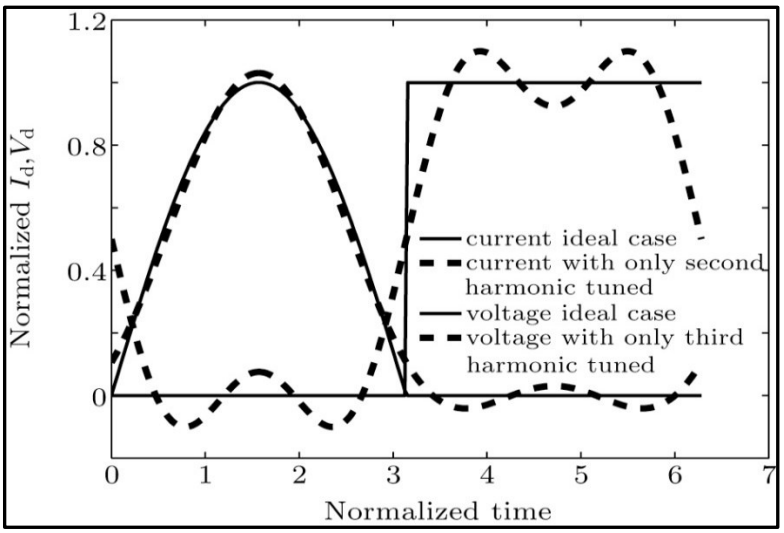


Fig. 5. Class-F ideal vs harmonic tuned output waveforms [34]

Class-F^{-1} amplifiers:

The main difference between class-F and F^{-1} amplifiers is that the latter has square drain current waveform and truncated half-sine drain voltage waveform in the output. Rest, everything is same as class-F and so it can be said to be the dual of class-F amplifiers. All higher order even harmonics are terminated into an open

circuit (or infinite impedance) and the odd harmonics are terminated in short circuit (or zero impedance)- just the opposite of what is done for class-F operation.

Harmonic terminations at the output:

Harmonic impedance terminations are the heart of class-F design as they are solely responsible for trapping and directing the harmonic power into the fundamental frequency. The desired harmonic terms, that are required for waveform shaping, are provided an open circuit at the drain so that their power can be trapped and directed toward the fundamental frequency. The unwanted harmonics (again that needs to be eliminated for waveform shaping) are terminated in short circuit at the drain. Thus, the power associated with these unwanted terms can easily be reduced. As obvious, the waveforms of class-F^{-1} would be opposite to that of class-F amplifiers. The output impedances are written below for simplicity:

$$Z_{2n} = 0, Z_{2n+1} = \infty, \text{ for class-F}$$
$$Z_{2n} = \infty, Z_{2n+1} = 0, \text{ for class-F}^{-1}$$

Where *n* is the order of the harmonic for which the impedance is calculated.

The 3rd harmonic peaking configuration:

Even if the class-F amplifier theoretically claims to have an efficiency of 100%, but designing a harmonic termination network that controls infinite harmonics are practically not possible. Thus, a practical class-F amplifier is limited to 80% efficiency with only a finite number of harmonics controlled.

The high frequency signals would leak through the transistor channel and be shorted to the ground because of the drain-source parasitic capacitance C_p [15]. Hence, higher order harmonics do not play a crucial role in determining the waveform shape and PAE as well. This drain-source capacitance is a major factor that limit the upper frequency of operation of the transistor. The schematic below shows the simplified output network. Practically only the 2nd and the 3rd harmonics can be controlled instead of infinite harmonics. Next is present the wave trap that is basically the impedance network for the harmonics as discussed earlier. In many architectures, this network is merged with the output matching network, but functionally it is not the same as a matching network. The impedance of the wave trap circuitry adds up with the amplifier impedance obtained earlier and that total impedance has to matched with the output port. Thus, it is always a good practice to keep these two networks separate, at least for intuitive clarity.

The class-F topology is classified based on the highest order harmonic that can be controlled [15]. If the output waveforms are controlled upto the 3rd harmonic, it is called a 3rd harmonic peaking (or a 3rd harmonic injection amplifier). In this thesis, a 3rd harmonic peaking class-F PA has been designed. Fig. 6 below shows the simplified configuration of a class-F 3rd harmonic peaking amplifier. The parallel resonator composed of $L_3||C_3$ resonates at the 3rd harmonic frequency and thus acts as an open circuit to the 3rd harmonic frequency but allows all other frequencies to pass through it. In the process, the 3rd harmonic power gets reflected back. The parallel resonator following it, composed of $L_1||C_1$ resonates at the fundamental frequency. This blocks the fundamental frequency and allows all other frequencies

to be shorted to the ground. In the ideal case, no harmonic power reaches the load (which is a 50Ω resistive termination). Another circuit configuration can be implemented as shown in Fig. 3(g). It uses a quarter wave micro-strip transmission line at the fundamental frequency and a parallel resonator (resonating at fundamental frequency) following it. The $\lambda/4$ line provides a 180° phase shift to all the odd harmonics while keeping the phases of the even harmonics constant. This is still a theoretical concept and cannot be implemented in practice because the $\lambda/4$ transformer shows inductive behavior as the frequency increases which makes an imperfect transformation from open to short. It is also assumed that the parallel resonator with the load has an infinite Quality factor (Q), which is practically impossible, as follows from the expression: $Q = R\sqrt{\frac{C}{L}}$. For an infinite Q, C and L should be very high and very low respectively.

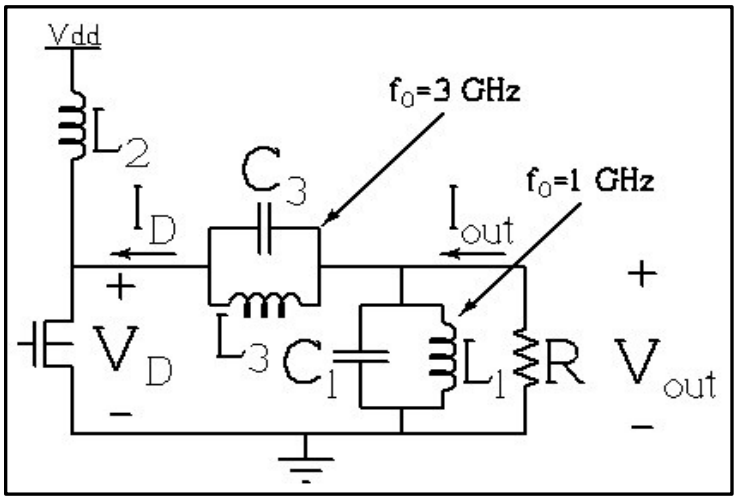


Fig. 6. 3rd harmonic peaking class-F operation

Class-F PAs can be implemented in two ways- by using lumped components and by distributed components. Owing to its reduced size, although designing PAs with lumped components seems to be alluring, but at higher frequencies, it is not advisable to do so (and not possible either). This is because inductors assume very small value (in pH range) and it is hard to find components with such values. This would make the design of the high-Q resonator rather difficult. In fact, as the frequency gets higher and higher, lumped elements tend to be leaky and their performance degrades. This compels us to switch to PA design using distributed elements (more specifically microstrip lines). In this thesis, except for a few biasing components and protective circuitry, microstrip lines have been used in the entire design. The matching networks and the wave shaping networks are all designed in microstrips and their performance plots have been provided separately.

4. PA design components

This section would discuss in detail all the components that were utilized for the designing of a class-F 3rd harmonic peaking broadband PA. They are described in sub-sections below.

4.1. 10W GaN HEMT from Cree Incorp.:

This is the transistor or the main active device that perform the task of amplification. It is a 10W GaN HEMT from Cree Incorp. with the model no. CGH400010F, suitable for high frequency and microwave applications (Fig. 7(a)). The software package is basically a large signal model that comes with schematic prints for easy incorporation in ADS schematics. Given below are the special features of the device [13]

- 28V operation
- Operation availability upto 6GHz
- Small signal gain of 16dB at 2GHz
- Small signal gain of 14dB at 4GHz
- Saturated power of 13W and 65% efficiency at saturation

This device finds use in 2-way private radio, broadband amplifiers, cellular infrastructure, test instrumentation and linear amplifiers like class-A, AB etc. suitable for OFDM, W-CDMA, EDGE and CDMA waveforms. Given below is a comparison table of all the semiconducting materials:

TABLE- I: Comparison of different semiconducting materials [15]

Material	μ (cm²/V-S)	ϵ	E_g(eV)	T_{max}
Si	1300	11.4	1.1	300°C
GaAs	5000	13.1	1.4	300°C
SiC	260	9.7	2.9	600°C
GaN	**1500**	**9.5**	**3.4**	**700°C**

Gallium Nitride shows superior performance than the others and hence is a criterion for choosing this material to build HEMTs. The electron mobility for GaAs is much higher than GaN but still GaN is used because of its wide bandgap. The bandgap of GaN is 10-20 times higher than GaAs and hence GaN components are much smaller and exhibit lower capacitance than GaAs counterparts. Also, the ability to withstand high voltages is greater in GaN than in GaAs.

4.2. Rogers RT5880 Duroid substrate:

In this thesis, Rogers RT5880 Duroid substrate has been used (Fig. 7(b)). It is a frequency stable substrate with low loss. Some important characteristics are listed below:

- ϵ_r= 2.2
- Relative permittivity= 1
- Substrate thickness= 1.575 mm

- Conductor= 2-sided copper (thickness 35μm)
- Conductivity of Cu=5.8e7 S/m
- Loss Tangent= 0.0009

4.3. Resistors:

Surface Mounted Thin-film (SMT) resistor from Dale series has been used in the design (Fig. 7(c)). They come in 0603 footprints and have a tolerance limit of $\pm 1\%$ to handle high power.

4.4. Capacitors:

Johnson R14S JTI0603 component is used as capacitor in this thesis (Fig. 7(d)). These capacitors provide very high Q-factor performances. Like the SMT resistors, they too come with 0603 footprints and are convenient to place on one layer (the top layer) of the board. The capacitor can be modeled as shown in Fig. 8 below.

The ceramic capacitor is modeled as a basic series RLC circuit having a reference of 50Ω. In the model, C denotes the actual capacitance of the component whereas, L denotes the factors responsible for propagation delay and losses [27].

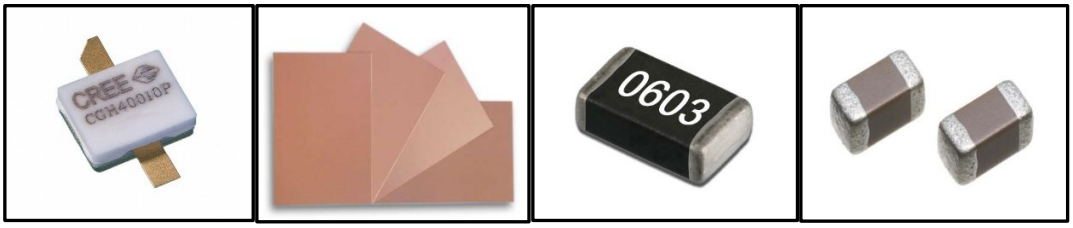


Fig. 7. (a) Cree GaN HEMT (b) Rogers RT Duroid 5880 (c) SMT resistor 0603 (d) SMD capacitor 0603

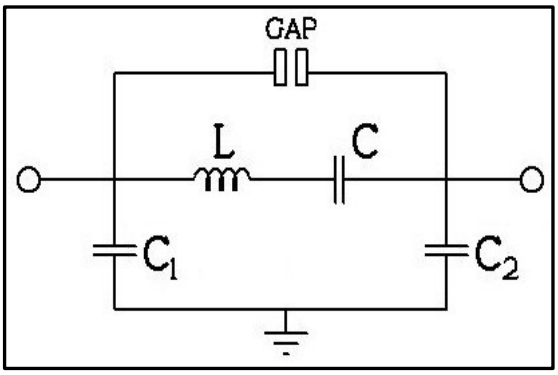


Fig. 8. Circuit representation of the SMD capacitor

5. ADS based design

This section onward deals with the design of the class-F broadband PA in Keysight's Advanced Design System (ADS) environment [21]. It elaborates sequentially, the steps one should undergo to design a PA that has a maximum PAE and delivers > 10W of power with good linearity at the design frequency.

5.1. PA design flow:

The PA design flowchart is shown in Fig. 9 below.

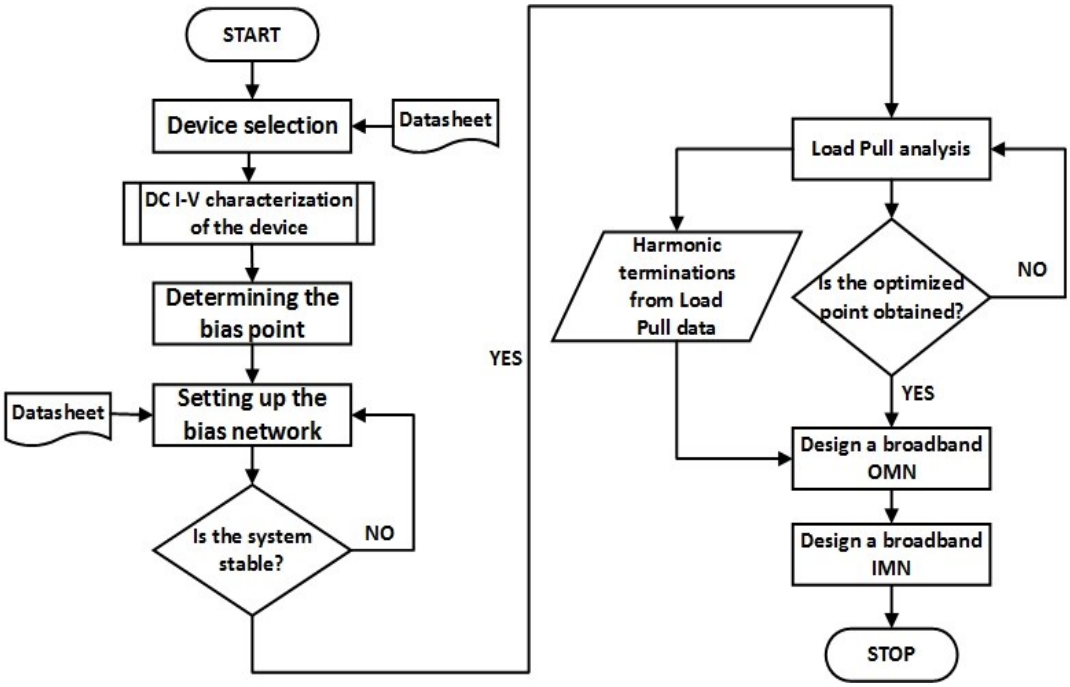


Fig. 9. PA design flow

The steps would now be discussed in detail.

5.1.1. Determining the bias point:

As discussed earlier, it is crucial to determine the bias point at which the transistor would be operating. This is done by performing the DC I-V tests on the device. The GaN HEMT model is tested on the FET Curve tracer test-bench of ADS as shown in Fig. 10.

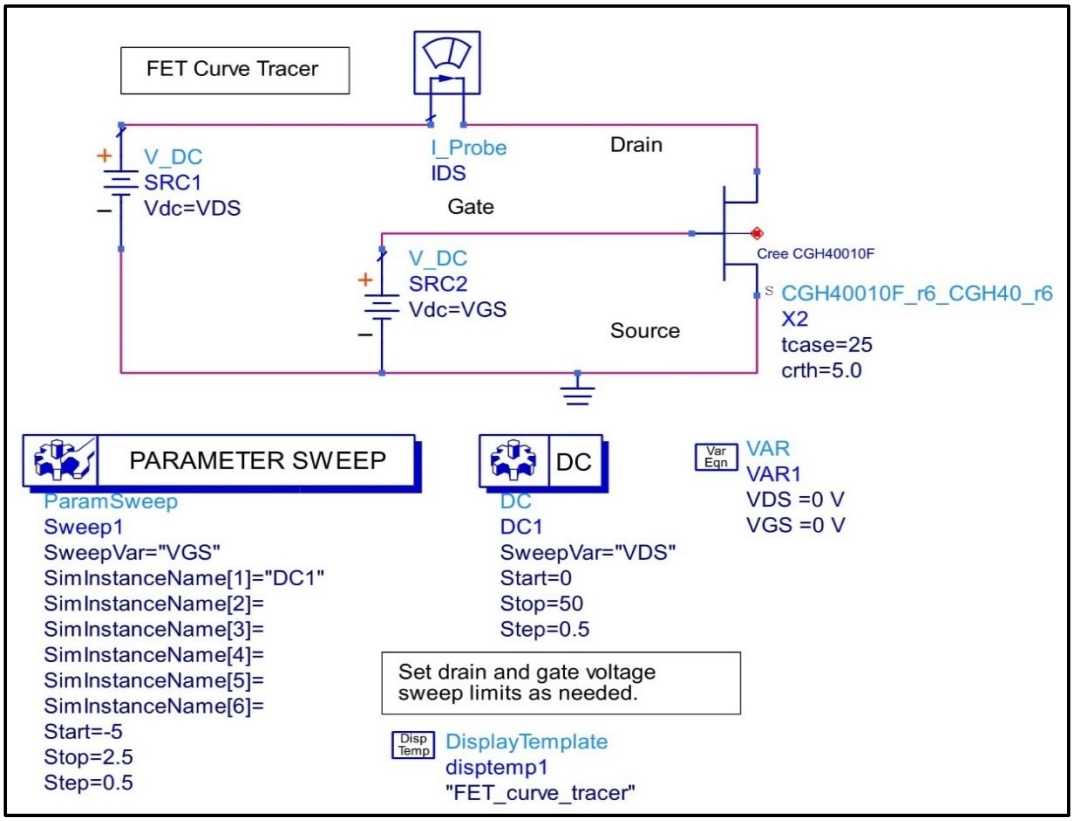


Fig. 10. Setup to determine the DC I-V characteristics

On simulating, the results are obtained as shown in Fig. 11.

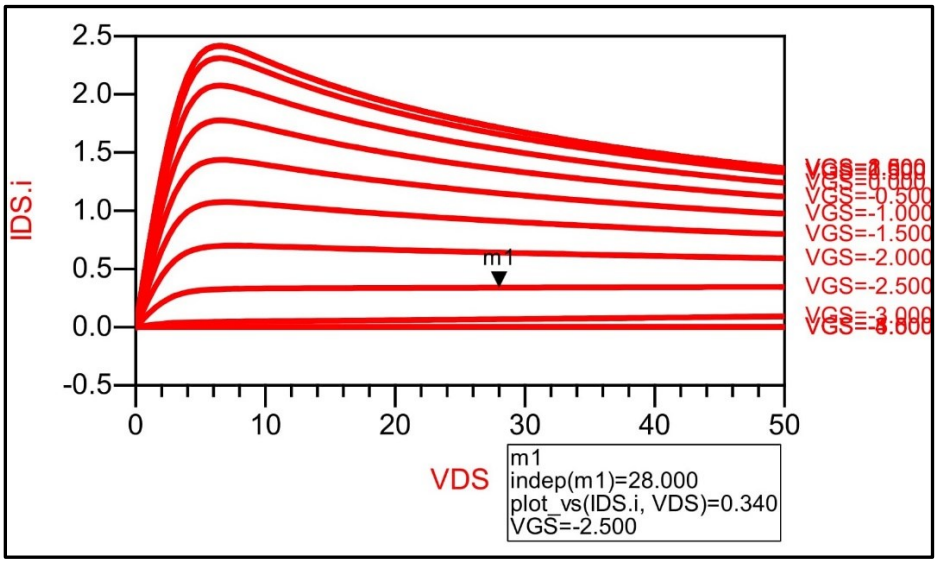


Fig. 11. Obtaining the DC bias point

Referring the datasheet, the device has been biased at a point shown by marker m_1. It corresponds to V_{DS} = 28.0V, V_{GS} = -2.5V and provides a drain current of 340mA. As evident, the bias point is very close to the cut-off region and is ideal for class-F performance.

5.1.2. The bias network:

For the transistor to operate successfully for amplification of the input signal, it has to be biased, i.e. its drain and gate voltages has to be fixed. Determination of the bias point is one of the most important thing in PA design as the operating class depends upon where we set up the bias point. Now the bias network should be designed in such a way that it delivers the required DC current and voltages on one hand, but on the other hand, it should provide a high impedance to the RF signals (the fundamental along with the harmonics) [27]. This is of utmost importance because otherwise, the RF signal would leak through the DC bias network into the supplies and would damage them. The bias network is designed with a $\lambda/4$ microstrip transmission line that provides a very high impedance at 2.4GHz, and functions as RF choke (or DC feed network). As a broadband PA is being designed, microstrip butterfly stubs would be used instead of simple open stubs. Butterflies have a good bandwidth performance and as they have a gradual flaring, they reduce the undue effects due to fringing and parasitics [28].

Once the biasing details have been obtained, the next step would be to design the network that provides the required I-V parameters to the transistor. The concept of a simple bias-tee has been used. The circuit consists of a simple $\lambda/4$ microstrip transmission line followed by a butterfly (MBSTUB)as shown in Fig. 12.

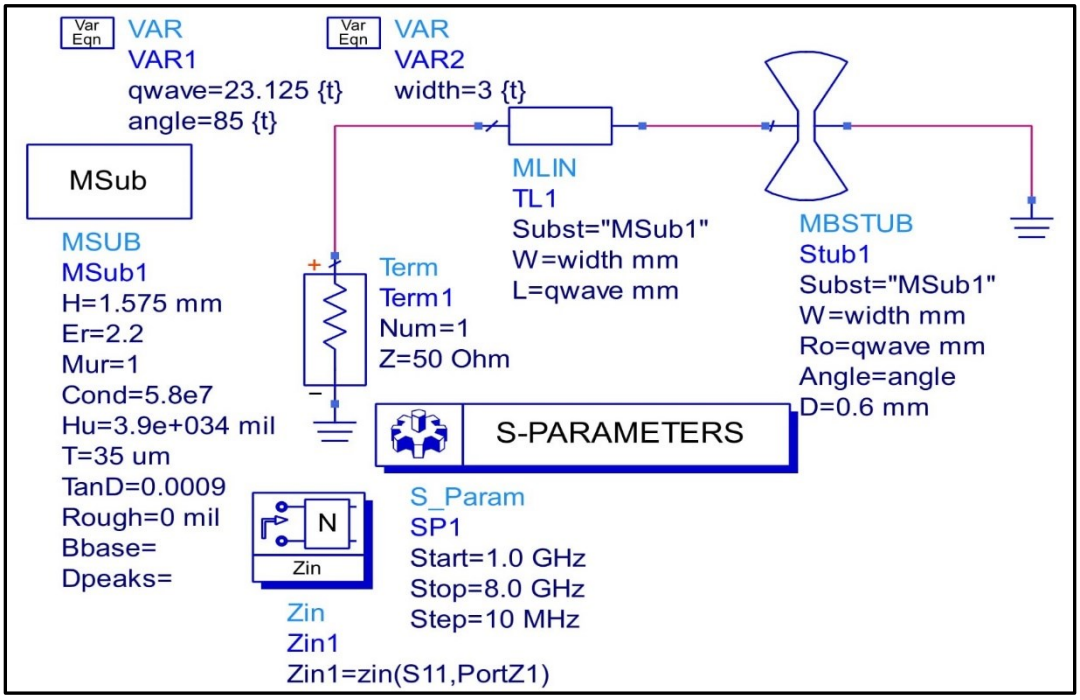


Fig. 12. Simple biasing circuit transistor

The length calculations are done in the LineCalc utility of ADS [31]. For full wave calculation, the schematic is shown below in Fig. 13.

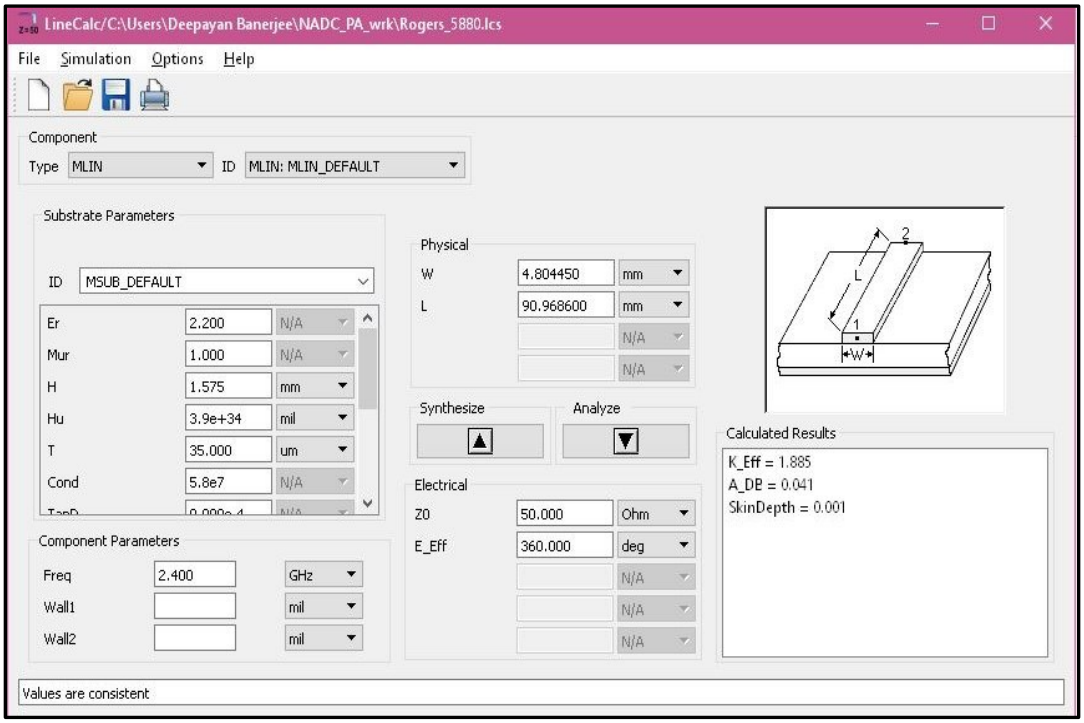


Fig. 13. LineCalc window for full wave dimension calculation of the bias-tee

Tuning is done to obtain the desired characteristics of the network. The result of the simulation is shown in Fig. 14.

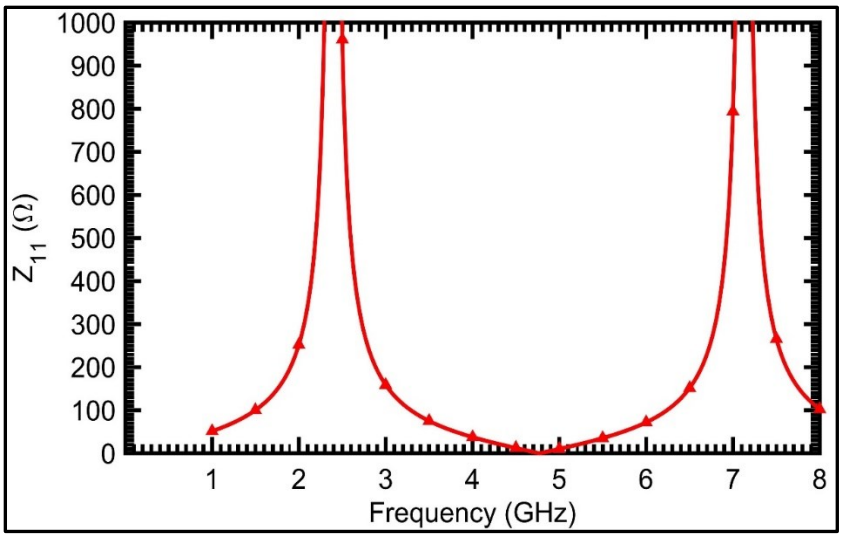


Fig. 14. Impedance characteristics of the bias-tee network

As evident from the result, the bias-tee network provides an open circuit (practically16,710.945Ω) to f_0 and $3f_0$ and a short circuit to $2f_0$. Thus, no power can leak through the bias network and damage the costly power supplies. Other higher order harmonics beyond $3f_0$ are not considered because the design is limited to 6GHz as the transistor fails to respond beyond that limit. The next step would be to stabilize the bias network.

5.1.3. Stabilization of the bias circuit:

It has been discussed earlier that stability is one of the most important criteria for amplification to take place, and is a big concern. Oscillations (instability) is possible if either the input or the output port impedance has a negative real part.

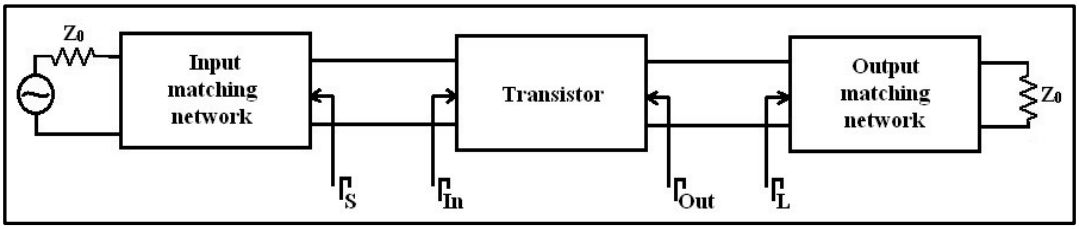


Fig. 15. Stability criterion for Power Amplifiers

It implies as $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$ for a particular range of frequencies. Because Γ_{in} and Γ_{out} depends upon the source and the load matching networks, the stability of the amplifier depends upon Γ_S and Γ_L as presented by the matching networks. So, stability can be obtained if the following two conditions are satisfied simultaneously:

- $|\Gamma_{in}| < 1$ and
- $|\Gamma_{out}| < 1$

If the above conditions are true for the entire frequency range of operation, then the PA is said to be unconditionally stable. If these hold true for a certain range of frequencies, then the amplifier is said to be conditionally stable [15].

An important method to test the stability of the amplifier is to undergo the $K - \Delta$ test. K is called the Rollet's stability factor which is calculated from a set of S-parameters at the design frequency. Δ is another parameter that is chosen to simplify derivations- a mathematical entity having dependency on S-parameters. They are listed under as:

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + \Delta^2}{2|S_{12}||S_{21}|}$$

The two necessary and sufficient condition for stability are discussed below as:

Unconditional Stability: An amplifier is said to be unconditionally stable if for all passive load and source impedances, the input and output impedances produce a positive real part. In terms of $K - \Delta$ analysis, the condition $K > 1$ and $|\Delta| < 1$ should hold true for the entire frequency range of operation.

Conditional Stability: If the above $K - \Delta$ condition doesn't hold true for a specific frequency range, then at those frequencies, the amplifier would produce a negative real part at the input or output network, thus leading to instability and hence, oscillations. Stability generally degrades at the lower end of the operating frequency spectrum and hence tests must be done over the entire frequency range of operation. Fig. 16 shows the stability analysis of the bias network designed (without a compensation network).

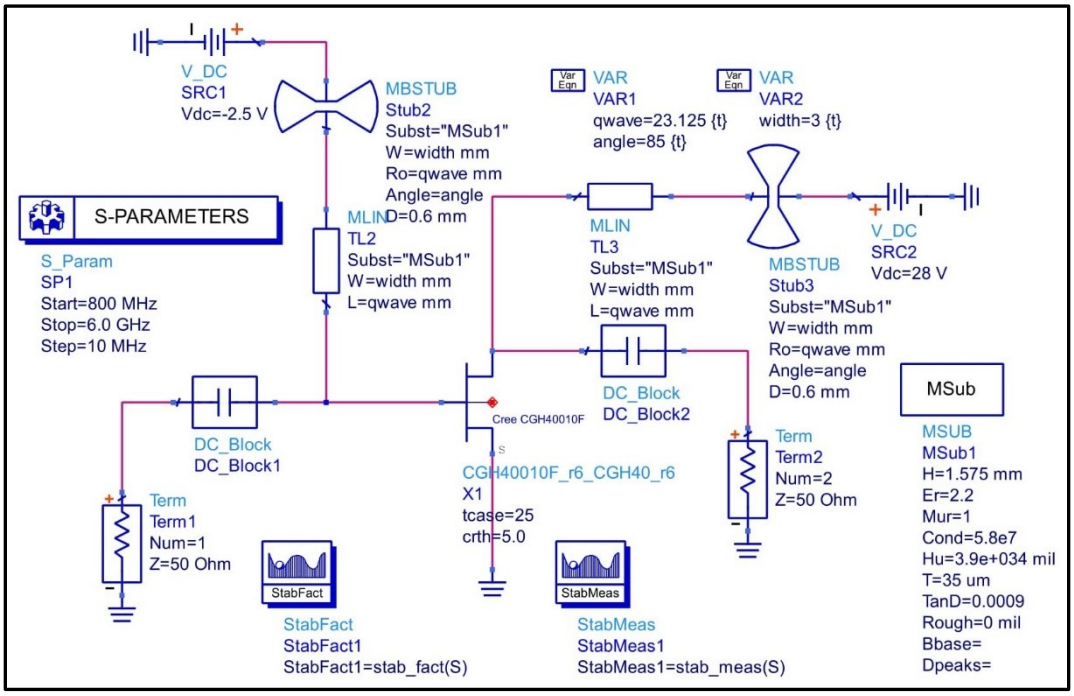


Fig. 16. Testing the bias circuit without stability networks

The gate is applied a voltage of -2.5V and the drain, 28V, according to the bias conditions obtained earlier. The bias-tee, composed of the butterfly (MBSTUB) and the $\lambda/4$ microstrip transmission line forms the DC feed that supplies the gate and the drain of the transistor. Two DC chokes are applied (DC_Block) each at the input and output of the transistor that prevents the leaking of DC into the signal generator. A point should be noted that this setup does not contain any stabilization circuit and the motive is to study the frequency behavior of the bias network without the same. The circuit is simulated over the entire frequency range of operation, viz. from 800MHz through 6GHz. Stability factors K and μ are studied (μ stability criterion is a recently proposed stability criterion well suitable for use in simulators owing to its computational convenience. It declares a system to be stable over a frequency range if the condition $\mu > 0$ holds true without exception). The results are given in Fig. 17.

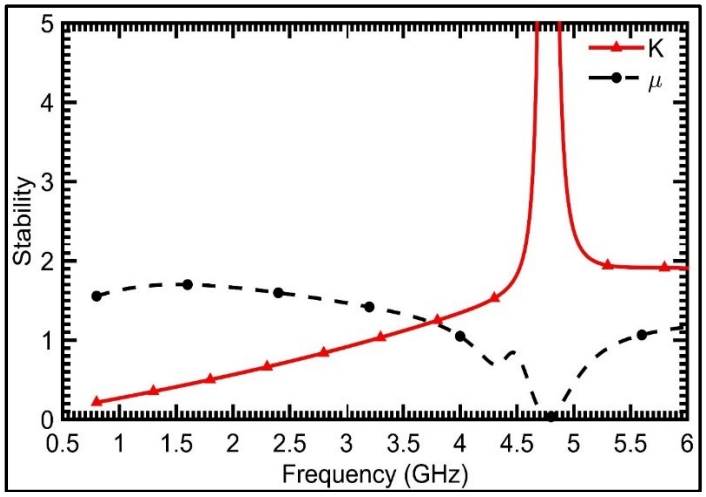


Fig. 17. Stability test without the bias stabilization network

It is evident from the results that the bias becomes unstable below 3GHz and again around 4.7GHz. Thus, we can say that the amplifier would not be 'unconditionally stable' at those frequencies. The next section would discuss about designing the bias stabilization network.

Bias stability networks:

The type of bias stabilization network required depends upon the application, i.e. the device that is targeted to stabilize. For instance, on stabilization of an LNA, resistive stabilization is not used as it degrades the Noise Figure (NF), whereas in case of PA design, a lossy resistive stabilization can be used as noise issues are not considered. Generally, to get an optimum performance, a combination of these are used [19].

Two stabilization networks find great use in modern circuits. They are discussed in detail below along with their simulation performances and results.

Parallel RC stabilization network:

It is a parallel RC network behaving as a High Pass Filter (HPF) thereby introducing loss and hence, stability for the lower frequency components whereas passing the higher frequency components unattenuated. The network is shown in Fig. 18 below.

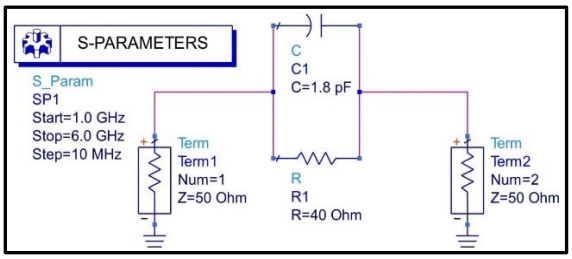


Fig. 18. Parallel RC stabilization network

Series RC stabilization network:

This network consists of a series RC circuit behaving as a Low Pass Filter (LPF). It introduces loss in the high frequency components, thereby inducing stability to the higher frequency components while passing the lower frequencies undisturbed. Fig. 19 below illustrates the series RC stabilization network.

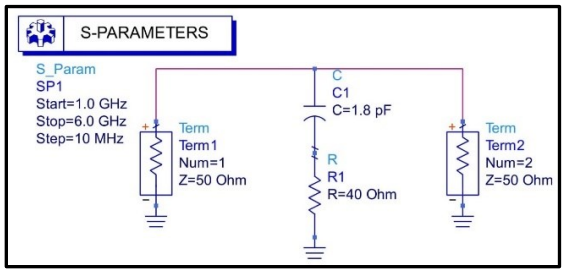


Fig. 19. Series RC stabilization network

The responses of these networks are shown in Fig. 20. The S_{21} response for each clearly shows an improvement in the behavior of the unstable portions.

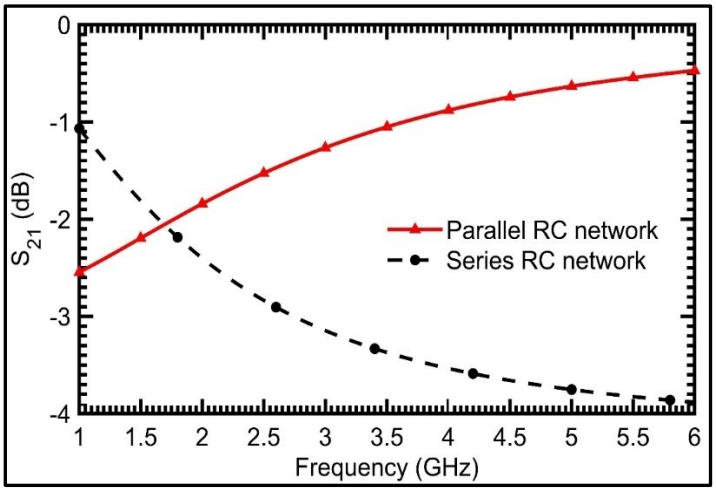


Fig. 20. Responses of the parallel and series RC stabilization networks

Now the parallel stabilization network was incorporated into the bias circuitry and stability analysis was done. This shows an improvement in the stability performance and as is evident from Fig. 22, that the amplifier behaves unconditionally stable at the operating frequencies. The final bias circuitry (tuned subsequently according to the stability criterion) along with stabilization networks are illustrated in Fig. 21. The DC blocks have been replaced with capacitors whose values are tuned accordingly.

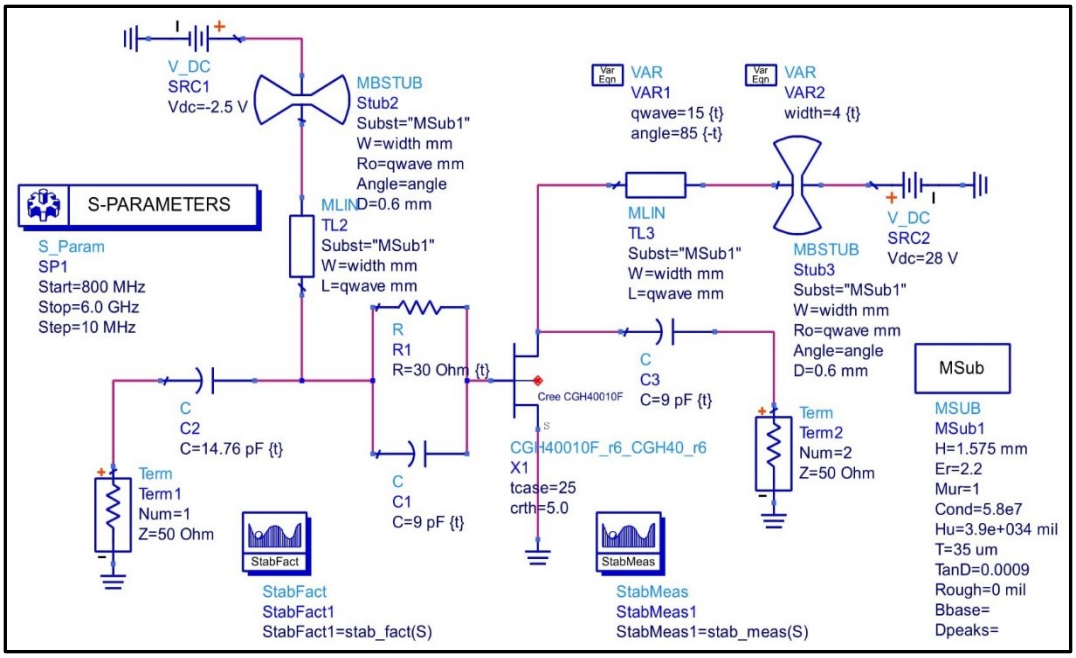


Fig. 21. The bias circuitry along with stabilization network

The levels of K and μ are kept around 1.3-1.8 and 1-1.2 respectively. It should also be noted that these values should not be kept excessively high as they introduce losses to a great extent which degrades the gain, and subsequently, the PAE of the amplifier.

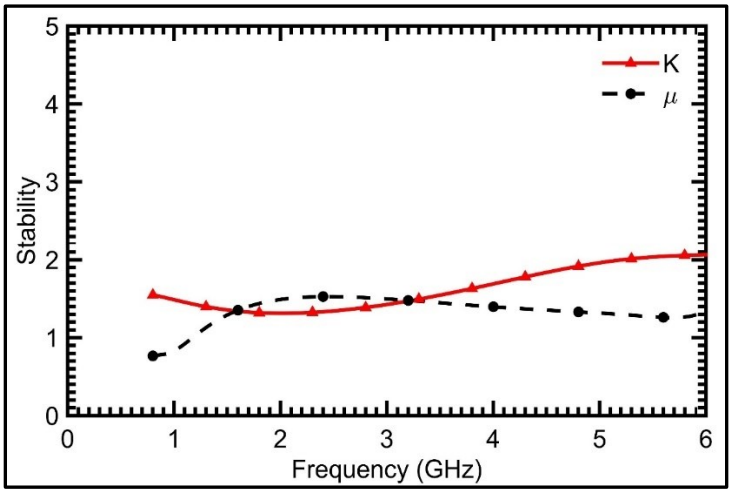


Fig. 22. Stability performance after incorporation of the bias networks

5.1.4. Load pull analysis:

Load pull analysis can be said to be the heart of PA design. This is the most important step towards designing a high efficiency PA and should be done with utmost care. This technique determines the optimum value of the load impedance that should be provided to the amplifiers output in order to have maximized PAE, optimum power delivered, gain and linearity. Fig. 23 shows a diagrammatic description of the load pull procedure. The load reflection coefficient Γ_L is defined as, $\Gamma_L = \frac{Z_L - Z_{out}}{Z_L + Z_{out}}$. Now, the input impedance as seen from the load side toward the amplifier, Z_{out} is fixed and cannot be altered. Thus, it is evident that the load reflection coefficient Γ_L becomes a function of the load impedance, Z_L [29]. Any variation in the load impedance would vary the load reflection coefficient and that is the basic philosophy behind the Load Pull technique. Basically, the simulator varies the load impedance over a selected area on the Smith Chart and plots contours having various values of PAE and P_{del}. The optimum point is determined by the intersection of the PAE_{max} and $P_{del_{max}}$ contours. In case of no intersection, the point of most proximity is chosen to be the optimum impedance point. The load pull analysis setup is shown in Fig. 24. The harmonic impedances are provided so as to obtain the square drain voltage and a truncated half-sine drain current. These conditions are imposed and then an area is chosen in the Smith chart where the load sweep would take place. This area has to be wisely chosen keeping in mind that it happens to be the determining factor behind the optimum performance of the PA.

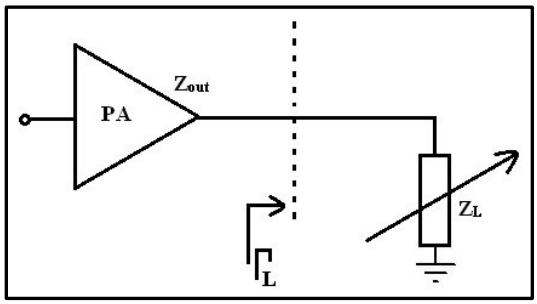


Fig. 23. Load Pull technique- basic idea

Steps to perform Load Pull analysis:

The load pull measurement refers to the measurement of an active device's efficiency or output power by varying the load impedance by an impedance tuner (either implemented in software or a physical tuner for a bench setup). This is done simply because the optimum load impedance cannot be found out from the small signal S-parameter model. Two tuners are present- the input and the output tuner. The source and the load impedances are tuned under a given input power to obtain the optimum output power [29].

- The input tuner is first adjusted to deliver maximum power from the signal source to the input of the active device, after which the output tuner is adjusted to deliver maximum output power to the load.
- Once the adjustments are completed, the impedance tuners are disassembled and the desired load and source reflection coefficients $\Gamma_{L,opt}$ and Γ_S are obtained by measuring the impedances of the impedance tuners.
- The spectrum analyzer and the power meter connected to the output impedance tuner make it possible to measure the exact value of the output power while simultaneously observing the output spectrum in the spectrum analyzer.
- In case of lower harmonics, the optimum load impedances can be obtained easily. However, a problem does occur when the harmonic impedances are to be considered.
- In general, the maximum output power is determined from the load impedance of the fundamental frequency but the efficiency varies according to the harmonic load impedance as is evident from the load pull results in Fig. 25 and Fig. 26.

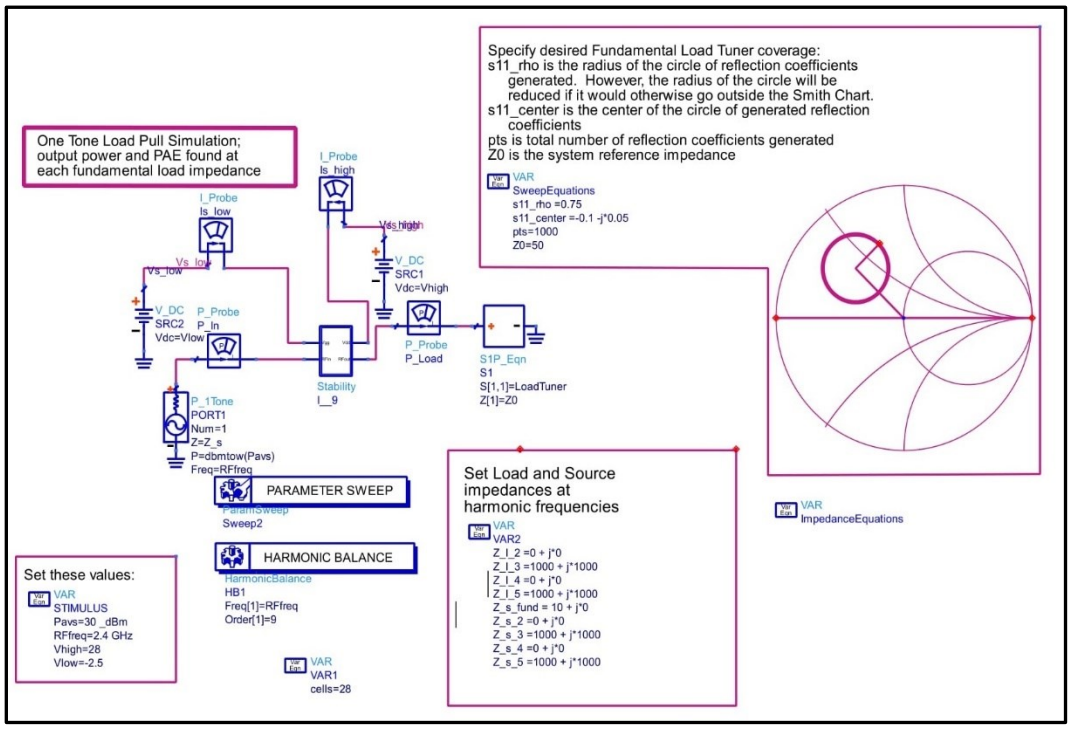


Fig. 24. Load Pull setup with harmonic terminations included

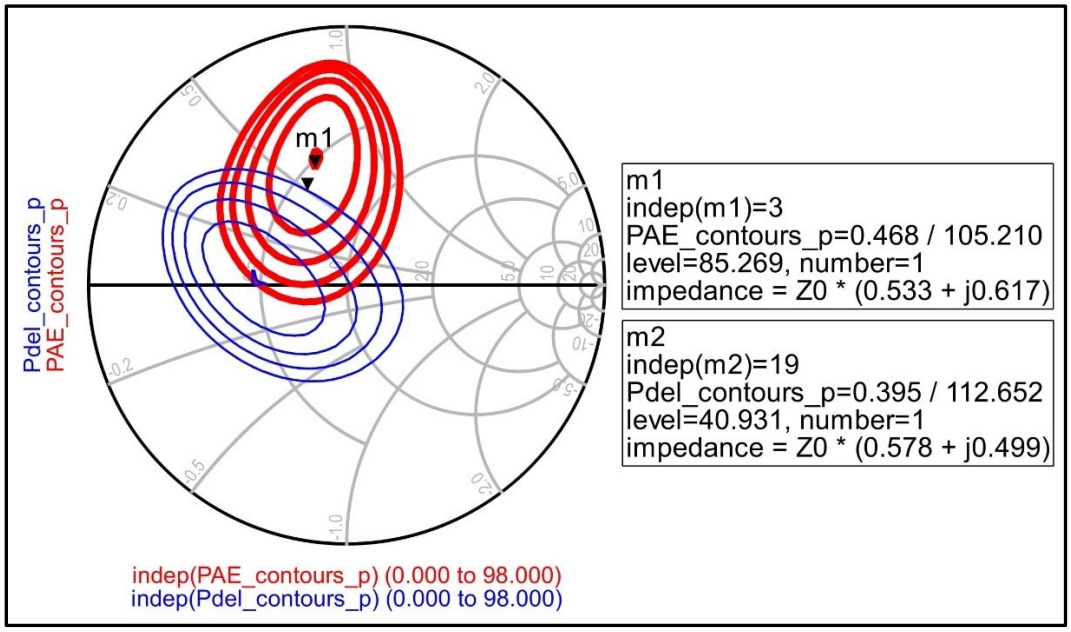


Fig. 25. PAE and P_{del} contours obtained from load pull analysis

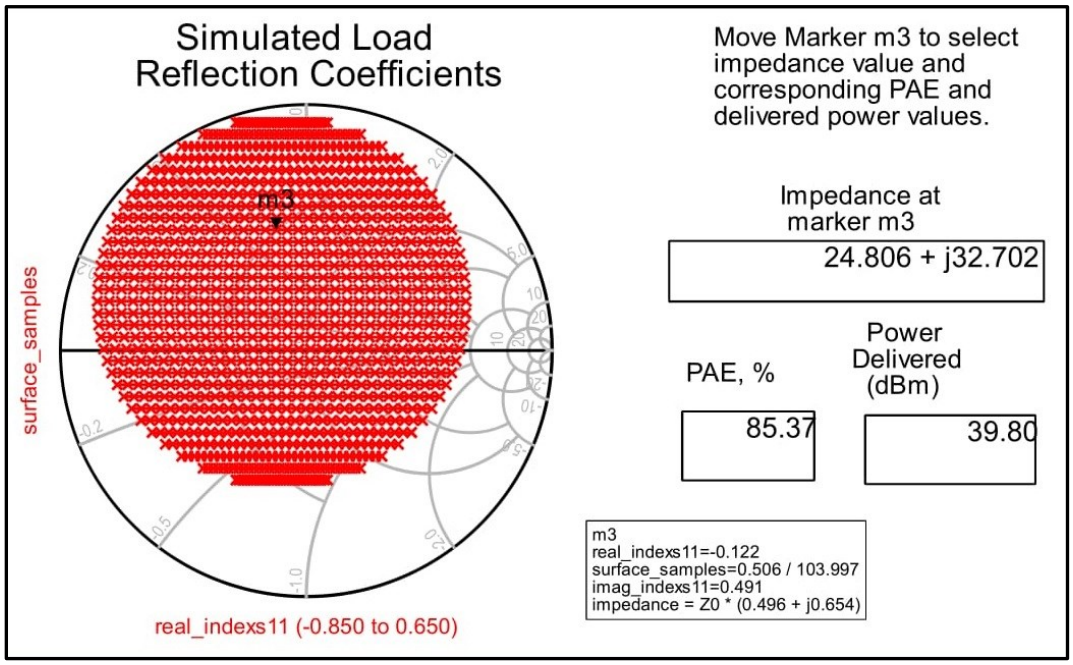


Fig. 26. Optimum impedance Z_{opt} obtained as shown by marker m_3

As seen from the load pull data, the impedances have been swept over the area shaded in red. Contours for PAE and P_{del} have been drawn over the same range of impedances. The best possible PAE that could be achieved was 85.37% with an approximately 40dBm of power. Once the optimum point has been determined, the next important task would be to design the output matching network that matches a 50Ω standard impedance to this value. The same is done using the Smith Chart utility of ADS and is described in the next section. [Detailed results of the Load Pull analysis have been provided in App. A]

5.1.5. Design of a broadband output matching network:

Matching topologies exist in literature that match a complex impedance to real load [32] – [33]. In this thesis, a simple wide-band matching has been used which works on the principle of admittance cancellation. Fig. 27 shows the Smith Chart matching utility that designs the output matching network.

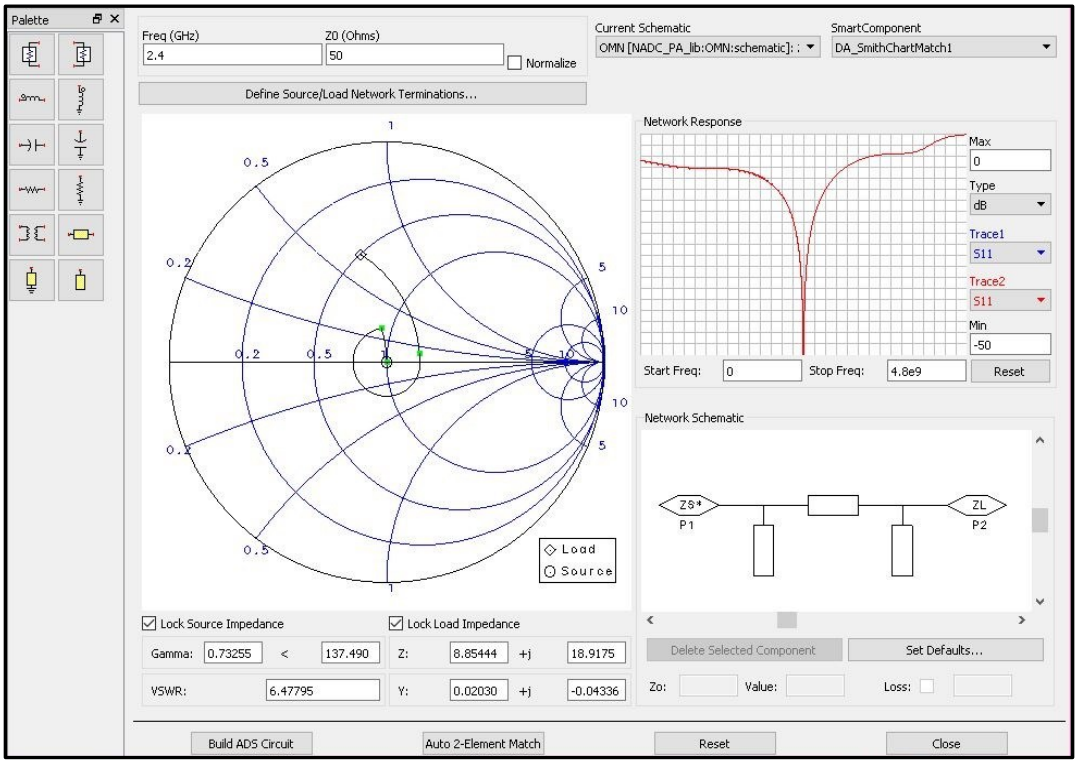


Fig. 27. Smith Chart utility for designing the output matching network

Upon designing the network, it is connected to the drain of the amplifier. The matching and the bandwidth results are provided in Fig. 28.

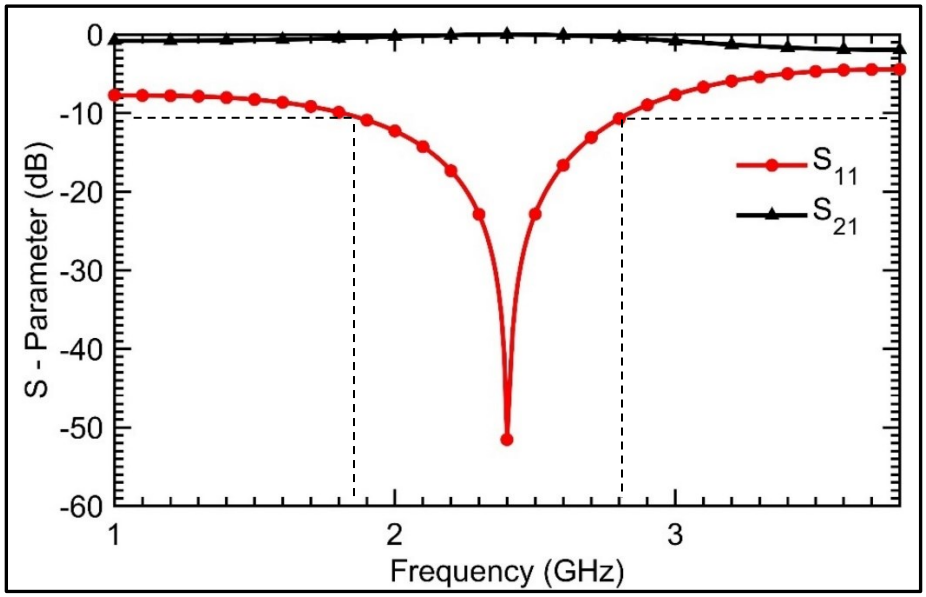


Fig. 28. S – Parameter response of the designed OMN

From the results, it can be noted that the matching levels are well around -50dB and the through power levels are also good. It transfers all the power at the design frequency and is a bit lossy at higher frequency, but that loss is well within 1.3dB. The operating principle of the output matching network is discussed in the next section.

Operating principle of the broadband OMN:

The designed OMN works on the principle of imaginary susceptance cancellation followed by transformation of the real conductance (or impedance) into the 50Ω load. Fig. 29 depicts the operation of the output matching network.

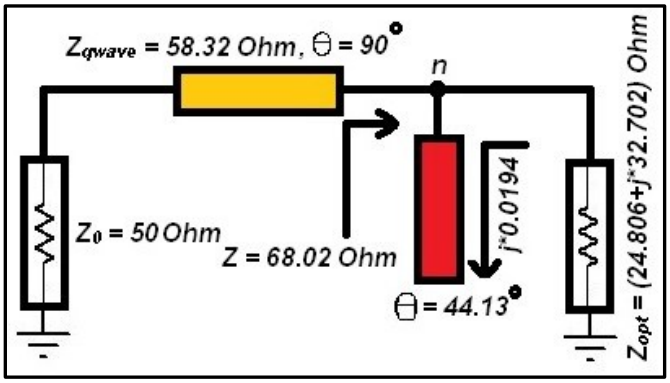


Fig. 29. Output matching network operation principle

The load is fixed at the Z_{opt} obtained from the load pull analysis. This is a Frequency Dependent Complex Load (FDCL) and hence can be represented in the general form of $R + jX$, where, R and X is the resistance and reactance of the FDCL respectively. As evident from the structure of the matching network, dealing with admittances would be easy and hence, an open stub is introduced. The admittance of the open stub cancels the admittance of the FDCL on the right of the node 'n'. After the admittance cancellation, a purely resistive load is observed at the left of node 'n', whose value is denoted by Z. This is then matched to the 50Ω termination by utilizing a quarter wave impedance transformer. It may be noted that in lieu of bandwidth increment, it is advisable to use slow wave structures (which are basically repeating structural patterns composed of open stubs and transmission lines). A tradeoff has to be made between device size and the length of the slow-wave structure used.

5.1.6. Design of a broadband input matching network:

After designing the output matching network, now attention has to be focused to design the input matching network. For this, the source pull technique has to be undergone. Source pulling is similar to load pull except that in this case, the load impedance is fixed and the source impedance is swept across a selected area on the Smith Chart. The optimum point is found out again and the input matching network is designed based on that impedance point. The source pull setup is similar to the load pull and is provided in Fig. 30.

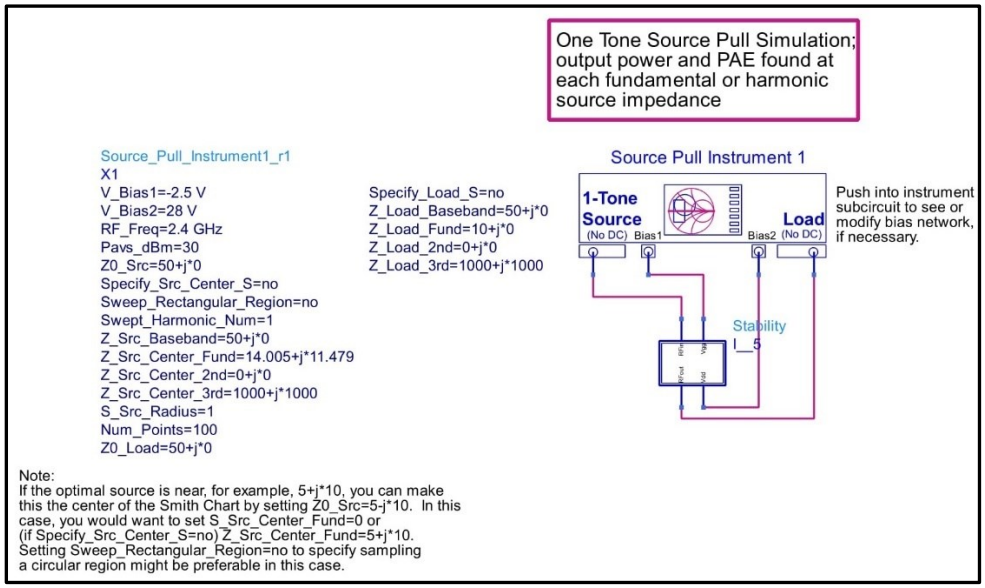


Fig. 30. Source pull setup

The simulation results for this setup are shown in Fig. 31 below.

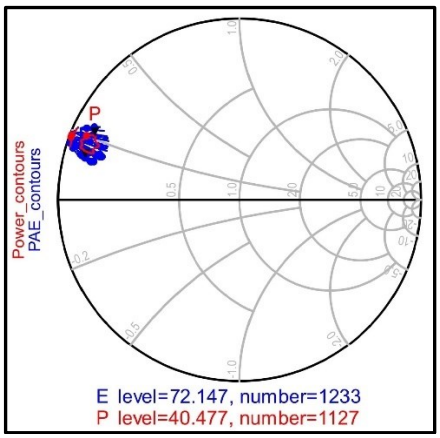


Fig. 31. Source pull results

The marker P correspond to the optimum Z_{in} point and the value corresponds to $Z_{in} = (5.200 + j * 7.577)\Omega$. The IMN is designed based on a similar configuration as the OMN. The input matching performance is provided in Fig. 32 below.

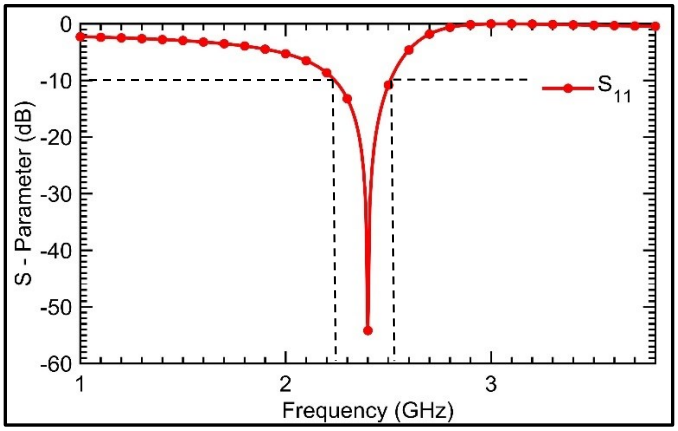


Fig. 32. Input Matching Network performance

It is evident from the figure that a very good matching is obtained at the design frequency along with a bandwidth of around 400MHz. As the source pull is not critical for PA design, so detailed discussion is averted here. [In PA design, noise performance need not be paid much attention as it is the last stage of any transmitter module. According to the Friis equation, if any component happens to be the first in the chain of interdependent processes, then the total noise figure of the system is dependent on the noise figure of the first stage. The total NF tends to cumulate if the first stage is not designed carefully. Hence, in LNAs design of the input matching network is very critical [30], whereas the same is true for output matching networks in PA]. Although Source Pull method has been discussed and simulations performed, this thesis does not incorporate the technique to design the input matching network.

6. Simulation results

This section discusses about the simulation results. The design has been made modular for the ease of debugging. Each module is presented separately and the overall complete circuit is provided in App. B.

6.1. Drain output waveform:

The output waveform should ideally be a square voltage and a half sine current at the drain. Idealities are not maintained in practice due to substrate effects and irregularities. Moreover, ideally, an infinite number of harmonics are to be controlled to obtain the waveforms as shown in Fig. 3(g), which is a practical impossibility. In this thesis, upto the 5th harmonic is being controlled and thus the drain output waveforms do not resemble the ideal ones. Fig. 33 depicts the output current and voltage waveforms with respect to time. The shaded area signifies area of overlap between the current and the voltage waveforms and hence quantifies power dissipation.

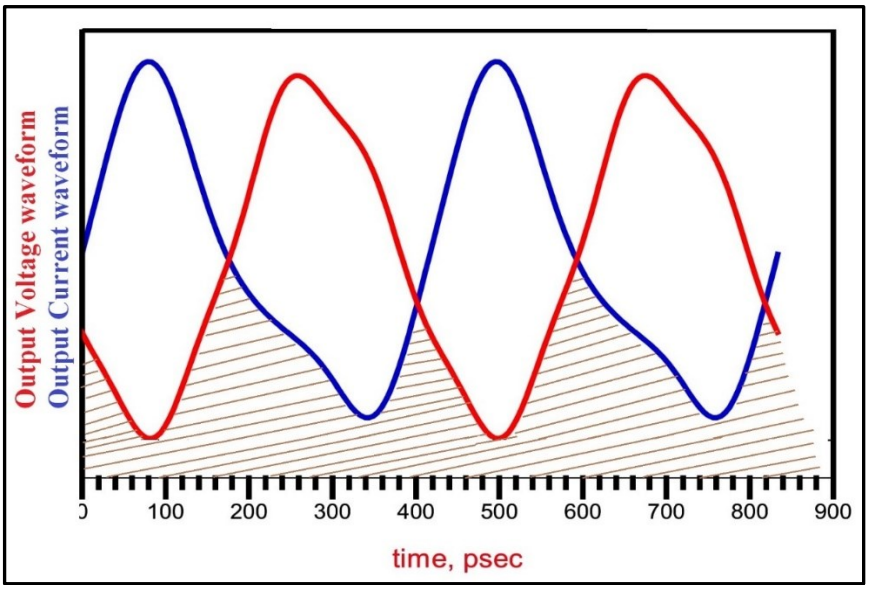


Fig. 33. Output voltage and current waveforms

The amount of power dissipated depends directly upon the quality of the bias network. If the stability network has a high Q-factor, it indicates the presence of a high resistive component which induces loss. Thus, it has to be made sure that the bias network be designed in such a manner that the loss factor is less and at the same time, the network remains stable for a wide range of frequencies. Loss also depends on the number of junctions or discontinuities present in the circuit. They include Tees, Crosses, Steps and other junctions which are used to maintain the continuity between two microstrip lines of varying width.

6.2. Output power spectrum:

Fig. 34 below shows the output power spectrum. It is evident from the figure that the odd harmonics i.e. 3rd and 5th, could be completely suppressed while the even harmonics- 2nd and 4th were also suppressed to a good extent. The fundamental power obtained is around 10W (a little less) at the design frequency, for an input power of 1W.

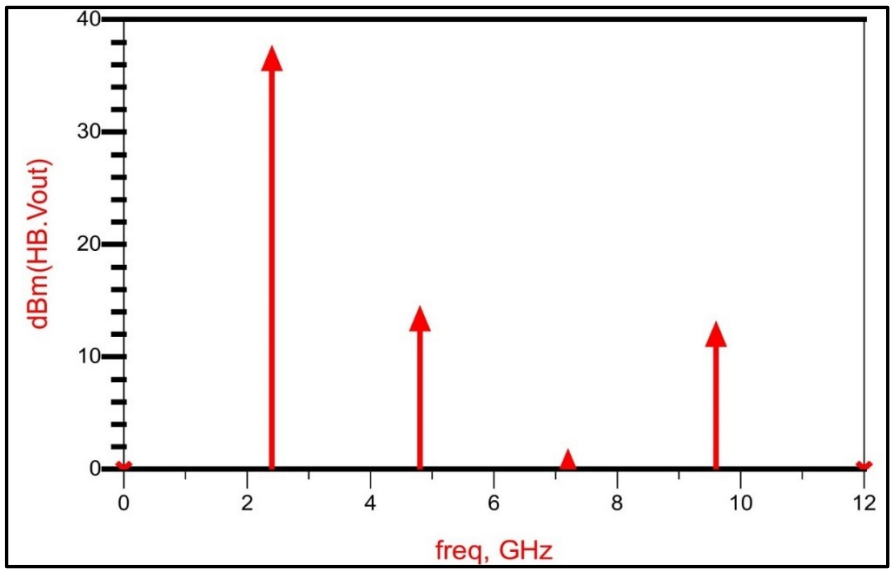


Fig. 34. Output spectrum (fundamental and harmonic included)

6.3. PAE and P_{del}:

PAE and P_{del} were the two specifying parameters in the design. PAE depends upon P_{del} in a linear fashion upto a certain limit of the input RF power. Beyond this, the PAE happens to decrease with increase in input power. This is the limit of linearity of the amplifier. Fig. 35 below depicts the PAE vs P_{del} plot.

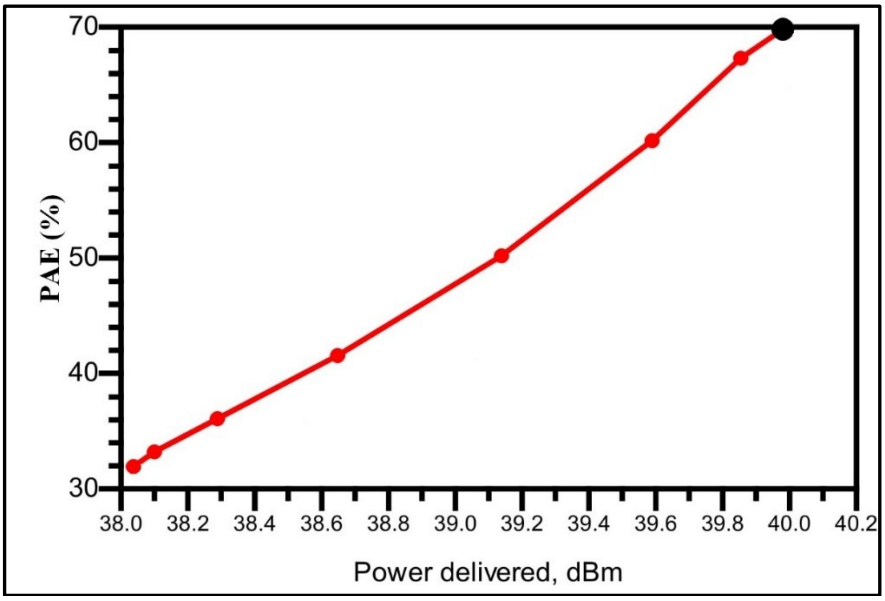


Fig. 35. PAE vs Power Delivered (in dBm)

It is evident from the figure that the PA performs linearly with an efficiency of 70% and output power of 40dBm. The peak is attained at the point denoted by the black marker, after which the PA operation becomes non-linear.

6.4. Phase vs PAE/P_{del}:

Fig. 36 below shows the overall performance of the PA parameters with respect to phase. The PAE, P_{del} and the phase of the load reflection coefficient has been considered in the analysis.

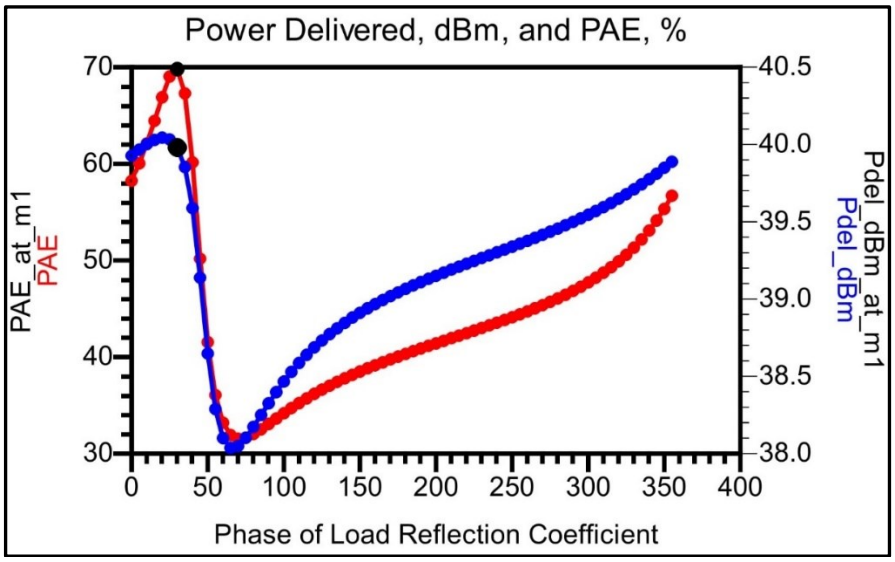


Fig. 36. Overall performance comparison in terms of PAE, P_{del} and phase

6.5. Gain vs P_{del}:

An important parameter to judge the PA performance is the gain behavior with respect to P_{del}. Fig. 37 depicts the plot of the fundamental output power level

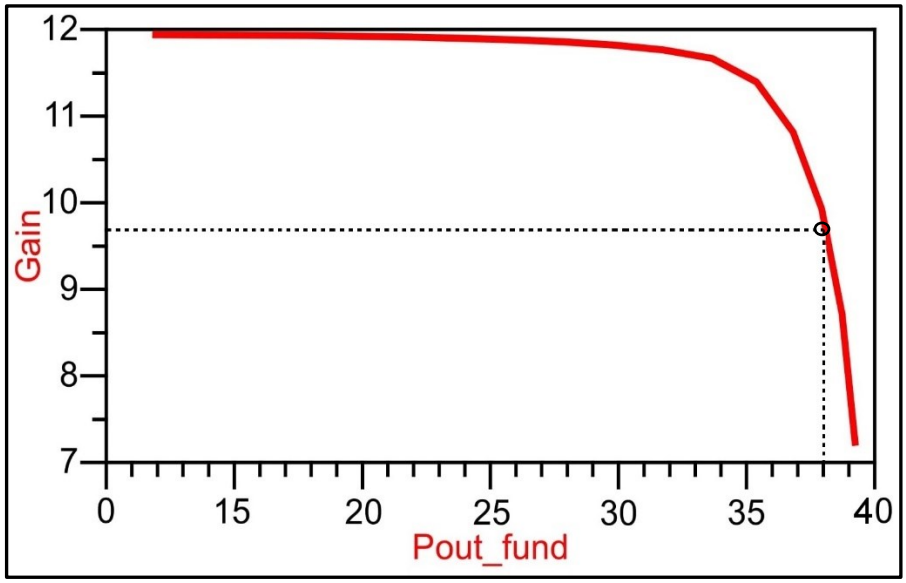


Fig. 37. Gain (dB) vs Power delivered (dBm)

vs the small signal gain. It is seen that at the output power level of 38dBm, the amplifier provides a small signal gain of 9.7. Gain compression, which is function of the input power level, is said to have occurred when the input power level of the amplifier is increased to such an extent that it ceases to behave linearly and the gain drops. This leads to non-linear increase in output power. Measurement of the compression point is important as it helps estimating the linearity limits. For instance, of a sinusoidal input signal, the output of the PA is no more sinusoidal at the post-compression region. Some of the output components appear in the harmonics rather than at the fundamental signal.

6.6. Matching network frequency behavior:

Fig. 38 depicts the frequency behavior of the input matching network. Frequency is swept across the design frequency to study the broadband behavior. It is seen that near the design frequency of 2.4GHz, a matching loop is present. The size of the loop is an indicator of the bandwidth of the PA. In Fig. 38(b), the case of

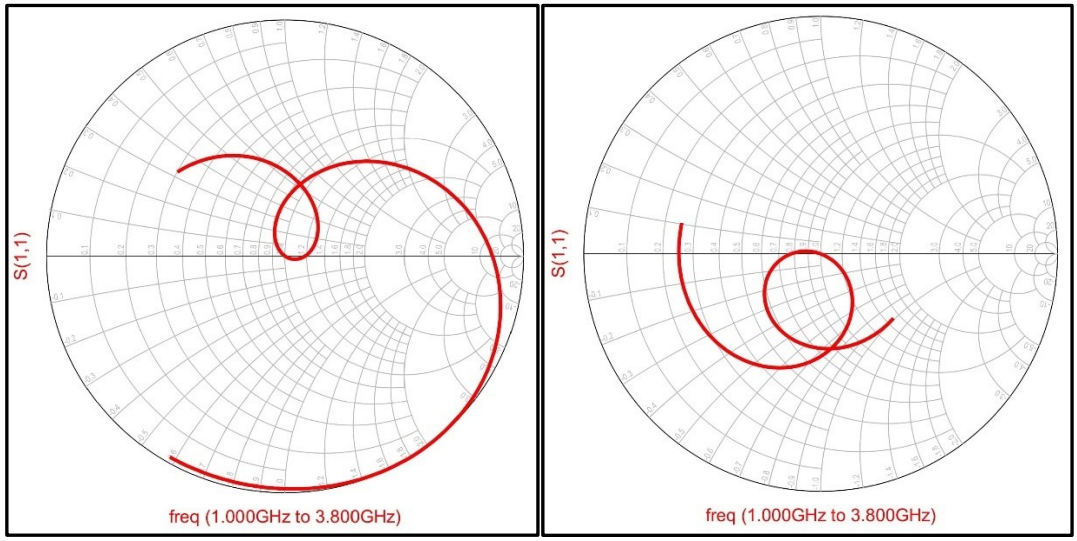


Fig. 38. (a) IMN frequency behavior (b) OMN frequency behavior

OMN, it is clear that the network shows a perfect match at the design frequency and a wide bandwidth around it (42.6%, 10dB BW point), while in the case of IMN, the match is obtained at the design frequency and a bandwidth of 17% is obtained. It should be noted that the input matching network could have been designed following the source pull steps as discussed earlier. This would include proper harmonic terminations (shorted 2^{nd} and 4^{th}, open 3^{rd} and 5^{th}) followed by varying the source impedance over constant power. The matching network designed by this technique would increase the bandwidth subsequently.

7.Conclusion

7.1. Discussion:

The target specification of the thesis was to design a PA that provides a PAE of more than 80%, delivers a power of 40dBm at the design frequency and provides a high bandwidth. The final results differed from the initial goals set. Firstly, the simulations were done on microstrip substrates and not on ideal lines. The substrate losses had an effect on the performance. The junctions present at the discontinuities (Tee, Cross, Step etc.) added to extra metal (conductor) that differed the electrical lengths of the transmission lines. The resistor and capacitor values were tuned to get the actual responses. Secondly, stabilizing the bias network was a big issue. One point of interest in the thesis is that the bias network is devoid of any lumped components. Conventional PA bias networks incorporate lumped capacitors and inductors to bias the network, which are often designed at lower frequencies less than 1GHz. This work incorporates use of butterflies (or radial stubs) and a wideband isolation network to design the RF choke. The disadvantage of this technique being additional losses (for a higher stability) that reduces the overall PAE.

Another interesting point of this work is the design of the output matching network. Conventional PA designs use a separate harmonic termination network prior to Load Pull, which sets the harmonic impedances. This work incorporates the harmonic terminations inside the Load Pull. In other words, it presents the design of a reduced output section that, on one hand, provides the harmonic termination impedances and on the other hand, matches the optimum load thus found, with the generic 50Ω termination.

7.2. Future work:

This work presented a simulation based design of a broadband high efficiency GaN HEMT Power Amplifier. Fabrication of the prototype could not be done due to the lack of facilities within the stipulated time.

The input matching network should be designed using the Source Pull technique. This should also incorporate the input harmonic impedance terminations.

Post fabrication tests should also be performed to verify the PA performance. These include ACPR (Adjacent Channel Power Ratio) evaluation and EVM (Error Vector Magnitude) calculation. These tests require a Digital source, for instance, a 16-QAM signal as the input.

References

[1] Oswald and Schelleng, "Power Amplifiers in Trans-Atlantic Radio Telephony", *Proc. IRE*, New York, May 1924.

[2] E.W Kellog, "Design of Non-Distorting Power Amplifier", *Trans. A.I.E.E*, Feb. 1925.

[3] K. Rawat, M.S Hashmi, F.M Ghannouchi, "Dual-Band RF Circuits and Components for Multi-Standard Software Defined Radios", *IEEE Circuits and Systems Mag.*, Vol. 12, Issue 1, pp. 12 – 32, Feb. 2012.

[4] K. Chen, D. Peroulis, "Design of Broadband High Efficiency Power Amplifier using in-Band Class-F/F^{-1}Mode-Transferring Technique", *Micr. Symp. Digest (MTT)*, 2012

[5] K. Chen, D. Peroulis, "Design of Broadband Highly Efficient Harmonic Tuned Power Amplifier using in-Band Continuous Class-F/F^{-1}Mode-Transferring", *IEEE Tran. Micro. Theory and Tech.*, Vol. 60, No. 12, pp. 4107 – 4116, Dec. 2012.

[6] P. Wright, J. Lees, J. Benedikt, P.J. Takser, S.C. Cripps, "A Methodology for Realizing High Efficiency Class-J in a Linear and Broadband PA", *IEEE Tran. Micro. Theory and Tech.*, Vol. 57, No. 12, pp. 3196 – 3204, Dec. 2009.

[7] K. Chen, D. Peroulis, "A 3.1GHz Class-F Power Amplifier With 82% Power Added Efficiency", *IEEE Micr. and Wireless Comp. Lett.*, Vol. 23, No. 8, pp. 436 – 438, Aug. 2013.

[8] P. Saad, H.M Nemati, M. Thorsell, K. Anderson, C. Fager, "An Inverse Class-F GaN HEMT Power Amplifier with 78% PAE at 3.5GHz", *Proc. of the 39th Euro. Micr. Conf.*, Sept. 2009.

[9] Y.Y. Woo, Y. Yang, B. Kim, "Analysis and Experiments for High Efficiency Class-F and Inverse Class-F Power Amplifiers", *IEEE Tran. on Micr. Theory and Tech.*, Vol. 54, No. 5, pp. 1969 – 1974, May. 2006.

[10] J.H Kim, G.D Jo, J.H Oh, Y.H Kim, K.C Lee, J.H Jung, "Modeling and Design Methodology of High Efficiency Class-F and Class-F^{-1} Power Amplifiers", *IEEE Tran. on Micr. Theory and Tech.*, Vol. 59, No. 1, pp. 153 – 165, Jan. 2011.

[11] D. Schmelzer, "A GaN HEMT class F amplifier at 2GHz with >80% PAE", *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 10, pp. 2130 – 2136, Oct. 2007

[12] F. H. Raab, "Maximum efficiency and output of Class-F power amplifiers", *IEEE Trans. Micr. Theory and Tech.*, Vol. 49, No. 6, pp. 1162 – 1166, June 2001

[13] Cree Inc. Datasheet for Cree CGH40010F, 10W, RF Power GaN HEMT.

[14] U.K. Mishra, P. Parikh, and Y.F. Wu. "AlGaN/GaN HEMTs: An overview of device operation and applications".

[15] Andrei Grebennikov, "RF and Microwave Power Amplifier Design", McGraw-Hill, 2005.

[16] Guillermo Gonzalez, "Microwave Transistor Amplifiers Analysis and Design", 2nd Edition, Prentice Hall Upper Saddle River, New Jersey

[17] Abdullah Eroglu, "Introduction to RF Power Amplifier Design and Simulation", CRC Press, Taylor and Francis Group, 2016.

[18] J.B Walker, "Handbook of RF and Microwave Power Amplifiers", Cambridge University Press, John Wiley and Sons. 2012.

[19] A. Rudiakova, V. Krizhanovski. "Advanced Design Techniques for RF Power Amplifiers", Springer.

[20] Peter B. Kenington, "High-Linearity RF Amplifier Design", Artech House, inc., 2000.

[21] Kyun-Whan Yeom, “Microwave Circuit Design- A Practical Approach Using ADS”, Prentice Hall, 2015.

[22] Bal S. Virdee, Avtar S. Virdee, Ben Y. Banyamin, “Broadband Microwave Amplifiers”, Artech House Inc. 2014

[23] Steve C. Cripps, “RF Power Amplifiers for Wireless Communications”, Artech House, inc., 2006.

[24] I. Rosu, “RF Power Amplifiers”, [Online] Available: http://www.qsl.net/va3iul/RF%20Power%20Amplifiers/RF_Power_Amplifiers.pdf

[25] RFIC Technologies, “Class E amplifier”, [Online] Available: http://www.rficdesign.com/rf/class-e-amplifier

[26] F. H. Raab, “An introduction to Class-F power amplifiers,” RF Design, Vol. 19, No. 5, pp. 79-84, May 1996.

[27] E. Benabe, K. Skowronski, T. Weller, H. Gordon and P. Warder, “Automated characterization of Ceramic Multilayer”, Electrical Engineering Department, University of South Florida.

[28] Chris Bowick, “RF Circuit Design, Newnes, inc., 2008.

[29] F.M Ghannouchi, M.S. Hashmi, “Load Pull Techniques with Applications to Power Amplifier Design”, Springer Netherlands, 2012.

[30] Jeremy Everard. “Fundamentals of RF Circuit Design: with Low Noise Oscillators”, John Wiley & Sons, Ltd, 2001. Artech House inc.,2004.

[31] ADS Circuit Design CookBook 2.0, Agilent Technologies.

[32] X. Liu, Y. Liu, S. Li, F. Wu, Y. Wu, “A Three-Section Dual-Band Transformer for Frequency-Dependent Complex Load Impedance”, *IEEE Micro. And Wireless Comp. Lett.*, Vol. 19, Issue 10, pp. 611 – 613, Oct. 2009.

[33] M.A Nikravan, Z. Atlasbaf, “T-section dual-band impedance transformer for frequency-dependent complex impedance loads”, *Electronic Lett.*, Vol. 47, Issue 9, pp. 551 – 553, May, 2011.

[34] Z.B Chao, L. Yang, W.J Xing, D. L.W Yi, C.M Yi, M. X Hua, H. Yue, “Analysis of the third harmonic for class-F power amplifiers with an *I– V* knee effect” , *Chinese Physics B*, 2015, 24(5): 058401

[35] Amplifiers- Classes [Online] http://www.electronics-tutorials.ws/amplifier/amp_5.html

APPENDIX

A. Load Pull Results: pp. 48

This section contains the Load Pull results in detail. The PAE and P_{del} contours along with their normalized values (normalized with respect to $50\,\Omega$) are presented. The optimum impedance is obtained and denoted by marker m_3. PAE and P_{del} values corresponding to that impedance is also denoted.

B. Modular PA design: pp. 49

Modularity is an important aspect in any design. A design is said to be modular if the entire circuit can be divided into discrete sections based on the function each section performs. This eases debugging and sectional performance characterization. In this thesis, the entire PA has been modularized into five sections- the Transistor, the gate bias circuit, the drain bias circuit, the input and the output matching networks. Each of them has been hierarchically decomposed in ADS, selecting any of which pushes into the descendant hierarchy. Local interconnections between the modules ensure a globally connected circuit that performs the action of power amplification.

C. Complete PA circuit: pp. 50

While the advantages of modular circuits have been discussed above, the full circuit is basically the base level of the hierarchy. It consists of the connected blocks with their modules decomposed. It gives an intuition as to how the entire circuit wood look like. This contains all the design parameters and the variables used to define the microstrip dimensions, that are not visible at the top level. The figure shows all the simulators and the optimizers used as well (though they are deactivated).

D. Friis Formula for Noise Figure of a Cascaded System:

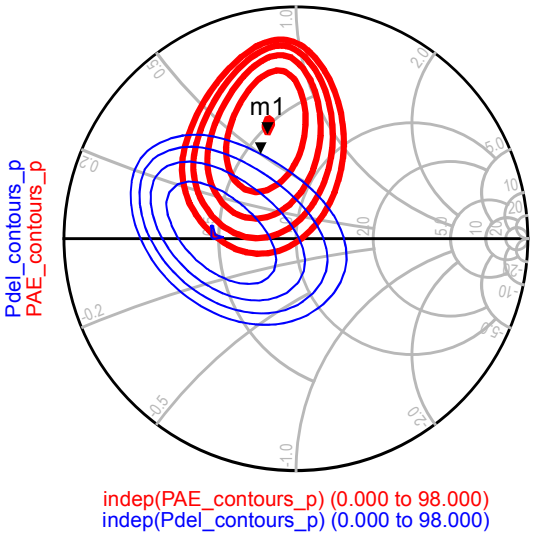
$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}}$$

where, F_i and G_i are the NF and Gain of the i^{th} block.

System Reference Impedance: 50.000

A

PAE (thick) and Delivered Power (thin) Contours



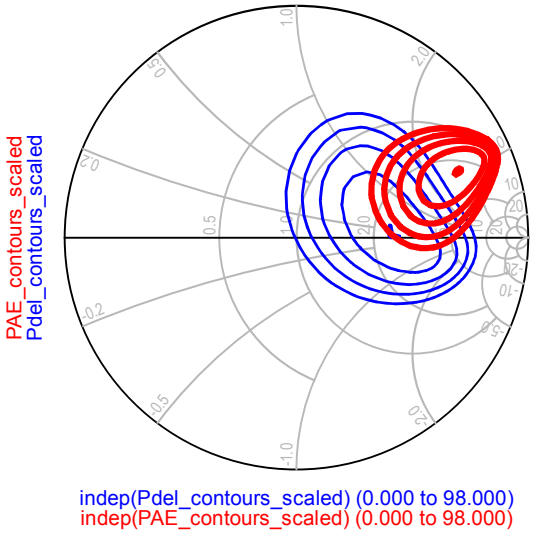
Set Delivered Power contour step size (dB) and PAE contour step size (%), and number of contour lines

Eqn Pdel_step=0.5
Eqn PAE_step=4
Eqn NumPAE_lines=5
Eqn NumPdel_lines=5

Maximum Power-Added Efficiency, %: 85.37

Maximum Power Delivered, dBm: 42.94

Re-Normalized PAE (thick) and Delivered Power (thin) Contours



Set new reference impedance:

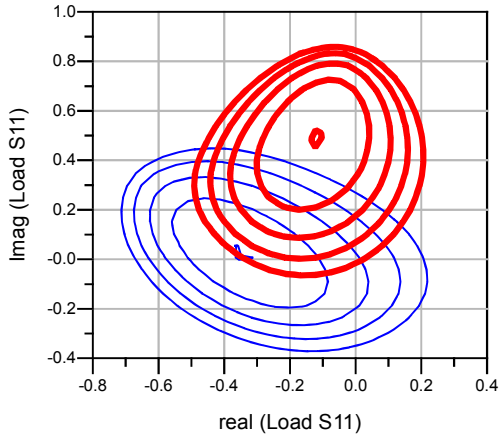
Eqn Z0new=10

m1
indep(m1)=3
PAE_contours_p=0.468 / 105.210
level=85.269, number=1
impedance = Z0 * (0.533 + j0.617)

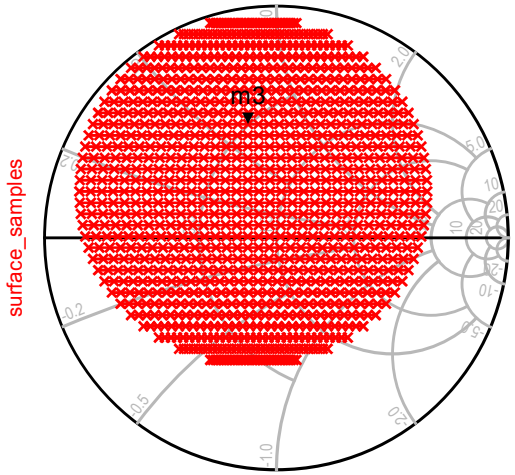
m2
indep(m2)=19
Pdel_contours_p=0.395 / 112.652
level=40.931, number=1
impedance = Z0 * (0.578 + j0.499)

Equations are on the "Equations" page.

PAE (thick) and Delivered Power (thin) Contours



Simulated Load Reflection Coefficients



Move Marker m3 to select impedance value and corresponding PAE and delivered power values.

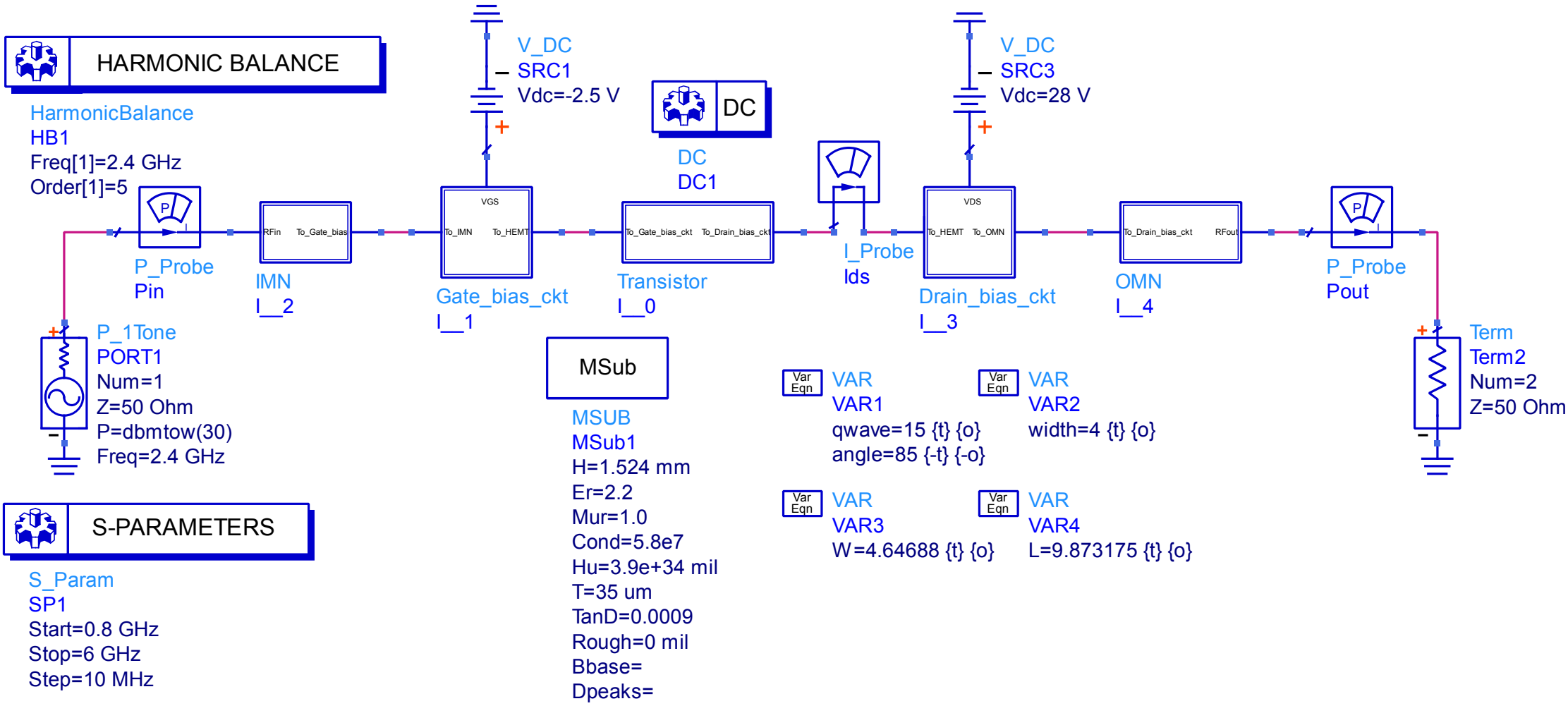
Impedance at marker m3: 24.806 + j32.702

PAE, %: 85.37

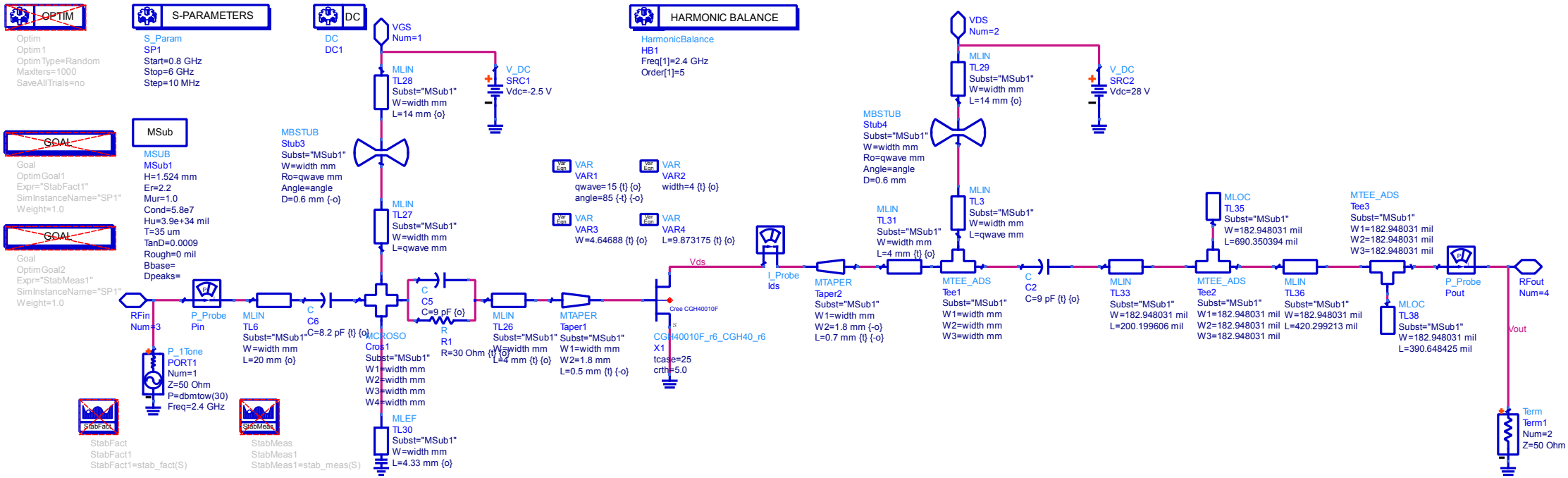
Power Delivered (dBm): 39.80

m3
real_indexs11=-0.122
surface_samples=0.506 / 103.997
imag_indexs11=0.491
impedance = Z0 * (0.496 + j0.654)

B


HARMONIC BALANCE
HarmonicBalance
HB1
Freq[1]=2.4 GHz
Order[1]=5
V_DC
SRC1
Vdc=-2.5 V
DC
DC
DC1
V_DC
SRC3
Vdc=28 V
P_Probe
Pin
IMN
I__2
VGS
To_IMN
To_HEMT
Gate_bias_ckt
I__1
To_Gate_bias_ckt
To_Drain_bias_ckt
Transistor
I__0
I_Probe
Ids
VDS
To_HEMT
To_OMN
Drain_bias_ckt
I__3
To_Drain_bias_ckt
RFout
OMN
I__4
P_Probe
Pout
Term
Term2
Num=2
Z=50 Ohm
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow(30)
Freq=2.4 GHz
MSub
MSUB
MSub1
H=1.524 mm
Er=2.2
Mur=1.0
Cond=5.8e7
Hu=3.9e+34 mil
T=35 um
TanD=0.0009
Rough=0 mil
Bbase=
Dpeaks=
VAR
VAR1
qwave=15 {t} {o}
angle=85 {-t} {-o}
VAR
VAR2
width=4 {t} {o}
VAR
VAR3
W=4.64688 {t} {o}
VAR
VAR4
L=9.873175 {t} {o}
S-PARAMETERS
S_Param
SP1
Start=0.8 GHz
Stop=6 GHz
Step=10 MHz

C


OPTIM
Optim
Optim1
OptimType=Random
MaxIters=1000
SaveAllTrials=no
S-PARAMETERS
S_Param
SP1
Start=0.8 GHz
Stop=6 GHz
Step=10 MHz
DC
DC
DC1
HARMONIC BALANCE
HarmonicBalance
HB1
Freq[1]=2.4 GHz
Order[1]=5
GOAL
Goal
OptimGoal1
Expr="StabFact1"
SimInstanceName="SP1"
Weight=1.0
GOAL
Goal
OptimGoal2
Expr="StabMeas1"
SimInstanceName="SP1"
Weight=1.0
MSub
MSUB
MSub1
H=1.524 mm
Er=2.2
Mur=1.0
Cond=5.8e7
Hu=3.9e+34 mil
T=35 um
TanD=0.0009
Rough=0 mil
Bbase=
Dpeaks=
VGS
Num=1
MLIN
TL28
Subst="MSub1"
W=width mm
L=14 mm {o}
V_DC
SRC1
Vdc=-2.5 V
MBSTUB
Stub3
Subst="MSub1"
W=width mm
Ro=qwave mm
Angle=angle
D=0.6 mm {-o}
MLIN
TL27
Subst="MSub1"
W=width mm
L=qwave mm
VAR
VAR1
qwave=15 {t} {o}
angle=85 {-t} {-o}
VAR
VAR2
width=4 {t} {o}
VAR
VAR3
W=4.64688 {t} {o}
VAR
VAR4
L=9.873175 {t} {o}
VDS
Num=2
MLIN
TL29
Subst="MSub1"
W=width mm
L=14 mm {o}
V_DC
SRC2
Vdc=28 V
MBSTUB
Stub4
Subst="MSub1"
W=width mm
Ro=qwave mm
Angle=angle
D=0.6 mm
MLIN
TL3
Subst="MSub1"
W=width mm
L=qwave mm
MLIN
TL31
Subst="MSub1"
W=width mm
L=4 mm {t} {o}
MLOC
TL35
Subst="MSub1"
W=182.948031 mil
L=690.350394 mil
MTEE_ADS
Tee3
Subst="MSub1"
W1=182.948031 mil
W2=182.948031 mil
W3=182.948031 mil
RFin
Num=3
P_Probe
Pin
MLIN
TL6
Subst="MSub1"
W=width mm
L=20 mm {o}
C
C6
C=8.2 pF {t} {o}
MICROSO
Cros1
Subst="MSub1"
W1=width mm
W2=width mm
W3=width mm
W4=width mm
C
C5
C=9 pF {o}
R
R1
R=30 Ohm {t} {o}
MLIN
TL26
Subst="MSub1"
W=width mm
L=4 mm {t} {o}
MTAPER
Taper1
Subst="MSub1"
W1=width mm
W2=1.8 mm
L=0.5 mm {t} {-o}
Vds
CGH40010F_r6_CGH40_r6
X1
tcase=25
crth=5.0
Cree CGH40010F
I_Probe
Ids
MTAPER
Taper2
Subst="MSub1"
W1=width mm
W2=1.8 mm {-o}
L=0.7 mm {t} {-o}
MTEE_ADS
Tee1
Subst="MSub1"
W1=width mm
W2=width mm
W3=width mm
C
C2
C=9 pF {t} {o}
MLIN
TL33
Subst="MSub1"
W=182.948031 mil
L=200.199606 mil
MTEE_ADS
Tee2
Subst="MSub1"
W1=182.948031 mil
W2=182.948031 mil
W3=182.948031 mil
MLIN
TL36
Subst="MSub1"
W=182.948031 mil
L=420.299213 mil
MLOC
TL38
Subst="MSub1"
W=182.948031 mil
L=390.648425 mil
P_Probe
Pout
RFout
Num=4
Vout
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow(30)
Freq=2.4 GHz
StabFact
StabFact
StabFact1
StabFact1=stab_fact(S)
StabMeas
StabMeas
StabMeas1
StabMeas1=stab_meas(S)
MLEF
TL30
Subst="MSub1"
W=width mm
L=4.33 mm {o}
Term
Term1
Num=2
Z=50 Ohm