



MULTIPLE VALUED CURRENT MODE LOGIC CIRCUITS

by

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Certificate

This is to certify that the thesis titled “ **Multiple valued Current Mode Logic Circuits**” being submitted by **Kunwar Tarun** to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

May, 2017

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Abstract

The circuits having more than two logic levels called as Multiple valued circuits have the potential of reducing area by reducing the on chip interconnection. Despite considerable effort, designing a system for processing a multiple valued signal is still a complicated task. Multiple valued circuits can be realized in voltage or current mode. Due to limited power supply, higher radix valued system is not feasible to design using voltage mode configuration. On the other hand, current mode circuits have the capability of scaling, copying, inverting using basic current mirror structure. The non self restoring nature and higher static power dissipation is the major problem in multiple valued current mode circuits. Self restoration circuits need to be developed for correct detectable output. In this study, performance of various fundamental current mode multiple valued operator is analyzed across different process corner and over wide temperature range. Voltage mode binary to current mode multiple valued encoding and current mode multiple valued to voltage mode binary decoding are presented here. Several combinational circuits such as Multiplexer, Demultiplexer and Full adder are proposed and discussed. Further sequential circuits such as Latch, D Flip-Flop, counters and arbitrary selected state diagram are presented here. Finally, 2-bit binary parallel adder and 1-digit quaternary full adder is compared in terms of various VLSI design criteria.

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Chapter 1

Introduction

Continuous scale down of technology nodes results in exponential increase in number of transistors per unit area. This has led to increase in number of interconnection. Routing of these interconnects over chip may consume area more than the active logic elements [1].

Multivalued circuits with more than two logic levels can be served as the solution to this problem. These circuits have a potential for reducing chip area consumed by interconnection wiring and functional units in very large scale integration (VLSI) [2]. Unlike binary with two logic levels, same range of data can now be carried over single wire. For example, two bit binary logic (00,01,10,11) is equivalent to single digit quaternary logic (0,1,2,3). Reduction in interconnection length or number of interconnection further results in reduction of interconnect delay, crosstalk noise and dynamic power dissipation. Interconnection delay is directly proportional to the square of the interconnection length. Crosstalk noise becomes significant as distance between interconnection decreases. The possible solution for this can be the increase in interconnection distance. Dynamic power consumption is reduced because of less interconnect capacitance. [3].

Although there are several advantages of multivalued logic over binary logic, but still implementing and building a design in multivalued logic requires considerable effort. Implementing basic functional sets and simplification of logic expressions is complex task for design engineer [7].

Multivalued logic circuits can be realized in voltage mode or current mode. Reduction of supply voltage in deep submicron technology nodes, will result in poor noise margin for the circuits implemented in voltage mode multiple valued logic. So higher radices can not be achieved in voltage mode multiple valued logic.

On the other hand, scaling, copying and sign changing using current mirrors are some of the potential advantages of current mode multiple valued logic circuits. Current mode multiple valued logic circuits are not self restoring and have static current mode power dissipation.

Chapter 2

Multivalued Logic Algebra

From the last couple of decades, multiple valued circuits are gaining importance in semiconductor industry. Unlike binary, these circuits have the capability of reducing the number of interconnection wires to great extent. For example, the decimal number '127' is represented as '1111111' in binary and '1333' in quaternary logic. The number of digits in quaternary logic is less than the binary logic to represent the same data.

Multivalued circuits can be realized in voltage mode or current mode. Continuous scaling of technology nodes has led to increase in chip density, which requires less power dissipation across the chip. As power consumption directly depends upon the square of the supply voltage across the chip, therefore dynamic range of voltage signals in multiple valued circuits is less for low power circuit. As a result, voltage mode multiple valued circuits can provide limited radix implementation.

On the other hand, current mode realization of multiple valued circuits can provide higher radix implementation because of good noise margin. In current mode, logic levels are defined as the integer multiple of the reference current. One of the potential advantage of the current mode circuits is the addition operation, which simply requires the connection of signal lines to a single node. The single binary addition requires 20 transistor. In current mode, the reference current is scaled, copied etc. with a simple current mirror. The major problem with the current mode circuits is that they have large static power dissipation and unlike binary circuits, they are not self-restoring. Accumulation of the deviation from expected output in cascading stages will heavily distort the output at final stage. Therefore, self restoration is required at every stage to restore the output to its original value.

The current mode and voltage mode logic levels for Quaternary circuits with reference current of 10uA and supply voltage of 1.2V respectively are discussed in Table 2.1

The noise margin of the current mode circuits is $\pm I_{ref}/2$. In current mode, the output deviations at each and every stage needs to be restored before the output current level of cascade stage exceeds the noise margin as shown in Table 2.2. This is called as level restoration.

Logic Level	Current Level μA	Voltage Level
0	0	0 V
1	10	0.4 V
2	20	0.8 V
3	30	1.2 V

Table 2.1: Logic levels of Quaternary mode signals

Logic Level	Current Level μA	Noise margin range
0	0	$I \leq 5\mu A$
1	10	$5\mu A \leq I < 15\mu A$
2	20	$15\mu A \leq I < 25\mu A$
3	30	$25\mu A \leq I$

Table 2.2: Noise margin for Quaternary current mode signals

2.1 Multiple Valued Operators

There are set of fundamental operators defined for multiple valued circuits. These fundamental operators are used to design complex combinational and sequential logic blocks. These operators are defined as follows :

Definition 1 *Complement[5] :The complement of x for radix r is defined as :*

$$\bar{x} = r - 1 - x \quad (2.1)$$

This operator can be designed using current mirror as shown in Figure 2.1

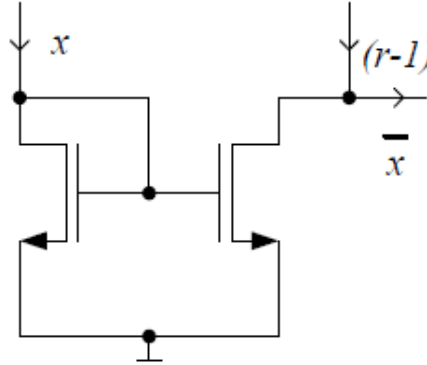


Figure 2.1: Complement Operator

The truth table for complement operator is shown in Table 2.3

x	0	1	2	3
$\bar{x}$	3	2	1	0

Table 2.3: Complement Operator

Definition 2 *Lower and Upper threshold[6] :The lower and upper threshold operators can be defined as :*

$$th_l :_b^c a = \begin{cases} c & \text{if } a \leq b \\ 0 & \text{otherwise} \end{cases} \quad (2.2)$$

$$th_u : a_b^c = \begin{cases} c & \text{if } a \geq b \\ 0 & \text{otherwise} \end{cases} \quad (2.3)$$

The realization of upper threshold circuit as discussed in [6] is shown in Figure 2.2. The lower threshold circuit can be realized by interchanging the inputs x and y.

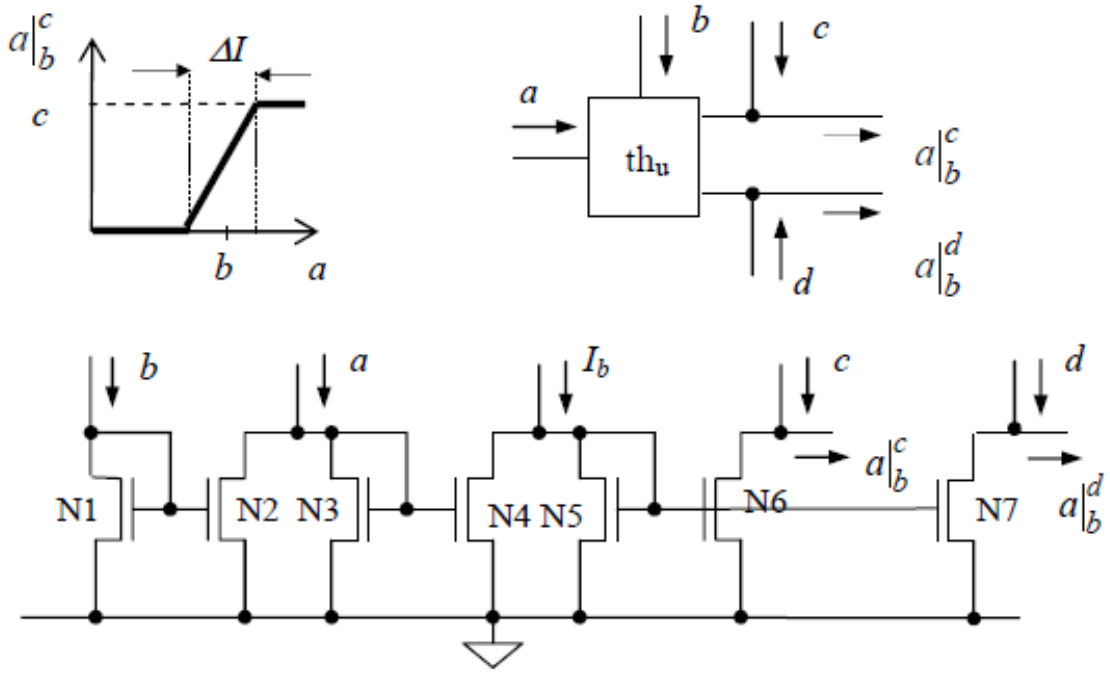


Figure 2.2: Upper threshold circuit

The truth table for the lower and upper threshold circuit is shown in Table 2.4 and 2.5 respectively

		b			
		0	1	2	3
a	0	c	c	c	c
	1	0	c	c	c
	2	0	0	c	c
	3	0	0	0	c

Table 2.4: Truth table for lower threshold circuit

		b			
		0	1	2	3
a	0	c	0	0	0
	1	c	c	0	0
	2	c	c	c	0
	3	c	c	c	c

Table 2.5: Truth table for upper threshold circuit

Definition 3 *Cyclic[5] :The cyclic operator shifts the input by specified amount. The clockwise cyclic shift (CWC) operator adds the specified amount of current to the input current. The counter clockwise cyclic (CCWC) shift operator subtracts the specified amount of current from the input current.*

$$CWC : \vec{x}^y = \begin{cases} x + y & \text{if } x + y \leq r - 1 \\ x + y - r, & \text{otherwise} \end{cases} \quad (2.4)$$

$$CCWC : \overleftarrow{x}^y = \begin{cases} x - y & \text{if } x - y \geq 0 \\ x - y + r, & \text{otherwise} \end{cases} \quad (2.5)$$

The truth table for the clockwise and counter clockwise cyclic operators is as shown in Table 2.6 and 2.7 respectively

		y			
		0	1	2	3
x	0	0	1	2	3
	1	1	2	3	0
	2	2	3	0	1
	3	3	0	1	2

Table 2.6: Truth table for clockwise cyclic operator

		y			
		0	1	2	3
x	0	0	3	2	1
	1	1	0	3	2
	2	2	1	0	3
	3	3	2	1	0

Table 2.7: Truth table for counter clockwise cyclic operator

The realization of clockwise cyclic operators discussed in [6] is shown in Figure 2.3, where r' is r-0.5 and r is the radix value.

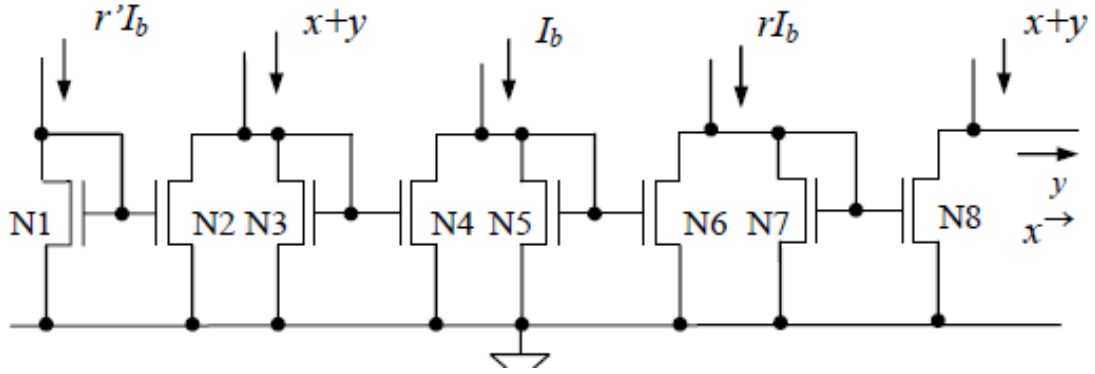


Figure 2.3: Clockwise cyclic circuit

Definition 4 *Minimum[5] :The minimum operator takes the input values and generates the output value which is minimum of the input values.*

$$\min(x, y) = \text{AND}(x, y) = x.y \quad (2.6)$$

The truth table for the minimum operators is as shown in Table 2.8

		y			
		0	1	2	3
x	0	0	0	0	0
	1	0	1	1	1
	2	0	1	2	2
	3	0	1	2	3

Table 2.8: Truth table for minimum operator

The realization of minimum circuit as discussed in [5] is shown in Figure 2.4.

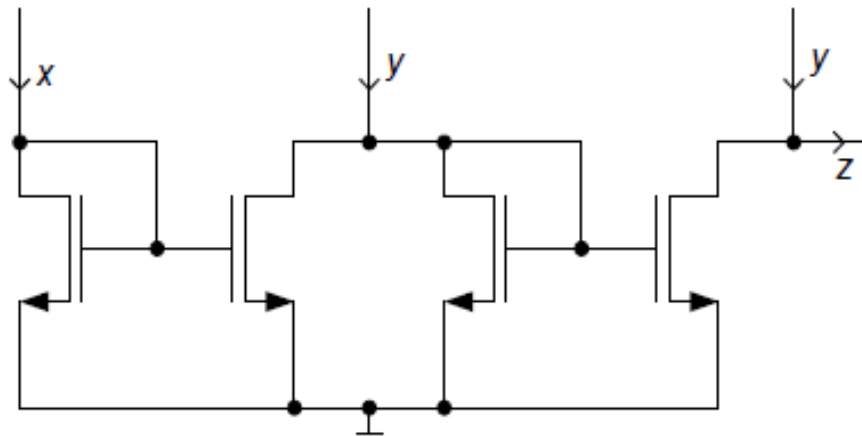


Figure 2.4: Minimum circuit

Definition 5 *Maximum[5] :The maximum operator takes the input values that generates the output value which is maximum of the input values.*

$$\max(x, y) = OR(x, y) = x + y \quad (2.7)$$

The truth table for the maximum operator is as shown in Table 2.9

		y			
		0	1	2	3
x	0	0	1	2	3
	1	1	1	2	3
	2	2	2	2	3
	3	3	3	3	3

Table 2.9: Truth table for maximum operator

The realization of maximum circuit as discussed in [5] is shown in Figure 2.5.

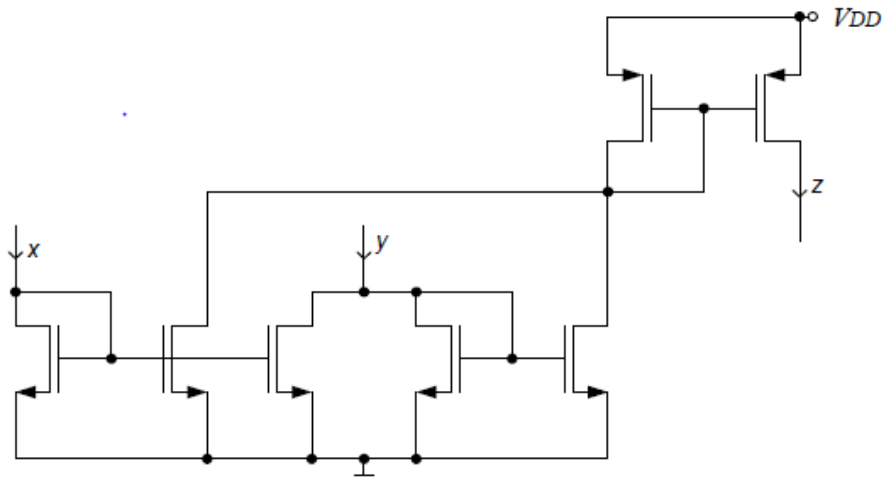


Figure 2.5: Maximum circuit

Chapter 3

Performance analysis of the multiple valued operators

In every current mode multiple valued circuit, current mirror is the fundamental building block. It is necessary to ensure that favourable design must have linear transfer characteristics, good transient behaviour and low dependence to parameter tolerances.

3.1 Linear Mirroring

The important parameter in mirror operation is maximum linear current range, MLCR, for chosen transistor sizes. To prove the robustness of the current mirror, the performance of the current mirror is analyzed in presence of transistor/process variation mismatches and wide temperature range.

Maximum linear current range (MLCR) is the maximum input current range for which output current should not vary beyond $\pm$ Noise margin i.e. $\pm I_{ref}/2$. Considering the process variation, maximum linear current range of the current mirror is the minimum of the maximum linear current range of all process corner. The Maximum linear current range (MLCR) is given as

$$MLCR = \min(MLCR_{slow}, MLCR_{fast}, MLCR_{typical}) \quad (3.1)$$

Noise margin is defined as half of the unit step or reference current.

$$NoiseMargin = I_{ref}/2 \quad (3.2)$$

For every process corner i.e. typical, fast, slow at W/L=3, the variation of the output current with input current in current mirror is shown in Figure 3.1.

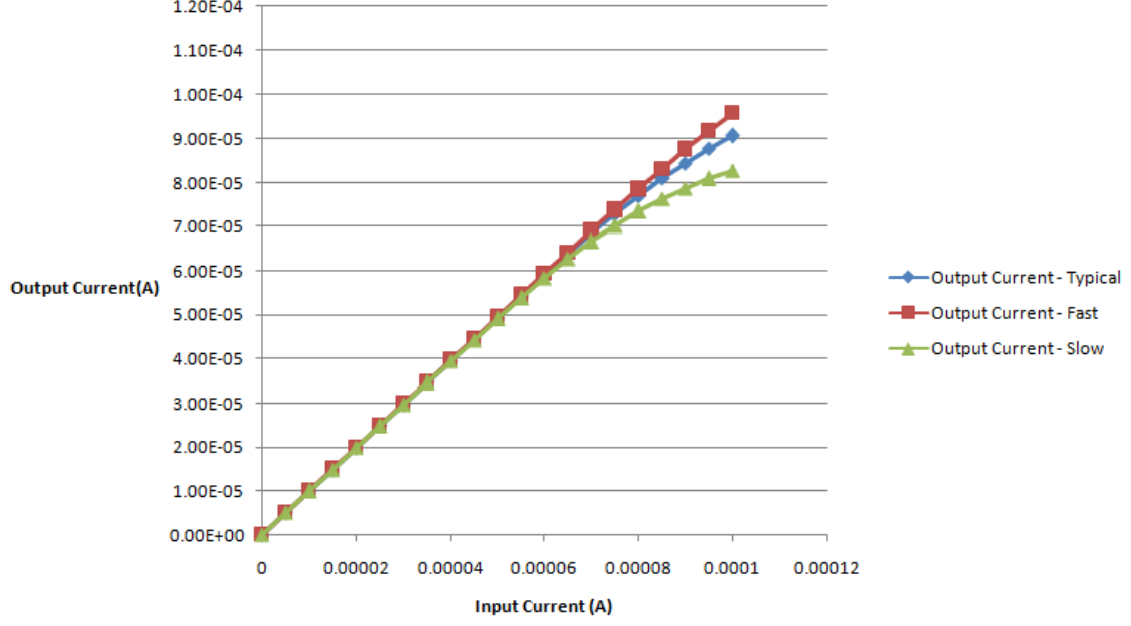


Figure 3.1: Linear variation of output current for different process corner

From the line graph in Figure 3.1, Maximum linear current range for all process corner is shown in equation 3.3

$$\begin{aligned}
 MLCR_{slow} &= 76\mu A \\
 MLCR_{fast} &= 98\mu A \\
 MLCR_{typical} &= 88\mu A
 \end{aligned} \tag{3.3}$$

By using equation 3.3 in equation 3.1, the Maximum linear current range is shown in equation 3.4

$$\begin{aligned}
 MLCR &= \min(76\mu A, 98\mu A, 88\mu A) \\
 MLCR &= 76\mu A
 \end{aligned} \tag{3.4}$$

The achievable Radix-r is given by :

$$\begin{aligned}
 Radix - r &\leq MLCR/I_{ref} \\
 &\leq 76\mu A/10\mu A \\
 &\leq 7.6 \approx 7
 \end{aligned} \tag{3.5}$$

Increase in sizing of current mirror ensures better matching characteristics. Input current is varied from 0 to 100 μ to achieve the linearity range of the output current. The line graph for variation of output current with input current for slow, typical and fast corner with different W/L is shown in Figure 3.2, 3.3, 3.4 respectively.

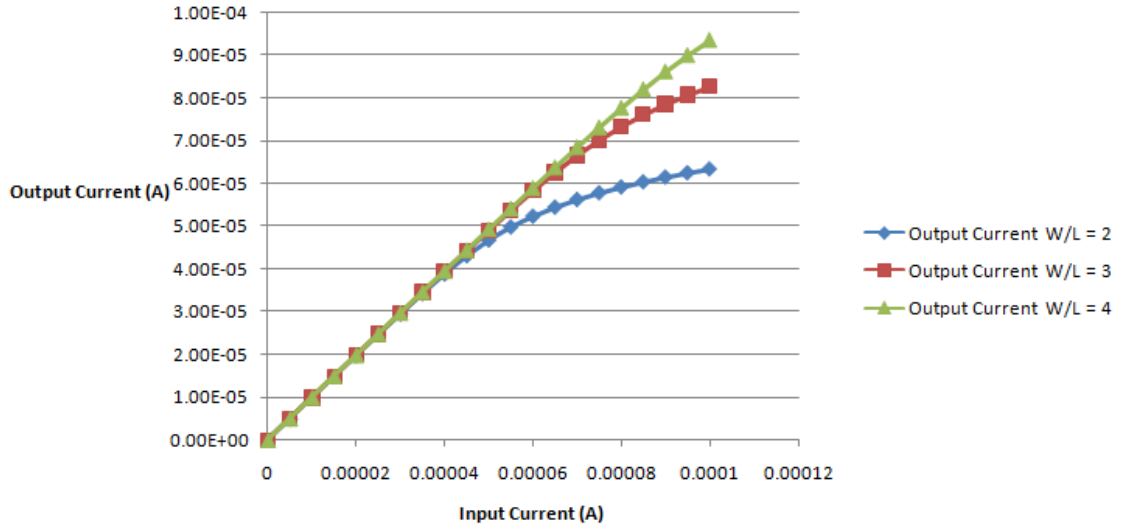


Figure 3.2: Linear variation of output current for slow process corner with different W/L

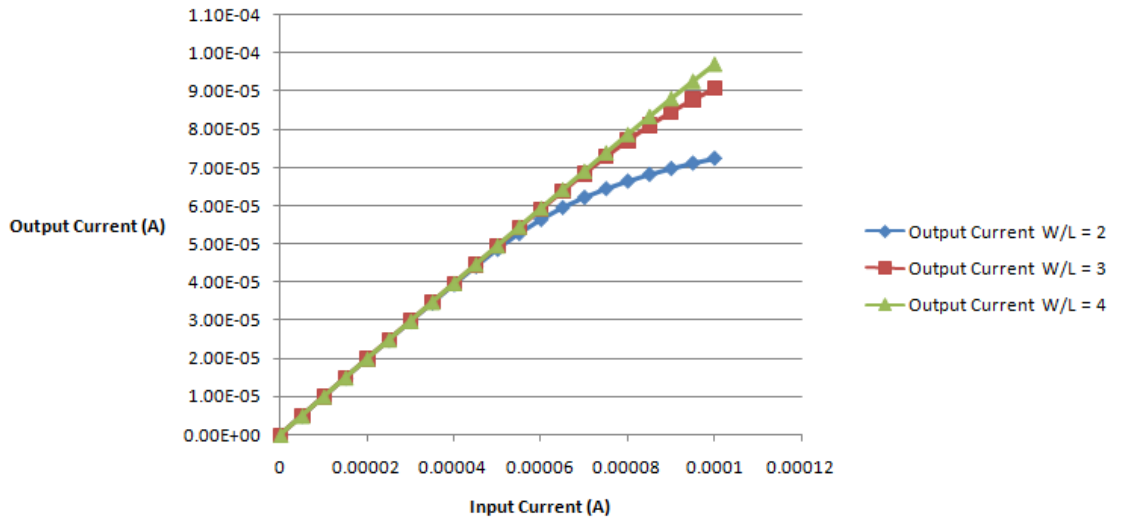


Figure 3.3: Linear variation of output current for typical process corner with different W/L

It can be seen from the Table 3.1 that, increase in sizing W/L results in increase in Maximum linear current range (MLCR).

$(W/L)_{NMOS}$	$MLCR_{typical}(\mu A)$	$MLCR_{fast}(\mu A)$	$MLCR_{slow}(\mu A)$	$MLCR(\mu A)$
2	63	74	54	54
3	88	98	76	76
4	100	100	95	95

Table 3.1: Variation of MLCR with transistor sizing W/L for different process corner

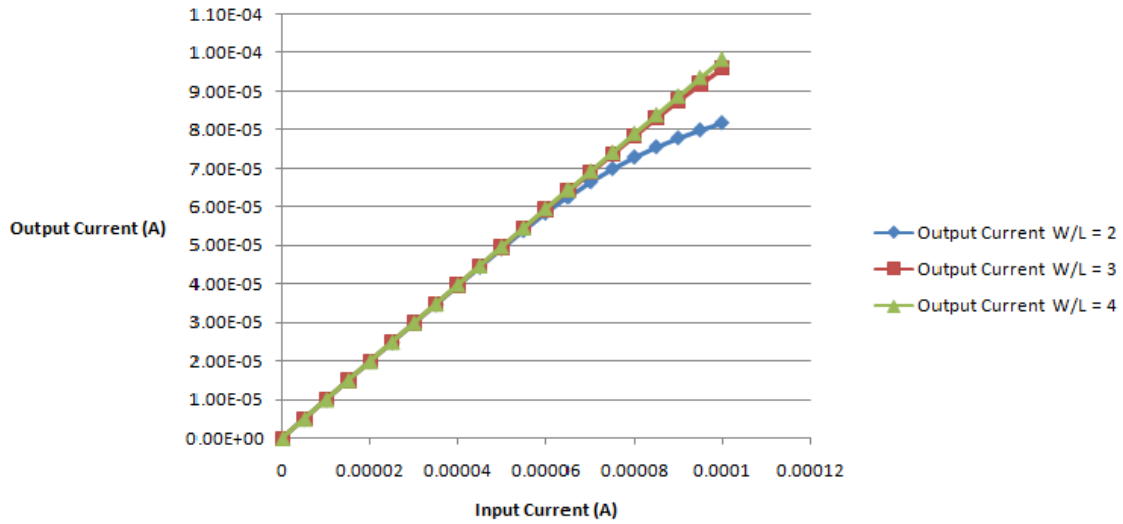


Figure 3.4: Linear variation of output current for fast process corner with different W/L

3.2 Complement operator

The performance of the complement circuit presented in Figure 2.1 is analyzed in terms of terms of wide temperature range and across different process corner. The variation of the output current for logic level 0,1,2,3 over wide temperature range from -40 to 120 degree are plotted in Figure 3.5

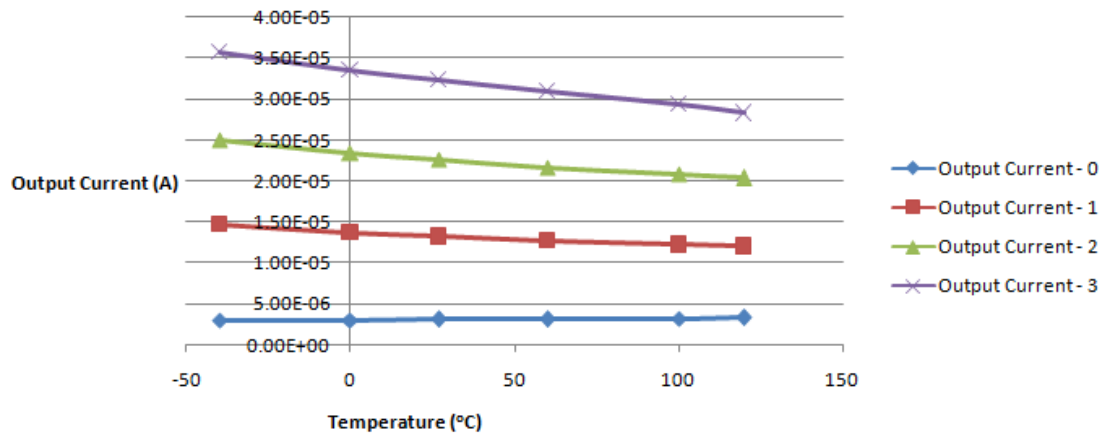


Figure 3.5: Variation of output current over wide temperature range in complement circuit

The variation of output current for logic level 0,1,2,3 across different process corner is shown in Figure 3.6

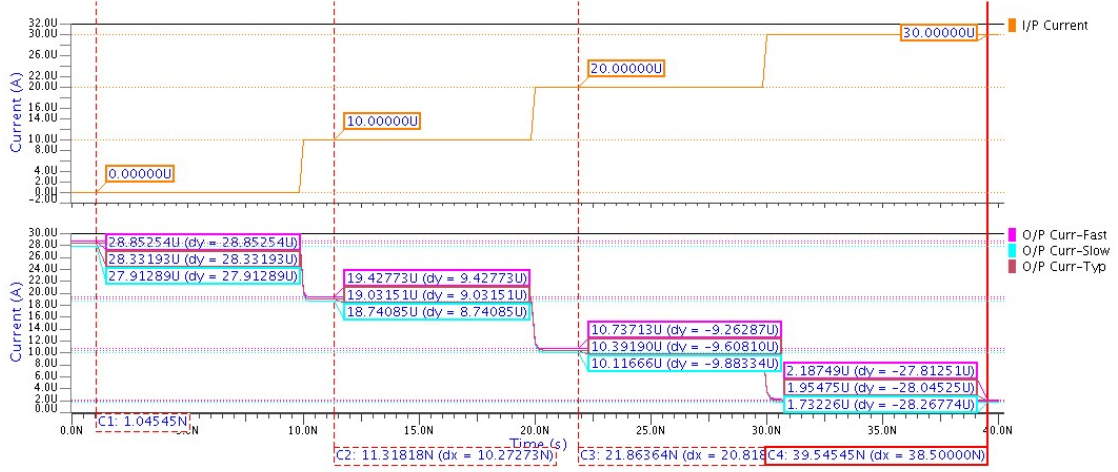


Figure 3.6: Variation of output current across different process corner in complement circuit

The worst case rise delay or fall delay for the complement circuit is determined from switching of logic level 0 to 3 or vice verse respectively. The Figure 3.7 and Table 3.2 shows the rise time and fall time delay of the circuit

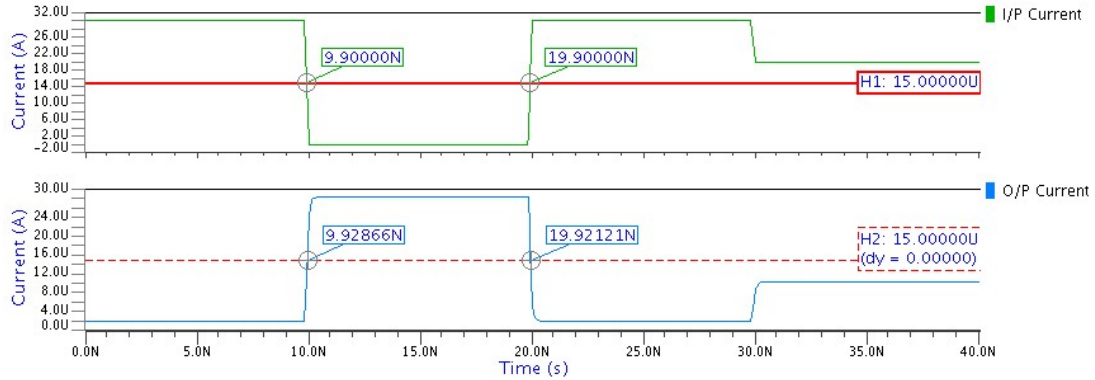


Figure 3.7: Worst case rise time and fall time delay of complement circuit

Worst case rise time delay	0.02866 ns
Worst case fall time delay	0.02121 ns

Table 3.2: Worst case rise time and fall time delay of complement circuit

3.3 Threshold Operator

The performance of the threshold circuit presented in Figure 2.2 is analyzed in terms of terms of wide temperature range and across different process corner. The variation of the output current for logic level 0,1,2,3 over wide temperature range from -40 to 120 degree are plotted in Figure 3.8

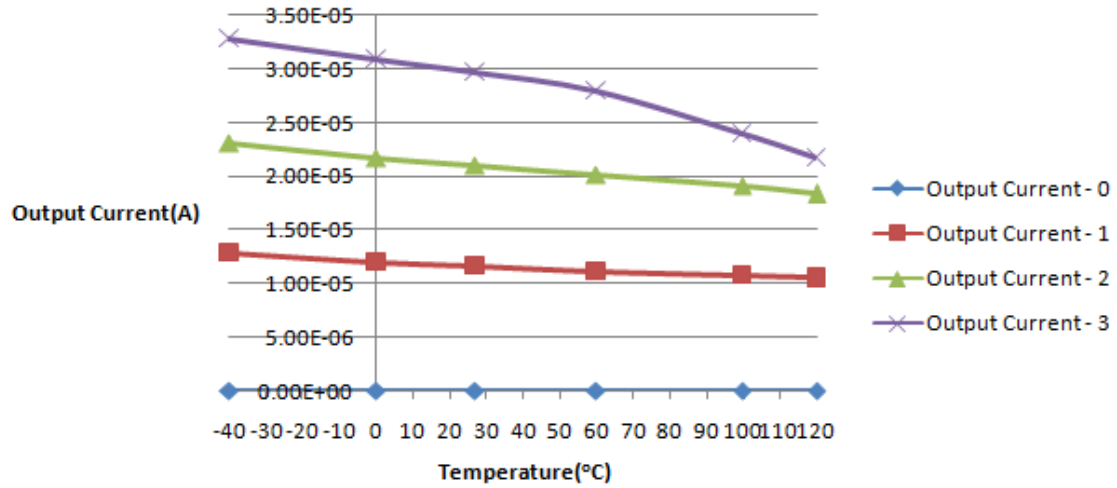


Figure 3.8: Variation of output current over wide temperature range in threshold circuit

The variation of output current for logic level 0,1,2,3 across different process corner is shown in Figure 3.9

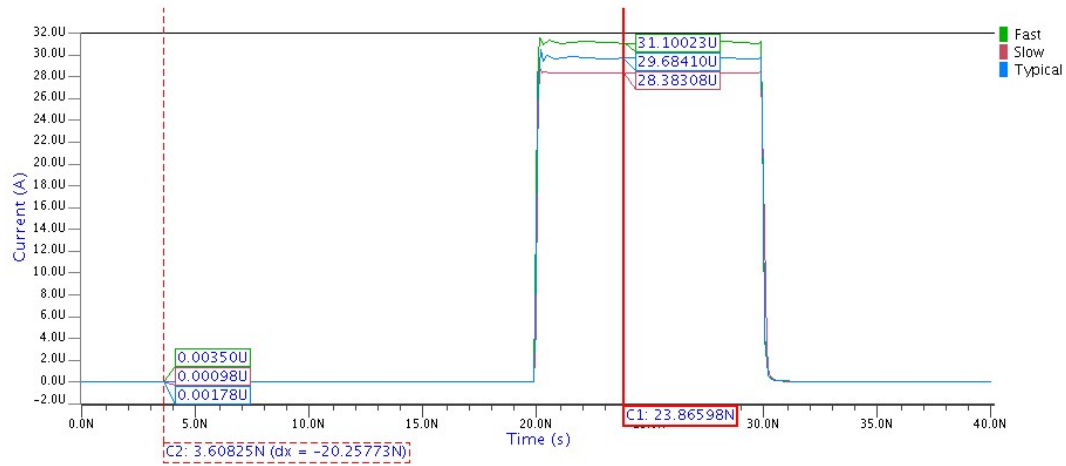


Figure 3.9: Variation of output current across different process corner in threshold circuit

The worst case rise delay or fall delay for the complement circuit is determined from switching of logic level 0 to 3 or vice versa respectively. The Figure 3.10 and Table 3.3 shows the rise time and fall time delay of the circuit

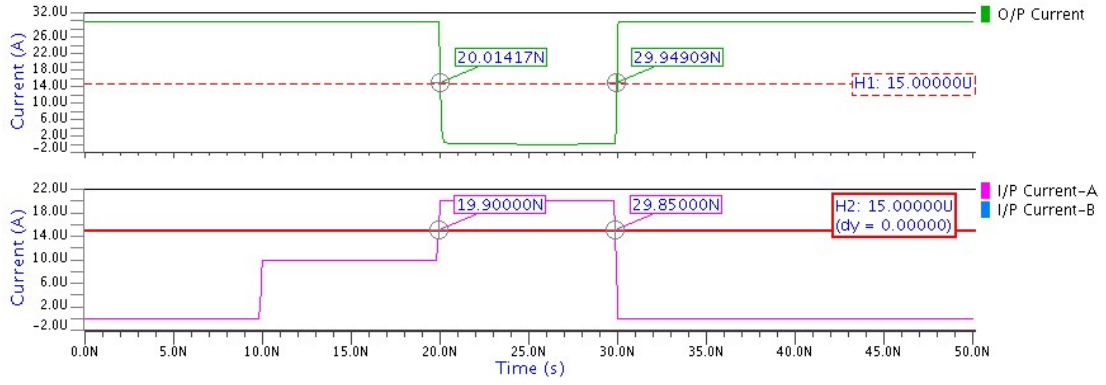


Figure 3.10: Worst case rise time and fall time delay of threshold circuit

Worst case rise time delay	0.09909 ns
Worst case fall time delay	0.11417 ns

Table 3.3: Worst case rise time and fall time delay of threshold circuit

3.4 Maximum Operator

The performance of the maximum circuit presented in Figure 2.5 is analyzed in terms of terms of wide temperature range and across different process corner. The variation of the output current for logic level 0,1,2,3 over wide temperature range from -40 to 120 degree are plotted in Figure 3.11

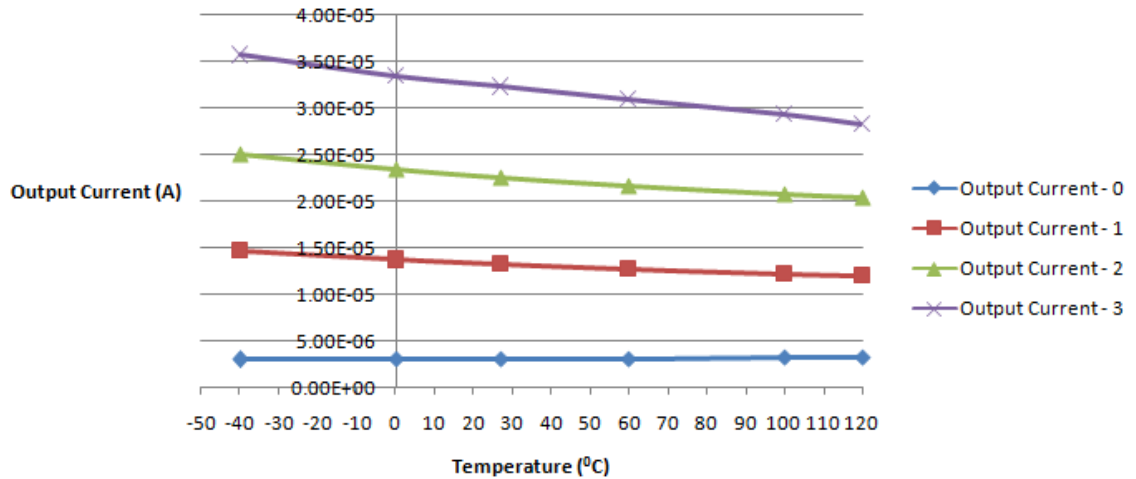


Figure 3.11: Variation of output current over wide temperature range in maximum circuit

The variation of output current for logic level 0,1,2,3 across different process corner is shown in Figure 3.12

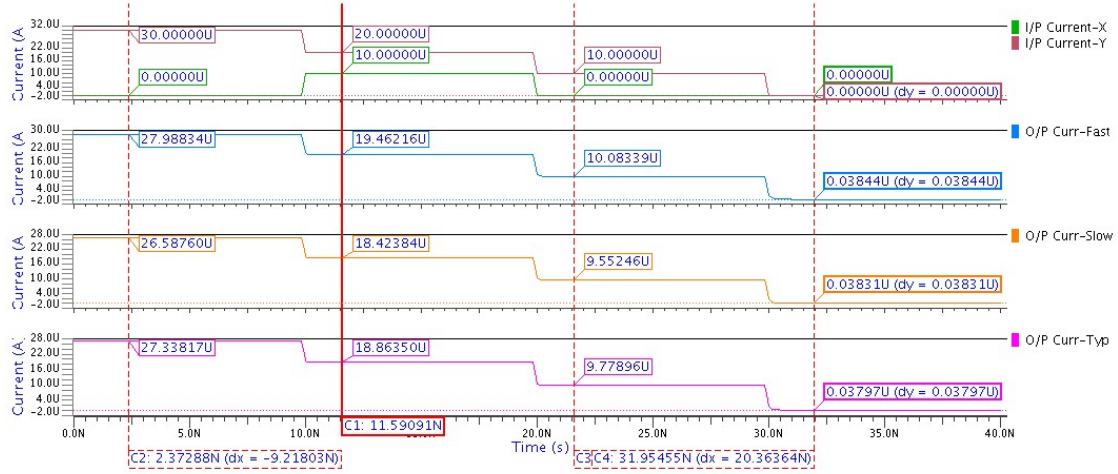


Figure 3.12: Variation of output current across different process corner in maximum circuit

The worst case rise delay or fall delay for the complement circuit is determined from switching of logic level 0 to 3 or vice versa respectively. The Figure 3.13 and Table 3.4 shows the rise time and fall time delay of the circuit

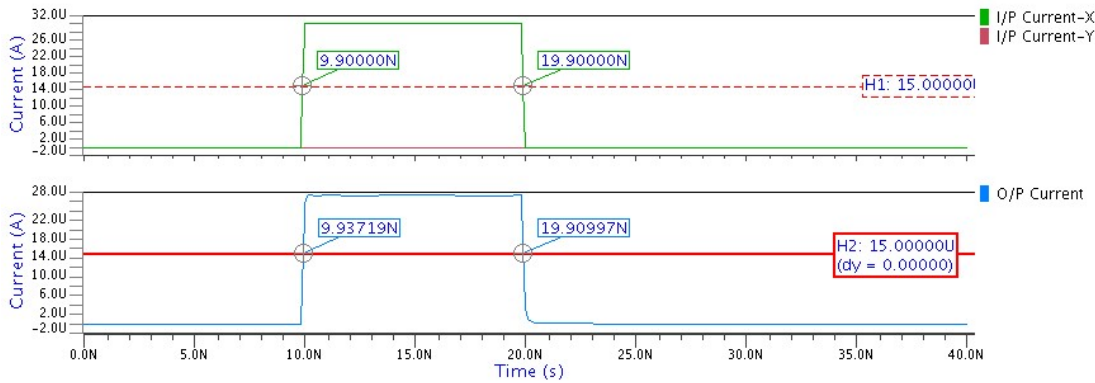


Figure 3.13: Worst case rise time and fall time delay of maximum circuit

Worst case rise time delay	0.03719 ns
Worst case fall time delay	0.00997 ns

Table 3.4: Worst case rise time and fall time delay of maximum circuit

3.5 Minimum Operator

The performance of the minimum circuit presented in Figure 2.4 is analyzed in terms of terms of wide temperature range and across different process corner. The variation of the output current for logic level 0,1,2,3 over wide temperature range from -40 to 120 degree are plotted in Figure 3.14

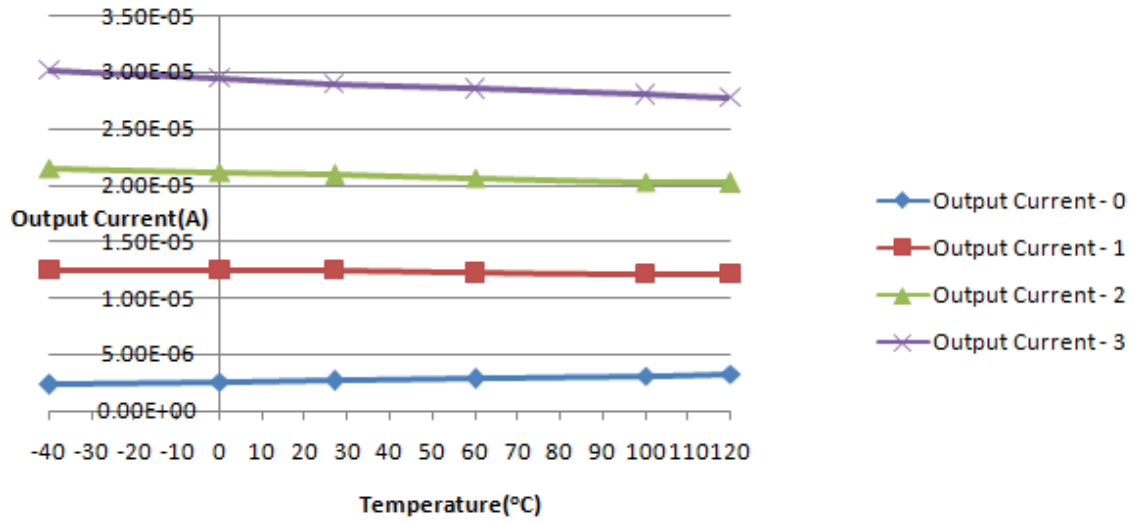


Figure 3.14: Variation of output current over wide temperature range in minimum circuit

The variation of output current for logic level 0,1,2,3 across different process corner is shown in Figure 3.15

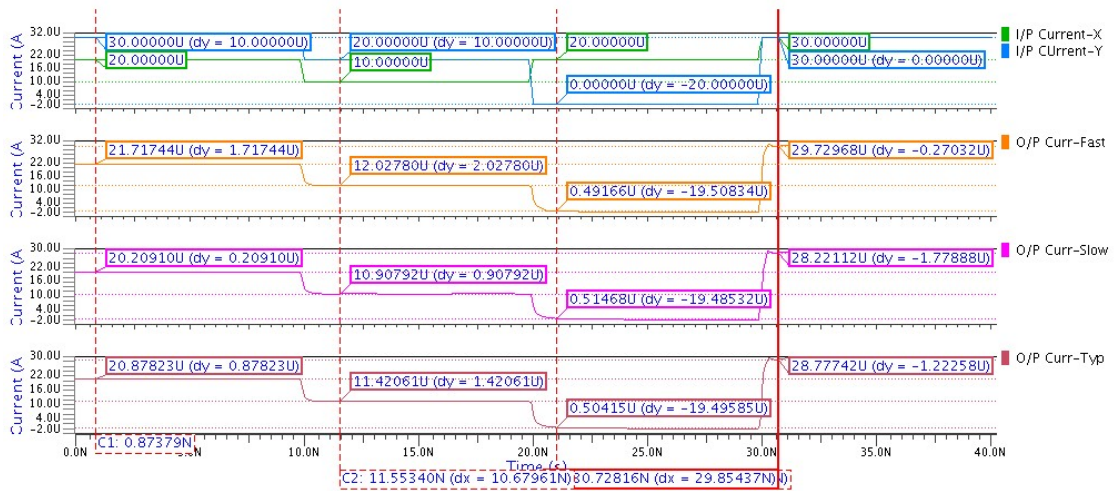


Figure 3.15: Variation of output current across different process corner in minimum circuit

The worst case rise delay or fall delay for the complement circuit is determined from switching of logic level 0 to 3 or vice verse respectively. The Figure 3.16 and Table 3.5 shows the rise time and fall time delay of the circuit

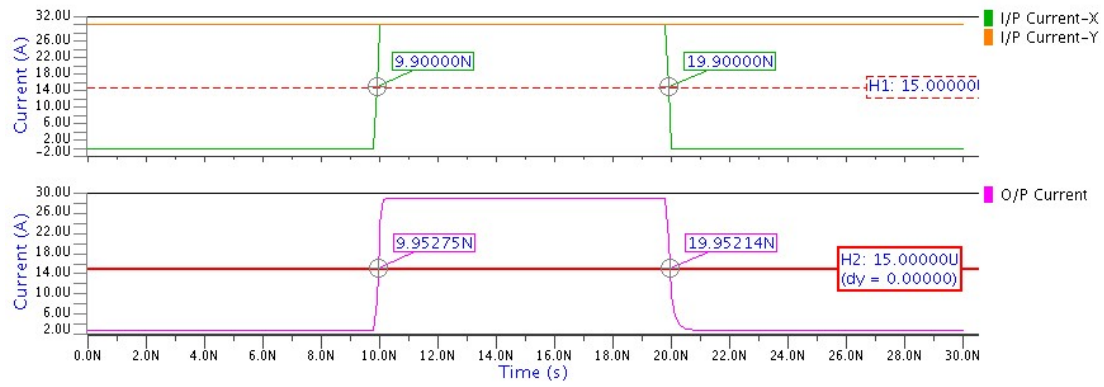


Figure 3.16: Worst case rise time and fall time delay of minimum circuit

Worst case rise time delay	0.05275 ns
Worst case fall time delay	0.05214 ns

Table 3.5: Worst case rise time and fall time delay of minimum circuit

Chapter 4

CMOS Current-Mode Binary/MVL Encoding and Decoding

The multiple valued logic circuits require encoding and decoding circuitry for interfacing them with on chip binary logic design. The conversion from binary voltage signal to multiple valued current signal is performed by encoder and from multiple valued current signals to binary voltage signal is done by decoder. The block diagram for the entire multivalued logic system with encoding and decoding is shown in Figure 4.1

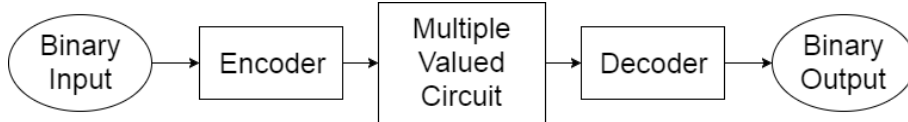


Figure 4.1: Block diagram of Multiple valued system

4.1 Encoder

The encoder circuit takes 2-bit binary input and generates 1 digit quaternary output or 4 quaternary current levels. For the n -bit binary input, the encoder circuit generates 2^n levels of output current. The reference current I_{ref} is applied to diode connected PMOS M1. This reference current is mirrored to PMOS M2 and M3 with current I and $2I$ respectively. The 2-bit binary input is applied as LSB and MSB to the series connected NMOS M4 and M5, which contributes to the output current I_{out} as shown in Figure 4.2. The operation of the encoder circuit for reference current $I_{ref} = 10\mu A$ is listed in Table 4.1

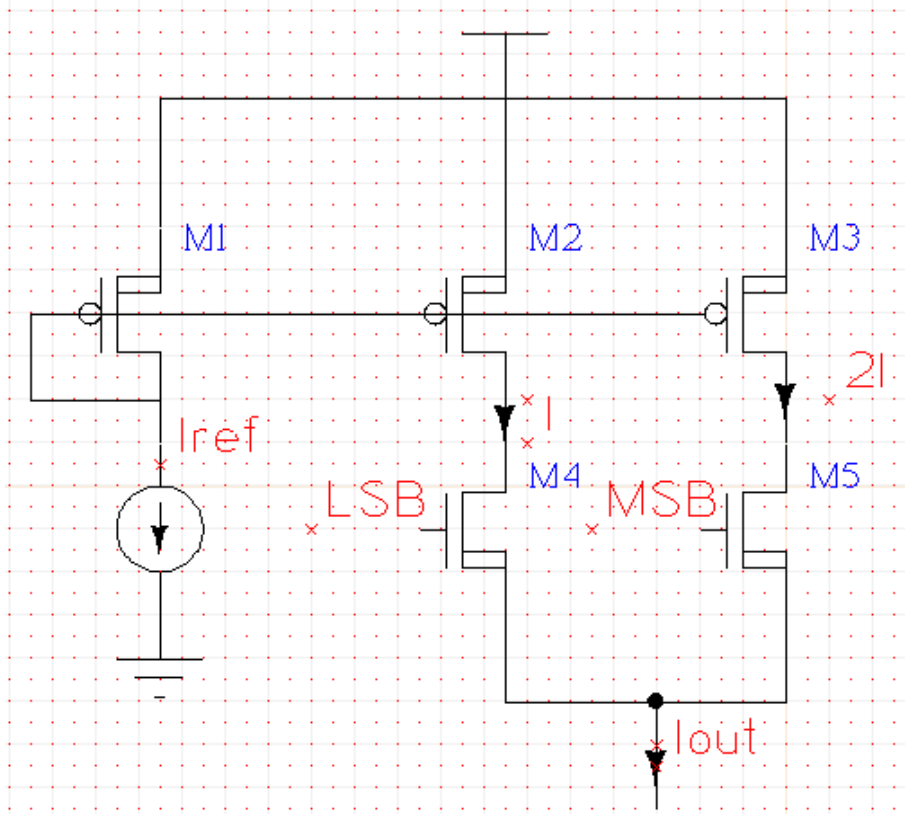


Figure 4.2: Encoder Circuit

MSB	LSB	Iout
0	0	$0\mu A$
0	1	$10\mu A$
1	0	$20\mu A$
1	1	$30\mu A$

Table 4.1: Operation table of encoder

4.2 Decoder

After encoding of binary signal to its multiple valued signal counterpart, multiple valued signal is processed in multiple valued circuit and it needs to be decoded again for the rest of the system. Decoder can be designed in two configurations as discussed below

4.2.1 Configuration 1

The operation of the decoder depends on current comparison. Multiple-valued input current is compared with the $(n-1)$ reference currents to produce $\log_2 n$ binary voltage signals as shown in Figure 4.3 from [5]. Appropriate combinational logic block is needed to convert $(n-1)$ comparator outputs to binary voltage signals.

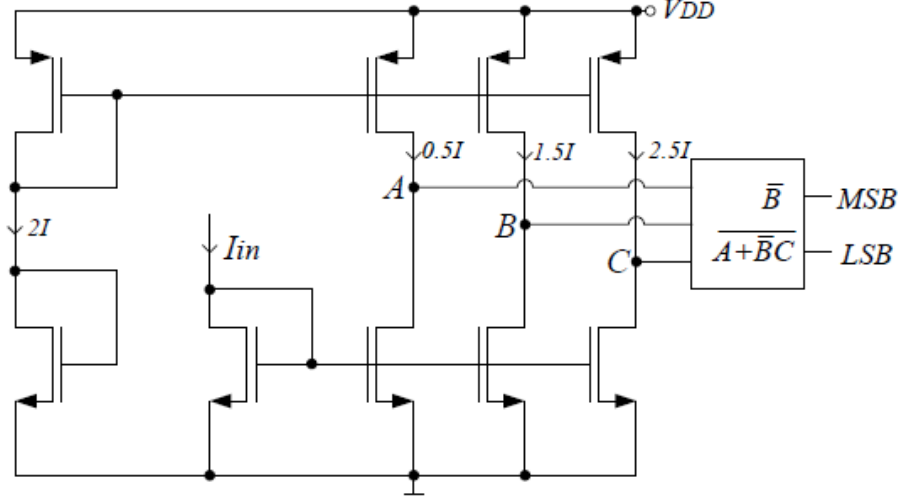


Figure 4.3: Decoder Circuit

4.2.2 Configuration 2

The Quaternary decoder is shown in Figure 4.4 from [4]. The circuit consists of the diode-connected input transistor M1, transistors M2 and M3 connected to replicate this input current, a reference current generating pair of transistors M4 and M5, transistors M6, M7 and M8 that replicate the reference current, a switching transistor M9, and two inverters. Transistor M4 and M5 generate a unit current I . Transistor M6, M7, and M8 generate threshold currents $1.5I$, $2I$, and $0.5I$ respectively. The decoder compares the generated threshold currents with the duplicated input currents at transistors M2 and M3. The decoder generates voltage-mode binary logic signal on output stage of 2^1 and 2^0 through the inverters. When $I_{in} < 0.5I$, the current through transistor M6 is greater than the current through transistor M2 and the current through transistor M8 is greater than the current through transistor M3, the output 2^1 and 2^0 of the decoder is 0 and 0 respectively and the transistor M9 is turned off. When $0.5I \leq I_{in} < 1.5I$, the current through transistor M6 is greater than the current through transistor M2 and the current through transistor M8 is less than the current through transistor M3, the output 2^1 and 2^0 of the decoder is 0 and 1 respectively and the transistor M9 is turned off. When $1.5I < I_{in} \leq 2.5I$, the current through transistor M6 is less than the current through transistor M2 and transistor M9 is turned on. The combined current through transistor M7 and transistor M8 is greater than the current of transistor M3. Therefore, the output 2^1 and 2^0 of the decoder is 1 and 0 respectively. When $I_{in} \geq 2.5I$, the current through transistor M6 is less than the current through transistor M2 and transistor M9 is turned on. The combined current through transistor M7 and transistor M8 is less than the current of transistor M3. Therefore, the output 2^1 and 2^0 of the decoder is 1 and 1 respectively. The operation of the proposed decoder is listed in Table 4.2.

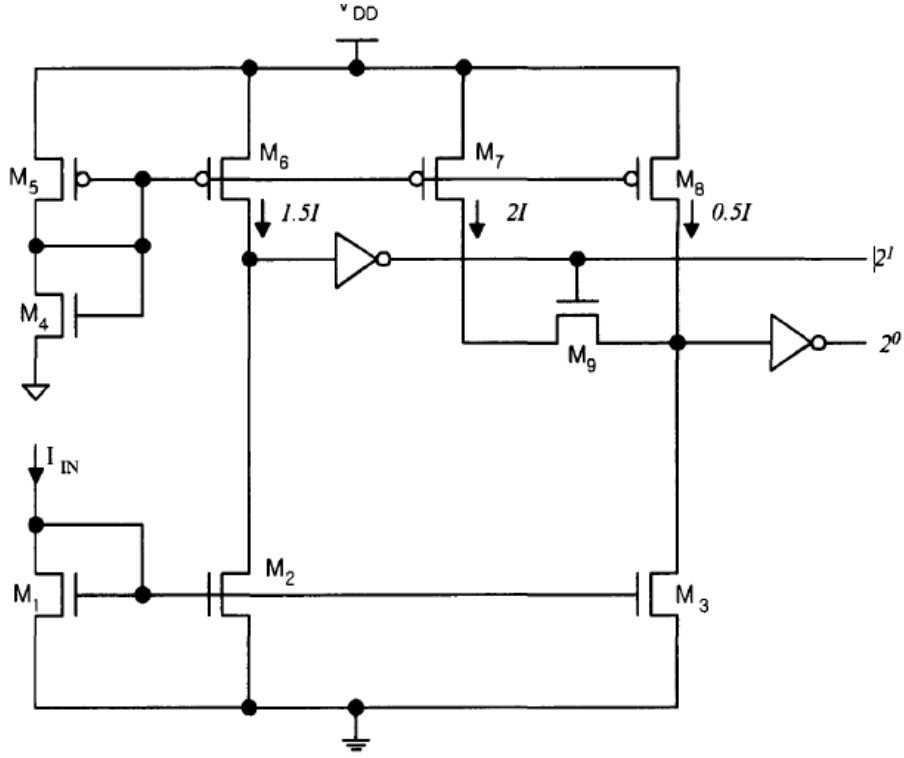


Figure 4.4: Decoder Circuit

Input Current (I_{in}) in μA	Output- 2^1	Output- 2^0
$I_{in} < 0.5I$	0	0
$0.5I \leq I_{in} < 1.5I$	0	1
$1.5I \leq I_{in} < 2.5I$	1	0
$I_{in} \geq 2.5I$	1	1

Table 4.2: Operation table of decoder

Chapter 5

Combinational MVL circuits

The output of any combinational circuit depends upon the present input at any time instant by some boolean expressions. This same concept is also applicable to multiple valued logic circuits. The fundamental multiple valued logic operators discussed previously in chapter 2 can be used to realize any multiple valued combinational circuits.

Some of the current mode multivalued circuits such as Multiplexer and Demultiplexer are proposed in this chapter.

5.1 Multiplexer

In this section, radix-4, 4x1 multiplexer is designed. For unique selection of 4 inputs, 2 select line is required in binary logic and 1 select line is sufficient in quaternary logic. The block diagram of radix-4, 4x1 multiplexer is shown in Figure 5.1.

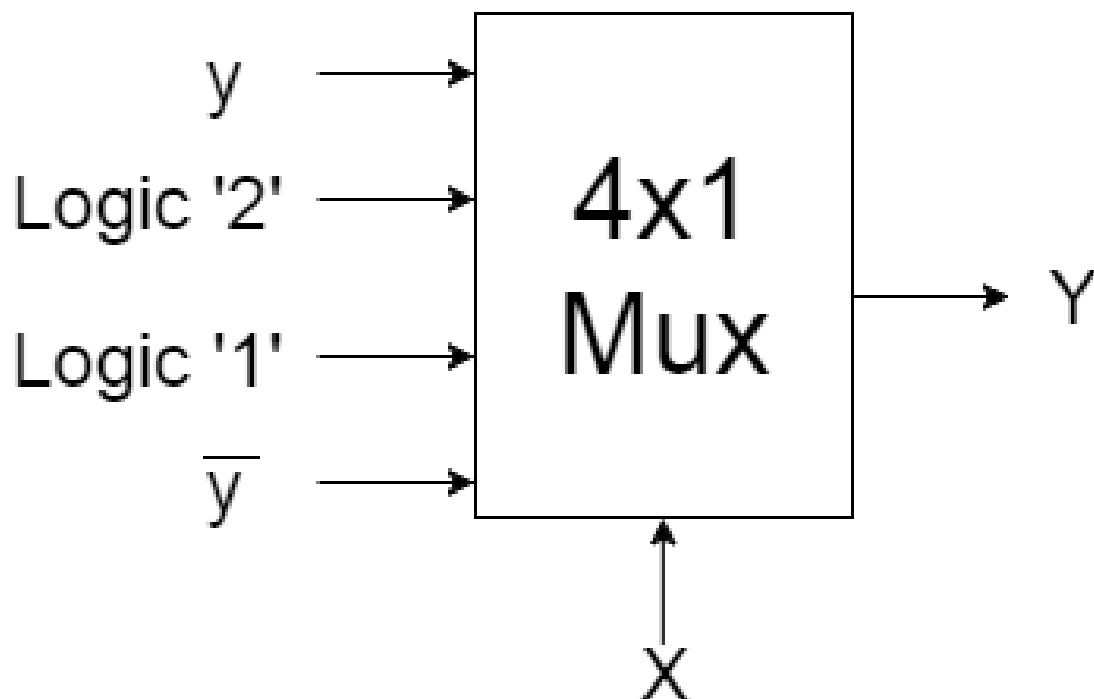


Figure 5.1: Radix-4, 4x1 Multiplexer

The quaternary select line X can take 4 values to select any of 4 input. The values of select line, input and output of this multiplexer is shown in Table 5.1

X	Y
0	y
1	Logic '2'
2	Logic '1'
3	$\bar{y}$

Table 5.1: Selection table of multiplexer

The radix-4, 4x1 multiplexer is designed using lower and upper threshold block as shown in Figure 5.2.

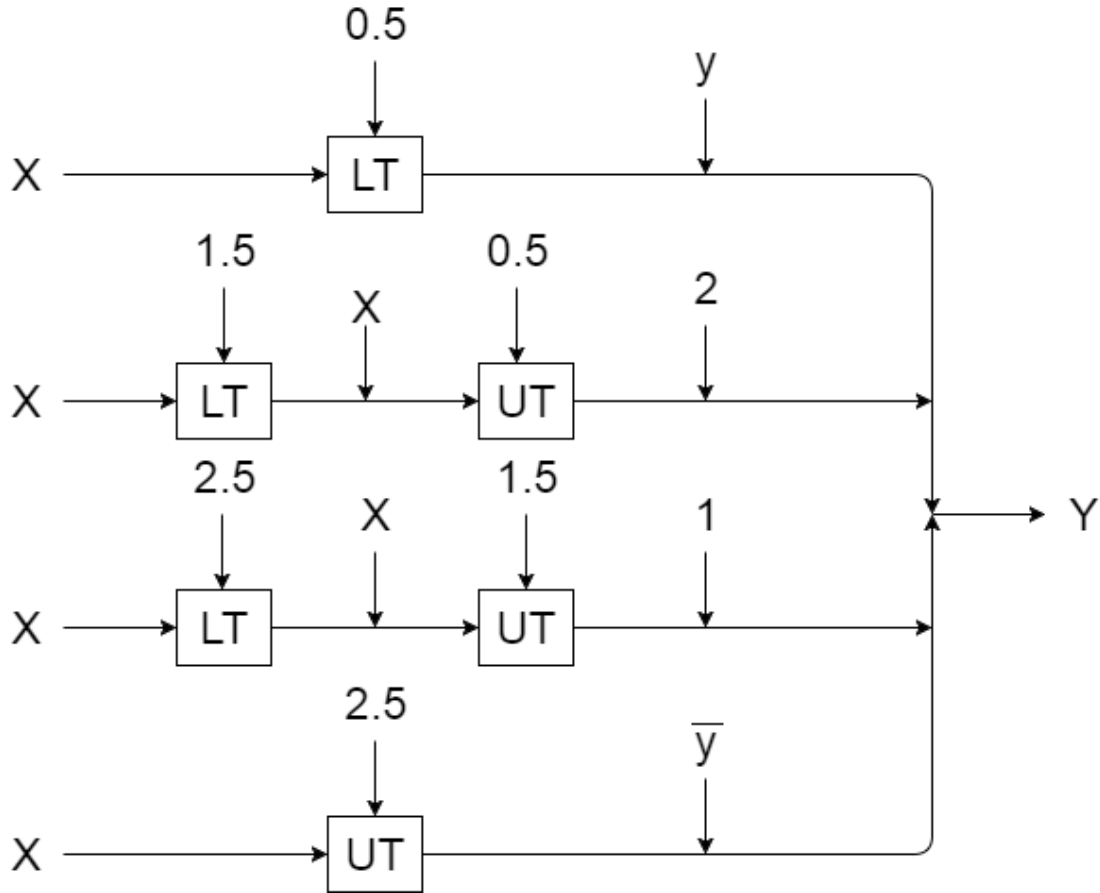


Figure 5.2: Radix-4, 4x1 Multiplexer

The brief functionality of upper threshold and lower threshold block is shown in Figure 5.3. For upper threshold UT, if X is greater than Y , then output is Z else output is 0. For lower threshold LT, if X is less than Y , then output is Z else output is 0.

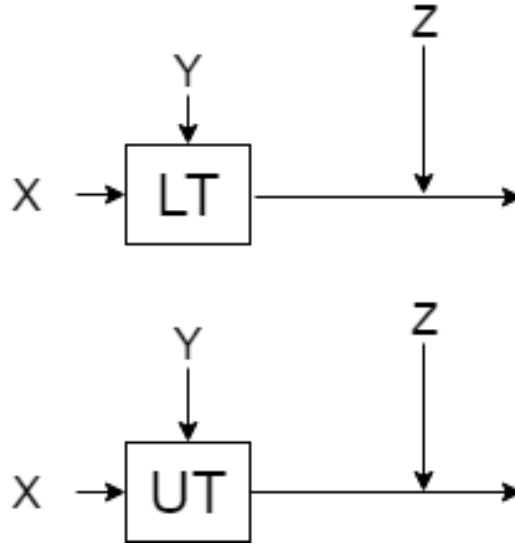


Figure 5.3: Lower and Upper threshold circuit block diagram

The simulation results showing the input, output and select line of the multiplexer is shown in Figure 5.4

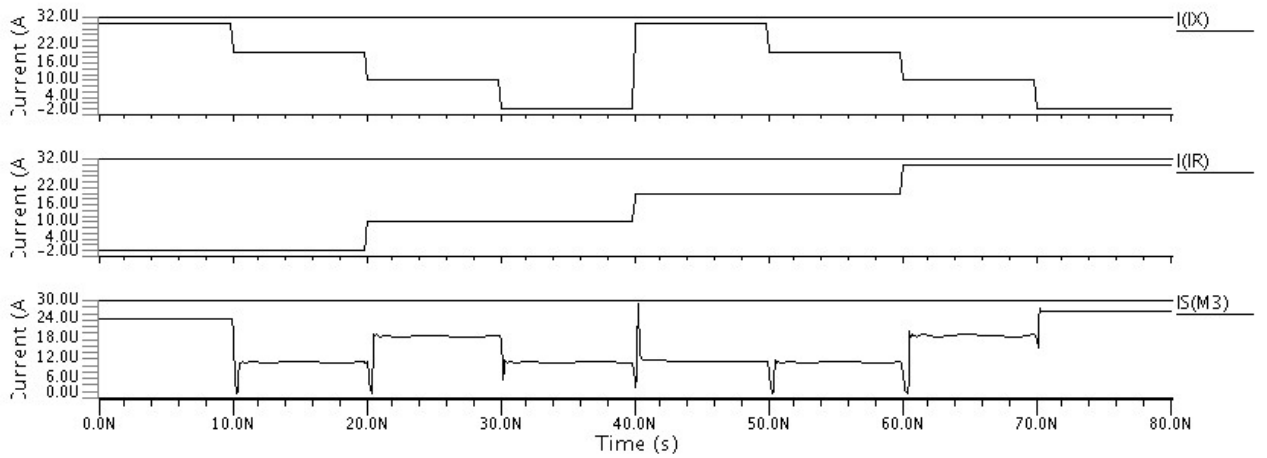


Figure 5.4: Simulation result of multiplexer

5.2 Demultiplexer

In this section, radix-4, 1x4 demultiplexer is designed. For mapping of the input to one of the 4 output, 2 select line is required in binary logic but in quaternary logic only 1 select line is sufficient. The block diagram of radix-4, 1x4 demultiplexer is shown in Figure 5.5.

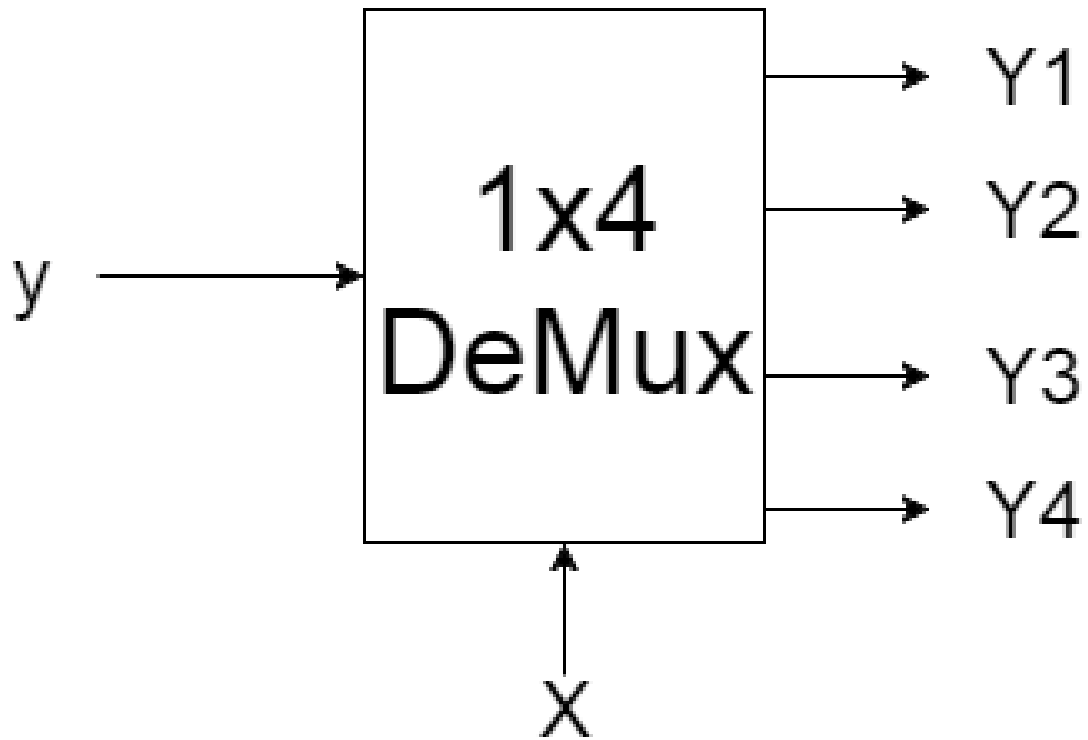


Figure 5.5: Radix-4, 1x4 Demultiplexer

The operation of the proposed demultiplexer is listed in Table 5.2 which shows the selection of output depending upon select line X. The radix-4, 1x4 demultiplexer

Select Line X	Input	Y1	Y2	Y3	Y4
0	y	y	0	0	0
1	y	0	y	0	0
2	y	0	0	y	0
3	y	0	0	0	y

Table 5.2: Selection table of demultiplexer

is designed using lower and upper threshold block as shown in Figure 5.6.

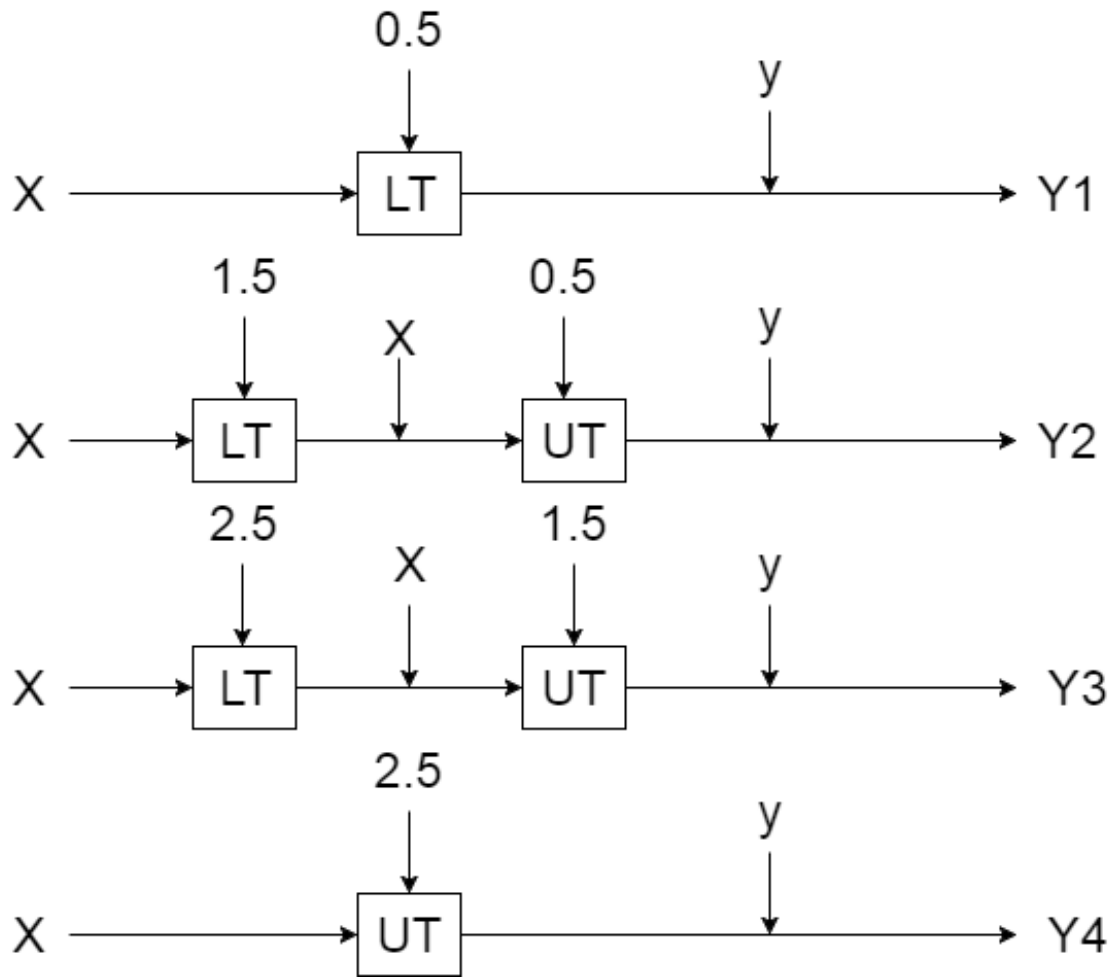


Figure 5.6: Radix-4,1x4 Demultiplexer

The simulation results showing the input, output and select line of demultiplexer is shown in Figure 5.7 and Figure 5.8

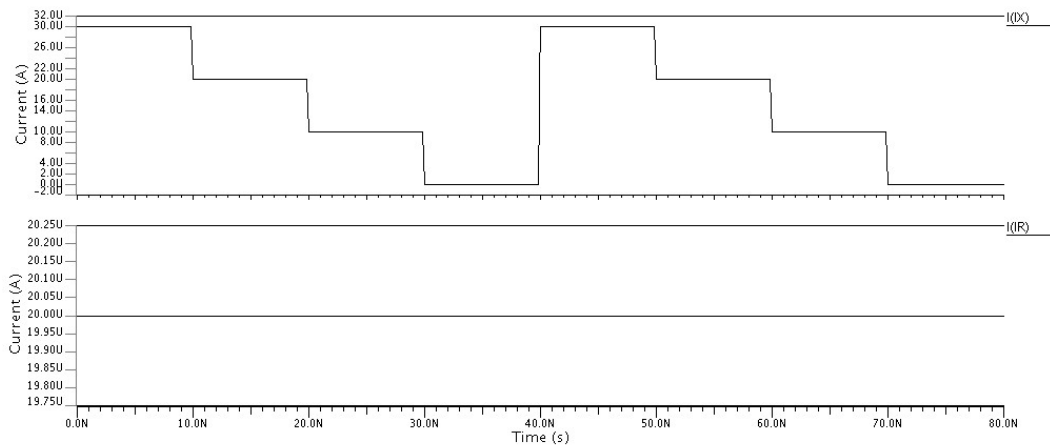


Figure 5.7: Input simulation result of the demultiplexer

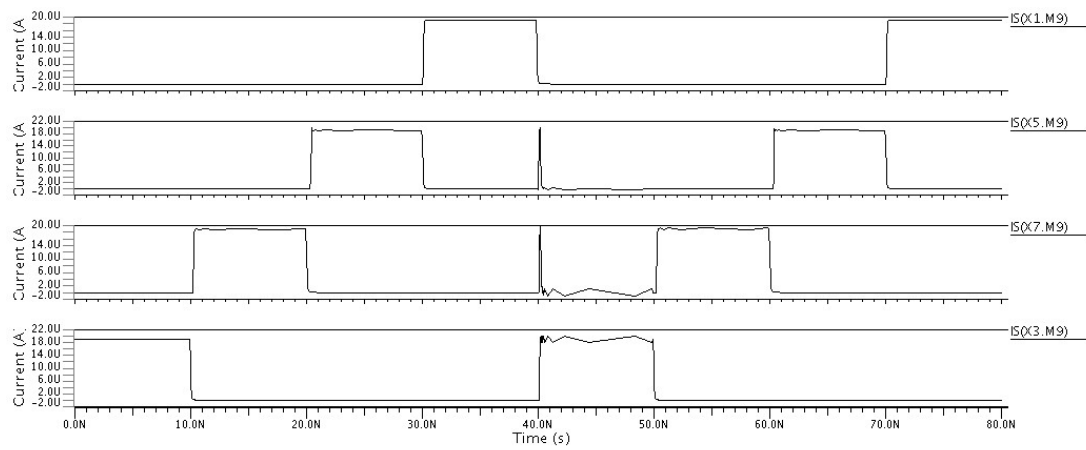


Figure 5.8: Output simulation results of the demultiplexer

Chapter 6

Sequential MVL circuits

The output of the sequential circuit depends upon the present input as well as the past output of the circuit. Sequential circuits can be realized with memory and combinational circuits as shown in Figure 6.1.

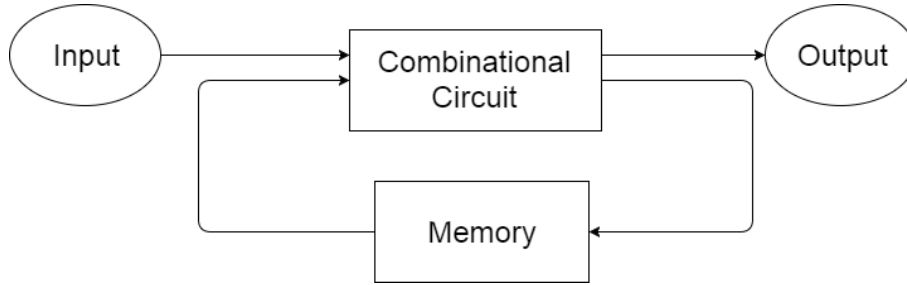


Figure 6.1: Block diagram of sequential circuit

The memory or storage element is required to hold and feedback the output to input. The memory element can be a latch or flip flop.

6.1 Quaternary Latch

Quaternary latch is the memory element that can hold the quaternary logic values such as 0,1,2,3. The reference current taken here is $10\mu A$. Quaternary logic level 0,1,2,3 is represented by current level 0,10,20,30 μA . In this study, Current mode quaternary latch circuit proposed in [5] is discussed.

This circuit operates in two phase, SETUP (clock signal "clk" is high) and HOLD (clock signal "clk" is low). When clock signal "clk" is high, the Input current " I_{in} " passing through diode connected transistor Min is mirrored by three NMOS transistors M4,M5,M6. The reference current I_{ref} of $10\mu A$ is passed through diode connected transistor PMOS Mref, which is mirrored by three PMOS transistors M1,M2 and M3. W/L of three PMOS M1,M2 and M3 are adjusted to get threshold current of 5,15 and 25 μA respectively to detect logic level 1,2 and 3. Three mirrored NMOS M4,M5 and M6 and three mirrored PMOS M1,M2 and M3 together form the current comparator. When input current is less then the threshold current of comparator, the output node a,b,c can fall to logic low. The output of three

comparator a,b,c is feeded to the three standard CMOS inverter to get output A,B,C respectively. The reference current I_{ref} of $10\mu A$ is mirrored to PMOS transistor M8,M9 and M10. The output of standard inverter A,B and C drives the series connected NMOS M11,M12 and M13 respectively. The diode connected NMOS M14 holds the total regenerated current I_{rg} . When clock signal 'clk' is low, the regenerated current I_{rg} is mirrored to M4, M5 and M6 in positive feedback. By this feedback, stable regenerated current I_{rg} is maintained in negative cycle of clock. The regenerated current is mirrored to transistor M16, M17 and M18 to feed the latch output to next corresponding stage. The circuit diagram of the Quaternary latch is shown in Figure 6.2

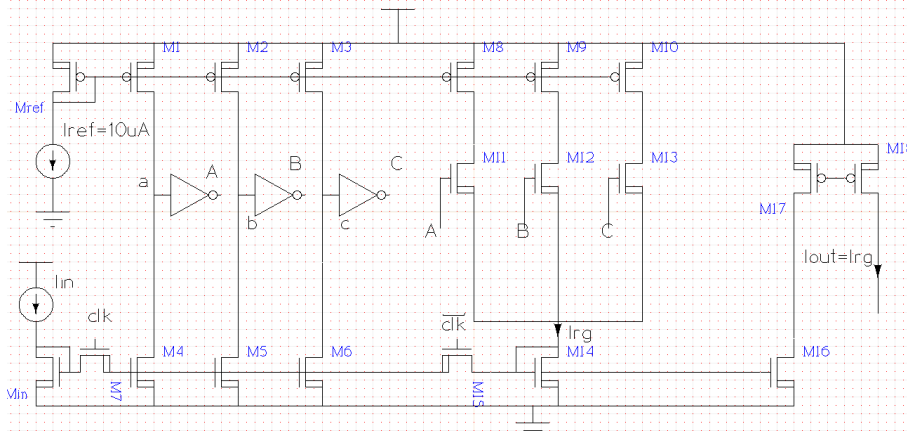


Figure 6.2: Current mode CMOS Quaternary Latch

The simulation result of the quaternary Latch is shown in Figure 6.3. In this Figure, the output current follows the input current in positive cycle of the clock and holds the value till next positive cycle.

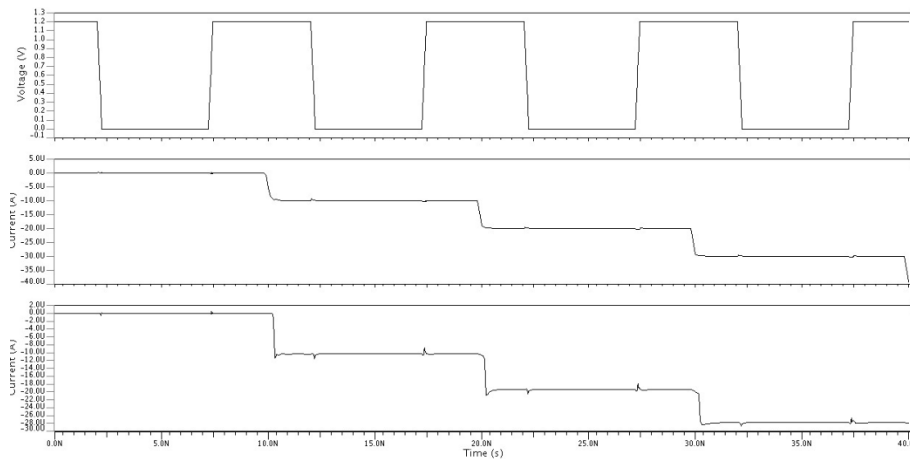


Figure 6.3: Simulation result of Current Mode CMOS Quaternary Latch

Since this circuit performs both latching and restoring, the positive feedback does not cause any oscillations in output.

6.2 Multivalued D Flip-Flop

SR and JK Flip-Flop needs complement operation for their realization which increases transistor cost and also SR Flip-Flop has indeterminate state. Therefore, to reduce complexity, D Flip-Flop is realized in multiple valued configurations. All the sequential circuits studied in this work uses Multiple valued D Flip-Flop. The characteristic equation of D Flip-Flop is as follows:

$$Q_{n+1} = D \quad (6.1)$$

This equation is valid for both binary and multivalued logic.

The transition table of multiple valued D Flip-Flop is shown in Table 6.1

		D						
		0	1	2	3	—	r-2	r-1
Q	0	0	1	2	3	—	r-2	r-1
	1	0	1	2	3	—	r-2	r-1
	2	0	1	2	3	—	r-2	r-1
	3	0	1	2	3	—	r-2	r-1
	—	0	1	2	3	—	r-2	r-1
	r-2	0	1	2	3	—	r-2	r-1
	r-1	0	1	2	3	—	r-2	r-1

Table 6.1: Transition table of D Flip-flop

The Multivalued D Flip-Flop can be derived by cascading two Quaternary latch discussed in Section 6.1 in master slave fashion as shown in Figure 6.4 .

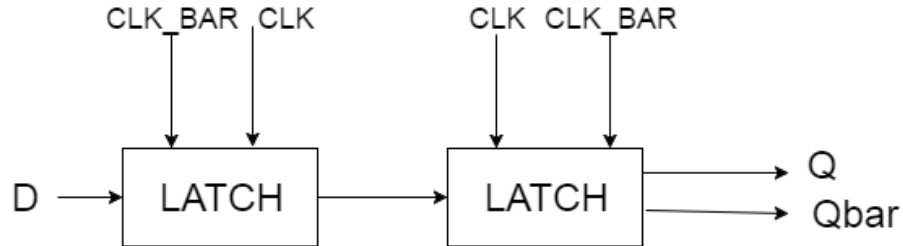


Figure 6.4: Block diagram of D Flip-Flop

The simulation result of the Current mode multiple valued D Flip-Flop is shown in Figure 6.5. In this Figure, the output current follows the input on the positive edge of the clock and holds its value till next positive edge of the cycle.

6.3 Modulo-4 Counter

In this section, D Flip-Flop proposed in Section 6.2 is used to design a 1 Digit Modulo-4 Counter. The counting diagram is shown in Figure 6.6.

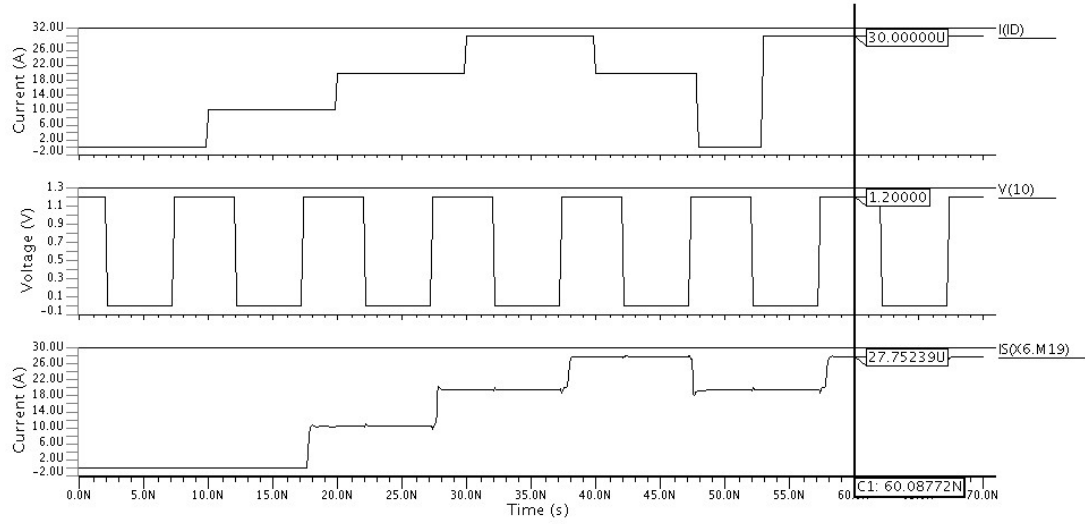


Figure 6.5: Simulation Results of Current Mode multivalued D Flip-Flop

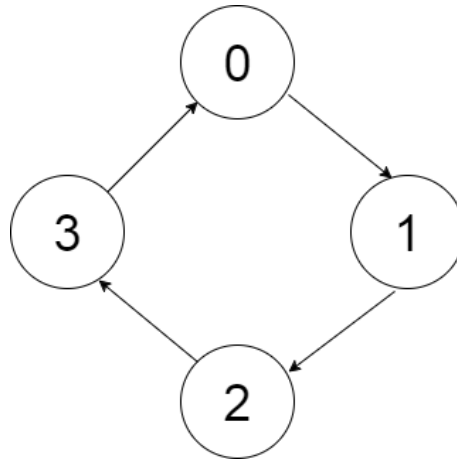


Figure 6.6: Counting diagram of Modulo-4 Counter

The state equation of this counter is same as the characteristic equation of the D Flip-flop. Based on this counting diagram, excitation table for this counter is shown in Table 6.2

Q_n	Q_{n+1}	D
0	1	1
1	2	2
2	3	3
3	0	0

Table 6.2: Excitation table of Modulo-4 Counter

The block diagram of 1 Digit Modulo-4 Counter is shown in Figure 6.7

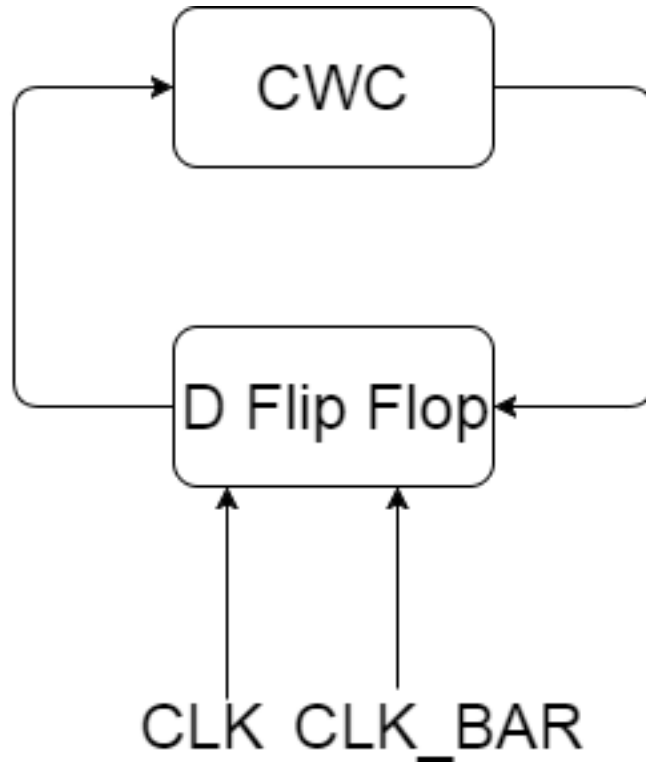


Figure 6.7: Block diagram of Modulo-4 Counter

The simulation results of 1 Digit Modulo-4 Counter is shown in Figure 6.8. At each positive edge of the clock, output current increments with unit reference current of $10\ \mu A$ because of clockwise cyclic circuit in feedback loop.

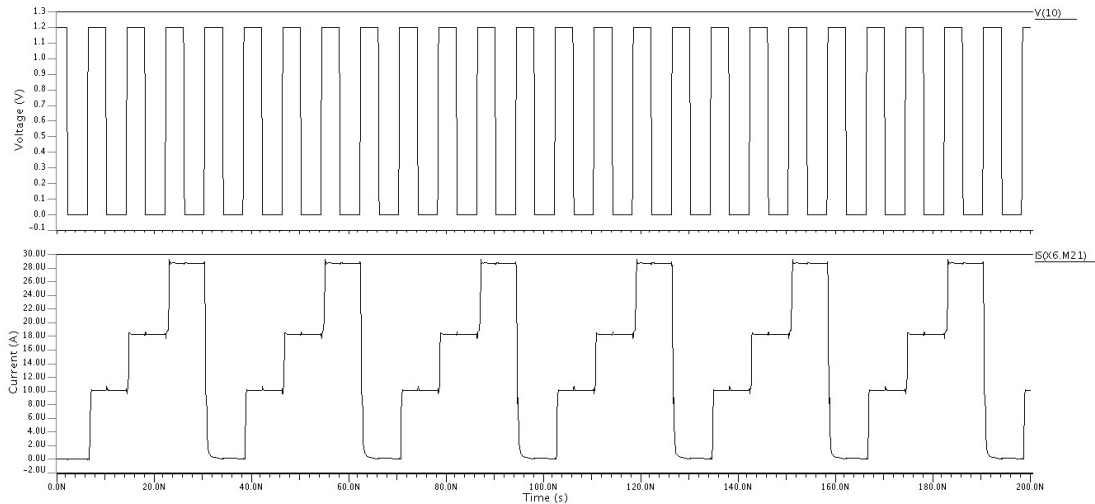


Figure 6.8: Simulation results of Modulo-4 Counter

6.4 Modulo-16 Counter

Modulo-16 counter can be realized with 4-bits as 0000,0001,0010....1111,0000.. in binary and with 2-digits as 00,01,02....33,00 in quaternary logic. The counter di-

agram of Modulo-16 counter implemented in Quaternary logic is shown in Figure 6.9

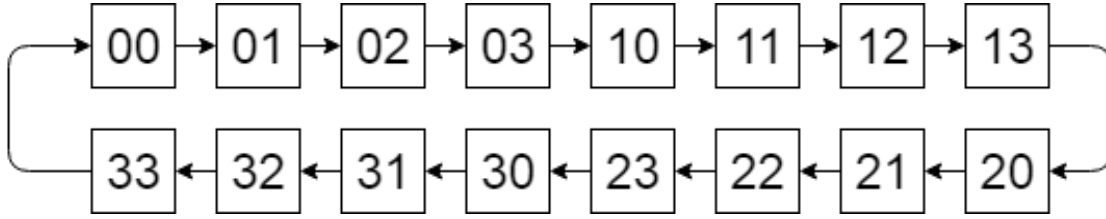


Figure 6.9: Counting diagram of Modulo-16 Counter

Based on the counting diagram, excitation table for this counter is shown in Table 6.3

Q_1	Q_0	Q_{1+}	Q_{0+}	D_1	D_0
0	0	0	1	0	1
0	1	0	2	0	2
0	2	0	3	0	3
0	3	1	0	1	0
1	0	1	1	1	1
1	1	1	2	1	2
1	2	1	3	1	3
1	3	2	0	2	0
2	0	2	1	2	1
2	1	2	2	2	2
2	2	2	3	2	3
2	3	3	0	3	0
3	0	3	1	3	1
3	1	3	2	3	2
3	2	3	3	3	3
3	3	0	0	0	0

Table 6.3: Excitation table of Modulo-16 Counter

The LSB of the Modulo-16 counter continuously counts as 0,1,2,3,0,... The output of first D-Flip flop generating the least significant bit(LSB) is fed to the clock generation circuit. The clock generation circuit generates clock for the D Flip-Flop which is generating the most significant bit(MSB). As soon as the LSB digit reaches logic level 3, the clock generator creates the positive level of clock for MSB D Flip-flop. The block diagram of Modulo-16 counter is as shown in Figure 6.10. The circuit diagram of clock generator is as shown in Figure 6.11 from [5].

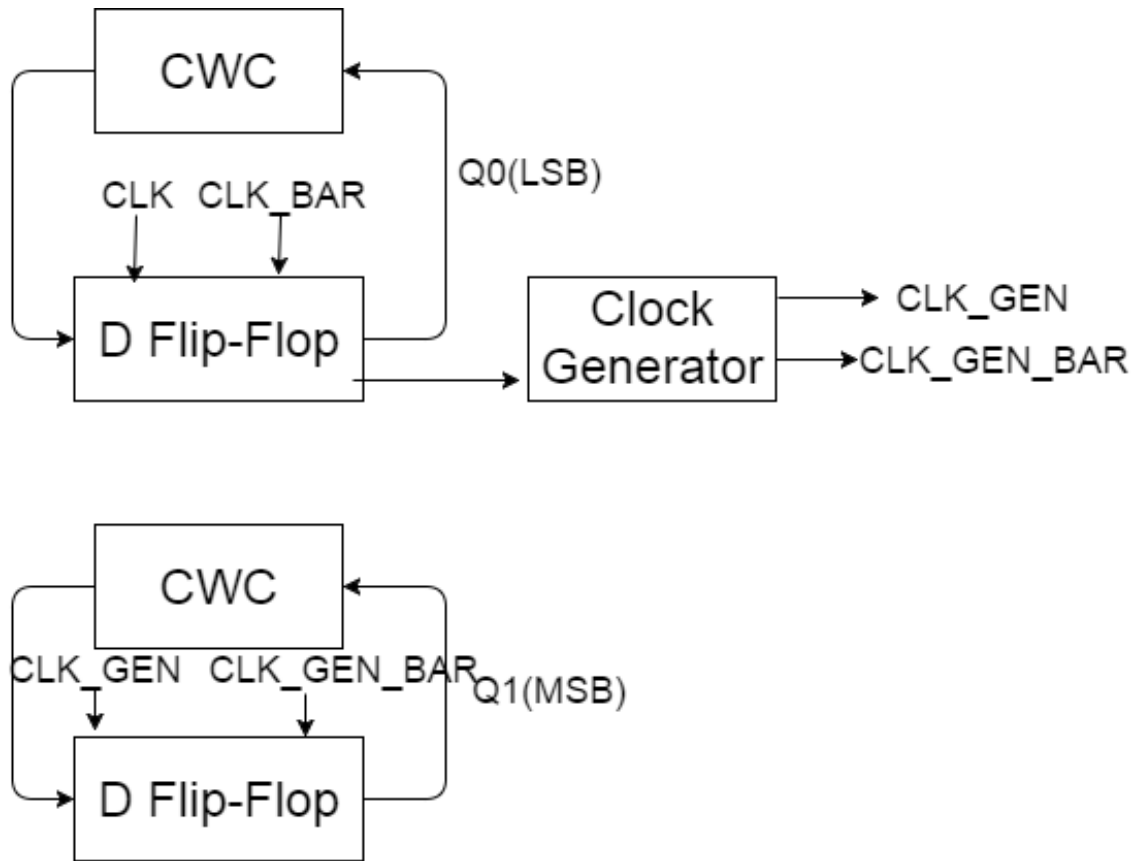


Figure 6.10: Block diagram of Modulo-16 Counter

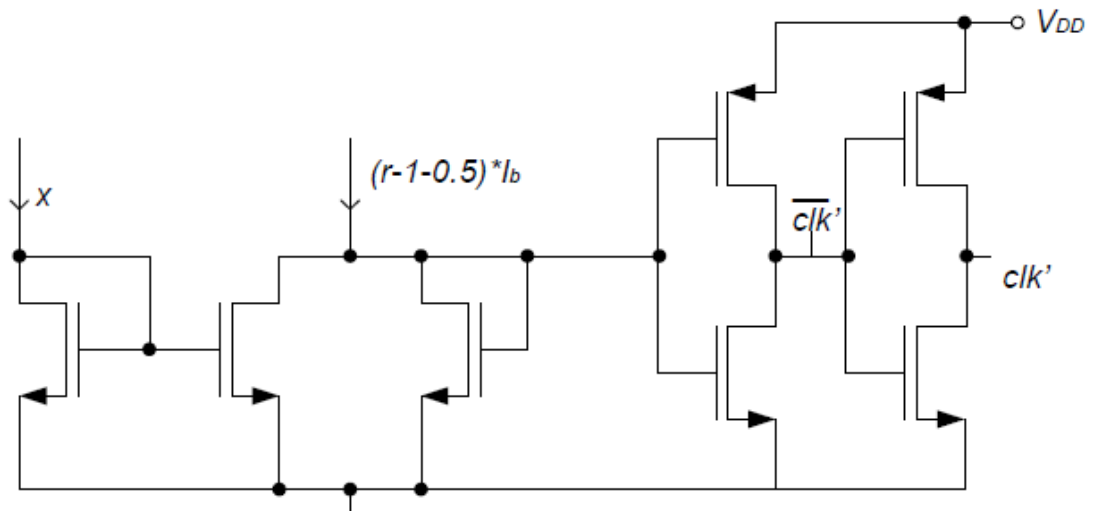


Figure 6.11: Circuit diagram of clock generation circuit

The simulation result of the 2 Digit Modulo-16 Counter is shown in Figure 6.12.

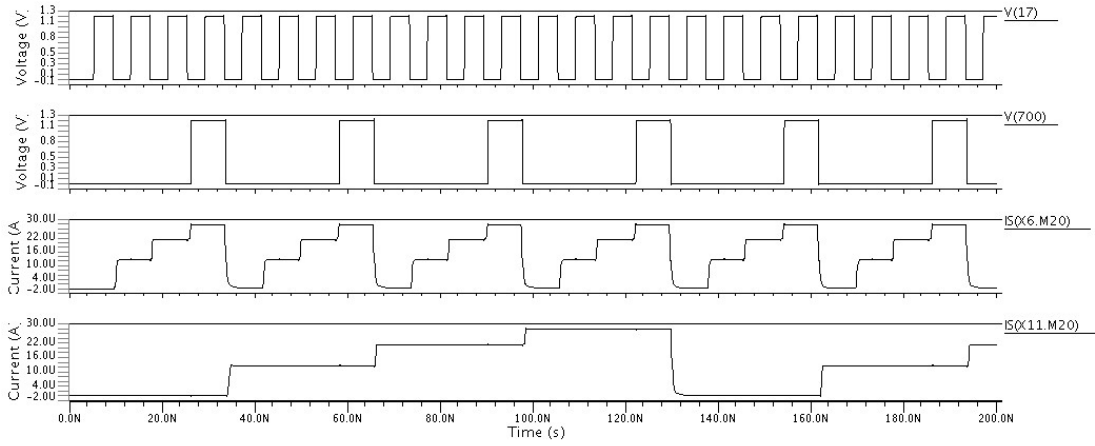


Figure 6.12: Simulation result of 2-digit Modulo 16 Counter

6.5 Arbitrary Selected State Diagram

In this section, two arbitrary selected State diagram are designed by using basic multivalued functional set discussed in Chapter 2 to further enhance the study of current mode multiple valued circuits.

6.5.1 State Diagram 1

The state equation for this arbitrary state diagram is given by :

$$Q_{n+1} = {}^2X^3 + \overline{Q_n} \quad (6.2)$$

$$Q_{n+1} = \max({}^2X^3, \overline{Q_n}) \quad (6.3)$$

The state table of this state diagram is shown in Table 6.4. The block diagram for this state diagram is shown in Figure 6.13

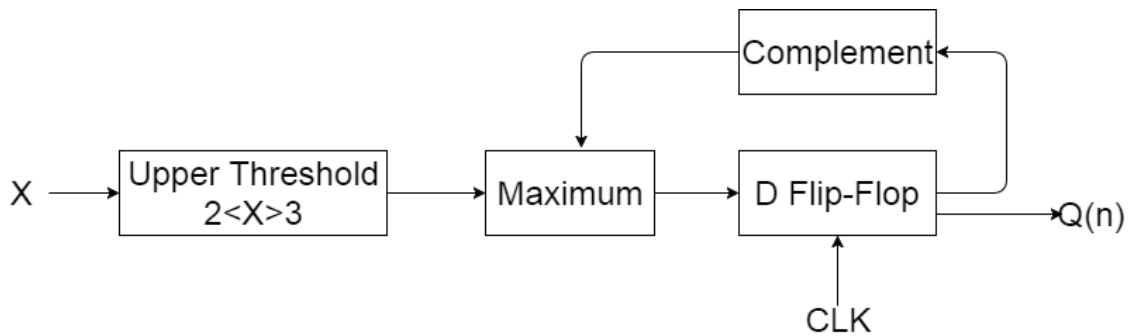


Figure 6.13: Block diagram of state diagram - 1

The simulation result of this state diagram is shown in Figure 6.14

X	Q_n	Q_{n+1}
0	0	3
0	1	2
0	2	1
0	3	0
1	0	3
1	1	2
1	2	1
1	3	0
2	0	3
2	1	2
2	2	2
2	3	2
3	0	3
3	1	3
3	2	3
3	3	3

Table 6.4: State table of state diagram - 1

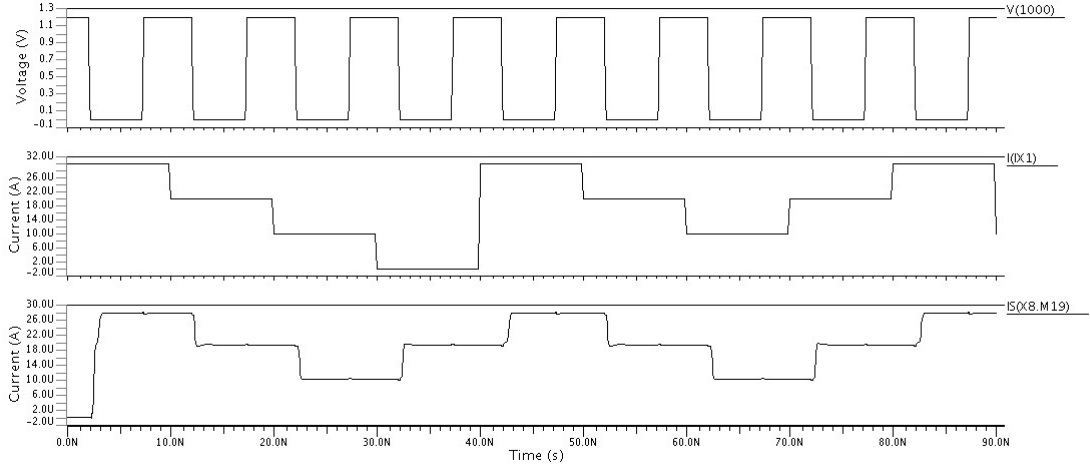


Figure 6.14: Simulation result of state diagram - 1

6.5.2 State Diagram 2

The state equation for this arbitrary state diagram is given by :

$$Q_{n+1} = \overrightarrow{Q_n} + \overline{X} \cdot Q \quad (6.4)$$

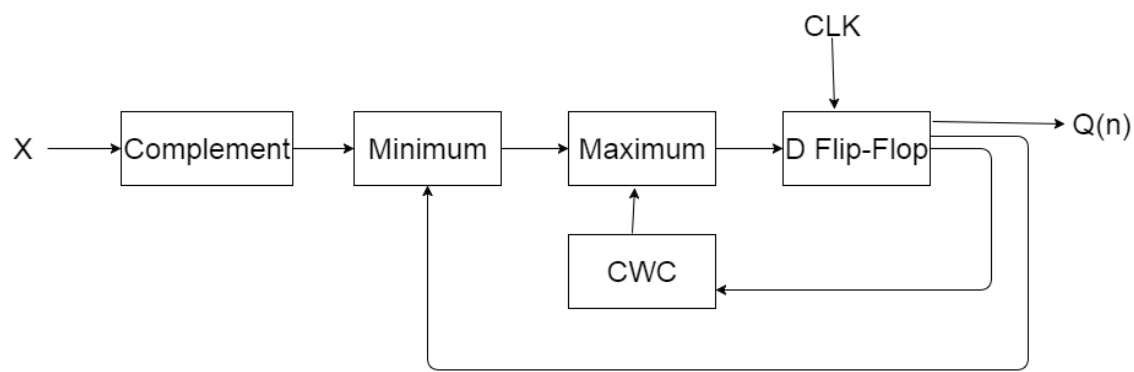
$$Q_{n+1} = \max(\overrightarrow{Q_n}, \min(\overline{X}, Q)) \quad (6.5)$$

The state table of this state diagram is shown in Table 6.5. The block diagram for this state diagram is shown in Figure 6.15.

The simulation result of this state diagram is shown in Figure 6.16

X	Q_n	Q_{n+1}
0	0	1
0	1	2
0	2	3
0	3	3
1	0	1
1	1	2
1	2	3
1	3	2
2	0	1
2	1	2
2	2	3
2	3	1
3	0	1
3	1	2
3	2	3
3	3	0

Table 6.5: State table of state diagram - 2



Text

Figure 6.15: Block diagram of state diagram - 2

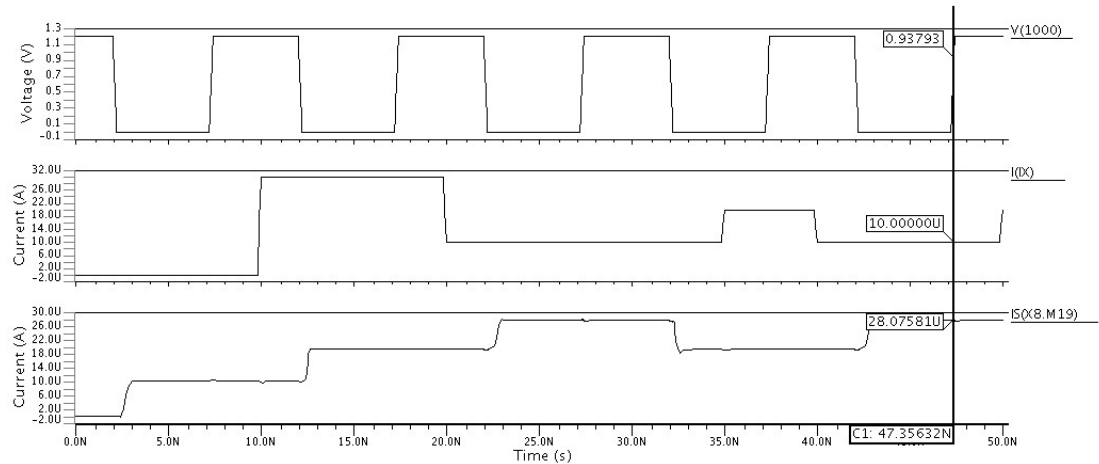


Figure 6.16: Simulation result of state diagram - 2

Chapter 7

Comparison between Multiple Valued and Binary Circuits

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. Although adders can be constructed for many number representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. Binary adders can be broadly classified as Half adder and Full adder. In this section Quaternary valued Full adder is proposed and compared with its binary equivalent. The digit '3' in quaternary is equivalent to '11' in binary. Therefore, single digit Quaternary full adder is equivalent to 2-bit binary parallel adder.

7.1 Quaternary Full adder

The Quaternary Full adder can be realized using clockwise cyclic operator (CWC). The circuit diagram of the Quaternary adder is shown in Figure 7.1. The simulation result of Quaternary full adder is shown in Figure 7.2

$$FA : \vec{x}^{y+Cin} = \begin{cases} x + y + Cin & \text{if } x + y + Cin \leq r - 1 \\ x + y + Cin - r, & \text{otherwise} \end{cases} \quad (7.1)$$

Quaternary full adder is compared with 2-bit binary parallel adder in terms of number of transistors, power consumption. For comparison, same input data set is considered say $x=2$ $y=1$ $Cin=1$ in Quaternary logic and $x1=1$, $x0=0$, $y1=0$ and $y0=1$ and $Cin=1$.

The block diagram of 2-bit binary parallel adder is shown in Figure 7.3

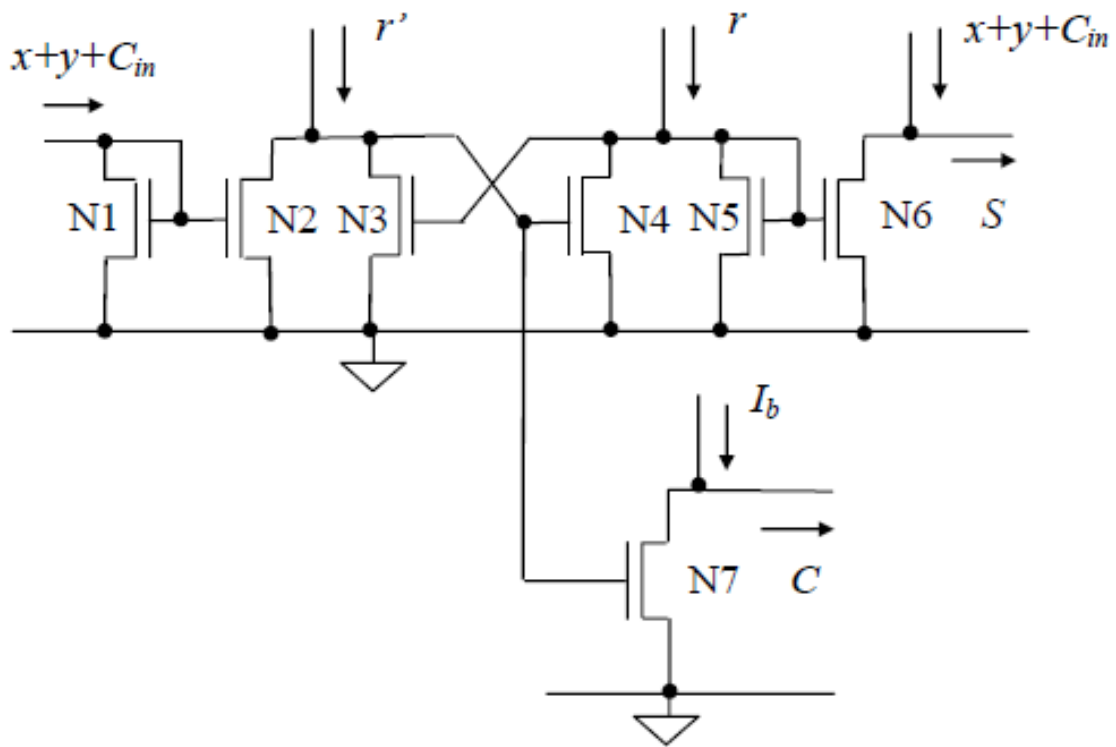


Figure 7.1: Multiple valued full adder circuit

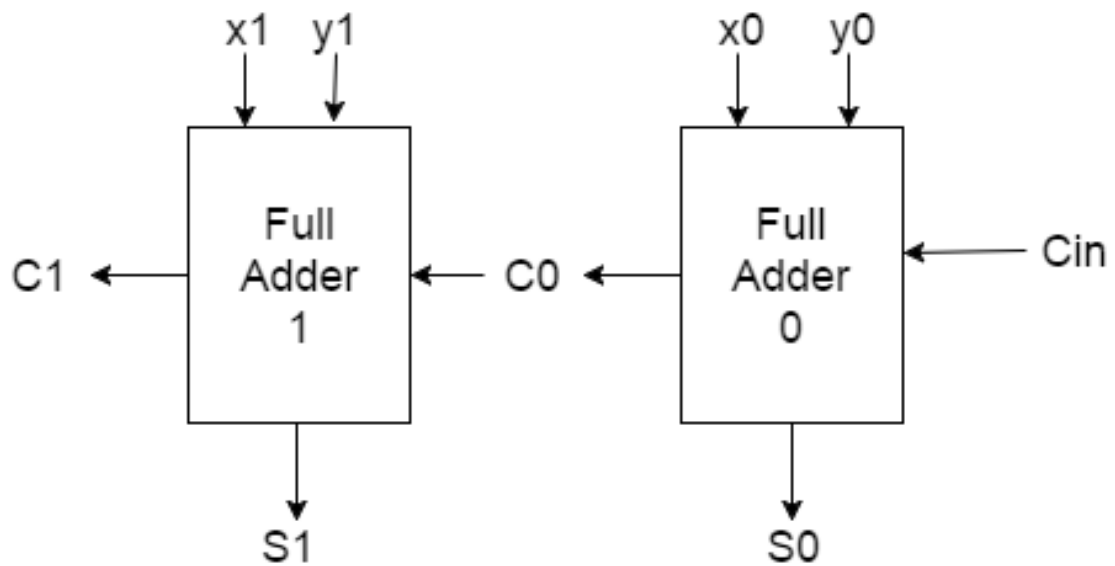


Figure 7.3: 2-bit binary parallel adder circuit

The circuit diagram of the binary full adder is shown in Figure 7.4

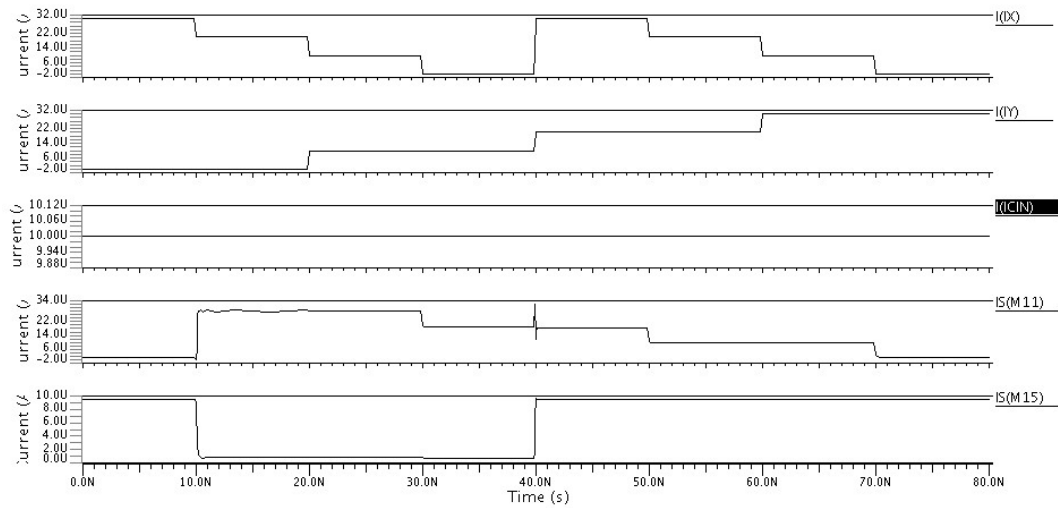


Figure 7.2: Simulation result of Quaternary full adder circuit

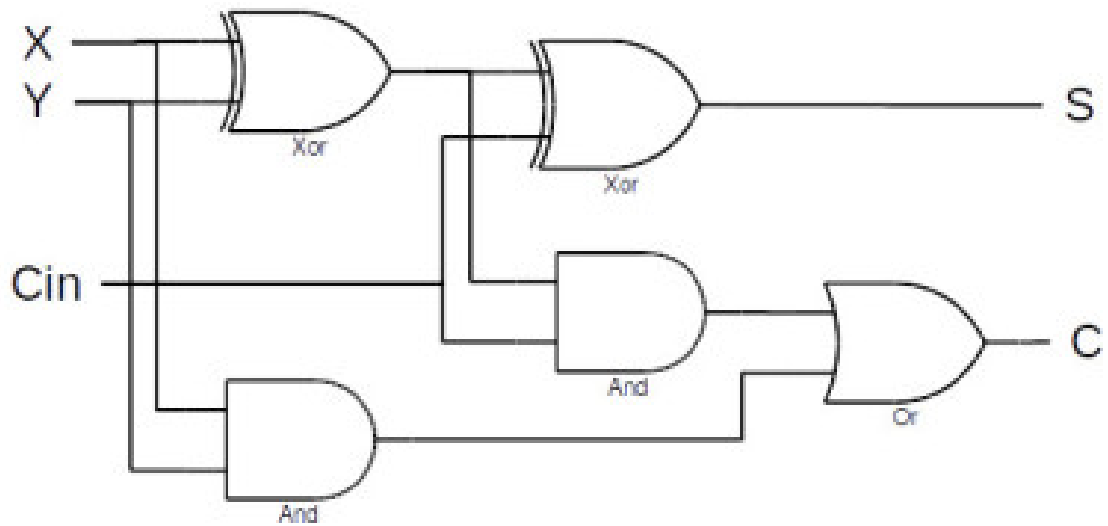


Figure 7.4: Binary full adder circuit

Designing the circuit in binary logic rather than multiple logic requires 257% increase in transistor count. Detailed comparison result in terms of number of transistors and power dissipation is shown in Table 7.1.

Type	Transistor count	Average power consumption (μ W)
Quaternary full adder	28	220
2-bit parallel adder	100	28

Table 7.1: Comparison table of 2-bit binary parallel adder and 1-digit Quaternary full adder

Chapter 8

Conclusion and Further Study

From the last couple of decades, multiple valued circuits has attracted a great attraction. These circuits have the potential of reducing the interconnection both on chip and between chip. In spite of potential advantages, the developments in multiple valued circuits are not satisfactory. Simplifying the logical expression, implementing the basic functional operators and processing the signal is still complicated task.

In this thesis, several MVL combinational and sequential circuits is discussed and analyzed. In chapter 2, basic set of fundamental multiple valued operators is discussed and analyzed. In chapter 3, performance of various fundamental current mode multiple valued operator is analyzed across different process corner and over wide temperature range. These multiple valued operators are basic building block in constructing any combinational or sequential digital circuits. In chapter 4, encoding and decoding scheme for multiple valued system is discussed that is required for its interfacing with binary circuits. In chapter 5, multiple valued multiplexer and demultiplexer is proposed and analyzed. The upper and lower threshold circuit discussed in chapter 2 is used to build multiple valued multiplexer and demultiplexer.

Except D-Flip flop, all other Flip-flop requires complement operation for its realization. This will add to increase in transistor costs as well as increase in power consumption. Moreover, D-Flip flop has same characteristic equation in both binary and multiple valued logic. Therefore, entire study throughout the work is carried out by using D-Flip Flop. Current mode CMOS Quaternary latch is discussed in this work. This latch is used as fundamental building block in developing sequential circuit. Multiple valued D Flip-flop is designed using Quaternary latch is master slave configuration. Modulo-4 and Modulo-16 counter is designed using Multiple valued D Flip flop which can further be used in clock generation of digital circuits. Robustness of the fundamental multiple valued operator is proved by implementing arbitrary state diagram.

In last part of thesis, a detailed comparison is made between 1-digit Quaternary full adder and 2-bit binary parallel adder circuit. Same set of input value is chosen for both design to ensure the fair comparison. It has been found that designing a circuitry in binary logic requires 257% percentage increase in transistor than multiple valued circuit. On the other hand, current-mode multi-valued circuits have constant current consumption, regardless of the switching activity, which makes the

power consumption 8 times higher than the binary one. Another advantage of binary design over multiple-valued ones is that, the binary circuits have a standard cell library. Since binary circuits have a standard cell library, therefore, designing a circuit in binary is not much difficult as compared to multiple valued case. No standard cell library is available for multiple valued system.

Multiple valued logic is not found to be superior in every VLSI design criteria. VLSI design always have some trade off between among design criteria like area, power dissipation, speed, design cost, pin reduction, CAD programs for IC design etc. Multiple-valued circuits and two-valued circuits must not be seen as competitors. Multiple valued circuits have some characteristics superior to corresponding binary circuits according to some VLSI design criteria and worse characteristics according to other criteria. The most important thing is to explore and examine the area, where multiple-valued circuits can be useful in binary world. The encoding and decoding discussed in this work is useful in binary to multiple valued and multiple valued to binary conversion respectively.

8.1 Further Studies

Current mode multiple valued circuits have the potential of reducing the number of interconnections and transistors. The major problem with the current mode multiple valued circuits is the increased power dissipation and non self restoring nature. The circuit performance becomes worst at higher radix due to increased power consumption.

Every fundamental multiple valued operator such as CWC, threshold, inversion etc requires current mirror for its operation. This causes increase in power consumption. Every replica of current requires a current mirror. Further study on multiple valued circuits should concentrate on reducing the current mirror which increases the power consumption.

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