Single Event Effect Hardened Cost Effective CMOS Circuits.

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Keywords: Soft error, Single-Event Upset, Single-event, Flip-flop, Sequential logic circuits.

Certificate

This is to certify that the thesis titled **"Single Event Effect Hardened Cost Effective CMOS Circuits"** submitted by **Sakshi Garg** for the partial fulfilment of the requirements for the degree of *Master of Technology* in *Electronics and Communication & Engineering* is a record of the bonafide work carried out by her under my guidance and supervision at Indraprastha Institute of Information Technology, Delhi. This work has not been submitted anywhere else for the reward of any other degree.

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Abstract

Moving towards deep-submicron technologies, packaging density of ICs is increasing and thus the number of storage elements is also increasing on an IC. Any data corruption in these storage elements leads to huge amount of loss to companies. With decreasing technology nodes, impact of radiation is increasing. Moreover, progress in technology is witnessing more timing violations with age of the IC.

This work is a study of effect of radiation induced soft errors on 180nm technology node CMOS circuits. It aims to develop radiation- hardened structures as well as explores the pre-existing designs to combat the effect of radiation on latches or Flip-Flops since Latches and Flip-Flops are critical to sequential circuits and as storage elements. Various parameters like Power dissipation, Area, and Propagation delay have been considered to evaluate the designs theoretically as well as on CAD level. According to CAD and Silicon results shared in this work, 'Single Phase Clock Design' is more robust and area and power effective than state of art techniques (like DICE, TMR).

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List of abbrevation

CAD	Computer Aided Design
CE	C-Element
DICE	Dual Interlock Cell
DMR	Dual Modular Redundancy
ET	Threshold energy
FF	Flip Flop
GND	Ground
LET	Linear Energy Transfer
O/P	Output
PVT	Process Voltage Temperature
QCRIT	Critical charge
RadHard	Radiation hardened
RHBD	Radiation hardened by design
SE	Soft error
SEE	Single Event Effect
SER	Soft error rate
SERR	Soft error rate ratio
SEU	Single Event Upset
SP	Single phase
TCLK	Clock time period
TF	Transient fault
TI	Tristate inverter
TMR	Triple modular redundancy
TSPC	True single phase clocking
VDD	Power supply
WOV	Window-of-vulnerability

Chapter 1

Introduction

Technological advancements leading to scaling in CMOS circuits have led to higher integration level and increase in package densities. Scaling has been observed in accordance to Moore's law. This law was stated in 1965 and according to this law, *"The number of transistors on a chip would double every two years for the next ten years."* For the successful implementation of Moore's law, significant number of steps have been taken by the industry that led to reduction in device parameters such as nodal capacitances, operating voltages, nodal separations, gate oxide length and thickness and increase in proximity of nodes. These changes have led to increased speed of ICs, lower transient time, less power dissipation, decrease in size of chips with increase in their functionality. This has also led to the possibility of smarter and smaller portable devices but at the expense of increased susceptibility of the circuits towards radiation strikes. The increased vulnerability towards SEE is due to the decrease in nodal capacitances, lower supply voltage values and increased proximity of nodes resulting from higher packaging density [1]. Proximity of nodes increases the possibility of single strike charge sharing [4], and Parasitic bipolar effect is mainly due to reduced gate length [5].

Soft errors are the "glitches" caused in semiconductor devices, due to excessive charge accumulation at any node. This charge accumulation is because of a high energy charged particle hitting the semiconductor device. These high energy particles might be generated from spatial activities and elements like cosmic rays or radioactive elements in packaging material like uranium and thorium.

The soft error rate of a design is generally quantified in terms of Failure-in-time or FIT where 1 FIT corresponds to one error per billion device hours. On an average, a latch Soft Error Rate (SER) may be 10^{-3} FIT [6]. Thus for design with millions of FFs, overall SER tends to thousand FITs. In an enterprise with over hundreds of processors, this SER will lead to an error every 2 to 3 days. Thus, it is of great importance to curb the effect of Soft Error (SE) in sequential elements. Memory elements within the sequential logic have been identified as largest contributors of SE [7]. Therefore, researchers are more concerned to proposing novel hardening approaches for latches and Flip-Flops.

Due to shrinking device technology, capacitance (C) values of the transistors and supply voltage

(V) of the CMOS circuits have scaled down considerably. According to Equation-(1.1), decrease in C or V leads to decrease in the Critical Charge (QCRIT) where QCRIT is the minimum amount of charge required to flip the data on any node of the circuit. Thus, low QCRIT means low energy particles from cosmic rays could also lead to SEU.

$$Q_{\text{CRIT}} = C_{\text{INT}} * V_{\text{SUPPLY}} \tag{1.1}$$

At ground level, radiation induced errors have created a need for radiation hardening of circuits. For example, in a video application, soft errors can manifest themselves as missing or incorrectly colored bits on a display screen [8]. In year 2000, Sun Microsystem's UltraSPARC II workstations crashed at an alarming rate. The inability to initially locate the source of the problem created significant customer dissatisfaction issues for Sun. The root cause of the problem was finally traced to IBM supplied SRAMs which were experiencing high upset rates due to charged particles causing soft errors in the memory system. Ultimately, not only did Sun switch memory vendors, they also designed new error checking and correcting logic and implemented it across the entire cache architecture [8].

This leads to the requirement of soft error resilient circuits. Various researchers have contributed to this field with Radiation hardening by design (RHBD) [1] or layout level hardening [9] or developing sensors ([10], [11]) for radiation hardened structures.

Existing radiation hardened by design (RHBD) approaches include Dual Interlocked cell (DICE) latches and Triple-Modular Redundancy (TMR). Likewise, an approach used to detect single event strikes is Dual-Modular Redundancy (DMR). These designs are based on the assumption that a single particle strike leads to charge collection on a single node in the circuit. Complex wiring of DICE and approximately three times increase in area and power of TMR makes them high cost solutions.

This work presents CAD analysis and comparison of various RadHard structures built on 180nm BCD technology of ST Microelectronics. Algorithms for evaluation of circuits have been discussed in detail. Moreover, new radiation hardened structures are proposed in this manuscript.

Background and History is covered in Chapter 2. Chapter 3 includes the initial experiments involving CAD level modelling of radiation particles and studying the effects. Chapters 4, 5 and 6 cover two types of radiation hardened Flip-Flop (FF) designs on basis of active clock edge. These chapters cover existing techniques as well as proposed designs. Results, analysis and conclusions are covered in Chapters 7 and 8 respectively.

Chapter 2

Background and Related Work

2.1 Overview

This chapter covers the history of radiation related anomalies in semiconductor devices and progress made in this field. Since this work aims at single event effects and RHBD methods only, MBU and other techniques for SEEs have not been extensively discussed. References have been provided if the reader wishes to explore similar topics in detail.

2.2 Background

Before 1978, radiation was a concern only for aero-space electronic equipment. This was mainly due to the presence of high energy protons and heavy ions in the space. With technology scale down and shrinking transistor sizes, radiation induced soft errors have crept to circuits operated at ground/sea level as well. Single event upset (SEU) is used to describe all effects caused by single strike of an energetic particle, including both soft and hard errors. Soft errors, unlike hard errors, are not permanent and can be reversed by overwriting the corrupted data by the correct one. However, FIT (as mention in Chapter-1) due to soft error is much more than that of hard errors.
Various spatial events like Solar flares, Cosmic ray particles, trapped radiation and the Proton Belt have been prominent source of soft errors for aerospace electronic components. Radiation induced soft errors is a critical issue for building reliable circuits at ground level also. Cosmic ray particles undergo collisions with earth's atmosphere and result in generation of secondary particles as ground level is reached (as shown in Figure-2.1). Near ground, neutrons are the main source of single event upsets (SEUs) as can be seen in the Figure-2.1. Different particles have varying energy levels (shown in Table-2.1) at different altitudes.

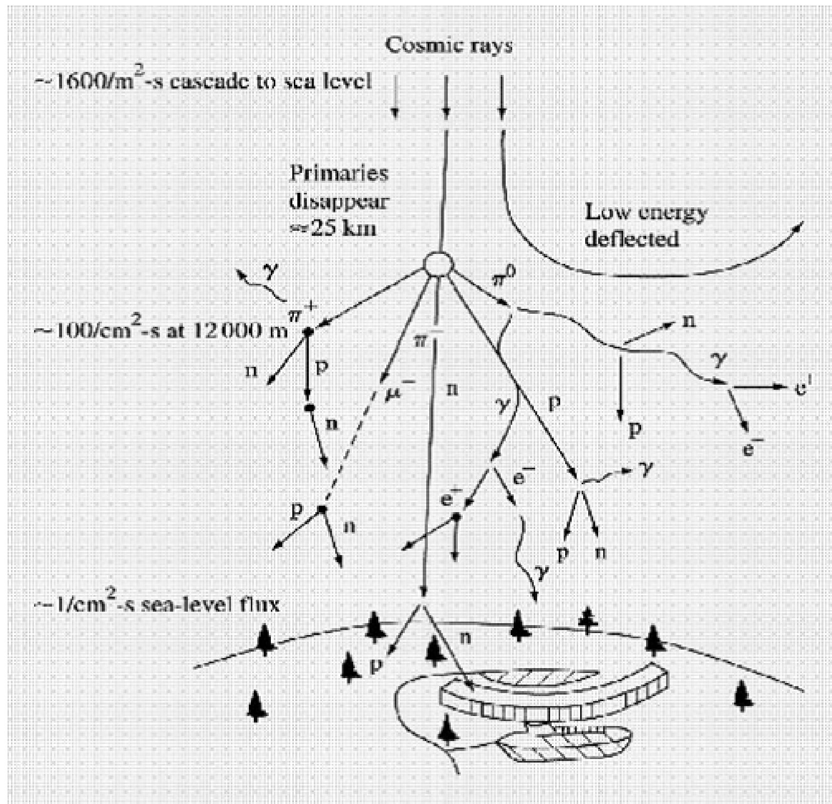

Figure 2.1: Schematic View of Cosmic Rays Causing Cascade of Particles [1]

2.3 Radiation Classification

Radiation can be classified as ionizing and non-ionizing. Non ionizing radiation includes visible and infrared light, microwaves and radio waves. It cannot induce SEUs as it has only sufficient energy to change the energy state of electrons. Thus this work concentrates on ionizing radiation because it can cause SEUs. Examples of ionizing radiation particles are alpha and beta particles, protons, X-rays, and gamma rays. Neutrons are not directly ionizing, but the resulting ions from their collisions with nuclei is ionizing. Ionizing particles result from spatial activities and/or radioactive decay of impurities in packaging material. Space radiation environment is an un-avoidable scenario. The main contributors to the high-space radiation environments are cosmic rays, solar flares, and trapped radiation [1]. The Earth's magnetic field can affect the trajectory of charged particles evolving in the near-Earth space. Some charged particles become trapped in the geomagnetic field lines and follow relatively reliable and stable trajectories [1]. The Earth's trapping phenomenon leads to accumulation of particles in specific areas of the magnetosphere called the Van Allen Belts. The sources contributing to the formation of the radiation belts are believed to be solar flares, cosmic ray particles from interplanetary space, reaction products from Galactic Cosmic Ray (GCR) collision with nuclei atoms present in the Earth's upper atmosphere (O and N), and exo-atmospheric nuclear explosions [1].

Table 2.1: Soft Errors at Different Altitude Levels

ENVIRONMENT (ELEVATION LEVEL)	**PARTICLES/ RAYS AFFECTING/ SOURCE OF SE**	**LET/ E_T**	**MAIN CONSTITUENTS**	**COMMENTS/ ORIGIN**
Space (Outer space)	Cosmic ray particles	up to 10^{19} eV	92% protons 6% alphas 1% heavy nuclei	Due to Supernova explosions, Pulsars, galactic explosions
Terrestrial environment ($< 60,000$ft) (Sea/ ground level)	cosmic particles	10^{11}eV	96% neutrons, $<$ 1% primary particles, (0% solar cosmic)	
	Alpha particles	4 to 9 MeV	Polonium (alpha emitter)	Due to packaging material consisting of thorium and uranium
	Neutrons	$<<$ 1MeV		Neutron interacts with Boron(10) to form alpha(1.47 MeV) and Li particles (0.84MeV)
		100 MeV to $>$ 10 GeV		Causes inelastic energy transfer to Si.
	High power sources in proximity		Power cables, supplies, and distribution units; Lighting systems; Power generators	SEUs can occur if high power systems are too close to the chassis or if multiple power cables are on or beside the chassis
Terrestrial environment (12000m)	Secondary cosmic particles		proton, neutrons, pions, muons, electrons, and photons	Due to Interaction of cosmic rays with atmospheric particles

2.4 Radiation Contributors causing SE

Main radiation contributors in semiconductor devices are as follows: 1) Radioactive elements in packaging material, 2) High energy cosmic ray particles, and 3) Low energy neutrons

2.4.1 Radioactive elements in packaging material

Radioactive impurities like Uranium and Thorium in packaging materials emit energy while decaying to lower energy states [2]. These unstable isotopes contain kinetic energy in the range of 4 to 9 MeV. Alpha particles emitted from these sources are a major source of SEs.

REACTION PRODUCTS AND THRESHOLD ENERGIES FOR n + ^{28}Si REACTIONS

Reaction Product	Threshold Energy (megaelectron volt)
$^{25}Mg + \alpha$	2.75
$^{28}Al + p$	4.00
$^{27}Al + d$	9.70
$^{24}Mg + n + \alpha$	10.34
$^{27}Al + n + p$	12.00
$^{26}Mg + {}^{3}He$	12.58
$^{21}Ne + 2\alpha$	12.99

Figure 2.2: Neutron and Si Reaction Result [2]

2.4.2 High energy cosmic ray particles

Cosmic radiation Neutrons with energy more than 1MeV produce secondary ions on reaction with Si nuclei, which result in SE in Semiconductor devices at terrestrial level. [2]

2.4.3 Low energy neutrons

Interaction of cosmic ray Neutrons with isotope Boron-10 (commonly used as p-type dopant for junction formation in IC) releases Li nucleus with energy around 1MeV, gamma photon with around 400KeV energy and alpha particle of 1.4MeV energy. This is a common source of SE especially in circuits with BPSG (Borophosphosilicate glass). [2]

2.5 Single Event Effect Mechanism

2.5.1 Collision of High Energy Particle

Collision of high energy particle leads to charge generation in semiconductor devices. This might be due to any of the two processes described below:

1) Direct ionization:

This refers to electron hole pair generation due to a heavy ion hit. An ion is categorized as heavy if its atomic number is greater than or equal to two. The ion frees electron-hole pairs as it traverses through the semiconductor and loses energy in the process. This energy lost per unit length is referred to as Linear Energy Transfer (LET) and the length of the path travelled by the particle is known as Range.

2) Indirect ionization:

Indirect ionization is a result of the nuclear interaction between an energetic particle and a struck

device, thereby resulting in ionization by secondary particles. The energetic particle in this case refers to lighter particles such as protons and/or neutrons, which can produce significant upset rates due to indirect mechanisms by undergoing elastic collisions with a target nucleus [1]. Examples of nuclear reactions that can occur due to the interaction between lighter particles and struck devices include: 1) elastic collisions producing Si recoils; 2) Alpha/Gamma particle emission and the recoil of a daughter nucleus (e.g., Si emits alpha-particle and a recoiling daughter Mg nucleus), and 3) spallation reactions (target nucleus is broken into two fragments (e.g., Si breaking into C and O ions), all of which can independently recoil [1].

Typically, inelastic collision products have fairly low energy and do not travel far from the particle impact site. The secondary particles also tend to scatter forward in the direction of the original lighter particles; hence a significant angular dependence on SEU sensitivity in microelectronic circuits [1].

2.5.2 Charge Generation and Collection

Charge carriers generated, due to high energy particle strike, move according to the electric field (applied or built-in fields) and doping of the substrate. Charge generation near reverse biased junction lead to major charge generation and collection due to drift process. The high electric field present at a reverse biased junction leads to separation of free charge carriers formed. This results in transient current pulse at the contact. Drift time period is limited by the Saturation Velocity of charge carriers. Thus it is extremely small. For electrons in Si, saturation velocity is 1×10^7 cm/sec [1]. The generated charge is collected and transported in following three main steps as in Figure-2.3:

1. Drift, 2. Diffusion and 3. Recombination

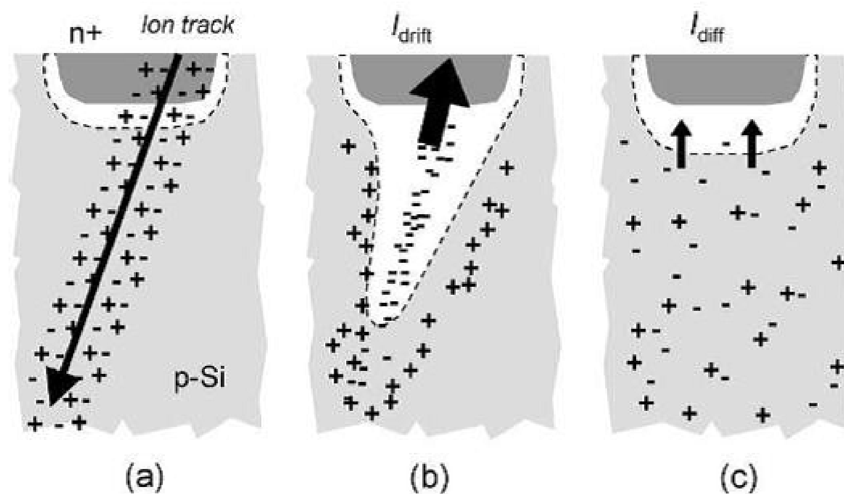

Figure 2.3: Mechanism of Charge Collection and Flow [2]

The Drift process leads to disturbance of junction electrostatic potential. This in turn leads to Field Funneling Collection process. This was discovered by IBM researchers in 1981 [3]. In this process, the high field region is extended in the shape of funnel due to the connection of deposited charge with depletion region. As a consequence, charges that were present outside the depletion region are also pushed to the depletion junction contacts and this leads to more charge being accumulated resulting in voltage level flip at the node. This process is followed by Diffusion. Diffusion process is a slow process and thus takes time many times more than drift process. Diffusion junction length determines the process at large.

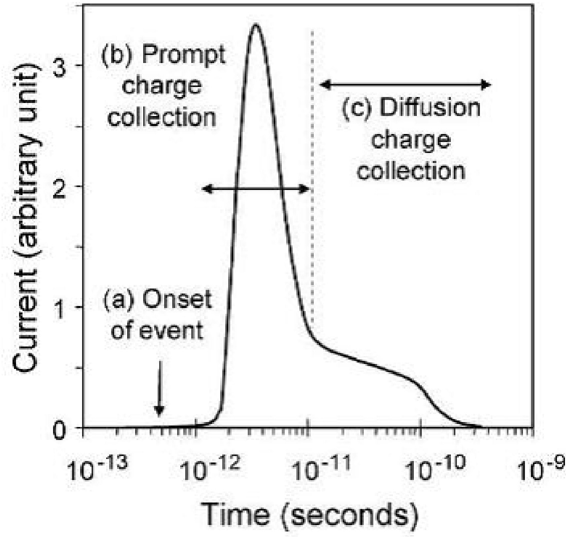

Figure 2.4: Radiation Induced Double Exponential Current [2]

These steps lead to transient pulse generation at the device terminal. The initial spike in the current pulse is short lived. This rising transient is due to Drift process. The shape of the current pulse can be expressed as I = dQ/dt (where I is the current, Q is the charge, and t is the time). Nature of the current pulse is as shown in Figure-2.4 [1]. The double exponential current pulse has a rise time in the order of tens of picoseconds (ps) and a fall time in the order of 200 ps to 300 ps. This current pulse can be modeled as double exponential current pulse

$$I_{\mathrm{p}} = I_{\mathrm{o}}(e^{\text{-t}/\mathrm{T_f}} - e^{\text{-t}/\mathrm{T_r}}) \tag{2.1}$$

Where, $\mathrm{I_p}$ is transient current pulse, $\mathrm{I_o}$is the peak current, $\mathrm{T_r}$ is the rise time for the current pulse, $\mathrm{T_f}$ is the delay time for current pulse. Critical charge for the node under test can be calculated by integrating the current pulse for the pulse period.

$$Q_{\mathrm{CRIT}} = \int_0^{\mathrm{T_{PERIOD}}} I(t)dt \tag{2.2}$$

2.6 Classification of Errors

Transient pulse generated at the device terminal might lead to hard error (permanent and destructive) or soft error (temporary error). Both the types of errors are discussed in this section.

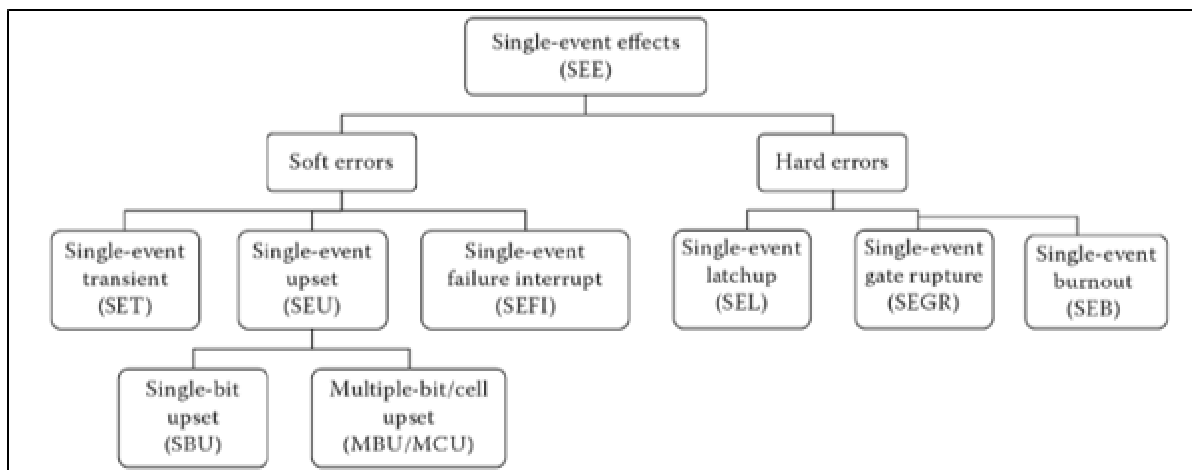

Figure 2.5: Classification of Single Event Phenomenon [3]

2.6.1 Hard Errors

SEB depends on the amount of current generated due to the ion strike. A regenerative feedback mechanism is started due to triggering on of the bipolar device. It might lead to permanent short between source and drain terminals in case of unlimited current flow. This type of break down is observed in power BJTs and MOSFETs. [1]

SEGR might take place concurrently to SEB. It involves rupturing of the gate oxide layer if electric field across it exceeds a threshold value due to trapping of ion strike charge beneath the gate region. It leads to increase in electric field of the dielectric.

An SEL is an effect common to CMOS devices due to the presence of the n-p-n-p junction in the process. Once the latchup is triggered, the sustained high current can destroy the device due to the thermal runaway or failure of metallization [1]. A reduction in power or removing power from the device in the latched state can help return the device to normal operation, thereby preventing destructive failure.

SEL requires a power reset. The IC can be permanently damaged if it is not protected with current delimiters. Thus, it is more severe than soft errors. Also, SEL can impact the long-term reliability of the IC.

2.6.2 Soft errors

Single Event Transient and Single Event Upset are some common temporary errors due to ion strike in semiconductor devices. Temporary errors can occur as a spurious signal (i.e. Single Event Transient - SET) or a latched spurious signal (i.e., Single Event Upset) as a result of an ion-strike. An SET is a voltage glitch in the normal circuit operation due to a SE, where the SE is the interaction of a single ionized particle with a semiconductor.

An SEU is a bit flip or change of state induced in a device by an SE. The change of state or upset can become an error if the signal is latched or misinterpreted as valid data by other circuitry. For this work, SETs and SEUs are major discussion points since charge sharing and parasitic bipolar amplification of SE currents can create temporary errors. Multiple Bit Upset (MBU) is another kind of temporary error wherein multiple circuits are affected from one event spreading to multiple sensitive nodes spaced close together.

2.7 Summary

SEEs are important to nullify in any circuit due to their drastic implications. Thus, it is a trending research topic. It is necessary to build a realizable (having practical area and power constraints) radiation hardened design. In order to get an insight, modelling and simulation of SEE effect on microelectronic devices is necessary. Circuit simulators can be used to simulate complex circuit designs and model the response of a single radiation strike on a CMOS circuit. Circuit simulations tend to represent realistic circuit performance and provide a cost effective way for analyzing the radiation performance of a circuit design. While it is true that circuit simulators sacrifice accuracy in device modeling, they make up for it with vastly increased computational throughput. This work makes use of circuit simulators to study the impact of single radiation pulse on various designs and eventually lead to building of a RADHARD design. Detailed analysis and comparison is provided between state-of-art technologies and the proposed structure.

Chapter 3

First Level Analysis

3.1 Overview

This chapter explores the initial set of study and experiments performed. Section-3.2 covers the modelling of ionizing particle effect, Section-3.3 involves study of Fall time variation on critical charge and peak current, The Stacked configuration analysis is covered in Section-3.4 and Section-3.5 closes the chapter with conclusions.

3.2 Modelling and Studying the Effect of Ionizing Particle on Various Models of Memory Elements (Flip-Flop)

To study radiation hardening on Flip-Flops (FFs), various configurations of FFs were made in 180nm technology. The configurations varied on the basis of presence and absence of set and reset pins. The basic approach to combat the issue is by first detecting the vulnerable points in any circuit. Thus evaluation of various FF designs to find the susceptible nodes and their vulnerability with the help of scripting Language (ECL) simulations was done.

3.2.1 Radiation Simulation

Any particle strike generates electron-hole pairs that result in current flow between drain-body terminals. Thus, the excessive current flow at drain by applying a double exponential current pulse as explained in Section-2.5.2 was simulated. This mechanism was used to calculate QCRIT at every node and the results were studied. Moreover, various structures were compared on the basis of their robustness using Monte-Carlo simulations. These simulations were done with the help of Mentor Graphics, ELDO. The structures were made with the help of Cadence Virtuoso. The algorithm in Figure-3.2 was devised to do the same.

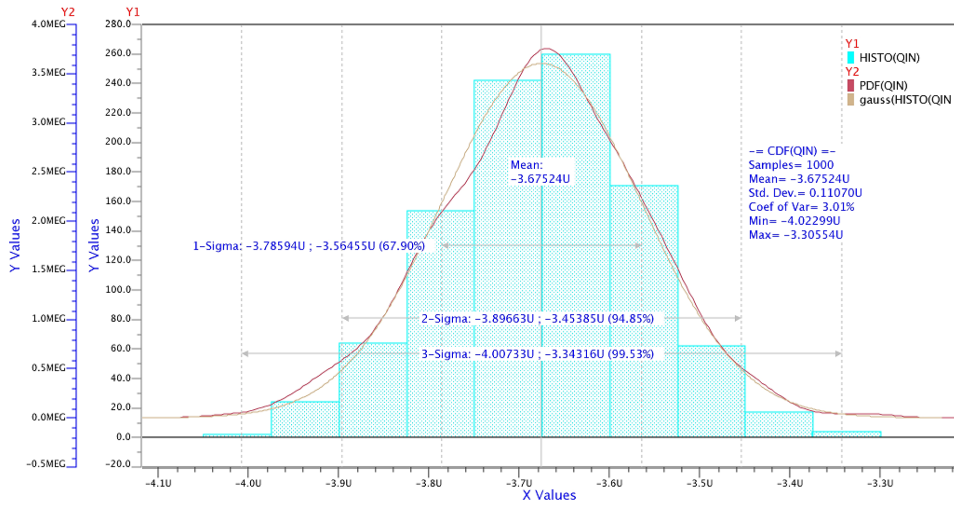

Figure 3.1: Histogram for Monte Carlo Iterations

3.2.2 Double Exponential Pulse Modelling

The double exponential pulse formation and mathematical modelling has been discussed in the Section-2.5. This Double exponential current pulse is applied either at source/sink according to the logic state of the node. Thousand Monte Carlo iterations having a distribution of current injected on sensitive nodes were performed for each structure.

3.2.3 Results

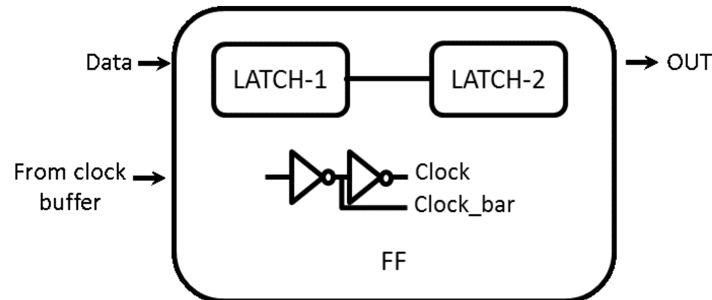

Figure 3.3: Node '0' Represents the Clock_bar Node, Nodes '1' and '3' are Internal Nodes of Latch-1 and Latch-2 Respectively, Node '2' is the Node Connecting Both the Latches.

The results have been normalized with respect to FF2 Node-0 (Figure-3.3) value.

Table 3.1: Critical Charge Values for FF Internal Nodes

Nodes	FF1		FF2		FF3		FF4		FF5	
	C	D	C	D	C	D	C	D	C	D
0	-0.9X	0.4X	-X	0.4X	-0.9X	0.5X	-1.1X	0.6X	-1.0X	0.4X
1	-0.6X	0.3X	-0.7X	0.3X	-0.7X	0.3X	-0.9X	0.3X	-0.7X	0.3X
2	-0.8X	0.5X	-0.8X	0.5X	-0.6X	0.6X	-0.9X	0.6X	-0.8X	0.5X
3	-0.4X	0.2X	-0.3X	0.2X	-0.4X	0.2X	-0.5X	0.4X	-0.3X	0.2X

** C denotes Charging and D denotes discharging

3.2.4 Conclusions

- According to the results, it can be concluded that PMOS is more robust than NMOS for circuits with uniform switching times.
- Increasing the fan-out (more load capacitance) makes the Flip-Flop more robust. This can be observed by the values for FF4 and FF5 where FF4 is the Flip-Flop with fan out of 4 and FF5 is the same configuration with fan out 1. This is because the charging/discharging time increases.

3.3 Fall Time Variation Effect on Critical Charge and Peak Current

3.3.1 Variation in Fall Time

The effects of fall time variation on charge accumulation were observed by varying the Fall Time of the double exponential pulse. the values of Fall Times used were 10pS, 100pS, 500pS and 1000pS. It was observed that slope for the erroneous data increases with increase in fall time i.e. erroneous flipping (of the output data value) starts late but attains the faulty level earlier than the outputs flipped with lesser fall times. So, the charge accumulation starts late but charge gets accumulated earlier with increase in Fall Times.

Difference was negligible (Figure-3.4) and thus effect of fall time variation was not considered for further analysis.

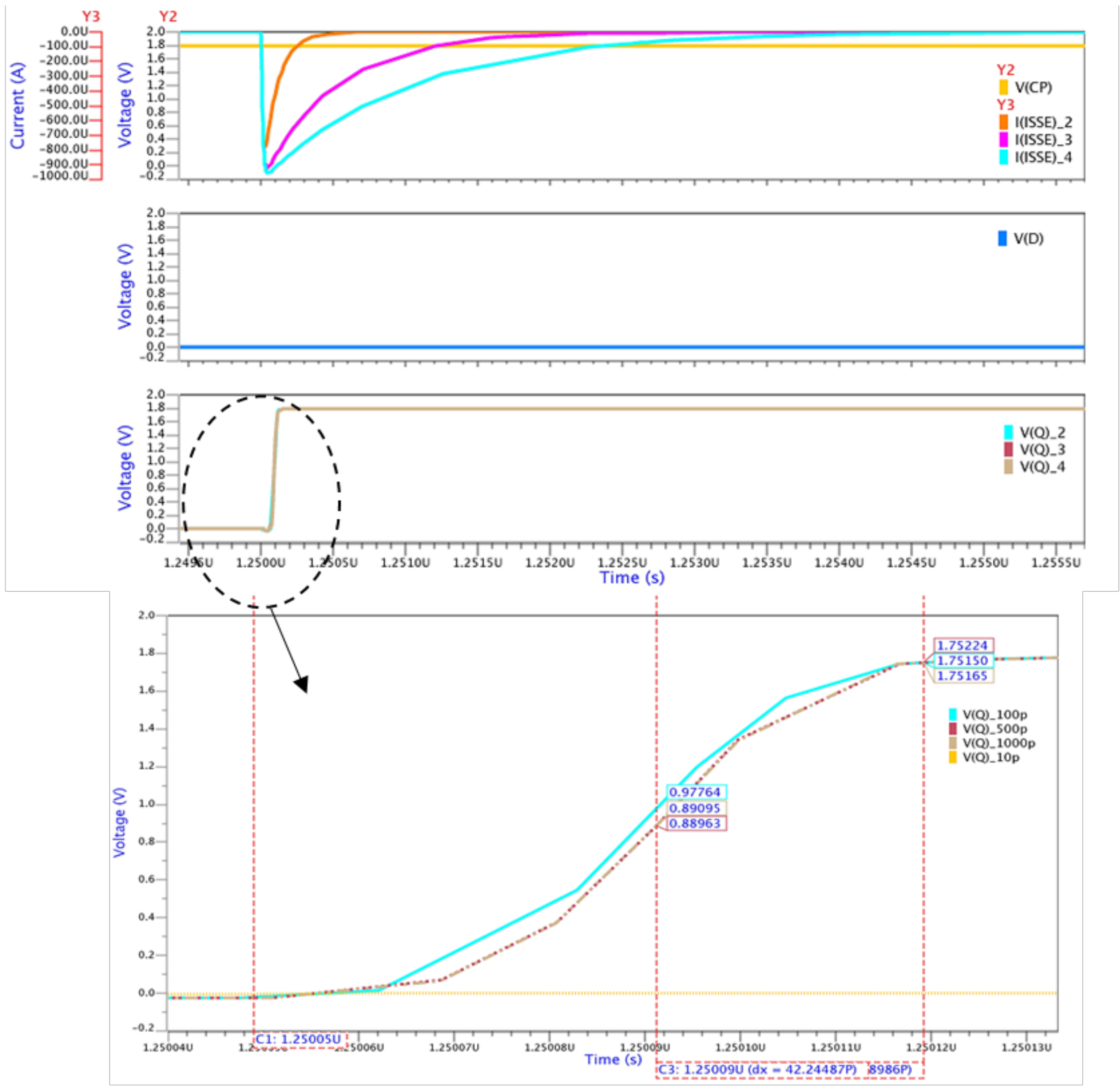

Figure 3.4: Output Variation Due to Varying Fall Times

3.3.2 Fall time variations were simulated and over 300 iterations (increasing peak current with every iteration) on a particular node of Flip-Flop.

Figure-3.5 is obtained from the analysis with (Clock, Data, Output) combination as (1, 0, 0). It was observed that more critical charge is being accumulated for lower current peaks with increasing fall time.

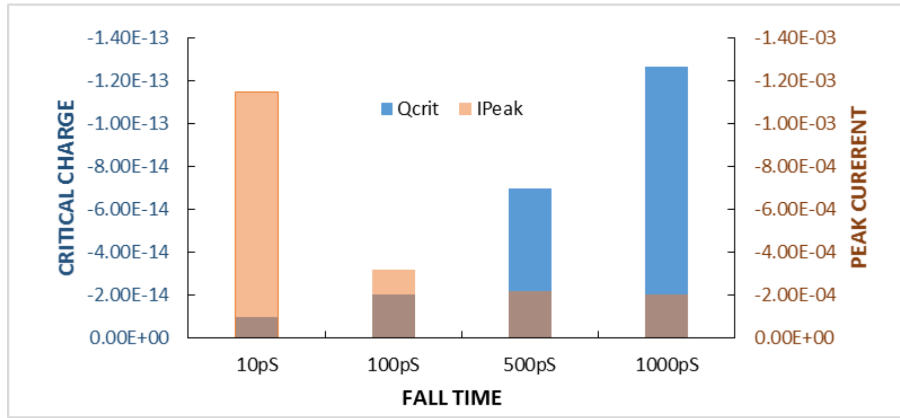

Figure 3.5: Fall Time Variation Results

3.4 The Stacked Configuration Analysis

Using the configuration consisting of 2 PMOS and 2 NMOS rather than one of each (Figure-3.6) leads to 50% more robust design on the expense of increased area.

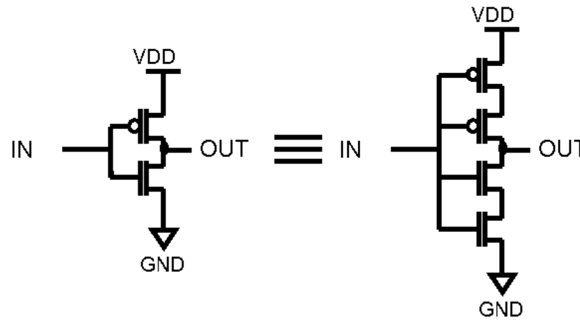

Figure 3.6: Regular Inverter (Left) and Stacked Inverter (Right)

Resistance of the circuit increases due to redundancy and thus the value at output node takes more time to flip while charge/discharge is to occur from rail to output node. By that time, the double exponential pulse dies and the erroneous value is not propagated. Difference of SER between DFF and stacked inverter based FF is caused by gate capacitance increment. This results in a circuit with higher delay due to larger gate capacitance and output resistance. Stacked Transistor configuration is preferred because critical charge required in stacked transistor is 20X more than the QCRIT of conventional transistor.

Following experiment was performed on a Flip-Flop configuration (FF2 from Table-3.1): Changed configuration refers to the one that has the Data-in MOS nearer to the Output of the Inverter rather than the clocked MOS. Current pulse was applied between the clocked and data-in transistor for the clock and data configuration as seen in the EZ-wave plots. Fall time of 460pS was used for 1.8V

power supply with (0.5*VDD) as threshold value for data flipping and following observations were made:

a) When clock is near output and data is near ground (0V)

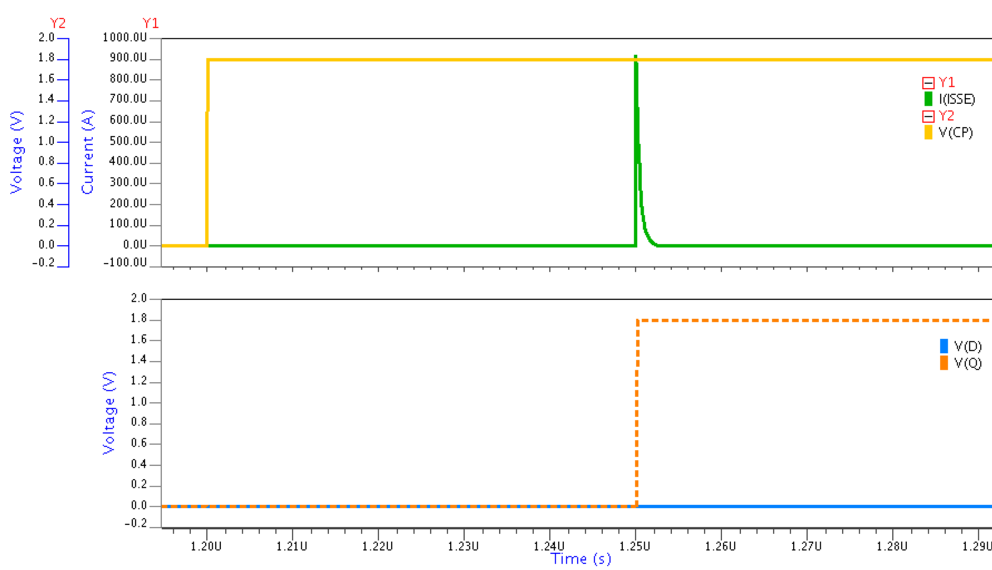

Figure 3.7: The Output is Flipped due to +1mA Current

Flipping of output was observed with QCRIT as 0.017pC at 0.06mA current peak.

b) When clock is near ground (0V) and data is near o/p

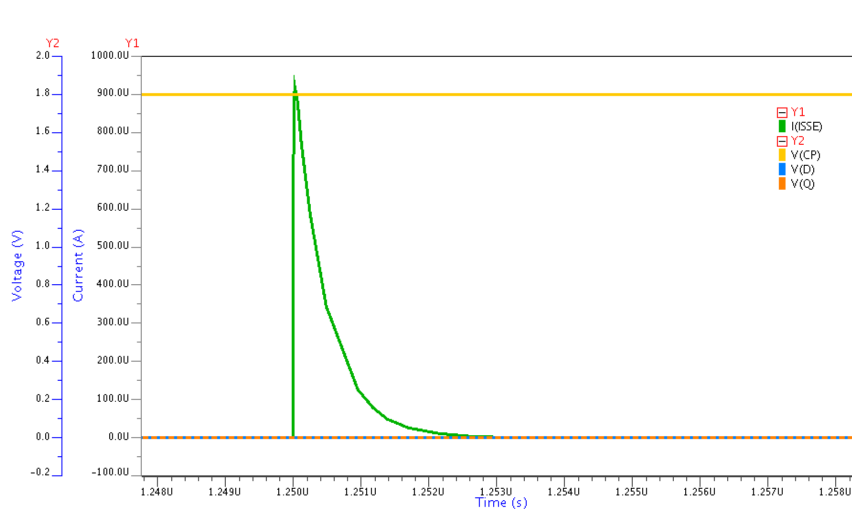

Figure 3.8: No Radiation Effect

No radiation effect was found. Thus, modified design is robust as compared to conventional configuration.

3.5 Conclusions

The set of experiments performed indicate that

- PMOS is more robust than NMOS transistors.
- Varying fall time does not have any major impact to be taken under consideration for further study.
- Increasing the resistance and capacitance increases the robustness against radiation induced errors.

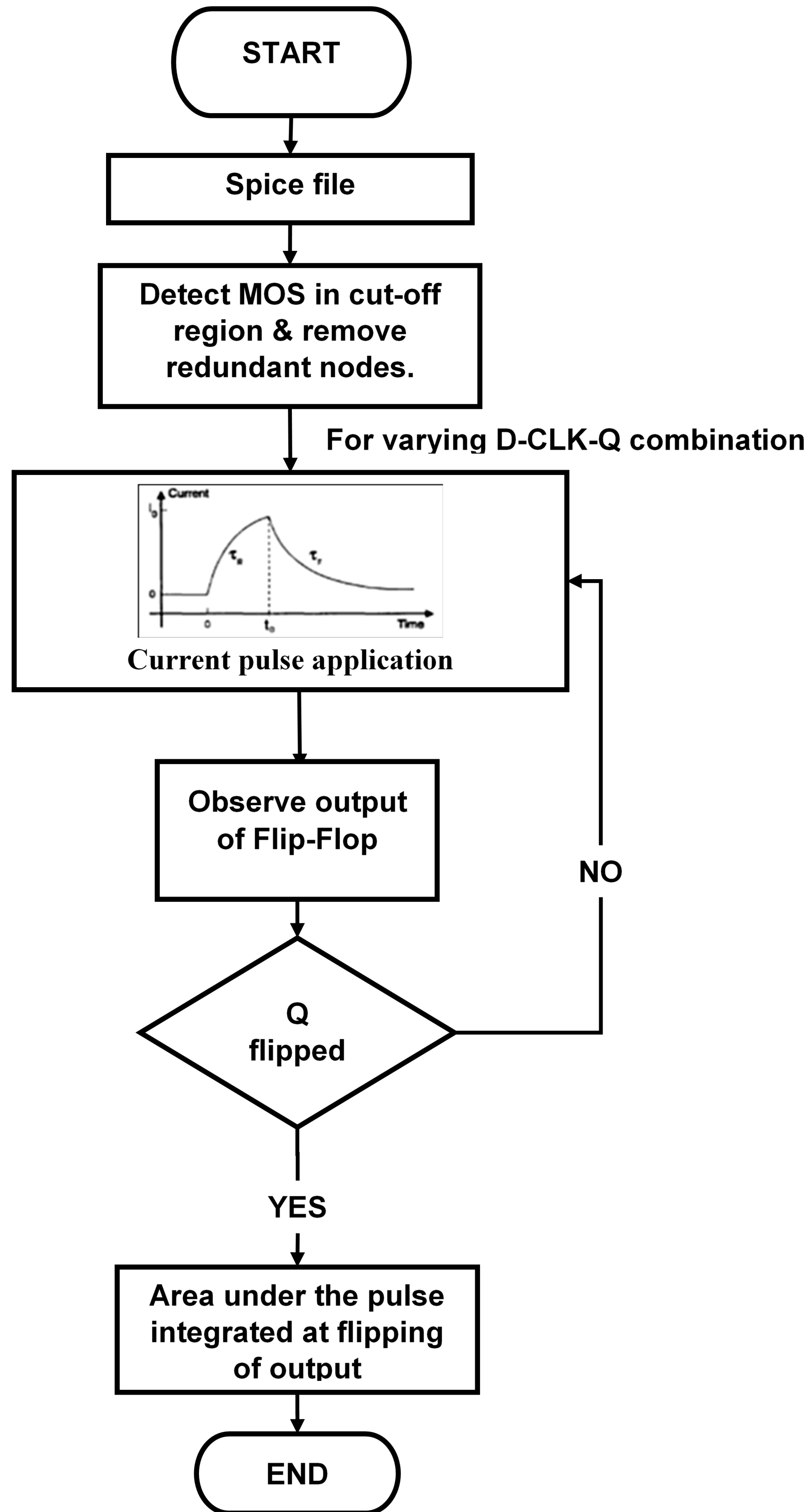

Figure 3.2: Algorithm to Check the Effect of Radiation

Chapter 4

Radiation Hardened Dual Phase Clocked Structures

4.1 Overview

High volume terrestrial applications are more cost sensitive than space applications. Hence, low-cost techniques to enhance circuit reliability in the event of soft errors are needed. Radiation hardened structures are made by implementing redundant structures which will result in extra delay between input and output of the Flip-Flop. If the delay is large enough so as not to let the single event transient pulse to travel to the output in time then the single event upset/latch-up will not occur. Redundancy also increases resistance of the design. Resistance of the circuit increases; thus increasing the time to charge/discharge the node and by this time the current pulse usually dies and the erroneous value is not propagated. This concept is used to make various Flip-Flop configurations in ST Microelectronics' Bipolar CMOS DMOS (BCD)-9s technology. Here BCD-9s refers to 180nm technology. This chapter discusses some radiation hardened designs using dual phase clocked structures.

4.1.1 Timing Constraints

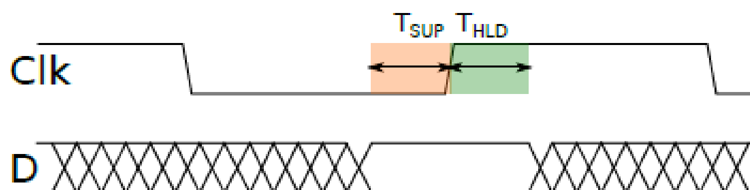

Figure 4.1: The Timing Constraints (Setup and Hold Time) of a Flip-Flop

The data path delays leads to changes in setup time (T_{SETUP}). T_{SETUP} is the amount of time for

which the data must be stable before the capturing edge of the clock (Figure-4.1). If the data input changes anywhere during this time, the captured data might go into metastable state. Depending upon which transistor in the circuit degrades the most, the setup time might increase or decrease for the data path. For long data paths, T_{SETUP} is considered whereas for short paths the hold time (T_{HOLD}) constraint (Figure-4.1) plays a crucial role. Thus, apart from designing a soft error robust circuit, Timing error hardened circuits are also crucial for proper functioning of the device.

4.1.2 C-element

This structure is used to correct soft errors in a latch or FF along with DMR technique. It was originally proposed by Intel as a part of BISER latch [12]. The structure and working of the element is discussed below.

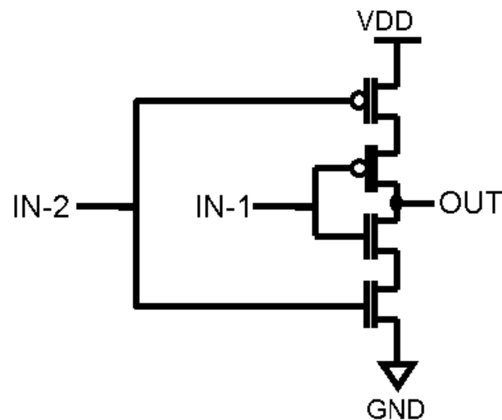

Figure 4.2: Structure of C-Element

Table 4.1: Truth Table of C-Element

IN1	**IN2**	**OUT**
1	1	0
0	0	1
0	1	Previous value attained
1	0	Previous value attained

According to the Table-4.1, in case of different inputs the C-element (CE) retains the previous value [13]. In case of both inputs same, the output is inverted value of the inputs.

4.2 DICE

The two fundamental concepts used in this design are redundancy and feedback. Redundancy preserves uncorrupted data on at least a node after a single-event strike. The uncorrupted data

provides state restoring feedback to recover the corrupted data. The DICE design has data stored as two pairs of complementary values on four nodes (A, B, C and D in Figure-4.3), effectively comprising a pair of bi-stable latches. Simultaneous access of these pairs is done via NMOS pass gates in write and read operations. The complementary pairs are sensitive pairs in this design, since simultaneous changes in both of the nodes in one of these pairs will upset the state of the cell. Therefore, these nodes should be placed far enough from one another to prevent the value changing in both of them due to one single event strike [14].

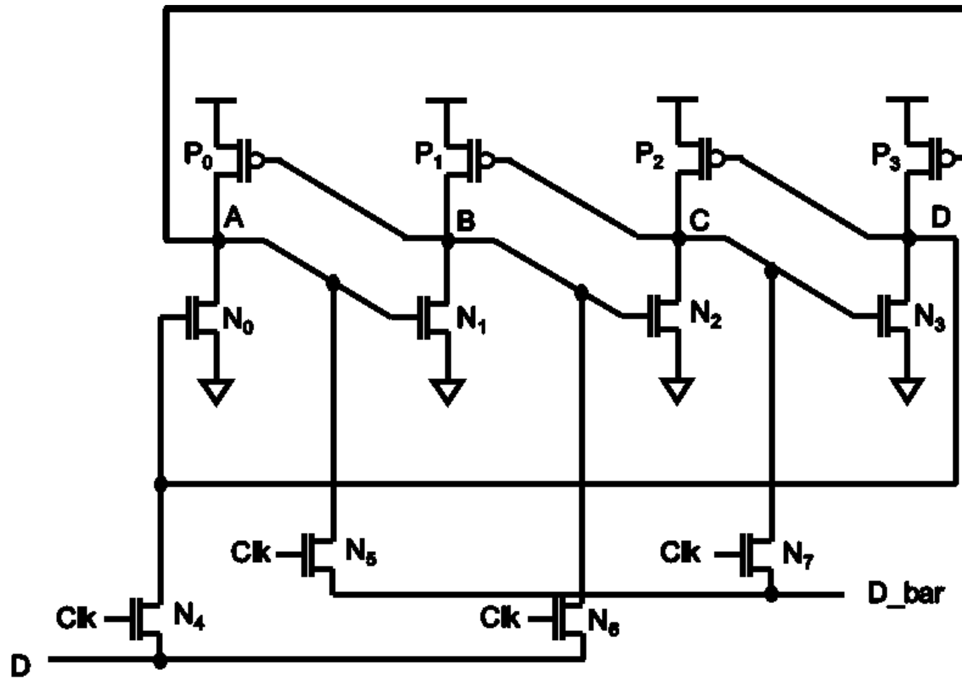

Figure 4.3: DICE

4.2.1 Functioning of DICE

If at high Clk, D is provided the value GND and D_bar as VDD then A = C = 0 and B = D = VDD. Thus at Clk equal to GND, the data will be latched. At this point radiation induced error might creep in. If due to radiation hit, value at B changes to GND, then P0 will turn on and N2 will turn off thus leading to the following state: A = X ; B = 0 ; C = Z ; D = 1. Due to floating value of C, the erroneous data is not propagated and eventually the value at node B is pulled up to VDD with the help of P1.

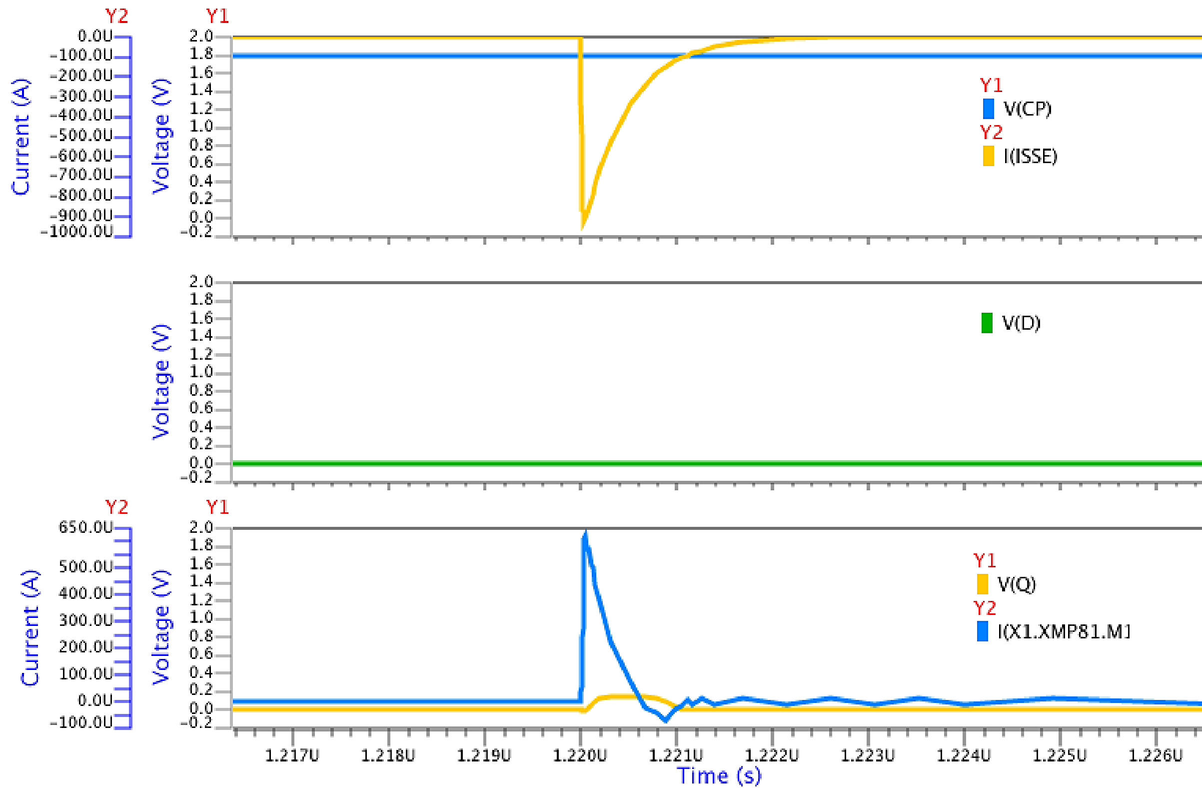

Figure 4.4: Simulation results of DICE

A basic FF was designed with DICE concept and effect of radiation was studied as shown in the Figure-4.4. When clock pulse (V(CP)) is high and data (V(D)) is low, the output of the Flip-Flop is retained as low even after application of radiation particle modelled as current pulse on node "M" of PMOS (XMP81) as denoted in the waveform. Thus, it can be observed that DICE provides robustness against radiation induced soft errors. With this technique error at the output of the logic is reduced to some extent, but introduced propagation delay of twice as with the conventional Flip-Flop. This technique utilizes more number of transistors as compare to conventional Flip-Flop. Power consumption is also worse with this technique i.e. around 3.5 times higher. So the DICE radiation hardening design has issues of delay and high power dissipation.

4.3 TMR

This is an age-old technique to provide RADHARD design without any complex wiring. TMR uses three identical copies of the original module operating in parallel as shown in Figure-4.5. An error is detected if the outputs of the modules differ. The error is corrected by voting, i.e., taking the most common output value out of 3 outputs as the correct result. In the case of soft errors, this approach is effective since, due to their low rate of occurrence, the probability of two soft errors striking the same module in the same clock cycle is negligible. The difficulty with TMR is that it

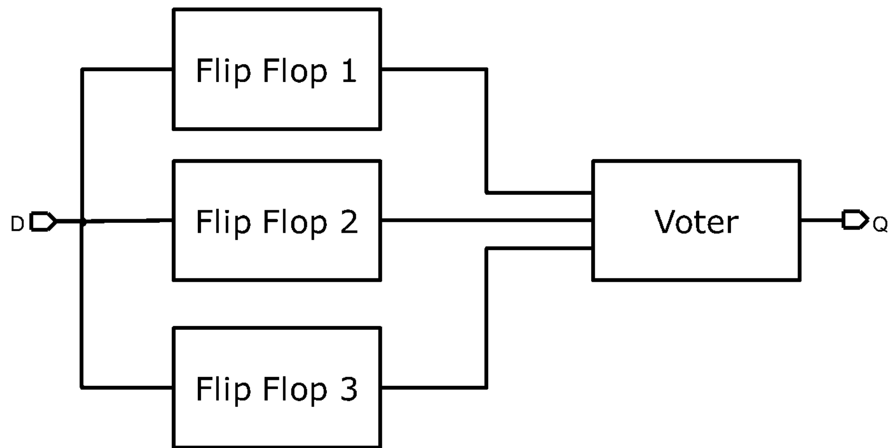

Figure 4.5: TMR Architecture

consumes area and power more than three times the cost of the basic circuit [15].

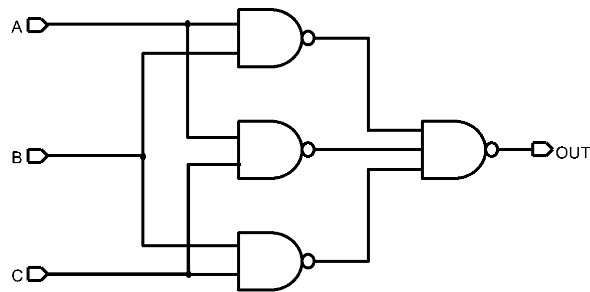

Figure 4.6: VOTER Schematic

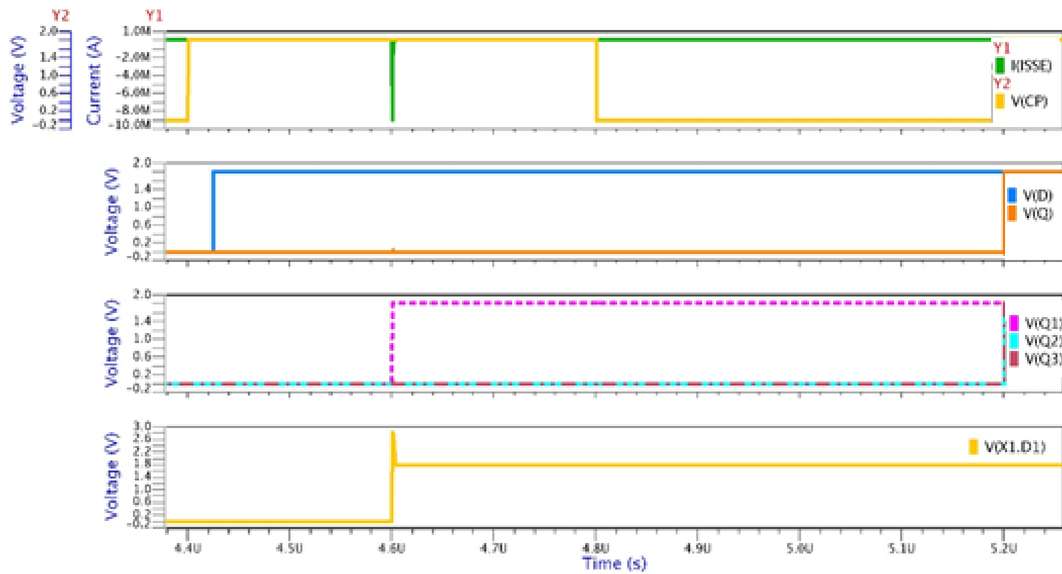

Figure 4.7: Simulation Results for TMR

According to the voter circuit (Figure-4.6) the Boolean expression for output of the TMR circuit is: OUT = A*B + B*C + A*C. Therefore, if any one of the inputs to the voter is different, then the output retains the value of the two identical inputs to the voter. Considering only Single event upsets, only one of the Flip-Flops will have erroneous output and other two will carry the correct value. As can be seen from the EZ-wave plot, the output value is retained as correct one irrespective of an erroneous value at Q1, where Q1 is the O/P of FF1, Q2 is the output of FF2, and Q3 is the output of FF3. D and Q are the TMR input and output respectively. CP represents the clock pulse and ISSE is the current pulse. As three different systems are running in parallel, this design technique introduces more complexity and thrice the area of a Basic FF [2].

4.4 DMR

A well-known state-of-art is DMR (Figure-4.8) whereby the original module is duplicated. This reduces cost and provides error detection but, conventionally, error correction is not possible since voting cannot determine which of the two modules is in error [15]. Its drawback is that this technique can help in error detection only. On application of current pulse on the master latch of first FF,

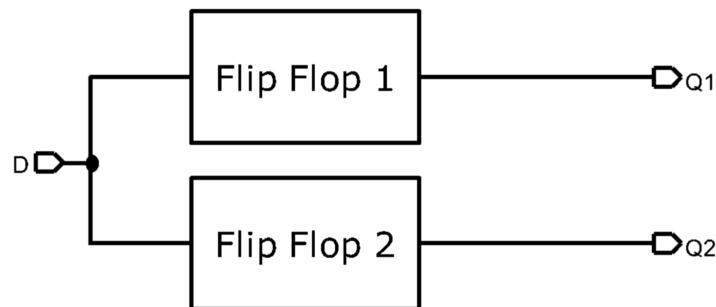

Figure 4.8: DMR

the waveform in Figure-4.8 has been obtained. The two outputs, Q1 and Q2, have been observed as different and this depicts the detection of the soft error. In this scenario, the correct output could not be detected. If both the outputs would have been same then it could be concluded that no error occurred and both the outputs are correct.

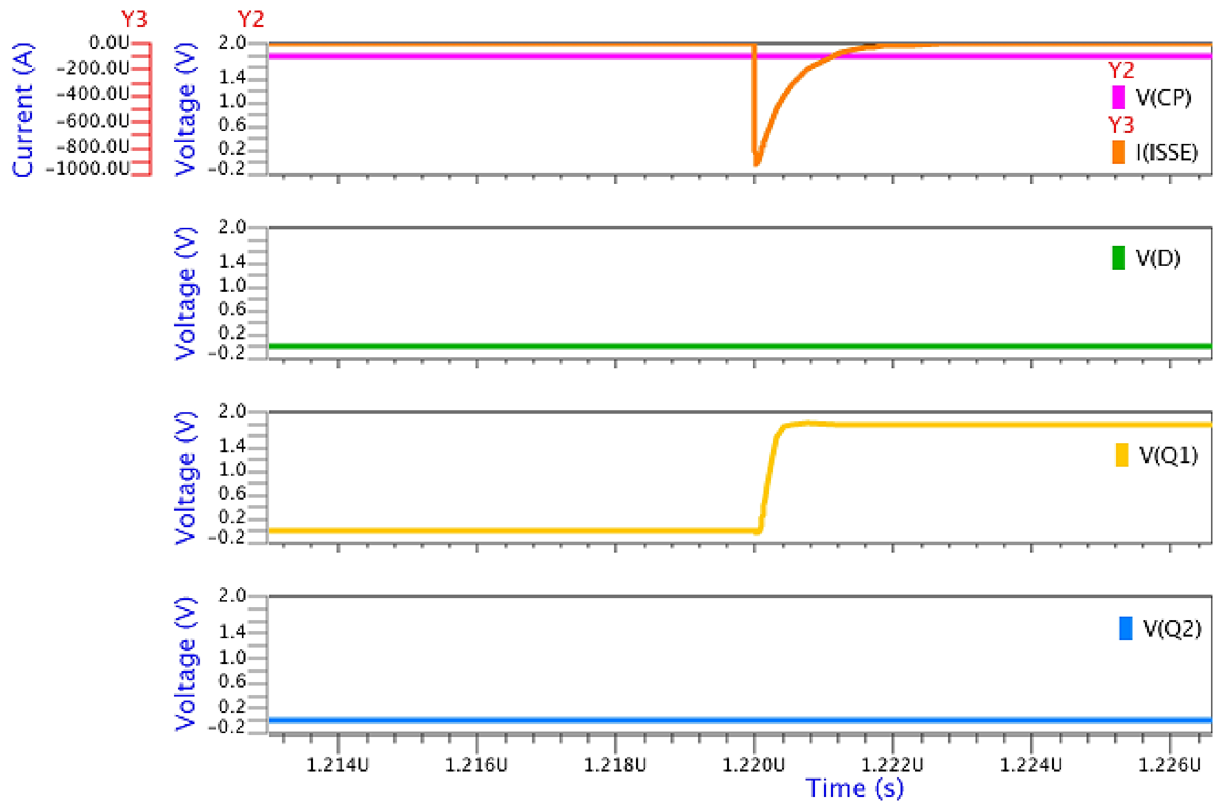

Figure 4.9: Simulation Results for DMR

4.5 Proposed Designs

Till now, we have discussed the state-of-art techniques to curb the SE in latches or FFs. The proposed designs in this chapter makes use of DMR technique and C-Element to enhance the error detection capability of DMR to error correcting one.

4.5.1 Basic DMR technique along with Error Correction and Delay Element (DMR-buff)

In this structure, as can be seen in Figure-4.10, the same data is captured in both the Flip-Flops but in FF-2, delay in data path is more than the delay in data path of FF-1 (from Section-3.2.3). Therefore, in case of timing issues, setup violation will occur first in FF-2. Care must be taken to set the clock frequency such that the setup violation does not occur. Such violation can be taken care by increasing the time period of the clock. Note that, a SE in the weak keeper (WK) does not have a major effect because the C-element output will be strongly driven by the latch contents (assuming single error) [16].

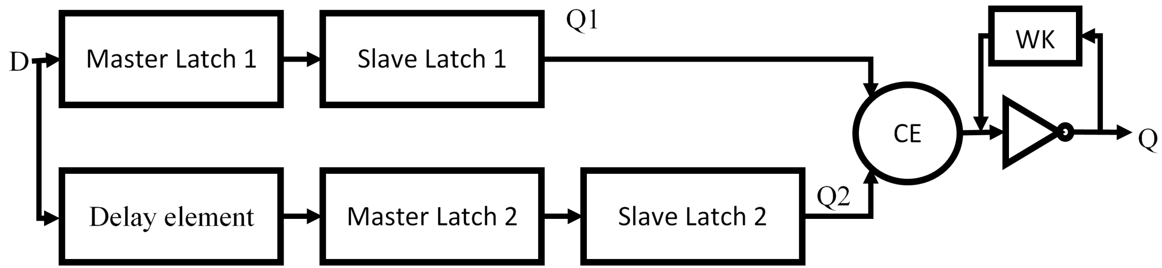

Figure 4.10: DMR-buff Architecture

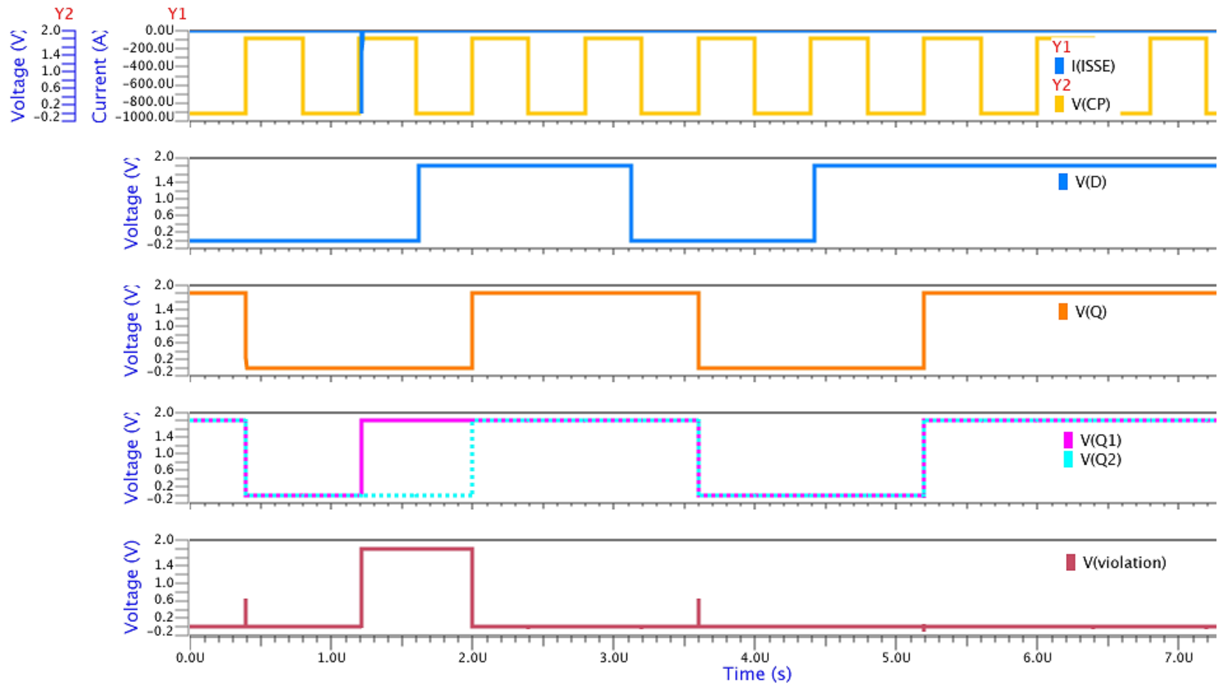

Figure 4.11: Simulation Results of DMR-buff Design

I(SSE) refers to radiation induced current pulse. V(CP) and V(D) refers to clock pulse and input data voltages respectively. Output of first stage (V(Q1)) and that of second stage (V(Q2)) forms the output of the system (V(Q)). This nomenclature is followed for all the simulation results in the manuscript.

4.5.2 DMR without Delay Element for high frequency clocked circuits (DMR-HF)

The delay in the DMR-buff design can be incorporated by using the internal delays of the two participating FFs rather than using the Delay Element. This in turn reduces area and power of the design.

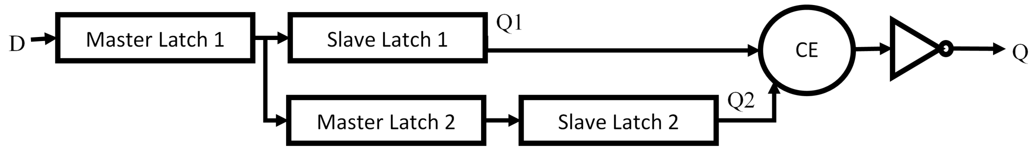

Figure 4.12: Architecture of DMR-HF

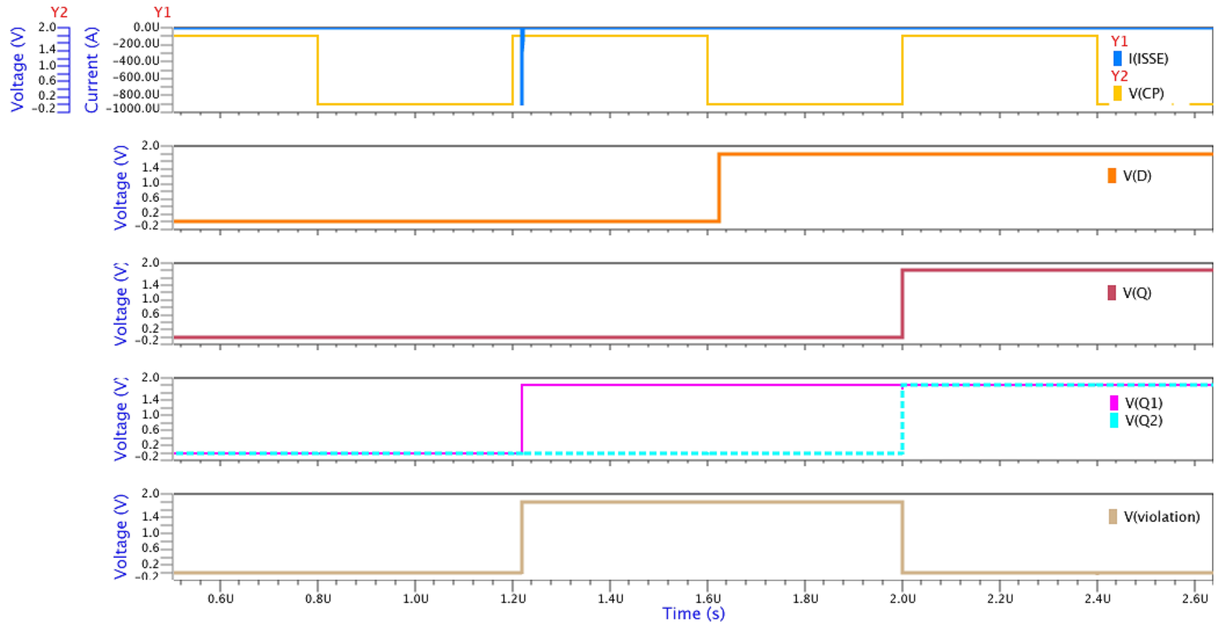

Figure 4.13: Simulation Results for DMR-HF Design

Similar to DMR-buff, DMR-HF is a robust solution but with lesser area. Working of both the designs can be compared with the respective simulation results.

4.5.3 DMR without Delay Element for clock gating circuits (DMR-PG)

Issue with DMR-HF is that it can be used in high frequency clock domains only. This is because the output node will gradually lose the charge stored in the state when CE is in float state. Thus DMR-PG has a Weak-Keeper to replenish the charge even if clock is gated low. Functioning whereas remains same for both the structures.

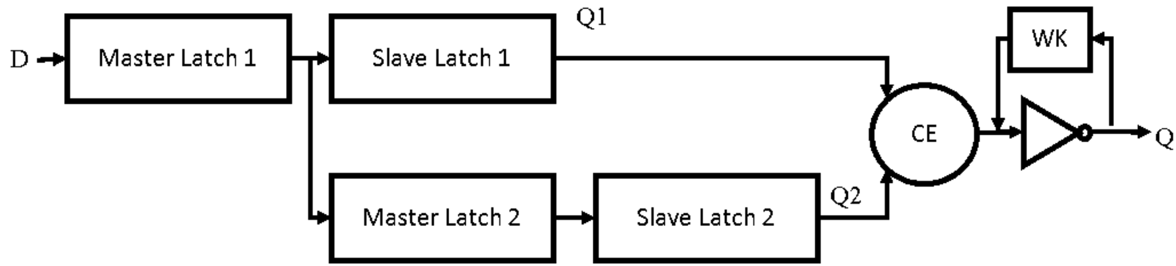

Figure 4.14: Architecture of DMR-PG

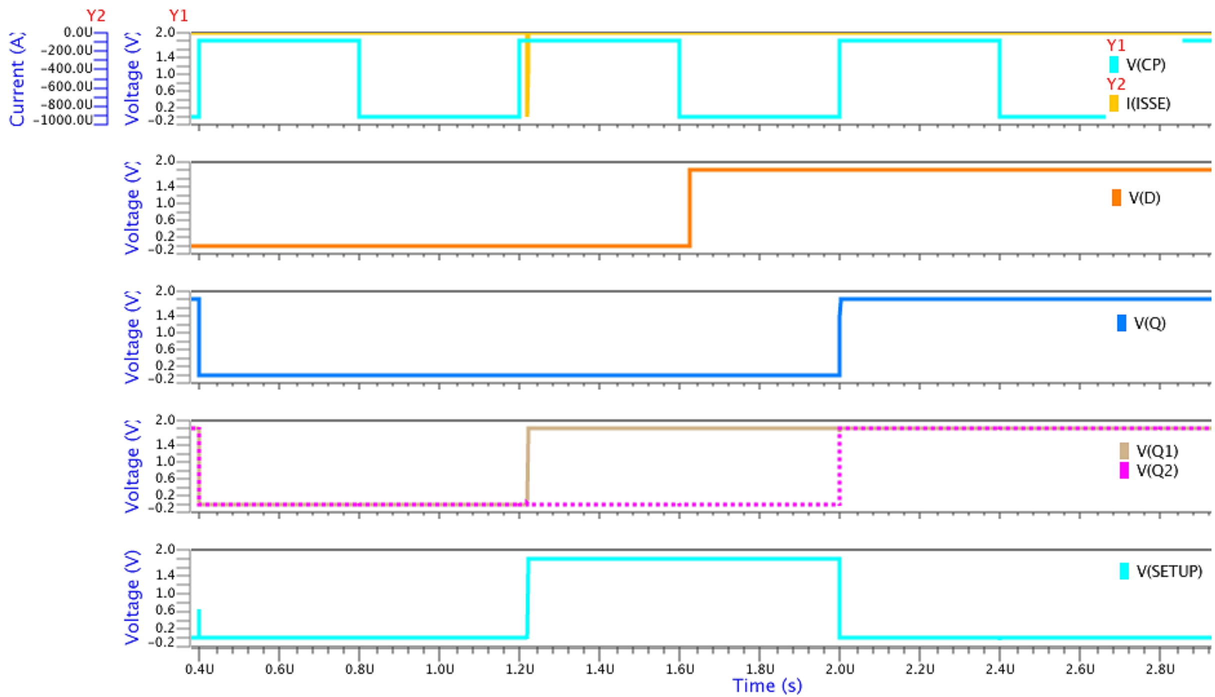

Figure 4.15: Simulation Results for DMR-PG

According to the simulation result of DMR-PG, this design is also error correcting design.

4.6 Summary

This chapter covered Dual Phase clock input designs. Starting with the state of art techniques for building RadHard Flip-Flop designs, some proposed structures like DMR-buff, DMR-HF and DMR-PG were discussed. According to the simulation results, the proposed designs are robust to the transient pulse.

Chapter 5

Radiation Hardened Single Phase Clocked Structures

5.1 Overview

In this section, a low cost radiation hardened structure is proposed. It makes use of capacitance stacking and DICE concept for increasing robustness. As opposed to dual phase clocked structures discussed in the previous chapter, single phase clocked structures work with inverted data along with direct data input. These structures give lower radiation sensitivity along with several times lower power consumption. A TSPC circuit with radiation hardened DICE latch was proposed [17]. It works on the phenomenon of pre-charged internal nodes which is sensitive to W/L of transistors. In the case of PVT variations, the pre-charging of nodes might fail. Moreover, in case of ion strike on TSPC input stage internal nodes, the data will flip, leading to erroneous results after C-element also. Thus it is not a practical design.

5.2 Why Single Phase Clocked Structures?

Number of sensitive nodes are less in Single phase (SP) clocked circuits. This can be understood as follows:

Let C1, C2, x, y, and z are capacitances of the marked nodes respectively. N and n denote the number of FFs that can be connected to clock buffers with output capacitance C2 and C1 respectively. Capacitance that a clock buffer can drive is same in both the cases. So C1 = C2. $x << a$ since the capacitance seen at a node due to a single inverter is much less than capacitance seen due to multiple connections in a Flip-Flop. Thus, number of FFs that could be branched out of clock buffer with o/p capacitance C1 is more than those connected to buffer with output capacitance C2.

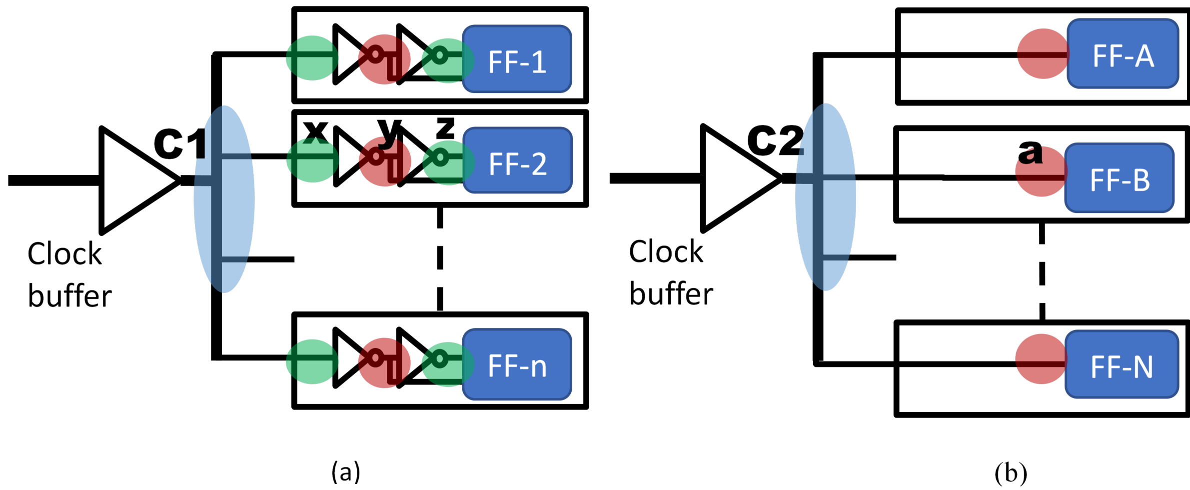

Figure 5.1: Clocked Structures (a) Dual Phase (b) Single Phase

Thus, if C1 = n * x ;
then C2 = N * a ;
where, $n > N$. Thus low capacitance nodes in the circuit are reduced in single phase clocked structures as opposed to Dual phase clocked structures.

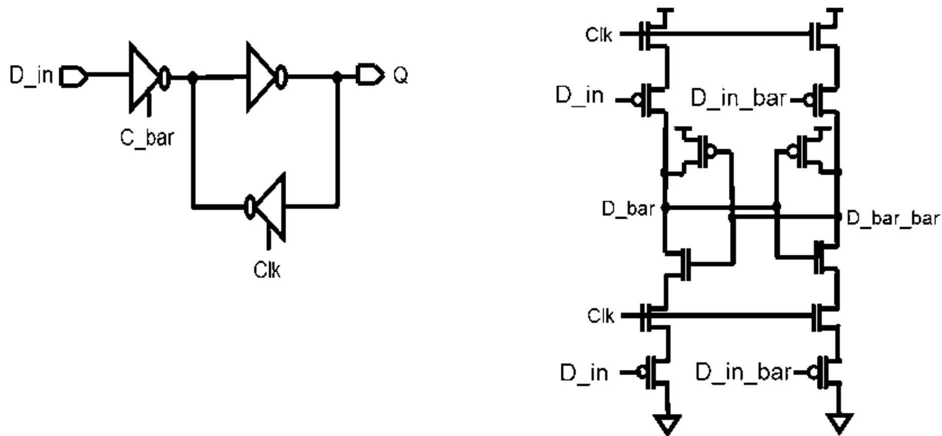

Figure 5.2: (left) Dual Clocked Latch, (right) Single Clocked Latch

5.3 Single Phase Clock FF Design

The proposed structure was formed in 180nm BCD9s technology implemented as differential input latches. It is a low cost alternative to dual phase clock design in terms of area and power. The design presented in this section makes use of capacitance stacking [13] [18], DICE concept [11-12], and single phase clock pulse based latches [10].

Dual phase clocked circuit require lesser number of clock tree cells for a particular number of FFs as

compared to single phase clocked circuit due to the lower capacitance seen at clock input of the FF. With lesser cells, power consumption would be lower in former in clock tree but internal inverter present in Flip-Flops would offset this gain and overall power consumption comes out to be more than single phase. For radiation hardening, the same quality results in robustness in single phase structures.

5.3.1 Principle of Operation

The proposed design is shown in the Figure-5.3 below. It utilizes following techniques: 1) Both master and slave blocks follow DICE redundancy scheme. 2) Single clock phase pulse for both master and slave blocks. 3) Transistor stacking is followed for both the blocks. 4) Cross coupling of master stage output and slave stage inputs. In conventional positive edge triggered FF designs

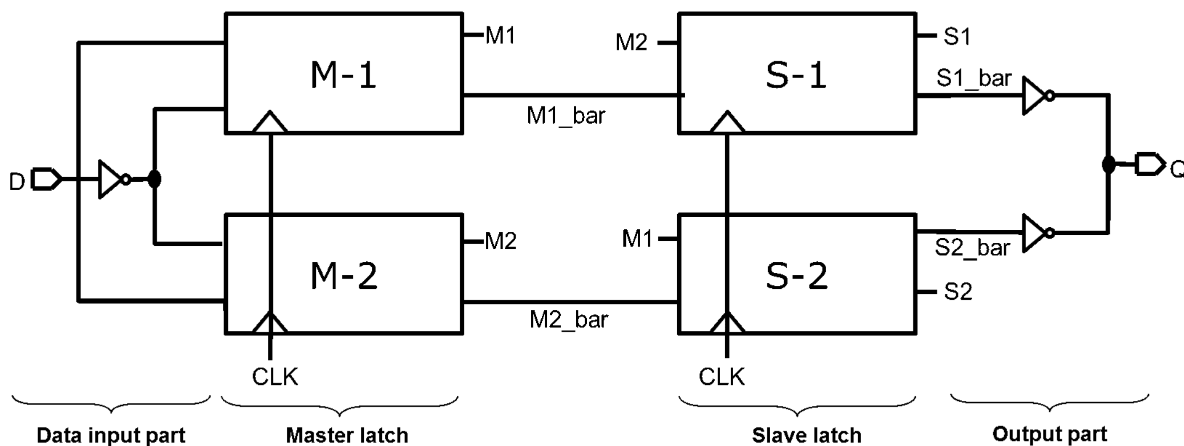

Figure 5.3: SPCD architecture

master latch and slave latch works on opposite phase clock pulse; whereas in SPCD designs, only a non-inverted clock input is enough for both master and slave latches to work as can be seen in Figure-5.3. This leads to reduction in error probability in case of glitches and skew in the clock input. Rather than using clock and its inverted input, this design requires the data and its inverted value to both the latches. The DICE configuration formed and cross coupling between master and slave stages provides the redundancy required for robustness. As opposed to pre-existing techniques like DMR and TMR, capacitance stacking is used to reduce the leakage current and in turn reduce power loss. This leads to higher resistance and capacitance as seen by any ion strike so a larger amount of charge is required for the flipping of the state stored. Thus, robustness of the design increases. Output of the slave stage is inverted to provide the final output of the Flop.

The restoration mechanism consists of master latch and its redundant block, data-input and its compliment. Data-input is translated to output (Q). In case of radiation strike on any sensitive node, the state might be affected and in this case, redundant nodes will help restore the correct value and thus prevent the output from flipping.

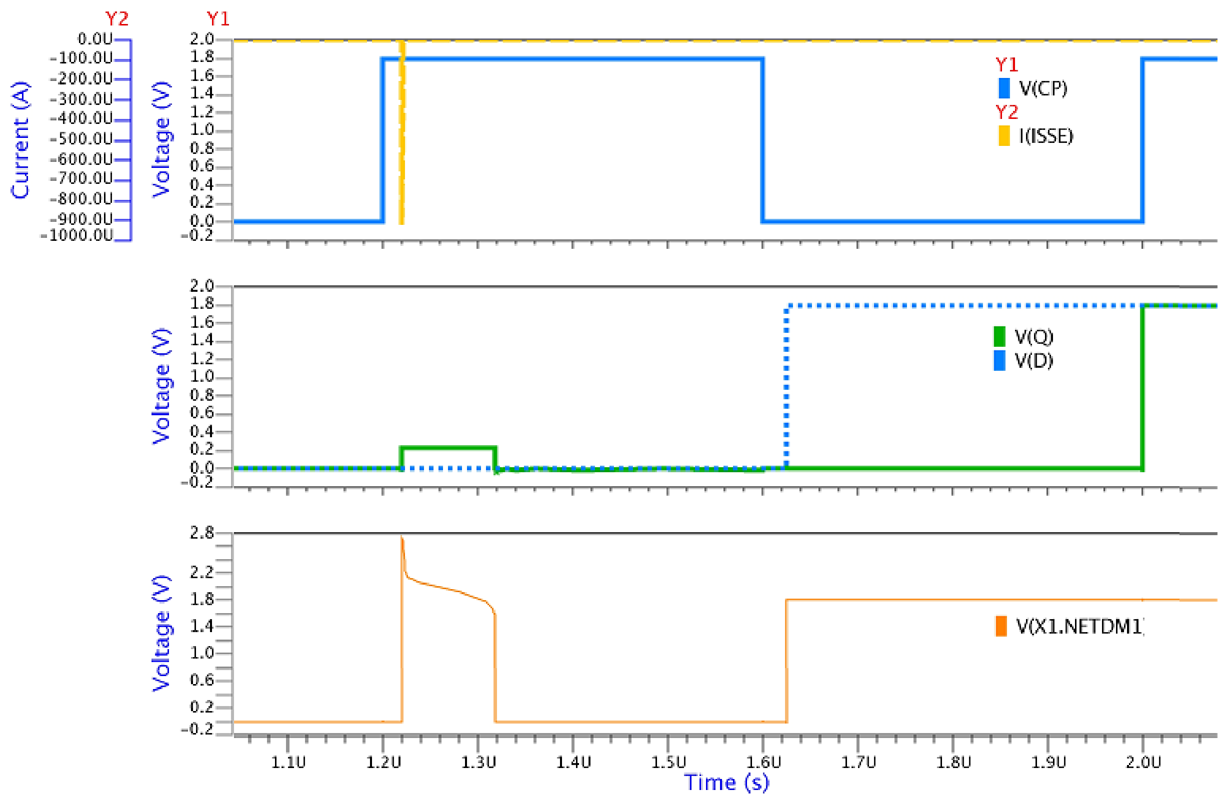

Figure 5.4: SPCD simulation result

Working of SPCD structure could be understood with the help of Figure-5.4 where transient pulse application at node 'netDM1' causes the state flip but this is not translated to the output. Moreover, the state of affected node is also recovering to the correct value with time.

Chapter 6

Results and Analysis

6.1 Overview

This chapter deals with analysis of various radiation hardened structures discussed in this work till now. The 7 Flip-Flop (FF) configurations were simulated at 25 degree Celsius (Typical scenario) with 1.8V and 1.2V as supply voltages. All the values plotted in the following graphs are normalized with respect to the basic FF structure.

Propagation delay, capacitances, power dissipation and timing analysis was done with the help of model file, spice (*.spi) file and input initialization of the circuit as set of inputs for the script. Further, functions were applied according to the analysis to be done. The calculations were done for varying clock slopes (20pS, 200pS, and 2nS). The results are presented in the subsequent pages.

6.2 Area Comparison

The 8 Flip-Flop configurations were compared on the basis of the area occupied and following results were obtained.

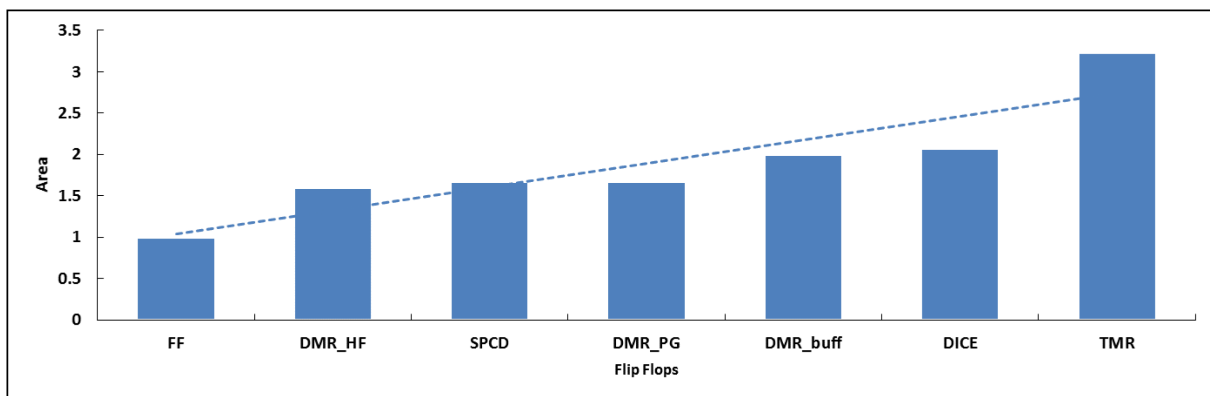

Figure 6.1: Graph for Area Comparison of all the FF Configurations

The proposed single phase design occupies lesser area than the traditional DICE design. With triple redundancy, TMR is most area expensive structure.

6.3 Propagation Delay Analysis

Propagation delay was calculated using the functions: TPDUD and TPDUU in ELDO where TPDUD is to calculate the fall delay and TPDUU is to calculate the rise delay. The following results were obtained:

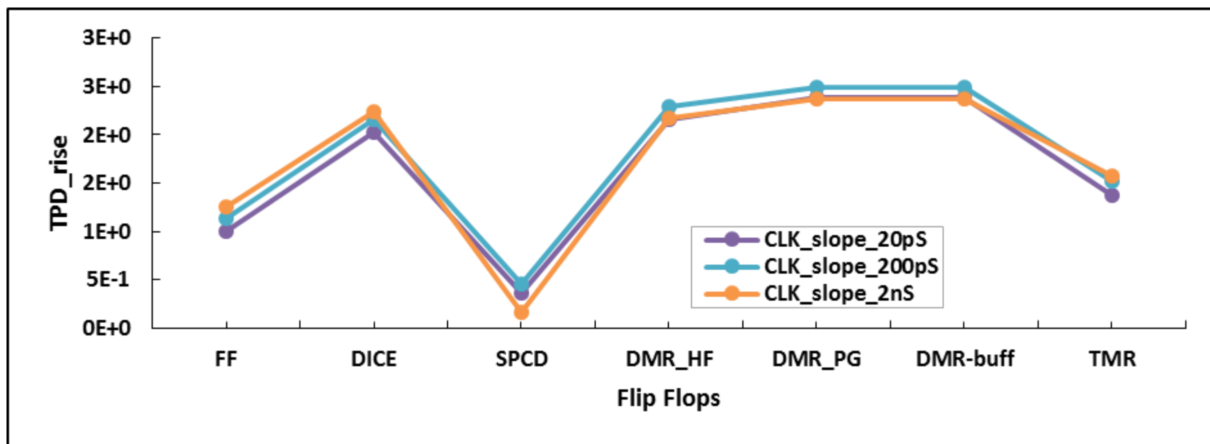

Figure 6.2: Rise time propagation delay with varying clock slope values

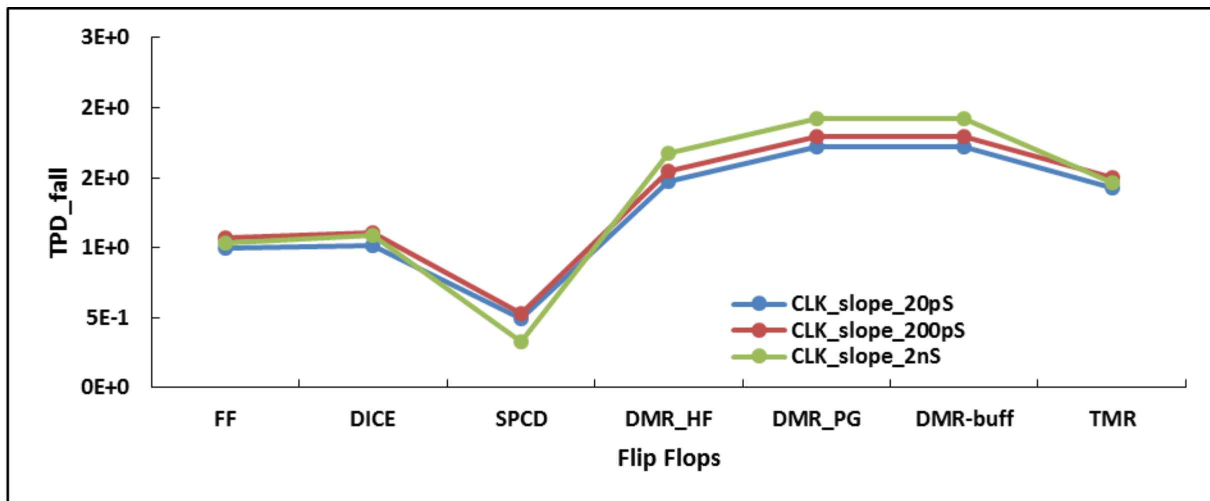

Figure 6.3: Fall time propagation delay with varying clock slope values

According to the trend, SPCD has least propagation delay whereas TMR is most expensive. This is because SPCD works on single clock phase. Thus both stages of a Flip-Flop works on the same edge rather than differing edges leading to fast output.

6.4 Clock Capacitance

The capacitance value seen at the clock input was calculated by integrating the current on that port and dividing it by the power supply value.

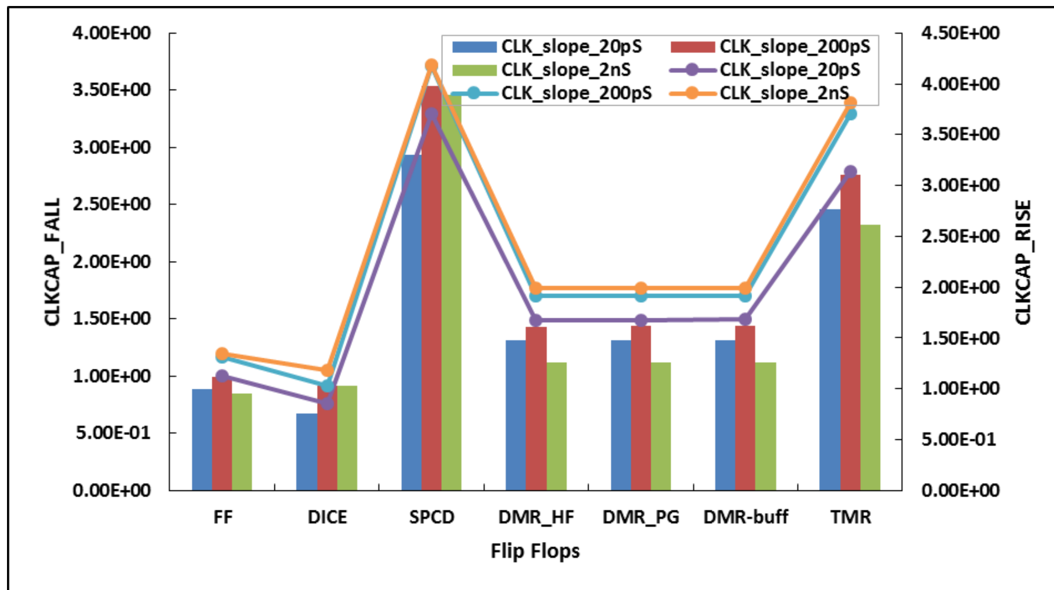

Figure 6.4: Rise time propagation delay with varying clock slope values. Bar graph present the Rising Clock Capacitance values whereas Line with Markers represent Falling Clock Capacitance values

Figure-6.4 shows the falling edge clock capacitance values plotted as lines and rising edge values as bar graphs. For both the values, SPCD has maximum capacitance and thus maximum robustness. Thus, more robustness is guaranteed in single clocked phase designs.

6.5 Timing Analysis

Less setup time is desired of a circuit. Delay in signal propagation increases with increase in resistance and capacitance of the circuit. Capacitance stacking leads to high RC circuits and this is the reason for high setup time in the proposed SPCD design.

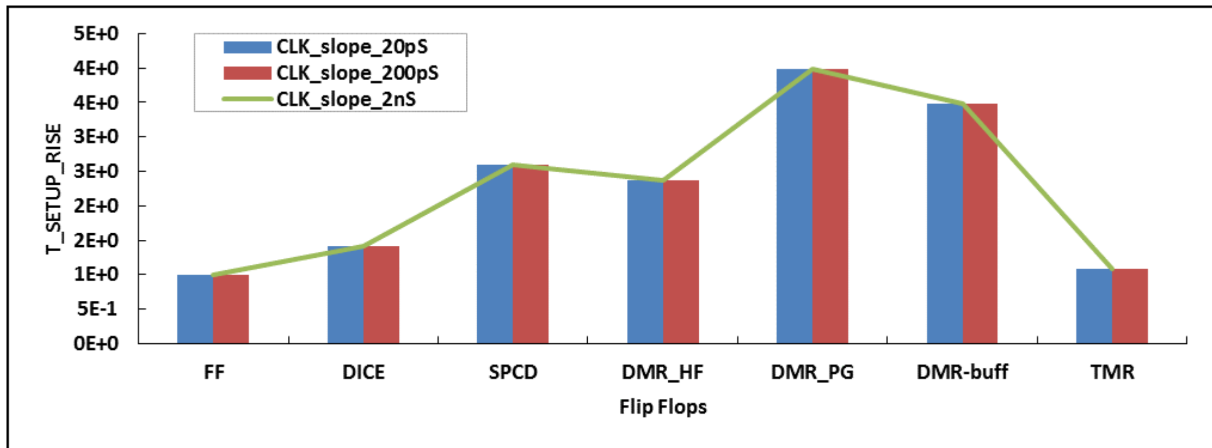

Figure 6.5: Setup Time for Rising Input Data

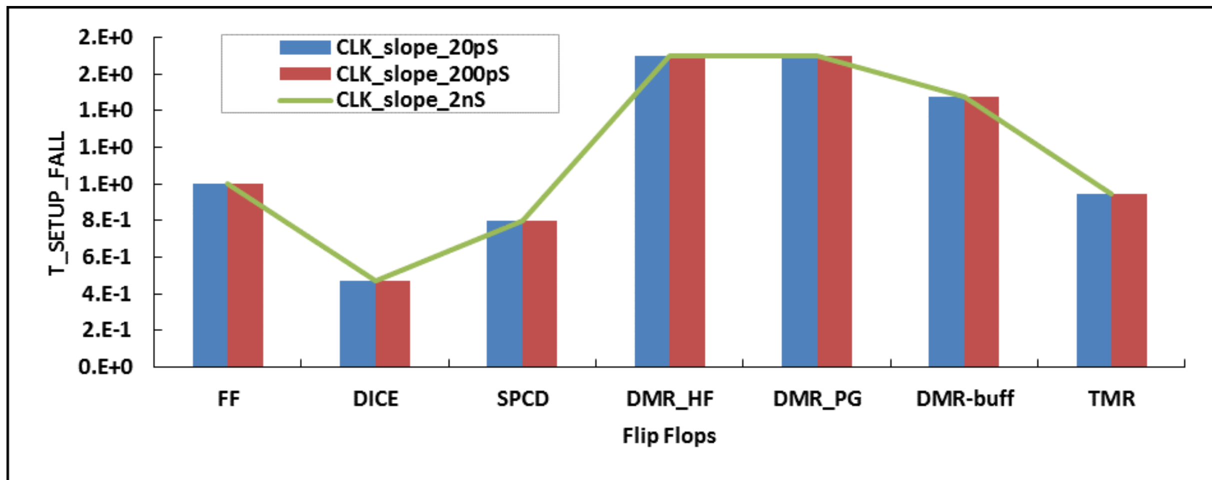

Figure 6.6: Setup Time for Falling Input Data

6.6 Activity Sensitive Power Analysis

Power analysis was done in three scenarios:

1. When activity factor = 0
2. When activity factor = 50%
3. When activity factor = 25%

Results are compiled in Figure-6.7 with varying clock slope for each type of analysis.

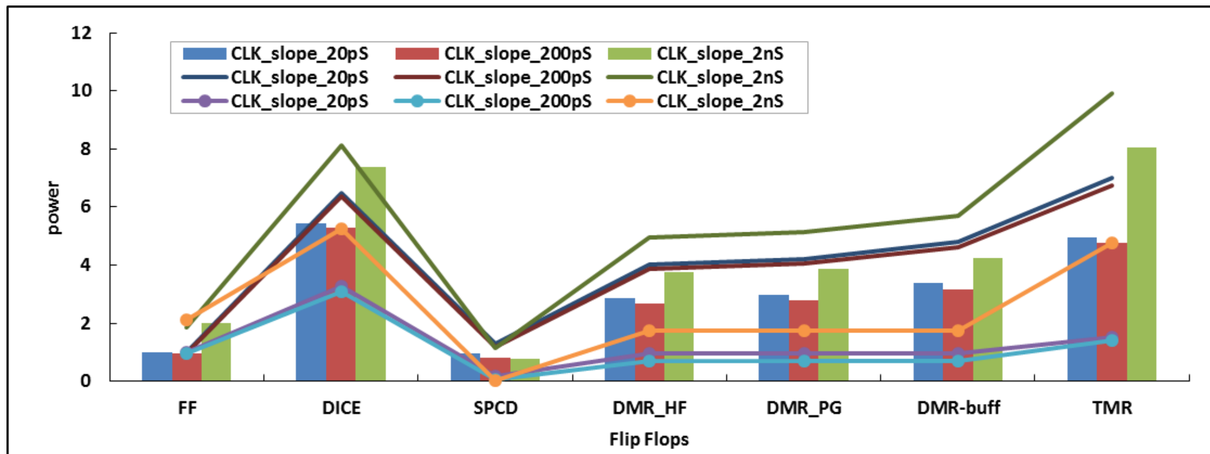

Figure 6.7: Power Analysis for Different Activity Factor and Clock Slope Line with Markers depict analysis with Activity Factor =0; Line Without Markers Depict 50% Activity Factor Analysis; Bar Graph Refers to 25% Activity Factor Analysis.

6.7 Overall Cost Analysis

For Clock slope of 200ps and 0.02pF of Load Capacitance, the data was analyzed and Table-6.1 was made. All the values have been normalized with respect to the Basic FF. This is to enable a comparison amongst all the structures for selection according to application requirements.

Figure-6.8, Figure-6.9 and Figure-6.10 shows the trend followed by various traits like Q_{CRIT} on clock node (Clk_node_Q_{CRIT}), Area, Propagation Delay, Capacitance at clock node and setup time of the flip-flop with respect to Dynamic power dissipation of the flip-flop with 0%, 50%, and 25% activity factor respectively.

Table 6.1: CAD Simulation Results and Comparative Analysis

Parameter	**Flip-Flops**						
	FF	DICE	TMR	SPCD	DMR_HF	DMR_PG	DMR_buff
Area	1	2.07	3.23	1.6	1.63	1.67	2
Propagation Delay (T_{PD})	1	1.406	1.428	0.457	1.693	1.900	1.900
Clock Node Cap. (Rising Clk Edge)	1	0.922	1.991	3.583	1.449	1.454	1.454
Clock Node Cap. (Falling Clk Edge)	1	0.786	1.986	3.193	1.460	1.463	1.463
Clock Node Cap. (Average Values)	1	-4.488	1.787	-11.934	1.895	1.821	1.818
T_{SETUP} (Rising Data Edge)	1	1.419	5.914	2.600	2.371	3.990	3.476
T_{SETUP} (Falling Data Edge)	1	0.474	2.514	0.798	1.696	1.696	1.478
T_{SETUP} (Average values)	1	0.946	4.214	1.699	2.034	2.843	2.477
P_{DISS} (Activity Factor = 0%)	1	1.033	3.220	0.070	0.726	0.727	0.729
P_{DISS} (Activity Factor = 50%)	1	6.646	7.311	1.246	4.060	4.225	4.837
P_{DISS} (Activity Factor = 25%)	1	4.919	5.545	0.854	2.820	2.920	3.329

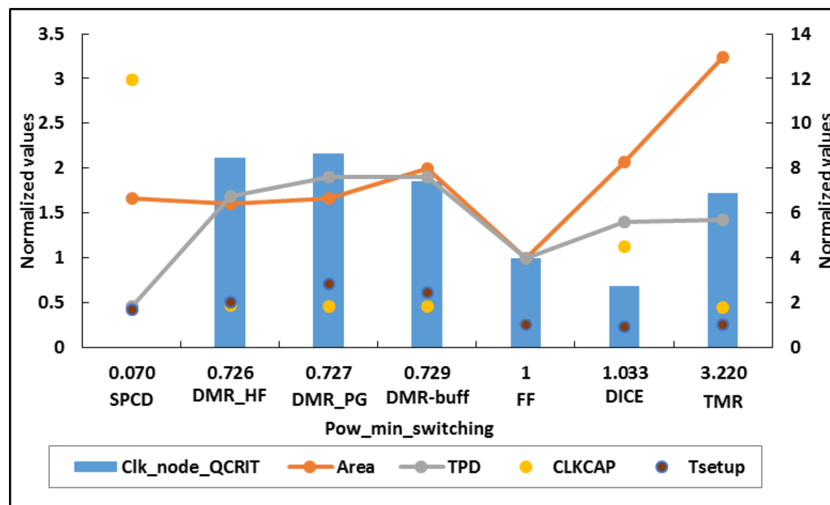

Figure 6.8: Variation of all parameters with respect to Power for 0% activity factor

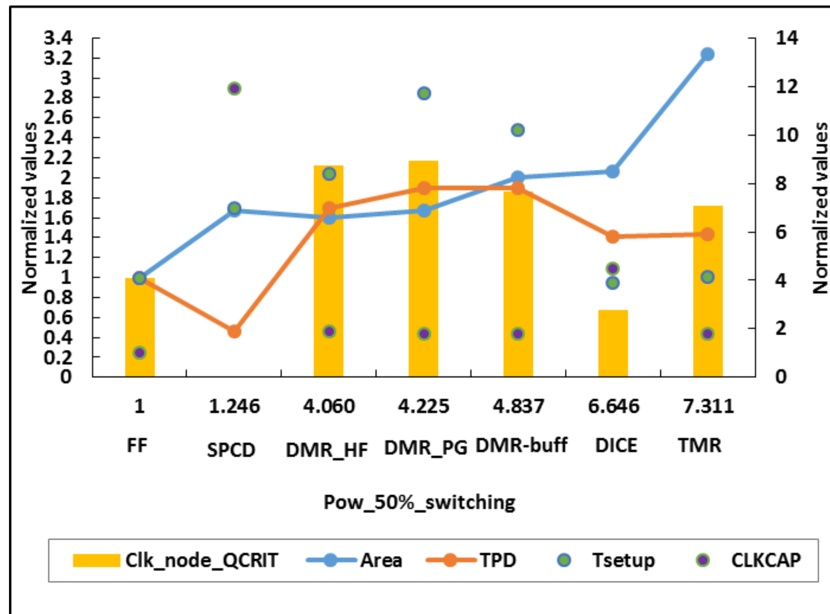

Figure 6.9: Variation of all parameters with respect to Power for 50% activity factor

As seen in Figure-6.9, TMR has highest power dissipation and area requirement. Clk_node_Q_{CRIT} is 0 for SPCD due to the absence of low capacitance clock node. Setup time is observed to be highest in canary FF based structures in Figure-6.8, Figure-6.9 and Figure-6.10.

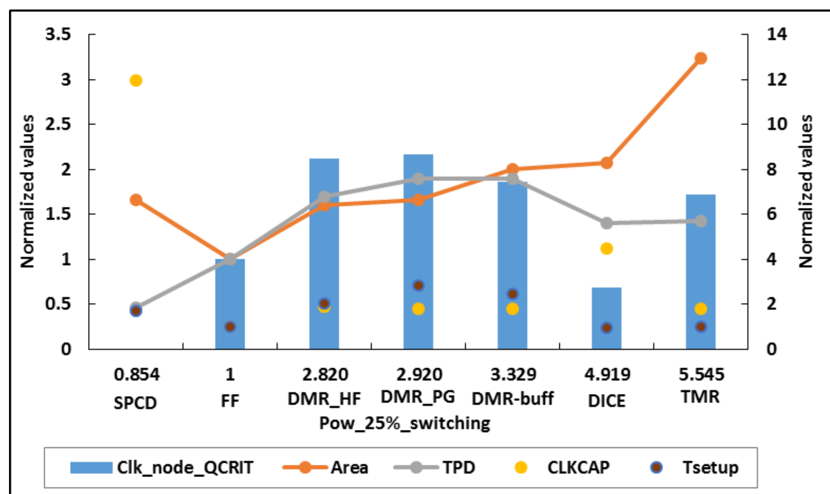

Figure 6.10: Variation of all parameters with respect to Power for 25% activity factor

Based upon above results, a set of design rules could be drawn to facilitate engineers to design the basic flip-flop according to their design requirements.

6.8 Robustness Analysis

To evaluate the radiation sensitivity at CAD level, a specific Monte-Carlo based current injection simulation environment was developed. In particular, a double exponential current pulse was used to reproduce the radiation-induced current, as discussed in Section-3.2.2. The pulse is introduced in the simulation either as a source or a sink depending on the logic state of the node. One-thousand Monte Carlo iterations [19] were performed for each structure, to obtain the distribution of the critical charge. The results are compiled in Table-6.2.

Table 6.2: Radiation Ion Simulation Results

Parameter	**Flip-Flops**						
	FF	DICE	TMR	SPCD	DMR_HF	DMR_PG	DMR_buff
Monte-Carlo Simulation Results	81.4%	0	0	0	0	0	0
Sensitive node Q_{CRIT} (pico-Coulomb)	0.002	0	0	0	0	0	0
Clock node Q_{CRIT} (normalized values)	1	0.68	1.72	No sensitive node	2.12	2.17	1.86

According to these values, SPCD is the most robust design.

6.9 Silicon Results

A test chip was made with radiation hardened shift registers, BIST and PLL for testing the basic Flip-Flop, DICE, TMR, and SPCD configuration under radiation environment. Alpha, heavy ion and neutron tests were performed. The results are presented in the form of ‘susceptibility of a device’ also known as ‘SEU cross section’ defined as probability that a device will fault per unit Fluence. Fluence refers to particles per cm^2.

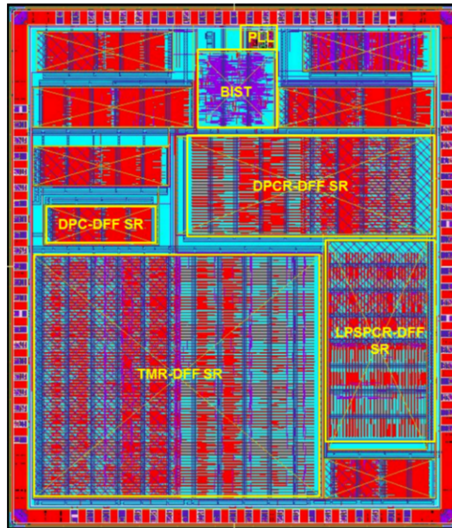

Figure 6.11: Test-Chip Layout View (Test-Chip Specifications: ST Confidential Information)

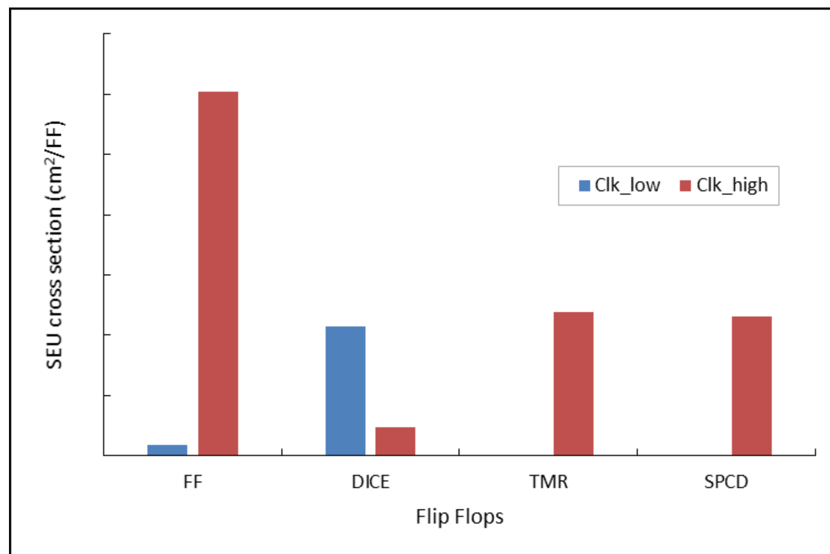

Figure 6.12: Alpha Particles Test Results (Test Facility: Dept. of Information Engineering, Padova, Italy) (Y-axis Values are ST Confidential Information)

According to Figure-6.12, TMR and SPCD are most robust whereas the basic FF is most sensitive to alpha particle radiation. LET of alpha particles is 5.49 MeV.

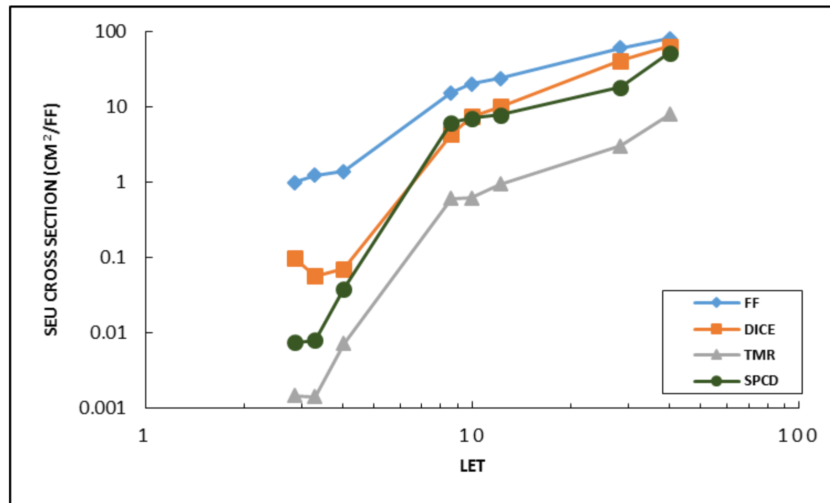

Figure 6.13: Heavy ION Radiation Test Results for Input Voltage 1.8V (Tests Facility: Legnaro National Laboratories, Italy) (Y-axis and X-axis values are scaled value; exact values are ST confidential information)

Heavy ions of varying LET were used to perform the tests and according to Figure-6.13, SPCD and TMR are most robust against heavy ions also.

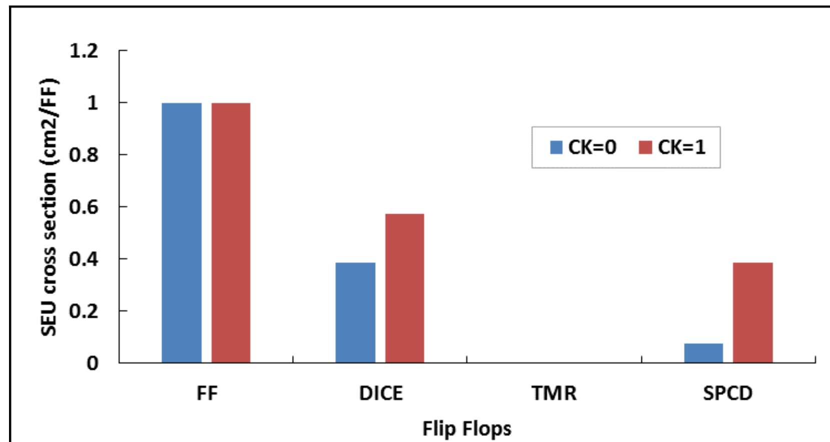

Figure 6.14: Neutron Test Results for Input Voltage 1.8V (Test Facility: Dept. of Information Engineering, Padova, Italy) (Y-axis values are scaled values; exact values are ST confidential information)

Continuing the trend of previous tests, neutron test prove that TMR and SPCD are most robust.

6.10 Summary

To avoid redundancy in the data, only 1.8V simulation results are shared since simulation results for 1.2 V were in accordance to the 1.8V results. It can be observed from the graphs that analysis for 20pS and 200pS clock slope show similar results whereas 2nS clock slope show slight deviation in absolute values but the pattern and flow of information is same for all the three sloe values.

According to the above study, single clock phase structure are faster and more robust with lesser area and power dissipation than the dual phase clock structures. TMR is made most area and power expensive in the process of being most robust.

Silicon results prove that TMR is most robust followed by SPCD structures. It is known that TMR is most costly solution to the radiation related issues. Thus, SPCD must be the most preferred choice for low cost radiation hardened solutions.

Chapter 7

Design Rules for Radiation Hardened Circuits as per Application Requirements

7.1 Overview

Each trait (area/ robustness/ power/ delay) of a CMOS circuit is required to be optimized. The problem during the circuit optimization is that various trade-offs can be seen; like, incorporating redundancy to increase robustness leads to increase in area and power of the circuit.

This chapter is to facilitate the engineer to choose from the designs according to the application requirements. For example, if a high speed application requires maximum robustness then TMR or SPCD must be the preferred designs as can be seen in previous chapters. Moreover, the design rules will help the designer to design FF configurations considering the trade-off according to their design requirements.

7.2 Design Traits

7.2.1 Robustness

According to the state-of-art techniques, robustness could be increased by:

1. Adding Redundancy
    - Tradeoff: Circuit will require high area and power. It might lead to increased propagation delay.
2. Increase in capacitance of a node [2]

- Tradeoff: Increased propagation delay.

3. Distant susceptible nodes

   - Distant susceptible nodes refers to far-apart placing of susceptible nodes.
   - For example, Each FF of a TMR circuit must be interleaved with another TMR's FFs so that if a radiation particle has long range then multiple bit upsets are not encountered in a FF.

4. Large load capacitance of design

   - This decreases susceptibility of the output node of the FF but in turn requires more power and time for the signal to propagate.

5. High power supply value

   - This leads to lower radiation susceptibility as well as lower Setup times and propagation delays but must not be a preferred choice for low power applications.

6. Large clock node capacitance

   - It is clear from the analysis till now that single phase clocked circuits [3] remove the low capacitance clock node from the list of susceptible nodes. Thus, as compared to dual-phase clocked circuits, single phase ones must be used for applications having radiation hardening as a critical requirement. At the same time, SPCD and similar structures have large Setup Time as can be seen from table-6.1.
   - According to the silicon results, TMR is the most effective radiation hardening methodology till date. Thus if area and power requirements can be compromised then TMR must be the most preferred architecture.
   - Order of robustness, as recorded through On-chip test results is as follows:

     TMR >= SPCD > DICE >> Basic FF

     According to this relation, maximum robustness might consume most area.

7.2.2 Setup Time

Delay in data path increases the Setup Time of the circuit. Due to large capacitance stacking at every stage in SPCD, large resistance and capacitance is seen by the input signals. Thus more delay in data path is experienced in Single phase clocked circuits than dual phase clocked structures. If less Setup time is demanded of the application then Capacitance stacking must be avoided at input stages specially. This would lead to lower capacitance and to more susceptible nodes.

Hence a trade-off exists between robustness and data path delay due to higher capacitance nodes.

7.2.3 Propagation delay

Circuits having higher Setup time will lead to more propagation delay due to high data path delay experienced. SPCD is the best choice for designing fast circuits.

Canary Flip-flop based circuits will have maximum propagation delay and thus must not be opted for fast processing circuits.

7.2.4 Area and Power

Redundancy is added to improve the robustness of the circuits. This in turn increases the area multiple folds. For example, TMR has over three times the area requirement and DICE has twice than a basic FF. Increase in area leads to proportionate increase in Dynamic Power dissipation.

Area does not have a linear relation with Propagation delay of FF designs. Whereas, it has a linear relation between Power Dissipation and Robustness also in few cases. Application Designer must take care of the fact that incorporating redundancy for robustness will lead to high area and power requirements in the circuit. Transistor stacking also increases area.

Differing trends were observed for power dissipation in circuit in case of high activity factor an in case of low activity factor. Higher activity factor shows larger power dissipation. As tabulated in Table-6.1, to build low power radiation hardened design, SPCD must be the preferred choice.

Conclusion and Future Work

This research contributes to the field of radiation hardened CMOS circuits. The impact of radiation on 180nm BCD technology was studied. A single phase clock, DICE and capacitance stacking based radiation hardened design is proposed and studied with the help of CAD level as well Silicon based simulations. RadHard designs with dual phase clock and DMR technique are also proposed and simulated. State-of-art technology designs and proposed designs were compared and studied. Cost effective solutions in terms of area and power are discussed and proposed. Authenticity of CAD level simulations is validated by theoretical framework as well as on-chip results.

This domain can be further explored with the help of device level modelling. This helps in analysis of effect of ion strike on the device by considering different parameters of the device as well as radiation particle. Further study could be done by considering multiple particle strikes (as seen in spatial-environment).

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