Digital LDO with Analog-Assisted Dynamic Reference Correction

Shrestha Bansal

Indraprastha Institute of Information Technology, Delhi

Under the supervision of

Dr. M.S. Hashmi
and
Mr. Nitin Bansal

Submitted in partial fulfillment for the degree of

Master of Technology

Electronics and Communication Engineering,
with specialization in VLSI and Embedded Systems

June, 2017

Certificate

This is to certify that the thesis titled "Digital LDO with Analog-Assisted Dynamic Reference Correction" being submitted by Shrestha Bansal to the Indraprastha Institute of Information Technology (IIIT) Delhi, for the award of the Master of Technology, Electronics and Communication Engineering (with specialization in VLSI and Embedded Systems), is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

Dr. Mohammad S. Hashmi
Associate Professor
Department of Electronics and Communication Engineering,
Indraprastha Institute of Information Technology (IIIT) Delhi,
New Delhi 110 020

Mr. Nitin Bansal
Director: Analog and Mixed Signal Design
INVECAS

This thesis is dedicated to mummy and papa for everything

Acknowledgements

The work of this thesis was carried out during the course of industrial internship at STMicroelectronics, India during the year 2016-17. I would first of all like to express my deep gratitude to my faculty advisor Dr. M.S. Hashmi for his invaluable support, guidance and for providing me with a learning environment throughout the course of my graduate studies. I would also like to thank my co-advisor Mr. Nitin Bansal (STMicroelectronics) for providing me with the opportunity to work in a highly learning oriented and research driven environment at STMicroelectronics, and his able guidance which motivated me to pursue analog circuit design.

This work could have never been completed without the technical discussions, interactions and support from Mr. Abhirup Lahiri at STMicroelectronics who also introduced me to the design of voltage regulators, and inculcated in me the interest for Digital LDOs.

I would always be indebted to Mr. Gaurav Sharma and Mr. Rahul Gupta, at STMicroelectronics for helping me understand the basic intricacies of analog circuit design and also for helping me with any issues during the implementation of this work. I am also thankful to Mr. Nishant Sharma at STMicroelectronics for doing the layout of this design.

I would next like to thank my senior, Shashwat for the discussions on the modelling of this design along with any big or small issue that I faced; my batch mates Yatharth, Paritosh, Ankush, Shivam, Vivek and Shipra for their valuable inputs and moral support; and my juniors Ishaind, Ankush and Vaibhav for help with figures.

Finally, I am grateful to mummy and papa for their constant love, support and belief in my abilities which motivate me to keep learning and progressing. I could never have done anything without the constant support and push by my brother Utkarsh.

Abstract

Most modern circuit designs have a mix of analog and digital circuit blocks integrated on a single chip. Such designs require a dedicated power management unit to provide a stable, regulated and clean power supply. This is achieved by using LDOs. Analog LDOs are accurate and have a fast transient response suitable for driving analog core on the chip. However, such LDOs are not scalable and cannot regulate lower voltage domains. Digital LDOs are thus used to supply lower voltage domains required for digital cores. Digital LDOs have a poor transient response with a poor DC load regulation.

A fully on-chip 200mA class, flash ADC based digital LDO is proposed in this work with analog-assisted dynamic reference correction to improve the DC load regulation and a faster transient response. The proposed LDO can be easily scaled to drive a larger or smaller load current. An effective way to test noise at the output of the power delivery network using S-parameters has also been demonstrated in this work. Using this PDN analysis, we show a significant reduction in the simulation time.

The full custom design has been implemented in STMicroelectronics 28nm FD-SOI CMOS technology and the device has been sent for fabrication. We achieve a 0.005mV/mA load regulation capability for 200mA load current variation using 5nF load capacitance, with a worst case settling time of 139ns and a peak-to-peak ripple of 7.8mV, using the post layout simulations.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

In the modern day, we are surrounded by gadgets and devices including portable ones which include mobile phones, tablets, music players, etc. Most of these devices are designed to operate at a pre-defined constant voltage. Almost all of these devices use a battery to operate. The battery supplies a voltage, which overtime keeps on reducing as a result of discharging. Due to this discharging, batteries are unable to supply a constant power supply. Consistent with the Moores law, technology has been scaling fast. This not only leads to the scaling of channel length of the transistor, but also of the voltage domains on which the circuits operate. As the operating voltage scales, a stable power supply is required since the device characteristics are very sensitive to supply variations. These issues coupled, lead to the demand of a voltage regulator circuit which can supply clean and regulated voltages.

Low dropout voltage regulators have become a preferred choice of voltage regulating circuits due to their high accuracy and current efficiency. Most integrated circuits (ICs) have a power management unit along with some analog and digital circuitry. With the advancement in IC design techniques, there has been a rise in IC designs which have multiple voltage domains existing on a single chip. For this purpose, switching regulators, primarily buck or boost as used to generate these domains from a constant supply. These switching regulators introduce large ripples in the supply due to the RLC oscillations introducing switching activity. Such a supply is not suitable for analog designs which are highly susceptible to noise in the supply. This calls for a need of LDOs between the circuitry and the switching regulators. Increasingly, there has been a demand for lower voltage domains for digital circuitry along with relatively larger voltage domains for analog circuitry. For larger supply domains, analog LDOs are generally used, which are unable to operate at near-threshold voltages, digital LDOs capable of doing this were designed. Digital LDOs however suffer from

large ripples, slow transient response and poor DC load regulation.

In this work, a digital LDO is designed and simulated with an improved DC load regulation capability, while minimizing the output ripple and improving the transient performance.

This dissertation is organized as follows: chapter 2 contains the background of the problem and related work done in this field; chapter 3 explains the proposed work which lays an outline for the digital LDO design; chapter 4 presents the power delivery network analysis to estimate output noise faster; chapter 5 shows the simulation results. After highlighting the possible future work in chapter 6, we conclude in chapter 7.

Chapter 2

Related Work

Conventional Analog LDO design as shown in Fig. 2.1, uses an error amplifier in a stable negative feedback configuration to vary the on-resistance of a pass transistor switch. This, in turn varies the amount of current flowing from the transistor into the load. As a result, the output voltage settles at the reference voltage, so that the transistor provides exactly the amount of current as required by the load.

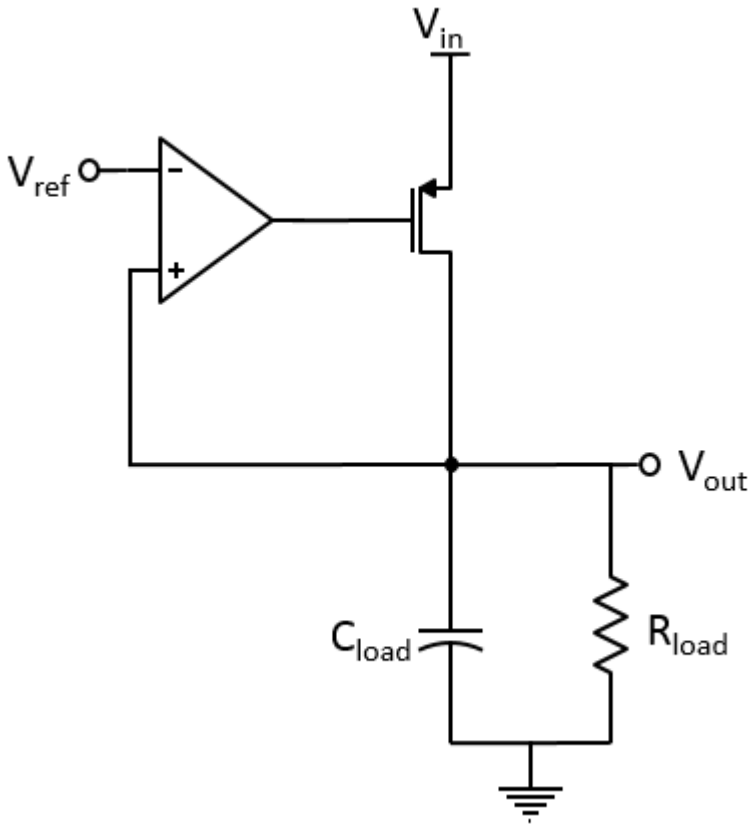

Figure 2.1: Analog LDO

Further, LDOs can be divided into classes based on their capability to ensure open-loop stability. A conventional LDO employs a large off-chip capacitor at the load to compensate a sharp transient in load current, creating a dominant pole at the output. This imposes a penalty in terms of larger chip area and also leads to several integration issues. Other LDOs use the Electrical Series Resistance (ESR) of the load capacitor to cancel the pole with zeros. In this case, however, stability is dependent on the value of ESR, which is itself dependent on temperature. Over time, designs have evolved to use Miller compensation techniques to generate an internal dominant pole, therefore ensuring stability without using a large off-chip capacitor. Such a LDO has a poor transient performance and a degraded PSRR as compared to conventional LDO. Several design modifications have been proposed to improve the transient performance of such LDOs. All such modifications lead to an area or power overhead. Even with the additional circuitry, such LDOs fail to operate at near-threshold voltages. Digital LDOs have become effective alternates for Analog LDOs due to their low-voltage operability and process scalability.

Digital LDOs use an analog-to-digital converter (ADC) to sense the output voltage and then perform reconstructive control on this digital value. The system then converts this digital signal back into analog output using a digital-to-analog converter (DAC). The advantage of a digital LDO is that it can work on low input voltages and is scalable. However, its performance is not as good as an analog LDO.

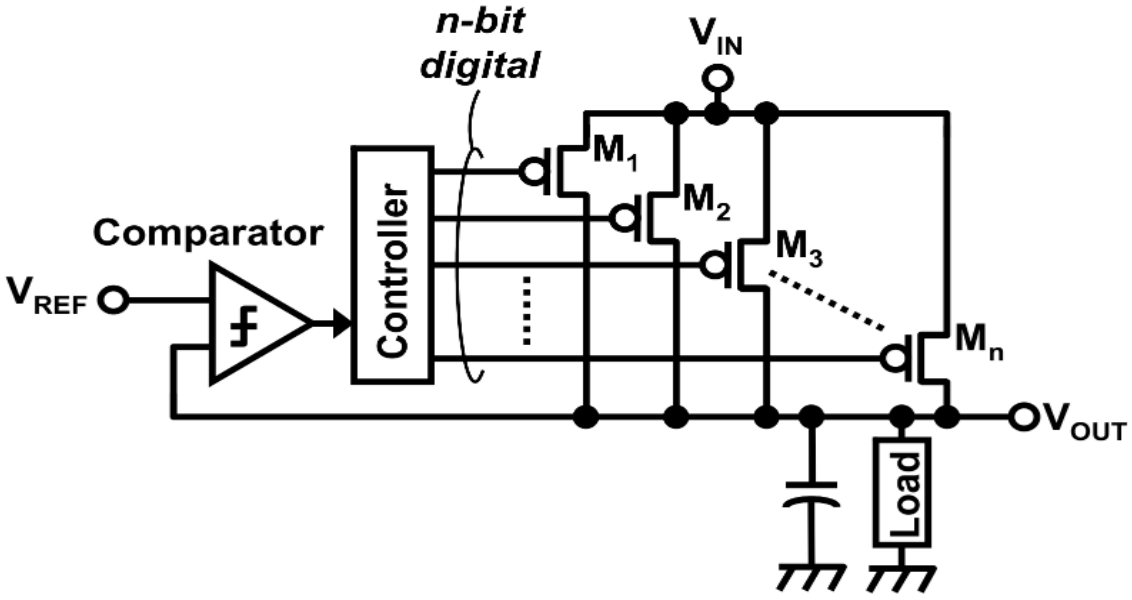

Figure 2.2: Conventional Digital LDO [7]

Digital LDO, first introduced in [7], used a bi-directional shift register to control the number of turned on switches based on the difference between reference and output voltage level. Fig. 2.2 shows a block diagram of this conventional digital LDO design. This design faced a large ripple of about 90mV, which might be undesirable. Besides, it had a poor DC load regulation of 0.65mV/mA. Coarse-Fine dual loop has been used in [3, 5] to improve the DC load regulation and minimize the output ripple magnitude. The transient performance of such an LDO is based on the speed of the clock driving the shift registers. A fast clock implies a fast transient response, with a large dynamic power consumption, governed by equation 2.1. A slow clock on the other hand would reduce the dynamic power consumption, but will also slow down the transient response. Thus, synchronous Digital LDO designs suffer from a power versus speed trade-off. To reduce the dynamic power consumption, an event-driven digital LDO was proposed in [4]. This design however faced large droop voltages of 10% value, while consuming a large on-chip area.

$$P_{dynamic} = \alpha.C_L.V_{DD}^2.f_{CLK} \tag{2.1}$$

In this work, a fully on-chip Digital LDO supporting load currents up to 200mA is proposed with a fast transient response and improved DC load regulation, using a small load capacitor.

LDO Specifications and Design Parameters

Dropout Voltage: It is the voltage difference between the input and output voltage to keep the regulator operational. It is defined as the voltage drop across the pass switch as shown in Fig. 2.1. A low dropout voltage is desirable as it leads to increased power efficiency of the regulator. However, to maintain the pass switch in saturation, a minimum fixed amount of dropout is required.

Quiescent current: It is defined as the current required by the regulator to ensure proper biasing conditions and remain operational in no-load conditions. Alternatively, it is defined as the difference between the current drawn from input supply and the output current delivered at the load. A lower quiescent current is desired for maximum power efficiency. It is the current that does not directly contribute to the output power delivered, and consists of bias currents to the reference generator, error amplifier, etc.

Load Regulation: It is defined as the capability of the regulator to maintain the desired output voltage as a result of change in load current. In other words, when the load current changes by 1mA, the corresponding change in the regulator output gives the load regulation capability of the LDO. It is defined by equation 2.2 and is measured in terms of mV/mA.

$$LoadRegulation = \frac{\Delta V_{out}}{\Delta I_{load}} \tag{2.2}$$

Transient Response: It is defined as the ability of the regulator to react to no-load to full-load change in the load current while regulating a desired output voltage. It takes several factors into account, like peak overshoots and undershoots, settling time and peak-to-peak ripple.

Current Efficiency: It is defined as the ratio of load current delivered to the total input current (comprising of the quiescent current and load current), as in equation 2.3.

$$\eta = \frac{I_{out}}{(I_{out} + I_Q)} * 100\% \tag{2.3}$$

Figure of Merit (FOM): It is defined as in equation 2.4, as in [1]. The lesser the value, the better regulator it is.

$$FOM = \frac{(C_{load}.\Delta V_{out}.I_Q)}{(I_{load}^2)} \tag{2.4}$$

Chapter 3

Proposed Digital LDO Design

3.1 Digital LDO design

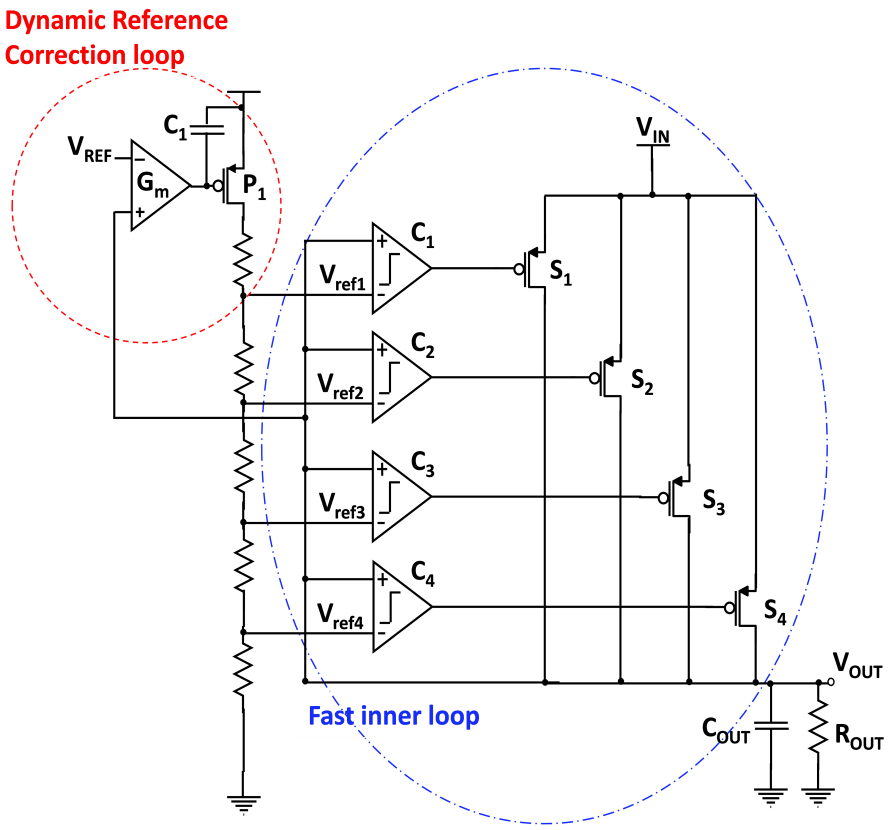

Figure 3.1: Proposed Digital LDO

It has already been established that Analog LDOs suffer from lack of low-voltage operability, and are not scalable. Digital LDOs on the other hand, have a slower transient response, and a poorer DC load regulation capability as compared to an

analog LDO. Therefore, in this work, a 200mA class Digital LDO with dynamic reference correction loop has been proposed to improve the load regulation capability and improve the transient response. The proposed LDO is scalable in terms of the load currents it can drive, which shall be established in the later sections.

As shown in Fig. 3.1, the proposed LDO is made using comparators, a gm-C integrator, pass switches, and a resistor ladder. Comparator stage is used to convert analog output to digital control signals, which control the states of the pass switches. These switches act as a digital-to-analog converter, which change the output voltage to minimize the error between the input and output voltages. The gm-C integrator is used to dynamically shift the references of the flash ADC, to improve the DC load regulation, as explained in subsequent sections.

3.1.1 Comparator

Analog LDOs use an error amplifier in the feedback loop to compare the difference between input and output voltages, and based on this difference vary the on resistance of a pass switch. In digital LDO, however, a comparator is used to sense the difference between the input and output voltages and based on the difference, give output as either digital bit 0 or 1. This digital bit varies the number of turned on pass switches. Fig. 3.2 shows the block diagram of a comparator.

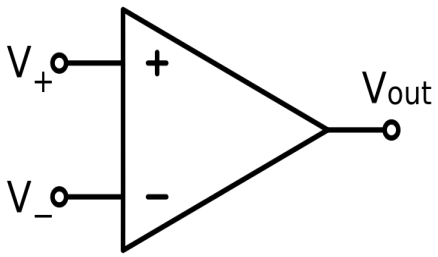

Figure 3.2: Comparator Block Diagram

Faster the response of the comparator, larger is the frequency at which the shift register can receive the control signal, thus making the transient performance better. This makes it absolutely necessary to have a fast comparator in the design. The

traditional comparator designs are made by using an operational amplifier in open-loop configuration. Such comparators are however slow, since the high gain of the op-amp limits its bandwidth, thus reducing their speed. Op-amp based comparators also suffer from a limited resolution governed by the input offset of the op-amp. To offset this limitation of limited resolution and slow speed, comparator operation is divided in two stages- comparison and decision stage, by using a clock signal. The compensation capacitor of the op-amp is disabled during the comparison phase to increase the speed. This however introduces clock-feedthrough effect due to unwanted charge injection when the transistors turn off. A multi-stage comparator can be used to solve this issue of clock-feedthrough. This type of design have a high resolution but require multiple phase clock signals, which slow down the circuits. To increase the speed, latched comparators with first stage as a pre-amplifier and a second track-and-latch stage are used. While the pre-amplifier stage, with a small gain (typically 4-10) improves the resolution, while track-and-latch stage amplifies the output further and makes it rail-to-rail. Such comparators, as shown in fig. 3.3, are very fast and are widely used in the reviewed digital LDO designs.

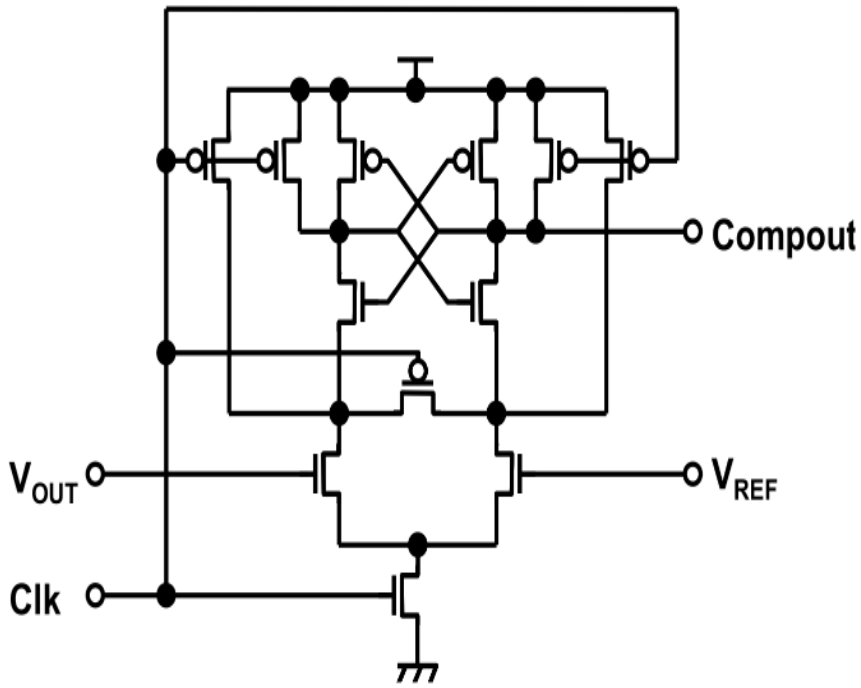

Figure 3.3: Latched Comparator [7]

Synchronous comparators as described above, use clock to switch between track and latch modes in the track-and-latch stage. The faster the clock speed, the better is the comparison speed of these comparators. However, as defined by eq. 2.1, dynamic power dissipation is directly proportional to the clock frequency. Using synchronous comparators would lead to lower power efficiency, which is undesirable. To reduce the dynamic power consumption in our design, we used asynchronous latched comparators. Fig. 3.4 shows the circuit diagram of the asynchronous comparator used in our design.

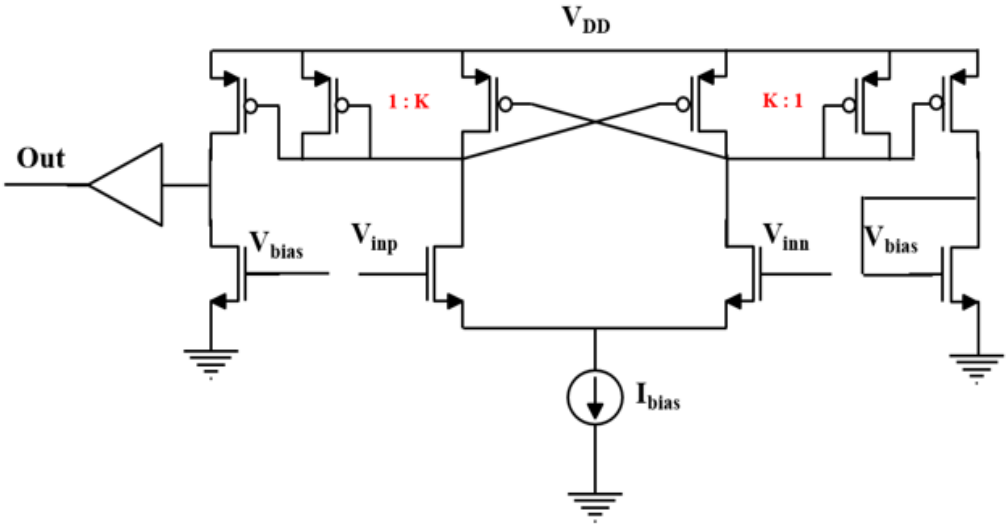

Figure 3.4: Proposed Comparator

In this circuit there are two feedback paths- a negative current series feedback from source nodes of M1 and M4, and another being a positive voltage shunt feedback from the latched connections (from gate to drain) of M2 and M3. If the positive feedback becomes greater than the negative feedback, there would be hysteresis in this circuit. So, to keep this circuit free from hysteresis, ratio of the sizes of M2 and M5 must be less than 1. Using K<1 in the circuit in fig. 3.4, we ensure a partial positive feedback, providing us with high gain of the comparator. Owing to its high gain, we obtain a high resolution, capable of detecting voltage differences of the order of μVolts. This circuit operates at a bias current of 10μA, and making it highly power efficient and giving comparison speeds of the order of 2GHz. The propagation delay of this comparator circuit is 450ps at typical operating conditions.

3.1.2 Pass Switch

Typically, pass switch in an analog LDO is modelled as a gm stage with a load resistance and load capacitance at its output. This is because the current through this switch is a function of its gate to source voltage, and the gate voltage depends on the difference of reference voltage and the output voltage. This generates a RC pole at the output. In digital LDO, however, this pass switch can be simply characterized as a Ron resistance since at any point of time, it is only acting as a binary switch, either on or off. The current through this switch is either zero or it is the current flowing through the source of this branch. It is in no way defined or controlled by this switch.

3.1.3 Dynamic Reference shifting controller

In conventional digital LDOs, it is observed that with the variation in the load current, output voltage settles at different DC voltage levels. This degrades the DC load regulation capability of the regulator. This level shift arises because for different values of load currents, a different number of pass switches are turned on, each of which corresponds to a different voltage level. At a higher load current, the output voltage DC level is lesser than the output voltage DC level at a lower load current.

Dynamic reference shifting controller is proposed in this work to cancel this DC shift on load current variation. It works as a $g_m - C$ integrator, which pumps in extra current when the DC level of the output voltage falls, therefore making the voltages across each of the resistors to increase. Similarly, when the output voltage DC level rises, it reduces the amount of current flowing into the ladder, thus reducing the voltage levels across each of the resistors. This controller forms a low-bandwidth, high gain loop which reduces the output voltage error, leading to better DC load regulation capability.

As shown in fig. 3.5, when the output voltage falls lower than the reference voltage, gate voltage of PMOS transistor goes down, as a result Vgs increases, thus increasing the amount of current flowing through PMOS transistor into the resistor ladder increases. This shifts up the internal references (Vref1 - Vref4) feeding the comparator reference voltages. Since the comparison thresholds go up, the output voltage also goes up.

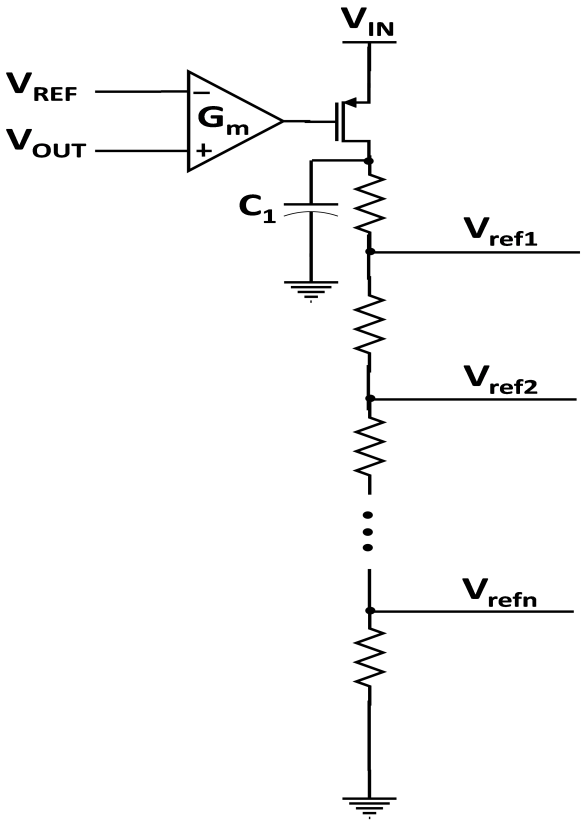

Figure 3.5: Dynamic Reference Shifting Controller

3.2 Scalability

This design can be easily modified to drive larger or smaller load currents by increasing or decreasing the size of the pass switch respectively. Reducing the size of the pass switch leads to a lower capacitance at the output, thereby reducing the response time of the comparator. As a result, output ripples reduce. This enables us to use smaller capacitance at the output. Thus, similar level of performance can be ascertained by reducing the load capacitance for a smaller amount of load current, and vice versa. For regulating a constant voltage V (given by equation 3.1), V is constant as long as the ratio $(I.\Delta t)/C$ is constant. For an increased load current, we can increase load capacitance to keep similar performance and for smaller load current, we can reduce load capacitance to keep similar performance.

$$V = \frac{I.\Delta t}{C_{load}} \tag{3.1}$$

3.3 Small signal model

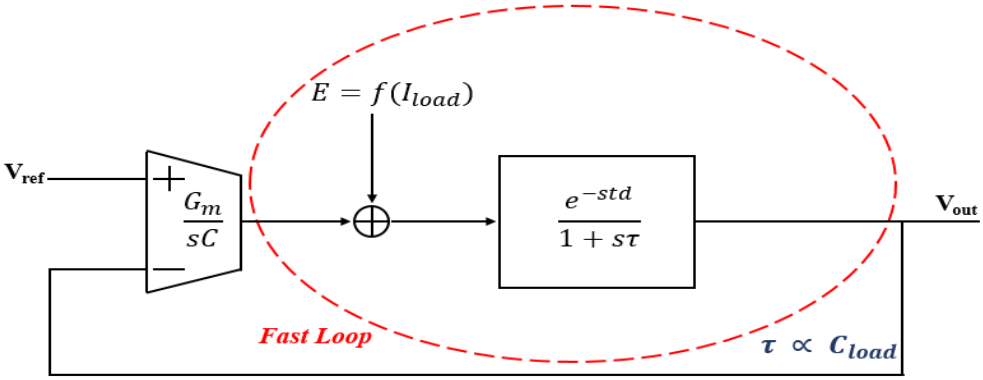

Figure 3.6: Small Signal Model

The small signal model is realized as shown in fig. 3.6. The dynamic reference shifting controller is modelled as a $g_m - C$ integrator, which forms a slow loop due to its large loop gain and small bandwidth. This slow outer loop introduces a pole in the system. Comparator stage is realized as a delay element with a large non-linear gain k. Pass switch stage is realized as a single-pole system with the pole at $1/\tau$, where τ is defined as in equation 3.2.

$$\tau = (R_{on}||R_{load}).C_{load} \tag{3.2}$$

The fast inner loop (flash), although suffers from stable limit cycle oscillations, it is stable in itself. The limit cycles oscillations arise due to the non-linear transfer function of the comparators. The transfer function of the system is given by equation 3.4, where k_1 is given by equation 3.5.

$$V_{out} = [V_{out} - \frac{g_m}{sC_1}.(V_{ref} - V_{out})].e^{-sT_d}.\frac{k_{out}}{1 + \frac{sR_{eq}C_L}{2\pi}} \tag{3.3}$$

$$\frac{V_{out}}{V_{ref}} = \frac{-2\pi g_m k_1}{s^2 R_{eq} C_1 C_L + sC_1(1-k_1)2\pi - 2\pi k_1 g_m} \tag{3.4}$$

$$k_1 = e^{-sT_d}.k_{out} \tag{3.5}$$

Stability of the system in figure 3.6 is ensured by making the bandwidth of the outer loop low. The error, E is a function of load current drawn, and is defined by equation 3.6. Here, I_{unit} is the maximum current that can pass through each ON pass switch at any point of time, and V_{LSB} is the minimum reference voltage of any comparator.

$$E \propto \frac{I_{load}}{I_{unit}}.V_{LSB} \tag{3.6}$$

Chapter 4

Power Delivery Network(PDN)

4.1 Power Delivery Network Analysis

For any circuit design implemented on silicon, there exists a requirement of packaging to ease its integration with devices. On-chip connections pass from the internal pins to the pins of the package through metal interconnects, which introduce non-idealities in the design and may cause some issues with the functioning of the chip. These non-idealities occur in the form of a combination of parasitic resistances, capacitances and inductances, which is usually modelled as in fig. 4.1. This network is termed as a power delivery network (PDN).

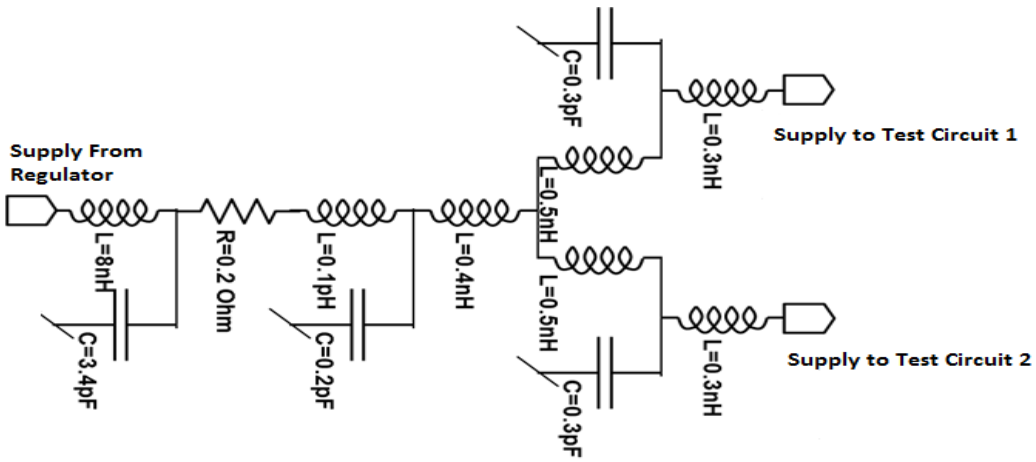

Figure 4.1: PDN Model

The important consideration for the designers of any circuit block that goes on chip is to ensure a smooth and stable supply through each of the pins to the chip. This makes it extremely necessary for the designers to test the functioning of their design

with a model of PDN expected to be present post fabrication. The noise due to PDN mainly comes from three sources:

1. IR Drop: The total resistance from the external supply to the chip pins comes from the resistance of the on-chip wires, resistance of solder bumps, resistance of package connections and the resistance of PCB plane. This resistance causes a drop in the voltage delivered to the chip, depending on the current flowing through it. There is an always flowing quiescent current in the chip, which contributes to the static component of IR drop. However, there is an additional flow of current due to switching of devices on-chip, which leads to the dynamic component of the IR drop.

2. Ldi/dt Noise: The parasitic model of a PDN in fig. 9 shows the inductance introduced in the system. This inductance leads to a voltage change at every instantaneous change in the current. This introduces a switching noise in the voltage levels, which may disturb the normal functioning of the circuit.

3. LC resonance: The capacitances introduced in the design cause LC oscillations at low frequencies, causing a noise. This noise is not filtered by the decoupling capacitances since it is low-frequency. This can be offset by having a large inductance in series with the PDN, but that would lead to a greater Ldi/dt noise. So, there exists a trade-off between Ldi/dt noise and the LC resonant noise.
   Due to these reasons, we decided to test our design of Digital LDO with the model of PDN supplying at both the supplies VDD and GND of a test circuit block. For this, the PDN model was used and a simple ring oscillator was designed to be used as test circuit.

4.1.1 Transient Analysis

The circuit was connected with a simplified model of PDN as shown in fig. 4.2, and transient analysis was performed to obtain the response of the circuit.

This is a rather slow simulation since it takes a long time of around 40 minutes to finish this simulation only at the typical corner at 27°C operating temperature. This time would be quite large for larger circuits with a lot of switching activity involved, e.g. Analog-to-Digital converter.

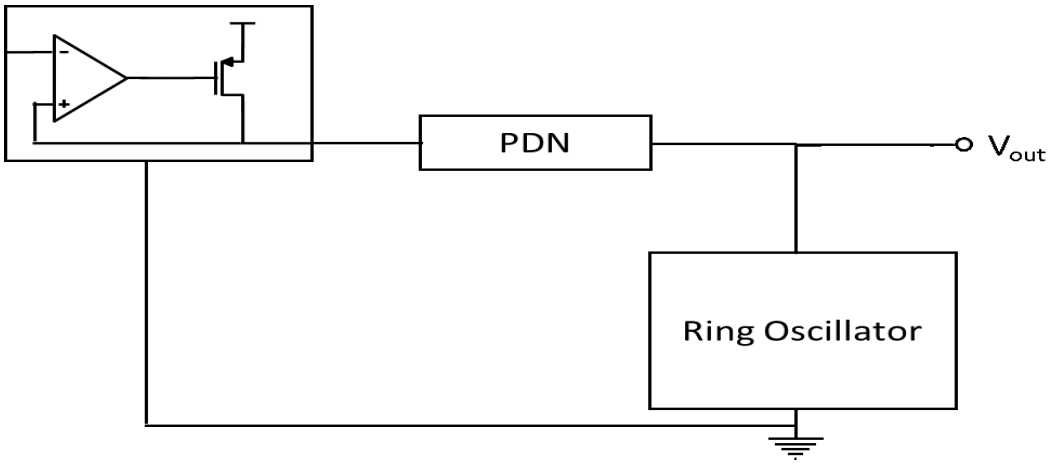

Figure 4.2: Transient setup with ring oscillator fed from LDO

4.1.2 S-parameter Analysis

For this analysis, first the S-parameters of the test circuit are extracted and then this S-parameter model of the test circuit is used in place of the actual test circuit. Transient analysis is then performed on this model, as shown in fig. 4.3.

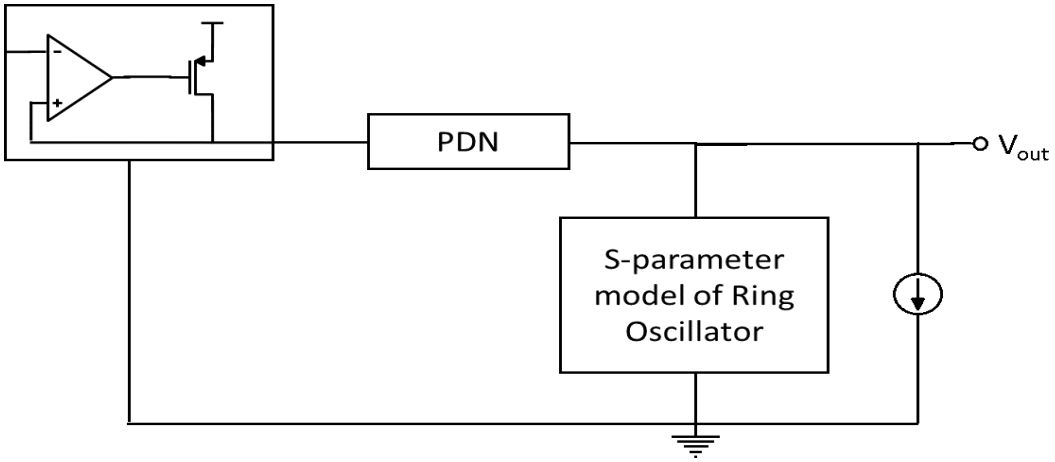

Figure 4.3: S-parameter analysis setup

This simulation is faster since it eliminates the actual model with a mathematical, S-parameter model, a lot of approximations are done, which reduce the amount of calculations on the part of the simulator, thus giving results faster. This simulation takes about 1 minute to simulate.

4.1.3 AC Analysis

Here, we make use of the fact that output impedance is a figure of merit (FOM) of any voltage source, and it can therefore be used to define a LDO as well [9]. The first step for this analysis is to find the output impedance of the LDO in the frequency domain. This is done by simulating the LDO in AC analysis. Next, we simulate the test circuit block in transient mode and obtain its input current profile. This becomes the load current profile in time domain for our analysis, since the input current of the test circuit is the load current for the LDO. This current profile is converted to frequency domain by taking fast Fourier transform (FFT) as in equation 4.1.

$$I(f) = fft\{i(t)\} \tag{4.1}$$

Switching noise at the output of the LDO is calculated by performing complex multiplication of output impedance of the regulator and the current in frequency domain, as given by equation 4.2.

$$\Delta V_{out}(f) = I_{load} * Z_{out} \tag{4.2}$$

The noise in time domain can be obtained by taking the inverse fast Fourier transform of this $\Delta V_{out}(f)$ [10]. This gives the switching noise profile at the output of the LDO. This analysis is very fast since it involves only mathematical equations to be solved rather than the simulation of actual circuits. This simulation gives the output in less than 20 seconds.

4.2 Ring Oscillator

A ring oscillator was designed as the test circuit for the purpose of testing our regulator with a PDN. Ring oscillator is a cascading of an odd number of inverters in series thus forming a ring, as shown in fig. 4.4. The output of the ring oscillator oscillates between the rail-to-rail supply levels. The resistors and capacitors are introduced between the stages to increase the delay between the two stages, thereby increasing the time period of oscillations. Such ring oscillators are found in a wide range of applications, including in voltage controlled oscillators (VCOs) etc.

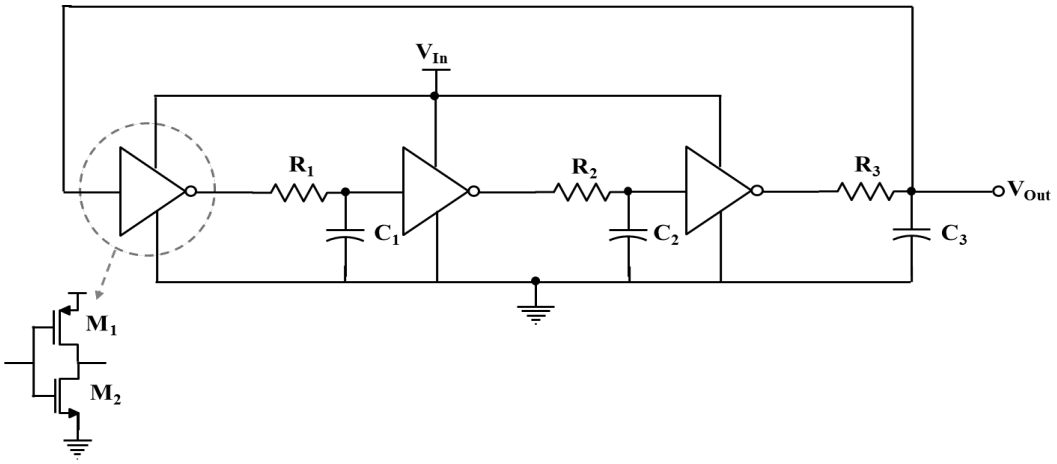

Figure 4.4: Ring Oscillator

The supplies of a ring oscillator are very critical, since they not only determine the voltages between which the output would oscillate but also determine the frequency of this oscillation. The delay of the inverter is a function of the current flowing through it. This means that if the VDD supply of the inverter is more, more current would flow through the PMOS M1 into the output of this inverter. This increases the rate of charging of the capacitor, thus reducing the delay between two inverter stages. This in turn, leads to a reduced time period of oscillations. For a ring oscillator with n inverter stages, and t delay between the two inverter stages, frequency of oscillation f is given by equation 4.3.

$$f = \frac{1}{2 * t * n} \tag{4.3}$$

Chapter 5

Simulation Results

The full custom design was implemented in STMicroelectronics 28nm FD-SOI process using the Cadence Virtuoso schematic editor. Further, layout of the design was done using Cadence Virtuoso layout editor. For pre-layout simulations, netlist was generated using ADE-L, and simulations were done using Mentor Graphics ELDO simulator at high precision accuracy (EPS = E-9). Post-layout (PLS) netlist was also extracted and PLS simulations were done using ELDO simulator. All the results of digital LDO presented in this section are from PLS simulations, while for the PDN, results are from pre-layout simulations. PDN simulations were not done with post-layout netlist since it is just an approximate model, and actual R, L, C values may vary after fabrication. Fig. 5.1 shows the layout of the digital LDO design. The total area occupied by digital LDO is $0.027mm^2$.

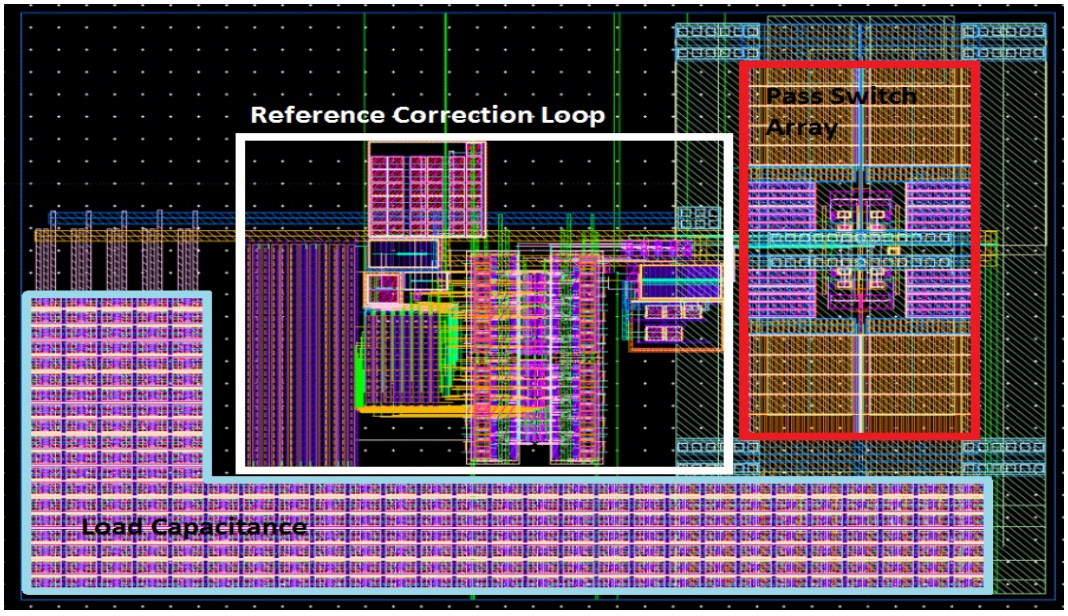

Figure 5.1: Layout of digital LDO design with on-chip load capacitor

5.1 Digital LDO Results

Fig. 5.2 shows the regulated output voltage using the designed LDO without the dynamic reference correction loop. It shows a 50mV DC level shift in the output voltage when load current is varied from no load to full load of 200mA.

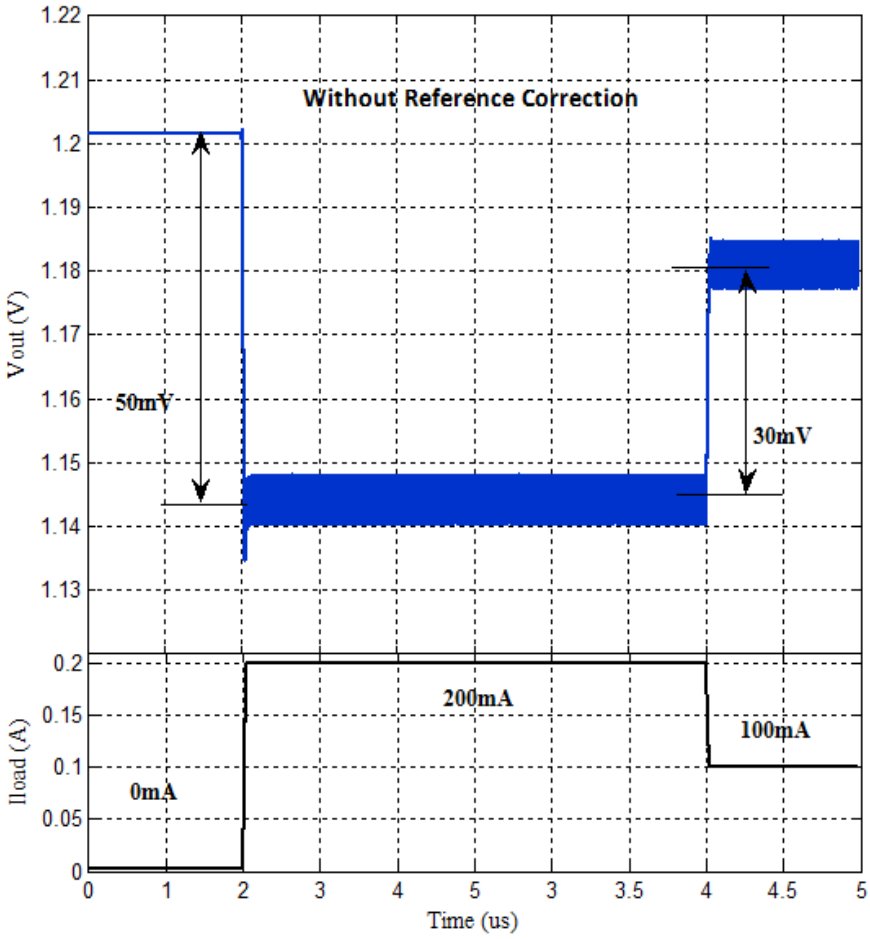

Figure 5.2: Regulated output voltage without dynamic reference shifting controller

Fig. 5.3 shows the shifting of the internal reference voltages on load change from no load (0A) to full load (200mA) and then to 100mA and finally to 50mA. It is evident from this figure that when load current increases, since output voltage falls, the outer reference correction loop shifts the internal references of the comparators up to compensate the DC shift. Similarly, when the load current falls from 200mA to 100mA, the internal references are shifted down to compensate the DC shift upwards in the output voltage.

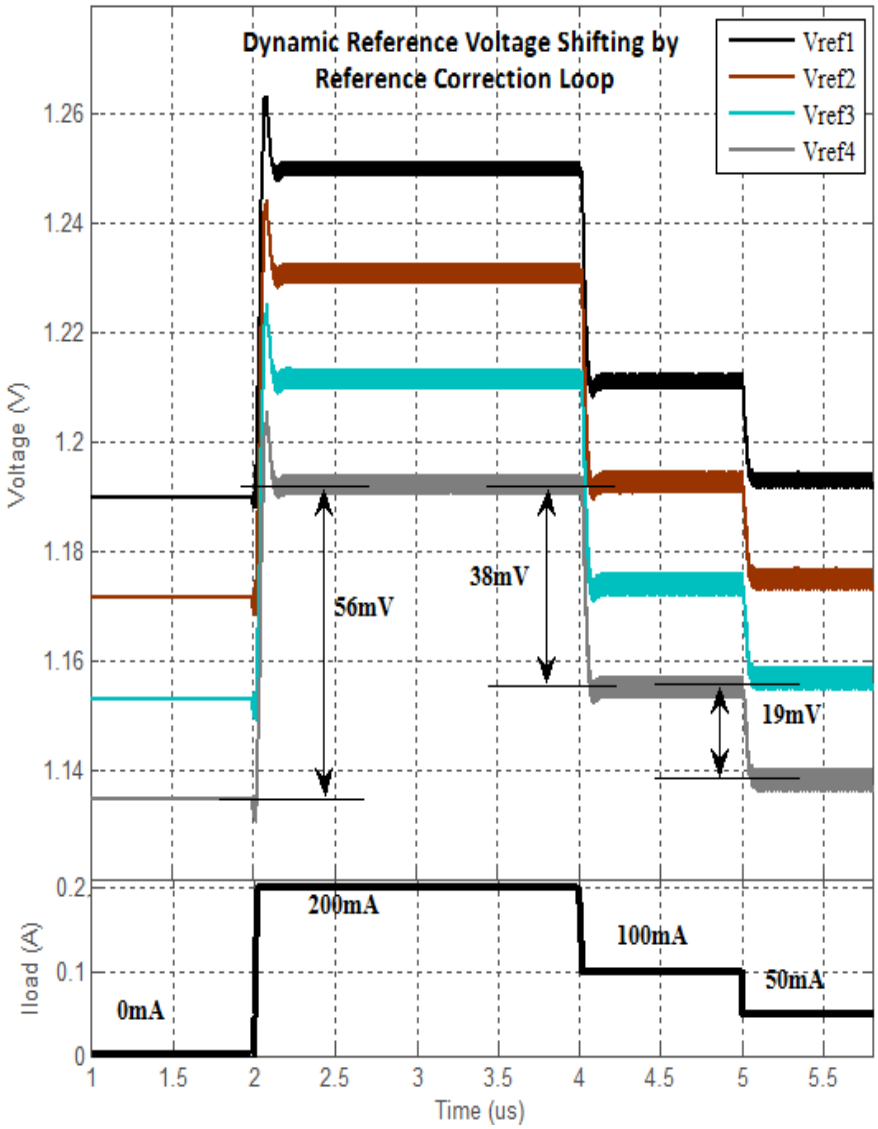

Figure 5.3: Shifting of internal reference voltages

It is observed from Fig. 5.3 that the internal references are shifted due to load variation. This shifting leads to compensation in DC shifting as well. Fig. 5.4 shows the regulated output voltage with the dynamic reference shifting controller working. It is evident that there is no DC level shift in this case.

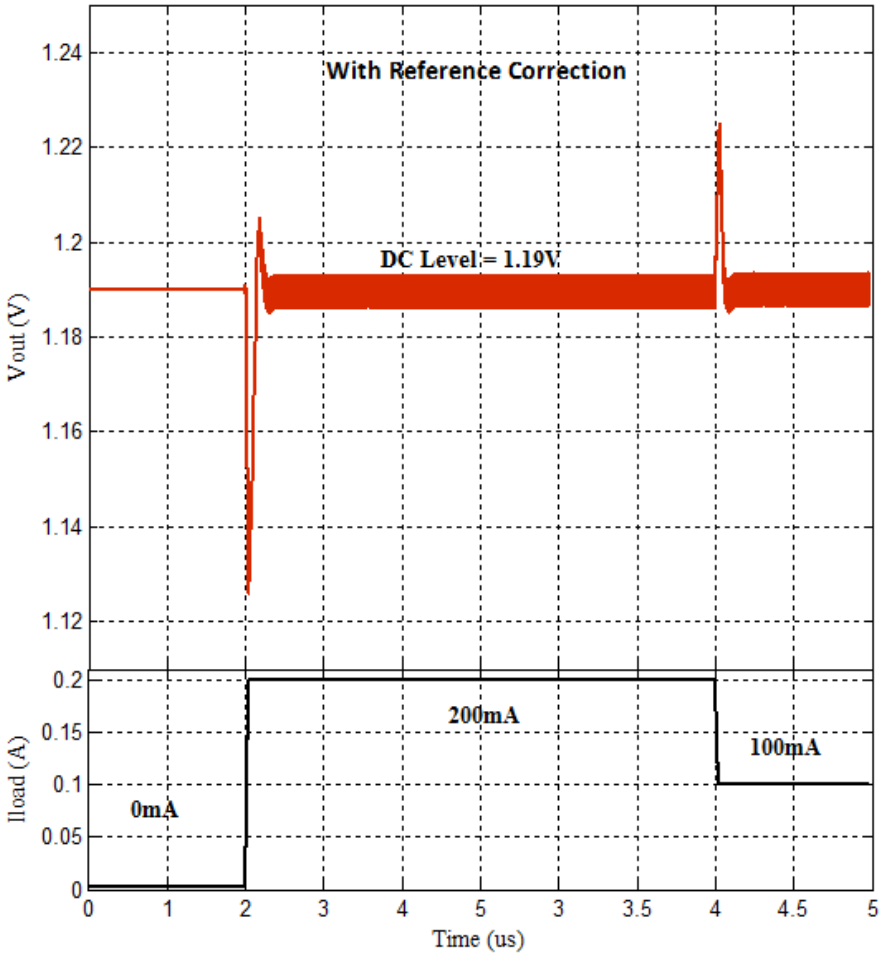

Figure 5.4: Regulated output voltage with dynamic reference shifting

Fig. 5.5 shows the transient response of the LDO with peak-to-peak ripples of 7.8mV, a maximum overshoot/undershoot of 64mV and a worst case settling time of 139ns for no load to full load variations.

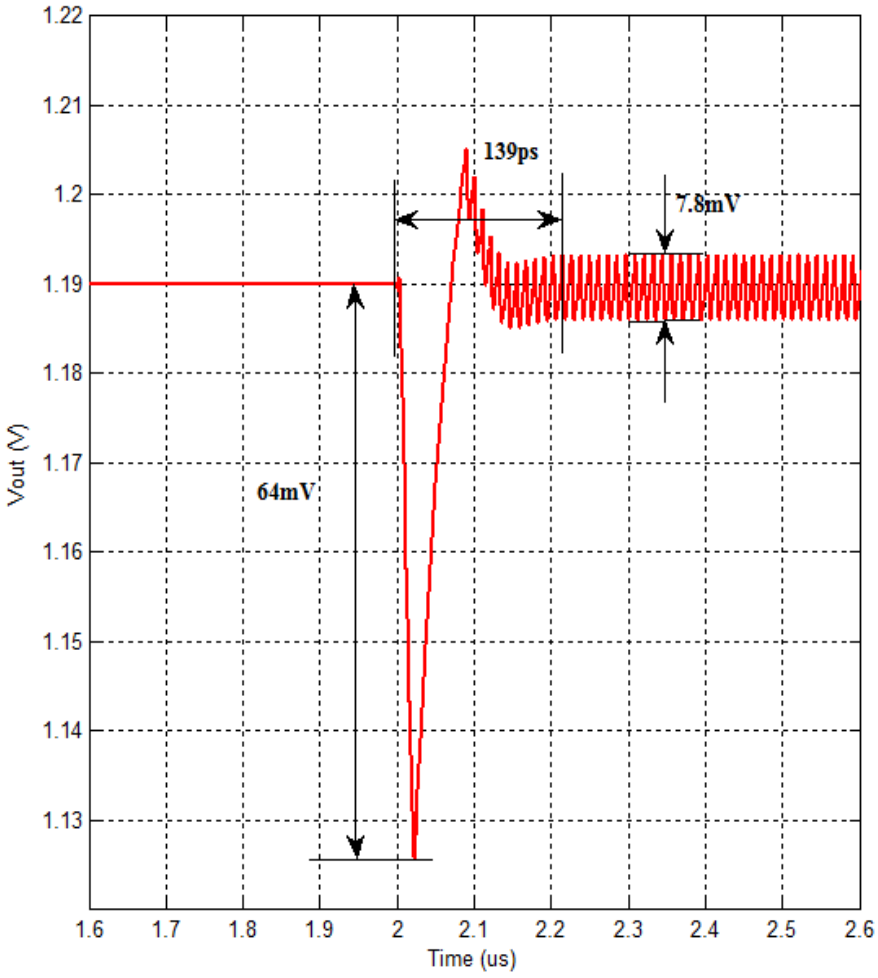

Figure 5.5: Transient performance of the designed Digital LDO

Scalability

We compared the performance of the presented design for various load currents, i.e. 2mA, 4mA, 20mA, 40mA, 100mA and 200mA. The performance comparison results are displayed in Table 5.1.

Table 5.1: Performance Comparison at Varying Load Capacitance And Currents

C_{load} (nF)	0.1		1		5	
I_{load} (mA)	2	4	20	40	100	200
ΔV_{out} (mV)	30.8	43	23.6	42.6	35.9	64
$T_{settling}$ (ns)	91	135	75	115	98	139

5.2 PDN Noise Analysis

Fig. 5.6 shows the output waveform obtained from S-parameter analysis match the one obtained from transient analysis. V(P3) is the output obtained from transient simulations using S-parameter analysis, while V(VDDS) shows the output obtained from full system transient analysis. The waveform wf(6) gives the error between the noise profile obtained using full-system transient analysis and the transient analysis using S-parameters. Even though there is a phase shift of 180 degrees, but the magnitude of output variation is similar in both the cases, validating our theory.

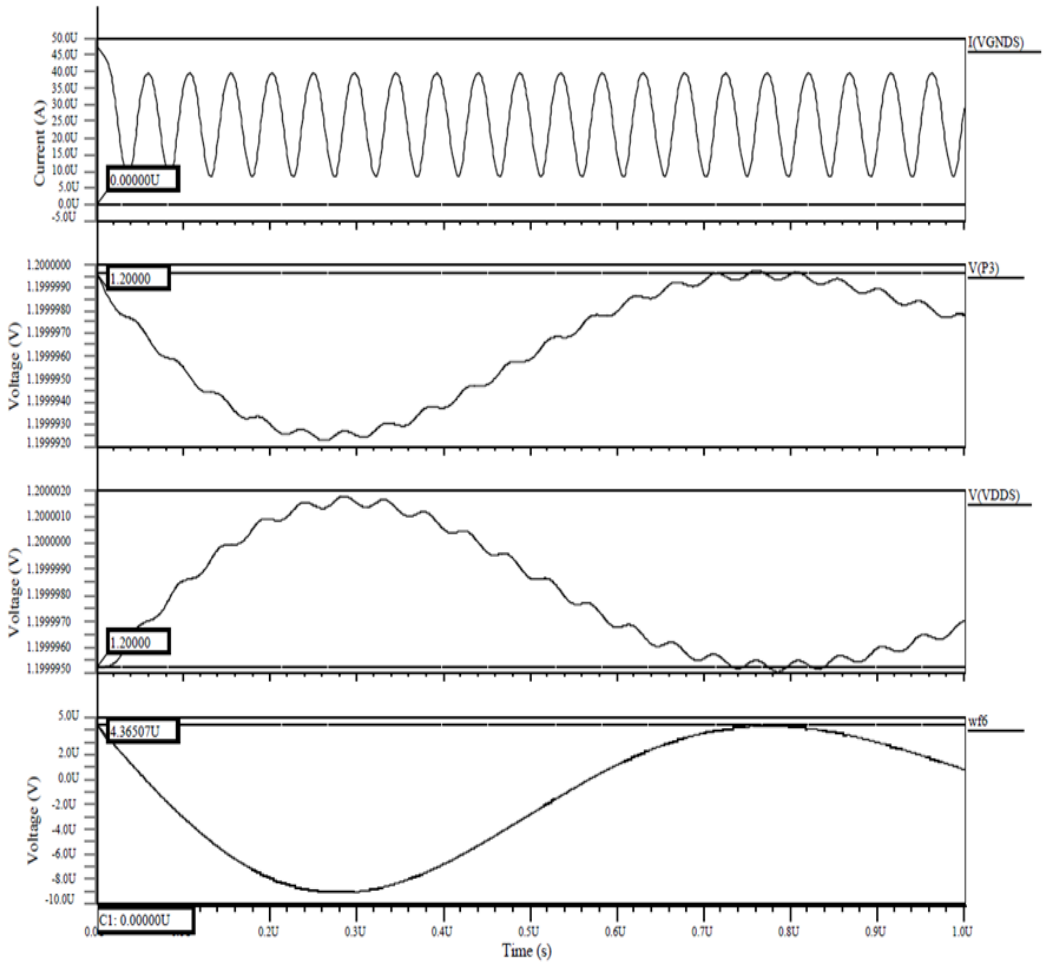

Figure 5.6: Transient simulations using S-parameters and using full-system simulations

Fig. 5.7 shows the output impedance characteristics of LDO along with the current and reconstructed output signal in frequency domain. Fig. 5.8 shows the reconstructed output waveform using the AC analysis method, in time domain. It can be

clearly seen that the noise profile is matching with the transient output. The peak-to-peak variation is nearly similar. The reconstructed waveform is limited in time due to the calculative limitations of the Ezwave waveform viewer which has been used for calculating and displaying the results.

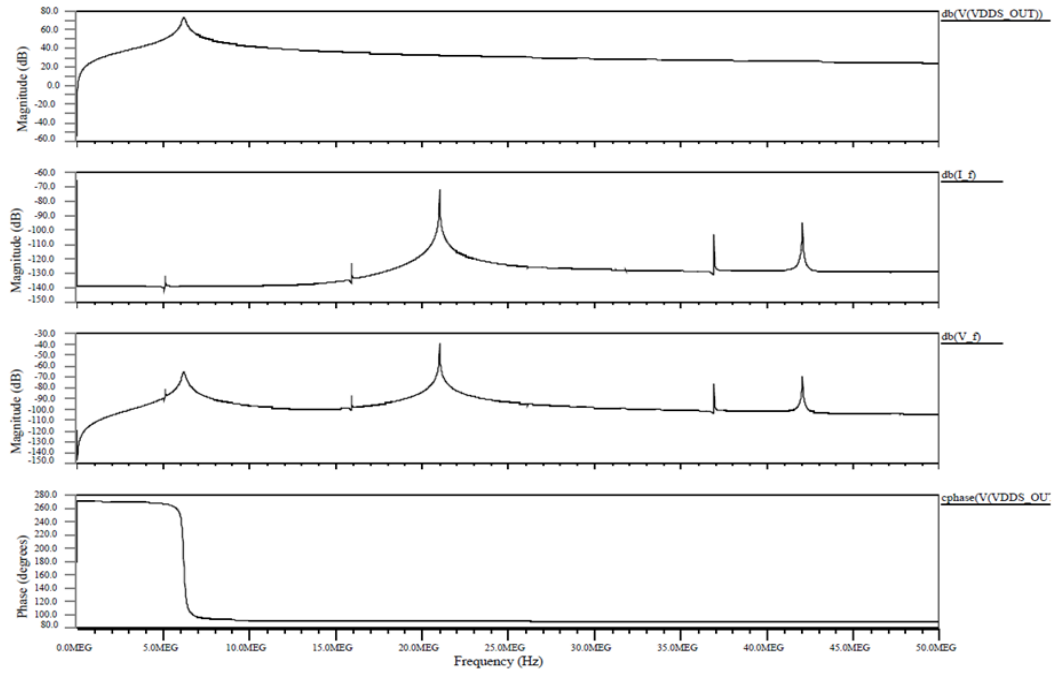

Figure 5.7: Output Noise profile in frequency domain

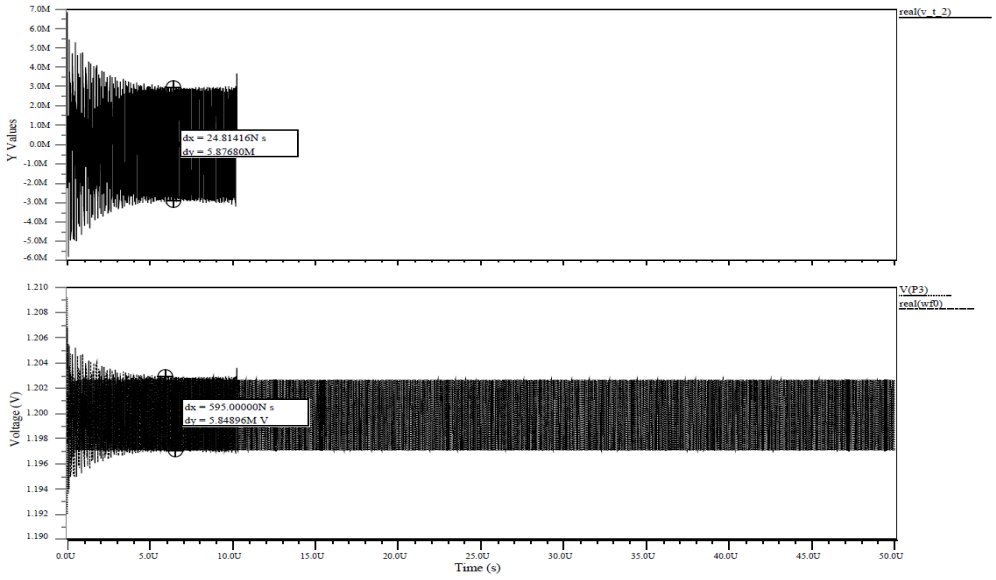

Figure 5.8: Output noise profile in the time domain

Chapter 6

Future Work

The design has been fully verified using post-layout netlist with extracted R and C, and the device has been sent for fabrication at STMicroelectronics fabrication lab. The post-silicon validation needs to be done on the manufactured device to test its functioning in practical operating scenarios.

As mentioned in chapter 1, we have used an asynchronous comparator in our design to reduce the dynamic power dissipation occurring due to switching of clock. This requires our design to have a larger quiescent current of $75\mu A$, which is quite large for the IoT applications. Also, there is a large offset present due to the minimal sizing of the transistors in the comparator. There is no easily implementable way to cancel this offset. For this, right now, we have gone for off-chip trimming, which needs to be done away with. Due to these reasons, using synchronous comparators needs to be tested. It is widely known that offset cancellation can be easily done in synchronous comparators, and they consume lesser static current as compared to asynchronous comparators. So, there might be a possibility that using synchronous comparators we can improve the current efficiency of our LDO without compromising much on dynamic power consumption.

Chapter 7

Conclusion

In this work, a fully on-chip, 200mA class digital low-dropout voltage regulator has been designed and implemented in STMicroelectronics 28nm FD-SOI process using a small on-chip load capacitance of 5nF. This design is highly scalable in terms of the load current it can support, and can be easily modified to drive larger or smaller load currents. The designed LDO has a superior DC load regulation capability due to the novel dynamic reference correction loop introduced, which shifts the internal references of the ADC up or down depending on the DC shift in the output voltage. The design also has a fast transient response time of 139ns for a full 200mA load current variation due to its Flash ADC based structure as opposed to SAR ADC based structure used in conventional digital LDO designs.

The power delivery network has also been modelled and an effective way to analyze the circuit behavior faster using S-parameters of the circuit block and the output impedance of the regulator has also been demonstrated in this work. This would help circuit designers to speed up the simulation process to effectively model the noise performance of their designs.

The total quiescent current consumption of this design is $75\mu A$ with all its peripheral circuitry involved. The maximum peak-to-peak ripple of 7.8mV is observed. This design gives a load regulation capability of 0.005mV/mA, which is better than almost all of the designs compared. The total active area of the design is $0.027mm^2$. The proposed design is able to regulate a reference voltage of 1.2V using a supply of 1.25V, giving a dropout of 50mV. We calculate the FOM of our design using the formula in equation 2.4, which is found out to be 0.61ps which is better than almost all of the previous designs despite having a larger quiescent current consumption. We achieve a maximum current efficiency of 99.96%, which is one of the best in this class

of digital LDOs surveyed. We finally compare the results of post-layout simulations of our design with other digital LDO designs in Table 7.1.

Table 7.1: Comparison with state-of-the-art Digital LDOs

Paper	**[7]**	**[4]**	**[6]**	**[8]**	**[2]**	**[5]**	**[3]**	**This Work**	
Process	65nm	65nm	130nm	65nm	65nm	28nm	65nm	28nm FD-SOI	
V_{in} (V)	0.5	0.5	0.5-1.2	0.5-1	0.5-1	1.1	0.6-1.1	0.9-1.3	
V_{out} (V)	0.45	0.45	0.45-1.14	0.3-0.45	0.45-0.95	0.9	0.4-1.0	0.85-1.2	
I_Q (A)	2.7	14	24-221	14	3.2	110	82	75	
I_{load} (mA)	0.2	0.4	0.5-2	2	10	180	2-100	4	200
C_{load} (nF)	100	0.4	1	0.4	0.1	23.5	1	0.1	5
ΔV_{out} (mV)	90	40	<40	40**	105	120	55	43	64
Load Regulation (mV/mA)	0.65	NA	<10	<5.6	NA	NA	0.06	0.005	0.005
FOM* (ps) [1]	NA	1400	240	199	0.336	9.57	0.43	20.1	0.61
Current Efficiency (%)	98.7	96.3	98.3	99.8	NA	99.94	99.92	99.96	99.96

*$FOM = \frac{C_{load}\Delta V_{out} I_Q}{I_{load}^2}$

**Authors have mentioned it only for a 1.06mA current variation while claiming the circuit operability at 2mA, i.e., 40mV@1.06mA

Appendix A

Research Impact

Patent:

1. Process has been initiated for the filing of the US Patent on this work titled, "Digital LDO with Analog-Assisted Dynamic Reference Correction for Fast and Accurate Load Regulation".

Publications:

1. Paper titled, "Digital LDO with Analog-Assisted Dynamic Reference Correction for Fast and Accurate Load Regulation" has been accepted at the 60th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) for poster presentation to be held in Boston, USA from August 6-9, 2017.

2. Paper titled, "A 200mA Digital LDO with low load capacitance and high current efficiency" was presented in STMicroelectronics India Techweek 2017 (internally archived conference) and was awarded the best paper award in the Analog Track.

References

[1] Peter Hazucha, Tanay Karnik, Bradley A Bloechel, Colleen Parsons, David Finan, and Shekhar Borkar. Area-efficient linear regulator with ultra-fast load regulation. *IEEE Journal of solid-state circuits*, 40(4):933–940, 2005.

[2] Mo Huang, Yan Lu, U Seng-Pan, and Rui P Martins. 20.4 an output-capacitor-free analog-assisted digital low-dropout regulator with tri-loop control. In *Solid-State Circuits Conference (ISSCC), 2017 IEEE International*, pages 342–343. IEEE, 2017.

[3] Mo Huang, Yan Lu, Sai-Weng Sin, U Seng-Pan, and Rui P Martins. A fully integrated digital ldo with coarse–fine-tuning and burst-mode operation. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 63(7):683–687, 2016.

[4] Doyun Kim and Mingoo Seok. 8.2 fully integrated low-drop-out regulator based on event-driven pi control. In *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*, pages 148–149. IEEE, 2016.

[5] Yong-Jin Lee, Wanyuan Qu, Shashank Singh, Dae-Yong Kim, Kwang-Ho Kim, Sang-Ho Kim, Jae-Jin Park, and Gyu-Hyeong Cho. A 200-ma digital low dropout regulator with coarse-fine dual loop in mobile application processor. *IEEE Journal of Solid-State Circuits*, 52(1):64–76, 2017.

[6] Saad Bin Nasir, Samantak Gangopadhyay, and Arijit Raychowdhury. 5.6 a 0.13 μm fully digital low-dropout regulator with adaptive control and reduced dynamic stability for ultra-wide dynamic range. In *Solid-State Circuits Conference-(ISSCC), 2015 IEEE International*, pages 1–3. IEEE, 2015.

[7] Yasuyuki Okuma, Koichi Ishida, Yoshikatsu Ryu, Xin Zhang, Po-Hung Chen, Kazunori Watanabe, Makoto Takamiya, and Takayasu Sakurai. 0.5-v input digital ldo with 98.7% current efficiency and 2.7-μa quiescent current in 65nm cmos. In *Custom Integrated Circuits Conference (CICC), 2010 IEEE*, pages 1–4. IEEE, 2010.

[8] Loai G Salem, Julian Warchall, and Patrick P Mercier. 20.3 a 100na-to-2ma successive-approximation digital ldo with pd compensation and sub-lsb duty control achieving a 15.1 ns response time at 0.5 v. In *Solid-State Circuits Conference (ISSCC), 2017 IEEE International*, pages 340–341. IEEE, 2017.

[9] Saurabh Kumar Singh and Nitin Bansal. Any capacitor stable lvr using sub-unity gain positive feedback loop in 65nm cmos. In *VLSI Design (VLSID), 2015 28th International Conference on*, pages 260–264. IEEE, 2015.

[10] Shiyou Zhao, Kaushik Roy, and Cheng Kok Koh. Frequency domain analysis of switching noise on power supply network. In *Proceedings of the 2000 IEEE/ACM International Conference on Computer-aided Design*, ICCAD '00, pages 487–492, Piscataway, NJ, USA, 2000. IEEE Press.