TIME TO DIGITAL CONVERTER FOR ALL DIGITAL PLL IN 65 nm CMOS TECHNOLOGY

by

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Certificate

This is to certify that the thesis titled "Time to Digital Converter for all digital PLL in 65 nm CMOS technology" being submitted by Vipra Shukla to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology,is an original research work carried out by her under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree or diploma

July 9, 2017

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Abstract

A new vernier delay line time to digital converter(TDC) architecture using a tristate buffer is proposed in my thesis work. The design being implemented in this thesis work is a single stage vernier delay line time to digital converter. The single stage tristate buffer TDC has very less power consumption,no metastability issues and a very high resolution of 4 ps. This technique enables the power and resolution efficiently. Time to Digital converter has been implemented in a standard 65 nm CMOS process. Single stage time to digital converter has a resolution of 4 ps with power consumption of 72.3 µW.

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Abbreviations

TDC	**T**ime **T**o **D**igital **C**onverter
PLL	**P**hase **L**ocked **L**oop
DCO	**D**igital **C**ontrol **L**oop
PFD	**P**hase **F**requency **D**etector
VCO	**V**oltage **C**ontrol **L**oop
ADC	**A**nalog **T**o **D**igital **C**onverter
GRO	**G**ated **R**ing **O**scillator
ADPLL	**A**ll **D**igital **P**hase **L**ocked **L**oop

Dedicated to my parents

Chapter 1

Introduction

Time to digital converters are not just the Phase detectors but are useful for have wider field of application such as time interval measurements, high-energy physics, laser range finders and test instrumentation[1,8].Now,TDCs are used as frequency synthesis unit in Digital PLL.Scaling difficulties of analog and mixed-signal circuits based on a signal representation in the voltage domain is a problem for nanometer CMOS technologies.Due to this we can easily represent the signal in time domain.New CMOS technology scaling has always been easy to work with digital circuits over the analog circuits.On the contrary, analog circuit design is facing increasing challenges to maintain the same gain, linearity, noise performance with the reduced voltage values and manufacture geometry.As a result, many analog circuit topologies are evolving to utilize more digital circuits in order to overcome the analog issues. One good example is the phase locked loop (PLL), which has recently been attracted the designers attention towards digital architecture of PLL for wireless applications. In the digital PLL design the phase detector has been replaced by TDC as compare to conventional analog charge-pump based PLL .By replacing the phase detector with a TDC, the charge pump and the analog loop filters can be replaced

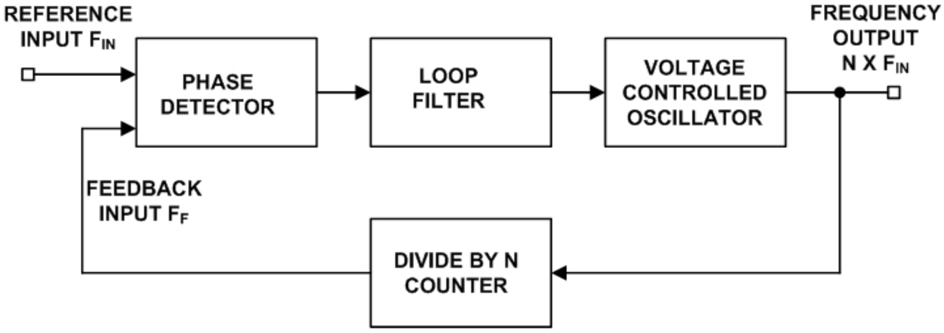


Figure 1.1: PLL block diagram

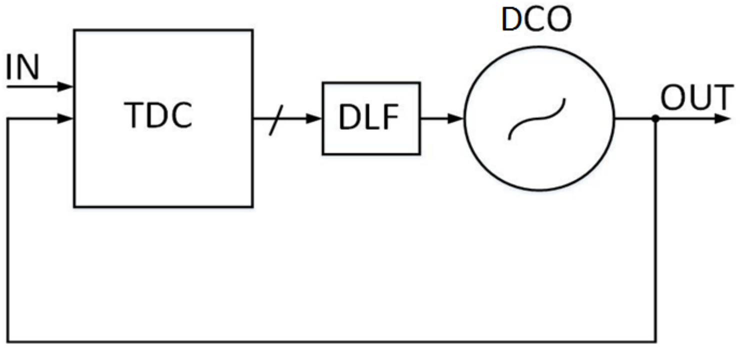


Figure 1.2: All Digital PLL block diagram

with digital filters and a digital control loop(DCO) .In analog loop-filter area does not scale with process due to the gate leakage current of thin oxide transistors .To overcome this problem the designers changed the loop filter that requires large and leaky integrating capacitors with a simple digital filter. Digital Time-to-digital converter(TDC) makes the overall architecture more scalable for future CMOS technology.In this chapter the research Scope, research motivation and the thesis outline are presented.

1.1 Research Scope

The first generation TDC (traditional) has two stages in first stage the time information is converted into the analog voltage and then the ADCs are required for analog to digital conversion [2].The block diagram of basic phase locked loop (PLL) and all digital PLL(ADPLL) are shown in Fig-1.1 and Fig-1.2. In traditional TDCs as the resolution of TDCs is limited by the ADC. The real need behind digital TDC is resolution, power and area. In this work we basically focus on digital TDC design.

1.2 Research Motivation

There are several aspect of proposed type of TDC design.With advances in CMOS technologies the Propagation delay of the CMOS gate defining the resolution of a TDC has reached the level of 20 to 30 ps .TDCs are becoming a good replacement of the conventional phase detector and charge pump. The first generation TDC (traditional) has two stages in first stage the time information is converted into the analog voltage and then the ADCs are required for analog to digital conversion [2].A matlab simulink implementation of analog TDCs is shown in Fig-2.1 of Chapter 2 . In traditional TDCs as the resolution of TDCs is limited by the ADC. The real need behind digital TDC is resolution, power and area. In this work we basically focus on digital TDC design. We propose a new vernier TDC architecture enabling resolution, power and area improvements .Now with new CMOS technology the low power and high resolution TDC can be realized .Time-to-digital converters (TDC) basically link with all digital phase locked loops (ADPLL) where a TDC serves as phase detector .Till now TDCs have been used for more than 20 years in the field of particle and high-energy physics, where precise time interval measurement is required[8].Other applications cover time-of-flight measurement, or measurement and instrumentation applications such as digital scopes and logic analyzers.Currently the micro-electronics community using time-to-digital converters . While the all digital PLL is the first and most famous TDC application while others emerge rapidly. TDC based analog-to-digital converter for instance shows that TDCs are not just phase detectors but useful in a wider field [8].The requirements for any micro-electronics application differ from the applications mentioned above with respect to acceptable price, reproducibility, and suitability for mass production. TDCs suddenly become popular in mainstream micro-electronics as modern VLSI technology is mainly driven by digital circuits. A comparable complexity was not feasible with an analog implementation due to area and power consumption but also due to variability and signal integrity. Flexible means re-configurable, adjustable or even programmable. Data can be stored easily in digital systems without any loss of information. The design of digital circuits is highly automated resulting in high design efficiency and productivity. However, the main advantage of digital signal processing is the inherent robustness of digital signals against any disturbances, i.e. noise and coupling, as well as the inherent robustness of digital circuits against process variations. It is true that these are critical issues especially for large chips fabricated in ultra deep sub-micron technologies. But compared to analog digital solutions are still by far more robust. As a consequence of all these advantages most digital signal processing systems are realized according to the generic structure. A small mixed-signal shell provides the interface between the digital core and the analog environment. While the mixed-signal interface is mainly responsible for the data conversion, the actual signal processing task is performed in the digital domain. In the input path some basic analog signal conditioning, e.g. coarse filters, amplifiers and mixers are followed by a sampler and a quantizer, i.e. an ADC. The sampler evaluates the input signal at discrete time instances and the quantizer maps the resulting continuous values to discrete ones. Both together result in a digital signal representation. In the output path the digital values provided by the signal processing core at discrete time instances are converted in voltages or currents and held constant until the next value occurs. The digital time to digital converters can be proved to be best in the following field

- Improvement with technology

- Lower chip area
- Lower power consumption
- Reconfigurability

1.3 Thesis Outline

The objective of this thesis is to present a implementation of an ADPLL. The report is organized in six chapters:
In Chapter 2, some fundamental aspects of TDC is presented in order.The types of TDC i.e. First generation TDC and Digital TDCs
In the Chapter 3, The state of art of Digital TDCs have been described.
In the Chapter 4,We described the new proposed TDC design single stage TDC.It's schematics and working.
In the Chapter 5,Simulation and results has been shown for resolution and power mearurements for new design.
Finally the conclusion and future work is presented in chapter 6.

Chapter 2

Time to Digital converter

On the basis of a generic mixed-signal system the scaling difficulties of analog and mixed-signal circuits based on a signal representation in the voltage domain are for nanometer CMOS technologies. Therefore, the advantages of a signal representation in the time domain are emphasized. The primary approach for time-to-digital converters (analog TDCs) is based on a two step approach translating the time interval into a voltage and this voltage into a digital value. Analog impairments and resolution limitations are taken care. Counter based time interval measurement and delay-line based TDCs (digital TDCs) are introduced and analyzed with respect to operating principle, basic implementation issues, and quantization error, i.e. resolution. In the ADPLL, the time to digital converter (TDC) serves as the phase frequency detector (PFD) meanwhile the digitally controlled Oscillator (DCO) replaces the VCO. The core module is DCO which avoids analog tuning voltage controls. The DCO is similar to a flip flop whose internal structure is analog. Compared to the analog PLL, the loop filter can be implemented in a fully digital fashion which will save a large amount of area and maintain low power consumption. The minimum power consumption of time and voltage-domain Flash ADCs structures for three different technology nodes is compared and plotted in Figure 2.1 for 10MHz frequency. This sampling frequency is chosen so that the time domain flash ADC can be implemented in all three CMOS technology nodes[10]. In other words, it should be low enough to be design in 350 nm CMOS.The voltage-domain flash ADC has lower power consumption in the conventional flash architecture resolution range (i.e, below 9 bits). When we move to 90nm CMOS technology, the power of voltage-domain flash ADC becomes larger than the power of time-domain flash ADC at approximately 8.5 bits of resolution. Moving to 45nm CMOS, this crossover happens at a lower resolution, around 7.5 bit. This comparison suggests that, in theory, time-based architectures are more efficient in advanced technologies with smaller gate lengths. This conclusion, can

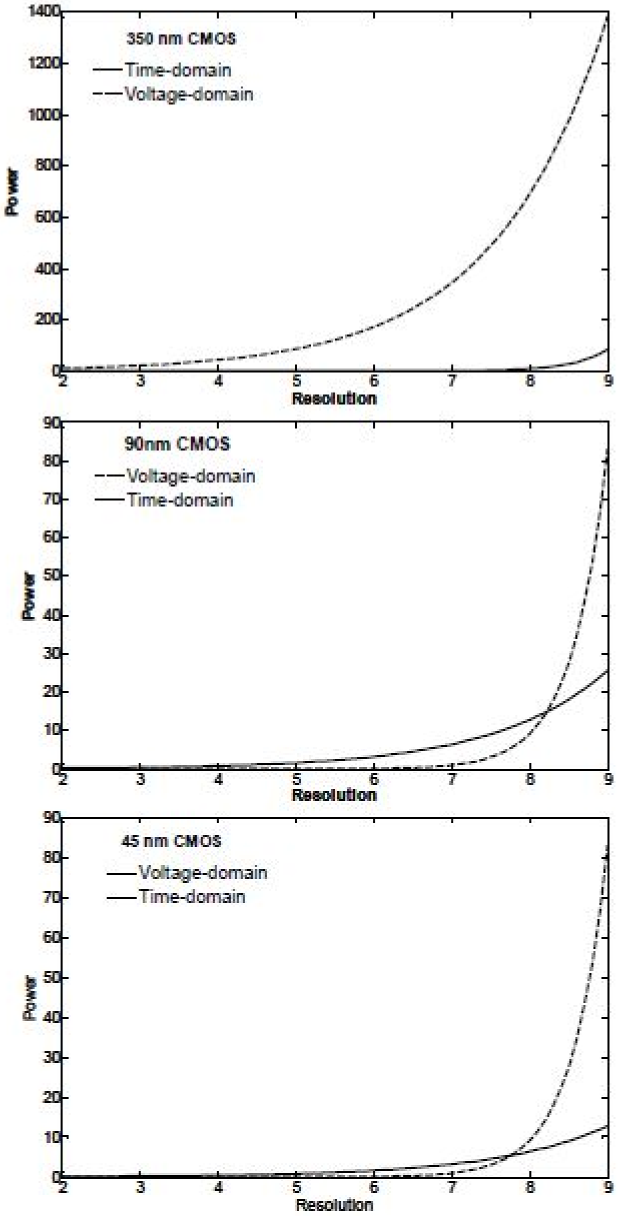


Figure 2.1: Time-domain and voltage-domain minimum power comparison

be helpful as to when we should consider replacing voltage-domain circuits with time-based depending upon CMOS technology. As the voltage supply is dropped, the voltage level detection is getting more and more challenging in presence of amplitude noise (e.g. voltage and current thermal noise). But, when we transfer the signal to time, the circuit works at the full supply voltage and hence is not affected by amplitude noise. It is imperative to recognize that the preceding analysis is carried out for the noise-limited circuit conditions. A similar approach can be used for the mismatch-limited circuit condition.flash ADC is not included in the formulations describing the total power consumption. In the same way, the voltage-to-time conversion function is not included in

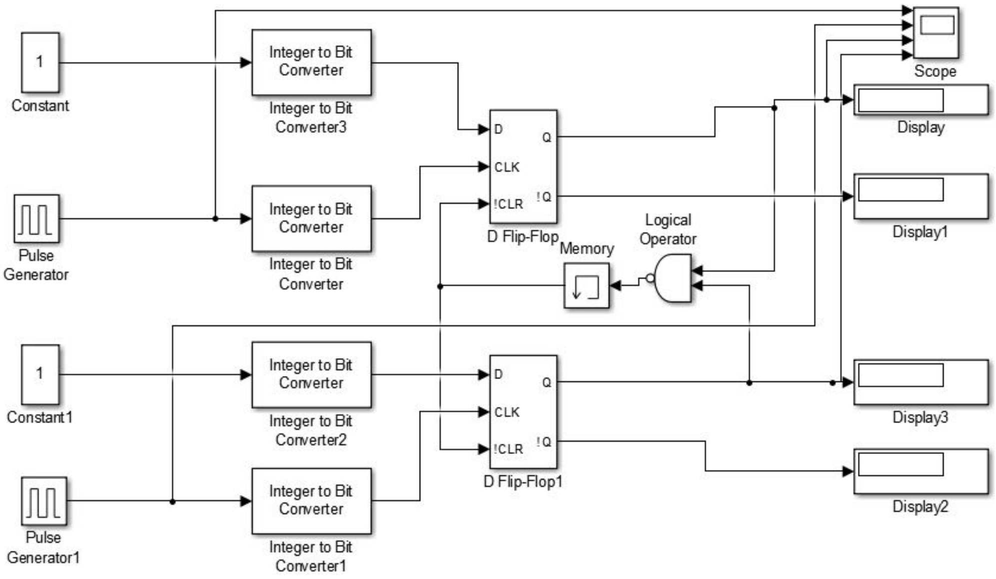


Figure 2.2: Block Diagram of basic Phase detector

the analysis of time-domain flash ADC architectures[10].

2.1 Phase detector

Initial Simulations are done in matlab simulink to understand the phase detector working model.In this work we have implement the basic phase detector design using two D-ff and logic gates. Consider the upper clock of D-ff as clock signal of high frequency and lower clock as reference clock signal. The output of the flip flop is consider as up and down. The output phase detected is as shown in TABLE 2.1 .Clock signal and clock reference signal have been taken of 100 MHz (0.1 ms).The phase difference between the two signal is (0.025 ms). Both up and down equal to 1 is also considered as zero phase detector output. As from the output waveform we can see that for the small time interval (0.025 ms) the value of up and down are 1 and 0 which means phase detector output is 1.

UP	DOWN	PHASE DETECTOR OUTPUT
1	0	+1
0	1	-1
0	0	0

Table 2.1: Phase Detector output

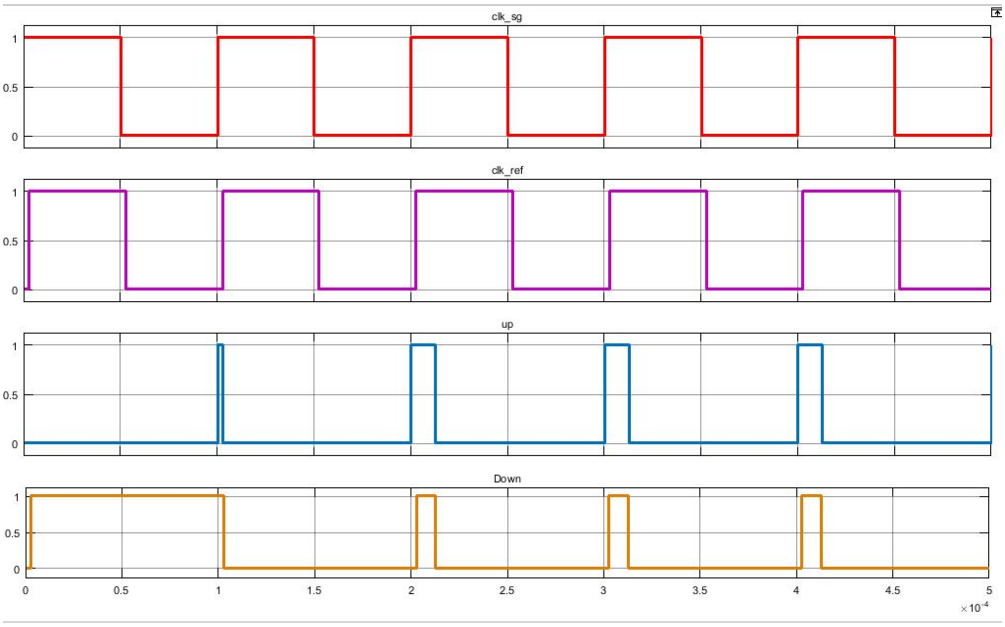


FIGURE 2.3: Simulation result of the above basic phase detector design in matlab simulink

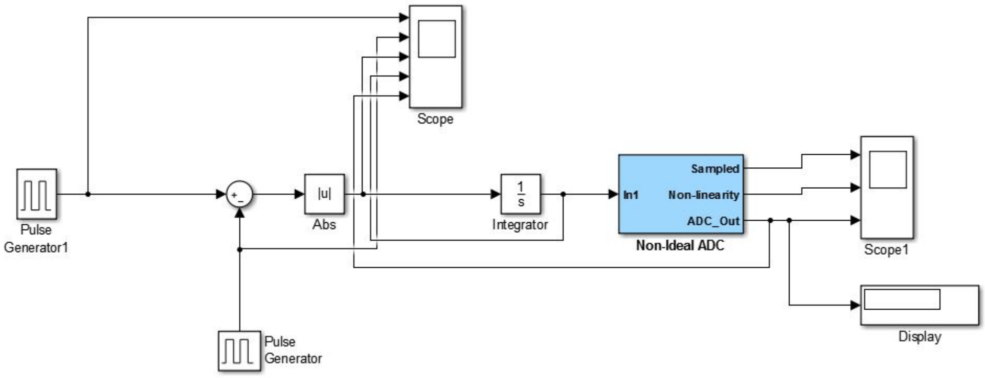


FIGURE 2.4: Analog TDC implementation in matlab simulink

2.1.1 Analog time to digital converter (first generation TDC)

The first generation TDC (traditional) has two stages in first stage the time information is converted into the analog voltage and then the ADC is required for analog to digital conversion[2].

In traditional TDCs as the resolution of TDCs is limited by the ADC.A fundamental trade-off between the dynamic range DR, i.e. the maximum time interval to be measured and the maximum number of bits N the ADC can accomplish is revealed by the following equation

$$DR = 2^{\mathrm{N}}.T_{\mathrm{LSB}} \tag{2.1}$$

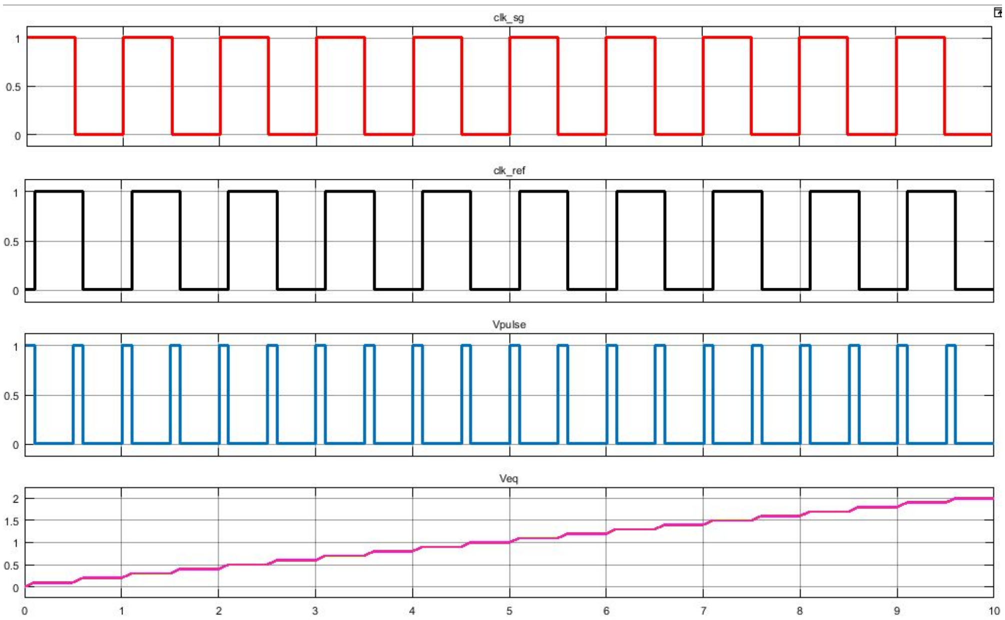


Figure 2.5: Simulation Result of above analog TDC implemented in matlab

The minimum time interval that can be resolved is given by T_{LSB}. As the maximum resolution of the ADC is limited by analog constraints a long measurement interval means low resolution and vice versa.Limitation given by equation 2.1 does not exists for TDCs, which is a great advantage over ADCs. There are also multi-stage approaches for digital TDCs but the motivation behind this is the reduction of area and power. The real need behind digital TDC is resolution, power and area. In this work we basically focus on digital TDC design.A matlab simulink implementation of analog TDCs(First generation TDC) is shown in Fig-2.4 and simulation results are shown in Fig-2.5.

2.1.2 Digital TDC

If the motivation for a TDC was just to implement a precise timer, an analog approach would be enough. However, the strategy to provide TDCs as generic mixed-signal building blocks for various applications rises the suitability issue in sub-micron scaled CMOS technologies.The advantages of time domain signal processing and the superior scaling properties of TDCs have been utilize in new design of all digital phase locked loop design(ADPLL).Which are not like analog TDC which converts time domain information first into the analog and then to the digital domain. Such TDCs consist mainly of an ADC so have all the impairments of analog circuits in deep sub-micron technologies. The advantages of the time domain can be exploited only if there is no analog conversion step in the time-to-digital conversion. Only if the TDC is designed by digital circuitry the scaling and robustness can be maintained. Therefore, digital conversion techniques are deployed.The simplest technique to quantize a time interval is to count the cycles of a

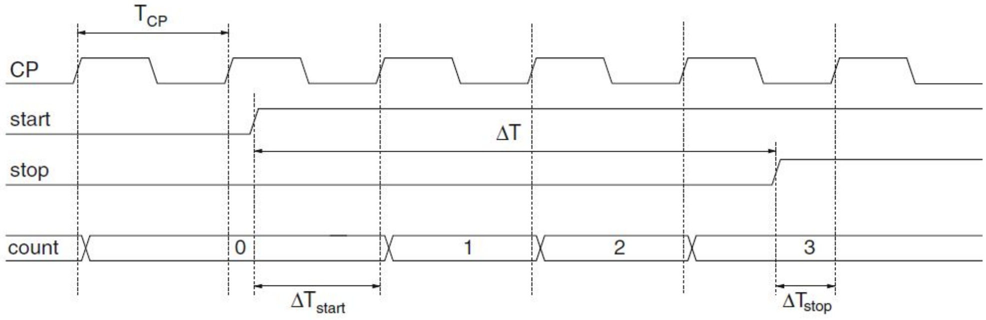


Figure 2.6: Principle of counter based TDC

reference clock fitting into the respective measurement interval.As shown in Fig 2.6 the measurement interval defined by the start and stop signal is completely asynchronous to the reference clock signal. This causes a measurement error ΔTstart at the beginning and ΔT stop at the end of the time interval. The measurement interval ΔT can be expressed as

$$\begin{cases} \Delta\ \mathrm{T}=\mathrm{N.T_{CP}}+(\mathrm{T_{CP}}\text{-}\Delta\ \mathrm{T}\ _{\mathrm{stop}})\ \text{-}(\mathrm{T_{CP}}\text{-}\Delta\ \mathrm{T_{start}}) \\ \Delta\ \mathrm{T}=\mathrm{N.T_{CP}}\text{-}\Delta\ \mathrm{T}\ _{\mathrm{stop}}\ +\Delta\ \mathrm{T}\ _{\mathrm{start}} \\ \Delta\ \mathrm{T}=\mathrm{N.T_{CP}}\ +\ \varepsilon T \\ \Delta\ \mathrm{T_{stop}} \in [0;T_{\mathrm{CP}}] \\ \varepsilon T\ =\Delta\ \mathrm{T_{start}}\text{-}\Delta\ \mathrm{T_{stop}} \in [-T_{\mathrm{CP}};T_{\mathrm{CP}}] \end{cases} \tag{2.2}$$

where N is the counter value and $\mathrm{T_{CP}}$ the reference clock period. $\Delta\mathrm{T_{start}}$ and $\Delta\mathrm{T_{stop}}$ are the time intervals between the start and the stop signal, respectively, and the next rising edge of the clock signal. The quantization error of the ΔT measurement is between -$\mathrm{T_{CP}}$ and +$\mathrm{T_{CP}}$, i.e. is limited to twice the period of the clock signal.

An even higher resolution is achieved by subdividing one clock period asynchronously into smaller time intervals. The digital circuit that performs this subdivision is actually what we call a digital time-to-digital converter.Resolution is the criterion that distinguishes a counter from a TDC.

$$\begin{cases} \Delta\mathrm{T}=\mathrm{N.T_{CP}}+(\mathrm{T_{CP}}\text{-}\Delta\mathrm{T_{stop}})\text{-}(\mathrm{T_{CP}}\text{-}\Delta\mathrm{T_{start}}) \\ \Delta\mathrm{T_{start}}=\mathrm{N1}.\frac{T_{\mathrm{CP}}}{k}\text{-}\varepsilon 1 \\ \Delta\mathrm{T_{stop}}=\mathrm{N2}.\frac{T_{\mathrm{CP}}}{k}\text{-}\varepsilon 2 \\ \varepsilon 1, \varepsilon 2 \in [0;\mathrm{T_{LSB}}=\frac{T_{\mathrm{CP}}}{k}] \\ \Delta\mathrm{T}=\mathrm{N.T_{CP}}+\mathrm{N1}\frac{T_{\mathrm{CP}}}{k}\text{-}\varepsilon 1 - N2\frac{T_{\mathrm{CP}}}{k} + \varepsilon 2 \\ \varepsilon_{\mathrm{t}} = \varepsilon 2 - \varepsilon 1 \in\ [\text{-}\frac{T_{\mathrm{CP}}}{K};\frac{T_{\mathrm{CP}}}{K}] \end{cases} \tag{2.3}$$

The measurement interval quantized with a TDC can be described by where the resolution $T_{\mathrm{LSB}} = \frac{T_{\mathrm{CP}}}{k}$ is increased by the factor k. The interpolation factor k describes in how many sub-intervals the reference clock cycle is partitioned, N1 and N2 indicate the position of the start and the stop event within such a reference clock cycle. The subsequent chapters describe the basic concepts of digital time-to-digital converters and explain how a higher resolution can be achieved even without a higher reference clock frequency.

Chapter 3

State of art

The time-to-digital converters (TDC) that offers precise measurement of the time interval between two events are widely used in different field. For high-energy physics application, it can provide very accurate time-of-flight measurement in term of picoseconds. For measurement instrumentation applications, it can be used to measure time information in digital oscilloscopes and logic analyzers. However, the most famous application of TDC is as a frequency synthesis, used by ADPLL[2]. In a divider-assisted ADPLL, Time-to-digital converter (TDC) is one of the most crucial blocks.TDC measures and digitizes the phase difference between reference signal and feedback signal. The TDC is a mixed-signal block and also work as a interface between time domain and digital domain. Therefore, it is unavoidable that the TDC induces quantization errors when converting time to digital words due to finite resolution. The quantization error could dominate the in-band phase noise at the output of ADPLL while it also limits the loop bandwidth. The limitation on the loop bandwidth in turn reduces the suppression of DCO phase noise, causing poor overall phase noise performance. The key to reduce quantization error is to improve the resolution of the TDC. Thus, design and implementation of high-resolution TDC become the ultimate goal for the TDC designers. With most recent process technology and refined architecture, the resolution can easily reach below 10 ps and also high-resolution, low dead time and large dynamic range are also required for high quality TDC. Dead time refers to the minimum time between two measurements. On the other hand, dynamic range(detection range), is the maximum time interval that can be measured by TDC[2]. Since the TDC may working at different frequencies, Both low dead-time and large dynamic range secure the functionality and stabilizability of the system. This chapter provides a review on different TDC architectures and explanations on their working principles. Apart from the fundamentals, design and implementation of the proposed Vernier gated ring oscillator based TDC is also described in this chapter.

3.1 Buffer delay line TDC

The higher resolution is achieved by delaying the original reference clock in a chain of digital delay elements. The resolution then depends on the delay of the delay elements in the chain. Figure 3.1 describes the operating principle of a TDC based on a digital delay-line. The reference clock which is in a more general sense an arbitrary start signal is delayed along the delay-line. On the arrival of the stop signal the delayed versions of the start signal are sampled in parallel. Either latches or flip-flops can be used as sampling elements. The sampling process freezes the state of the delay-line at the instance where the stop signal occurs. This results in a thermometer code because all delay stages which have been already passed by the start signal give a HIGH value at the outputs of the sampling elements, all delay stages which have not been passed by the start signal yet give a LOW value. The position of the HIGH-LOW transition in this thermometer code indicates how far the start signal could travel during the time interval spanned by the start and the stop signal. Hence this transition is a measure for the time interval. The number N of all sampling elements with a HIGH output is related to the measurement interval ΔT according to

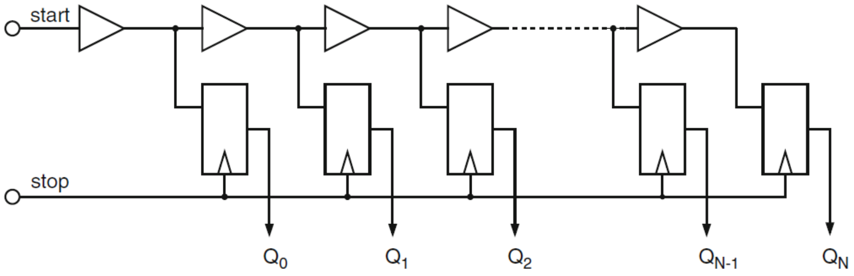


FIGURE 3.1: Buffer delay line TDC

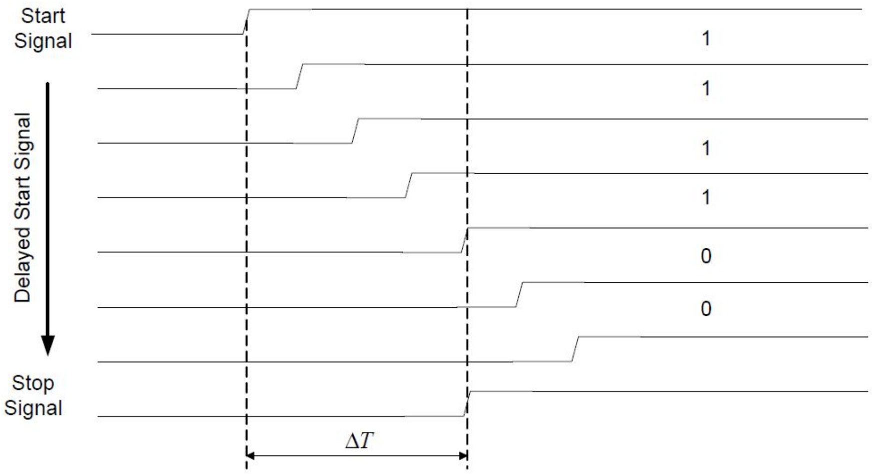


FIGURE 3.2: Buffer delay line TDC Waveform

$$N = \frac{\Delta T}{T_{LSB}}$$

where T_{LSB} is the delay of a single delay element in the delay-line. The time interval ΔT can be calculated from the number of HIGH outputs by

$$\Delta T = N.T_{LSB} + \varepsilon$$

where ε describes the quantization error that arises as a delay element has been either passed by the start signal yet or not.Any intermediate state is not possible. The start signal ripples along the buffer chain and flip-flops are connected to the outputs of buffers. On the arrival of stop signal the state of delay line is sampled by flip-flops. One of the obvious advantages of this TDC is that it can be implemented fully digital. Thus it is simple and compact. However, the resolution is relatively low as it is the delay of one buffer.

3.2 vernier delay line TDC

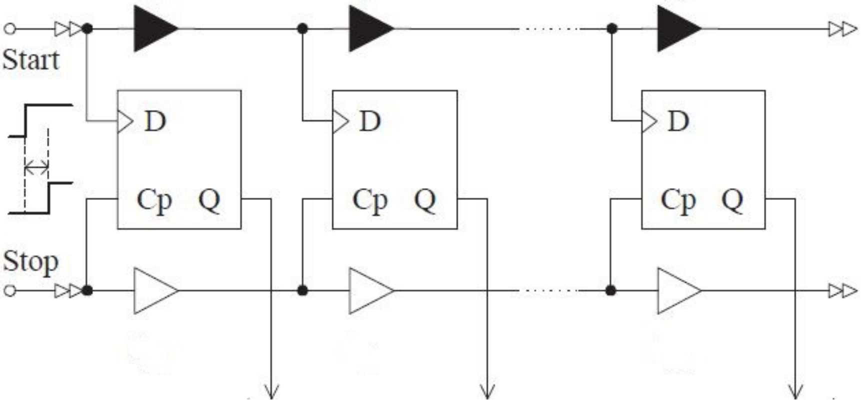


FIGURE 3.3: vernier delay line TDC

The resolution in this TDC is the delay of difference of inverters in upper and lower delay chain which is very high compared to buffers delay chain. In this case, the length of measurement intervals is not indicated by the position of high to low transition but by a phase change of the alternation of high to low sequence. Consequently, the rise and fall delay of inverter should be made equal which requires highly match of the process. In addition, the resolution is still limited by technology and therefore not high enough in our application of ADPLL. A start signal propagates through one of the delay chain with lager unit delay of 1, while the stop signal propagates through the other with smaller unit delay 2, clocking the flipflop at each stage. The resolution is determined by the

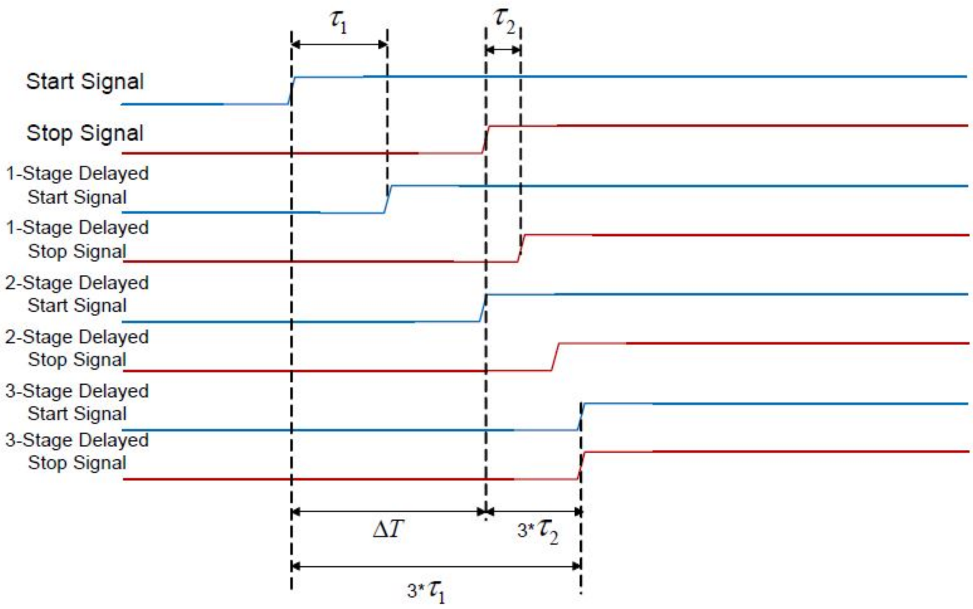


FIGURE 3.4: vernier delay line TDC Waveform

difference between two propagation delay values. Assume that after N stages of delay the rising edge of stop signal catches up with start signal, the measurement time interval can be given by

$$\Delta \mathrm{T} = \mathrm{N}(\tau 1 - \tau 2) + \varepsilon$$

where ε corresponds to the quantization error

3.3 Gated ring oscillator (GRO) TDC

The GRO TDC could achieve large dynamic range with small number of delay elements. It measures the number of delay element transitions during measurement interval. By preserving the oscillator state at the end of the measurement interval [k1], the quantization error [k1], from that measurement is also preserved. In fact, when the following measurement of [k1] is initiated, the previous quantization error is carried over as [k] = [k1]. This results in first-order noise shaping of the quantization error in the frequency domain. Apart from the quantization noise, GRO TDC structure realizes first order shaping of mismatch error. Thus, we can expect that this architecture ideally achieve high resolution without calibration even in the presence of large mismatch. A logic block generates the enable signal to control the GRO to oscillate at the arrival of start signal and disables the GRO when stop signal arrives. Then the outputs of GRO are fed into a

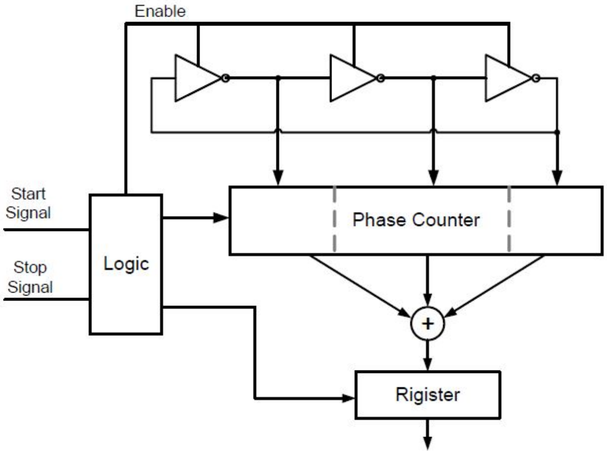


Figure 3.5: Block diagram of a GRO TDC

phase counter. The measurement of time interval is realized by counting the transitions of each GRO output phase during the given time interval [12]. The measurement time interval can be given by

$$\Delta\mathrm{T[k]}=\mathrm{N[k]}.\tau_{inv}+\varepsilon\mathrm{[k]}$$

where N is the number of counted phase transitions, τ_{inv} is the delay of each inveter in GRO, also equivalent to the raw resolution of GRO TDC, and ε is the quantization error.

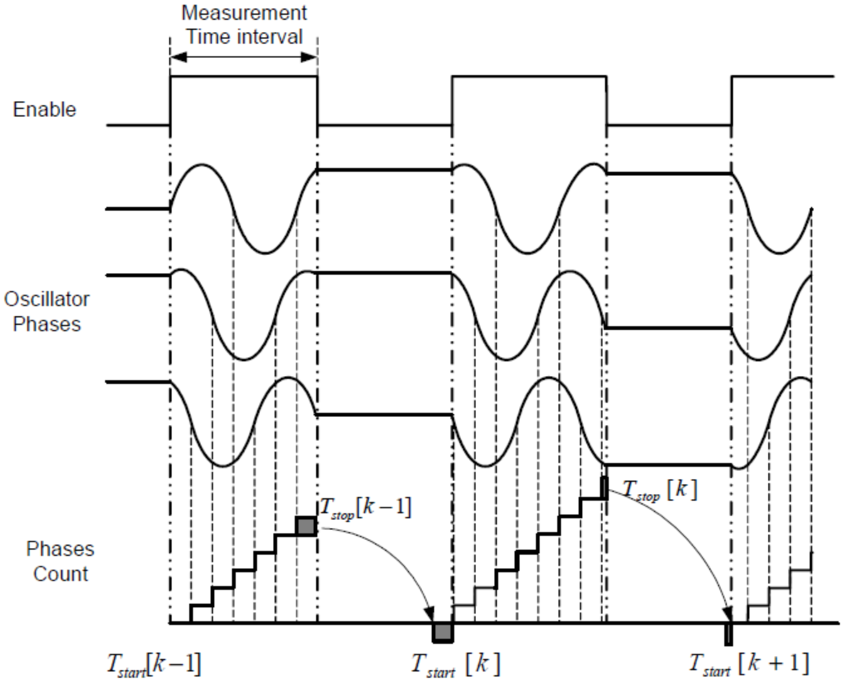


Figure 3.6: Waveform generated by a GRO TDC

Chapter 4

Proposed TDC design

A TDC converts the time difference between two input signals to the digital output. In a single delay line TDC the time resolution is limited by the gate delay in the delay chain whereas a Vernier TDC can achieve sub gate-delay resolution.As shown in Fig. 4.1 Assuming that the unit delays of the start and stop delay lines are $\tau 1$ and $\tau 2$ respectively, the resolution of a Vernier TDC is given by the delay difference in two delay chain elements

As the CMOS technology evolves the delay is reduces by a huge amount.The decrease in the delay of individual delay line will reduces the τ_{LSB}.This will result in the high resolution TDC designs. A new proposed Vernier architecture is described in this chapter uses the tristate buffer in place of D flip flop,as D flip-flops going into metastability state is a big challenge for TDC designers[4].The vernier delay line TDC with D flip flop have larger area and high power dissipation compare to proposed technique .The proposed TDC designs have very low power requirements compare to other presently

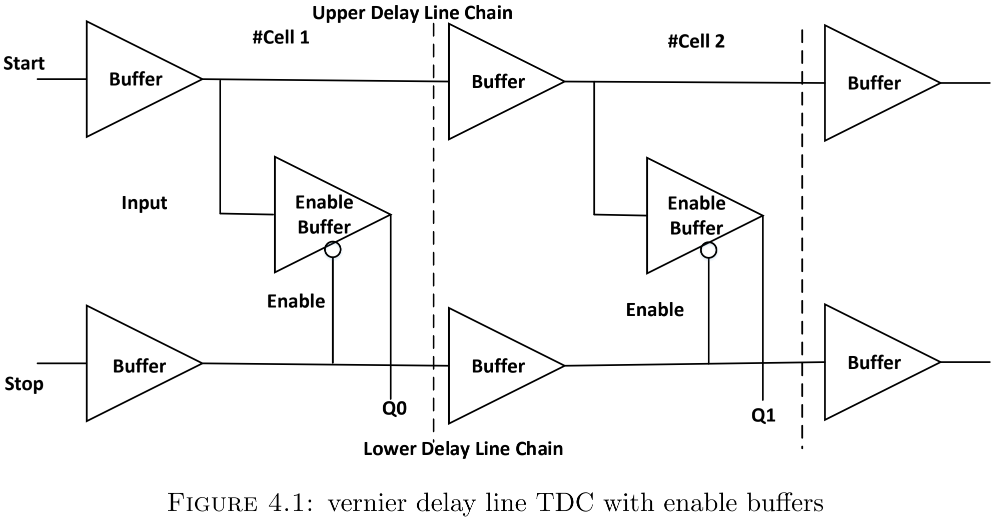


Figure 4.1: vernier delay line TDC with enable buffers

available TDC designs.Cadence virtuoso is used for designing and simulating the proposed techniques.

4.1 Single stage tristate buffer TDC

The basic unit of the proposed design is tristate buffer. The design of tristate buffer is shown in Fig-4.2 The PMOS M0 and M1 have width 4λ and NMOS M2 and M3 have width 2λ.For all the mos length is 65nm.This will maintain equal rise and fall time at output. Vernier delay line TDC are used to achieve high resolution but the power dissipation is high .So this work is helped in design of low power and high resolution TDC design. We have used two delay line and tristate buffer to reduce the power dissipation as shown in Fig-4.1. The D flip flop have been replaced by a tristate buffer which have lower power dissipation and smaller circuitry compare to traditional D flip flop based TDC .The input to TDC are main clock signal and reference clock signal, The main clock comes from the source and reference clock will be the feedback from the PLL

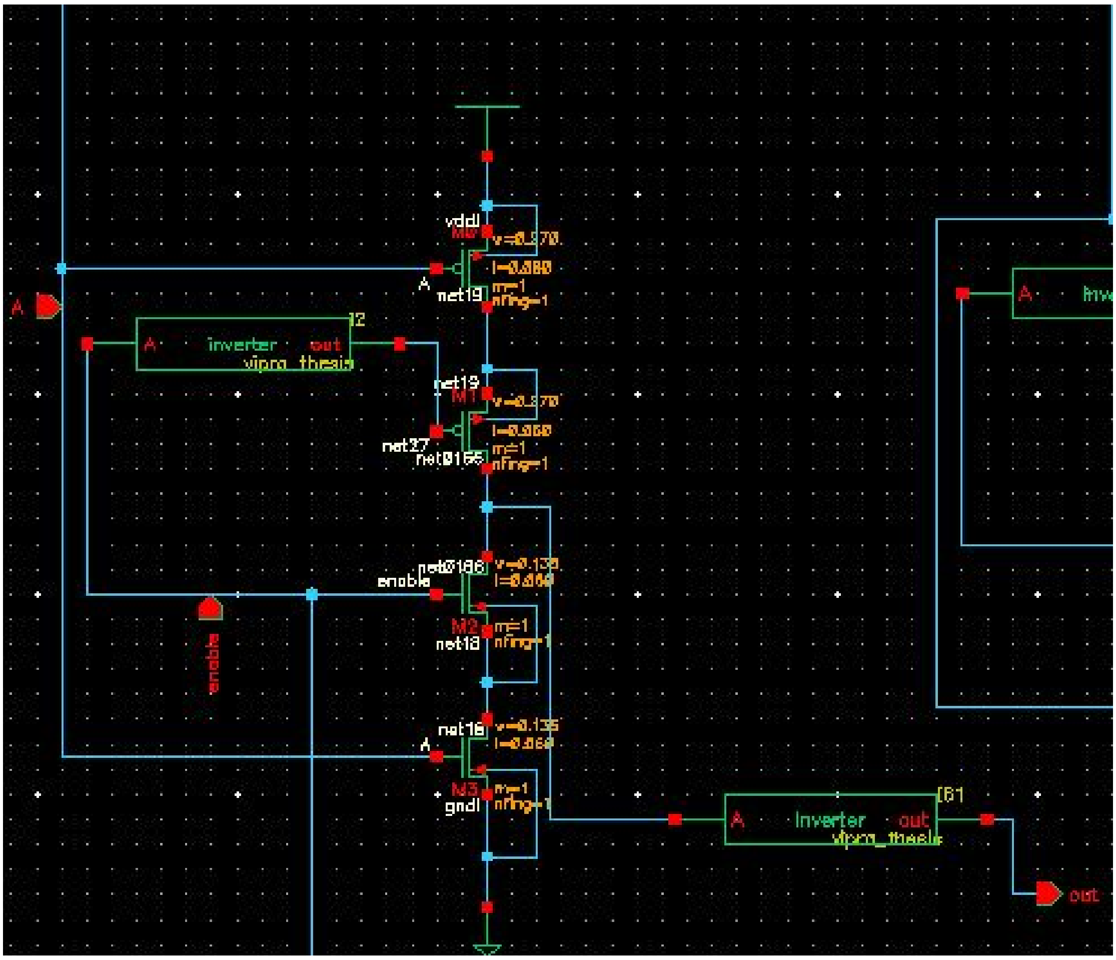


Figure 4.2: tristate buffer

output and can be considered as second clock signal .The main clock act as the input to buffer and reference clock is act as enable signal to the TDC through delaying by buffer delay chain. The A(start signal) is main clock and enable(stop signal) is reference clock signal as shown in Fig-4.3.The B0,B2 and all even number buffer represents upper delay line and B1,B3 all odd number buffers represents lower delay chain.`I_en0` are used for tristate inveters.M0,M1 pmos and M2,M3 nmos are scaled as define above for tristate buffer.

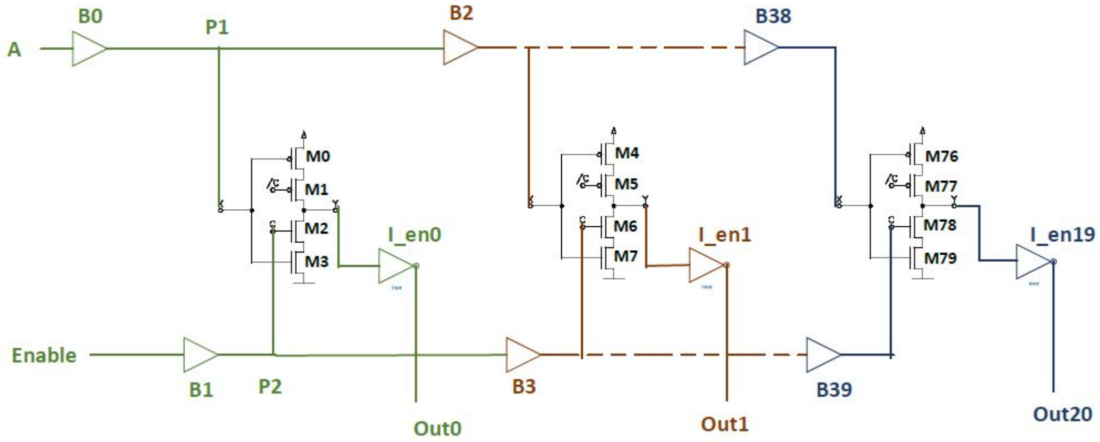
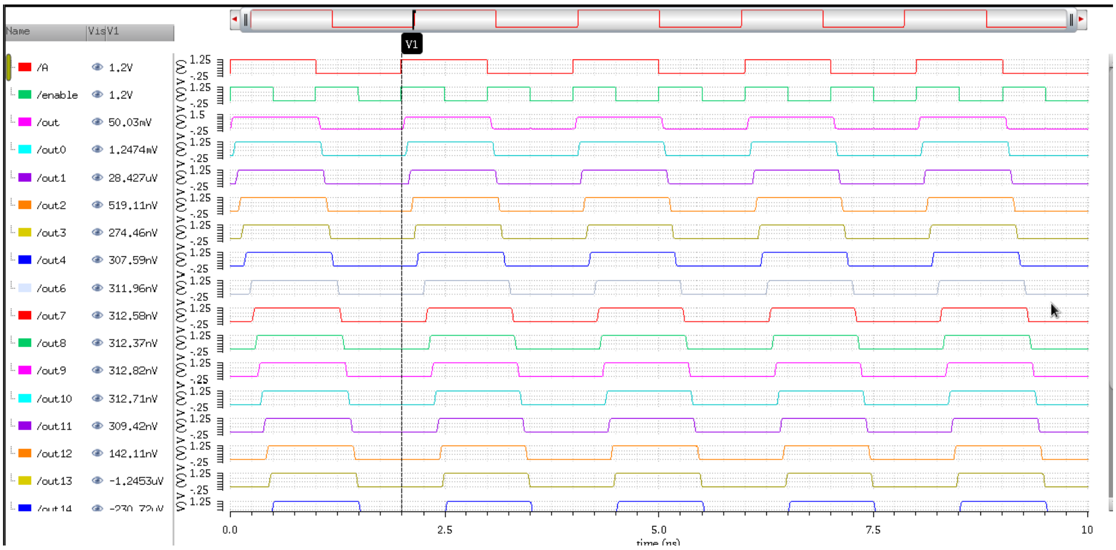


Figure 4.3: vernier delay line TDC using tristate buffer

the output signal is present at the output data line .We vary the time difference between the two clocks signals i.e. main clock and reference clock signal and observes the change in output data line we observes the variations in output data lines i.e.out0,out1 etc from Fig-4.3.Cadence virtuoso has been used to implement design schematic. The difference in the two delay chain will define the resolution of TDC. The proposed TDC architecture is also work effectively at high frequency up to 1 GHz. In the simulation of the proposed TDC design the A is a high frequency clock signal and enable is reference clock signal. The input to the TDC is the time difference between two signals. As shown in the Fig-4.1 the output from each stage is Q0, Q1 and so on. In the Schematic Fig-4.3 the output from each stage is represented by out0, out1 and similarly. In the Fig-4.3 we can see only the two stages of the proposed TDC.C and C_{bar} represent the enable and enable complement available at the same time. The delay line chain shown in the proposed TDC the buffer in the upper and lower chain have different delay, which will delay the signal with different values and the difference between the two delay chains will decide the resolution. In figure 4.4 we can see how output datalines are moving with respect to the delay elements in delay chain.



Name	Vis	V1
/A	👁	1.2V
/enable	👁	1.2V
/out	👁	50.03mV
/out0	👁	1.2474mV
/out1	👁	28.427uV
/out2	👁	519.11nV
/out3	👁	274.46nV
/out4	👁	307.59nV
/out6	👁	311.96nV
/out7	👁	312.58nV
/out8	👁	312.37nV
/out9	👁	312.82nV
/out10	👁	312.71nV
/out11	👁	309.42nV
/out12	👁	142.11nV
/out13	👁	-1.2453uV
/out14	👁	-230.72uV

FIGURE 4.4: output data line of vernier delay line TDC using tristate buffer

Chapter 5

Simulations and results

The technique implemented in this work, enables the power and resolution efficiently.Time to Digital converter has been implemented in a standard 65nm CMOS process .Single stage has a resolution of 4 ps with a power consumption of 72.3 uwatt .The Monte carlo simulations are performed to observe the delay with the PVT variations.As we can see that the power is significantly low and resolutions is very high for new design.This technique has good results compare to presently available TDC designs in terms of resolution as well as power.

5.1 Resolution measurement

The resolution results will show how accurately and what minimum difference between the two signal can be measured and calculate by the TDC. The maximum clock signal frequency used is of 1 GHz and there are 20 number of stages .We measure the delay provided by upper and lower delay lines as shown in Fig-5.1 and Fig-5.2. Resolution is

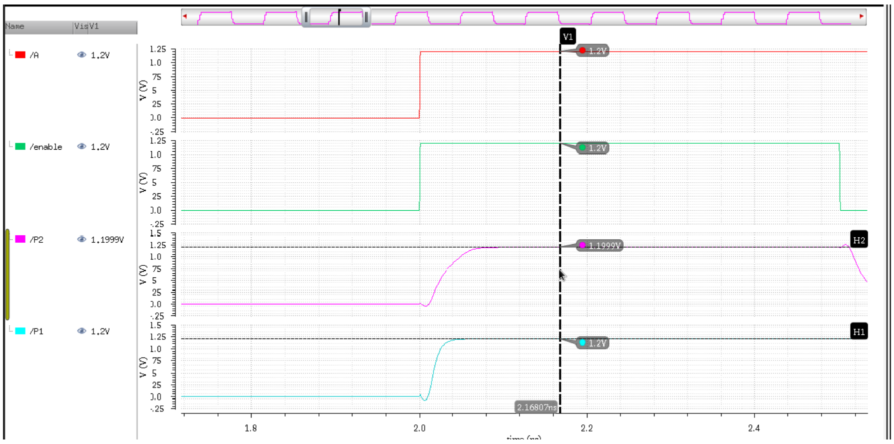


Figure 5.1: single stage tristate buffer TDC upper delay line

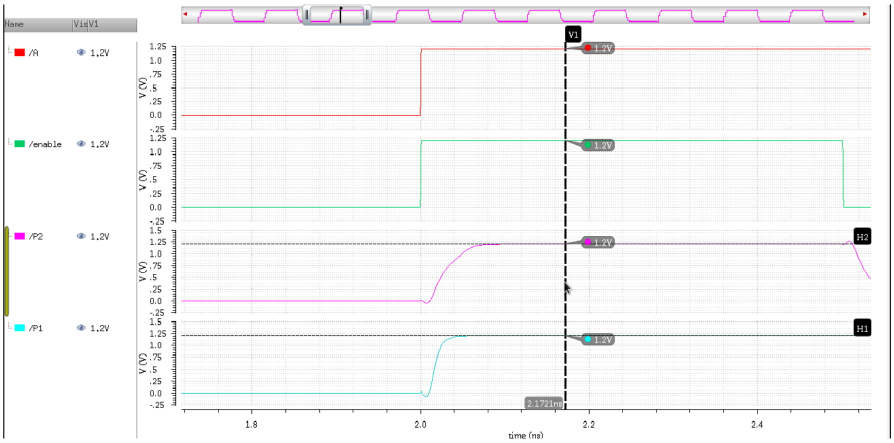


FIGURE 5.2: single stage tristate buffer TDC lower delay line

define as the difference in the both delay line($\tau 1$ -$\tau 2$).P1 and P2 are the delayed version of A and enable signal from first stage.The Enable signal is 1 ns period and 1 ps rise time and fall time pulse and signal A is 2 ns period and 1 ps rise time and fall time.

$$Resolution = \tau 1 - \tau 2$$

$$\tau 1 = (2.1721 - 2.001) = 0.1711 ns$$

$$\tau 2 = (2.16807 - 2.001) = 0.1670 ns$$

$$Resolution = 4 ps$$

5.2 Power measurement

The power measurement is done using calculator and saving pwr signal in result browser of ADE-L simulation window as shown in Fig-5.3. The average power is 72.5 W

5.3 Monte carlo simulation

Monte Carlo simulations have been performed on above described technique designed in a 65 nm CMOS process to predict how the delay difference is affected by the process variations. The supply voltage is 1.2 V. From the histogram shown in Fig. 5.4. It can be concluded that the TDC has an expected time resolution of 4.00225 ps with a variance of 396.547 fs for single stage TDC due to process variations and transistor mismatch.

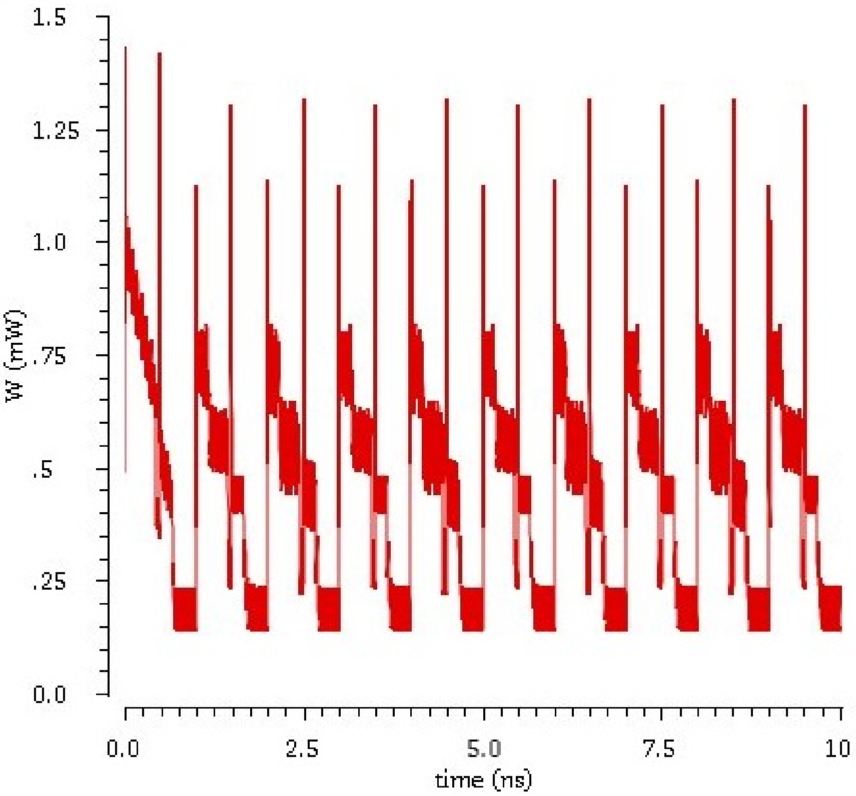


FIGURE 5.3: power measurement at single stage tristate buffer TDC

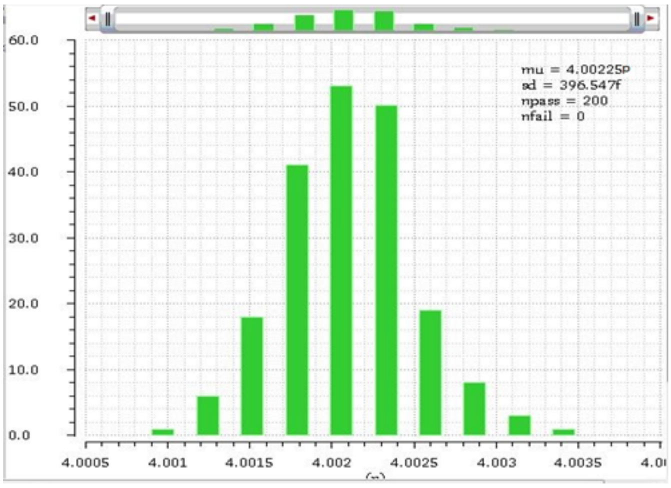


FIGURE 5.4: Monte carlo single stage tristate buffer TDC

5.4 Thermometric code decoder

This is also known as thermometer code encoding. This name is used because the design is similar to a mercury thermometer, in which the mercury column always rises to the appropriate temperature and no mercury is present above that temperature.The thermometer code is then decoded to the appropriate digital output code

5.4.1 Multiplexer based Decoder Design for TDC

The multiplexer based thermometric to digital decoder is shown in the Fig-5.5. The thermometric output data from the TDC is fed into the thermometric decoder.We have implemented it for 4 bits.The digital output data from the decoder is shown in Fig-5.6.

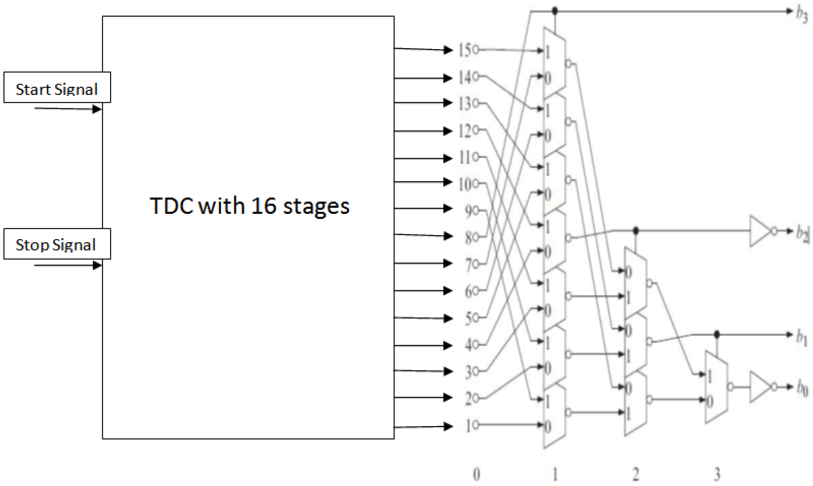


FIGURE 5.5: Thermometric decoder design for TDC

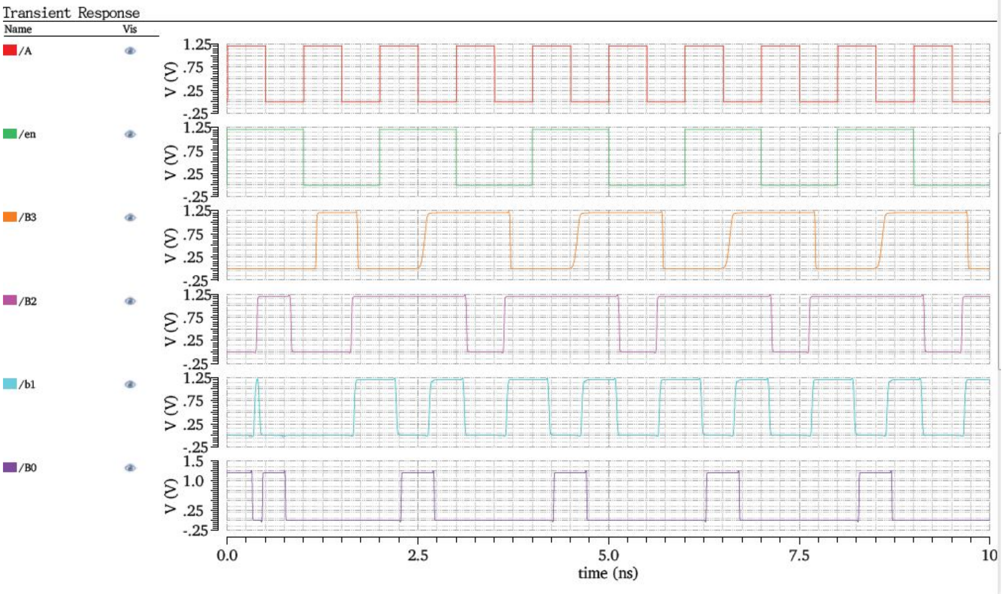


FIGURE 5.6: Output from Thermometric decoder

Chapter 6

Conclusion and future work

We have encountered the problem related to the analog TDC (first generation TDC).So we have presented system design, circuit simulation and result for digital TDC for digital PLL application in deep-submicrometer CMOS technology. The TDC design implemented here is used to replace the conventional phase detector and charge pump. In this design we used enable buffers which have less power and area requirements.In Table 6.1 we have compared our work with some presently available TDC designs.This work have good performance compare to other designs in terms of power and resolution. The design has good performance in terms of resolution and power as compared with the already implemented techniques.Table-1 shows the comparison between some of the presently existing techniques to the technique which we have implemented in this paper. Since the entire ADPLL system is very large and complex, so we are not able to run simulations on the entire circuit so we run simulation on TDC part. The result of the TDC circuit simulation only provide very few information. It would be worth spending more time

WORK	TECHNIQUE	CMOS TECHNOLOGY	POWER	RESOLUTION
This work	single stage vernier delay line TDC	65 nm	72.3 µW	4 ps
1	Delay Latch Chain Architecture	65 nm	1.14 mW	5.7 ps
2	Pseudo differential DL	90 nm	1.8 mW	17 ps
3	Vernier+GRO	90 nm	3.6 mW	1.8 ps

Table 6.1: Comparison between different TDC design

on the circuits simulation and collecting more simulation points with different parameters and noise for complete ADPLL, although the schematic level simulation results are satisfactory. It would also be interesting to explore the possibility of further higher frequency range of the ADPLL for an even higher resolution, meanwhile the suppression on the noise generated by the TDC and DCO should also be taken into consideration.

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