Process, Voltage and Temperature Compensated Oscillator for Phase Change Memories.

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IIIT-D-MTech-ECE-VLSI-15-17
April 04, 2017

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Submitted in partial fulfillment of the requirements
for the Degree of M.Tech. in Electronics and Communication,
with specialization in VLSI and Embedded Systems

Certificate

This is to certify that the thesis titled **"Process, Voltage and Temperature Compensated Oscillator for Phase Change Memories."** submitted by **Vivek Tyagi** for the partial fulfillment of the requirements for the degree of *Master of Technology* in *VLSI & Embedded Systems* is a record of the bonafide work carried out by him under my guidance and supervision in the Smartpower Technology Group at ST Microelectronics, Greater Noida. This work has not been submitted anywhere else for the reward of any other degree.

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Abstract

Non Volatile Memories (NVM's) are an integral part of every System-on-Chip (SoC) for retaining the data when power goes off. Phase change memory (PCM) is type of NVM and exhibits significant advantages over existing NVM alternatives, such as fast read access time, high write endurance, higher retention time and fast modify cycles. In PCM, the current pulses are used to change the state of bit cells (set or reset) and duration of current pulse is decided by the on-chip oscillator. The large inaccuracy in oscillation frequency will result in unreliable modify operation and may cause failure in read-write operations. The commonly used high accuracy clock references are realized by crystal oscillators, as they are immune to process, voltage and temperature variations, but integrating them with on-chip circuits increases the overall cost and power of system. Hence, it is important to investigate the high accuracy on chip clock generation strategy for low cost and low power applications.

In this dissertation, a 10MHz, 84µW, 73ppm/℃ PVT compensated ring oscillator and 10 MHz, 69µW, 42ppm/℃ PVT compensated latch based oscillator is presented in 110nm BCD9S Technology for PCM application. The presented PVT compensated oscillators consumes significant lesser power as well as area compared to traditional crystal counterparts. An on-chip voltage regulator is also designed to generate stable supply for oscillator and associated bias circuits to generate the frequency reference immune of large supply variations.

Acknowledgments

This thesis work has been supported by and carried out at ST Microelectronics, Greater Noida, India in the year 2016-2017.

My foremost expression of thanks is dedicated to the Almighty God for his blessings. I express my heartfelt gratitude to my supervisor, Dr. MS Hashmi, for his continuous guidance and support throughout this thesis. I am highly thankful to my mentors at ST Microelectronics, Mr. Ganesh Raj and Mr. Vikas Rana, for providing suggestions and valuable feedback in the above endeavor, which are indispensable and without which it would not have been possible to accomplish the above task effectively. I also earnestly acknowledge the support and guidance of all my team members at ST Microelectronics. Last but not the least, I express sincere thanks to my parents, for their unconditional love, support and encouragement in all my efforts.

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Chapter 1

Introduction

Phase change memory is a type of embedded non-volatile memory and exhibits significant advantages over conventional flash memories such as fast read access time ($< 20ns$), high write endurance of about 10^{12} cycles and higher retention time. It also exhibits fast modify cycles almost an order less than the conventional floating gate based memory cell.

1.1 PCM and its Operation

PCM bit cell consists of resistor (heater) and word line select transistor. This resistor is made up of phase change material, which is a chalcogenide alloy. On application of high magnitude of current pulses PCM alloy changes its state from amorphous to crystalline or vice versa. In amorphous phase, bit cell resistor exhibits high impedance (RESET) state and in crystalline state bit cell exhibits low impedance (SET) state. Large difference in resistivity of cell material easily helps in determining the state of the cell by measuring the current flowing through cell during read operation [1]. Fig.(1.1) shows the basic principle of phase change memories, i.e. phase change materials can change its state reversibly from amorphous to crystalline or vice versa.

Fig.(1.2)(a) represents the transistor level schematic of bit cell, it consists of word line (WL) select transistor M1 and phase change material represented as a resistor, the bit cell is connected with bit line (BL). Fig.(1.2)(b) represents the current pulses used during set and reset operation of bit cell and Fig.(1.2)(c) represents the state of phase change material. The memory cell is selected by driving the word line and bit line to a voltage levels corresponding to operation to be performed. Current pulse of 500µA having duration of 100ns is used for reset operation and pulse of 300µA having plateau duration of 200ns is used for the set operation. Cell exhibits resistance of $K\Omega$ in crystalline (SET) state and $M\Omega$ in amorphous (RESET) state.

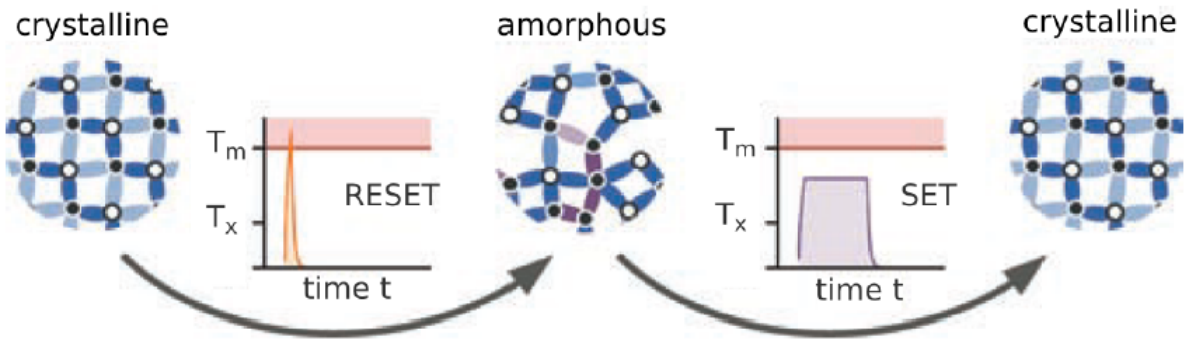

Figure 1.1: Basic principle of PCM

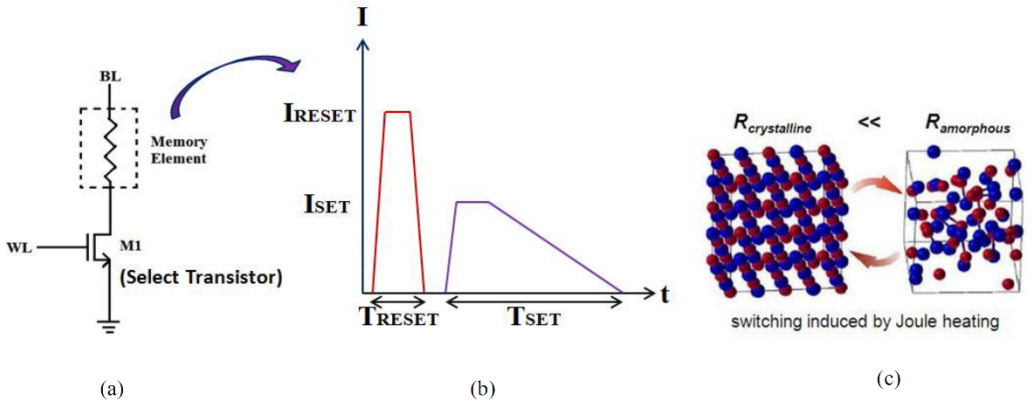

Figure 1.2: a) PCM memory cell schematic b) Current profile for set and reset pulses c) Switching profile of memory cell between amorphous and crystalline state

1.2 Need of PVT compensated oscillator in PCM

In PCM, the duration of set and reset pulse defines the state of cell therefore, for safe and reliable operations across process, voltage and temperature (PVT) variations, it is important to generate the stable on chip frequency reference which decides the duration of current pulses in set and reset operation of memory.

During a write operation, PCM bit cell draws a high magnitude current to change the phase of chalcogenide alloy. Clock from oscillator block acts as a reference for digital controller, which is responsible for selecting the desired bit cell from memory array. It is also responsible for generating write pulse that is used to turn on the transistor M1 as shown in Fig.(1.3). Here, M1 enables the current mirror, and modify current flows through the bit cell. Process, Voltage and Temperature (PVT) compensated oscillator guarantees the accurate timings of write and read operation, which improves the reliability and retention ability of bit cell.

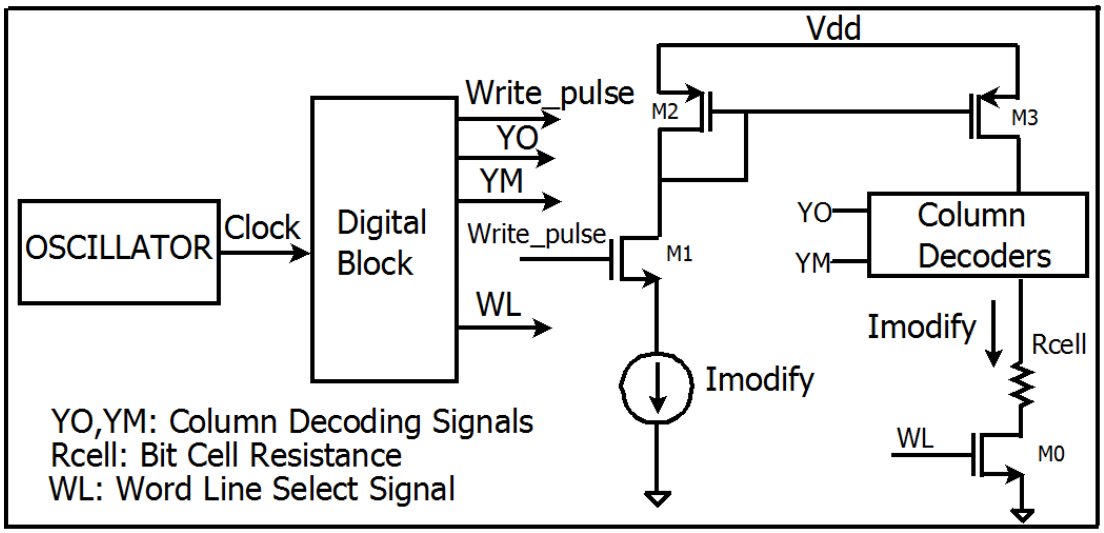

Figure 1.3: Oscillator block along with modify path

1.3 Literature Review

In recent years, many authors had proposed the different strategies to design the PVT compensated on-chip oscillator and few of them are listed below:

- A 7 MHz PVT compensated ring oscillator is designed in 250nm CMOS technology [2]. It uses a voltage regulator to generate stable supply for oscillator and associated bias circuits. The voltage controlled differential cells are used in three stage ring oscillator to generate the frequency reference. The control voltage of differential cell is generated by a threshold voltage detector reference circuit, which helps in achieving the process compensation. The output of oscillator is converted to full swing rail to rail signal by using a process independent voltage comparator to increase the noise immunity. It exhibit frequency variation of $\pm 0.84\%$ for operating range of -40℃ to 125℃ and consumes significant amount of on-chip area as well as power.

- In other architecture, a 1 MHz relaxation oscillator is designed in 130nm CMOS technology [3]. It consists of biasing reference to generate reference current, timing circuit to generate delay, comparator to generate rail-to-rail output and latch to store output value. The output frequency of relaxation oscillator depends on product of resistor and capacitor hence, for temperature insensitive operation, it uses resistors having zero temperature coefficient and fixed metal-insulator-metal (MIM) capacitor. The latch is also redesigned for making its delay independent of temperature and process. Frequency variation of $\pm 0.5\%$ across operating temperature range of 25℃ to 180℃ is reported in this work. The MIM capacitors along with Poly-resistors requires large on-chip area.

- In similar architecture of relaxation oscillator, 150 KHz reference is designed in 65nm CMOS technology [4]. It utilizes relaxation oscillator, controlled by a current proportional to mobility and a temperature sensor on a single chip to realize a temperature compensated oscillator. Output frequency of oscillator is used as a reference of phase locked loop (PLL), which comprises of phase detector, voltage controlled oscillator (VCO) and frequency divider circuit. For process compensation, digital trimming bits are introduced in design to correct the oscillation frequency. It exhibits the frequency variation of $\pm 0.5\%$ across temperature range of -55℃ to 125℃. This design exhibits significantly less temperature sensitivity at a cost of low operational frequency.

- In another design, a 10 MHz temperature compensated ring oscillator is presented in 180nm CMOS technology [5]. This design consists of supply regulated ring oscillator, which uses differential amplifier in place of inverter. It employs frequency to voltage conversion circuit in a feedback loop to convert frequency of oscillator into a reference voltage which is compared with band-gap generated reference voltage to generate error signal and this error signal drives the VCO. This design incorporates low power techniques and generates reference voltage in sub-threshold region. It exhibits a frequency variation of $\pm 0.4\%$ across temperature range of -55℃ to 125℃ and $\pm 0.04\%$ across supply voltage of 1.1 to 3.3V.

- Another closed loop design of 30 MHz temperature and supply compensated frequency reference is presented in 350nm CMOS technology [6]. The operation principle of this oscillator is somewhat similar to [5], but here a current controlled oscillator is used in feedback loop. In place of frequency to voltage converter used in [4], frequency to current converter block is used. The output of frequency to current converter block generates an oscillator's frequency equivalent current that is compared with temperature and supply compensated reference current. The error signal is a difference in these two currents and it drives the current controlled oscillator. This design exhibits a frequency variation of $\pm 0.5\%$ across operating temperature range of -20℃ to 100℃. This work does not report the frequency variation characteristics above 100℃, which makes the design less attractive for automotive applications.

In this work two oscillators are proposed that exhibits inherent temperature compensated behaviour and does not employ any feedback loop, or any on chip bias compensation circuit to achieve temperature compensation behaviour. The operation of oscillator is made current controlled and it helps in achieving the oscillation frequency immune to supply voltage variations. To compensate the process variations, control bits or trimming bits are also included in the design that helps in achieving the desired oscillator's frequency during calibration of the oscillator.

1.4 Outline of the Thesis

Chapter 1 introduces the reader with basic operation principle of phase change memories and explains the need of Process, Voltage and Temperature (PVT) compensated oscillator and existing PVT compensation strategies present in literature.

Chapter 2 deals with oscillator's fundamental principle and parameters which defines the oscillation frequency. It also discuss about the effects of temperature variations on CMOS circuits and use of MOS as an on-chip capacitor in design of oscillator.

Chapter 3 presents the working principle of proposed oscillator designs and PVT compensation techniques introduced in them. It also talks about the simulation results observed and frequency sensitivity results with process, voltage and temperature variations.

Chapter 4 discusses about the design of on-chip voltage regulator for making the frequency of oscillation immune to large variations in supply voltage.

Chapter 5 presents the conclusions and compares the performance and temperature sensitivity results with state-of-the-art designs available in the literature.

Chapter 2

Oscillator

An oscillator does not require any input and produces a periodic output usually in form of voltage. An oscillator is viewed as an amplifier in a positive feedback. Consider a unity gain negative feedback based amplifier as shown in Fig.(2.1). Its transfer function can be written as:

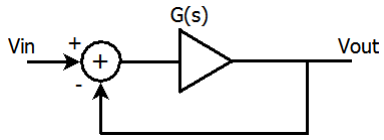

Figure 2.1: Feedback System

$$H(s) = \frac{G(s)}{1 + G(s)} \tag{2.1}$$

If the amplifier exhibits so much phase shift at high frequencies such that overall feedback becomes positive, and it starts oscillation. It can be explained as, for s = jω_o, G (jω_o) = -1, closed loop gain H(s) in Eq.(2.1) approaches infinity at 'ω_o'. The input of oscillator is a noise component at ω_o which experiences a gain of 1 with a phase shift of '180^o'. For oscillations to begin feedback loop gain G(jω_o) has to follow two loop conditions [7]:

- Loop gain of unity or greater is necessary i.e. $|G(j\omega_o)| \geq 1$.
- Frequency dependent phase shift of 180^o should be present i.e. $\angle G(j\omega_o) = -180^o$.

These conditions are only necessary conditions but not sufficient to generate oscillation across process, voltage and temperature variations. In order to guarantee the oscillation across PVT variations, loop gain of at least twice or thrice the required value is selected.

2.1 Principle of ring oscillator

Ring oscillators are most commonly used voltage controlled oscillator or current controlled oscillator in phase locked loops [5] [6] and clock recovery circuits. Ring oscillators are designed with a ring of cascaded inverter stages. Odd number of inverters are used in ring oscillator such that, output of last stage is inverse of the input of first stage. However, single stage inverter does not oscillate because it cannot provide frequency dependent phase shift of 180^o in loop. The time delay introduced by individual inverter stage can be written as:

$$t_d = \frac{C_{out}(V_H - V_L)}{I_{ref}} \tag{2.2}$$

Here, C_{out} represents load capacitance present at output node, I_{ref} represents the reference current used to charge the output load capacitance and $(V_H - V_L)$ represents the voltage swing at output node of inverter. In order to achieve high accuracy frequency reference across PVT variations, Eq.(2.2) should have to remain constant irrespective of PVT variations.

2.2 Effects of temperature on CMOS circuits

Threshold voltage (V_{th}) of device and the mobility of the carriers (μ) varies significantly with temperature. The effects of these two parameters are discussed in detail:

- Threshold voltage (V_{th}) variation: The threshold voltage is defined for an n-channel MOSFET as the value of gate-source voltage, which gives the same concentration of electrons in the inverted n-type channel as there is of holes in the ptype substrate.

  $$V_{th}(T) = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \tag{2.3}$$

  V_{FB}, is the flat band voltage, ϕ_F is the Fermi energy and γ is body effect parameter. As the operating temperature increases, the threshold voltage of the device decreases [8].

- Mobility (μ) variation: The carrier mobility (μ) (cm^2/Vs) defines the drift velocity of carrier in electric field. As the operating temperature increases the probability of scattering of carrier with crystal lattice increases, this causes reduction in mobility of the carriers at the high temperature [8]. The relation can be modeled as:

  $$\mu(T) = \mu(T_o)\{\frac{T}{T_o}\}^{-1.5} \tag{2.4}$$

  Here T represents absolute temperature, T_o is the reference temperature and $\mu(T_o)$ is mobility of carriers at reference temperature.

2.3 MOS capacitance

MOSFET can also work as a voltage dependent capacitor apart from its conventional operation. However, its capacitance value depends on operating region of MOSFET; therefore it is also termed as variable capacitor (var-cap). The gate layer and charge layer present in substrate acts as a two parallel plates of capacitor and thin oxide layer acts as a dielectric layer between two capacitor plates. Consider an NMOS present in Fig.(2.2); its gate voltage is varied from $-V_{dd}$ to V_{dd}. Initially when gate is biased to $-V_{dd}$, wide depletion region is available, since gate is negative biased, positive holes present in substrate are accumulated below the oxide layer, hence effective width of capacitor is equal to the width of oxide layer. In this region NMOS is operating in accumulation region, since holes present in substrate are accumulated in the channel region.

When gate starts rising from negative voltage towards positive voltage, the positive holes present at the oxide-substrate interface are repelled and pushed back into the bulk leaving a depletion layer. This depletion layer counters the positive charge on the gate and keep on increasing till the gate voltage is below the threshold voltage. When the channel region is free of any charge carrier, maximum separation distance will exist between two parallel plates of capacitor. Minimum value of capacitance is obtained in this operating region, since capacitance value is inversely proportional to separation distance of parallel plates. In this region NMOS is biased in depletion region, because channel area is depleted of any charge.

When gate voltage starts rising again and reaches V_{dd}, the channel will consists of free electrons which are accumulated below the gate-substrate interface. This free electron layer again reduces the separation distance between two plates of capacitor; hence capacitance will be high in this region. In this region of operation, NMOS is biased in strong inversion region since free electrons are available in the channel region. In strong accumulation and deep inversion region, MOS capacitance exhibits maximum value of gate capacitance. The total gate capacitance can be expressed as a sum of gate to source capacitance(C_{gs}), gate to drain capacitance(C_{gd}) and gate to bulk capacitance(C_{gb}).

$$C_g = C_{gs} + C_{gd} + C_{gb} \tag{2.5}$$

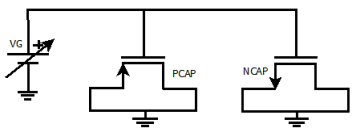

Figure 2.2: Setup for estimation of gate capacitance of NMOS and PMOS having W=1μm and L=1μm

It can be concluded from Fig.(2.3), that the operating region of MOS defines the gate capacitance value and to get a constant value of gate capacitance, it is important to bias the MOS either in strong depletion or in strong inversion region.

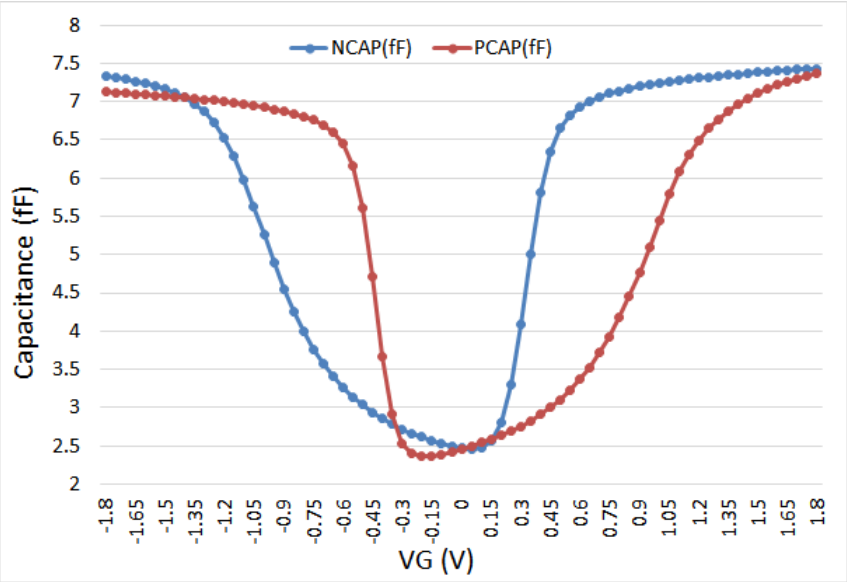

Figure 2.3: Gate capacitance (C_g) of NMOS and PMOS across different value of gate voltages in typical process.

2.4 Accuracy of Oscillator

Accuracy or stability of oscillator is a measure of variation of output frequency of oscillator due to temperature, process corners, voltage and noise. If nominal frequency is f_o and absolute variation in output frequency is $\triangle$f, then error can be written as:

$$f_{error}(\%) = \frac{\triangle f}{f_o} \times 100 \tag{2.6}$$

There is another term used to represent accuracy of oscillator only across temperature variations, it is called as temperature coefficient (ppm/ ℃) and expressed as:

$$TC = \frac{\triangle f}{f_o.T} \times 10^6 \tag{2.7}$$

An electronic system requires different level of accuracy for the frequency references as per their applications. For instance, micro-controller application requires accuracy of 100 ppm to 10,000 ppm whereas mobile handset devices require accuracy of 2.5 ppm. To achieve such high accuracy crystal or MEMS based oscillators are used. However integration of crystal based oscillator is a cost intensive process, which is not a feasible solution in low cost applications for moderate accuracy frequency reference [9].

Chapter 3

PVT Compensated Oscillators

This chapter will discuss about the design strategies and simulated result of proposed PVT compensated oscillators. A ring oscillator and a latch based oscillator is presented in this chapter along with PVT compensation strategies to achieve stable frequency reference for phase change memories.

3.1 Ring Oscillator

Ring oscillator consists of an odd number of inverter stages present in a loop. Each stage is responsible for adding a frequency dependent phase shift and also provides a gain to satisfy the necessary condition of oscillation. Fig.(3.1), shows the architecture of proposed ring oscillator. First two inverter stages comprising of transistors M0-M3 are current starved stages and remaining three stages consisting of transistors M4-M9 are biased at supply voltage.

The first current starved stage is responsible for maximum amount of loop delay and the second current starved stage is used for the temperature compensation of the oscillator. The rest of supply biased inverter stages allows the next generated phases to have rail to rail voltage swing. The PMOS transistor M18 is used as a capacitor after first stage and is biased either in the inversion or in accumulation region to get an almost constant value of gate capacitance. In this design, most of the loop delay comes from the first stage itself and it arises due to charging of gate capacitance present at 'CAP' node. while other inverter output nodes have only small parasitic capacitors. The charging current (I_{cap}) of capacitor can be written as:

$$I_{cap} = I_{bias} \times \frac{(W/L)_{11}}{(W/L)_{10}} \tag{3.1}$$

Where I_{bias} represents the reference current and it is assumed to be constant across PVT variations and W/L denotes the aspect ratio of the respective transistors. Subsequently, the charging

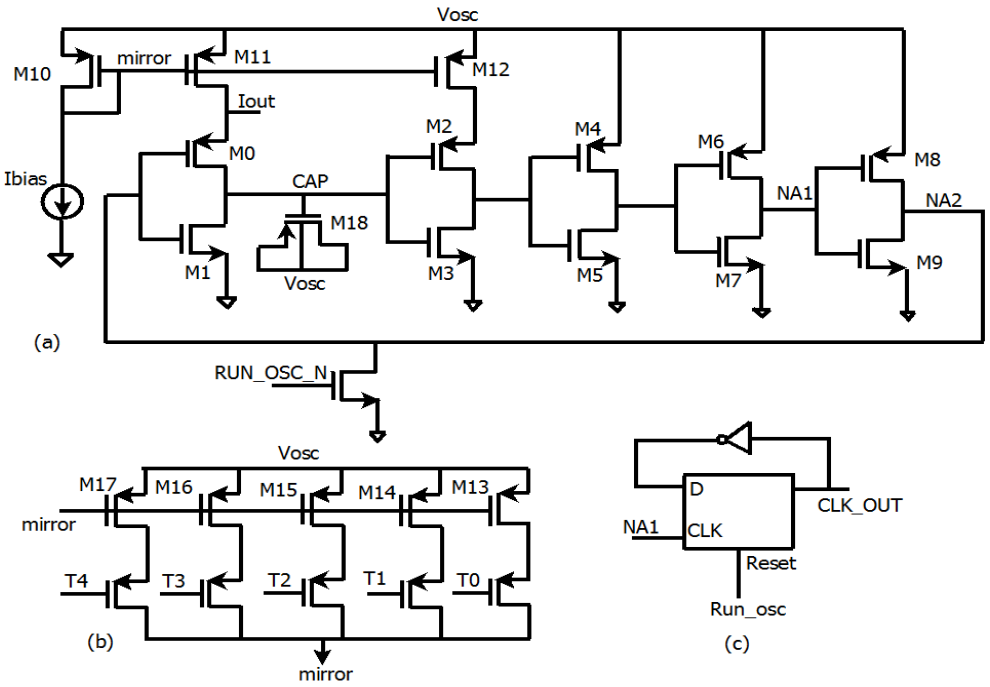

Figure 3.1: a)Schematic diagram of proposed PVT compensated ring oscillator. b) Trimming bits transistors T0-T4 used to vary the width of diode connected transistor M10. c) D flip-flop is used to generate the clock having 50% duty cycle.

time ($T_{charging}$) of gate capacitor (C) of M18 can be expressed as:

$$T_{charging} = \frac{CV_{cap}}{I_{cap}} \tag{3.2}$$

The term V_{cap} is also equal to gate to source voltage of device M3 and it can also be written as:

$$V_{cap} = V_{GSM3} \tag{3.3}$$

The second stage of ring oscillator is also current starved hence fixed current is used to charge the output node of second stage which consists of small parasitic gate capacitance of M4 and M5. If the transistors M11 and M12 are matched, then V_{GSM3} can be expressed as:

$$V_{GSM3} = V_{THM3} + \sqrt{\frac{2.I_{cap}}{\mu_n.C_{ox}.(\frac{W}{L})_3}} \tag{3.4}$$

3.1.1 Principle of Temperature Variation Compensation

In Eq.(3.2), capacitor (C) and current (I_{cap}) are independent of temperature variations but V_{cap} is a temperature dependent term. However, the dependence of V_{cap} or V_{GSM3} on temperature

is apparent in Eq.(3.4). This dependence of V_{GSM3} on temperature can be nullified if negative temperature coefficient of threshold voltage is equal to the positive temperature coefficient of overdrive voltage of M3. The temperature coefficient of threshold voltage is technology dependent [8] but the temperature coefficient of overdrive voltage is dependent on aspect ratio of transistor and hence proper sizing of M3 can compensate the variations arising in V_{GSM3} due to temperature.

3.1.2 Principle of Process Variation Compensation

Moreover, Eq.(3.4) also suggests that dependence of V_{GSM3} on process can lead to variation in the charging time. Therefore, the charging time will remain fixed across process variations only if V_{cap}/I_{cap} ratio remains constant. In order to achieve this, the capacitor-charging current can be modulated using trimming bits according to different process corners. In Fig.(3.1)(b), T0-T4 represents trimming bits transistors, which act as switches for M13-M17 transistors. These bits modulate the equivalent width of transistor M10. From Eq.(3.1) it can be deduced that the increase in width of transistor M10 will decrease the capacitor charging current (I_{cap}). This programming ability in design provides the ease to designer to correct the oscillation frequency of oscillator during calibration of oscillator.

3.1.3 Principle of Voltage Variation Compensation

The voltage variations will not have significant impact on frequency of oscillation since $T_{charging}$ does not show any dependence on supply voltage. The inverter stages biased at supply voltage will have no impact on oscillation frequency as they do not provide significant loop delay. The total loop delay (T_{delay}) and frequency of oscillation (f_{osc}) can be expressed as:

$$T_{delay} = T_{1ststage} \tag{3.5}$$

$$T_{1ststage} = T_{charging} \tag{3.6}$$

$$f_{osc} = 1/T_{delay} = \frac{I_{cap}}{CV_{cap}} \tag{3.7}$$

It can be inferred from Eq.(3.7) that the frequency of the proposed oscillator is independent of supply voltage. The temperature variations that impact the term V_{cap} are compensated by proper sizing of transistor M3 and the process variations are compensated by varying the capacitor charging current I_{cap} across different process corners.

3.2 Latch Based Oscillator

Fig.(3.2) shows the schematic of proposed oscillator. The architecture of oscillator block consists of cross coupled latch having transistors M1-M4 and equal sized gate capacitors M0 and M5. The reference current I_{ref}, is provided by an on-chip reference current generator, which provides constant current across PVT variations. The transistors M16-M25 represents the current mirror transistors that are used to generate the I_{bias}, I_{curr1} and I_{curr2} from reference current. The current I_{bias} is used to charge the cross coupled latch output nodes 'A' and 'B' during the oscillator operation. Moreover, the currents I_{curr1} and I_{curr2} are equal magnitude currents that are used to charge the gate capacitors of transistors M5 and M0 present at node 'AN' and 'BN' respectively. The transistors M6-M13 acts as the switches used for charging and discharging of gate capacitors. V_{dd} and EN represents the supply voltage and enable signal of oscillator block. MOS capacitors present at the node 'AN' and 'BN' are biased in either strong inversion region or strong accumulation region to get the constant capacitance value.

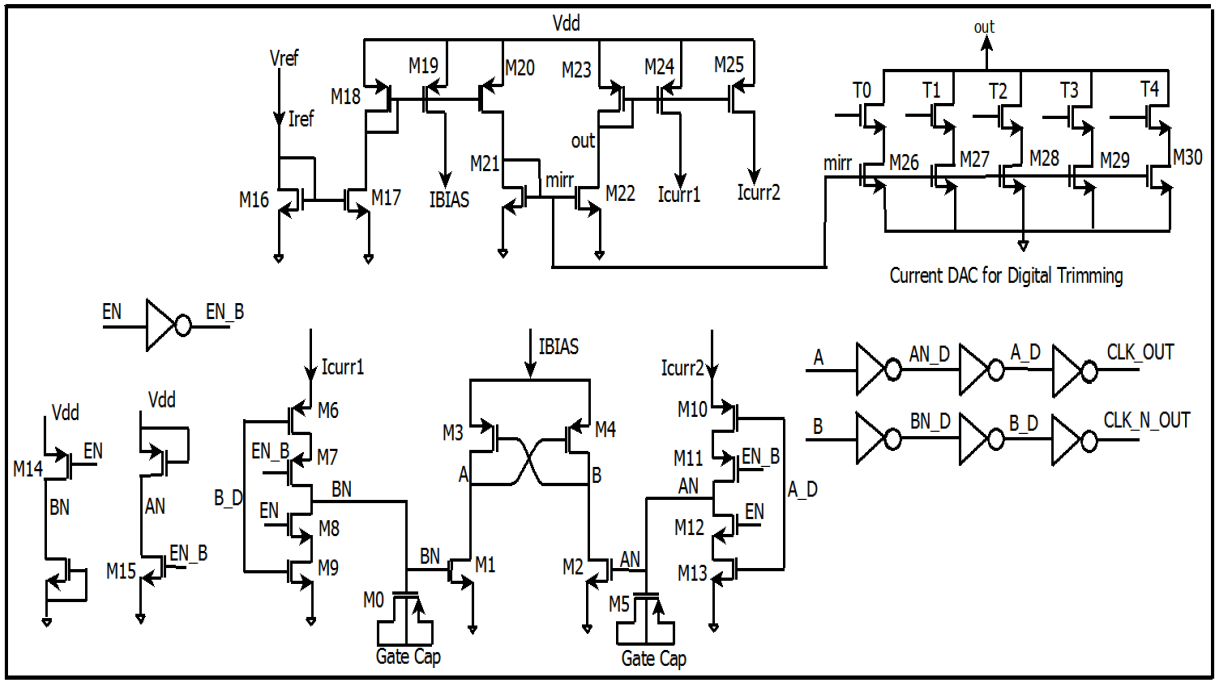

Figure 3.2: Schematic diagram of proposed Latch based oscillator

3.2.1 Operation Principle

Initially enable signal (EN) = 0, M14 and M15 turns on and provides BN = V_{dd} and AN = 0. Latch stores value of A_D = 0 and B_D = V_{dd}. These node voltages remains fixed until enable signal goes high to V_{dd}. Fig.(3.3) represents charging and discharging path for capacitors when enable signal rises to V_{dd}. The switching transistors M8 and M9 turns on and discharges

the capacitor present at node 'BN' that turns off transistor M1. At same instant, transistors M10 and M11 turns on and I_{curr2} charges the capacitor present at node 'AN'. The voltage at node 'AN' rises linearly with time, since constant current charges a fixed capacitor value. As the voltage of node 'AN' exceeds the threshold voltage of M4, it turns on and pulls the node B to ground and node A starts rising. The final value stored in latch will be A_D = V_{dd} and B_D = 0, which is exactly opposite of initially stored values. This change of state changes the charging and discharging path as shown in Fig.(3.4).

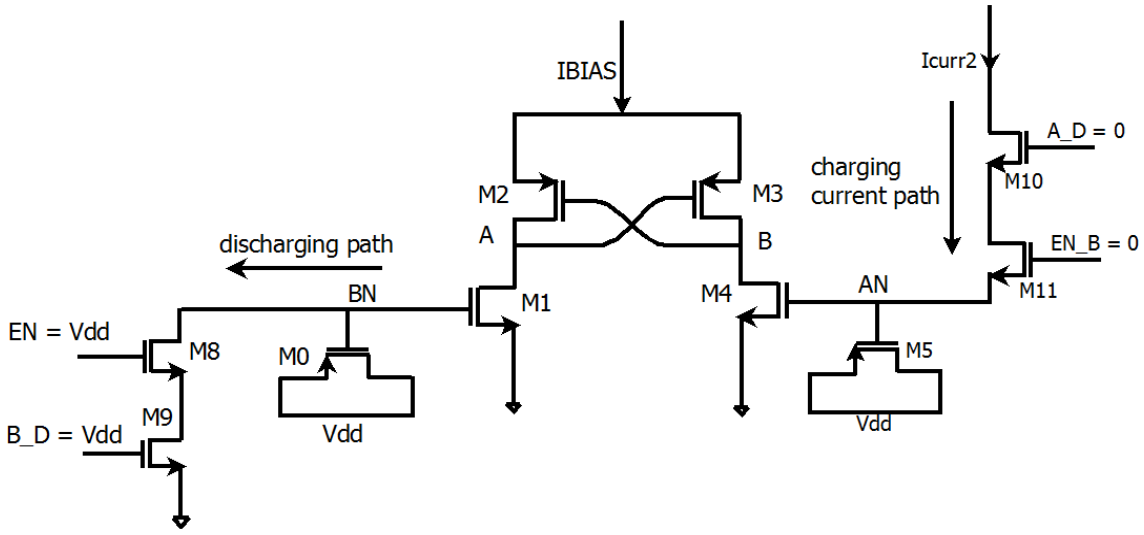

Figure 3.3: Operation of oscillator when A_D = 0 and B_D = V_{dd}

At this instant, capacitor at node 'BN' charges by I_{curr1} through M6 and M7 and capacitor at node 'AN' discharges by M12 and M13. Charging occurs until voltage at node 'BN' exceeds the threshold voltage of M1, which forces the latch to change its state. This charging and discharging of nodes 'AN' and 'BN' keeps on going till enable signal is high.

The output of oscillator CLK_OUT and CLK_OUT_N have almost 50% duty cycle because of symmetric structure of oscillator and also consumes lesser power, as the small magnitude of current is used in latch and charging of capacitors. The proposed design do not requires any poly resistances as used in conventional relaxation oscillators, hence it will consume much lesser area and provides much better stability across different process corners. The charging of capacitor at node 'AN' or 'BN' by constant current I_{curr1} or I_{curr2} occurs linearly with time with help of M6-M7 or M10-11 and discharging occurs instantly as the capacitor is connected to ground node directly during discharge path either by M8-M9 or M12-M13.

3.2.2 Principle of Temperature Variation Compensation

The principle of temperature compensation employed in this design utilizes the complementary to absolute temperature (CTAT) behaviour of threshold voltage and proportional to absolute

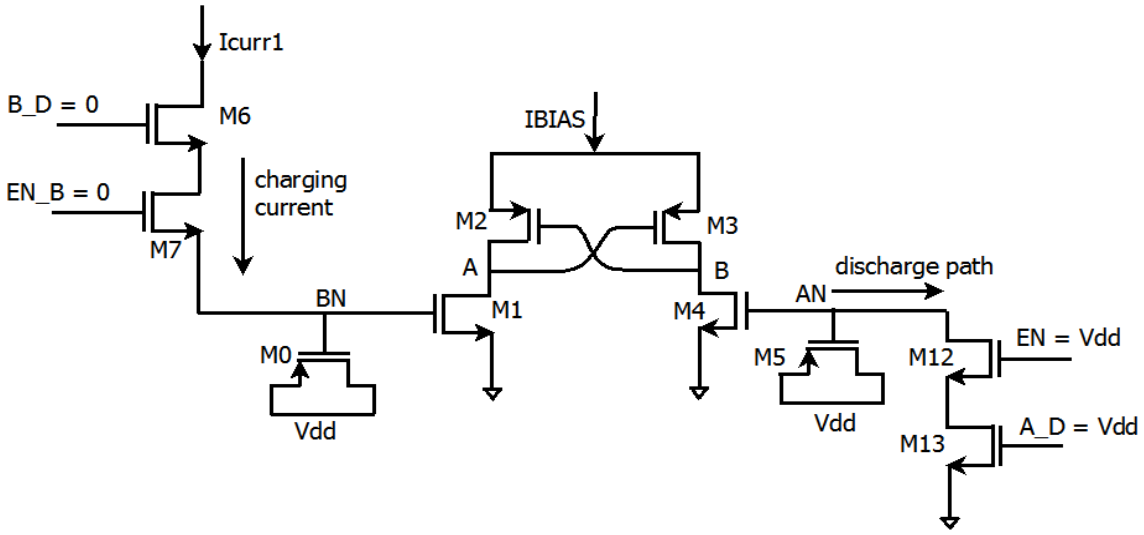

Figure 3.4: Operation of oscillator when A_D = V_{dd} and B_D = 0

temperature (PTAT) behaviour of overdrive voltage of transistor [8]. Frequency of oscillator is governed by the charging time of the capacitors hence charging time has to remain constant across operating range of temperature. The gate capacitors of M0 or M5 will be charged till their voltage level reaches the threshold voltage of either M1 or M4. This charging time can be written as:

$$T_{charging} = \frac{C.V_{GSM1}}{I} \tag{3.8}$$

Here I, denotes the charging current either I_{curr1} or I_{curr2} and C, denotes total capacitance at node either 'AN' or 'BN'. In Eq.(3.8), capacitance (C) and charging current (I) are constant across temperature variations but V_{GSM1} is a temperature dependent term and expressed as:

$$V_{GSM1} = V_{THM1} + \sqrt{\frac{2.I_{bias}}{\mu_n.C_{ox}.(\frac{W}{L})_1}} \tag{3.9}$$

In Eq.(3.9), threshold voltage exhibits negative temperature coefficient. The aspect ratios of transistor M1 and M4 decides the positive temperature coefficient of overdrive voltage. If negative temperature coefficient of threshold voltage is exactly equal to positive temperature coefficient of overdrive voltage then V_{GSM1} will remain constant across operating range of temperature. The total time period of oscillation is given by:

$$T_{OSC} = 2 \times T_{charging} = \frac{2CV_{GSM1}}{I} \tag{3.10}$$

$$f_{osc} = \frac{1}{T_{OSC}} = \frac{I}{2CV_{GSM1}} \tag{3.11}$$

3.2.3 Principle of Process Variation Compensation

From Eq.(3.9), it can be inferred that V_{GSM1} is process dependent parameter because of its dependence on threshold voltage and process parameters ($\mu_n C_{ox}$). Hence it can be stated that numerator of Eq.(3.10) will vary with process variations. The denominator of Eq.(3.10) can be scaled in same proportion of numerator to keep T_{OSC} constant across different process corners. It means current I_{curr1} and I_{curr2} need to be scaled according to the process corners. In order to achieve this trimming bits are introduced in the design to vary the magnitude of current. The different combinations of trimming bits are stored in on-chip digital controller, that helps in achieving the correct oscillation frequency during calibration of the oscillator. As shown in Fig.(3.5), trimming bits transistors T0-T4 are used to control the overall width of transistor M22.

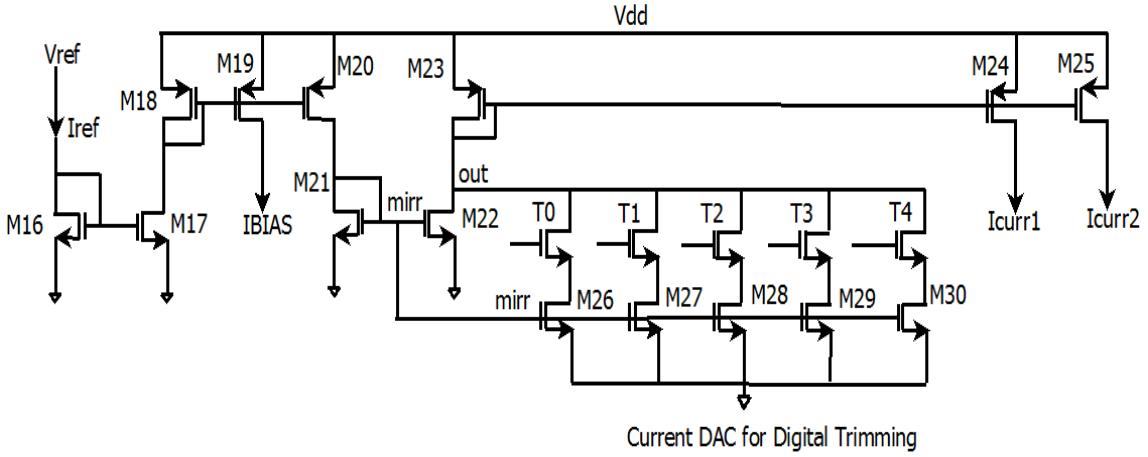

Figure 3.5: Digital trimming bits T0-T4 used to control the width of transistor M22

This modulation in width changes the amount of current flowing through it, hence decides the magnitude of capacitor's charging current I_{curr1} and I_{curr2}. In the proposed oscillator, '5' bit digital trimming is used for obtaining 2^5 different current levels, which are used to generate the target frequency of oscillation, according to the different process corner.

3.2.4 Principle of Voltage Variation Compensation

It can be observed from Eq.(3.11), that the frequency of oscillation is independent of supply voltage variations. The parameters present in Eq.(3.11) I, C and V_{GSM1} all are supply voltage independent terms. However, small frequency variations can be introduced due to supply voltage variations because few inverters are present in the design, whose delay may vary with supply voltage variations. Although proposed design is inherently immune to small voltage variations, but for wide supply voltage variations, on-chip voltage regulator [10] can be integrated in the design to generate stable regulated supply voltage across PVT variations.

Table 3.1: Threshold voltage of NMOS and PMOS at -40℃ and 150℃ for different process corners in BCD9S technology

Process	NMOS	PMOS	V_{TN}(mV) at T=-40℃	V_{TP}(mV) at T=-40℃	V_{TN}(mV) at T=150℃	V_{TP}(mV) at T=150℃
MAX	FAST	FAST	498.41	-426.41	361.62	-267.74
MIN	SLOW	SLOW	651.7	-594.32	507.09	-435.78
TYP	TYP	TYP	584.59	-522.39	442.79	-363.81
NFPS	FAST	SLOW	498.41	-594.32	361.62	-435.78
NSPF	SLOW	FAST	651.7	-426.18	507.09	-267.74

3.3 Simulation Results

The proposed oscillators are designed in $0.11\mu m$ BCD 9S (Bipolar CMOS DMOS) ST Microelectronics technology and simulated in Mentor Graphics ELDO simulator. The design is simulated for five process corners MAX, MIN, TYP, NFPS and NSPF across -40℃ to 150℃ operating temperature. Table(3.1) represents the variation of threshold voltage across different process corners at -40℃ and 150℃.

3.3.1 Ring Oscillator Results

The simulation of proposed PVT compensated ring oscillator are performed on post layout generated netlist, extracted using C_{max} strategy. The layout of ring oscillator is shown in Fig.(3.6) and it requires an area of $320\mu m^2$.

To have an oscillation frequency of 10 MHz, the value of capacitor is decided in a manner to get an approximate delay of 50ns from the first stage. The magnitude of gate capacitor introduced due to M18 varies with the voltage at 'CAP' node. The gate capacitance variation of transistor M18 with the variation in 'CAP' node is shown in Fig.(3.7) and it can be observed that the capacitance value will remain almost constant only if M18 will be biased in inversion region.

The sizing of transistor M3 in ring oscillator decides the accuracy of temperature compensation. The eq.(3.2) suggests that charging time will remain fixed across temperature variations only if V_{GSM3} remains fixed across temperature variations. The Fig.(3.8) represents the temperature variation of V_{GSM3} for different value of channel length of transistor M3.

The transient behaviour of different nodes present in ring oscillator is shown in Fig.(3.9). It can be observed that the voltage across 'CAP' node rise linearly with time during charging. The inverter stages biased at supply voltage provides rail-to-rail output signals. The output of ring oscillator 'NA1' and 'NA2' do not have 50% duty cycle, that's why D flip-flop is used to generate the output clock (VCLK) having equal on time and off time duration.

The 'CAP' node will vary from -4.7mV to 695mV during the charging period. It can be observed

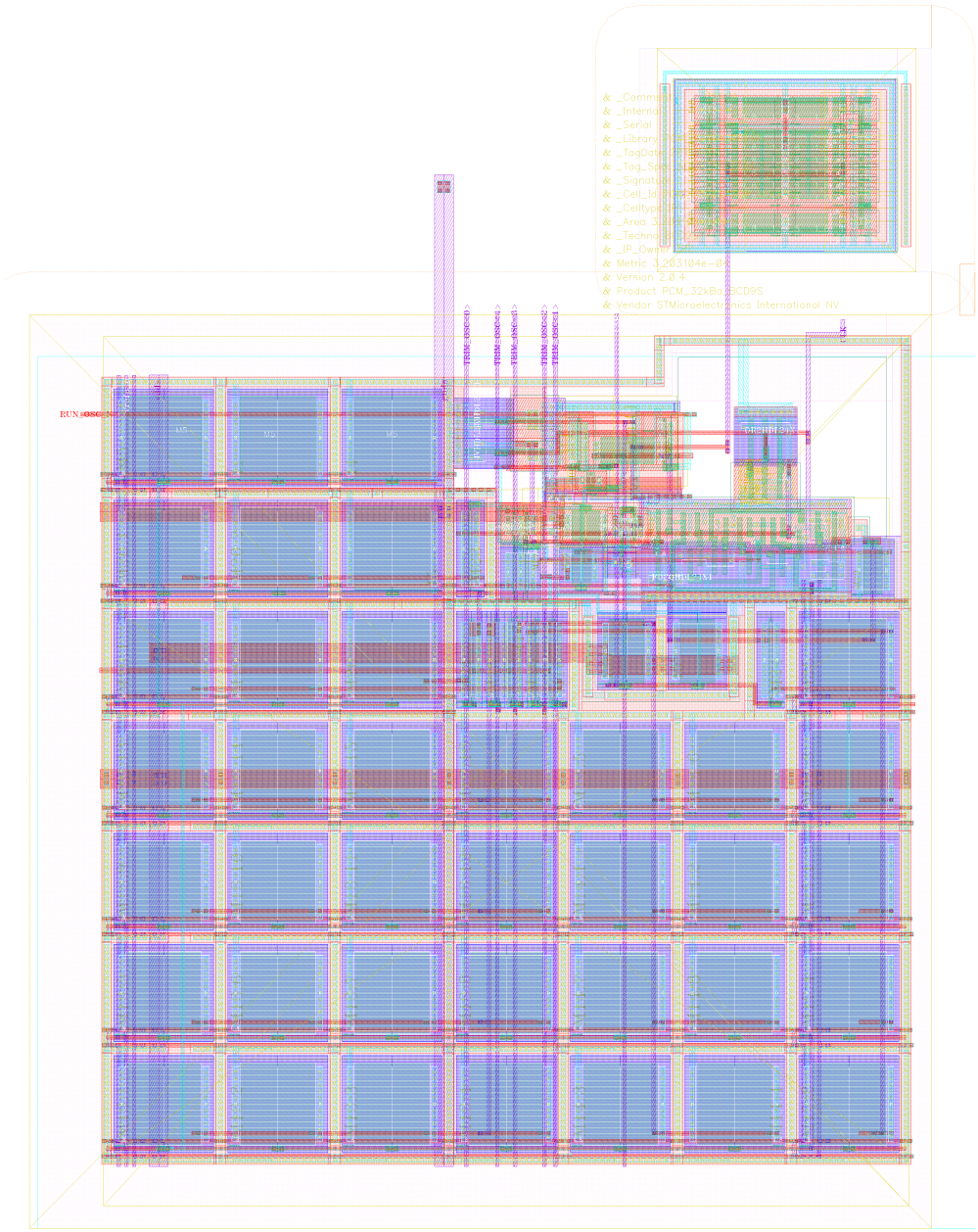

Figure 3.6: Layout of proposed PVT compensated Ring Oscillator

from Fig.(3.7) that during this variation of 'CAP' node, the transistor M18 will exhibits gate capacitance of almost constant value of 75fF. The transient behaviour of capacitor during the charging and discharging period is shown in Fig.(3.10). It is observed that gate capacitor of M18 will exhibit insignificant variation due to variation in 'CAP' node and its value can be approximated as a constant value during operation of oscillator.

The frequency of oscillation remains temperature compensated across process variations as shown in Fig.(3.11). The maximum frequency variation of ±18% is observed across different process

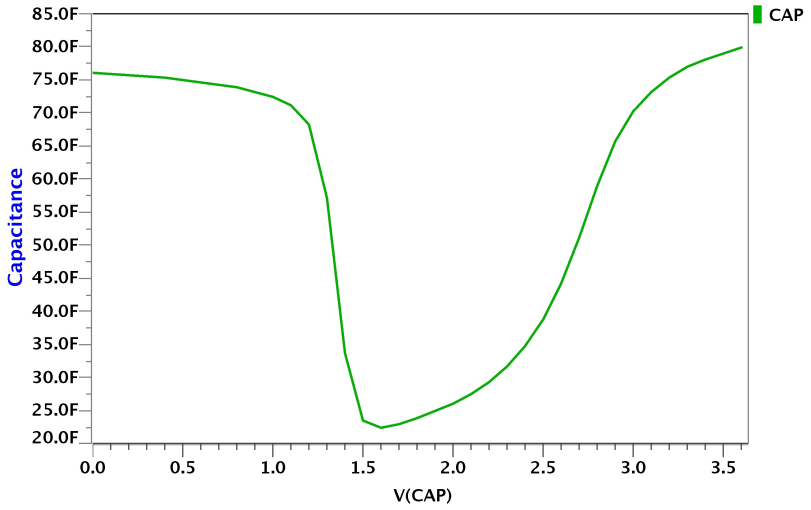

Figure 3.7: Variation of gate capacitor of M18 with variation in CAP node

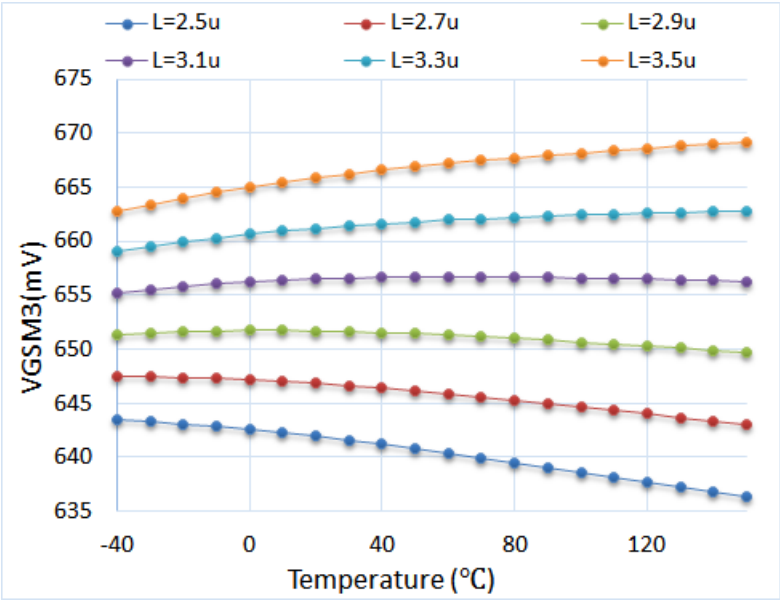

Figure 3.8: Variation of V_{GSM3} across temperature range of -40°C to 150°C for different aspect ratio of M3.

corners.

The trimming bits are used to configure the charging current of capacitor according to the process corner and try to correct the oscillation frequency. It is observed from Fig.(3.12), that in TYP, MIN, MAX, NFPS and NSPF process corners, the frequency variation of ±0.7%, ±2.25%, ±0.75%, ±0.45% and ±1% is exhibited by oscillator respectively.

Fig.(3.13), shows that for ±10% variation in supply voltage of 1.8V, the frequency variation

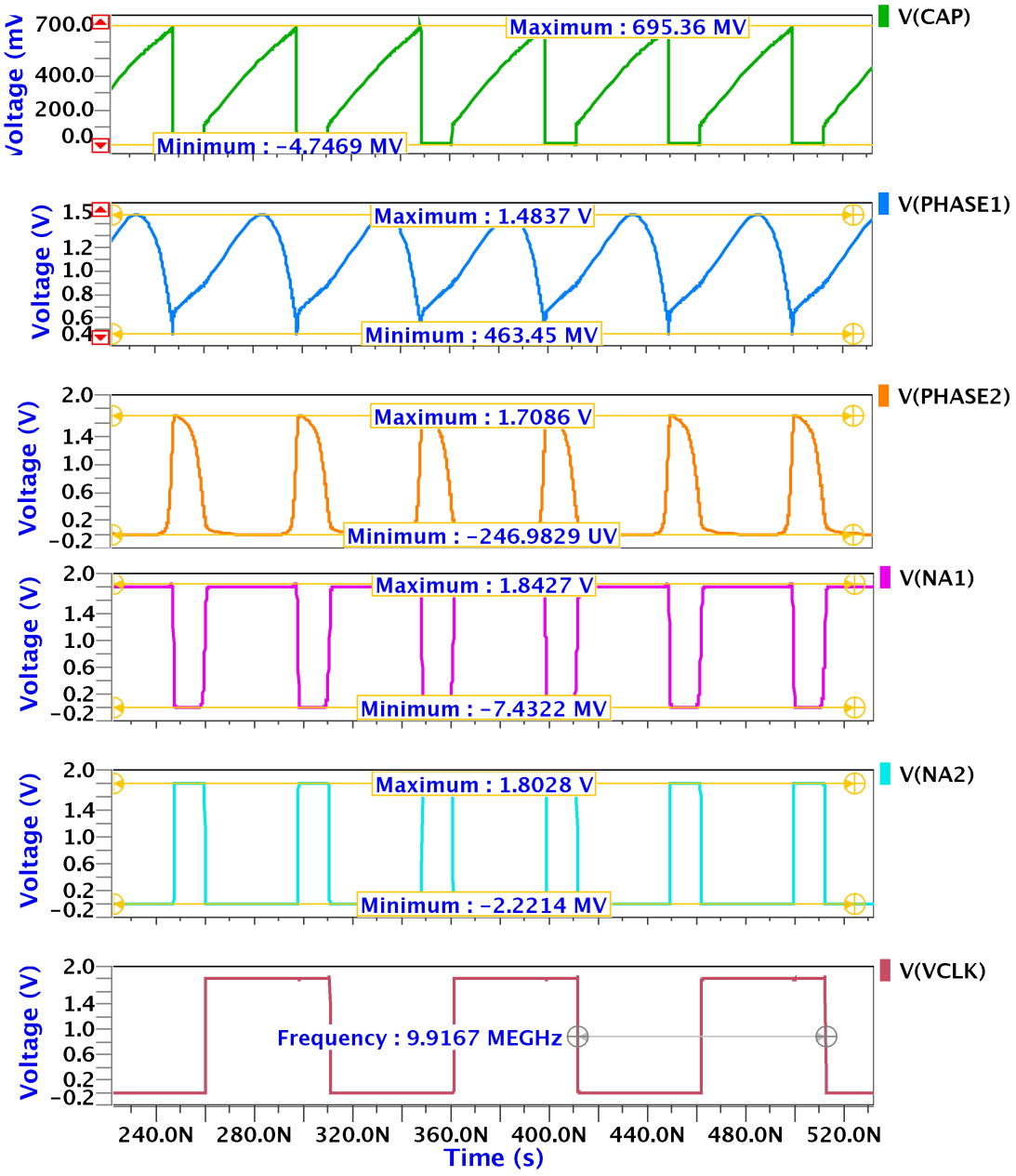

Figure 3.9: Transient behaviour of different node voltages of ring oscillator.

of ±3.1% is obtained. This frequency variation is due to the variation in delay introduced by inverter stages present in the loop biased at supply voltage and the variation in delay of D flip flop due to supply voltage. Moreover, the frequency variations can be reduced by generating a stable supply using on-chip voltage regulator but it will impact total on-chip area as well as the power consumption.

The simulation performed across different process corners provides much pessimistic results as it considers maximum process parameters variations. Monte Carlo simulations are also performed

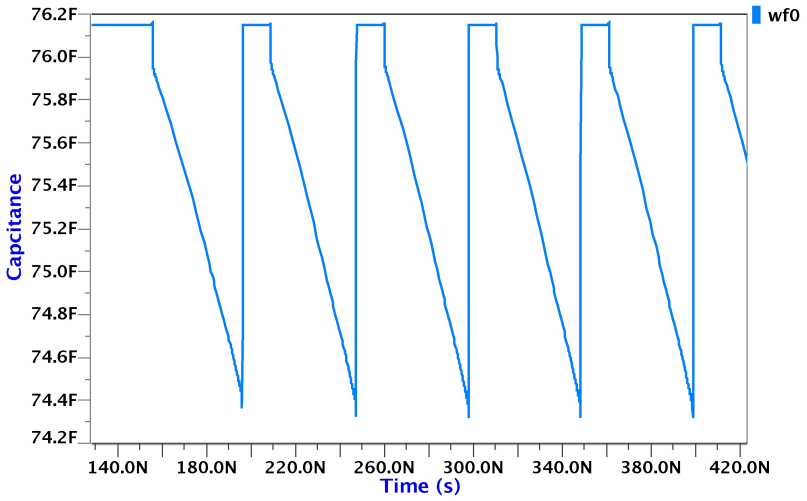

Figure 3.10: Transient behaviour of the gate capacitor of transistor M18.

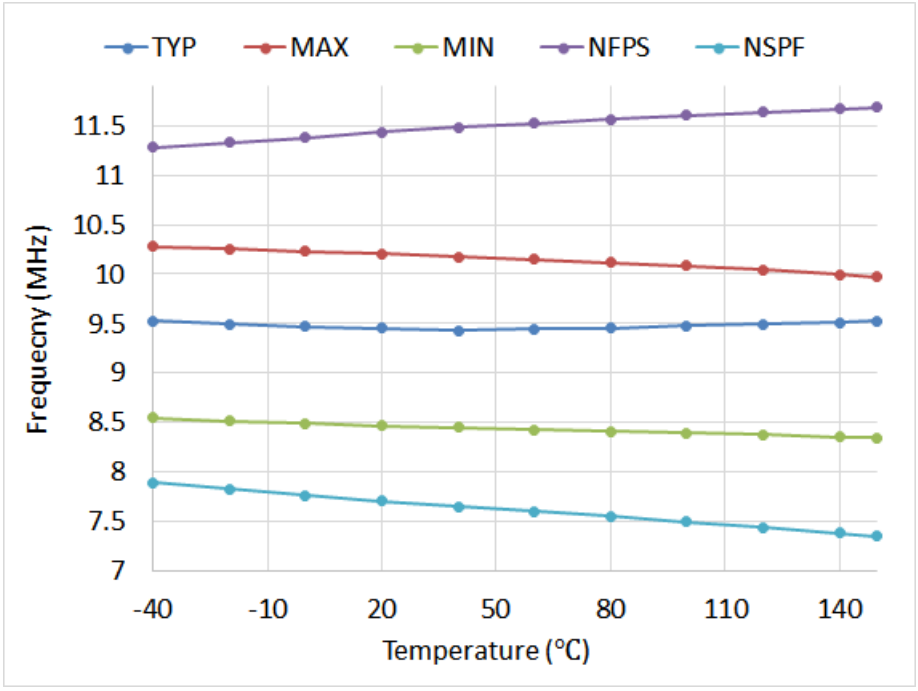

Figure 3.11: Variation of frequency across different process corners from -40℃ to 150℃ without using trimming bits

to incorporate the random mismatches and process variations of sensitive devices. Fig.(3.9), Fig.(3.10) and Fig.(3.11) represents Monte Carlo simulation results performed over 5000 samples at -40℃, 27℃ and 150℃ respectively in statistical corner. Table(3.2), shows the parameters observed in Monte Carlo simulations.

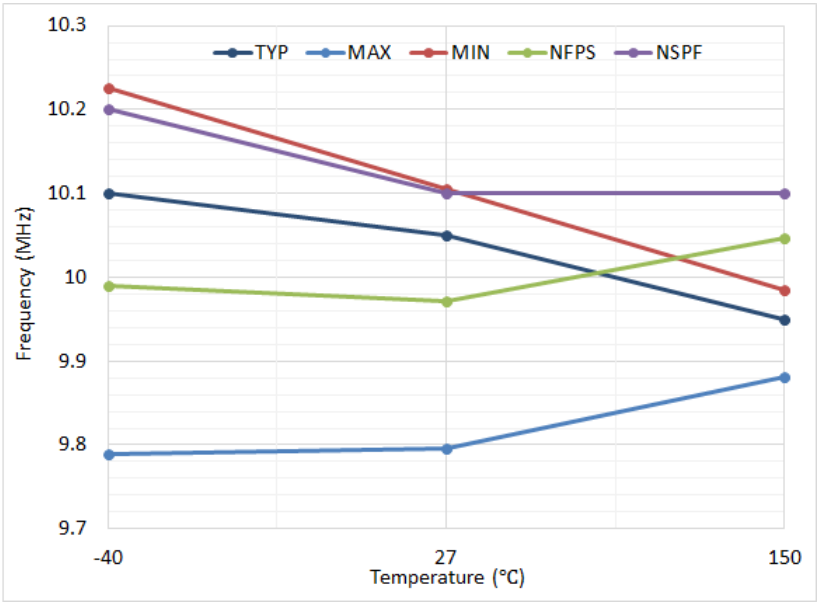

Figure 3.12: Variation of frequency across different process corners for temperature range from -40℃ to 150℃ using digital trimming bits.

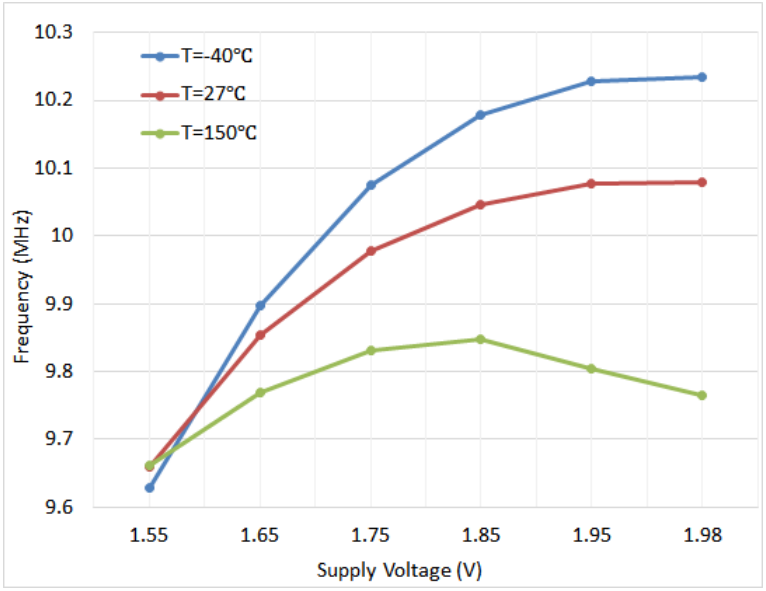

Figure 3.13: Variation of frequency across supply voltage ($1.8V \pm 10\%$) variations for typical process corner at -40℃, 27℃and 150℃.

3.3.2 Latch based Oscillator Results

As discussed in previous section, aspect ratio of transistors M1 and M4 decides the accuracy of temperature compensation in latch based oscillator. Fig.(3.17) represents the variation of V_{GSM1} for different values of channel length across -40℃ to 150 ℃. At W = $3\mu m$, L = $6\mu m$ and I_{bias} = $5\mu A$, V_{GSM1} exhibits better temperature compensated behaviour.

Table 3.2: Parameters obtained from Ring Oscillator Monte Carlo simulation

Temperature	-40℃	27℃	150℃
Mean (μ) MHz	10.01496	10.1323	9.84257
Standard Deviation (σ) MHz	0.13061	0.1598	0.10277
Coefficient of Variation (%)	1.30	1.58	1.04
($\mu \pm 3\sigma$) Range (MHz)	9.55-10.45	9.56-10.66	9.53-10.150

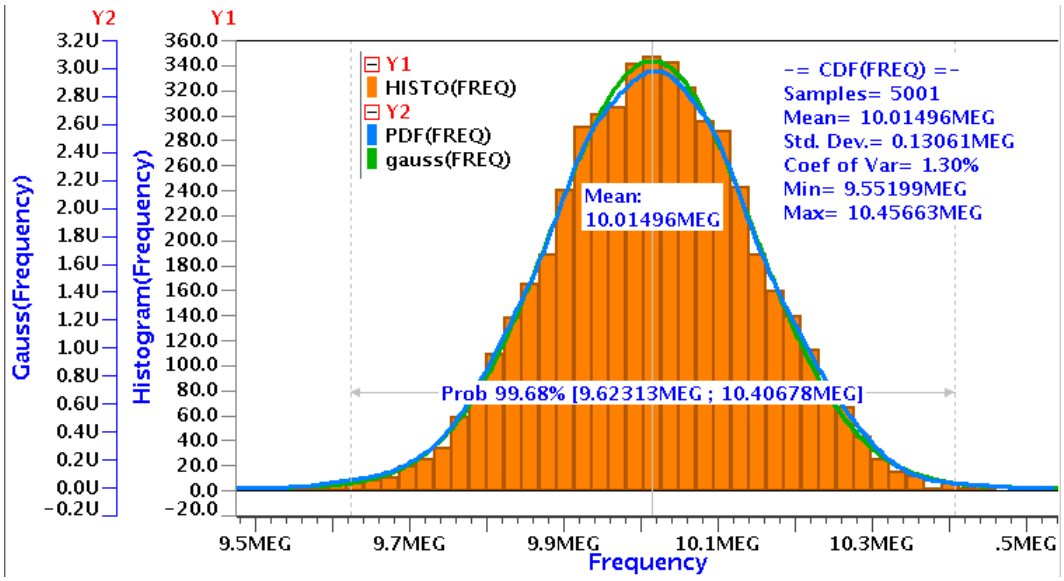

Figure 3.14: Monte Carlo simulation results at temperature= -40℃.

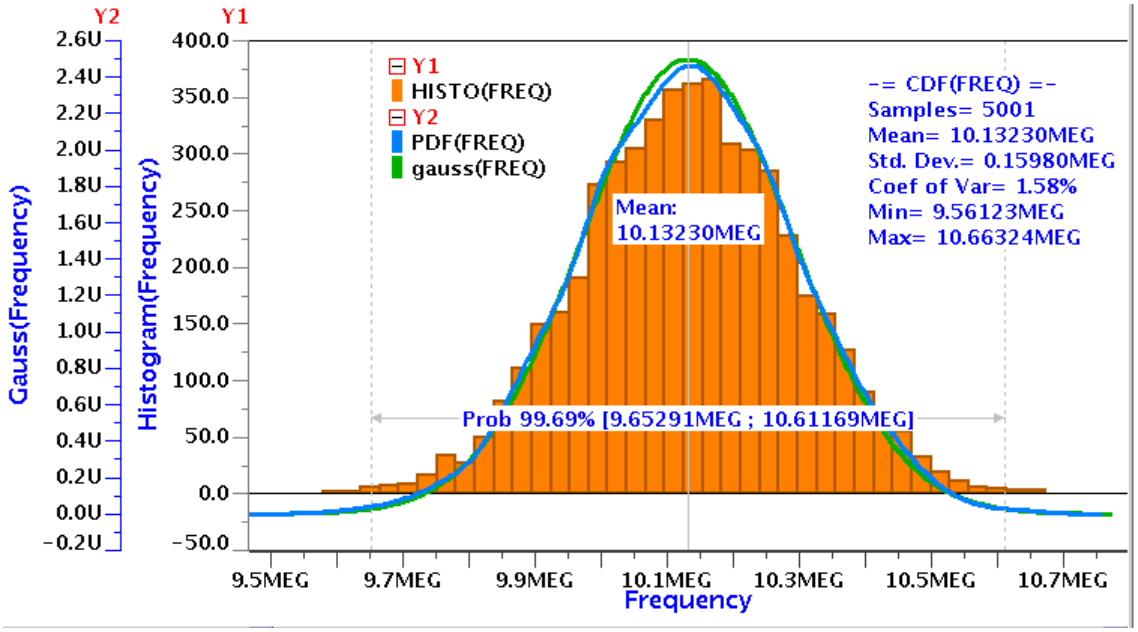

Figure 3.15: Monte Carlo simulation results at temperature= 27℃.

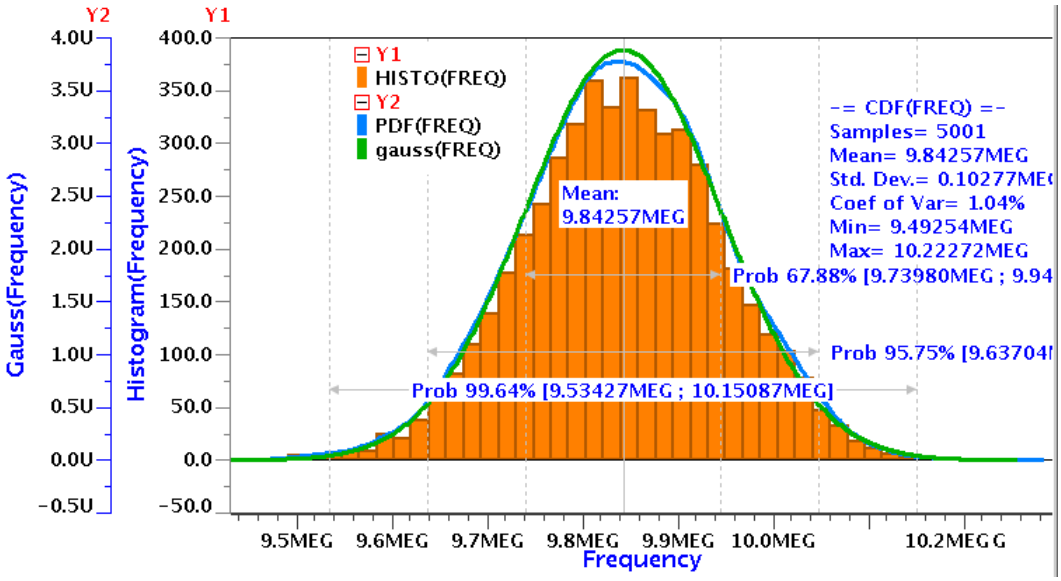

Figure 3.16: Monte Carlo simulation results at temperature= 150℃.

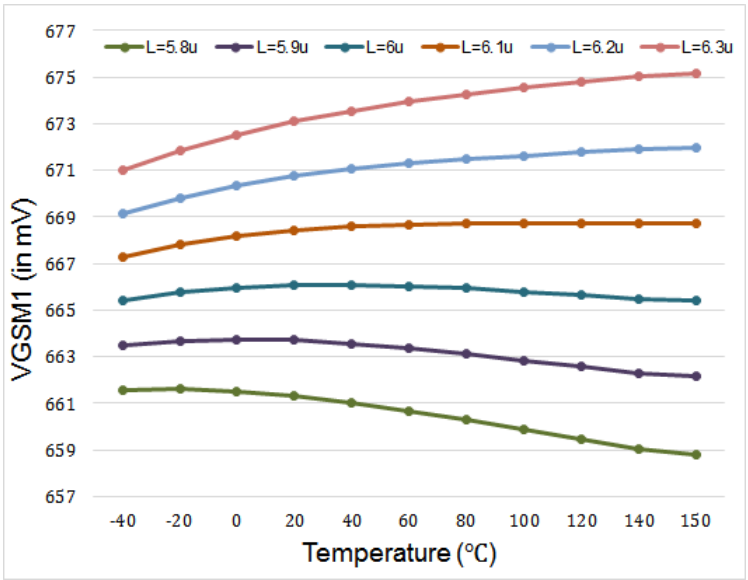

Figure 3.17: Variation of V_{GSM1} for different channel length of M1 at $I_{bias} = 5\mu A$ and W = $3\mu m$.

Fig.(3.18) represents the behaviour of threshold voltage and overdrive voltage for W = 3 μm and L = 6 μm. The threshold voltage exhibits negative temperature coefficient of -0.859mV/℃ and overdrive voltage exhibits positive temperature coefficient of 0.85957mV/℃.

The variation in magnitude of gate capacitor of M0 and M5 with variation in gate voltage is shown in Fig.(3.19). The transistors M0 and M5 are equal sized transistor used as a gate capacitor at nodes BN and AN respectively.

The transient behaviour of internal nodes of latch based oscillator is represented in Fig.(3.20).

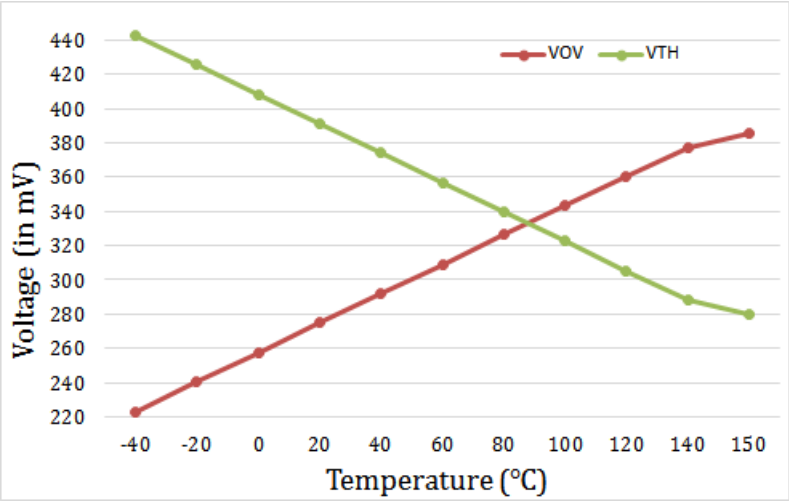

Figure 3.18: Variation of threshold voltage and overdrive voltage of M1 across -40°C to 150°C

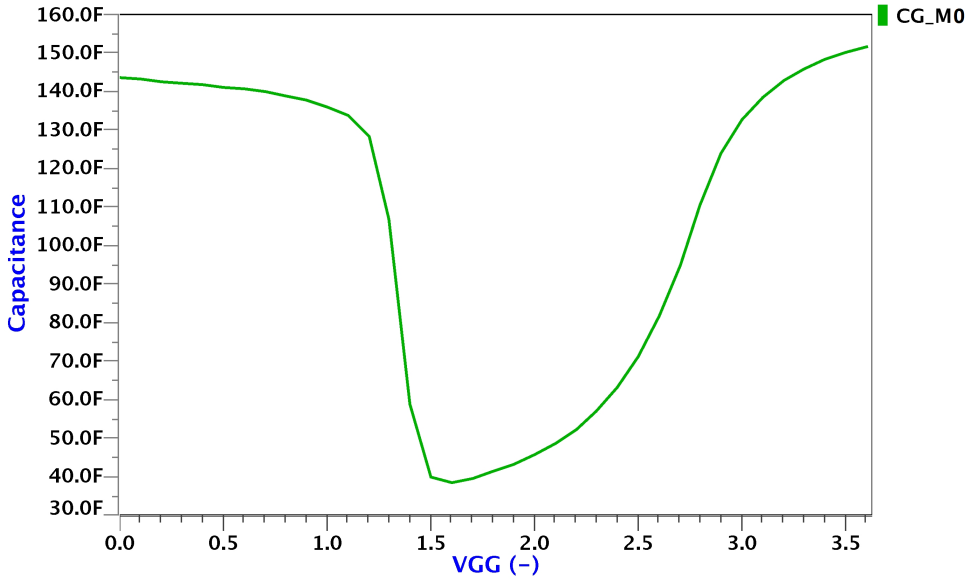

Figure 3.19: Variation of gate capacitor of M0 or M5 with variation in BN or AN nodes respectively.

The voltage at capacitive nodes 'AN' and 'BN' increases linearly with time during the charging. From Fig.(3.20), it is observed that voltage at node AN varies from -17mV to 729mV and node voltage at BN varies from -17mV to 726mV. The gate capacitor of M0 and M5 will exhibit almost constant capacitance value, during this voltage range, since M0 and M5 will be operated in strong inversion region.

The transient behaviour of gate capacitance during operation of oscillator is attached in Fig.(3.21). Fig.(3.22) represents the simulation results of oscillator without digital trimming. The frequency variations introduced in oscillation frequency across all process corners from -40°C to 150°C is

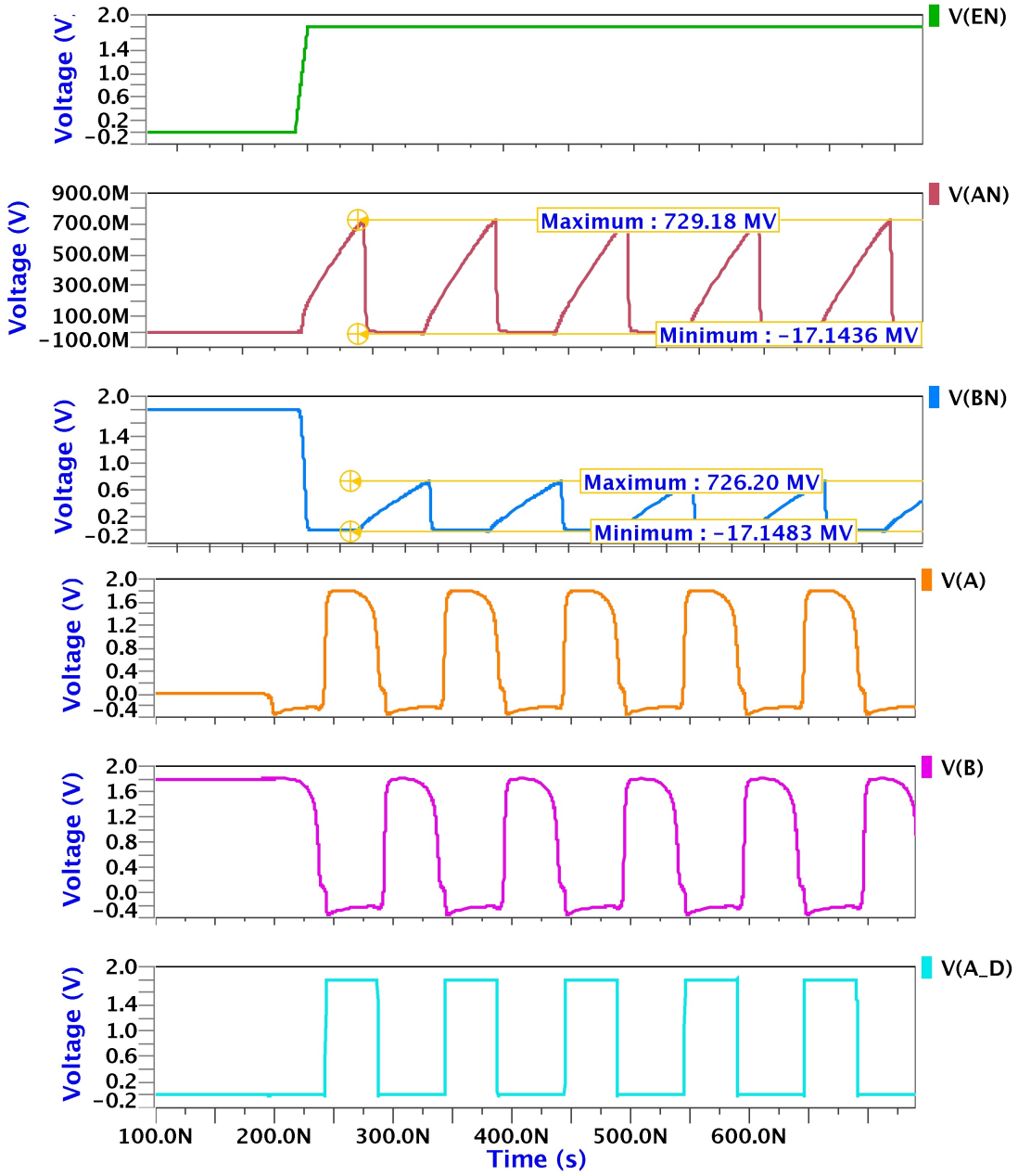

Figure 3.20: Transient behaviour of various nodes of Latch based oscillator.

±16%. Moreover, the design exhibits the inherent temperature compensated behaviour. As discussed in previous section, the concept of digital trimming improves the frequency correction capability across process variations and minimizes the frequency variations. Fig.(3.23) represents the variation of frequency across 32 trimming bit combinations for different process corners at 27°C. It can be observed that in all process corners, oscillation frequency of 10 MHz can be achieved by selecting correct combination of trimming code.

Fig.(3.24) represents the variation of oscillation frequency across ±10% variations in 1.8V supply

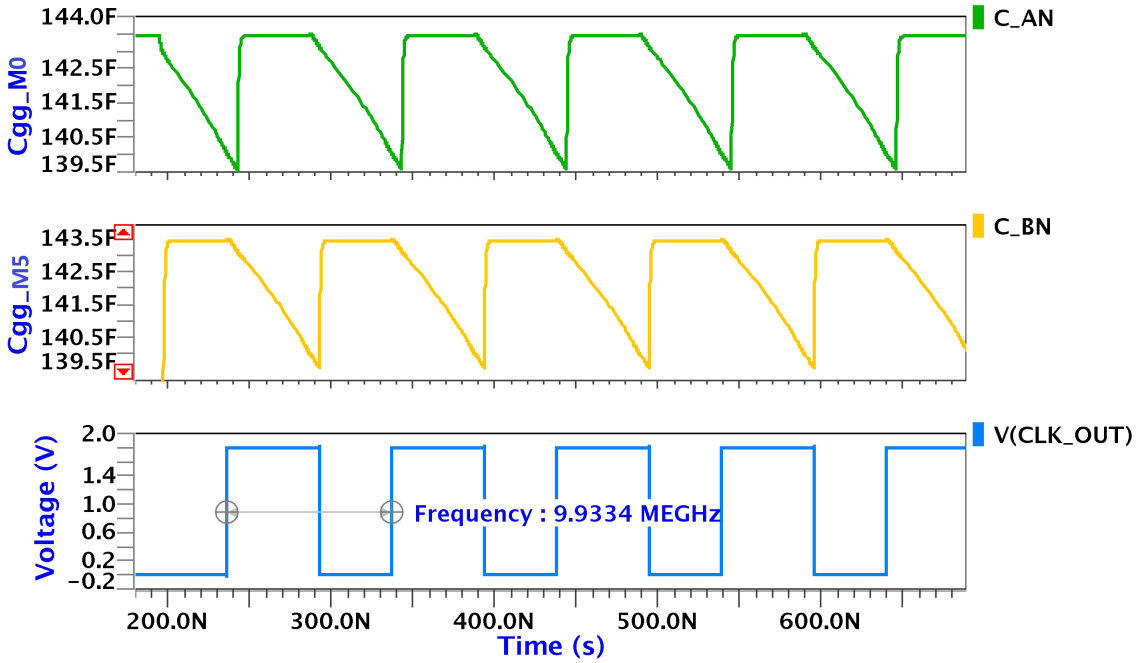

Figure 3.21: Transient behaviour of gate capacitance of M0 and M5 during operation of oscillator.

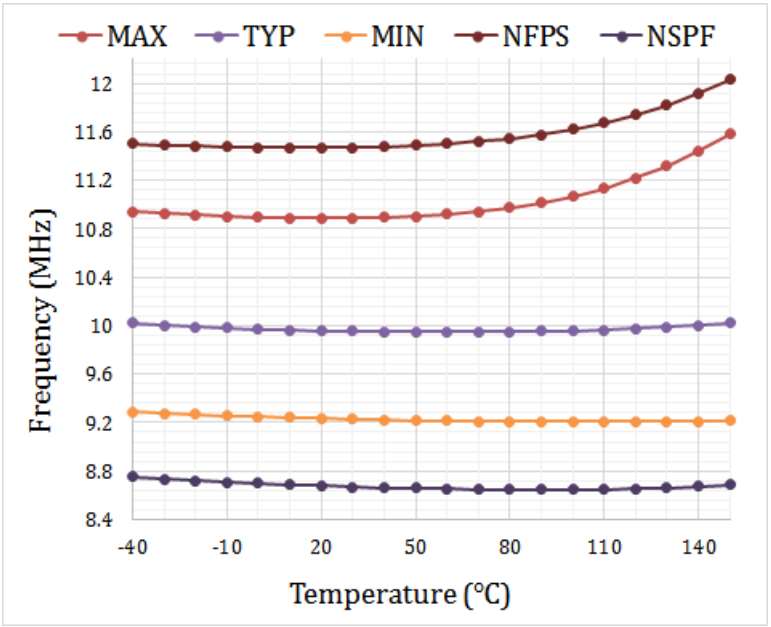

Figure 3.22: Frequency variation for different process corners across -40°C to 150°C without digital trimming

voltage for typical process corner. Frequency variations of ±1.65% are observed in simulation, which is due to the variation in delay of inverters used in the design. However, variation due to supply voltage can be compensated by incorporating a voltage regulator in design to generate stable regulated supply voltage. The accuracy of oscillator is significantly dependent on the accu-

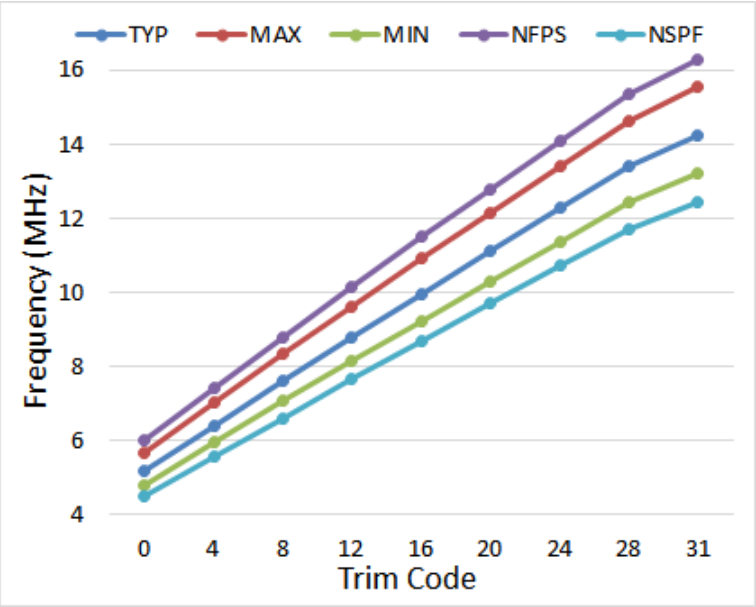

Figure 3.23: Variation of frequency of oscillator across different combination of trim code at all process corners.

racy of reference current. The state-of-the-art reference current generator circuits exhibits some little dependence on temperature and process variations [11] [12] [13]. However, the variation in reference current in this work is considered up to ±5%. Fig.(3.25) represents that for ±5%, variations in reference current, frequency deviation of ±4.09% is observed in simulations. It is due to the fact that oscillation frequency is directly proportional to reference current.

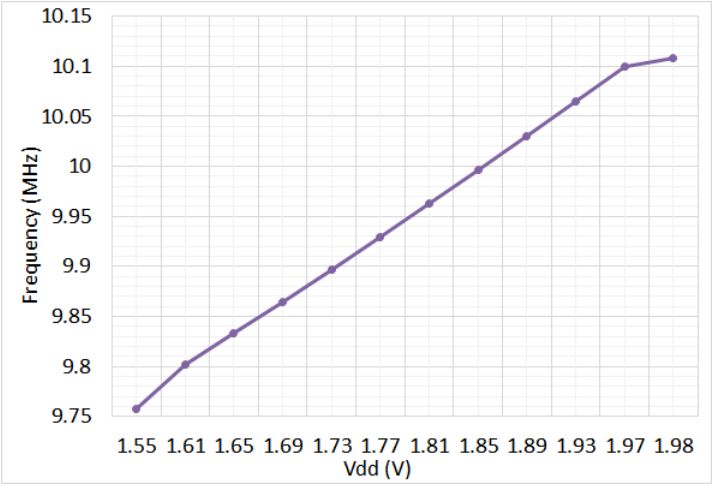

Figure 3.24: Variation of oscillation frequency across ±10% supply voltage variations

Predefined corners represents only rare case events hence provides much pessimistic results than actual results. For much better estimate of overall variations (device mismatch and process variability) and yield analysis, Monte Carlo simulation is performed over different operating tem-

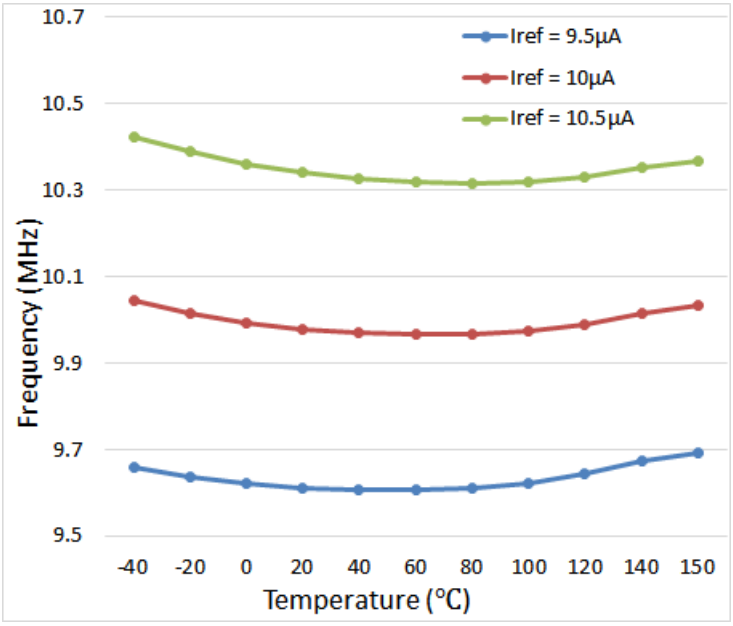

Figure 3.25: Variation of oscillation frequency across ±5% reference current variations

perature. There are various parameters (mean, standard deviation, coefficient of variation etc.) obtained from Monte Carlo simulations that are tabulated in Table(3.3). Fig.(3.26), (3.27) and (3.28) shows Monte Carlo simulation results for -40℃, 27℃ and 150℃ respectively in statistical corner.

Table 3.3: Parameters obtained from Latch based Oscillator Monte Carlo simulation

Temperature	-40℃	27℃	150℃
Mean (μ) MHz	10.04566	9.97563	10.048
Standard Deviation (σ) MHz	0.16224	0.1426	0.236
Coefficient of Variation (%)	1.62	1.43	2.36
($\mu \pm 3\sigma$) Range (MHz)	9.55-10.53	9.54-10.40	9.28-10.91

It has been discussed in previous section that digital trimming technique improves the accuracy of achieving desired frequency of oscillation across different process corners. Fig.(3.29) shows the frequency variations in different process corners using digital trimming bits combination to achieve correct target frequency of 10MHz. It is observed that in typical corner, oscillator exhibits frequency variation of ±0.4%, whereas $\pm 2\%, \pm 1.5\%, \pm 1.5\%$ and ±0.65% in MIN (slow), MAX (fast), NFPS and NSPF process corners. Maximum power of $69\mu W$ is consumed by oscillator in MAX process corner at 150℃.

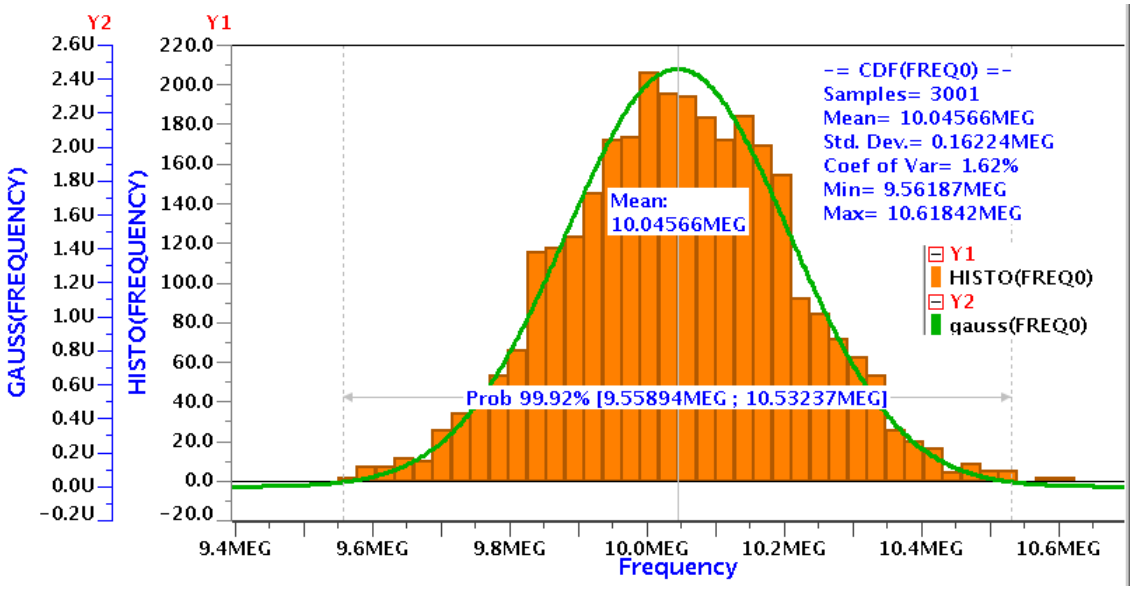

Figure 3.26: Monte Carlo simulation results at temperature= -40°C.

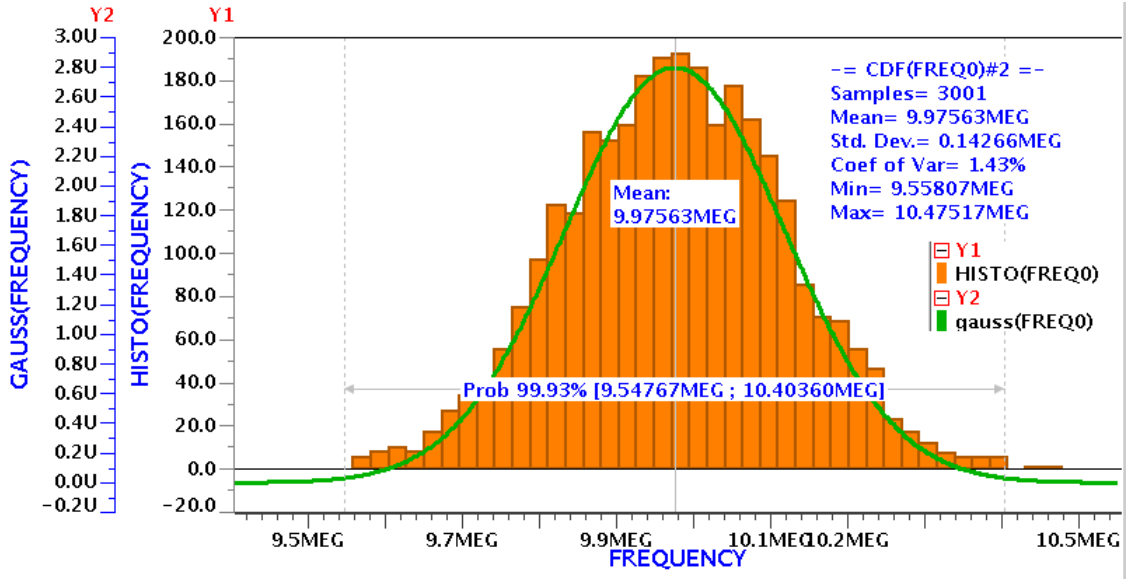

Figure 3.27: Monte Carlo simulation results at temperature= 27°C.

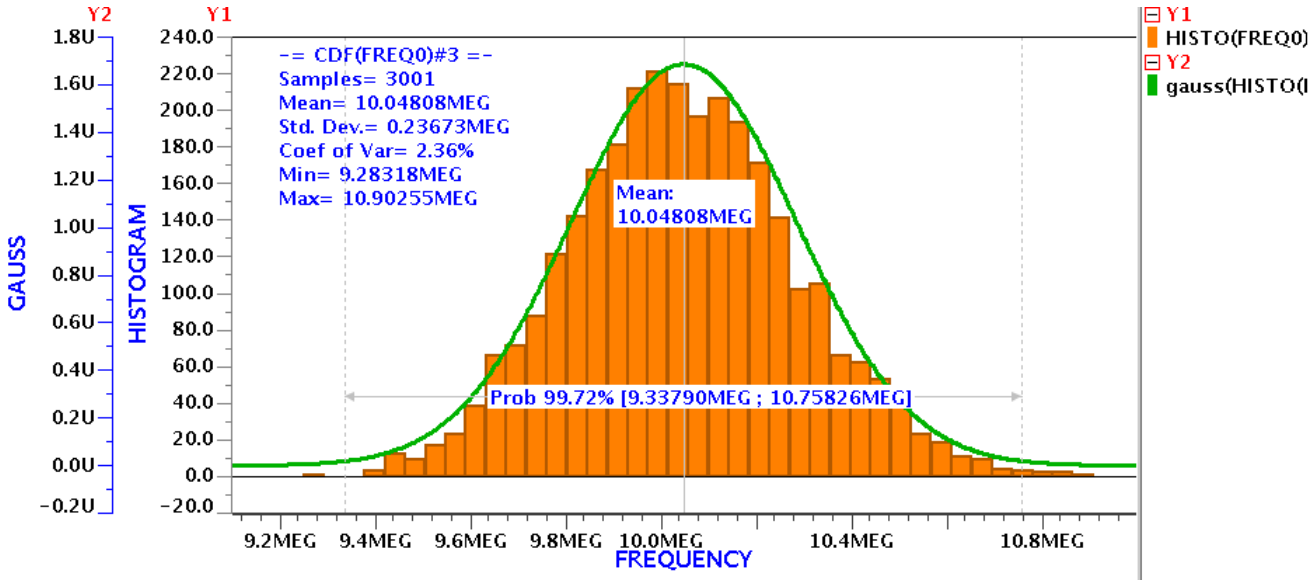

Figure 3.28: Monte Carlo simulation results at temperature= 150°C.

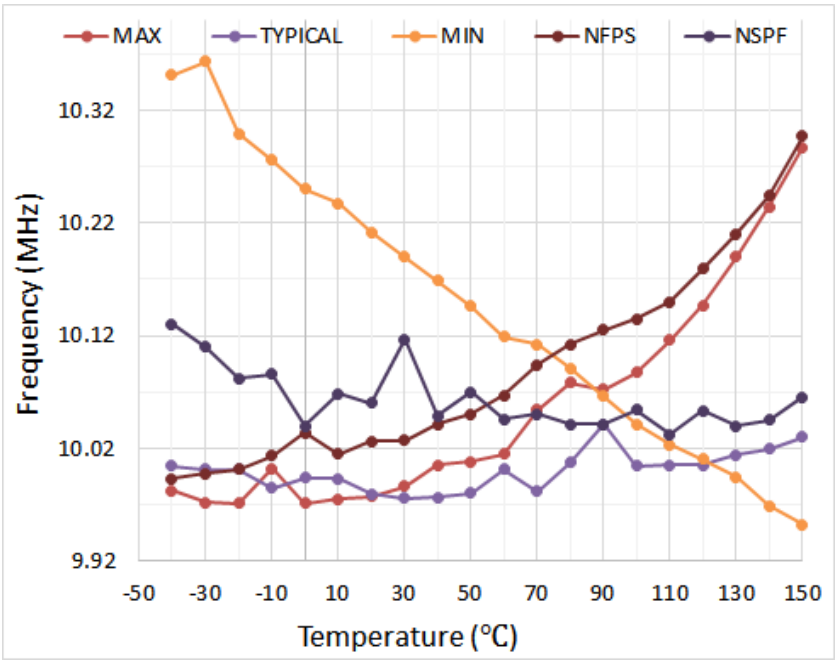

Figure 3.29: Variation of frequency across -40°C to 150°C for different process corners using digital trimming.

Chapter 4

Design of Voltage Regulator

Voltage regulator [10] is used to generate stable supply voltage for oscillator, which is immune to external supply voltage variations. The voltage regulator consists of an operational amplifier in first stage and a pass transistor with feedback resistors in second stage. Fig.(4.1) shows the schematic diagram of conventional voltage regulator integrated with oscillator.

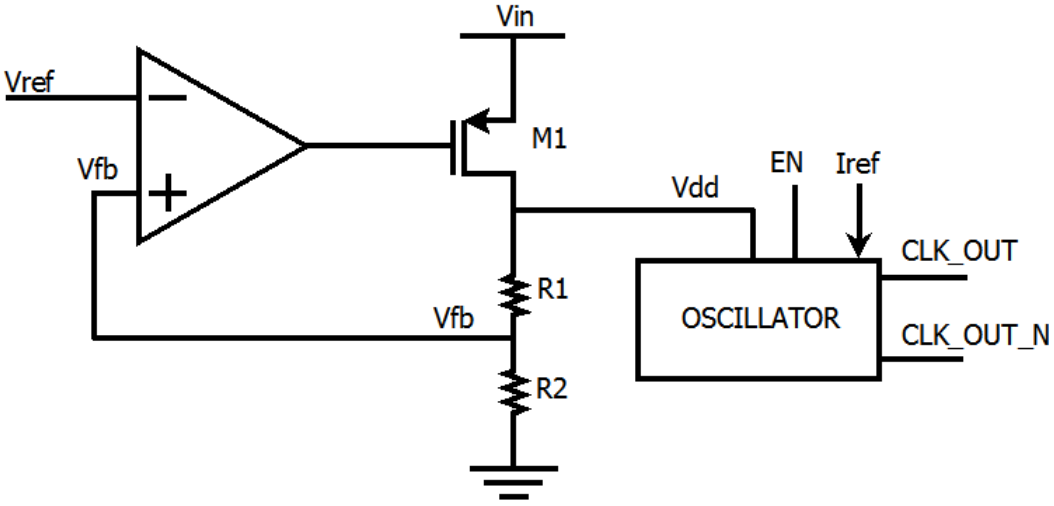

Figure 4.1: Voltage regulator generating the regulated supply (V_{dd}) for Oscillator.

Here, V_{ref} denotes the reference voltage generated by band-gap reference and V_{fb} denotes the feedback voltage applied at positive input of error amplifier. The role of operational amplifier is to minimize the error between the reference voltage and feedback voltage. This error voltage drives the gate of PMOS transistor M1 and tries to keep the regulated output voltage V_{dd} constant irrespective of variation in input voltage V_{in}. The aspect ratio of transistor M1 decides the load current, which can be drawn from the regulator, without varying its output voltage level.

4.1 Fundamental Terms related with Voltage Regulator

- Dropout Voltage: It is the difference between input (V_{in}) and output (V_{dd}) voltage of regulator at that input voltage below which, regulator cannot regulate fixed voltage. If the input voltage goes below a minimum level, then pass transistor operates in a linear region and cannot provide a regulated output.

- Quiescent and Ground Current: It is the minimum current drawn from the input supply to turn on the operational amplifier associated bias circuits when external load current is zero.

- Efficiency: Efficiency can be defined as the ratio of power delivered to output load to the power consumed by the voltage regulator. It can be written as:

$$\eta(\%) = \frac{P_{out}}{P_{in}} = \frac{I_{load}.V_{out}}{(I_{load} + I_{gnd}).V_{in}} \times 100 \tag{4.1}$$

  Here I_{load} denotes the load current drawn from the regulator, V_{out} denotes the output voltage level of regulator, I_{gnd} denotes the additional current drawn from input supply other than load current and V_{in} represents the input voltage levels. To obtain high efficiency, I_{gnd} as well as difference between input and output voltage have to be minimized.

- DC Load Regulation: It is the ability of regulator to maintain the same output voltage level over varying load current conditions.

$$Load\ Regulation = \frac{\triangle V_{out}}{\triangle I_{load}} \tag{4.2}$$

- DC Line Regulation It is the ability of regulator to maintain the fixed output voltage over varying input voltage.

$$Line\ Regulation = \frac{\triangle V_{out}}{\triangle V_{in}} \tag{4.3}$$

- Load Transient Response It is defined as an output voltage variation over step change in load current of the regulator. It is dependent on capacitive load of the regulator, gain-bandwidth of regulator's control loop and slew of load current change. If the output voltage transients are very fast, then loop will not be able to track the variations and ringing can be observed in regulated voltage. The ringing can be viewed as an outcome of poor phase margin of regulator's feedback loop.

- Line Transient Response It is defined as variation in output voltage level of regulator over sudden step change in the input voltage of the regulator. It is also the function of gain-bandwidth product of control loop of the regulator.

- Power Supply Rejection Ratio (PSRR) It is defined as ability of regulator to reject the noise and spurious ripples present in input power supply that can corrupt the output voltage of regulator. It is defined as:

$$PSRR = 20log\frac{\triangle V_{in}}{\triangle V_{out}} \tag{4.4}$$

Here $\triangle V_{in}$ and $\triangle V_{out}$ are supply noise signal present at both input as well as output of the regulator. PSRR is not defined as a single value; it is a frequency dependent term. The error amplifier guarantees the high PSRR for lower frequency ranges.

4.2 Generation of Reference Voltage

Fixed reference voltage for voltage regulator is generated by band-gap reference circuit. Fig.(4.2) shows the schematic diagram of band-gap reference present in [7] [14].

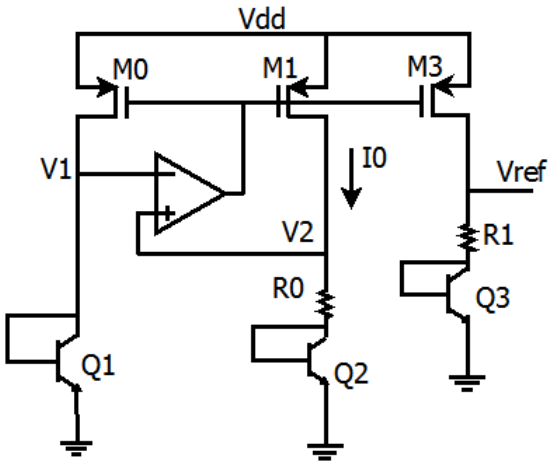

Figure 4.2: Schematic of Band-gap Reference for generation of reference voltage (V_{ref})

The band-gap reference utilizes the CTAT behaviour of base to emitter voltage (V_{be}) and PTAT behaviour of difference between two base to emitter voltages ($V_{be1} - V_{be2}$). The operational amplifier tries to minimize the error between two input nodes. It can be written as:

$$V_1 = V_2 \tag{4.5}$$

$$V_{be1} = V_{be2} + I_o.R_o \tag{4.6}$$

Here V_{be1} and V_{be2} denotes the base-to-emitter voltages of n-p-n transistors Q_1 and Q_2 respectively.

$$I_o = \frac{V_{be1} - V_{be2}}{R_o} \tag{4.7}$$

The collector current I_c in n-p-n transistor can be written as:

$$I_c = I_s exp(\frac{V_{be}}{V_T}) \tag{4.8}$$

Where, I_s is the saturation current and it is proportional to μKTn_i^2 and V_T denotes the threshold voltage of the device. The term V_{be} can be written as:

$$V_{be} = V_T ln(\frac{I_C}{I_S}) \tag{4.9}$$

If Q1 and Q2 have size in the ratio of 1: n, then numerator of Eq.(4.7) can be written as:

$$V_{be1} - V_{be2} = V_T ln(\frac{I_{c1}}{I_s}) - V_T ln(\frac{I_{c2}}{nI_s}) \tag{4.10}$$

$$V_{be1} - V_{be2} = V_T ln(n) = \frac{KT}{q} ln(n) \tag{4.11}$$

$$I_o = \frac{KT}{R_o q} ln(n) \tag{4.12}$$

The current I_0 will flow through M3, if M1 and M3 are equal sized matched transistors. Hence V_{ref} can be written as:

$$V_{ref} = I_o R_1 + V_{be3} \tag{4.13}$$

$$V_{ref} = \frac{R_1 KT}{R_o q} ln(n) + V_{be3} \tag{4.14}$$

First term in above equation exhibits positive temperature coefficient (PTAT) and second term exhibits negative temperature coefficient (CTAT). The reference voltage V_{ref} can be made immune to temperature variations if positive temperature coefficient term nullifies negative temperature coefficient term. The temperature dependence of V_{be3} is constant and cannot be controlled, but slope of first term can be controlled by selecting the appropriate value of resistance R_o and R_1 and size ratio parameter 'n' respectively. In above Eq.(4.14), V_{be3} is again a process dependent term. The trimming bits are added in the design to change the resistance value to get correct value of voltage reference in different process corners.

4.3 Voltage Regulator

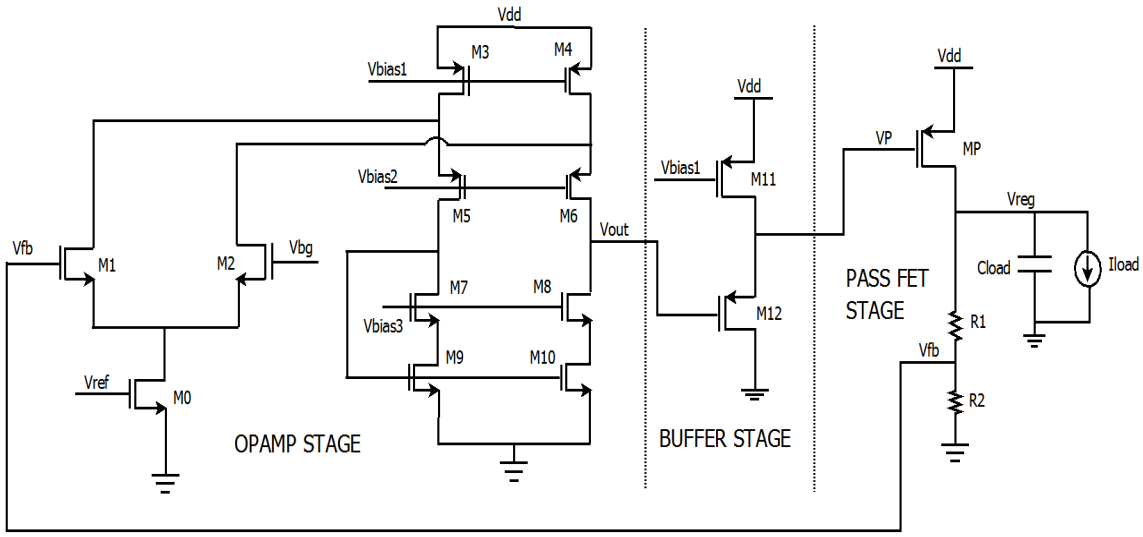

Figure 4.3: Schematic diagram of Voltage Regulator

The first stage of voltage regulator is folded cascode stage that is used to provide high gain and helps in providing feedback loop in the regulator. Here the reference voltages are generated from reference current to stabilize the operation across process and temperature variations. Here V_{bg} denotes the band-gap reference voltage and V_{reg} denotes the regulator's output. The gain of an op-amp stage can be written as:

$$A_{v1} = g_{m1}\{((g_{m5} + g_{mb5})r_{o5}(r_{o3}||r_{o1}))||(g_{m7} + g_{mb9})r_{o7}r_{o9}\} \tag{4.15}$$

The second stage is a buffer stage which, is used to drive the pass FET stage. The gain of second stage can be written as:

$$A_{v2} = \frac{g_{m12}(r_{o12}||r_{o11})}{1 + g_{m12}(r_{o12}||r_{o11})} \approx 1 \tag{4.16}$$

The voltage level at gate of transistor M_P varies significantly according to load current requirements. The voltage buffer is used to isolate the output of an op-amp from the gate voltage variations of pass-FET. The gain from final pass-FET stage can be written as:

$$A_{v3} = -g_{mP}(1/(sC_{load})||(R_1 + R_2)||r_{oP}) \tag{4.17}$$

Inherently, the voltage regulator loop is not stable due to the excessive phase shift across feedback loop. To guarantee the stability of voltage regulator, compensation strategies are employed in the design to generate the stable accurate frequency response. In this work, miller compensation strategy is utilized and an additional resistance is also included in compensation path to relocate

the zero introduced by miller capacitance.

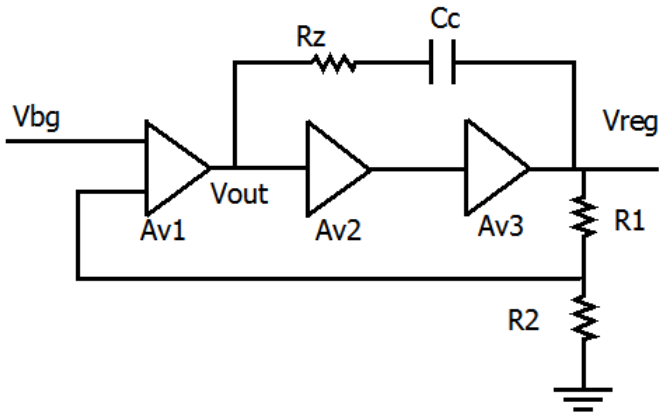

Figure 4.4: Miller Compensation strategy with series Resistance

The small capacitance (C_c) is introduced in the feedback path along with series resistance (R_z). The equivalent miller capacitance introduced after stage will become very large and acts as a dominant pole (ω_{p1}) of the regulator and load capacitance will behave as non-dominant pole (ω_{p2}) of the system. The series resistance is introduced in the compensation path to relocate the zero introduced due to miller capacitance (C_c). The poles and zeroes location after compensation are [7] [14]:

$$\omega_{p1} = \frac{1}{A_{v2}A_{v3}C_c(((g_{m5}+g_{mb5})r_{05}(r_{03}||r_{01}))||(g_{m7}+g_{mb9})r_{07}r_{o9})} \tag{4.18}$$

$$\omega_{p2} = \frac{1}{C_{load}((R_1+R_2)||r_{oP})} \tag{4.19}$$

$$\omega_z = \frac{1}{C_c(g_{mp}^{-1}-R_z)} \tag{4.20}$$

The location of zero can be changed by varying the resistance (R_z) value. The resistance value is selected in a manner such that, non-dominant pole and compensation path zero cancels each other.

4.4 Simulation Results

The band-gap reference exhibits the temperature dependence of $44\mu V/$℃ for typical corner. The dependence of band-gap reference on process variations can be minimized by employing the digital trimming technique in the resistances R_0 and R_1 used in the band-gap reference. Fig.(4.5) represents the variations in band-gap reference voltage across temperature range of -40℃to 150℃

in typical process corner.

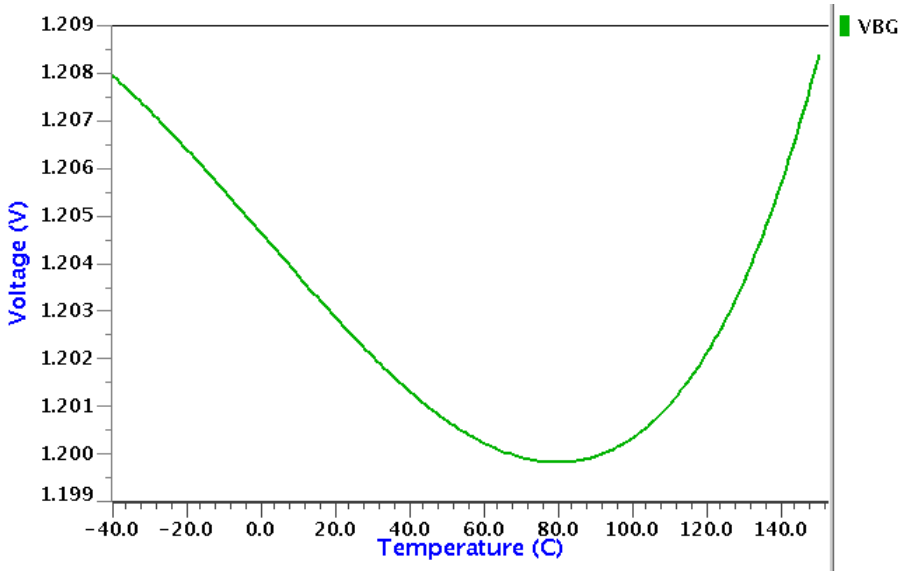

Figure 4.5: Variation of Band-gap Voltage across temperature variations

The specifications of designed voltage regulator are listed in Table(4.1). The open loop gain and unity gain bandwidth is one of the performance parameters of voltage regulator design and they are dependent on the operation amplifier and subsequent stages used in the design. If the open loop gain of voltage regulator is very high, then closed loop gain is reduced to constant feedback factor. The open loop gain is a function of frequency and exhibits maximum value at DC.

Table 4.1: Specifications of Voltage Regulator

Input Reference voltage	1.2
Output Voltage	1.8V
Load Capacitance	0-40 pF
Input Supply	2V – 3V
Load Current	0-20mA

In this work, a two stage voltage regulator is designed other than final stage of NMOS based pass transistor. Addition of each stage in the design introduces a pole at every subsequent stage which can cause excessive phase shift, which can results in unstable behaviour of voltage regulator. Fig.(4.6) represents the frequency response of open loop voltage regulator without any compensation. This uncompensated behaviour is obtained due to close locations of output pole and other non-dominant poles present after each stage. Fig.(4.7) represents the frequency response of open loop gain of voltage regulator with compensation. Minimum DC loop gain of 103.11 dB and worst case phase margin of 59.62° is achieved after employing compensation. The worst case unity gain bandwidth (UGB) obtained from simulation is 13.150MHz. The high value of unity gain bandwidth is required for fast transient response of voltage regulator [14].

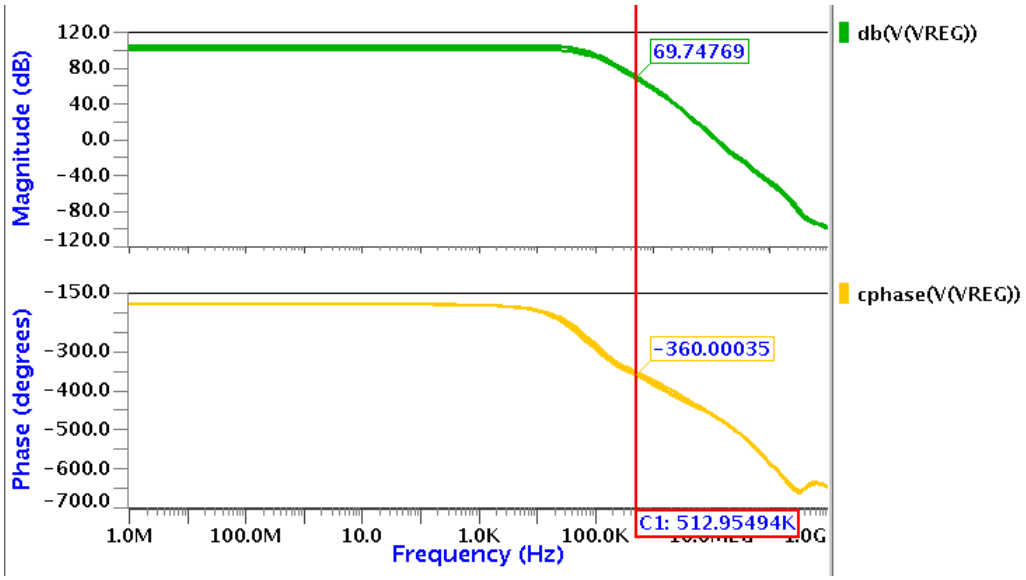

Figure 4.6: Frequency response of open loop gain without compensation

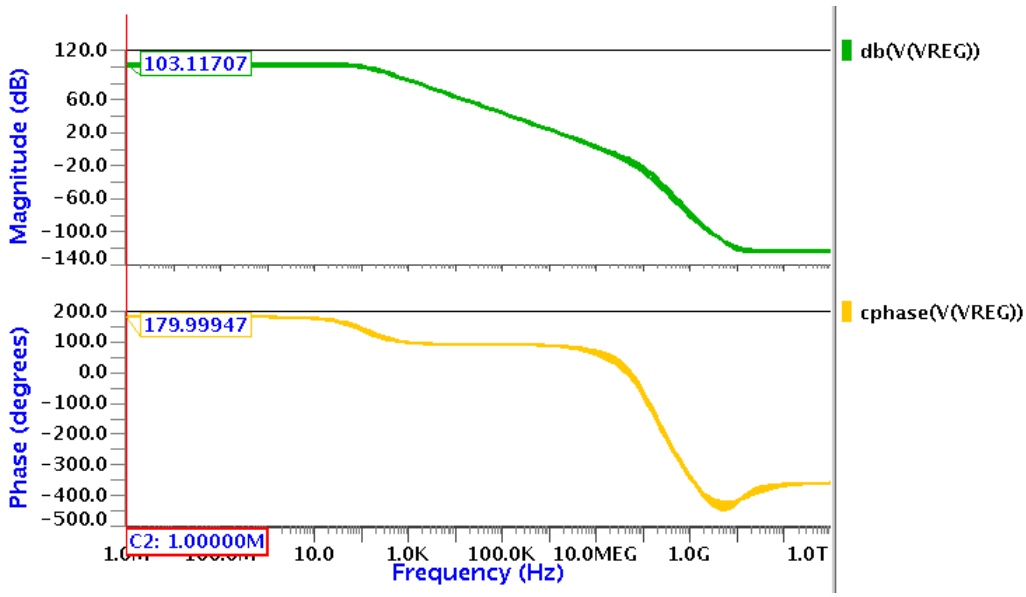

Figure 4.7: Minimum DC Loop gain across all process corners

Fig.(4.9) represents the PSRR frequency response of voltage regulator. The value of PSRR at DC is determined by the gain of the operation amplifier. The proposed design exhibits PSRR of -83.89 dB at DC. The PSRR value between 100 KHz and 1 MHz is an important aspect if output of DC/DC switched mode power supply (SMPS) is used to power the voltage regulator. PSRR of -80.19 dB at 100 KHz and -63.37 dB at 1MHz is observed in the simulation.

The output voltage level of voltage regulator should have to be independent of load current, but it exhibits small dependence. This dependence is termed as load regulation of the regulator.

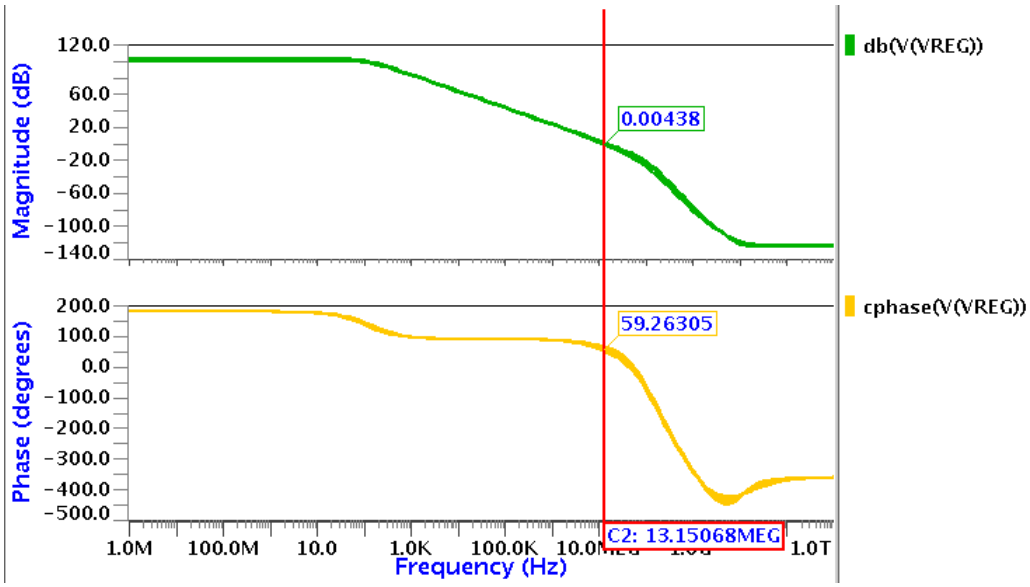

Figure 4.8: UGB and Phase Margin of Open Loop Transfer Function of Voltage Regulator

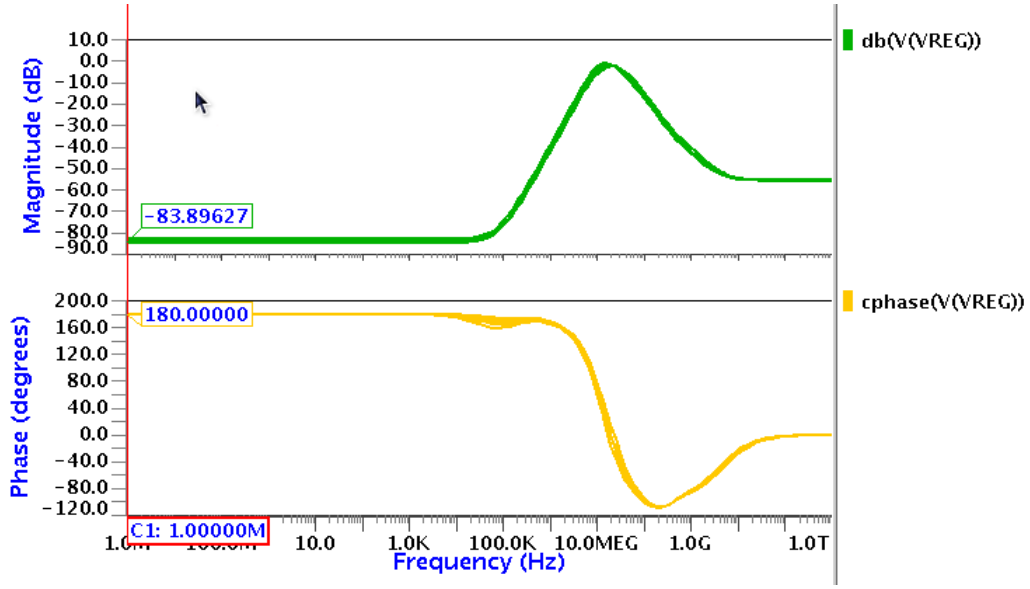

Figure 4.9: PSRR frequency response of voltage regulator.

Fig.(4.10) represents the load regulation in different process corners. The output of voltage regulator should also have to be immune of variations in input voltage. The variation of output with input supply variations is termed as line regulation of the regulator. Fig.(4.11) represents the variation of regulator's output with input supply variations across different process corners.

Fig.(4.12) represents the transient response of voltage regulator for sudden load current requirements. The sudden load current changes causes charging and discharging of load capacitor that results in sudden drop and rise in regulator's output voltage level. The voltage regulator feed-

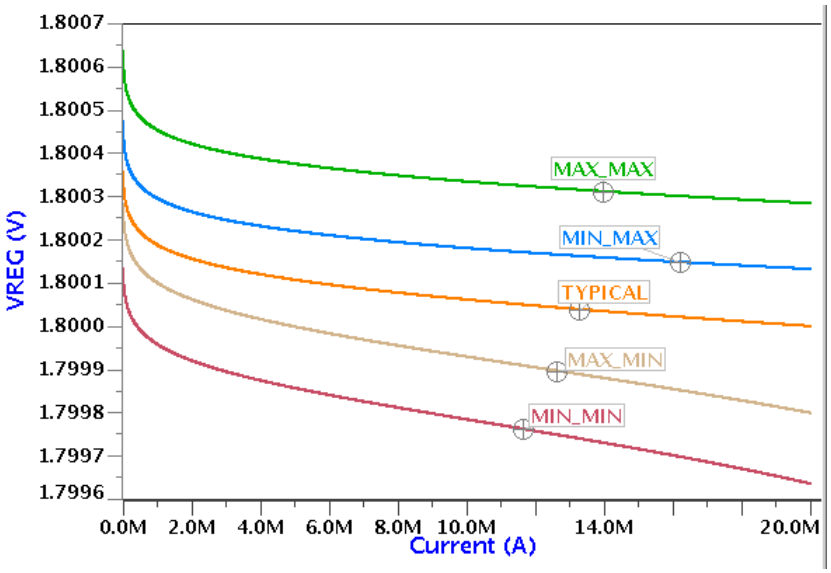

Figure 4.10: Variation of Regulator's Output Voltage with Load Current in Different Process Corners

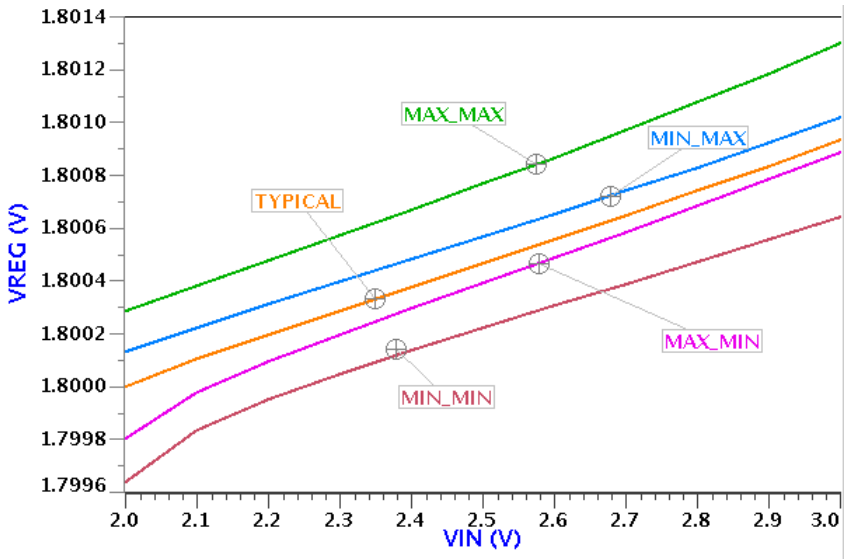

Figure 4.11: Variation in Regulator's Output Voltage with variation in input supply voltage.

Table 4.2: Load and Line regulation in different process corners

Process	Load Regulation (mv/mA)	Line Regulation (mV/V)
MAX	0.0175	1
MIN	0.0245	0.4
TYP	0.0191	0.9
NFPS	0.0245	1.08
NSPF	0.0171	0.8

back loop requires some finite amount of time to correct the gate voltage of pass-FET according

to load current requirements. Once the loop gets settled, the output of regulator again reaches its correct value. The time taken by loop to correctly adjust the gate voltage of pass-FET is dependent on the unity gain bandwidth of voltage regulator.

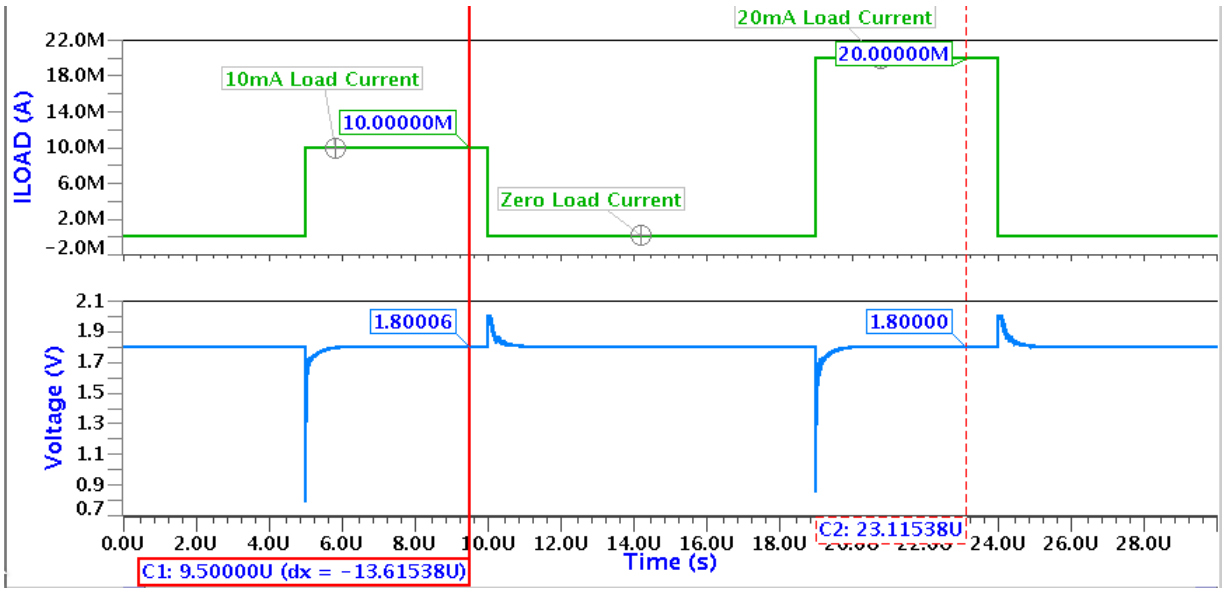

Figure 4.12: Transient response of voltage regulator for different load current conditions

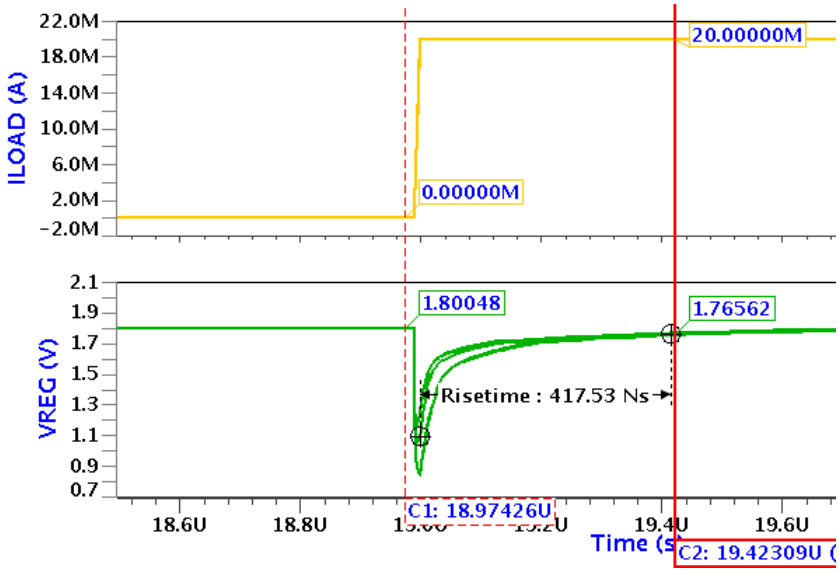

Figure 4.13: Variation in output voltage of regulator during full load current condition.

The magnitude of drop in output voltage level during sudden load current requirement is dependent on magnitude of load capacitor present at output of voltage regulator. Larger the load capacitor, lesser will be the voltage drop in the regulator's output level and vice-verse. Fig.(4.13) represents that rise time of 417.53 ns is required to reach the 95% level of voltage regulator's final value of 1.8V during sudden requirement of full load current of 20mA.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

Two PVT compensated oscillators are designed in $0.11\mu m$ BCD9S Technology for embedded Phase Change Memories. The proposed oscillators are inherently temperature compensated and does not require any other on chip analog block or feedback circuit for temperature compensation. Digital trimming technique is employed for process compensation in the presented designs. The proposed strategy of ring oscillator design exhibits significant less spread with temperature variations and with incorporation of digital trimming, spread is reduced from ±18% (untrimmed) to ±2.25% (worst case in MIN corner) for operating temperature range of -40℃ to 150℃. The latch based oscillator reduces the worst case frequency spread significantly from ±16% (untrimmed) to ±2% (worst case in MIN corner) for operating temperature range of -40℃ to 150℃. The worst case total power consumed by PVT compensated ring oscillator and latch based oscillator is 84 μW and 69 μW respectively. The proposed oscillators design strategy achieves significantly less temperature dependence and low power consumption than state-of-the-art oscillator circuits. Table(5.1) compares the frequency variation and power consumption of proposed work with various state-of-the-art designs. In this work a High PSRR, low quiescent current on-chip voltage regulator is also presented and its specifications are listed in Table(5.2).

5.2 Future Work

This work can be extended further to perform the phase noise analysis of proposed oscillators. Moreover, miller compensation strategy employed in voltage regulator can be replaced with voltage buffer compensation or flipped voltage follower based buffer architecture [16] [17]. This improvement in compensation strategy can result in significant reduction in on-chip compensation capacitor.

Table 5.1: Comparison of proposed oscillators with state-of-the-art designs

Work	Process (nm)	Frequency (MHz)	Frequency Variation (typical corner) (%)	Power(μW)	TC(ppm/℃)
[2], exp	CMOS 250nm	7	±0.84 @ -40℃ to 125℃	1500	315
[3], exp	CMOS 130nm	1	±0.5 @ 25℃ to 180℃	428	108
[4], exp	CMOS 65nm	0.15	±0.5 @ -55℃ to 125℃	51	300
[5], exp	CMOS 180nm	10	±0.4 @ -20℃ to 100℃	80	67
[6], exp	CMOS 350nm	30	±0.7 @ -20℃ to 100℃	180	90
[15], exp	CMOS 180nm	14	±0.75 @ -20℃ to 100℃	45	91
Ring Osc, sim	BCD9S 110nm	10	±0.7 @ -40℃ to 150℃	84	73
Latch Osc, sim	BCD9S 110nm	10	±0.4 @ -40℃ to 150℃	69	42

exp: experimental results, sim: simulated results, Osc :Oscillator, TC: Temperature Coefficient

Table 5.2: Performance Summary of Voltage Regulator

Input Supply (V_{dd})	2V-3V
Dropout Voltage (V_{do})	200 mV
Output Capacitor	40pF
Quiescent Current	30μA
Load Current	20mA
Compensation Capacitor	10pF
Load Regulation	0.0191mV/mA @ V_{out} = 1.8V and I_{load} = 20mA
Line Regulation	0.9mV/V @ V_{out} = 1.8V and V_{in} = 2V-3V
PSRR	-63.37dB @1MHz

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