Wide bandgap-HEMT device (GaN) modelling for High Power Amplifier Design

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M.Tech-Electronics and Communication Engineering-2015-2017
June, 2017

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Submitted in Partial fulfilment of the requirements
for the degree of M.Tech in Electronics and Communication Engineering

Student's Declaration

I declare that the dissertation titled "Wide bandgap-HEMT device (GaN) modelling for High Power Amplifier Design" submitted by Shipra Batra for the partial fulfilment of the requirements for the degree of Master of Technology in Electronics and Communication Engineering is carried out by me under the guidance and supervision of Dr. M. S. Hashmi at Indraprastha Institute of Information Technology, Delhi. Due acknowledgements have been given in the report to all material used. This work has not been submitted anywhere else for the reward of any other degree.

..... Place and Date: …….....
Shipra Batra

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

……..
Dr. Mohammad. S. Hashmi

ABSTRACT

Material properties of wide-bandgap semiconductors are excellent candidates to build highly-efficient and highly-linear power amplifiers required to support cellular communication. AlGaN/GaN HEMTs are considered the most capable of all available wide-bandgap devices, as they combine material properties of GaN with the principle of HEMTs.

This dissertation presents a large-signal modelling strategy for small-sized (4*100 µm) AlGaN/GaN HEMT that is capable of being ported to computer-aided design of power amplifiers.

A large signal model capable of simulating the output power and non-linear behavior of the device is very crucial for the design of a Power Amplifier. This is the main problem addressed by this thesis. Large signal modelling begins with the development of a linear model. A bottom-up empirical modelling approach is followed in this work. It required selecting an appropriate electrical equivalent circuit which accounted for the complex parasitic and maintained a clear physical interpretation of the model parameters. Further, an efficient algorithm for extracting and optimizing parasitic is adopted. This has set the foundation for non-linear modelling.

The large-signal model includes a non-quasi static formulation of the gate-charge and a dispersive-drain current (I_{ds}) model. Non-quasi static parameters are calculated from small-signal intrinsic parameters by using path-integrals. Various mathematical interpolation techniques are applied while doing integration taking care that the parameters do not lose their physical significance. The I_{ds}-model parameter extraction is based on DC-IV and pulsed-IV measurements. Large-signal models are developed and directly implemented in CAD-software to perform model simulations. The results of the simulations performed are compared with the measured data. The results show high correlation between them making it a competent model for High Power Amplifier design for small-sized AlGaN/GaN devices.

ACKNOWLEDGEMENTS

The work for this thesis was carried out at Circuit Design and Research Lab, IIIT-Delhi, India, during the year 2016-2017.

Firstly, I would like to thank my adviser Dr. Mohammad. S. Hashmi for providing excellent guidance and encouragement throughout the journey of this work. Without his guidance, this work would never have been a successful one. I also take this opportunity to express a deep sense of gratitude towards Mr. Shashwat Kaushik for his support and encouragement for conquering every hurdle that I have encountered throughout the process. My regards to all my friends at IIIT-Delhi who made this journey a wonderful one. Last but not the least; I would like to thank my Parents for supporting me spiritually, morally and emotionally in every way possible.

"If it doesn't challenge you, it doesn't change you" – Fred DeVito

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1 INTRODUCTION

In the present era, telecommunication plays a pivotal role in almost every sphere of life. In the last two decades, the use of mobile devices has grown rapidly across the world. Countries in North America and Western Europe were the first areas to begin swift adoption of mobile phones in the late 1990's, with many countries in Western Europe reaching almost 100% penetration by 2003. These countries generally had strong wireline infrastructure before the advent of mobile devices. Sudden growth and popularity of mobile devices is related to more flexible connectivity and communication provided by the mobile devices. Fig, 1.1 below shows the mobile phones penetration in each country in 2013.

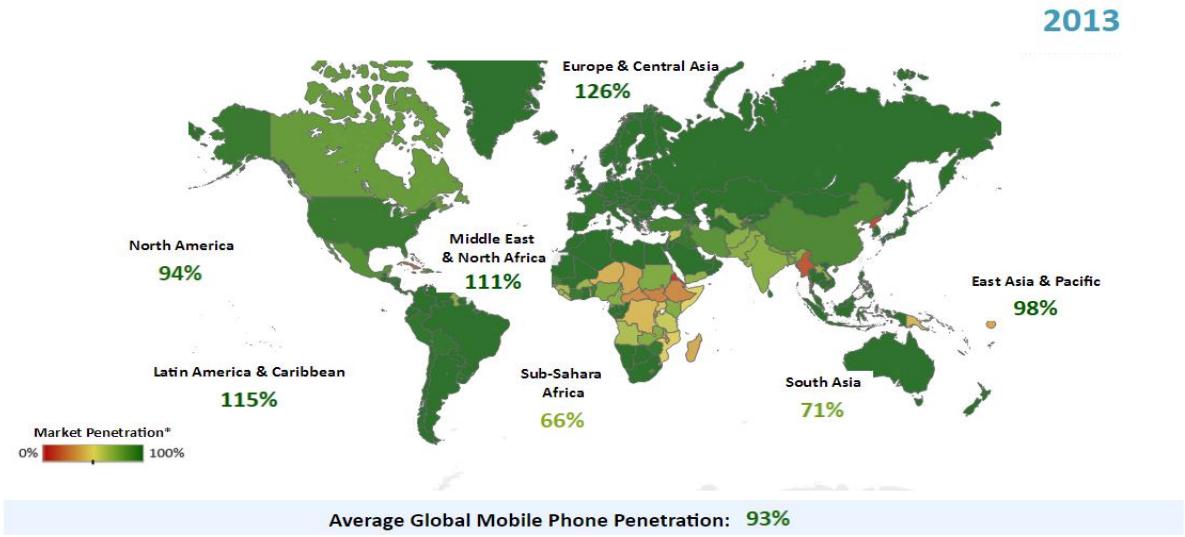

FIGURE. 1.1 MOBILE PHONE PENETRATION IN EACH COUNTRY IN 2013 [COURTESY: OPEN STREET MAP CONTRIBUTORS]

Mobile devices these days are not only used for calling purposes, but their domain has extended. Cellular devices are expected to perform video calling, instant messaging, excellency in voice calls and many more. All this has been possible because of the 3G and 4G standards defined by the International Telecommunications Union (ITU). 3G and 4G standards are expected to provide services with higher data speed and data bandwidth [1]. With the 4G telecommunications systems still in the deployment stage, eyes are set towards the development of 5G services. Even in India, the 3G data consumption has seen 85% rise from 2015-16. The Internet user base in India is booming more with the penetration of 3G and 4G in market and is expected to hit 600 million users by 2020.

To account for the high data delivery rates which these newer generations ought to provide, the telecommunication infrastructure needs to be improved tremendously to meet the quality of services. Among these, RF High Power Amplifiers (HPAs) are considered to be the most crucial

and challenging area. In order to, provide high quality of service and support high user capacity highly linear Power Amplifiers (PAs) with high power efficiency are required. [2,3].

PAs linearity can be increased by adding external circuitry to it. But this involves more area, difficulty of adjustment and hence more cost. Other way to improve linearity and add efficiency to a PA is by improving its design. Technology dependent parameter, leakage current is an important barrier to designing a highly power efficient PA. [4,5]. It becomes imperative to consider an improved device technology for designing a PA for higher generation systems.

The technologies presently in use for HPA design like Si-LDMOS are reaching extremes, main constraint being the operating frequency which is limited to about 4 GHz. Therefore, intensive research in recent years has made it possible to develop new device process technologies using new wide bandgap materials. AlGaN/GaN HEMT has proven to be an excellent candidate for fabrication of PAs. It has high sheet carrier density, high saturation electron velocity thereby high output power. It has high electron mobility, responsible for low on-resistance thereby adding high power efficiency. AlGaN/GaN HEMT can achieve very high breakdown voltage, very high current density and can even sustain very high channel operating temperature. AlGaN/GaN can achieve power densities upto 30 W/mm on SiC substrates [6], 9.4 W/mm on GaN substrates [7], 12 W/mm on silicon substrates [8] and 12 W/mm on sapphire substrates [9] making AlGaN/GaN fit for being used for RF applications.

However, AlGaN/GaN HEMT is still in very early stages of development and commercial devices are still unavailable. Though recent times have seen rapid development of AlGaN/GaN HEMT with focus on increasing output power and linearity of the device. [6, 10-12]. Therefore, designing PAs for communication systems based on AlGaN/GaN HEMT requires accurate and precise large-signal model of this device.

1.1 Transistor Modelling For High Power Amplifier Design

The design of PAs improves considerably by using models of the device that can be executed in the computer-assisted design (CAD) environment, because in such environments multiple simulations can be performed at different conditions and the behaviour of the device can be predicted and studied by the designer before it can go for actual fabrication. This reduces the iterations of fabrication that are required for a successful prototype. The transistor is the most crucial power amplifier therefore, it becomes imperative to model the transistor correctly in a circuit.

Transistor modelling can help improve the process of device fabrication by correlating the measured results with the fabrication process and material properties. Therefore, the transistor model should account for the physical aspects of the material and structure.

Modelling of a transistor beings with small signal modelling which involves *linearization* around an operating point. However, non-linear effects of the device can be completely studied by using

large-signal models. Transistors are designed to consider the key non-linear effects like trapping effects, dispersion effects and thermal effects.

Large signal modelling is a hot research topic due to the non-linear effects and the novelty of processing technology, therefore, major research is being carried in this regard. [13]. Fig. 1.2 describes the circuit design and model development using CAD before fabrication.

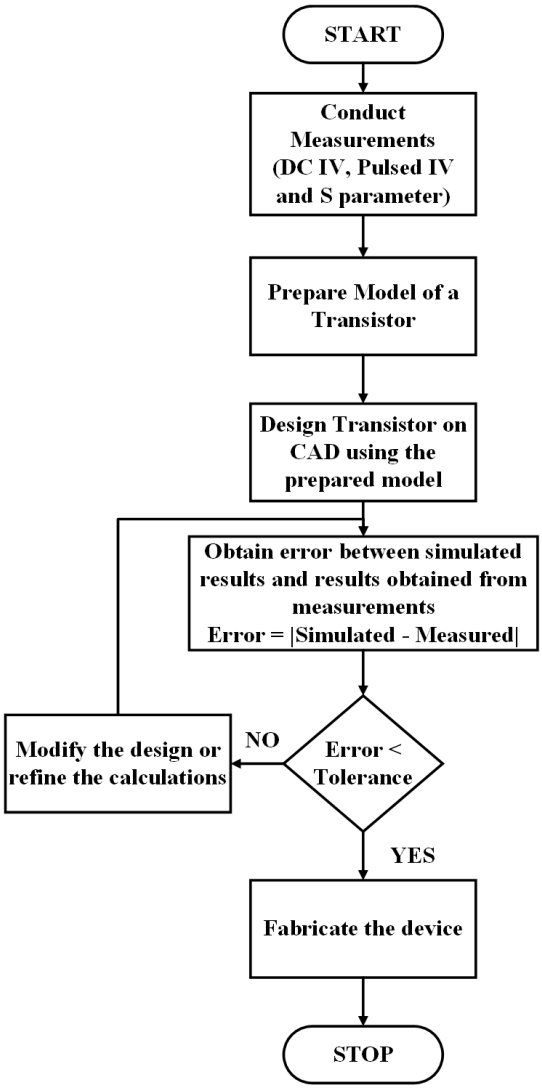

FIGURE. 1.2 MODEL DEVELOPMENT USING CAD BEFORE FABRICATION

1.1 Challenges Pertaining To Modelling Transistor For HPA Design

Modelling GaN devices with equivalent circuits requires comprehensive networks with many parameters due to complex parasitic and non-linear effects. As the model parameters, grow in number the methodology adopted for extraction of parameters and algorithm for optimizing the process of accurate parameter extraction also becomes complicated. Mathematical optimization conceals the physical interpretations of the device.

1.2 Aim Of The Research

The main objective of this thesis is to investigate a large-signal modelling strategy for a small-size GaN HEMT for designing a High Power Amplifier used in communication systems. This thesis formulates the modeling strategy comprehensively to account for all the complex effects and parasitic in the model by carefully studying the layout of the device. The calculation of the model parameters is based on electrical measurements and on data that is easily available. The size of the database is kept moderate so that it is easy to acquire. Lastly, the thesis assures successful implementation of the model in CAD-software to ease and escalate the process of fabrication.

1.3 Thesis organization

The thesis is organized as follows. Chapter 1 introduces the reader to the research field, describing the challenges in this field and stating the main objective of this thesis. Chapter 2 highlights the positive points and drawbacks of the wide-bandgap semiconductors used for fabrication. It also compares GaN with presently used materials. The chapter explains basic definition of HEMT and the principle of operation of a HEMT device and the related effects. Chapter 3 gives an overview of the general modelling approaches, their advantages and disadvantages. The bottom-up modelling approach, used in this thesis is described along with quasi-static and non-quasi-static models. Chapter 4 gives an outline of the small-signal modelling approach. It introduces to the electrical equivalent circuit used for modelling. It provides an algorithm adopted for parameter extraction and optimization and discusses the result of the algorithm henceforth. Moving on, Chapter 5 proposes the large signal modelling strategy. It describes the model adopted for AlGaN/GaN HEMT. This chapter explains the model parameter extraction. The chapter implements the model developed in CAD and verifies the simulated and measured results. Conclusions and recommendation for further work are then drawn and written in Chapter 6.

2 ALGAN / GAN HEMTS

Devices fabricated with GaN and SiC are considered excellent candidates for high power amplifiers due to physical properties of such materials [14]. In this chapter, properties of various semiconductor materials used to fabricate these devices are compared. Also, since most of the research work in this direction is focused on GaN HEMTs so this chapter also shows the advantages of GaN with respect of other devices. The structure and principle of operation of GaN is also explained in this chapter.

2.1 GAN COMPARED WITH GAAS, SI AND SIC

Several publications [14-17] indicate that device performance for functioning as a power amplifier improve if the material properties of the device semiconductor have the following desired properties –

1. Higher energy bandgap E_g
2. Higher electron mobility μ
3. High breakdown electric field E_c
4. High thermal conductivity *k*
5. Low dielectric constant Ɛ
6. High electron saturation velocity v_{sat}

GaN and SiC has most promising and desired properties for being used as a wide-bandgap semiconductor for power amplification applications. Whereas, GaAs and Si are most commonly used as GaN and SiC have not been harnessed to their full capacity. Table 2.1, shows the comparison of the material properties of these semiconductor materials.

TABLE 2.1 COMPARISON OF VALUES OF MATERIAL PROPERTIES FOR DIFFERENT SEMICONDUCTORS [14,17]

Property of bulk material [unit]	GaN	4H-SiC	Diamond	GaAs	Si
Bandgap [eV]	3.4	3.2	5.5	1.4	1.1
Electron mobility at 300 °K [cm^2/V·s]	440	700	1900	4000	1500
Electron saturation velocity [10^7 cm/s]	2.5	2.0	2.7	1.0	1.0
Breakdown field [MV/s]	3.3	3.0	5.6	0.4	0.3
Thermal conductivity [W/cm·°K]	1.3	3.7	20	0.5	1.5
Relative dielectric constant [-]	9.0	10.0	5.5	12.8	11.8

Although diamond has several desired properties but it's high cost of production and complex fabrication process limit its usage [17]. The possibility to fabricate devices with higher values of electron mobility than in bulk materials (HEMTs) is well-known for GaAs [18] and GaN [14]. Therefore, low value for bulk GaN does not pose a real problem, also other properties for GaN and SiC allow better performances in power amplifiers than GaAs and Si [19].

2.2 BASIC HEMT DEFINITION

As shown in previous section that the desired properties of a semiconductor material include high electron mobility and abundant carrier concentration. To increase the carrier concentration doping is the done, which in turn reduces the mobility in the semiconductor material. Therefore, the aim is to establish high carrier concentration without affecting the mobility of the transistor. This introduces the concept of HEMTs or High Electron Mobility Transistors. The high electron mobility transistor (HEMT) is the fundamental component for state-of-the-art high-performance microwave devices. It is a heterostructure field effect transistor, which has the benefit of high transport properties because of abundant carrier present in potential well. A heterostructure consists of at least two layers of different semiconducting materials with distinct bandgaps. The interface between the layers of the two different semiconductor materials is called heterojunction.

A simplified band diagram of HEMTs is shown in Fig 2.1 consists of two different bandgap materials, one with n-type doping and other is undoped. Initially, when materials are kept far apart the Fermi level of n-type material is closer to conduction band edge and undoped material Fermi level is at centre of the bands. When these two materials are placed closer to each other, the electrons tend to transfer from the n-type doped layer into the undoped layer to align the Fermi levels of the two materials. Also, the conduction band on the AlGaAs side lies energetically higher than that on the GaAs side. Thus, electrons in the conduction band of the AlGaAs layer possess higher energy than the ones in the GaAs layer. As electrons tend to occupy the lowest allowed energy state, they are encouraged to move from AlGaAs to GaAs. This results in increase in the electron concentration within the GaAs layer even without the introduction of ionized donor impurities.

At the doped/undoped interface a sharp dip of the band edge is seen. The sharp dip results in high carrier concentration in a narrow region. The spread of electrons in the quantum well or narrow well is two-dimensional. Hence, the charge density is termed a two-dimensional electron gas (2DEG) and quantified in terms of sheet carrier density n_s.

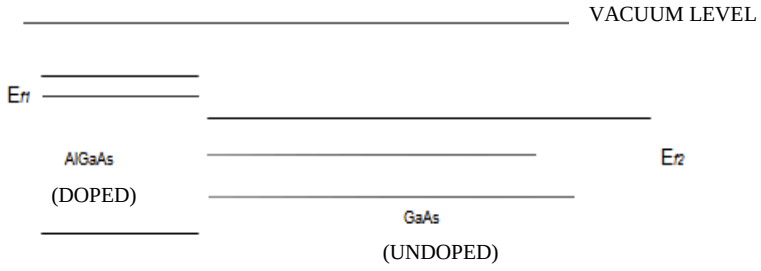

FIGURE 2.1 ENERGY BAND DIAGRAM OF ALGAAS/GAAS LAYERS [20]

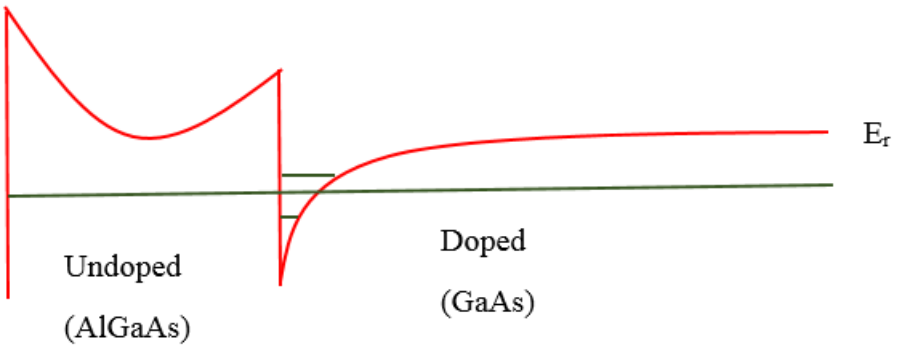

FIGURE 2.2 ENERGY BAND DIAGRAM OF A HETEROSTRUCTURE. THE TWO DASHED LINES REPRESENT THE ENERGY SUBBANDS ARISING FROM SPATIAL QUANTIZATION EFFECTS [21]

2.2.1 ALGAN / GAN STRUCTURE

AlGaN/GaN HEMT has been fabricated in a similar way using doped or undoped AlGaN layer as shown in Fig. 2.3. GaN HEMTs heterojunction was formed with n-type doped AlGaN as barrier layer and GaN as channel layer. Metal contacts are placed on the top for drain and source. A Schottky contact for the gate is also present. A semi-insulating substrate is present at the bottom. It has been observed that even if there is no intentional doping, a 2DEG is formed in the AlGaN/GaN interface. Therefore, to form 2DEG here is due to presence of a strong polarization field across the AlGaN/GaN heterojunction. A 2DEG with the sheet carrier density up to 10^{13} cm^{-2} can be achieved without any doping [18].

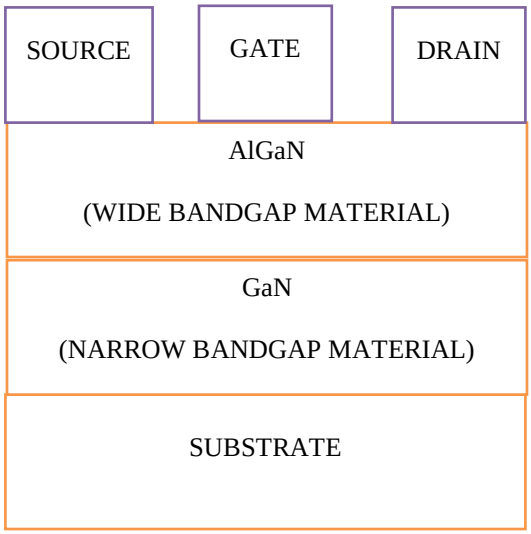

FIGURE 2.3 BASIC ALGAN/GAN HEMT LAYER STRUCTURE

2.3 ALGAN / GAN PERFORMANCE

2.3.1 IV CHARACTERISTICS

Fig. 2.4, shows the DC IV characteristics for a 4*100 µm. As can be seen from the figure, increasing the drain-source voltage (VDS) the knee voltage also shifts to the right and the breakdown voltage shifts to the left, thereby narrowing the power delivering region.
Power transferred is given as –

$$Pout = \frac{1}{8}(Imax - Imin)(BVgd - Vknee) \qquad (2.1)$$

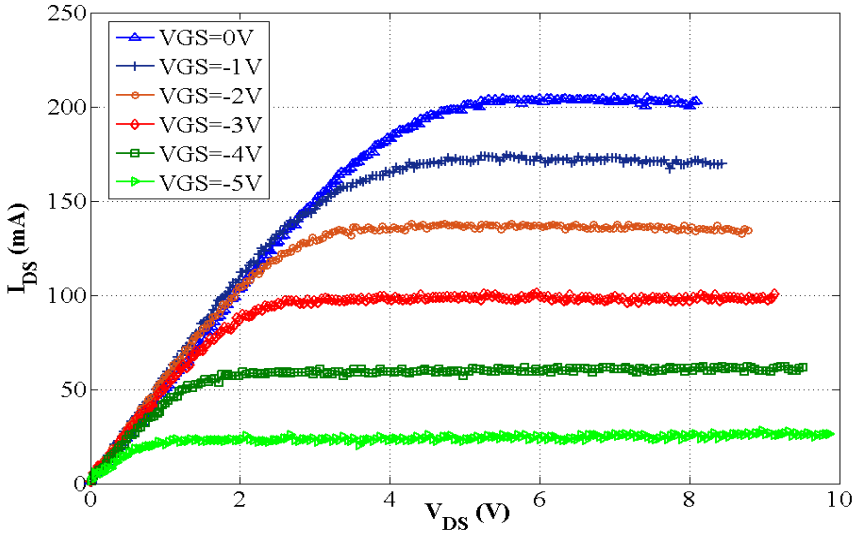

FIGURE 2.4 DC IV CHARACTERISICS FOR A 4*100 µM DEVICE

2.3.2 RF CHARACTERISTICS

For understanding the frequency response performance of a transistor, the unity current gain frequency (f_t) and the maximum oscillation frequency (f_{max}) are useful figures of merit. f_t is the frequency at which the short circuit current gain, h_{21}, is unity. It can be extracted from S-parameter measurements. Equation for extracting h_{21} from S-parameter measurements is given as-

$$h21(dB) = 20\log\left(-\frac{2S21}{(1-S11)(1+S22)+S12\,S21}\right) \qquad (2.2)$$

Unity current gain frequency, f_t is a good indication of the maximum achievable gain-bandwidth for resistively terminated device. f_{max} is the frequency at which maximum unilateral gain (MUG) is unity. It is calculated with the condition of conjugate matched input and output of the device (max power transfer) and eliminating the feedback gate-drain impedance. This frequency is the maximum possible frequency to achieve power amplification using the device. f_{max} can be extracted from the S-parameter measurements by the following expression-

$$MUG(dB) = 10\log\left[\frac{1}{(1-|S11|^2)}\,|S21|^2\,\frac{1}{(1-|S22|^2)}\right] \qquad (2.3)$$

The values of f_t and f_{max}, at certain bias condition are function of the structure of the device, which provides the values of the intrinsic parameters and the parasitic elements. Fig. 2.5, shows the extracted value of f_t and f_{max} at different bias points for a 2x200 μm gate width AlGaN/GaN HEMT.

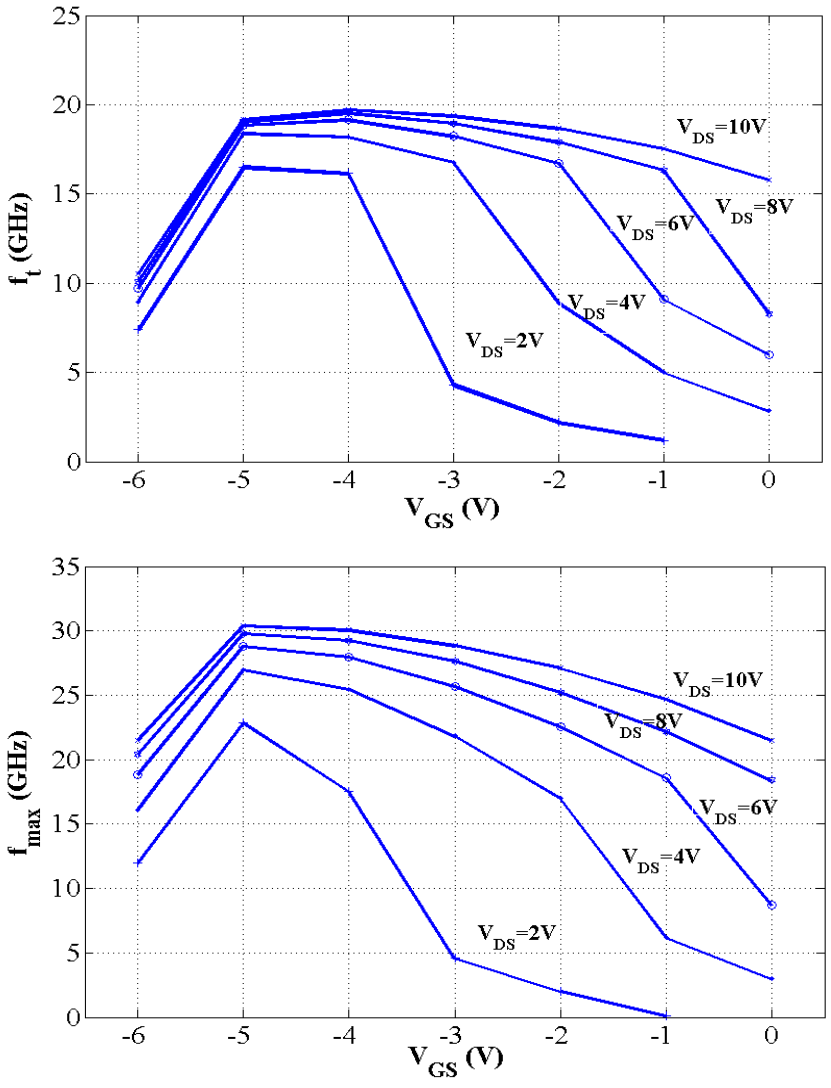

FIGURE 2.5 MEASURED UNITY GAIN FREQUENCY (F_T) AND MAXIMUM OSCILLATION FREQUENCY (F_{MAX}) VERSUS GATE VOLTAGE FOR A 2*200 μM GATE WIDTH ALGAN/GAN AT DIFFERENT DRAIN VOLTAGES .

As can be seen from graph above, Fig. 2.5, it can be observed, at lower voltages or at lower drain current, f_T increases with an increase of Vgs voltages due to an increase of the transconductance. At higher voltage values, f_T decreases due to the self-heating effect, and it reduces the value of electron velocity thereby leading to the smaller values of transconductance. f_{max} has the same trend as f_T because they are correlated.

3 FUNDAMENTALS OF ACTIVE DEVICE MODELLING

In this chapter, fundamental principles of active device modelling are presented. Firstly, general modelling approaches are described. Following, bottom-up modelling approach is explained and techniques of modelling the dynamic behaviour of the device. Finally, measurement techniques, which play an important role for defining the accuracy of the device model, will be described.

3.1 DEVICE MODELLING APPROACHES

Device modelling methods can be classified into two main approaches, physical and empirical modelling. Physical modelling relies on physics-based parameters which describe the geometry and technology of a device. Empirical modelling depends on measured characteristics of the device that describe the behaviour of the device.

3.1.1 PHYSICAL MODELLING

In this modelling approach device performance can be predicted from physical data like carrier transport properties, material characteristics, and the device geometry describing the device [22-24]. The main advantage of this approach is that it describes the device operation in terms of the device physics making it is more usable for device designer who has some control over the device fabrication process. In this approach, the response of the device is obtained by solving a set of coupled nonlinear differential equations describing the internal field of the device and electrical charge transport. The equations are complex and normally require numerical methods to obtain solutions which requires longer time and larger memory storage. Moreover, it is difficult to obtain technology related information making this approach infeasible in many cases.

3.1.2 EMPIRICAL MODELLING

Empirical modelling, also called measurement-based modelling because it depends on measured data. It is also called behavioural modelling because it depends on observed response due to stimulation signal. Empirical models can be constructed using analytical equations for the description of measured data. They are also termed "analytical models" [25-27]. These models can also be constructed based upon a lookup table developed from the measured data, and are called "table-based models" [28-29]. These models can also be classified as equivalent circuit models as these are based on observed input-output data of the device. The main advantages of the analytical models are: computational efficiency, automatic data smoothing, simplicity, and ability to simulate out of measurements range. The main disadvantages are limited accuracy due to use of simplified expression, technology dependent, difficulty in extraction of the model fitting parameters, and no physical meaning for the fitting parameters. Table-based models can also be considered as an equivalent circuit based models, but instead of using mathematical expressions, multidimensional spline functions are used to fit the measured data and only fitting coefficients need to be stored. They are more accurate than the analytical models and are ideal for application where the functional form of the behaviour is unknown. The physical reliability of the models can be improved by using an equivalent circuit that can fit the device physics. Data

smoothing can be improved in these models by using spline function that can maintain the continuity of the measured data. It can be concluded from this comparison that the table-based models can compromise between simulation accuracy and implementation reliability. Therefore, this approach will be followed in this research for large-signal modelling of AlGaN/GaN HEMT.

3.2 BOTTOM UP MODELLING TECHNIQUE

In bottom-up modelling technique a small-signal measurement is carried out over a range of bias points, and large signal model is then determined from small-signal models derived at those bias points. In the small-signal models the intrinsic circuit is crucial, because it describes the nonlinear characteristics of device. This intrinsic part is extracted by de-embedding the parasitic elements (extrinsic part) of the device. If the extrinsic part is not completely de-embedded, residual parasitic effect will be produced, which will deteriorate the intrinsic circuit modelling and correspondingly derived large-signal model. To reduce the residual parasitic effect the small-signal model topology should highly match the structure of the device, hence electrical equivalent circuit chosen for modelling should be highly accurate.

3.2.1 QUASI-STATIC & NON-QUASI-STATIC FET LARGE SIGNAL MODELLING

The basis for quasi-static large-signal modelling approach is that device intrinsic elements are only voltage dependent [30]. Therefore, dynamic response of the device can be predicted from static behaviour of the device at different bias condition. This assumption helps to define functional relationships under low frequency (quasi-static) operation conditions, instead of using large-signal device characteristics at high frequency, which are more time-consuming [31]. Quasi-static assumption is a good first-order approximation in modelling of active device, but does not hold in the whole range of different operation condition. Trapping and self-heating induced current dispersions have strong impact on the RF performance of the device in which quasi-static models do not function appropriately. Therefore, non-quasi-static implementation for the large-signal drain current source should be used to predict this effect. Also at high frequency operation, the device channel charge under the gate does not response immediately to the stimulation signal [32,33]. This requires a relaxation time to build up. Moreover, the device channel transconductance, G_m, cannot respond instantaneously to changes in the gate voltage at high frequency. Therefore, time delay inherent to this process should be accounted in the small-signal model.

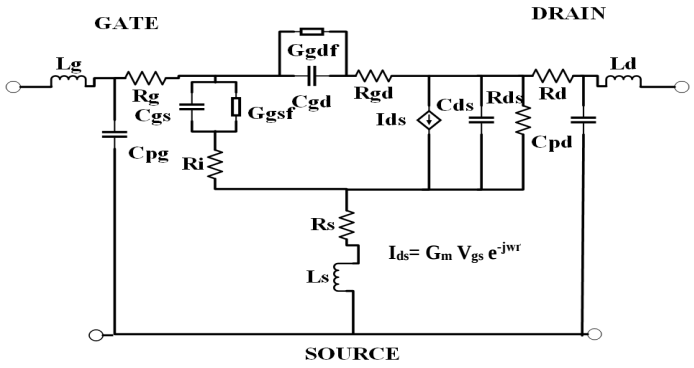

FIGURE 3.1 INTRINSIC NON-QUASI-STATIC LINEAR DEVICE EQUIVALENT CIRCUIT

The small signal model adopted is given in Fig.3.1. In this model, the series resistances R_i and R_{gd}, account for the quadratic frequency dependency of Y-parameters. The transconductance time delay with respect to the applied gate voltage is described by transit time, τ. In the large-signal model, shown in Figure 3.2, the simplest way to approximate the charge relaxation is by including a series bias-dependent resistance by each charge source. This topology also can reflect the symmetrical structure of the device especially at low drain-source voltages, while $Q_{gs} \approx Q_{gd}$ [34]. To incorporate the effect of C_{gs}, C_{gd}, and C_{ds} while maintaining the consistency of the large-signal model, the charge sources, Q_{gs} and Q_{gd}, can be formulated as given in Chapter – 5.

3.3 Device Characterization

Device characterization defines the reliability and accuracy of the device model. The reliability of small-signal model parameter extraction depends strongly on the measurement uncertainty. The measurement-based large-signal model relies heavily on the quality of the measurements. Therefore, due to the importance of the measurements, this section will give an overview about the main measurements, which are usually used for the device characterization and modelling.

3.3.1 DC IV Measurements

DC IV measurements of active devices are fundamental measurements for device modelling. The DC measurement set-up could be part of high frequency on-wafer (S-parameter) measurement system or included in a pulsed IV measurement system, explained later. Biasing and measurements are accomplished simultaneously by DC measurements. As the inherent self-heating is inevitable through these measurements, the delay time between each two measurements should be high enough to cool down the device. Therefore, the chances to obtain uncorrelated measurements are high through DC measurements. Such measurements cannot be used for RF device characterization because in RF situation the device temperature does not clearly change with the applied RF signal. For modelling of the gate-forward and gate-breakdown the device need to be characterized beyond the rate values of the device. The DC IV measurement system is unfit for this purpose because this can lead to physical (chemical) alteration for the device properties, or local destruction in the device structure.

3.3.2 Pulsed IV Measurements

Pulsed IV measurements can overcome the main limitations of the corresponding DC measurements. As mentioned in the previous section, modelling of self-heating induced current dispersion requires isothermal measurements. Also, due to temperature dependency of the trapping mechanism [35], this effect should be characterized under negligible self-heating, therefore, pulsed IV measurements can approach the isothermal condition. The pulsed IV measurements under appropriate quiescent bias conditions can also be used for trapping induced dispersion characterization [36]. Pulsed IV measurements offer a way to investigate the characteristic of the device in ranges where damage or deterioration can occur as pulsed measurements make it is possible to extend the range of measurements without harm [37].

3.3.3 S Parameter Measurements

The most common measurements utilized for characterization of active devices for small-signal model parameters extraction purposes are S-parameter measurements. These measurements can characterize small-signal performance of the device under certain bias conditions. Under this condition, the measurements are used to determine a unique set of values for small-signal equivalent circuit elements. From the dependency of the equivalent circuit elements on bias condition, large-signal model for the device can be derived. For more accuracy of the derived model, the measurements need to be performed over appropriate bias ranges varying from strong non-linear regions (ohmic, breakdown and forward). Accuracy of device measurements depends vastly on the system calibration and the de-embedding of the device test fixture [38].

4 BIAS DEPENDENT LINEAR ALGAN / GAN HEMTS MODEL

This chapter gives a glimpse of the linear modelling of the AlGaN/GaN HEMT. The chapter describes the electrical equivalent circuit implemented, the algorithm adopted for extraction of parameters and the results hence obtained.

4.1 OVERVIEW OF SMALL SIGNAL MODELLING APPROACH

The precision of a large signal model depends on efficiency of the small signal model. A small signal model derivation begins with defining an electrical equivalent circuit (EEC). There are various basic EEC given in literature over the years [39-40]. Having an accurate EEC depends on carefully studying the layout of the device taken into consideration along-with maintaining the aspects of device physics. The complexity of corresponding EEC increases with device layout, conductive substrate and underdeveloped device processing technology. The EEC of the small sized device in consideration can be modelled with less extrinsic parameters, hence an 18-element model has perfectly suited our requirements as shown in the Fig. 4.1. In this work, small-signal model parameters of a FET are extracted using available S-parameter data under different bias conditions over a range of frequencies in conjugation with physical layout and geometry data. S-parameter of different device sizes maybe predicted by the designers even if the small signal elements are scaled with gate width and the number of fingers of the device.

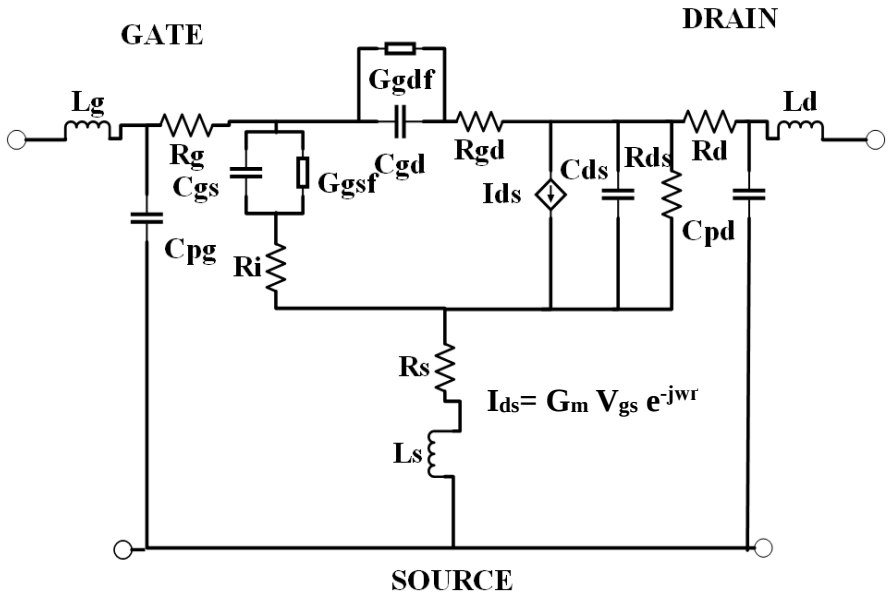

FIGURE 4.1 EQUIVALENT CIRCUIT OF A SMALL SIGNAL MODEL ADOPTED IN THIS WORK

The parameter extraction procedure is divided into two parts – extrinsic and intrinsic. Intrinsic part covers the active region below the gate. Extrinsic part represents the parasitic section, that are considered independent to the frequency of the applied RF signal and the bias point. In Fig. 4.1, L_g, L_s and L_d and R_g, R_s and R_d for gate, source and drain respectively show the distributed inductive and resistive effects due to electrodes enacting as transmission lines and C_{pd} and C_{pg} represent the parasitic capacitances due to pads, all these form the part of extrinsic circuit. Intrinsic parameters include forward conductance of gate-drain (G_{gdf}) and gate-source (G_{gsf}) regions. R_i and R_{gd} also form a part of the intrinsic circuit as explained by [41].

References [42-43], provide a standard procedure for estimating small signal model parameters. The success of the procedure depends on starting values of parameters chosen and the optimization done. In this work, a simplified algorithm is adopted for extracting various small signal parameters based on the device under test. The algorithm is presented as given in Fig. 4.2.

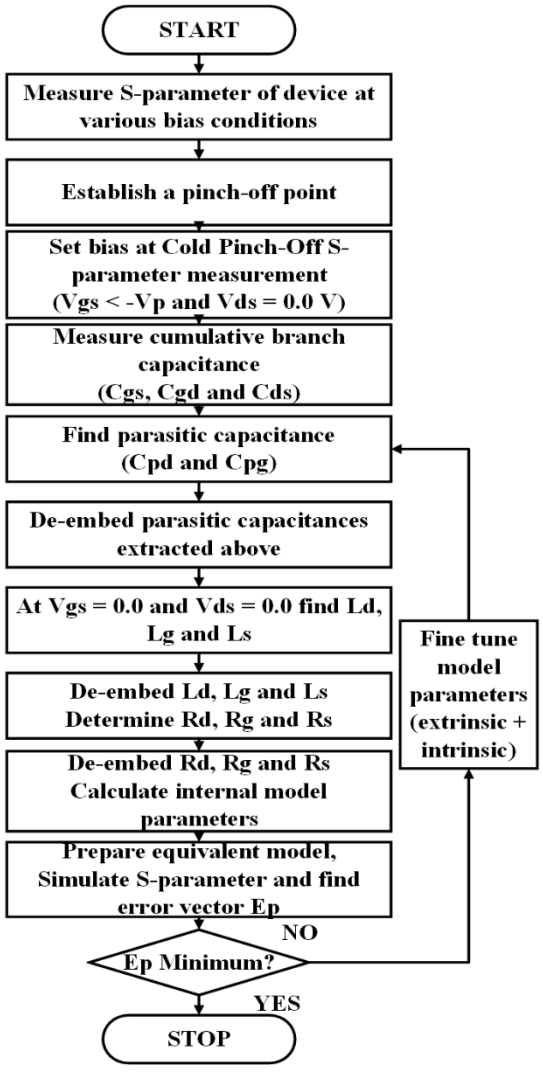

FIGURE. 4.2: FLOWCHART OF ALGORITHM FOR THE MODEL PARAMETER EXTRACTION

The extracted values of the extrinsic elements of the linear model are given in Table 4.1.

TABLE 4.1: EXTRACTED VALUES OF EXTRINSIC PARAMETERS

Extracted parameters	Values
L_g (pH)	138.34
R_g (ohm)	2.395
L_d (pH)	123.2
R_d (ohm)	1.2725
L_s (pH)	1.93
R_s (ohm)	1.1035
C_{pg} (fF)	170
C_{pd} (fF)	18

C_{gd} and C_{gs} form the parallel-plate capacitance with plates being formed by metal gate and 2DEG. With a constant V_{ds}, and V_{gs} decreasing from 0 to pinch-off voltage, negative charges accumulate at gate due to negative V_{gs} thereby reducing the charge storage at gate-source and gate-drain region. G_{gdf} and G_{gsf} depict the conduction currents through gate diodes. Hence, they grow with increasing forward bias on gate-voltage as can be seen from Fig. 4.3

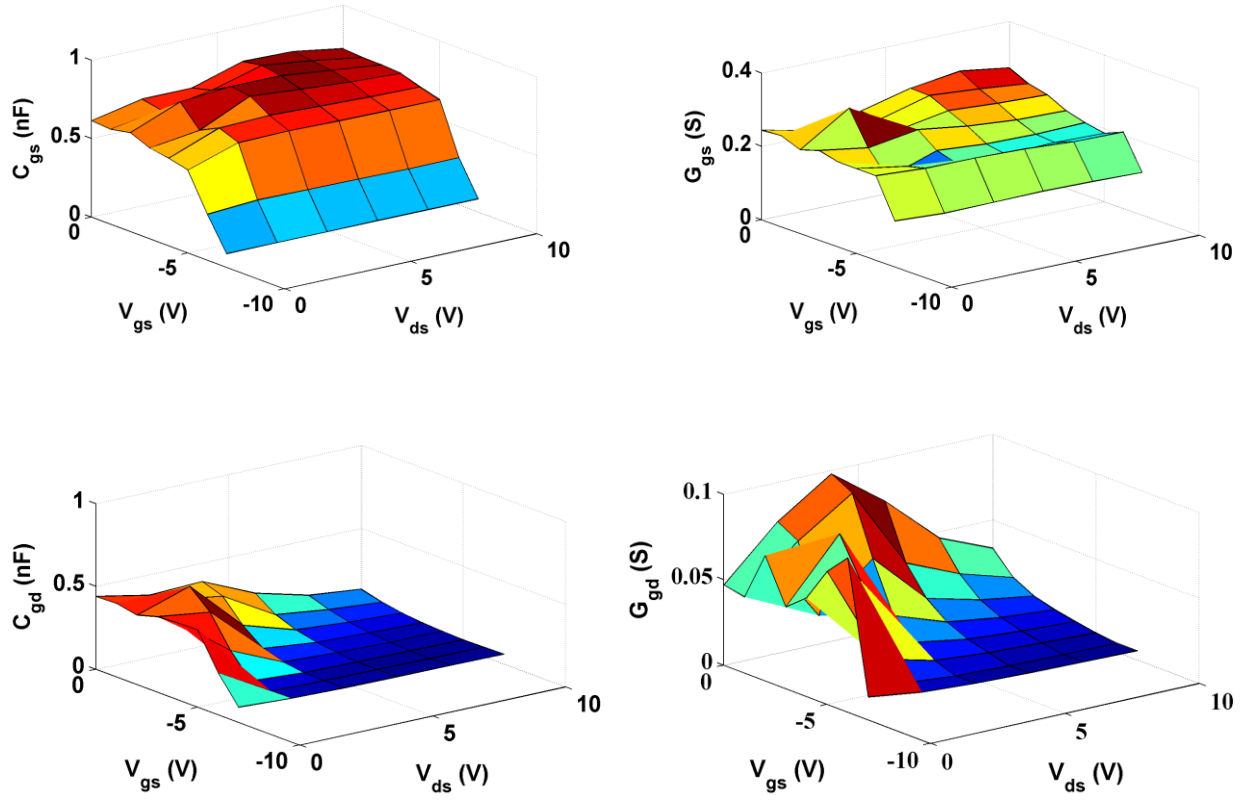

FIGURE 4.3(I): EXTRACTED LINEAR PARAMETERS AS A FUNCTION OF EXTRINSIC VOLTAGES FOR 4*100 µM DEVICE

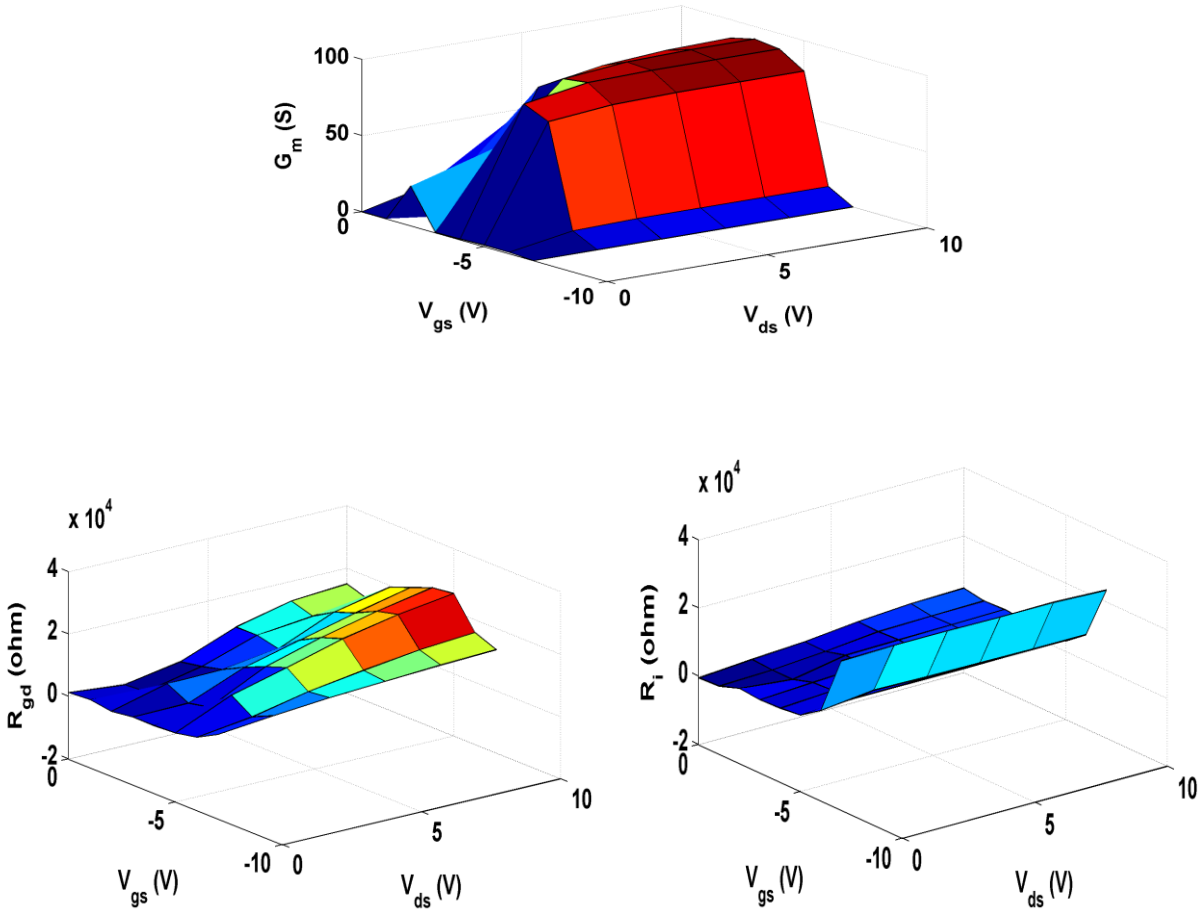

FIGURE 4.3(II): EXTRACTED LINEAR PARAMETERS AS A FUNCTION OF EXTRINSIC VOLTAGES FOR 4*100 µM DEVICE

5 PROPOSED STRATEGY FOR LARGE SIGNAL MODELLING

A precise description of the non-linear effects in a transistor is essential for optimal design of power amplifiers in modern technologies. For this, the small signal model should progress into a large signal model. The large signal model is empirical and derived from physically relevant distributed small – signal model derived in the last chapter.

The model is formulated using an electrical equivalent circuit (EEC) which is described initially. Next, the procedure of the model element extraction is explained. Moving on, the model implementation is shown in ADS. Finally, the model is verified.

5.1 LARGE SIGNAL MODELLING WITH ELECTRICAL EQUIVALENT CIRCUITS

Empirical large-signal models with equivalent circuits use non-linear sources of current and charge to represent the current flow in the transistor. These non-linear sources are voltage controlled and surrounded by linear circuit, known as the extrinsic elements. The current sources are conduction current sources, namely I_{gs} and I_{gd} [44] which can be understood as current components related to motion of charge carriers [45]. Q_{gs} and Q_{gd} characterize displacement current sources [44] which represent current components related to time varying accumulation of charge [45]. The non-quasi-static effect in the channel charge is modelled by two bias-dependent resistors Ri in series with Q_{gs} and R_{gd} in series with displacement current source, Q_{gd}. This improves the model simulation at milli-meter wave frequencies as it takes into account the charging time for capacitances in the depletion region. These charging times in the model are described by R_iC_{gs} and R_dC_{gd}. The non-quasi-static equivalent circuit adopted in this thesis is shown in Fig. 5.1

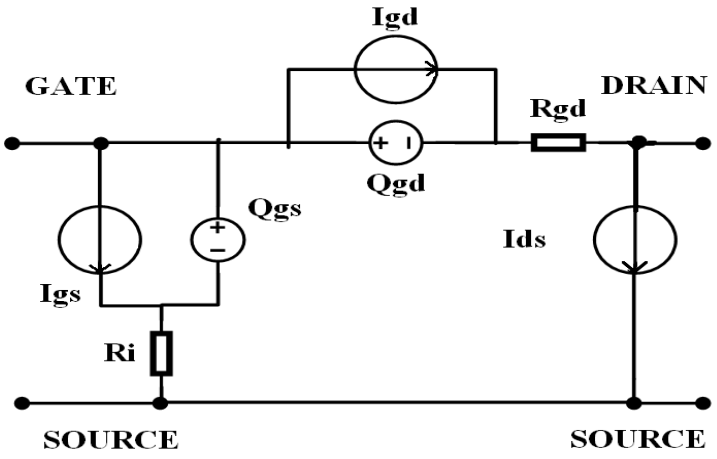

FIGURE.5.1: EQUIVALENT CIRCUIT ADOPTED FOR NON-LINEAR MODELLING OF GAN HEMT

The non-quasi-static equivalent circuit adopted for small-signal modelling in Chapter-4 corresponds well with the physical effects in the small signal. Furthermore, it has a topology which matches well with the non-quasi-static equivalent circuit of a large signal model.

5.1.1 GATE CHARGE MODELLING

The relationship between non-linear charge sources and linear intrinsic capacitance is expressed as follows, as [46].

$$Qgs\,(Vgs,Vds) = \int_{(Vgso,Vdso)}^{(Vgs,Vds)} Cgs\,dVgs + \int_{(Vgso,Vdso)}^{(Vgs,Vds)} Cds\,dVds \qquad (5.1)$$

$$Qgd(Vgs,Vds) = \int_{(Vgso,Vdso)}^{(Vgs,Vds)} Cgd\,dVgs + \int_{(Vgso,Vdso)}^{(Vgs,Vds)} (-Cgd - Cds)dVds \qquad (5.2)$$

The values of V_{gs0} and V_{ds0} represent the starting point of the integration. V_{gs0} and V_{ds0} can be chosen to be any arbitrary value from the V_{gs}-V_{ds} grid making the integration in the equations above to be path dependent as established by [46].

In the Chapter 4, bias-dependent extrinsic elements are extracted as a function of the extrinsic voltages V_{GS} and V_{DS}. For calculating displacement and conduction currents by integration it becomes imperative to consider the voltage drop across the extrinsic resistances as well. Hence, a correction needs to be done. The intrinsic voltages are thus calculated as shown-

$$Vds = VDS - (Rd + Rs)\,Ids - Rs\,Igs \qquad (5.3)$$

$$Vgs = VGS - (Rg + Rs)\,Igs - Rs\,Ids \qquad (5.4)$$

The voltage re-mapping as expressed by above equations (5.3) and (5.4) is evaluated with extracted values of R_g, R_s and R_d with the measured voltages and currents from the static-DC IV characteristics. The voltage-remapping implies that the intrinsic voltages V_{gs} and V_{ds} achieved are no longer orthogonal, which makes the integration of intrinsic elements difficult to achieve. Moreover, this representation is not convenient to be handled in Agilent ADS® which is ultimately required for simulating the circuit in CAD. Thus, numerical re-gridding must be applied on C_{gs}, C_{gd} and C_{ds} to achieve Q_{gs} and Q_{gd}.

In this thesis, the re-gridding is implemented using B-spline approximation technique, used for interpolation in MATLAB® [47]. B-spline approximation techniques unlike polynomial or Bezier are used for their high approximation accuracy to the supplied data and continuity of higher-order derivatives of the received data [47]. In b-spline technique polynomial basis function of degree k are used to force fitting curve to pass the data in a smooth manner. Therefore, it can maintain the continuity of the data and its higher derivatives up-to $(k-1)^{th}$ derivative [48]. On the other hand, b-spline techniques are not proved to be useful in extrapolating data, as they produce unreliable values. Fig 5.2, shows equidistant fitted data for

C_{gs} and Q_{gs} using cubic b-spline approximation technique. The required re-gridding only indicates interpolation, so that path-integral formulation can be applied.

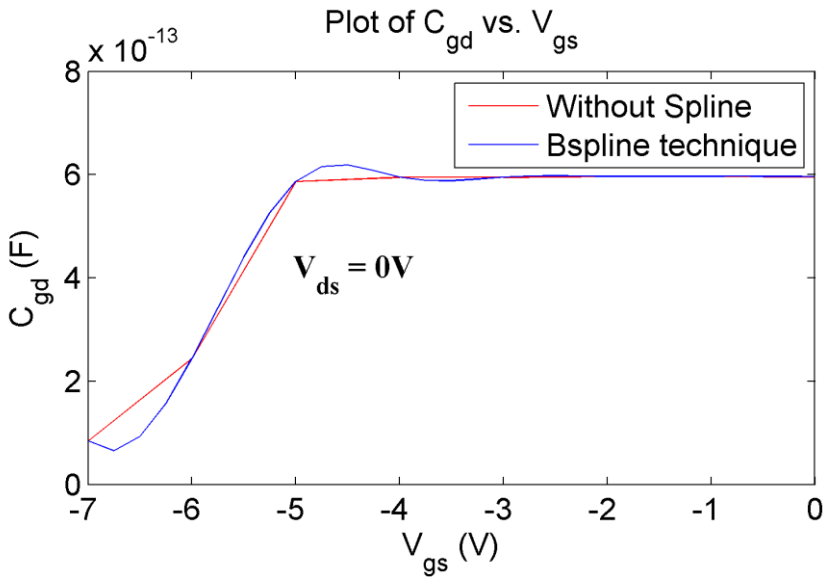

FIGURE 5.2: INTERPOLATION USING B-SPLINE TECHNIQUE AND WITHOUT USING ANY INTERPOLATION TECHNIQUE

In this thesis, grid regions without data points are termed as *off-range* regions. In this thesis, bias-dependent parameters are handled as MATLAB® arrays or stored in excel files, cells of the array which depicted values in the *off-range* region were given the string "*NaN"* (not-a-number) (This is the native way for MATLAB® to understand the value is not available while executing routines or doing calculations).

A problem arises when the b-spline approximation technique in MATLAB® automatically extrapolates value in the off-range region. Nonetheless, undesired extrapolation by the routine does not occur if it is forcefully configured to take up "*NaN*" value in the *off-range* region.

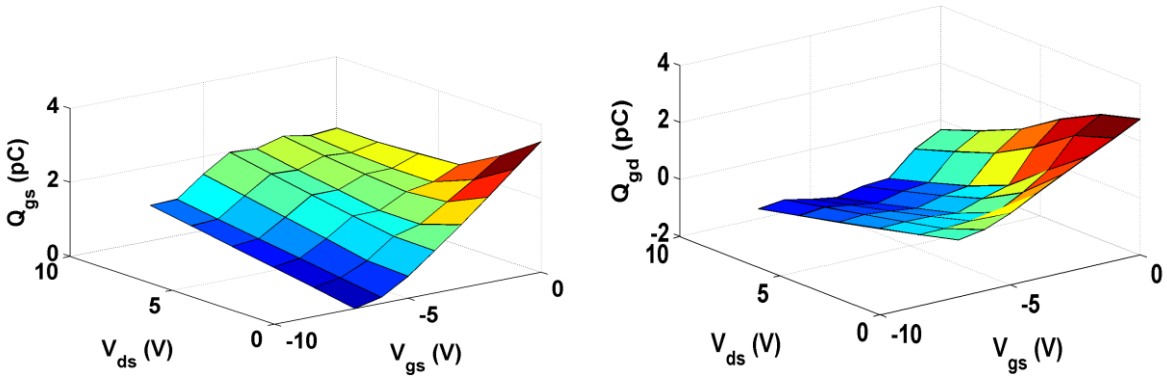

FIGURE. 5.3: CALCULATED GATE CHARGE SOURCES VERSUS INTRINSIC VOLTAGES V_{GS}-V_{DS} FOR THE DEVICE IN CONSIDERATION

As can be inferred from the Fig 5.2, b-spline approximation technique preserves the continuity of the data and it's derivative up-to 2nd derivative. This will improve the model simulation of inter modulation distortions and harmonics[49]. The intrinsic capacitances C_{gs}, C_{gd} and C_{ds} are integrated according to the equations (5.1) and (5.2), to find out Q_{gs} and Q_{gd}. The shapes of the curves obtained thereafter as depicted from Fig, 5.3, are similar to the ones reported by [41] for AlGaAs/GaAs HEMT. The values reported for Q_{gs} and Q_{gd} by integration can be written down in a CITI-file for implementation in ADS.

5.1.2 Gate Current Modelling

Gate currents I_{gs} and I_{gd} follow the similar modelling approach as gate charges Q_{gs} and Q_{gd}. Equations (5.5) and (5.6) [46], show the corresponding path-integrals of small-signal gate conductances G_{gsf} and G_{gdf} as expressed by following equations –

$$Igs\,(Vgs,Vds) = \int_{(Vgso,Vdso)}^{(Vgs,Vds)} Ggsf\; dVgs \qquad (5.5)$$

$$Igd(Vgs,Vds) = \int_{(Vgso,Vdso)}^{(Vgs,Vds)} Ggdf\; dVgs - \int_{(Vgso,Vdso)}^{(Vgs,Vds)} Ggdf\; dVds \qquad (5.6)$$

The G_{gsf} and G_{gdf} values originally extracted from V_{GS}-V_{DS} grid were re-gridded to express them on orthogonal V_{gs}-V_{ds} grid as done for C_{gs}, C_{gd} and C_{ds}.

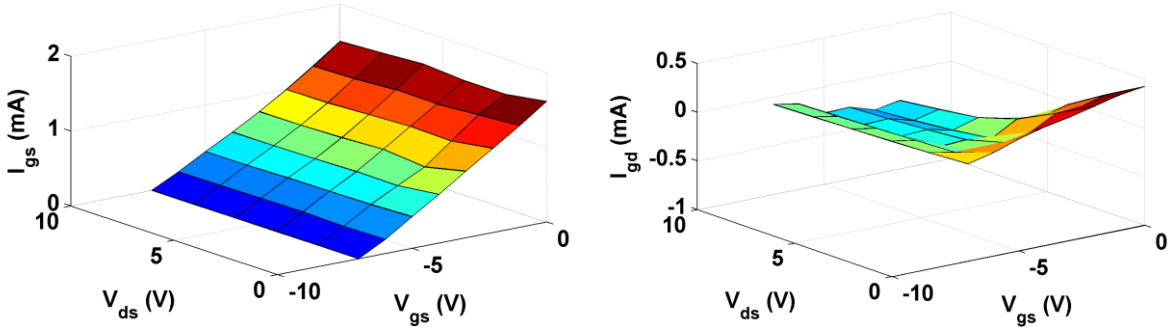

FIGURE. 5.4: CALCULATED GATE CURRENT SOURCES VERSUS INTRINSIC VOLTAGES V_{GS}-V_{DS} FOR THE 4*100 µM DEVICE UNDER TEST

The resulting I_{gs} and I_{gd} values exhibit expected dependency on the applied DC voltages, as depicted in Fig. 5.4. Significant effect of I_{gs} and I_{gd} is shown in the high-V_{gs} and low-V_{ds} region, since their calculation is based on G_{gsf} and G_{gdf}, whose major effect is observed in this region only.

For V_{gs} above 0V and growing I_{gs} agrees aptly with the expected exponential increase of the current of the gate-source diode when forward biased. Similarly, for V_{gd} (V_{gs}-V_{ds}) above 0V and

increasing I_{gs} agrees well with the expected exponential increase of the gate-drain diode when forward biased.

5.1.3 Drain Current Modelling

The most vital non-linear effect in the large signal model is the drain current source. It is a well-known fact that for HEMTs drain current has a more promising effect on the model than the gate displacement and conduction currents.

Quoting [50], Ids is affected by: (i) device self-heating and charge trapping known as low-frequency dispersive phenomena (ii) spatial delays of the charge to rearrange the 2DEG known as the non-quasi-static effects. Dynamic effects when accredited to self-heating and charge trapping are termed as long-term memory effects, and when attributed to non-quasi-static phenomena are termed as short-term memory effects.

The parameter Γ extracted in the Chapter-4, stands for the propagation delay of the electrons in the 2DEG and it signifies the non-quasi-static effects of I_{ds}. However, an additional model design for the drain current is needed to account for low-frequency dispersive phenomena, where the time constants are longer than the period of the RF signal. Pulsed DC-IV measurements measured from a *quiescent* bias point is related to the device RF response on that bias point. As suggested in [51], measured data of pulsed-DC IV represents a suitable database for the large-signal modeling of Ids in measurement-based models.

Definitions of the adopted I_{ds} Model

According to [29], proposed empirical model for Ids calculation for GaAs MESFETs based on pulsed-DC IV measurements is given as –

$$Ids\ (vgs, vds) = Ids(Iso)(vgs, vds) + \alpha G(vgs, vds)(vgs - Vgs) + \alpha D(vgs, vds)(vds - Vds) \qquad (5.7)$$

Definition 1: v_{gs} and v_{ds} are voltage signals at intrinsic ports of the device. V_{gs} and V_{ds} represent the average value of the signals. The time varying component of these signals are v_{gs}-V_{gs} and v_{ds}-V_{ds}.

Definition 2: $I_{ds}^{Iso}(v_{gs}, v_{ds})$ represents a theoretical isothermal DC IV characteristic of an operation with constant channel temperature.

Definition 3: The functions $\alpha_D(v_{gs}, v_{ds})$ and $\alpha_G(v_{gs}, v_{ds})$ represent the differences between static and dynamic drain current (I_{ds}) due to charge trapping, for each pair of instantaneous voltages v_{gs}, v_{ds} applied to the device.

5.2 LARGE SIGNAL MODEL IMPLEMENTATION

The derived nonlinear elements Q_{gs}, I_{gs}, Q_{gd} and I_{gd} are written in tables versus V_{gs} and V_{ds} in an output file. Values of intrinsic resistances R_{gd} and R_i, transconductance time delay, transconductance values are also defined as bias-dependent table based elements in the same output file as previous one. These elements, are written in a conventional CITI-file format which have orthogonal set of V_{gs} and V_{ds} values. Fig. 5.5, presents the implementation of the table-based large signal model in Agilent ADS®. The extrinsic elements i.e. R, L and C are represented as lumped passive elements. The intrinsic non-linear elements are represented in a Symbolically Defined Device (SDD). The first two ports contain displacement and conduction current elements. The next two ports have non-quasi-static elements namely, R_i and R_{gd}. The drain current is implemented from port 5. The values from the CITI-file are read into the model i.e. into SDD from Data Access Components (DACs).

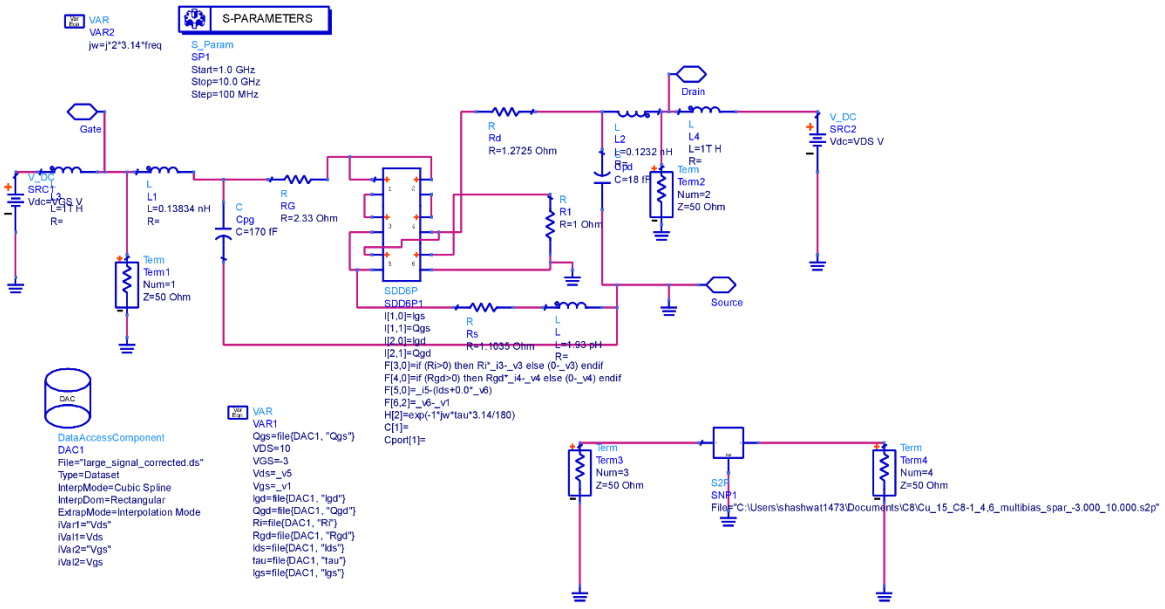

FIGURE. 5.5: IMPLEMENTAION OF LARGE SIGNAL MODEL IN AGILENT© ADS

5.3 SIMULATION AND MEASUREMENT RESULTS

The developed large-signal model is simulated and verified by standalone measurements, DC-IV and S parameter measurements from which this large signal model is derived.

5.3.1 S PARAMETER

S-parameter simulations are verified against the measurement results in Fig 5.6. The simulation and measurement results show good agreement showing there is consistency between the large signal and small signal model.

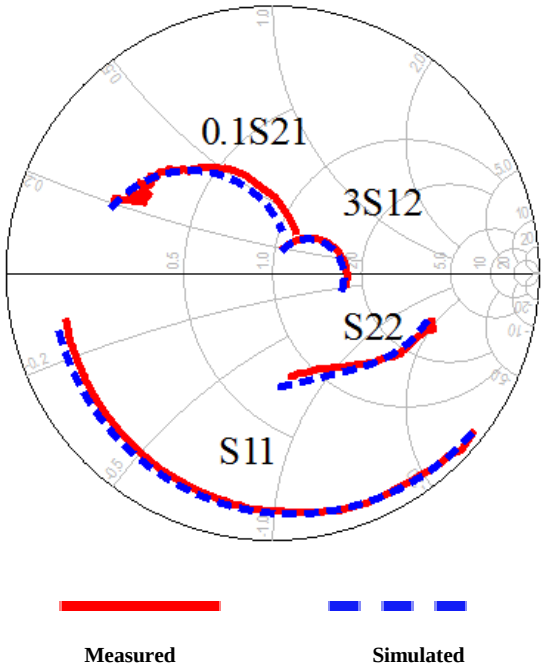

FIGURE. 5.6: S PARAMETERS (FREQUENCY 1 GHZ TO 10 GHZ.) OF THE DEVICE. MEASURED (RED LINES) AND SIMULATED (BLUE DOTTED LINES) RESULTS AT BIAS POINT V_{GS} = -3V AND V_{DS} = 10V

At the above-mentioned bias point, i.e. V_{GS} = -3V and V_{DS} = 10V the error percent is 4% between simulated and measured result. In the two systems, due to different measurement uncertainties (calibration procedure, measurement procedure, probe tip position etc.) small discrepancy between simulated and measured results in seen by the S-parameter analysis. Average error across all bias points is calculated to be 7.33%.

5.3.2 IV CHARACTERISTICS

Fig. 5.7, shows pulsed IV simulations. There is a very good agreement between measurements and simulations showing the ability of the model for describing several non-linear effects.

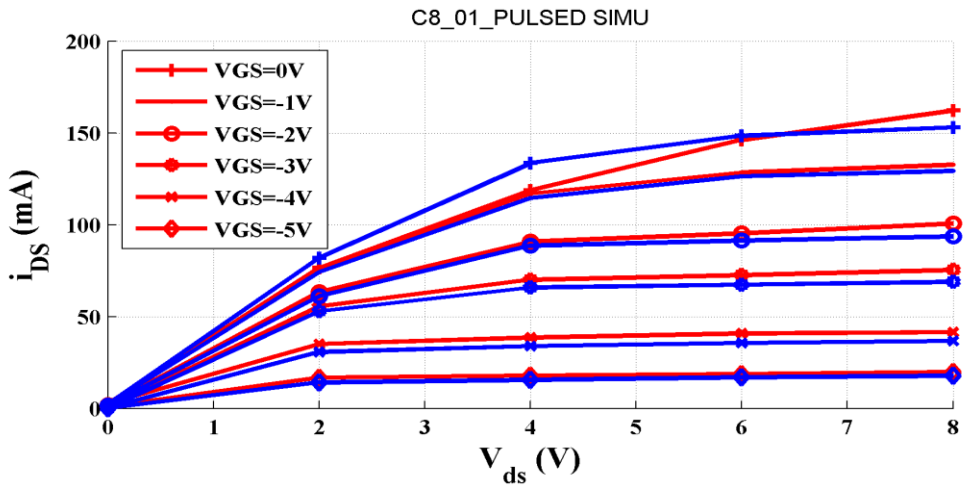

FIGURE. 5.7: PULSED-DC IV MEASUREMENTS (RED LINES) AND SIMULATED RESULTS (BLUE DOTTED LINE) AT DIFFERENT QUIESCENT BIAS POINTS.

6 CONCLUSION & FUTURE WORK

This chapter summarizes the research work done in this dissertation. Also, future prospects of this research are discussed.

6.1 CONCLUSION FROM RESEARCH RESULTS

The thesis started with outlining the motivation for large-signal modelling of a AlGaN HEMT. The primary goal remains to be the need for large-signal models capable of predicting the linearity of the device precisely and accurately. The availability of such models facilitate designing HPA using AlGaN transistors.

The large-signal modelling process starts with small-signal modelling of the device. In this thesis, a large signal model is developed from a physics-relevant small-signal equivalent circuit model by using bottom-up modelling technique. The small-signal model topology is constructed to account for the main physical and electrical characteristics of the small size high power devices of dimensions 4*100um. The characteristics include parasitic, gate-forward and gate-breakdown effects. An efficient algorithm for reliable extraction of small-signal model parameters was adopted. The extrinsic parameter extraction part in the small-signal model required high-quality starting values which were generated using cold S-parameter measurements. Afterwards, optimization process was carried out which required searching for optimal values for the extrinsic parameters. In the intrinsic parameter extraction part, an efficient technique was proposed for optimal extraction.

The extracted intrinsic gate capacitances and conductance of the linear model were integrated to find the displacement and conduction currents of the large signal modelling assuming that these elements satisfy the integral path-independence condition. The intrinsic channel conductances are very delicate for the trapping and self-heating effects, therefore these can't be used to model drain current. For calculating drain current pulsed DC-IV measurements at different quiescent bias points to account for such effects are required. It is found that using b-spline approximation technique for interpolation can improve the capability of the model for harmonics and IMD simulations. The approximation can maintain the continuity of the higher order derivatives of the currents and charges, hence it reduces the measurement uncertainty especially near the pinch-off region. All the bias dependent model parameters have been formulated in terms of intrinsic voltages but derived from data at extrinsic device ports. Hence, re-gridding technique had to be applied. In this thesis, this approximation technique was used to construct model database, which is saved in a data file (look-up table) in Agilent ADS®.

The large-signal modelling process was completed and the model was implemented in Agilent ADS®. Successful model verification under different excitation signals has been completed. The model verification was conducted at different modelling stages. The S-parameter simulation of the large-signal model showed good comparison to the data obtained from measurements. These tests confirm the consistency of the large-signal model.

Pulsed DC-IV measurements agree well with the simulation results confirming that the large-signal model predicts well the drain current under pulse excitations.

6.2 Future Work

Measurement based large-signal modelling techniques will remain as the most practical approach for power FETs modelling. The challenges in modelling of FETs with increasingly larger size and greater power handling capacity should be tackled with measurement based approach. As the device size increases certain complex physical processes occur within the device and it requires a more refined electrical equivalent circuit for modelling. Challenges related to table-based model implementation should also be resolved. Robust and reliable interpolations and extrapolations technique should be there and/or use of combined analytical and table-based data. Furthermore, the large signal model presented in this thesis can be used to measure characteristics of a High Power Amplifier like Inter Modulation Distortions etc.

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