A High-Efficient Current-Mode PWM DC-DC Buck Converter Using Dynamic Frequency Scaling

by

Ankit Rehani

A thesis submitted in partial fulfillment for the
degree of Master of Technology

under supervision of
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Department of Electronics and Communication Engineering
Indraprastha Institute of Information Technology, Delhi

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Certificate

This is to certify that the thesis titled "A High-Efficient Current-Mode PWM DC-DC Buck Converter Using Dynamic Frequency Scaling" being submitted by Ankit Rehani (Roll No.- MT16085) to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original work carried out by him under my supervision. In my opinion, thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The results contained in the thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

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Abstract

Power Management Integrated Circuits (ICs), such as high-efficient switched mode dc-dc converters are essential building blocks in portable battery operated devices. This work presents design and implementation of a novel high-efficiency current-mode pulse width modulated (PWM) buck converter with dynamic frequency scaling. This circuit is capable of ensuring high efficiency under different load conditions, by dynamically changing the frequency of operation with respect to the load current with the help of a novel frequency decision circuit. In addition, soft start operation protects the circuit from large in-rush current during start up of the converter. The proposed circuit is implemented in TSMC 16nm CMOS technology. Simulation outcome has shown an output voltage of 0.8V, when the input voltage is ranging from 2.3 to 3.6V, with a maximum conversion efficiency of 92.25% (heavy loads) and 92.11% (light loads), making this circuit quite useful in power management ICs.

Lower technology nodes such as 16nm dont allow voltage more than 1.8V across their junctions. In this work, 3.3V input supply is converted to 0.8V to supply a digital logic block of memory controller used in micro SD card. The design ensures the difference between no two junction voltages exceed 1.8V.

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This work is dedicated to my parents, Late Sh. Mukesh Rehani and Mrs. Sonia Rehani for their teachings and values passed on to me. I thank their understanding even in those moments in which my immaturity prevailed. To my brother, Akshay Rehani for all his support and friendship throughout these years.

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Contents

List of Figures

List of Tables

Dedicated to my beloved parents...

Chapter 1

Introduction

Most hand-held and battery operated electronic devices require power management solutions to enhance their battery life. High-efficient switched mode power converters (SMPC) are an integral part of such power management solutions. A voltage regulator ensures reliable and constant supply voltage under varying load currents. Voltage regulators can be broadly classified into two types: Linear regulators and switching regulators. The choice of regulator in our work is based on the application requirements. The regulator is required to convert an external unregulated supply voltage of 2.3-3.6V (from Li-ion battery) to a regulated 0.8V supply voltage. This voltage is used to drive digital logic blocks inside a memory controller. The digital blocks can consume currents in the range of 400mA. Pulse wdth modulated (PWM) SMPCs have power efficiency above 90% for these range of load currents. Hence, if a PWM based dc-dc buck converter is used, the current drawn from the main power supply would be 75% lesser than in the case of linear regulator. It is so because linear regulator efficiency can never be greater than the voltage conversion ratio. Hence, our work implements a current-mode PWM dc-dc buck converter for driving digital logic blocks in a memory controller die. A novel dynamic frequency scaling technique is implemented to improve the efficiency of the voltage regulator over wide range of load currents.

The use of SMPC as a power management solution reduces the amount of current flowing in the power divider network that transfers external power supply to the input pad of memory controller die [2] [3]. This reduces the resistive drops in the power divider network and also limits the increase in ambient temperature for the die.

1.1 Motivation

In high performance applications such as memory controller processing blocks, voltage regulator block is indispensable. The regulation is required in high-performance applications where systems are increasingly more integrated. Voltage scaling is important as it ensures power density of ICs remains below a certain limit to ensure reliability of semiconductor devices. It is desirable that higher voltages are supplied to the input pad of ICs such that resistive voltage drops due to off-chip power divider network can be reduced [2] [3]. Hence, the power management solutions in most portable devices are used to generate a constant or programmable output power supply from high range input supplies (e.g., Li-ion: 2.3-3.6V).

Lower technology nodes such as 16nm don't allow voltage more than 1.8V across their junctions. The cascode structure of the power switches used in [4] provides a way to generate low output voltages from a high input voltage supply using a switched mode power converter (SMPC). The design ensures the difference between no two junction voltages exceed 1.8V. Hence, ensuring reliability of the devices. However, the design suffers from high losses at low and medium load currents. To utilize the maximum benefits of switching converters, power efficiency needs to be improved for full range of load currents. Fixed frequency PWM dc-dc converter provides high efficiency for high loads (active mode), whereas, it has poor efficiency for light loads (stand-by mode) [5] [6]. Improving power-efficiency during stand-by mode is important to increase run time of devices, such as, mobile phones, PDAs etc.

1.2 Objectives

The objective of this thesis is to develop a high-efficient current-mode PWM dc-dc buck converter. PWM based control is chosen as it provides high efficiency at high load currents. Current controlled PWM is employed instead of voltage controlled PWM as it allows faster transient response [6] [7]. However, improving efficiency of the converter at low load currents is still a challenge. Some techniques that can address this limitation includes: operating PWM dc-dc buck converter in Discontinuous Conduction mode (DCM) [8] and in dual-mode [9]. In [8], a zero-current crossing detection circuit is used to reduce conduction losses during discharge-phase of the regulator. In [9], the characteristics of Pulse Frequency Modulation (PFM) control is used to improve efficiency at low load currents. In both the techniques, efficiency in stand-by mode is improved. However, [8] only removes conduction losses for light loads, whereas, [9] uses an extra control loop for regulating the same output voltage.

This work proposes a novel dynamic frequency scaling technique to improve the efficiency of current-mode PWM control dc-dc converter. The current sensing circuit required for current controlled architecture is used to develop a novel frequency decision circuit which improves the efficiency of the system over wide range of load currents. The dc-dc buck converter in this work is designed on TSMC 16nm CMOS technology to covert 2.3-3.6V input voltage to 0.8V output voltage which can support upto 400mA current. The use of SMPC to supply a regulated 0.8V voltage to digital blocks of a memory controller allows better system efficiency. The regulator requires the PWM control system for stable closed loop feedback regulation. The off-chip components are: inductor (L = 4.7μH), capacitor (C = 10μF) with equivalent series resistance of $R_{ESR} = 200m\Omega$. The high values of LC filter reduce the ripples at the output voltage node. Whereas, a high value of R_{ESR} can increase the UGF of the system and cause ripple amplification. The ripple amplitude at the output voltage is limited to 4mV peak-to-peak voltage.

1.3 Structure of the Work

This thesis is divided in 6 chapters to reflect the necessary information that lead up to the complete design of the regulator system.

- **Chapter 2: Switching Voltage Regulators**
  This chapter gives the description about the basic structure of a switching regulator and terminologies related to a switching regulator.
- **Chapter 3: Control Systems for SMPC**
  This chapter discusses different types of control systems that can be implemented for a switching regulator. This chapter will explain why current-mode PWM control is chosen in this work.
- **Chapter 4: System design**
  This chapter discusses about the design and implementation of proposed current-mode PWM dc-dc buck converter. All the different blocks would be discussed along with the proposed frequency decision circuit. Design steps for each block would be explained on the basis of system level specifications.
- **Results and Discussion**
  This chapter shows the results of the proposed switching voltage regulator.

- **Conclusions**
  This chapter concludes all the findings and contributions of this work and discusses about possible future work.

Chapter 2

Switching Voltage Regulator

Switching regulators are preferred over their linear counterparts due to the advantages highlighted in Chapter 1. When the conversion ratio is as low as 0.25 (V_{OUT}/V_{IN} = 0.8V/3.6V), the linear regulator's efficiency can at best be 25% (assuming 100% current efficiency). Linear regulators offer poor efficiency because they achieve voltage conversion by dissipating the excess power into a resistor. Whereas, switching regulators use energy-storing passive elements and switches to alter the connections between them. This mechanism allows switching regulators to achieve dc-dc voltage conversion with high efficiency.

The basic circuit diagram for an ideal switching dc-dc buck converter is shown in Fig. 2.1. The circuit can operate in two modes based on the behaviour of current ($I_L(t)$) flowing through the inductor. Both the conduction modes (continuous and discontinuous) will be discussed in this chapter. All the different parameters associated with a switching regulator, such as voltage conversion ratio, conversion efficiency and output voltage ripple will be discussed in this chapter. Various conclusions and trade-offs will be drawn on basis of these discussions. Impact on efficiency and voltage conversion ratio will be seen when ideal switches are replaced by MOSFET switches in the circuit shown in Fig. 2.1.

2.1 Continuous Conduction Mode

As the name suggests, in this mode of operation for inductive dc-dc buck converter, the inductor current remains continuous in both the complementary clock phases, ϕ_1 and ϕ_2. The principle of operation for continuous conduction mode (CCM) can be explained on the basis of inductor charging and discharging phase, as follows:

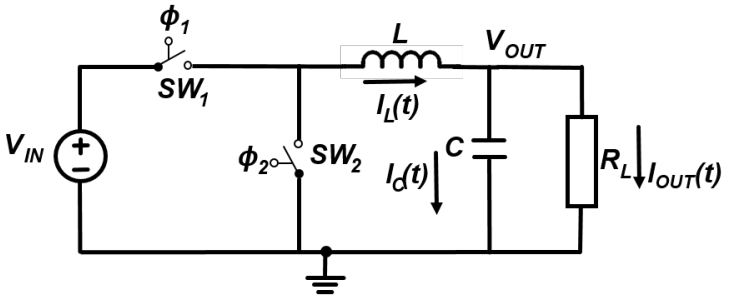

FIGURE 2.1: Circuit diagram of an ideal switching dc-dc buck converter.

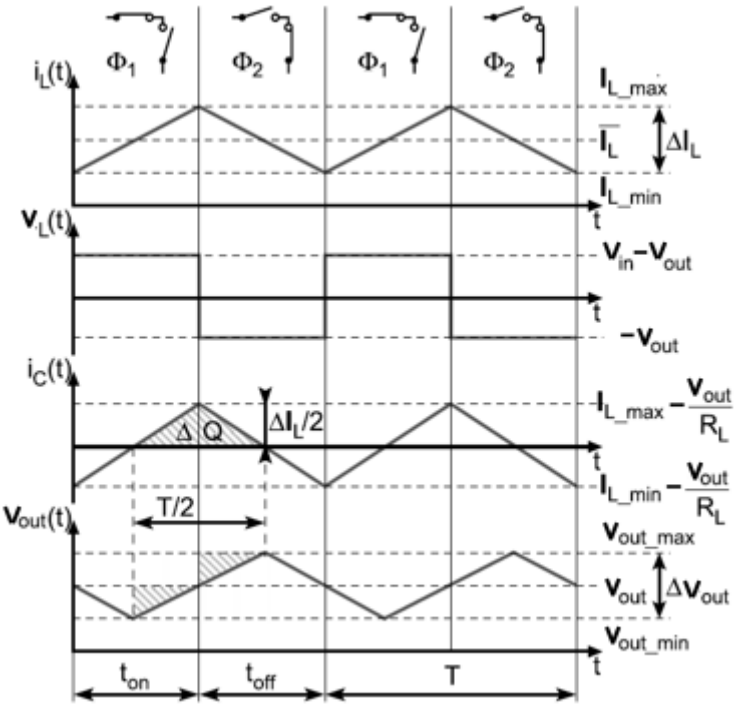

FIGURE 2.2: Working of an ideal switching dc-dc buck converter in CCM [1].

- ***The inductor charge phase*** ϕ_1**:** This phase occurs when switch SW_1 is closed and switch SW_2 in Fig. 2.1 is opened for a certain on-time t_{on}. During ϕ_1, inductor 'L' is charged in series with capacitor 'C' and load 'R_L'. This action makes inductor current to increase from its minimum value (I_{L_min}) to its maximum value (I_{L_max}), as depicted in Fig. 2.2. The average value of inductor current ($\bar{I_L}$) would be equal to the load current (I_{OUT}). Therefore, when inductor current is less than its average value, it needs help from the charge stored in capacitor to supply the load current. Hence, there is a small decrease in the output voltage due to the lost charge in capacitor. Similarly, when inductor current becomes more than the load current (due to the charging by the supply V_{IN}), capacitor 'C' is also charged. Hence, there is a rise in output voltage.

- ***The inductor discharge phase*** ϕ_2**:** The regulator enters this phase when the

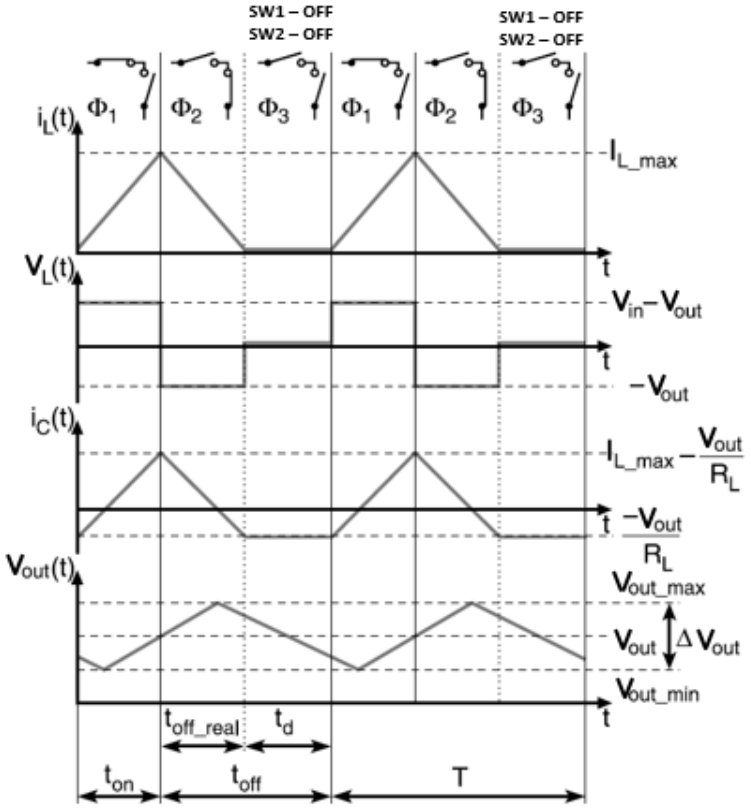

FIGURE 2.3: Working of an ideal switching dc-dc buck converter in DCM [1].

control system of the regulator detects that output has risen above the desired value. This detection makes the switches to flip their state i.e. switch SW_1 is opened and SW_2 is closed for a certain off-time t_{off}. The working and circuit implementation of the control system is explained in Chapter 3 and 4. During this phase inductor current is discharged into 'C' and 'R_L'. When inductor current becomes less than the dc-load current (I_{OUT}), the load is powered by the discharging inductor and capacitor. The loss in charge of capacitor causes V_{OUT} to drop below its desired value, in response to which the control system again kicks in the charging phase ϕ_1 and the cycle continues.

2.2 Discontinuous Conduction Mode

In discontinuous mode, the inductor current varies between a finite positive value and zero. This mode experiences a 'dead-time' in which there in no current flowing through the inductor and output load current is supported by capacitor alone. The principle of operation for discontinuous conduction mode (DCM) can be seen in Fig. 2.3. The working is explained in the following three phases:

- ***The inductor charge phase*** ϕ_1**:** This phase occurs when switch SW_1 is closed and switch SW_2 in Fig. 2.1 is opened for a certain on-time t_{on}. During ϕ_1, inductor 'L' is charged in series with capacitor 'C' and load 'R_L'. This action makes inductor current to increase from zero to its maximum value (I_{L_max}), as depicted in Fig. 2.3.

- ***The inductor discharge phase*** ϕ_2**:** This phase occurs when switch SW_1 is opened and switch SW_2 in Fig. 2.1 is closed for a certain off-time t_{off_real}. During this phase inductor current is discharged into 'C' and 'R_L', causing it to fall from its maximum value to zero. The condition when inductor current falls to zero occurs when load current is less than half of the peak-to-peak inductor current. The mathematical expression of this condition and its dependence on circuit parameters would be explained in next section 2.3.

- ***The dead-time phase*** ϕ_3**:** The regulator enters this phase when the control system detects a *zero-crossing* of inductor current. In this phase, both the switches SW_1 and SW_2 of Fig. 2.1 are opened. Hence, in this phase the output load current is drawn from the charge stored by the capacitor 'C', as shown in Fig. 2.3.

2.3 Performance Parameters

All the different performance parameters for a switching dc-dc buck converter would be discussed in this section. The concept of capacitor charge balance and inductor voltage-second balance [1] will be used to enable quick derivations of all the parameters.

2.3.1 Voltage Conversion Ratio

Voltage conversion ratio is an important parameter for any regulator. In a switching dc-dc regulator, it controls the duty cycle (D) of the switching clock. Therefore, the parameters t_{on}, t_{off} and/or t_{dead} are directly related to the voltage conversion ratio of the regulator (V_{OUT}/V_{IN}). It can be derived by applying voltage-second balance equation for the inductor 'L'. 'L' has a voltage 'V_{IN} - V_{OUT}' across it in time t_{on}, and 'V_{OUT}' in time t_{off} for CCM operation. Using these conditions and inductor voltage-second balance equation, voltage conversion ratio can be determined as shown in equation 2.1

$$\begin{aligned} (V_{IN} - V_{OUT}) * t_{on} - V_{OUT} * t_{off} &= 0 \\ \frac{V_{OUT}}{V_{IN}} = \frac{t_{on}}{t_{on} + t_{off}} &= D \end{aligned} \tag{2.1}$$

Similarly, voltage conversion ratio can be derived when regulator is in discontinuous conduction mode. For DCM, the expression is the same as in equation 2.1 but the time period of clock is '$t_{on} + t_{off} + t_{dead}$'. The absence of load current from the expression of V_{OUT}/V_{IN} shows that for an ideal switching dc-dc regulator, power conversion efficiency is 100%. Theoretically, this is possible because output voltage can be obtained by the clock (which controls the switches of the regulator) parameters. Hence, the power conversion efficiency would be 100%, independent of the load current as there is no concept of controlling the resistor divider network to regulate the output voltage.

2.3.2 Power Efficiency

Power efficiency is the ratio of power delivered to the regulated output by the power taken from the unregulated supply. As seen from the voltage conversion expression, as output voltage is independent of load current, the power efficiency should be 100%. To prove this, we need to take charge balance equation for the input voltage source V_{IN} (fig. 2.1). The input voltage source delivers a current of I_{OUT} in time t_{on} and zero current in time t_{off}. Using these conditions and applying charge balance equation for input voltage source, I_{OUT}/I_{IN} can be determined and power conversion efficiency can be computed, as shown in equation 2.2.

$$
\begin{aligned}
I_{OUT} * t_{on} - I_{IN} * (t_{on} + t_{off}) &= 0 \\
\frac{I_{OUT}}{I_{IN}} = \frac{t_{on} + t_{off}}{t_{on}} &= \frac{1}{D} \\
Power\ \ efficiency = \frac{V_{OUT} * I_{OUT}}{V_{IN} * I_{IN}} = \frac{D}{D} &= 1
\end{aligned}
\tag{2.2}
$$

2.3.3 Output Voltage Ripple

The working of CCM and DCM explained that both inductor current and output voltage are not constant and oscillate about their respective average value. Here, the inductor current and output voltage ripple will be computed. From the expression and theoretically, it would be seen how these parameters can be minimized from certain circuit parameters. From Fig. 2.2 it can be seen that inductor voltage $V_L(t)$ is 'V_{IN} - V_{OUT}' for time t_{on} and '$-V_{OUT}$' for time t_{off}. Using these conditions inductor current ripple ($\Delta I_L = I_{L\_max} - I_{L\_min}$) can be derived as shown in equation 2.3. From the equation for ΔI_L, it can be seen that inductor current ripple can be minimized by either increasing the frequency of clock generated by the control system that controls the switches of the

regulator or by increasing the inductor value. In both cases, time period of the clock is made smaller than the time constant (L/R) of the regulator to reduce ΔI_L.

$$
\begin{aligned}
I_L(t) &= \frac{1}{L}\int_0^{t_{on}+t_{off}} V_L(t)dt \\
\frac{\Delta I_L}{I_{OUT}} &= \frac{V_{OUT} * t_{off}}{L * I_{OUT}} \\
\frac{\Delta I_L}{I_{OUT}} &= \frac{(1-D) * (t_{on}+t_{off})}{\frac{L}{R}}
\end{aligned}
\tag{2.3}
$$

From Fig. 2.2 and explanation of CCM operation, it can be observed that capacitor current ripple is same as that of inductor current ripple. Voltage ripple is caused due to the excess charge pumped into capacitor as inductor current becomes greater than the load current. Using these conditions and equation 2.3, output voltage ripple can be computed as shown in equation 2.4. It can be seen from equation 2.4 that output voltage ripple can be reduced by either increasing the clock frequency or by increasing circuit parameters 'L' and 'C'. In both the cases, time period of clock is made smaller than the natural frequency of LC filter to reduce ΔV_{OUT}. Here, output voltage ripple dependence on capacitor depicts that if capacitor has more charge holding capacity then it can sustain load current for a longer time. The dependence on inductor is there because inductor controls the amount of current supplied to the output voltage terminal.

$$
\begin{aligned}
\Delta V_{OUT} &= \frac{1}{C}\int_0^{(t_{on}+t_{off})/2} I_C(t)dt \\
\Delta V_{OUT} &= \frac{1}{2} * \frac{t_{on}+t_{off}}{2} * \frac{\Delta I_C}{2} * \frac{1}{C} \\
\frac{\Delta V_{OUT}}{V_{OUT}} &= \frac{(1-D) * (t_{on}+t_{off})^2}{8LC}
\end{aligned}
\tag{2.4}
$$

2.3.4 DCM and CCM Boundary Condition

For designing a switching dc-dc buck converter, it is important to know for what conditions and load currents the circuit would operate in either discontinuous or continuous conduction mode. It is so because power efficiency can be optimized according to that. In next sub-section, discussion on power efficiency would be done. Here, boundary condition for CCM and DCM is discussed. The regulator will move from CCM to DCM when the load current becomes half of the inductor current ripple. Using this condition and equation 2.4 this condition can be derived as shown in equation 2.5.

$$\frac{V_{OUT}}{R_L} < \frac{\Delta I_L}{2}$$

$$\frac{V_{OUT}}{R_L} < \frac{V_{OUT} * (1-D) * (t_{on} + t_{off})}{2 * L}$$

$$\frac{2 * L}{R_L * (t_{on} + t_{off})} < (1-D) \tag{2.5}$$

2.3.5 Impact of non-ideal components on Efficiency

The discussion thus far has considered ideal switches, for which the power conversion efficiency can be shown to be 100%. In reality, these switches would be implemented by MOSFETs (either nMOS or pMOS switch based on where the switch is placed). The regulator efficiency depends on the losses that are incurred in these switches. Majorly, they suffer from two types of losses:

- **Conduction losses**: This type of loss is mainly due to the non zero on-resistance of the switches during on-state and a high but finite off-resistance during off-state. For applications having high load currents, they are dominated by the I-R (or V_{DS}) drop of the switches. These are the dominant losses for the regulator for high or medium load currents.
- **Switching losses**: These losses incur during the switching operation, where both current through the switch and voltage across it is non-zero. They are dominant losses for the regulator for low load currents.

2.4 Summary

In this chapter, working of a inductor based switching dc-dc buck regulator was discussed. The behavior of circuit in these two modes and dependence of various performance parameters on circuit parameters was discussed. Later, power losses due to the switches was discussed. The choice of control system will depend on the application of the regulator. In our design, a regulated output voltage of 0.8V needs to be generated from an unregulated 3.6V supply, which can support high load currents upto 400mA. As discussed in this chapter, for high load currents, the conduction losses are dominant. Hence, the choice of control system to be used should be made accordingly. In this next chapter, it would be explained that why this design follows a pulse-width modulated (PWM) control system. In addition to that, drawbacks of the control system would be discussed and the how the novel dynamic frequency scaling concept can reduce those drawbacks and enhance the power conversion efficiency for low load currents.

Chapter 3

Control Systems

In the previous chapter, it was deduced that output voltage depends solely on clock parameters. Hence, the switching dc-dc converter needs a mechanism that can control the on-time and off-time of the switches that are used in the power converter stage. The control system is responsible for performing this task, their main function is to regulate the output voltage to the desired level. The control of output voltage is achieved by using a feedback mechanism. The control system takes feedback signal (from output voltage and/or inductor current) as its input and controls the switches of the power converter stage. By doing so, it can regulate the output voltage of the system. This mechanism is explained in Fig. 3.1. The control system physically controls the switches of the dc-dc converter based on the information it gets from output voltage and/or inductor current. The control systems for switching regulator are classified into two categories based on the mechanism they follow to control the switches. Both the strategies are explained in this chapter, along with a comparison which allows us to choose the control system depending on our application of using the regulator to generate regulated supply for current heavy digital processor blocks in memory controller.

3.1 Pulse Frequency Modulation

The pulse frequency modulation (PFM) control scheme regulates output voltage across different load conditions by varying the switching frequency of the regulator. Conceptually, it modulates the switching frequency based on the load current. This can be achieved by keeping a constant on-time t_{on} and varying off-time t_{off}. The concept of PFM with constant on-time t_{on} is shown in Fig. 3.2. This type of control system lowers the frequency for low load current and increases the frequency for high load currents by changing its off-time t_{off} as shown in Fig. 3.2. In both the operation, same on-time is

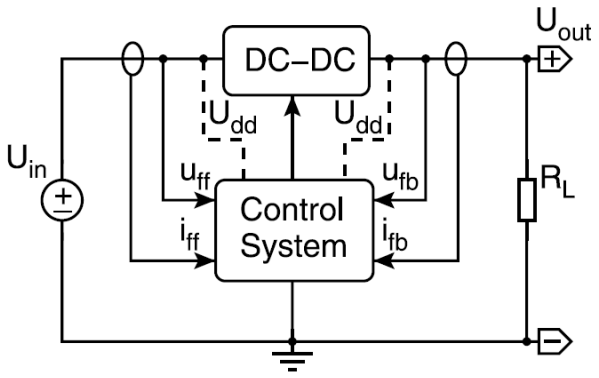

FIGURE 3.1: Conceptual diagram of control system for dc-dc converter [1].

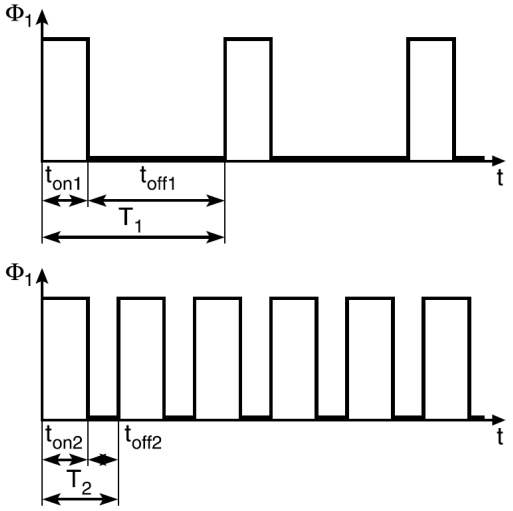

FIGURE 3.2: Pulse Frequency Modulation scheme with constant on-time for low load current (upper graph) and high load current (upper graph) [1].

used. Now consider the voltage conversion formula from equation 2.1, in this to maintain a constant ratio of V_{OUT}/V_{IN} with constant on-time t_{on}, t_{off} requires to be varied for varying load currents. This type of control system is generally used for low and medium load currents [9]. It is so because, at low load currents, switching losses are dominant and PFM has the ability to reduce switching frequency such that switching losses are reduced. The power conversion efficiency tend to decrease for these systems as the load current is increased. It is so because high load currents cause more conduction losses and at high load currents, in order to maintain the desired output voltage, PFM control system increases the switching frequency and in-turn switching losses in the system. In our work, high load current requirement of the digital processor block of memory control requires efficiency to be good for at high load currents upto 400mA. Hence, this type of control system wouldn't be used in this work.

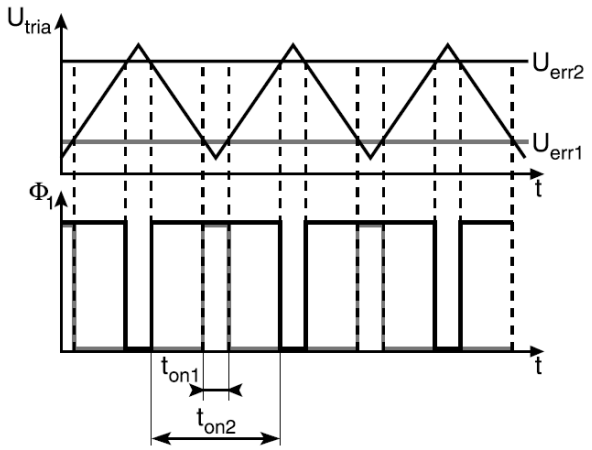

FIGURE 3.3: Pulse Width Modulation scheme for different output voltages [1].

3.2 Pulse Width Modulation

The regulation of output voltage to its desired value by keeping duty cycle D constant, as shown in Fig. 3.3 for ϕ_1. This regulation scheme is different to that of PFM in many ways. The switching frequency is always constant and duty cycle of the clock ϕ_1 (which controls the switches in power stage) is controlled based on the output voltage. This is done by comparing a triangular wave or a saw-tooth wave (triangular wave shown in Fig. 3.3 can be replaced by a saw-tooth wave) with an error voltage. This error voltage is generated by comparing a feedback signal derived from output voltage with a reference voltage. It can be seen from Fig. 3.3 that for different values of error voltages, different on-time is generated but switching frequency of ϕ_1 is constant. Hence, according to equation 2.1 any output voltage can be derived from the unregulated input voltage by using this mechanism.

This type of control strategy is generally used for high load currents as the switching frequency is constant and thus at high load currents switching losses become nominal and conduction losses dominate. The switches can be sized in such a way that conduction losses are minimized to a certain extent. In this work, power conversion efficiency of upto 92.25% is achieved for high load currents. However, fixed frequency PWM controller suffer from poor power efficiency at low load currents [5] [6] [10]. Power conversion efficiency for low load currents is equally important to improve run time of battery operated devices. In order to overcome this drawback in PWM controlled inductive switching regulators, a novel dynamic frequency scaling technique is adapted. This technique senses the load current using the current sensing technique required for current-mode PWM controller and dynamically changes the switching frequency of the clock. Hence, reducing the switching losses at low load currents. This is done without degrading the power efficiency at high load currents. Current mode PWM

control is adopted in this work as it allows faster transient response compared to its voltage counterpart [6] [7].

3.3 Summary

This chapter discussed the different control strategies for inductive switching regulators. The control mechanisms of PFM and PWM were discussed. It is observed that PFM controls the output voltage by varying switching frequency of the system for different load conditions. However, PWM maintains a constant switching frequency and ensures that duty cycle of the clock generated by it to control the switches of the power stage is kept constant for a constant regulated output voltage. The power conversion efficiency of both the control strategies was also discussed and it was decided that PWM control is more suitable for applications such as digital processor block which consume large amount of load currents from the regulated power supply. Hence, PWM control system is chosen for this work. Later, it was discussed that fixed frequency PWM control suffers from poor efficiency performance for low load currents which is an important parameter for improving run time of battery operated devices. Hence, a novel dynamic frequency scaling technique is developed in this work which would improve the power efficiency of the dc-dc buck converter at low load currents without degrading its efficiency at high load currents. The design and implementation of various blocks including the novel frequency decision circuit will be discussed in next chapter.

Chapter 4

System Design

4.1 Motivation

The focus of this thesis is to develop a high efficiency current-mode PWM dc-dc converter with dynamic frequency scaling. Voltage regulators are important part of power management solutions for battery operated hand held devices such as mobile phones, cameras etc. The power conversion efficiency of the voltage regulator is important in improving the run time for these devices. Thus, this work has chosen switching regulator over their linear counterparts. The control mechanism in switching regulator doesn't rely on wasting power in a resistor divider network to regulate the output voltage. Whereas, it uses energy-storing passive elements and switches to change their arrangement to provide a regulated supply voltage.

This work focuses on developing a dc-dc buck converter for digital processor block of a memory controller. These blocks consume a lot of current from the supply. Thus, pulse width modulation control mechanism is chosen over pulse frequency modulation as they provide high efficiency for high load currents. Whereas, fixed frequency PWM controller has lower efficiency in light load [10].

In order to improve efficiency of PWM control dc-dc converter over wide range of load currents, this work proposes a novel dynamic frequency scaling technique to improve the efficiency of current-mode PWM control dc-dc converter. The current sensing circuit required for current controlled architecture is used to develop a novel frequency decision circuit which improves the efficiency of the system over wide range of load currents. The dc-dc buck converter in this work is designed on TSMC 16nm CMOS technology to covert 2.3-3.6V input voltage to 0.8V output voltage which can support upto 400mA current. The off-chip components are: inductor (L = 4.7μH), capacitor (C = 10μF)

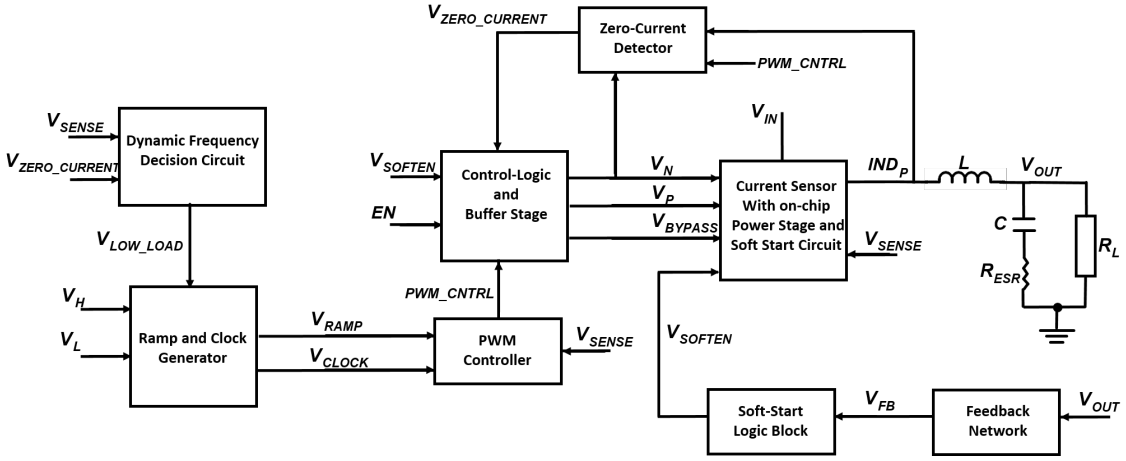

FIGURE 4.1: Functional block diagram of proposed dc-dc converter.

with equivalent series resistance of $R_{ESR} = 200m\Omega$. The high values of LC filter reduce the ripples at the output voltage node. Whereas, a high value of R_{ESR} can increase the UGF of the system and cause ripple amplification. The ripple amplitude at the output voltage is limited to 4mV peak-to-peak voltage.

4.2 System Architecture

The dc-dc buck converter in this work is designed on TSMC 16nm CMOS technology to covert 2.3-3.6V input voltage to 0.8V output voltage which can support upto 400mA current. The proposed design provides high efficiency for a wide range of load currents through dynamic frequency scaling. The functional block diagram of the proposed converter can be seen in Fig. 4.1. The controller moves into soft-start mode when EN signal is high till V_{OUT} is less than 0.8V. The controller by-default enters high frequency mode and switches to low-frequency mode only when V_{LOW_LOAD} becomes high. Signal V_{LOW_LOAD} is generated by the dynamic frequency decision circuit. V_{LOW_LOAD} becomes high when $V_{ZERO\_CURRENT}$ signal toggles 8 times (8μs), depicting stand-by mode (light-load) for the converter. The change in frequency is done by changing the current in ramp and clock generator block. PWM controller block uses a ramp signal to control the duty cycle (D) of the system which in-turn decides the regulated output voltage (V_{OUT} / $V_{IN} = D$). Current-mode control allows a faster transient response during load regulation [6] [7]. Current-mode control requires current sensing block for its operation. The load condition detected by the current sensing block is used to determine the frequency of operation for PWM controller.

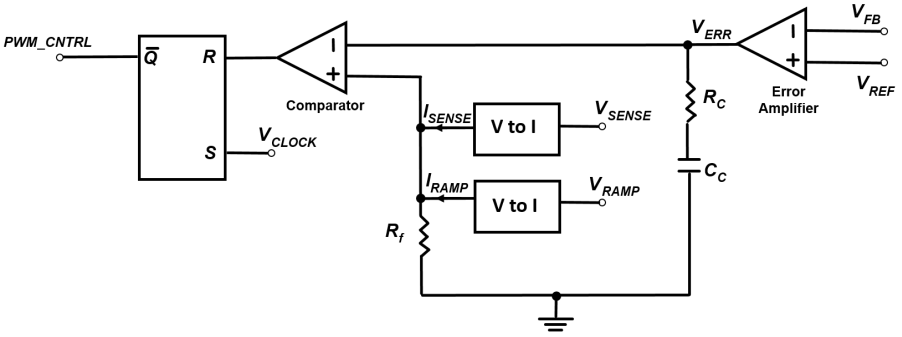

FIGURE 4.2: PWM controller with ramp compensation.

4.2.1 Controller Design and Stability

Simplified schematic of current-mode PWM Controller is shown in Fig. 4.2 [6]. The V to I block converts sense voltage (which contains inductor current information) and ramp voltage to current. Both the currents (I_{SENSE} and I_{RAMP}) are added and applied to scaling resistor R_f as shown in Fig. 4.2. When this signal becomes larger than error voltage signal (V_{ERR}), the PWM controller instructs the buffer stage to toggle the power switches and enter into discharge phase. After each clock cycle, V_{CLOCK} instructs the controller to send a signal to the buffer stage to enter into charging phase. This action allows PWM controller to regulate the output voltage at the cost of a small output ripple voltage. Feedback signal from V_{OUT} is fed to the negative terminal of error amplifier whose gain should be high to ensure high DC accuracy. The error amplifier's design parameter such as trans-conductance (G_m) and capacitor C_C are important in deciding the unity-gain frequency (UGF) of the system. It should be made sure that UGF is always less than the switching frequency of the regulator to avoid ripple amplification of the output voltage, by the control loop.

The small signal and steady state analysis of current-mode PWM controller has been well established and studied in literature [11] [12]. The transfer function derived in [11] is used to perform stability analysis of the loop. The system (see Fig. 4.1) consists of two inherent poles, ω_{P1}: due to output capacitor 'C' and load resistance 'R_L', ω_{P2}: due to comparator's voltage to duty cycle conversion. ω_{P2} can be canceled by the zero formed due to equivalent series resistance (R_{ESR}) of load capacitor 'C' (ω_{Z1}). The error amplifier is used to create the dominant pole of the system ($\omega_{P,ERR}$). It can be seen in Fig. 4.2 that R_C and C_C are added to create a dominant pole and a zero ($\omega_{Z,ERR}$), which is used to cancel ω_{P1}. The transfer function of the system is shown in equation 4.1 [11].

The current mode PWM controller suffers from sub-harmonic oscillations when duty cycle (D) is greater than 0.5. It is so because any perturbation in inductor current is

amplified by a factor of D/D' (D' = 1 - D) leading to instability and can cause pulse skipping as well [6]. To eliminate this problem, current ramp compensation is used. To ensure stability, slope of ramp (m_c) should be greater than half of inductor current slope (m_2) during discharge cycle of the switching regulator [11].

$$
\begin{aligned}
T(s) &= \frac{A(0)(1+\frac{s}{\omega_{Z,ERR}})(1+\frac{s}{\omega_{Z1}})}{(1+\frac{s}{\omega_{P,ERR}})(1+\frac{s}{\omega_{P1}})(1+\frac{s}{\omega_{P2}})} \\
&where, \\
\omega_{Z,ERR} &= \frac{1}{R_C * C_C} \\
\omega_{Z1} &= \frac{1}{R_{ESR} * C_L} \\
\omega_{P,ERR} &= \frac{1}{r_{o,err} * C_C} \\
\omega_{P1} &\approx \frac{1}{R_L * C_L}
\end{aligned}
\tag{4.1}
$$

4.3 Circuit Implementation

A novel dynamic frequency scaling circuit is designed to improve efficiency for lower load currents. The 'high-load' frequency of operation is 1MHz, the circuit switches to a lower frequency of operation of 500kHz during low load condition. the area and power overhead of the proposed circuit is minimal as it requires a simple digital circuit for its implementation. The digital circuit required for dynamic frequency scaling only operates when load switches from high to low load conditions or vice versa. In addition, a simple and efficient soft-start circuit is also implemented to suppress the inrush-current such that over-current damages are avoided and efficiency is not hampered even during the power-on phase of the converter. In this section, circuit implementation and design considerations of each block shown in Fig. 4.1 is discussed.

4.3.1 Current Sensor and Soft-Start Circuit

The current sensing circuit shown in Fig. 4.3 uses the virtual short property of Operational Trans-conductance Amplifier (OTA) [13]. A constant current source (I_{CONST}) and switch M_9 is added to the conventional design for soft-start operation. If V_{DS} of switch M_8 is small and V_{BYPASS} is low, then the equal node voltages allow inductor current flowing through M_O to be copied to M_{OR}. The ratio by which current is copied is decided by the W/L ratios of M_O and M_{OR}. In our design, it is given by 1000:1. The

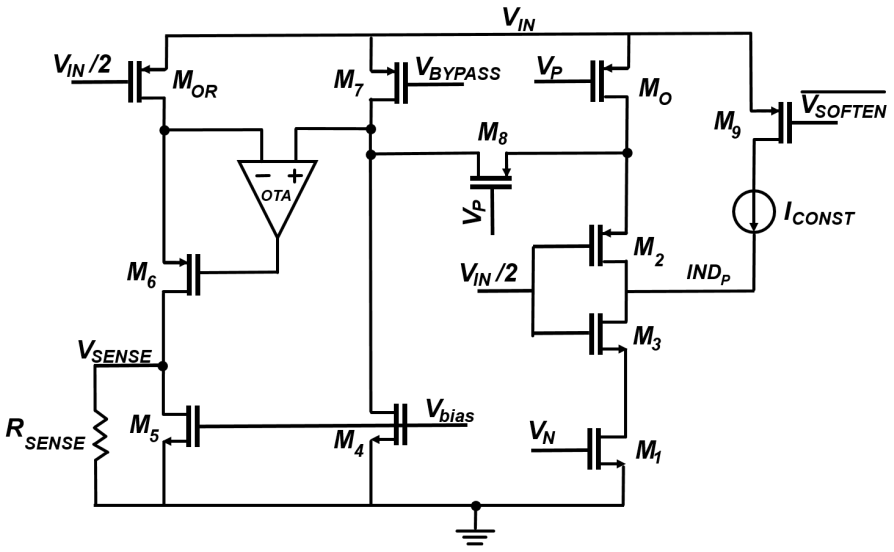

FIGURE 4.3: Schematic of current sensing and soft-start Circuit.

current sensed by M_{OR} flows through resistor R_{SENSE} to generate voltage V_{SENSE}. The signal V_{BYPASS} makes sure that the current-sensing circuit only operates in charging phase of the switching regulator. Transistor M_2 and M_3 are present to ensure the reliability of the power switches M_O and M_1. The unity-gain frequency of loop providing virtual-short condition between drain voltages of M_O and M_{OR} should be high enough to ensure fast settling time. In our design, minimum UGF across PVT and load variations is 6MHz.

The constant current source (I_{CONST}) shown in Fig. 4.3 ensures that only 100mA current flows through the inductor during soft-start operation. This mechanism protects the circuit from a high in-rush current, which can cause damage to the power stage [14]. When V_{OUT} slowly charges close to the desired output voltage, soft-start logic block shown in Fig. 4.4 will disable I_{CONST} and allow PWM controller to regulate the output voltage. The comparator used in the soft-start logic block should have some hysteresis to avoid incorrect operation of soft-start circuit due to inherent ripples at the output voltage node. Our design implements a comparator with hysteresis of 20mV. The analog MUX present in Fig. 4.4 ensures that the soft-start circuit is not incorrectly triggered during load transients. Thus, V_{REF1} is less than V_{REF2} for the circuit shown in Fig. 4.4.

4.3.2 Oscillator and Ramp Generator

The circuit shown in Fig. 4.5 [6] is used to generate clock and ramp signals for current-mode PWM controller. A switch, M_O is added in the conventional circuit of [6] to allow dynamic frequency scaling. The PWM controller uses these two signals to regulate the

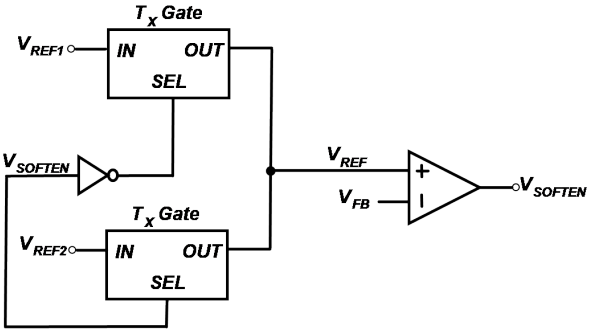

FIGURE 4.4: Soft-start logic block.

output voltage. The reference voltage V_{REF} and a combination of resistors R_1 and R_2 control the current flowing into capacitor C_1. The amount of current flowing decides the frequency of operation and slope of the compensation ramp signal. When V_{RAMP} rises above V_H, S-R latch is triggered and V_{CLOCK} becomes high. When V_{CLOCK} is high, V_{RAMP} falls sharply as switch M_1 (in Fig. 4.5) is turned on till V_{RAMP} becomes lower than V_L. This causes S-R latch to trigger again and V_{CLOCK} becomes low. Hence, a saw-tooth wave is generated at V_{RAMP} having frequency same as V_{CLOCK}. The signal V_{LOW_LOAD} is used to make the frequency of operation half when low-load condition is detected. When V_{LOW_LOAD} is low, switch M_O (in Fig. 4.5) is off and V_{REF}/R (R_1 = R_2 = R) current flows through the circuit. When V_{LOW_LOAD} is high, V_{REF}/2*R flows which reduces the frequency of operation by a factor of two and in-turn reduces the switching losses for the converter.

For stable operation of the controller, condition shown in equation 4.2 for slope of compensation ramp (m_c) and inductor current slope (m_2) should be met. In the circuit shown in Fig. 4.5, the slope of ramp signal is given by f_{osc}*(V_H - V_L). This slope should be equal to m_c/k. Here, k is current to voltage ratio of current sensing circuit. In our design, it is given by 1000/1500. Using the value of m_c computed from equation 4.2, parameters V_H and V_L can be determined.

$$m_c \geq \frac{1}{2} m_2 = \frac{V_{OUT} - V_{IN}}{L} \tag{4.2}$$

4.3.3 Voltage to Current Converter

In current-mode PWM controller, ramp compensation of inductor current is required for stable operation. Hence, the compensation ramp signal has to be added to inductor current signal. For accurate addition of these two signal, they should be converted into current domain. The V to I block converts ramp signal V_{RAMP} and sensed inductor signal V_{SENSE} to current to allow addition in current domain, which is then passed

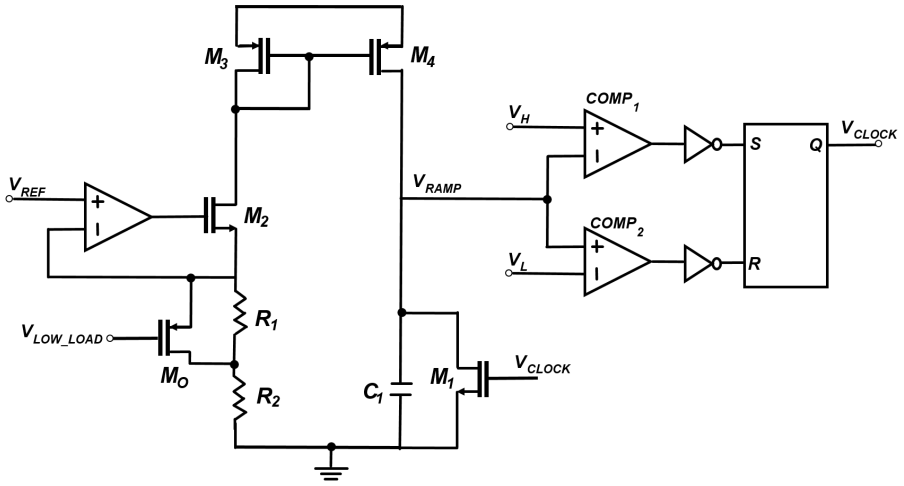

FIGURE 4.5: Schematic of oscillator and ramp generator.

through resistor R_f as shown in Fig. 4.2. The circuit implementation of V to I block is shown in Fig. 4.6. Transistors M_0-M_3 and M_1-M_2 along with resistor R_S in Fig. 4.6 form a cascaded structure of source follower and source degenerated common-source configuration. The first stage source follower acts as a dc-level shifter as V_{SENSE} voltage level coming from current sensing block can be lower than 1V. The analysis shown in equation 4.3 is used to find the current I_1 flowing through transistor M_3. The extra term V_{SG0}/R_S in this equation of I_1 is not required for voltage to current converter output. Hence, this can be removed by subtracting current $I_2 = V_{SG1}/R_S$ from I_1. This action is performed by the mirroring transistors M_4-M_7. The design needs to make sure that M_0 and M_1 have same W/L ratios and current flowing through them.

Here, for input voltage V_{SENSE} from the current sensing block shown in Fig. 4.3 would be given by '$I_L * R_{SENSE}$'. Hence, the presence of R_S in the denominator of equation derived for I_{OUT} is important. It makes sure that the sensed current is independent of absolute value of any resistor. The ratio of resistors can be easily controlled across different corners using analog layout techniques [15].

$$
\begin{aligned}
V_A &= V_{IN} + V_{SG0} \\
G_{m3} = \frac{I_1}{V_A} &= \frac{g_{m2}}{1 + g_{m2}R_S} \approx \frac{1}{R_S} \quad for \;\; g_{m2}R_S >> 1 \\
I_1 &= \frac{V_A}{R_S} = \frac{V_{IN} + V_{SG0}}{R_S}
\end{aligned} \tag{4.3}
$$

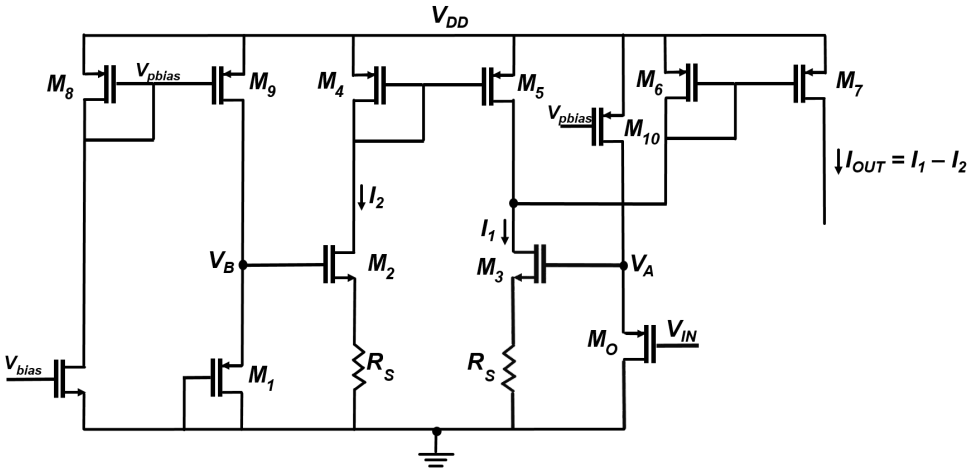

FIGURE 4.6: Schematic of voltage-to-current converter.

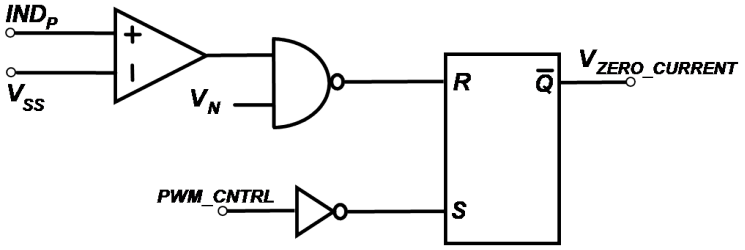

FIGURE 4.7: Schematic of zero current detector.

4.3.4 Zero Current Detector and Buffer Stage

The zero current detector block is essential for DCM operation of the converter. The converter operates in discontinuous conduction mode when load current is less than half of the peak-to-peak inductor current. Fig. 4.7 shows the schematic for zero current detector circuit [9]. When the drain voltage of NMOS switch (M_1 in Fig. 4.3) becomes positive, it depicts that inductor current starts to flow in the opposite direction as that of load current. Comparator shown in the circuit detects the change and sends a signal to the buffer stage to turn off M_1. This helps in improving power efficiency as it reduces the conduction loss during discharge phase [8].

The schematic of buffer stage that drives the power switches M_O and M_1 is shown in Fig. 4.8 [16]. The circuit ensures that both the power stage switches are not on at the same time. Hence, reducing shoot-through current loss. A simple buffer chain would create a short-circuit path for small instances of time, causing unnecessary power consumption. Therefore, the circuit shown in Fig. 4.8 is designed to avoid short-circuit power consumption [16]. The modifications made in the conventional circuit ensure the following conditions: i) Both M_O and M_1 are turned OFF when either converter is disabled ($EN = 0$) or when soft-start circuit is active ($V_{SOFTEN} = 1$). ii) NMOS switch

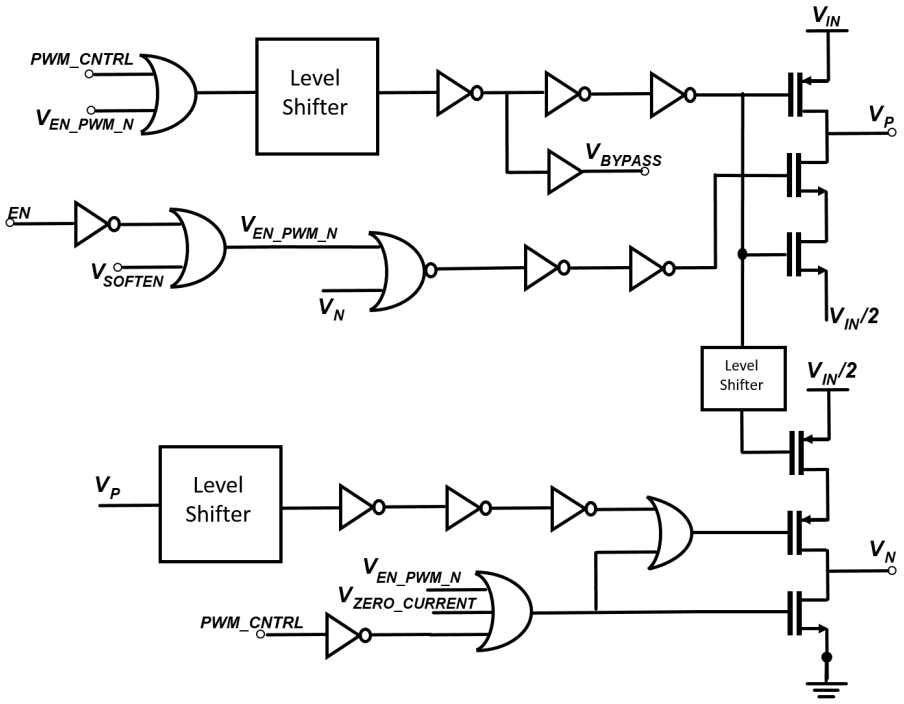

FIGURE 4.8: Schematic of buffer stage.

M_O is turned OFF when inductor current becomes zero ($V_{ZERO\_CURRENT} = 1$). iii) The supply voltages arrangement and Level-Shifter block ensure reliability of transistors as the difference between no two junction voltages exceed 1.8 V.

4.3.5 Frequency Decision Circuit

A Frequency Decision circuit is implemented and shown in Fig. 4.9. This block uses zero-current detector output to decide the frequency at which current-mode PWM controller should operate. The PWM controller offers high efficiency at high load currents but low efficiency at low load currents. The degradation in efficiency is mainly due to the switching losses at low load current. To decrease these losses, this block identifies the state in which the regulator is operating and changes the frequency of operation. The circuit shown in Fig. 4.9 enables a simple and efficient way to improve the efficiency of current-mode PWM controller.

The counter operates when zero-current is detected in our circuit. This condition would happen when load current is less than half of the peak-to-peak inductor current, this value of load current is 70mA ($I_{CRITICAL}$) for our design. When the load current remains below this value for eight clock cycles, the signal V_{LOW_LOAD} goes high. V_{LOW_LOAD} instructs oscillator and ramp generator block to lower the frequency of operation. Hence, reducing the switching losses of the regulator. To ensure low power overhead of this circuit, the counter is set to reset state once the instruction to change the frequency

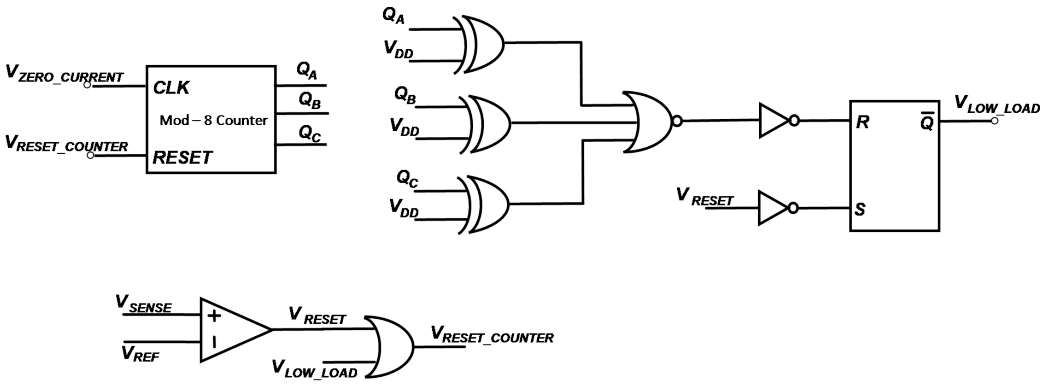

FIGURE 4.9: Schematic of frequency decision circuit.

domain is sent. To ensure proper functioning, the counter remains in reset state for another condition i.e. when load current is higher than $I_{CRITICAL}$. This decision is made by the comparator shown in Fig. 4.9.

Once in low-load (or low-frequency) state, the circuit needs to ensure that it switches to high-frequency state as soon as load regulation causes load current to rise above $I_{CRITICAL}$. To ensure this, V_{RESET} signal triggers to S-R latch to make V_{LOW_LOAD} low. Hence, an instruction is sent to the oscillator and ramp generator to increase the frequency of operation. This mechanism ensures high efficiency at both the load conditions.

4.4 Summary

The detailed analysis and design considerations for all the building blocks required for a high efficiency current-mode PWM control dc-dc buck converter were discussed in this chapter. A novel frequency decision circuit which helps in improving performance for low load currents was also discussed. It will be shown in comparison to the conventional design, the efficiency of the regulator improved by upto 11.35%. This improvement has been achieved with very less area or power overhead. It is so because as explained in the working of the design, the circuit implementation of the novel frequency decision circuit is such that it operates only when load transients are persistent and significant for the regulator. Block level and system level simulation results will be shown in the next chapter. A use case will be displayed where load current switches from low load to high load and visa versa, showing the functioning of the proposed voltage regulator.

Chapter 5

Results and Discussion

This chapter will present the simulation results of the proposed voltage regulator. The schematics are designed in Cadence Virtuoso and TSMC 16nm technology model libraries are used. To verify that the design is robust to a certain extent to PVT variations, the simulations are performed with supply variations (2.3-3.6V), four process combinations and temperature variations (-40°C to 125°C). A current-mode PWM buck converter with novel frequency decision circuit is implemented with TSMC 16nm technology. The converter can be supplied with a voltage of 2.3-3.6V. The output supply voltage is of 0.8V.

5.1 System Level Simulation

The flow chart shown in Fig. 5.1 explains how the regulator switches between different modes to improve efficiency over a wide range of load currents. When EN signal is high, soft-start circuit starts charging the output capacitor towards the desired value. When V_{OUT} becomes close to 0.8V, the soft-start logic block instructs the PWM controller to take over from soft-start circuit. The comparator implemented for this detection has a hysteresis of 20mV such that soft-start circuit is not incorrectly enabled for inherent ripples present in the switching regulator output. The soft-start logic block also takes care that soft-start circuit is not enabled during load current transients. The PWM controller is implemented with current control and zero crossing detection scheme. The frequency decision circuit monitors the zero crossing detection signal to decide the mode of operation. If low load situation is detected, the frequency decision block instructs the ramp and clock generator to reduce the frequency of the system till the load current is increased again.

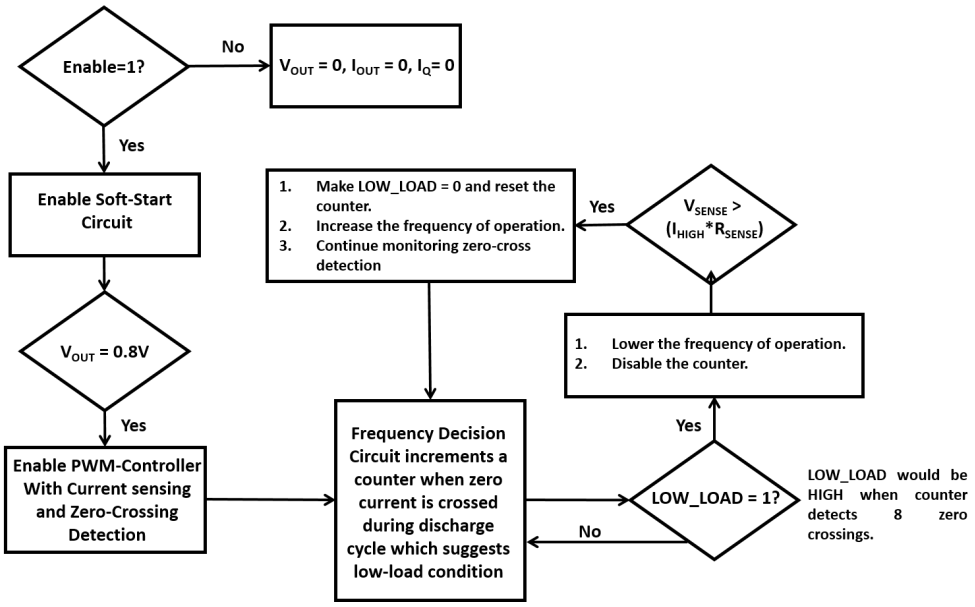

FIGURE 5.1: Flow chart explaining different modes of operation for proposed voltage regulator.

To verify the proper functioning of our design, system level simulation results are shown in Fig. 5.2. It can be seen that V_{OUT} slowly ramps up due to the soft-start circuit implementation. When V_{OUT} reaches close to the desired output level, V_{SOFTEN} becomes low and PWM controller regulates the output voltage. The converter initially starts with high frequency mode and switches to low-frequency mode after eight pulses of zero crossing detector circuit. It can be seen from Fig. 5.2, signal V_{LOW_LOAD} switches high to instruct clock frequency to slow down under low-load condition. When load current changes from 10mA to 300mA, the circuit again enters high-frequency mode.

5.2 Efficiency vs. Load Current

The converter operates properly in both frequency modes. The maximum efficiency of the converter is 95.25% at 190mA load current. The maximum efficiency in low-frequency mode is 92.4% at 50mA load current. The maximum gain in efficiency due to the frequency scaling circuit is of 11.36% at 30mA load current. The efficiency vs. load current plot is shown in Fig. 5.3 for the converter design with and without frequency scaling circuit. Our design achieves an efficiency of greater than 80% across a wide range of load current from 10mA to 400mA. The use of PWM controller provides efficiency at high load currents. The novel dynamic frequency scaling technique implemented in this work allows improvement in efficiency of the voltage regulator at low and medium load currents. For low and medium load currents, switching losses are dominant. Hence, the circuit implemented reduces the frequency of operation for specific load currents that

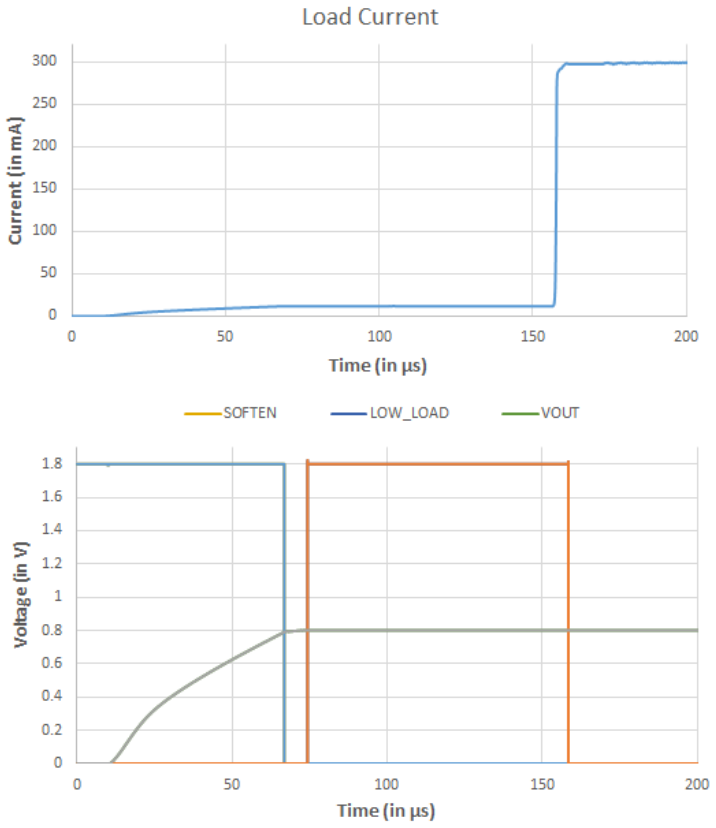

FIGURE 5.2: System level simulation results.

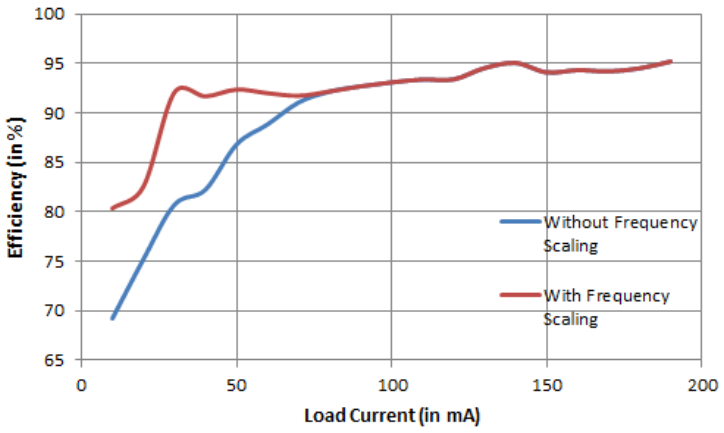

FIGURE 5.3: Efficiency vs. load current plot.

are lower than half of the inductor current ripple. The presence of current mode control and zero-current detection scheme in a PWM control dc-dc converter has made the novel frequency decision circuit to be area and power efficient.

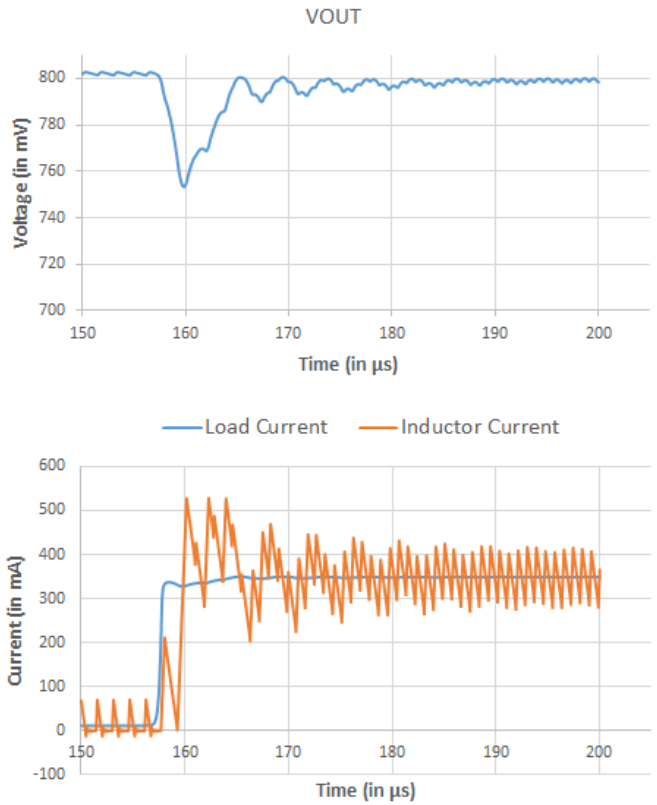

FIGURE 5.4: Efficiency vs. load current plot.

5.3 Output voltage ripple and Load regulation

The simulation results showing load transient response and load regulation of the implemented design is shown in Fig. 5.4. It can be seen that output voltage suffers from a droop of only 50mV for load switching from 10mA to 350mA. The dc load regulation for the implemented current-mode PWM dc-dc converter is 5mV across the PVT variations mentioned in this section before.

5.4 Summary

The simulation results in the chapter are provided to show the proper functioning of a novel current-mode PWM control dc-dc converter. A summary of all the results discussed in this chapter is shown in table 5.1. The design is able to achieve high efficiency at both light and heavy loads. The proposed converter has a small area and power overhead as it doesn't require another control loop to improve efficiency at light loads. The digital circuit required for its implementation only operates during load transitions.

Table 5.1: Summary of Results

Technology	TSMC 16nm
Supply	3.3V (2.3V to 3.6V)
Output Voltage	0.8V
Inductor	4.7μH
Capacitor	10μF
Switching Frequency	0.5MHz and 1MHz (Novel Frequency Scaling)
Peak Efficiency (active-mode)	95.25%
Peak Efficiency (standby-mode)	92.4%
Maximum Load Current	400mA
Output Ripple	4mV
Load Regulation	5mV

Chapter 6

Conclusion

A novel high-efficient current-mode PWM buck converter with dynamic frequency scaling is implemented. The thesis addresses design considerations, circuit implementation and performance analysis of the dc-dc converter. Firstly, the working of a switching regulator is explained to show that the efficiency of an ideal switching regulator can be 100%. The main advantage of using switching regulator over their linear counterparts are highlighted. The discussion on control systems provide insight on various control system implementations available for a switching dc-dc regulator and why PWM controller is chosen over PFM. The regulator is designed for memory controller which has high current requirements. Hence, PWM is chosen as it provides high efficiency for high load currents. The drawbacks of using a PWM controller are highlighted and how the novel dynamic frequency scaling technique overcomes the challenge of improving efficiency at low load currents for PWM controller is shown as a part of this thesis.

Simulation results show that converter regulates properly for input voltage of 3.6V and output voltage of 0.8V. The maximum efficiency of the converter is 95.25% at 190mA load current. The maximum efficiency in low-frequency mode is 92.4% at 50mA load current. The converter has over 80% efficiency for 10mA to 400mA load current. The efficiency of the converter is improved by load-dependent dynamic frequency scaling technique. The implemented technique is area-power efficient. As a result of dynamic frequency scaling, improvement of upto 11.35% in efficiency is shown as compared to the efficiency without dynamic frequency scaling. The converter can operate for input voltage range of 2.3-3.6V. Further, output voltage of 0.8V is assured with device reliability for 16nm technology devices. Power management for battery-operated devices is an important issue and this work helps in improvement of a PWM buck-converter over a wide range of load currents and different power modes.

6.1 Future Work

There exists inherent voltage ripple noise from the output supplied by a switching regulator. Hence, these regulators needs to be cascaded with a low-dropout linear regulator to provide a clean supply to digital blocks present in memory controller die. In future, this switching regulator can be cascaded with a capacitor-less LDO which offers high power supply rejection for wide range of frequencies. The power efficiency would not be degraded by more than 10% because the dropout voltage would be very low for this kind of an architecture.

Publication

[1] The paper titled A High-Efficient Current-Mode PWM DC-DC Buck Converter Using Dynamic Frequency Scaling has been accepted in IEEE conference ISVLSI 2018.

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