Realizing AND functionality using single Tunnel Field-Effect Transistor

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Submitted
in partial fulfillment of the requirements for the degree of
Master of Technology in
Electronics and Communication Engineering

to

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Certificate

This is to certify that the thesis titled **"Realizing AND logic functionality using single Tunnel Field-Effect Transistor"** submitted by **Saptak Banerjee** for the partial fulfillment of the requirements for the degree of *Master of Technology* in *Electronics and Communication Engineering* is a record of the bonafide work carried out by him under my guidance and supervision at Indraprastha Institute of Information Technology, Delhi. This work has not been submitted anywhere else for the reward of any other degree/diploma.

July, 2018

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Abstract

In this thesis, a single Double-Gate Tunnel Field-Effect Transistor (DGTFET) is proposed to realize the AND functionality. Using two-dimensional device simulations, it is shown that a single DGTFET can realize logic functionality by biasing the two gate terminals independently. The key elements in obtaining the required functionality using a DGTFET are:

1. Employing a gate-source overlap
2. choosing an appropriate silicon body thickness.

The two-dimensional device simulations demonstrate that the electrical characteristics of the proposed device correctly implements the AND functionality. Specifically, the drain current under the biasing conditions at two inputs 11, 01, 10 and 00 are in the order of 1×10^{-8}, 1×10^{-15} 1×10^{-15} and 1×10^{-15} respectively. Therefore, an impressive I_{ON}/I_{OFF} ratio of 1×10^{8} is attained.

Further, it is demonstrated that realized device is operational even for low supply voltages. But the I_{ON}/I_{OFF} ratio keeps on deteriorating as the supply voltage is reduced. However, for future applications, it must be ensured that the proposed device must exhibit sufficiently high I_{ON}/I_{OFF} ratio, especially at low supply voltages. In this thesis, the challenges involved in enhancing the I_{ON}/I_{OFF} ratio in a TFET that realizes the AND functionality, are investigated. The study shows that the techniques that boost the I_{ON} in a TFET, for example using a low bandgap material, does not necessarily enhance the I_{ON}/I_{OFF} ratio in the device. This is primarily due to challenges involved in turning-OFF the device when only one of the terminals is biased at logic "1". Further, the efficacy of using Dual Material Gate (DMG) and optimizing silicon body thickness to improve the I_{ON}/I_{OFF} ratio is explored.

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4.1 Device Parameters of the SDGTFET used to realize the AND functionality (Other device parameters are same as those listed in Table 3.1) 19

List of Abbreviation

MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
DGTFET	Double-Gate Tunnel Field-Effect Transistor
NMOS	N-type MOSFET
PMOS	P-type MOSFET
BTBT	Band-to-Band Tunneling
DMG	Dual-Material Gate

Chapter 1

Introduction

1.1 Motivation

The reduction in the size of transistors has revolutionized the semiconductor industry by enabling large scale integration. This has led to decrease in power consumption, increase in switching speed and increase in density of the components in the Integrated Circuits (ICs). Typically the building blocks of these circuits are MOSFETs. However, this scaling down is facing a major roadblock, as reduction in the supply voltage of transistors has to be accompanied by reduction in threshold voltage, this leads to increase in the leakage current. In turn, this results in increase in the power consumption by the circuit.

The main cause of the above problem is the characteristic transport mechanism of MOSFET. The current in a MOSFET is generated by thermionic injection of electrons over the energy barrier caused by the gate voltage. This sets a fundamental limit on the Subthreshold Swing (SS) which is $60mV/dec$ at $300K$. Subthreshold Swing characterizes the steepness of the slope of the transfer characteristics when the transistor switches from ON to OFF state.

In order to circumvent this problem extensive research is being carried out to explore devices with different mechanisms of current transport. One such device is Tunnel Field Effect Transistor (TFET), which uses quantum mechanical tunneling as its transport mechanism . Consequently, TFETs have been demonstrated to exhibit Subthreshold Swing much below $60mV/dec$ at room temperature and can operate at very low supply voltages. Therefore TFETs are being contemplated as suitable replacements of conven-

tional MOSFET for future CMOS technologies.

In general, for CMOS technologies it is desirable that a given functionality is implemented using as small area as possible. One ways to achieve this is by reducing the number of transistors in implementing basic logic gates. A possible way is by using different gates of the same multi-gate transistor as independent inputs. For example, the two gates of a Double-Gate MOSFET can be used as two terminals of an AND gate. Since TFETs operate via a different current transport mechanism, it provides opportunities to explore distinct architectures that can be more energy-efficient and compact compared to conventional MOSFET.

The above observations has motivated to explore the possibility of realizing AND logic functionality by using Double Gate TFET (DGTFET). In this thesis, the focus has been particularly on the AND functionality, because it is challenging to suppress current flow in the device when only one of the terminals is connected to logic "HIGH".

1.2 Scope of the work

All the results presented in the thesis have been obtained by using two-dimensional (2D) TCAD simulations. In this thesis, all simulations have been carried out using Atlas version 5.22.1.R [3]. Non-local band-to-band tunneling (BTBT) model has been used that takes into account the spatial profile of the energy bands to compute the tunneling current. The non-local BTBT model of Atlas has been widely used in investigating TFETs and has shown good match with theoretical and experimental results [4–6]. Band gap narrowing effects, Fermi-Dirac statistics and Shockley-Read-Hall recombination models were incorporated. The simulation model is calibrated using [7] and the same simulation setup has been used in [8,9]. Despite differences in device parameters of this work and [7], it is assumed that the calibrated model has reasonably good predictability due to similarity in structures and operating principle. A sample ATLAS input file is given in Appendix 1.

1.3 Thesis Organization

The thesis is organized as follows:

- **Chapter 2: A Review of TFET**
  This chapter provides review of TFETs. The device structure and operating mechanism is described in detail.

- **Chapter 3: Realizing AND functionality**
  This chapter describes how AND functionality is realized using a single TFET. The device structure and the modifications are discussed.

- **Chapter 4: Realizing AND functionality for low operating voltages**
  This chapter discusses the characteristics of the proposed device at low operating voltages.

- **Chapter 5: Conclusion**
  This chapter concludes the thesis and presents scope of future work.

Chapter 2

A Review of TFET

This chapter reviews basics of TFET, it gives a brief overview of device and discusses its differences with the MOSFET architecture.

2.1 Device Structure

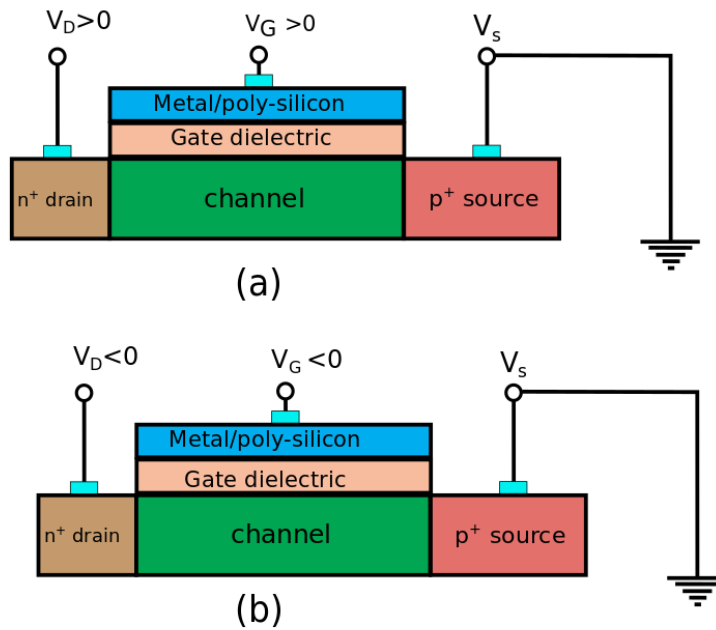

Figure 2.1: An implementation of TFET and its biasing schemes (a) n-type TFET (b) p-type TFET [1]

TFET has a p-i-n structure, where the intrinsic region is gated like a MOSFET. Fig 2.1(a) and Fig 2.1(b) show the structure of an n-type and a p-type TFET, respectively. A stark contrast with the MOSFET architecture is noted. In a MOSFET the drain and source are doped with a similar doping type(n^+ or p^+). However, in TFET the drain and source are doped with opposite doping types.

In an n-type TFET, the drain is highly doped n-type semiconductor. On the other hand, the source is highly doped p-type semiconductor. For a p-type TFET, exactly opposite configuration is employed. The channel region in a TFET is intrinsic or lowly-doped p-type or n-type semiconductor. The channel is separated from the gate electrode by a dielectric, similar to a conventional MOSFET.

In Fig 2.1, the biasing schemes for an n- and a p-type TFET are highlighted. It can be seen that for an n-type TFET, the source is grounded and a positive voltage is applied to the drain and the gate electrodes. On the other hand, for a p-type TFET, the source is grounded and a negative voltage is applied to the drain and the gate electrodes. Conventionally, a TFET is termed as an n-type TFET or a p-type TFET depending on the majority carrier present in the channel when the TFET is turned ON. The dominant carriers in the an n-type TFET are electrons while in p-type TFET the dominant carriers are holes.The terminals are called source or drain depending on whether the dominant carriers enter or leave the channel through that terminal.

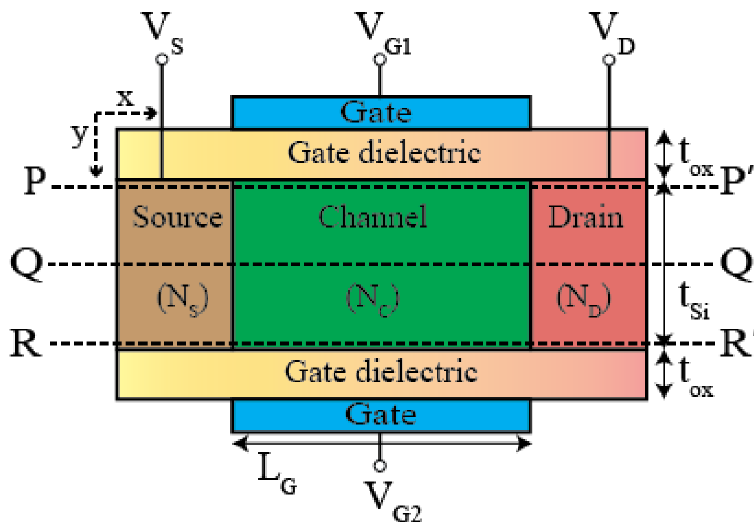

Figure 2.2: Cross-sectional view of an n-type DGTFET

The implementation of TFET shown in Fig 2.1, is a simple and naive way to represent

its structure. The implementation which would be used throughout this thesis is a n-type Double-Gate Tunnel Field Effect Transistor (DGTFET), shown in Fig 2.2. It has two gates, the top gate is biased to voltage V_{G1} and bottom gate biased to voltage V_{G2}. The drain and source region are biased to voltages V_D and V_S respectively. The doping concentration of source, channel and drain region are N_S, N_C and N_D respectively. t_{ox} is the oxide dielectric thickness and t_{Si} is the thickness of the Si body. PP', QQ' and RR' are the cutlines through the top, middle and bottom sections of the Si body.

2.2 Operation of TFET

The operation of a TFET is based on band-to-band tunneling (BTBT) mechanism. This mechanism involves tunneling of carriers from the valence band into the conduction or the other way around through the forbidden bandgap.

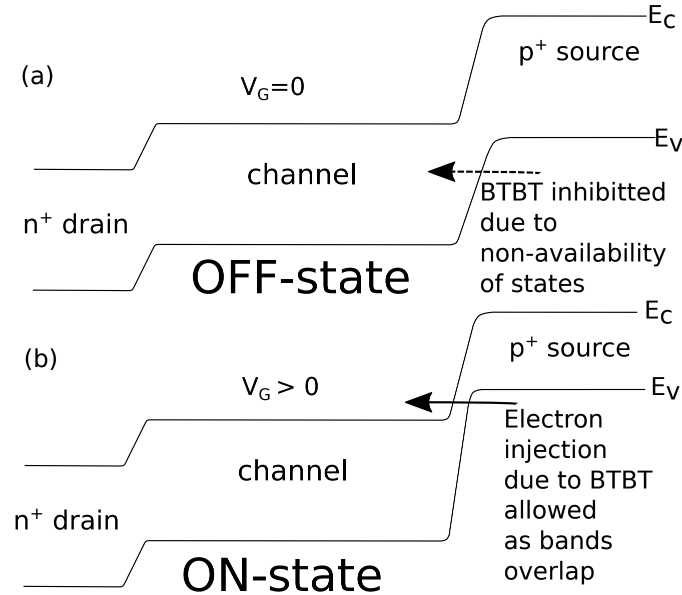

Figure 2.3: The band-diagrams of TFET when it is in (a)ON- and (b)OFF-state [1]

In Fig 2.3 the band diagrams of a typical n-type TFET in its OFF- and ON-states are shown. It can be seen from this Figure 2.3(a) that when the gate voltage V_G is close to zero, the TFET is in the OFF-state. It shows that the conduction band in the channel region lies above the valence band in the source region. As a result, BTBT is inhibited

and this explains the OFF-state with extremely low drain current. As the gate voltage is increased to a positive value ($V_G > 0$), it modulates the carrier density of electrons below the gate and the conduction band in the channel is lowered. When sufficiently high voltage is applied to the gate, band bending increases at the source such that the valence band in the source and the conduction band in the channel gets aligned (as shown in Fig 2.3). As a result, the electrons in the valence band in the source region can undergo tunneling to the conduction band in the channel region. The electrons that tunnel into the channel region are pulled into the drain terminal by the positive bias of the drain. This forms the basis of operation for an n-type TFET.

2.3 Tunneling current in TFET

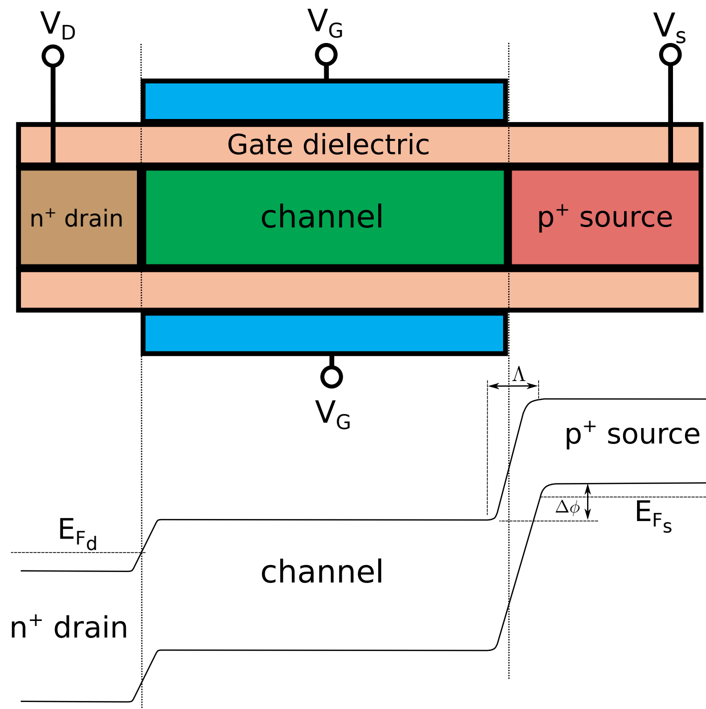

Figure 2.4: Band diagram in a n-type DGTFET. The various device parameters are shown.

Having described the mechanism of tunneling current, the expressions which quantify the magnitude of this current are described next. In Fig 2.4 the band diagram and related parameters of a TFET are shown. When a positive potential ($V_{GS} > 0$) is applied to the gate, the valence band of the channel is pushed below the conduction band of the

source and band-to-band tunneling is enabled. The overlap of the valence band in the channel with the conduction band in the source is shown as $\Delta\Phi$. The transition region at the source–channel interface is shown as Λ. The Λ describes the width of the tunneling barrier and depends on the geometry and other parameters of the device, which will shall be discussed later in this section.

An analytical expression for the drain current in a TFET can be obtained by using the Landauer equation and assuming a triangular barrier. Under this condition the drain current (I_D) using WKB approximation is given by:

$$I_D \propto exp\left[\frac{-4\sqrt{2m^*}E_g^{*3/2}}{3 \mid e \mid \hbar(\Delta\Phi + E_g^*)}\Lambda\right]\Delta\Phi \tag{2.1}$$

where m^* is the effective mass of electron, E_g^* is the effective band gap, e is charge of electron, $\hbar$ is the reduced Planck constant and

$$\Lambda = \sqrt{\frac{\epsilon_{Si}t_{ox}t_{Si}}{\epsilon_{ox}}} \tag{2.2}$$

where ϵ_{Si} and ϵ_{ox} are the permittivity of Si and the oxide dielectric, respectively. t_{ox} and t_{Si} are the thickness of the oxide and Si channel region, respectively.

2.4 Promises and Challenges of TFET

Tunnel FET (TFET) uses quantum mechanical tunneling as the mechanism for the current transport. Hence over the past few decades TFETs have been studied with very deep interest. They exhibit excellent subthreshold swing and can operate at very low voltages, hence they promise to be futuristic energy-efficient switches [1, 10–12]. They also have certain limitations such as low ON current and ambipolar behaviour. TFETs have been used to realize logic gates which demonstrate very interesting characteristics [13–15]. For efficient utilization of area the logic gates should have a compact realization, one of the ways to achieve this is to reduce the transistor count in the realizations. To this end, multiple gate transistors with different gates treated as independent inputs has been proposed to be a viable solution for conventional devices [16–18]. However, it would

require an ingenious design of TFET to realize the appropriate logic functionalities. In this thesis, the focus is on one such architecture namely, the DGTFET in realizing the AND logic functionality. For completeness, it is noted here that DGTFET has been extensively investigated in [7, 19, 20].

Chapter 3

Realizing the AND functionality

In this chapter, it is demonstrated that a single DGTFET can be used to realize the AND functionality. The important architectural modifications are explained and the device is optimized to obtain a good AND behavior using a DGTFET.

3.1 Device Structure

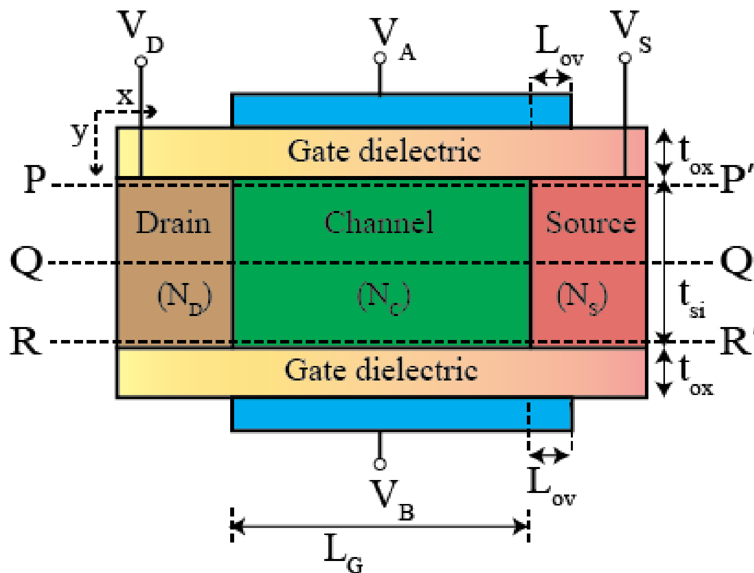

Figure 3.1: Cross-sectional view of the proposed DGTFET used to realize the AND functionality [2]

Table 3.1: Common Device Parameters used in the simulation

Parameter	**Value**
Supply voltage (V_{DD})	1.2 V
Drain doping (N_D)	$1{\times}10^{18}$ $atoms/cm^3$
Source doping (N_S)	$1{\times}10^{20}$ $atoms/cm^3$
Channel doping (N_C)	$1{\times}10^{17}$ $atoms/cm^3$
Gate length (L_G)	100 nm
Gate length (L_{ov})	20 nm
Silicon film thickness (t_{si})	10 nm
Gate oxide thickness (t_{ox})	3 nm
Gate oxide permittivity (ϵ_{ox})	$16\epsilon_0$

The cross-sectional view of the proposed DGTFET that realizes the AND functionality is shown in Fig 3.1. The two gates of the DGTFET are independently-biased: the top-gate at V_A and the bottom gate at V_B. Another distinct architectural modification is the addition of gate-source overlap with length L_{ov}. The purpose of gate-source overlap is explained later in this chapter. The device parameters of DGTFET used in simulation are shown in Table 3.1. The drain doping concentration $N_D = 1 \times 10^{18}$ $atoms/cm^3$ is kept at lower value with respect to the source doping concentration $N_S = 1 \times 10^{20}$ $atoms/cm^3$. This is to ensure a low value of ambipolar current. The channel is lowly doped with a doping concentration of $N_C = 1 \times 10^{17}$ $atoms/cm^3$. The gate work function has been chosen to be $\phi_G = 5.0$ eV. Since an n-type DGTFET is used the V_{DS}=V_{DD} is taken. In this work, the voltage V_{DD} is treated as logic "1" and ground (Gnd or 0 V) as logic "0". The current flowing through the device when the top and bottom gates of the DGTFET are at logic A and B respectively, are denoted as I_{AB}. For example, the current I_{01} denotes the current when $V_A = 0$ and $V_B = V_{DD}$.

When a single DGTFET is used to realize a logic function, the magnitude of drain current flowing through the device depends on the input to the gate terminals (V_A and V_B) and the intended functionality. For example, when a DGTFET works as an AND logic, then a high current flows through DGTFET when $V_A = V_B = V_{DD}$ and a low current flows when any of the gate terminals is grounded. The I_{ON} is the minimum current for which

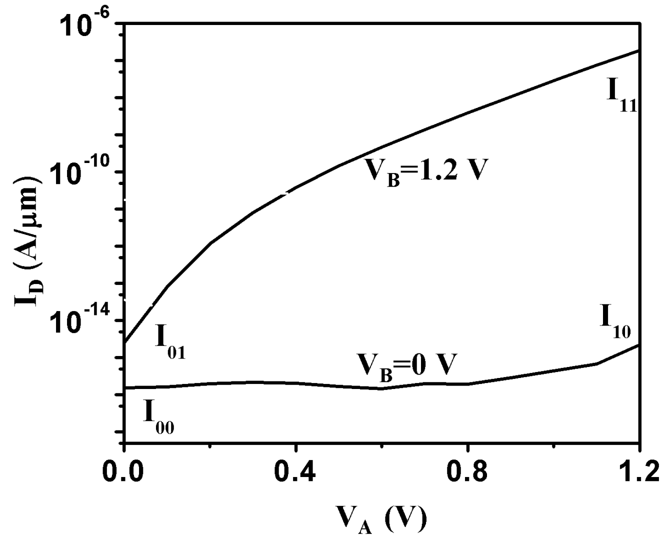

Figure 3.2: Transfer characteristics of the realized AND functionality

the logic output is at expected to be at logic "1". The I_{OFF} is the maximum current for which the logic output is expected to be at logic "0". For DGTFET employed in realizing logic functions it is desirable to maximize I_{ON}/I_{OFF} ratio. The transfer characteristics of the realized AND functionality using the modified DGTFET architecture is shown in Fig 3.2. The value of I_{ON}/I_{OFF} for the realized functionality is 1×10^8.

3.2 Why DGTFET architecture needs to be modified to attain AND functionality?

Before proceeding with detailed discussion on the modified DGTFET architecture that is used to realize the AND functionality, it must be noted as to why these modifications were made. In a conventional DGTFET, significant BTBT occurs in the region close to the gate connected to V_{DD}, irrespective of bias applied at the other gate. However, to realize the AND functionality, it is required that BTBT should occur only when $V_A = V_B = V_{DD}$. Therefore, BTBT must be suppressed when only one of the gates is at V_{DD}. This is achieved by using gate-source overlap and choosing an appropriate silicon body thickness, as explained below. The next section explains the consequent change in characteristics of the device due to the above modifications and how they were optimized to attain a high

value of I_{ON}/I_{OFF} ratio.

3.3 Device Parameters of modified DGTFET

Important device architectural modifications and parameters to realize AND functionality are as follows:

1. Incorporating gate source overlap L_{ov}
2. Optimizing the silicon body thickness t_{si}
3. Optimizing the gate work function ϕ_G

3.3.1 Gate-Source overlap

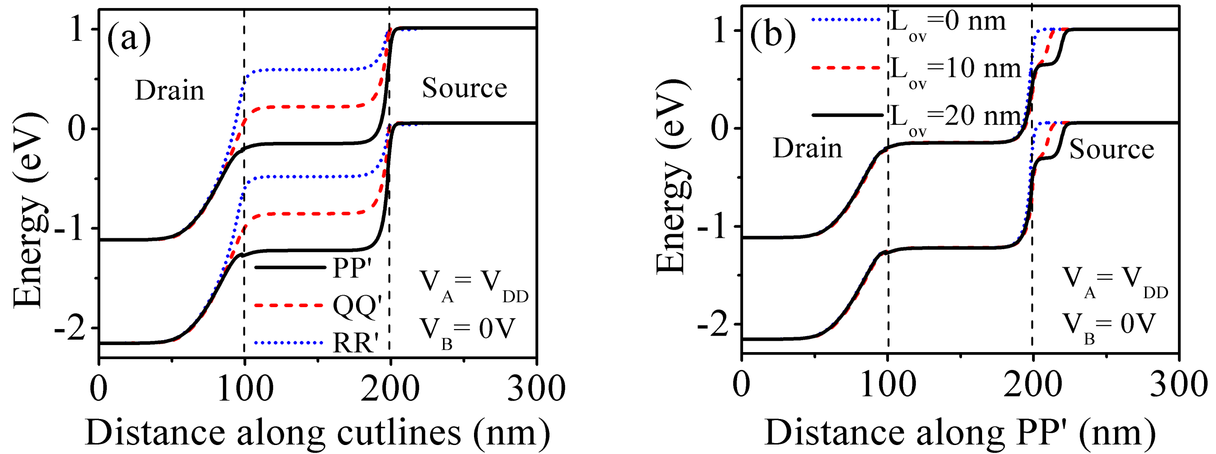

Figure 3.3: Band diagrams for $V_{DS} = V_{DD}$, $V_A = V_{DD}$ and $V_B = 0$ (a) Along cutlines shown in Fig 3.1 for $L_{ov} = 0$ (b) Along PP$'$ for different L_{ov}

For a conventional DGTFET (L_{ov}=0 nm), the band diagram for the case $V_A = V_{DD}$ and $V_B = Gnd$, is shown in Fig 3.3(a) along three different cutlines. It is evident that tunneling width is appreciably smaller in region close to the top gate (PP'), and therefore, BTBT is enabled at the top surface in contrast to the regions close to bottom gate (RR') and the middle of the silicon body (QQ'). However, as shown in Fig3.3 (b), the addition of the gate-source overlap increases tunneling width and suppresses BTBT at the top surface.

The tunneling width increases as the L_{ov} increases till L_{ov}=20 nm. For $L_{ov} > 20\ nm$, there is no further increase in the tunneling width. Hence, $L_{ov} = 20\ nm$ is taken for obtaining AND function.

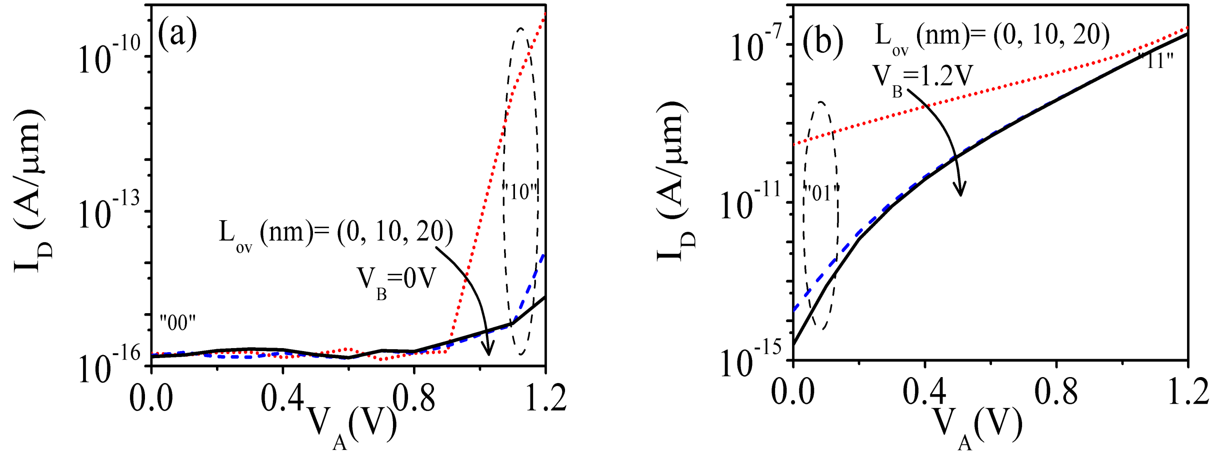

Figure 3.4: Transfer characteristics to illustrate influence of overlap (L_{ov}). L_{ov} is varied from 0 to 20 nm and V_{DS}=V_{DD} (a)$V_B = Gnd$ and V_A is varied from 0 to V_{DD}, Due to increase in the overlap length (L_{ov}) there is decrease in drain current. (b)V_B=V_{DD} and V_A is varied from 0 to V_{DD}. Introduction of overlap does not affect the drain current.

This is demonstrated using the transfer characteristics of the device as shown in Fig 3.4(a). Fig 3.4(a) shows the characteristics with $V_B = Gnd$ and V_A is varied from 0 to V_{DD}. The value of drain current when V_A =V_{DD} keeps on decreasing as L_{ov} is increased. The presence of gate-source overlap does not have effect the ON current of the proposed device. This is demonstrated in Fig 3.4(b). In the above figure the transfer characteristics of the device when V_B=V_{DD} and V_A is varied from 0 to V_{DD} is shown, when $V_A = V_B = 1.2\ V$, the drain current remains almost unchanged across all overlap lengths.

3.3.2 Work function of the gate

For realizing AND functionality, the gate work function (ϕ_G) is chosen such that a high I_{ON}/I_{OFF} ratio is obtained. This is shown in Table 3.2. As ϕ_G is varied from 4.8 eV to 5.2 eV, the highest value of I_{ON}/I_{OFF} is obtained for $\phi_G = 5.0\ eV$. Therefore $\phi_G = 5.0\ eV$ is taken to be the golden value of gate work function.

Table 3.2: Gate Work function (ϕ_G) engineering for optimum performance

ϕ_G (eV)	I_{ON}/I_{OFF}
4.8	1×10^4
4.9	1×10^5
5.0	1×10^8
5.1	1×10^7
5.2	1×10^6

3.3.3 Thickness of Silicon body

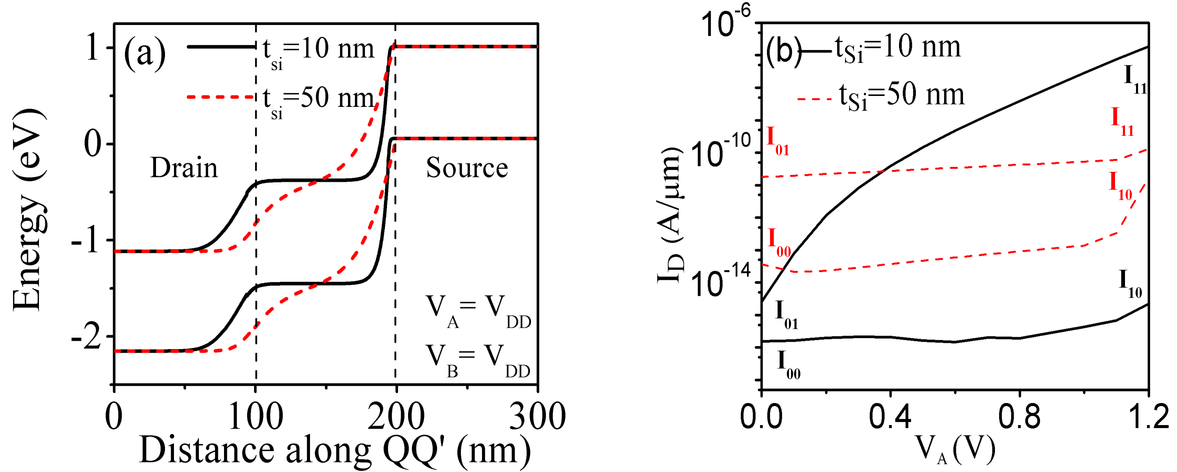

Figure 3.5: (a)Band diagram of the proposed DGTFET for V_A=V_B=V_{DD} along the middle of Si body. It is apparent that tunneling width across the channel-source junction increases with increase in thickness (b)Transfer characteristics of the device for different values of t_{Si}

Fig 3.5 (a) shows the band diagrams of the DGTFET with L_{ov}=20 nm at $V_A = V_B = V_{DD}$, along the middle of the silicon body for $t_{si} = 10\ nm$ and $t_{si} = 50\ nm$. It may be noted that the effect of overlap disappears across the middle of Si body. For $t_{si} = 10\ nm$, tunnel width decreases due to the combined effect of the top and the bottom gates, in contrast to DGTFET with $t_{si} = 50\ nm$. As a result, it is observed that the I_{ON}/I_{OFF} ratio increases from 10^1 to 10^8 as t_{si} is decreased from 50 nm to 10 nm. Hence, for realizing AND function, a small t_{si} is desirable. The transfer characteristics of the proposed device for t_{Si} = 10 nm and 50nm are shown in Fig 3.5(b).

The chapter has described how a single DGTFET can be used to realize an AND functionality. All the device modifications and optimization were discussed. In the next chapter,

the device is explored further to see how it functions at low operating voltages.

Chapter 4

Realizing AND functionality for lower operating voltages

In the previous chapter it was demonstrated that the AND functionality can be realized using a single DGTFET. This chapter explores how the device performs under low operating voltages. Further, it is demonstrated that the techniques which are employed to boost I_{ON} in a TFET do not necessarily improve the I_{ON}/I_{OFF} ratio of the proposed device.

4.1 Operation of the proposed device under low operating voltages

One of hallmarks of a TFET is that it can be operate at voltages much lower than CMOS technology. Therefore it is important to examine variation in I_{ON}/I_{OFF} ratio of the proposed device at lower supply voltages (V_{DD}). The variation is shown in Fig 4.1. As the supply voltage (V_{DD}) across the proposed device is decreased, the work function of the gate (ϕ_G) must also be decreased, this is also shown in the figure below. The decrease in work function of the gate shifts the threshold voltage (V_{Th}) of the DGTFET to lower values. This ensures an uniform value of the overdrive ($V_{DD} - V_{Th}$) across the device for each of the corresponding operating voltages.

The AND functionality is retained for voltages upto $V_{DD} = 0.4V$, it can be seen that

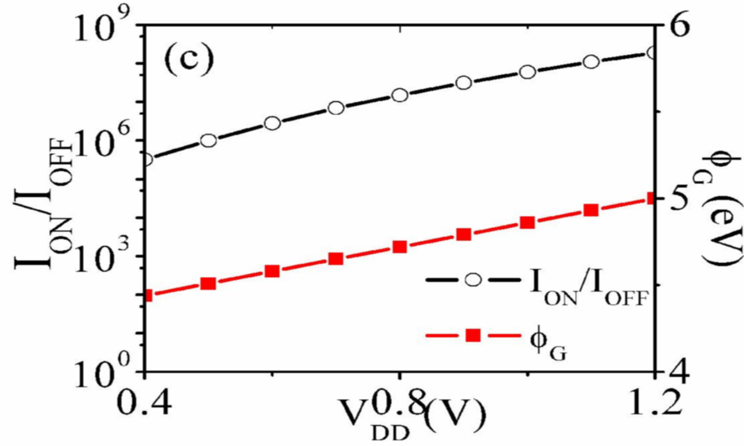

Figure 4.1: Variation of I_{ON}/I_{OFF} ratio with supply voltage V_{DD} [2]

I_{ON}/I_{OFF} has a high value of 10^6 for supply voltage as low as $V_{DD} = 0.5V$. It must be noted that the I_{ON} deteriorates for lower values of V_{DD}. This is a well known problem in a TFET [21]. Hence boosting the value I_{ON} such that the value of I_{OFF} remains low is important for TFETs in realizing logic functionality. In the next section, the challenges in achieving the same are illustrated using strained DGTFET (SDGTFET),

4.2 Strained DGTFET

The structure of SDGTFET is same as a normal DGTFET except that the normal Silicon body is replaced by "strained" Silicon. For the fabrication of the structure the single layer strained Silicon on insulator(SSOI) technology is used [22]. SSOI is a SiGe-free material system that has the advantages of strained silicon while improving the scalability of thin-film SOI. The amount of strain in an SSOI is controlled by varying the mole fraction of Ge (x) in the relaxed SiGe buffer layer that is used during its fabrication.

4.2.1 Modelling of strain

When strain is introduced, it causes the band gap and effective mass of the carriers in Si to decrease, and electron affinity to increase. This can be modelled by the following equations:

$$(\Delta E_g)_{s-Si} = 0.4x \tag{4.1}$$

$$(\Delta E_C)_{s-Si} = 0.57x \tag{4.2}$$

$$V_T ln \frac{N_{V,Si}}{N_{V,s-Si}} = V_T ln \frac{m^*_{h,Si}}{m^*_{h,s-Si}} \approx 0.075x \tag{4.3}$$

where x is the Ge mole fraction in the relaxed SiGe buffer layer; $(\Delta E_g)_{s-Si}$ is the decrease in the bandgap of silicon due to strain; $(\Delta E_C)_{s-Si}$ is the increase in electron affinity of silicon due to strain; V_T is the thermal voltage; $N_{V,Si}$ and $N_{V,s-Si}$ are the density of states (DOS) in the valence band in the normal and strained silicon, respectively; $m^*_{h,Si}$ and $m^*_{h,s-Si}$ are the hole DOS effective masses in normal and strained-silicon, respectively.

For normal Si the value of $E_g = 1.08\ eV$, $E_C = 4.17\ eV$ and $N_{V,Si} = 1.04 \times 10^{19}\ cm^{-3}$. Using Eq 4.1, 4.2 and 4.3 the above values for strained Si can be calculated for different Ge mole fraction x. An extensive study of the performance of DGTFET with a strained Si body has been carried out in [22]. It has been demonstrated that an introduction of strain leads to decrease in tunneling width, which in turn increases the drain current. In the next section, the performance of SDGTFET when it is used to realize the AND functionality is studied.

4.2.2 AND functionality using strained DGTFET

The device structure of the SDGTFET that realizes the AND functionality is same as in Fig 3.1. The device parameters of the device are listed in Table 4.1.

Table 4.1: Device Parameters of the SDGTFET used to realize the AND functionality (Other device parameters are same as those listed in Table 3.1)

Parameter	**Value**
Supply voltage (V_{DD})	0.5 V
Gate work function (ϕ_G)	4.51 eV

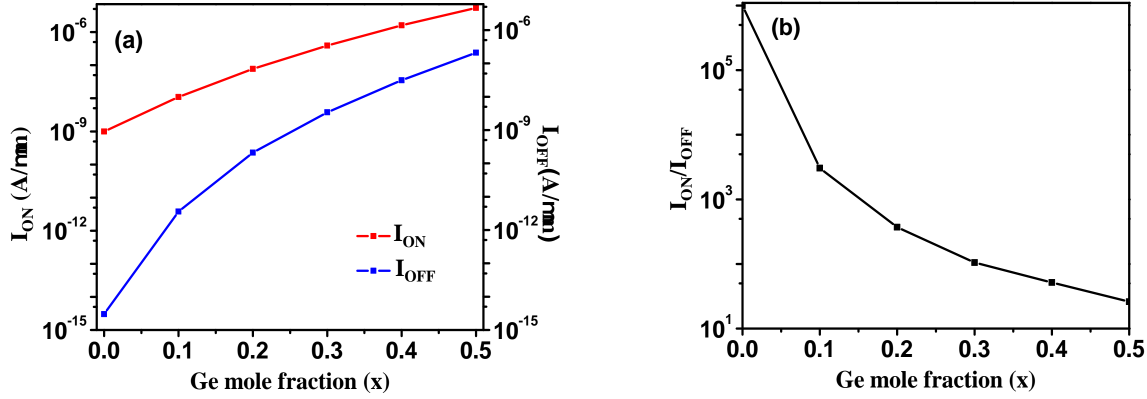

Figure 4.2: The variation of (a)I_{ON}, I_{OFF} (b)I_{ON}/I_{OFF} with change in mole fraction (x)

In Fig 4.2(a) and (b), the I_{ON}, I_{OFF} along with I_{ON}/I_{OFF} ratio is shown for different value Ge mole fraction (x). With increase in mole fraction there is significant rise in I_{ON}. However, to realize an AND functionality one of the most crucial challenges is to ensure that the current flowing through the channel should be very low when only one gate terminal is connected to V_{DD}. It becomes difficult to turn OFF the device when one of the terminals is at V_{DD}.

As strain is introduced in the Si body, it is noticed that the effective region of tunneling changes. For lower mole fraction ($x < 0.2$),the tunneling is mostly confined to regions close to the Si-gate dielectric interface. However, when the mole fraction becomes high ($x > 0.2$), then BTBT gets enabled throughout the Si body. Fig 4.3(b) shows that when x=0.5, there is large band overlap in the middle of the Si body. It may be noted that, when the BTBT occurs in the middle of Si body, then it becomes challenging to stop tunneling using gate-source overlap. As a result a low I_{ON}/I_{OFF} ratio is obtained with x=0.5. Further it can be intuitively inferred that if the Si body is made thin probably gate-source overlap can be effective in supressing the BTBT when V_A=0.5 V and V_B = Gnd or vice-versa. Therefore, the I_{ON}/I_{OFF} value at smaller Si body thickness is examined in Fig 4.4 for a mole fraction (x)=0.1. As the Si body thickness (t_{Si}) is decreased, it can be observed that the I_{ON}/I_{OFF} ratio improves. A peak value of $I_{ON}/I_{OFF} = 1 \times 10^5$ is obtained for t_{Si}=5 nm.

For values of t_{Si}<5nm, there is drastic decrease in I_{ON} current. When both gate terminals are connected to logic "1", the majority of tunneling occurs across the mid-section of the Si body. However with further decrease in Si body thickness, this area of this section

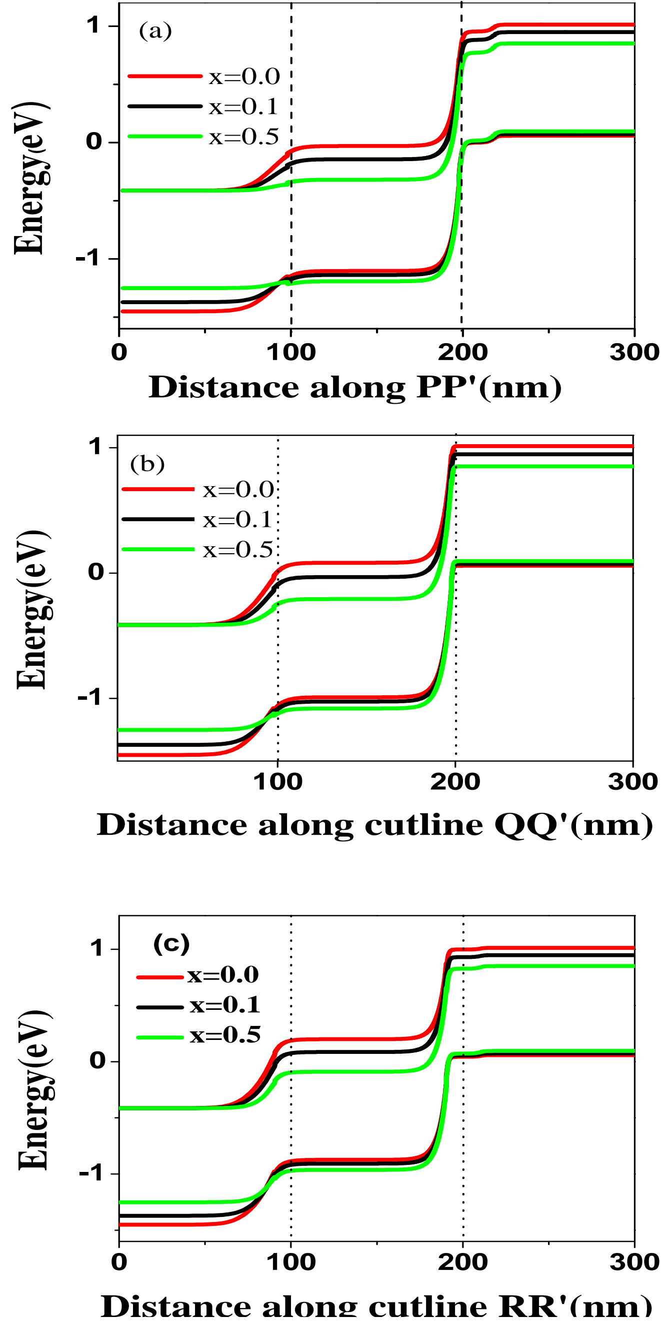

Figure 4.3: Band diagrams to illustrate impact of strain on the the strained DGTFET. The top gate is biased at $V_A = V_{DD}$ and the bottom gate is biased at $V_B = Gnd$ (a) Across cutline PP' just below the top surface (b) Across cutline QQ' near the mid-section (c) Across cutline RR' just above the bottom surface

reduces, and that explains drastic decrease in I_{ON}.

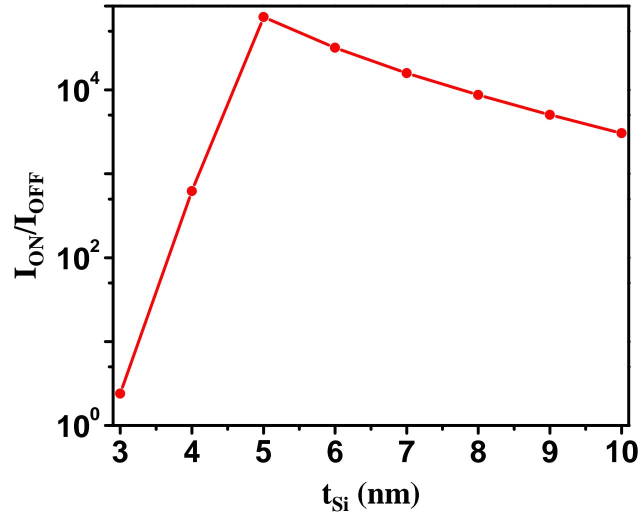

Figure 4.4: The variation of I_{ON}/I_{OFF} ratio of SDGTFET with the Si body thickness (t_{Si}) for x=0.1

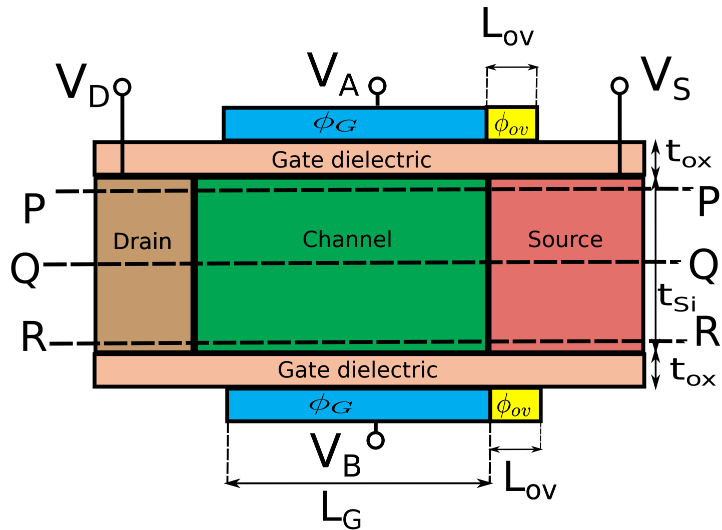

Figure 4.5: Cross-sectional view of DGTFET structure with Dual-Material Gate

By introducing strain the conduction band in the channel gradually lowers down with rise in mole fraction x, this leads to reduction of the tunneling width. The purpose of introducing overlap was to increase the tunneling width such that tunneling is suppressed across the top and bottom surfaces. However as apparent from Fig 4.3(a) the energy of the conduction band of the channel goes down with increase in x, while there isn't significant impact on the valence band energy of the source. Hence the tunneling width reduces

and the impact of overlap nullifies. To circumvent this problem using a Dual Material Gate (DMG) is explored as shown in Fig 4.5. DMG is incorporated, with a lower value of work function on the source side for $x = 0.1$. This is done to ensure that along with the middle of the Si body, BTBT is also supressed near the top and bottom surfaces. This leads to a further decrease in I_{OFF}. The modified device structure is shown in Fig

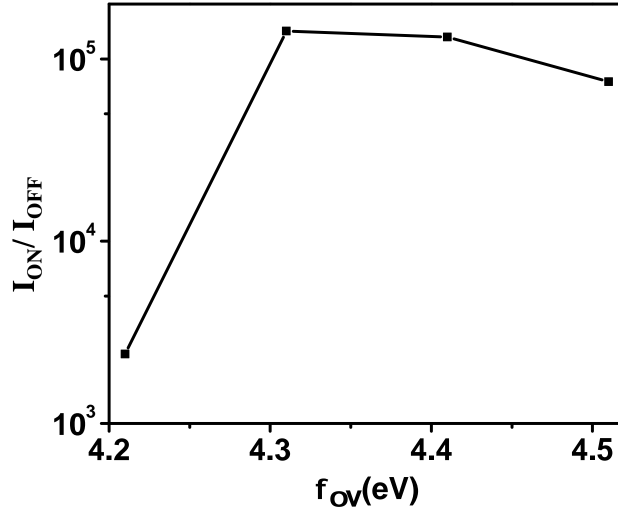

Figure 4.6: The ϕ_{ov} is varied from 4.51 eV to 4.21 eV to further reduce the tunneling across the top and bottom surfaces. The Si body thickness (t_{Si}) is 5 nm and Ge mole fraction (x)=0.1

4.5, there is a lower work function ϕ_{ov} over the overlap length L_{ov}. As apparent from Figure 4.3, with the introduction of strain the conduction band in the channel goes down however the valence band in the source side remains almost invariably at the same energy irrespective of the introduction of strain. This leads to lowering of the tunneling width, the introduction of overlap has no impact as the tunneling overlap(there is large difference in energies of the valence band in the source and conduction band in the channel). The work function of gate is engineered such that the work function of gate above the channel has value $\phi_{Gchannel}$=4.51 eV and ϕ_{ov} is varied from 4.51 eV to 4.21 eV. This is shown in Fig 4.6. It is observed that for $\phi_{ov} = 4.31$ eV there is improvement in the I_{ON}/I_{OFF} ratio. Similar characteristics is observed for other Si body thicknesses.

The above analysis reveals the challenges in suppressing BTBT across the complete device when only one of the gate terminals is at logic "1". An introduction of strain (which has been used to enhance I_{ON} in TFETs) cannot be directly employed in the proposed device to yield higher I_{ON}/I_{OFF}. Si body thickness optimization and using DMG have been

proposed as possible ways to circumvent the above problem.

Chapter 5

Conclusion

In this thesis, it was demonstrated that AND functionality can be realized using a single DGTFET. The two gates of the DGTFET were used independently as two inputs to the device. To realize a device with the best performance gate-source overlap was incorporated and the device thickness was optimized. The device was also shown to operate well at low operating voltages. Lastly, it was demonstrated that the methods which are typically used to boost the ON-state current in a TFET, cannot be directly applied to a TFET that realizes the AND functionality. This is because it is difficult to suppress current flow through the device when only one of the terminals of the device is connected to logic "HIGH".

As a future work, the performance of the realized AND functionality can be further improved. The device structure can be modified to yield better I_{ON}/I_{OFF} ratio. It may be noted that, the study is based on a simple simulation model. However, a detailed analysis that accounts for gate-oxide tunneling, quantum confinement etc. effects must also be done.

Appendix I

A sample input file for the proposed DGTFET which is used to realize the AND functionality. Please refer 3.1

5.1 A1.Sample Input file

```
# Input file for device simulation tool ATLAS
go atlas
#Defining meshes for the device: Meshes should be as fine as possible,
#meeting the computer resource constraints.
mesh space.mult=1.0

x.mesh loc=0.000 spac=0.01
x.mesh loc=0.095 spac=0.001
x.mesh loc=0.098 spac=0.0001
x.mesh loc=0.100 spac=0.0001
x.mesh loc=0.105 spac=0.0001
x.mesh loc=0.110 spac=0.001
x.mesh loc=0.155 spac=0.001
x.mesh loc=0.158 spac=0.0001
x.mesh loc=0.160 spac=0.0001
x.mesh loc=0.165 spac=0.001
x.mesh loc=0.190 spac=0.0001
x.mesh loc=0.200 spac=0.0001
x.mesh loc=0.210 spac=0.001
x.mesh loc=0.400 spac=0.01
```

```
y.mesh loc=-0.003 spac=0.0005
y.mesh loc=0.000 spac=0.0002
y.mesh loc=0.003 spac=0.001
y.mesh loc=0.005 spac=0.0005
y.mesh loc=0.007 spac=0.001
y.mesh loc=0.010 spac=0.0002
y.mesh loc=0.013 spac=0.0005


# defining another mesh for non-local BTBT modelling in ATLAS
qtx.mesh loc=0.04 spac=0.01
qtx.mesh loc=0.09 spac=0.0001
qtx.mesh loc=0.095 spac=0.0001
qtx.mesh loc=0.10 spac=0.0001
qtx.mesh loc=0.105 spac=0.0001
qtx.mesh loc=0.110 spac=0.01
qtx.mesh loc=0.150 spac=0.0001
qtx.mesh loc=0.170 spac=0.01
qtx.mesh loc=0.190 spac=0.0001
qtx.mesh loc=0.205 spac=0.0001
qtx.mesh loc=0.210 spac=0.001
qtx.mesh loc=0.360 spac=0.01


qty.mesh loc=0.000 spac=0.0005
qty.mesh loc=0.003 spac=0.001
qty.mesh loc=0.005 spac=0.0005
qty.mesh loc=0.007 spac=0.001
qty.mesh loc=0.010 spac=0.0005

#Defining regions of the device
region num=1 y.max=0.000 material=Oxide
```

```
region num=2 y.min=0.000 y.max=0.010 material=Silicon
region num=3 y.min=0.010 material=Oxide

#Defining electrodes: channel length in this example is 100 nm
# The top gate A, it is named gate
electrode name=gate x.min=0.1 x.max=0.160 top
#The bottom gate B, it is named substrate
electrode name=substrate x.min=0.1 x.max=0.160 bottom
#The drain electrode
electrode name=drain x.max=0.030 y.min=0.000 y.max=0.0
#The source electrode
electrode name=source x.min=0.35 y.min=0.0 y.max=0.0

#Defining doping: The doping profile is assumed to be abrupt
doping uniform n.type conc=1e17 x.min=0.100 x.max=0.200 reg=2
doping uniform n.type conc=1e18 x.max=0.100 reg=2
doping uniform p.type conc=1e20 x.min=0.200 reg=2

#Defining the tunneling parameter for silicon:
material material=Silicon me.tunnel=0.14 mh.tunnel=0.14 region=2
material material=Oxide permittivity=16


#Defining contacts
contact name=gate workfunction=5.0
contact name=substrate workfunction=5.0

#The structure file for the device in equilibrium
save outf=test_eqb_and.str

#Defining physical models: Band gap narrowing effect is included.
#The effect of concentration dependent mobility and SRH models are also
#included, though their impact in this example is found to be not appreciable.
models bbt.nonlocal qtunn.dir=1 qtunn.el qtunn.ho   bgn consrh conmob print
```

```
#included to improve the convergence
method newton
solve init

#Applying bias for simulation
solve vsource=0.0
solve vgate=0.0
solve vsubstrate=0.0
output val.band con.band charge e.lines
save outf=test_vd_and.str

#in order to improve convergence, drain voltage is increased gradually
solve vdrain=0.03125
solve vdrain=0.0625
solve vdrain=0.125
solve vdrain=0.25
solve vdrain=0.5
solve vdrain=1.00
solve vdrain=1.20
output val.band con.band charge e.lines
save outf=test_00_and.str

#Simulating the transfer characteristics
#the bottom gate biased at 0 V.
#The top gate is varied from 0 to 1.2 V
log outf=./transfer_X0_and.log master
solve vgate=0.0 vstep=0.1 name=gate vfinal=1.2
output val.band con.band charge e.lines
save outf=test_10_and.str

#A temporary file
log outf=./temp_and.log master
solve vgate=0.0
solve vsubstrate=0.2
```

```
solve vsubstrate=0.4
solve vsubstrate=0.8
solve vsubstrate=1.0
solve vsubstrate=1.2

#Simulating the transfer characteristics
#the bottom gate biased at 1.2 V.
#The top gate is varied from 0 to 1.2 V
log outf=./transfer_X1_and.log master
output val.band con.band charge e.lines
save outf=test_01_and.str

solve vgate=0.0 vstep=0.1 name=gate vfinal=1.2
output val.band con.band charge e.lines
save outf=test_11_and.str

quit
```

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Publications based on this work

1. Saptak Banerjee, Shelly Garg and Sneh Saurabh, "Realizing logic functions using single Double-Gate Tunnel FETs: A simulation study," *IEEE Electron Device Letters.* Vol. 39, pp. 773-776, May 2018 (Impact Factor: 3.048).

2. Saptak Banerjee and Sneh Saurabh, "Challenges in implementing AND functionality using single Tunnel FET at low operating voltages," *To be submitted in VLSID Conference 2018.*

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