Continuous Time Linear Equalization based Gigabit Receiver for Parallel Interface

by

Tejaswini K

A thesis submitted in partial fulfillment for the
degree of Master of Technology

under supervision of
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Certificate

This is to certify that the thesis titled "Continuous Time Linear Equalization based Gigabit Receiver for Parallel Interface" being submitted by Tejaswini K (Roll No.- MT16117) to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original work carried out by her under my supervision. In my opinion, thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The results contained in the thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

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Abstract

Modern processors are capable of working at a very high frequency with the advent of technology scaling. However, memory limits the overall speed of operation. In order to take complete advantage of these modern high-performance processors, it is essential to improve the data transfer rates in the memory. As per open NAND flash interface (ONFI) standard, the current data rate is around 800MBps. Between every successive ONFI standard, a 100% improvement in data rate has been observed. By extrapolating the existing trend, the data rate of next generation of ONFI can be about 1600MBps. This project aims at achieving 1333MBps to support an industrial need. Since the speed focused on Silicon is 1333MBps, the thesis strives to achieve 1400MBps in order to accommodate parasitics. At this high frequency, the channel response deteriorates because of dielectric loss and Inter-Symbol Interference (ISI). Additionally, crosstalk in parallel interface degrades the signal integrity. The technique used to restore the channel loss is called equalization. The thesis presents a design of Continuous Time Linear Equalization (CTLE) based gigabit receiver for ONFI parallel interface on 16nm FinFET technology. The design consists of a CTLE, a latch, a Current Mode Logic (CML) to Complementary MOSFET (CMOS) converter and a duty cycle corrector (DCC). A novel design has been proposed to support rail to rail Input Common Mode Range (ICMR) of the receiver to provide flexibility to the transmitter. This receiver compensates an estimated channel loss of 4dB at 1400MHz and provides a dc-gain of 10dB. Further, it maintains 50±1.5% duty cycle to support Double-Data-Rate(DDR) (2.8GbBs). For a given ICMR,a power efficiency of 1.4pJ/bit is achieved which is superior to the state-of-art designs. However, in order to support complete rail to rail ICMR the novel design was showing 4.7pJ/bit.

Acknowledgements

I would like to thank my supervisors Dr. Pydi Ganga, Mr. Shiv Mathur and Mr. Ramakrishnan Subramanian for their guidance and corrections made in the scope of this work.

This work is dedicated to my parents Dr. R Prema, Mr. K G Anantha Rao and my mentor Mr. Aras Kumar R for their teachings and values passed on to me. I thank their understanding even in those moments in which my immaturity prevailed.

I would also like to thank all the team members of the ASIC Analog IO team at SanDisk for their help on obtaining this works final results. Special thanks to Subba Siddamurthy for their enthusiastic discussions. Performing this work among these outstanding professionals contributed a lot to my evolution as a professional and a human being.

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Dedicated to my beloved parents and coach...

Chapter 1

Introduction

Memory has been conspicuously requisitioned in the fast-paced era of electronics. Memory is used in the place where an application needs to load some data during processing, while hard disk storage involves storing data for long and short retention period.

NAND flash memory is a type of hybrid memory which is non-volatile and has an erasable read/write option. In order to read/write data into memory, a controller is needed. The architecture of controller along with the memory is as shown in Figure 1.1. It shows the controller driving NAND flash memory.

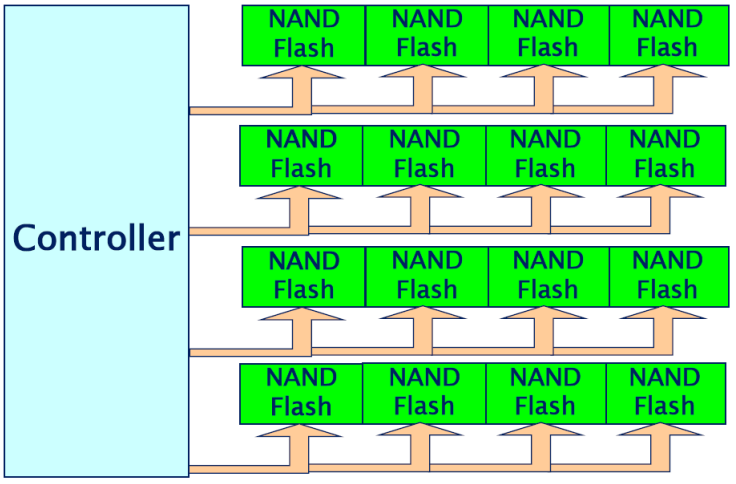
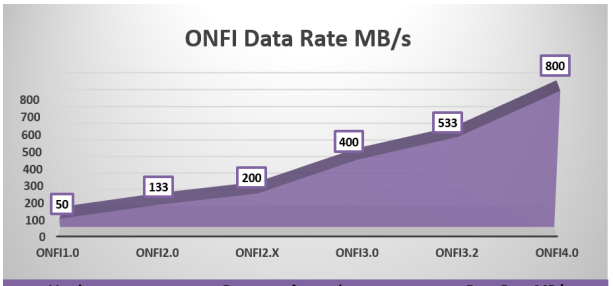


FIGURE 1.1: Controller driving NAND Flash[1]

1.1 Open NAND Flash Interface (ONFI)

There was a need to standardize NAND flash to make it easier to switch between NAND chips from different producers, thereby permitting the faster development of NAND-based products and lower prices via increased competition among manufacturers. The Open NAND Flash Interface (ONFI) is an industry workgroup made up of more than 100 companies that build, design-in, or enable NAND Flash memory. It is dedicated to simplifying NAND Flash integration into consumer electronic products, computing platforms, and any other application that requires solid-state mass storage. It defines standardized component-level interface specifications as well as connector and module form factor specifications for NAND Flash[1]. The trend of increase in the data rate of ONFI is from 50MB/s to 800MB/s over 1.0 to 4.0 version. The Figure 1.2 shows a 100% improvement of data rate from version to version.



Versions	Data transfer modes	Data Rate MB/s
ONFI 1.0	Asynchronous mode	50
ONFI 2.0	source synchronous mode	133
ONFI 3.0	Dual data rate mode	400
ONFI 4.0	Dual data rate mode 2	800

FIGURE 1.2: Trend of ONFI Data Rate[1]

1.2 Parallel Interface

It can be seen that in Figure 1.1 the data transfer is done parallely. The advantages of parallel interface are as follows.

- ☐ Programming is easy;
- ☐ Data rate is high since there is no handshaking of signals required.
- ☐ No latency time.
- ☐ Support large amount of data transfer.
- ☐ For time-sensitive data.

Thus parallel interface has been adopted to drive flash memory. A real-time example of parallel transmission can be video streaming. The concurrent 8-bits of parallel transmission reduces the buffering, unlike serial transmission which has single bit at a time. Hence parallel transmission is preferred for high-speed data transmission.

1.3 Channel

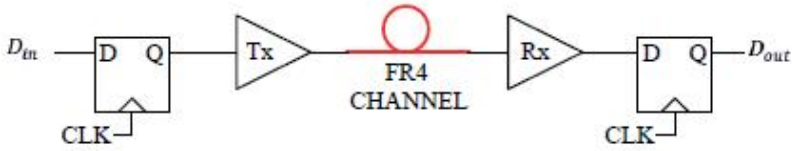


FIGURE 1.3: Transmitter and Receiver with the channel [2]

The controller and NAND flash are connected using metal connectors. The set of metal connectors is called channel. Figure 1.3 shows the transmitter(memory) and receiver(controller) along with the channel. The channel differs from each other depending on electrical and dimensional parameters. The resistivity of the channel increases with the length; the capacitance and inductance are distributed along the length. The interelement capacitance shown in Figure 1.4 affects the signal propagation by the formation of the pole and thus reducing the gain at higher frequencies as shown in Figure 1.5. Usually, the channel is a Flame Retardant4 (FR4) microstrip line. The skin effect, the impedance of the line, the propagation constant, etc. hamper the signal propagation.

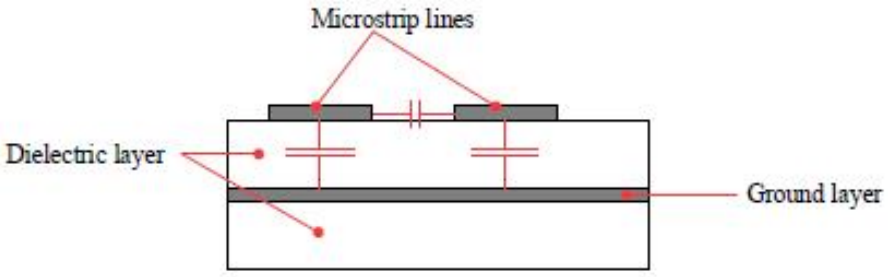


FIGURE 1.4: Microstrip line with interelement capacitance [2]

The requirement to improve speed directly affects the hardware and power constraints. Even though there has been a rapid growth in devices to support high-speed performance, the interconnects have not improved in the same fashion. The channel between the controller and the memory deteriorates the signal with the increase in speed. The ac response of the channel is as shown in Figure 1.5 which shows a drop to -45dB at 20GHz.

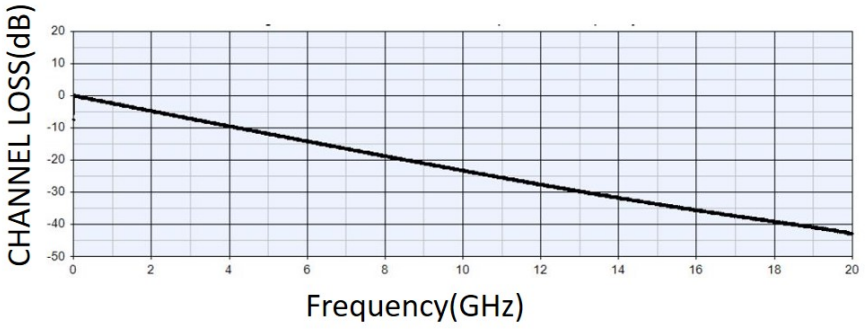


FIGURE 1.5: Channel Response vs Frequency [2]

1.4 Motivation

By extrapolating ONFI data rate, the next version is expected to have 1600MBps of data rate. The main bottleneck involves the presence of a pole at such high frequency which causes the degradation in the channel response. The scenario worsens with factors like crosstalk, jitter, insertion loss, inter-symbol interference, etc leading to the closing of the eye of the signal after channel as shown in the Figure 1.6. The technique of overcoming these shortcomings of the channel at high frequency is called equalization. This technique leads to the opening of the eye which implies reliable data transfer, reduction in jitter, insertion loss, etc.

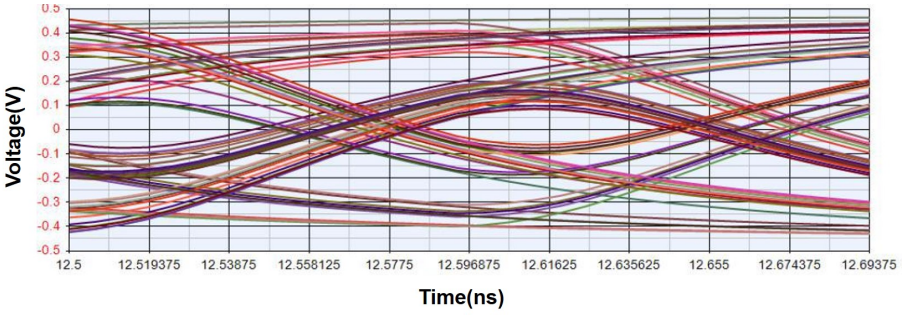


FIGURE 1.6: The closed eye of the signal after channel [2]

1.5 Objectives

The objective of the work involves designing a receiver for NAND Flash Memory.

- ☐ To achieve the targeted data rate of the receiver is 2.8GBps in order to support future versions of ONFI.
- ☐ The expected channel loss of 4dB at 1.4GHz has to be compensated by an equalizer in the receiver.

- A 12dB gain has to be achieved to obtain a reliable transfer of data by the receiver.
- The output signals of the receiver must have a 50% duty cycle.
- A rail to rail input common mode support has to be given to the receiver since the input common mode is unknown at pre-Silicon level.
- The aim is to achieve low power consumption.

1.6 Contribution

The reported work on CTLE based receiver till date supports a constant Input Common Mode Range (ICMR). There is a need to support rail to rail ICMR in order to provide flexibility to the transmitter design. This project has proposed a novel design to operate for a large ICMR and has achieved the desirable performance across Process-Voltage-Temperature (PVT) variation.

1.7 Structure of the Work

This thesis is divided into 5 chapters to reflect the necessary information that leads up to the complete design of a receiver system.

- **Chapter 1:Introduction**
  This chapter gives the introduction to the topic continuous linear time equalization based gigabit receiver. It describes the challenges faced at high-speeds. Additionally it elucidates the motivation,objective and contribution of the project.
- **Chapter 2:High Speed Design Techniques**
  This chapter provides an account for different circuits used in high-speed designing. There is a brief explanation of wideband amplifiers, equalization techniques, rail to rail input common mode amplifiers, gain stage and duty cycle corrector.
- **Chapter 3:Proposed Design of the Receiver**
  This chapter discusses the proposed receiver design and working. The detailed analysis of equalizer, latch, Current Mode Logic (CML) to CMOS converter and duty cycle correcter has been given.
- **Chapter 4:Results and Discussions**
  This chapter shows the results of the proposed receiver. The process corners SS,

TT, FF along with the temperature of -40^oC, 25^oC and 125^oC are varied. The voltage variation is $V_{DD} \pm 5\%$ has also considered.

- **Chapter 5:Conclusions and Future Scope**
  This chapter concludes all the findings and contributions of this work and discusses possible future work.

Chapter 2

High-Speed Design Techniques

There are different techniques to realize high-speed designs. The circuit must have higher bandwidth. It needs to pump large current for faster performance. The power consumption has to be optimized. Keeping the above design concerns, this chapter gives techniques to design high-speed circuits.

2.1 Current Mode Logic Structures

It is a challenge to operate the MOS at unity gain current cut-off frequency (fT). High speed implies charging and discharging capacitors at that high speed. The high-speed blocks must use very less number of active devices in-order to overcome unnecessary loading at each stage; further, the usage of PMOS has to be reduced owing to its low mobility. Current Mode Logic (CML) structures are faster because of there low output swing. Thus it has been adopted in the thesis for high-speed designing.

2.2 Wide Band Amplifiers

As we know using a multistage architecture relaxes the gain-bandwidth requirement per stage, but we still require wide bandwidth in each stage to ensure that the -3 dB bandwidth of the multistage amplifier (ω_A) meets the design specification. In fact, the required single-stage bandwidth (ω_B) is always greater than the multistage amplifier bandwidth i.e.$\omega_B \geq \omega_A$. Therefore, it is important to understand the various methods that can extend the bandwidth of stages.

2.2.1 Capacitive degeneration

One of the methods to achieve a broadband response is to degenerate the transistors in a differential pair such that the effective transconductance of the circuit G_m increases at high frequencies thereby compensating for the gain roll-off due to the pole at the output node. Such an arrangement is shown in Figure 2.1.

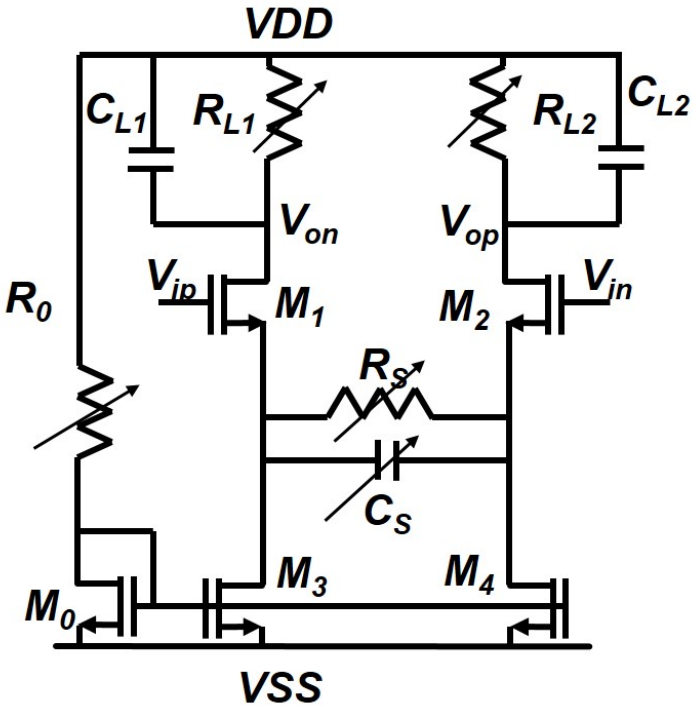


FIGURE 2.1: Wideband amplifier with capacitive degeneration

The circuit transconductance can be expressed as

$$G_m = \frac{g_m(R_s C_s s) + 1}{R_s C_s s + 1 + g_m R_L/2} \tag{2.1}$$

From above notice that the circuit transconductance G_m contains a zero z_1 and pole p_2 at frequencies

$$z_1 = 1/R_L C_L \tag{2.2}$$

$$p_2 = \frac{1 + g_m R_s/2}{R_s C_s} \tag{2.3}$$

If the zero z_1 cancels the pole $p_1 = 1/R_L C_L$ at the drain node, then the amplifiers bandwidth can be extended to pole $p_2 = (1+g_m R_s/2)/R_s C_s$. However, this increase in amplifier bandwidth is obtained at the cost of a proportional reduction in the DC voltage

gain $A_v = g_m R_L/(1 + g_m R_s/2)$. Figure 2.2, shows the variation in circuit transconductance G_m and the voltage gain Av as a function of frequency. In a variation of this pole-zero cancellation technique explained above, if the zero is pushed slightly towards lower frequency (by making C_s large) the frequency response will show a peaking. This technique is called source-peaking. Note, however, that C_s should not be made too large because the resulting gain peaking can distort the overall frequency response of the multistage amplifier. Other advantages of using this method include controlling the stage gain by varying R_s.

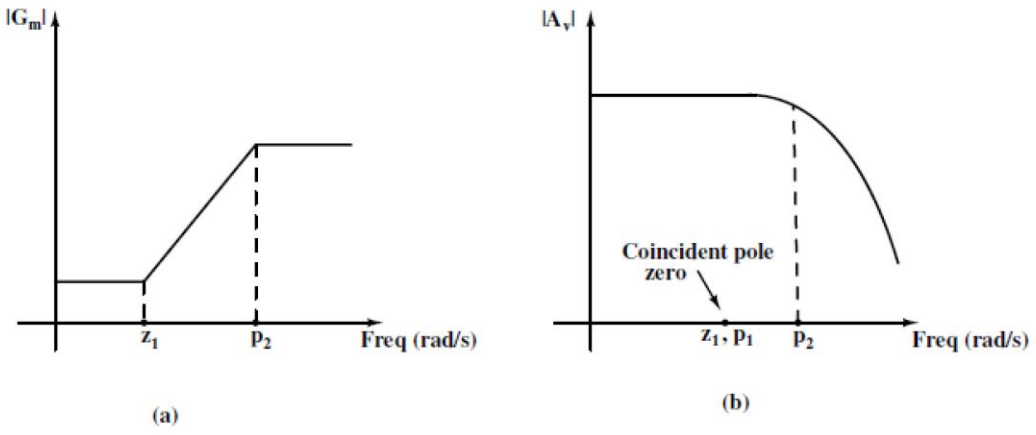


FIGURE 2.2: Variation of (a) Circuit transconductance G_m. (b) Voltage gain A_v with frequency (rad/s)[2]

For further study on wideband amplifiers [2] can be referred.

2.3 Equalizers

The channel loss caused by the microstrip line has to be compensated at high frequency for which wideband amplifiers are needed. The dielectric loss and skin effect lead to large intersymbol interference (ISI) in the channel transmitting data with errors. The technique to compensate the channel loss is called Equalization. It can be done either at transmitter or receiver side. First, let us understand different kinds of the equalizer and later the application of wide-band amplifier.

2.3.1 Feed Forward Equalization

Feed Forward Equalization (FFE) is usually built at the transmitter side of the channel. The coefficients for FFE are calculated based on pre-cursor and post-cursor (evaluated from pulse response of the channel) of the channel response using convolution. The aim

is to remove pre-cursor and post-cursor and obtain solely the main cursor. The cursors are weighted and then added to the system thus reducing the loss. Figure 2.3 shows the architecture of FFE. For a further understanding of DFE and FFE, [5] can be referred.

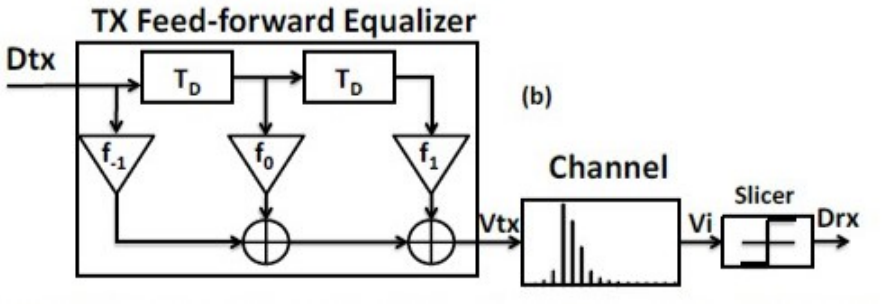


FIGURE 2.3: Feed Forward Equalization

2.3.2 Decision Feedback Equalization

The correction bits amplifies the noise as well in FFE. There is a requirement of clean correction bits to remove the noise amplification, which is done by DFE. The effect of post-cursor is eliminated by this feedback FIR. The equalizer can be made adaptive with the change in the property of the channel. This equalization can only account for post-cursor. This is done on the receiver side and can be seen in Figure 2.4. But the power consumption is high and implementation is difficult.

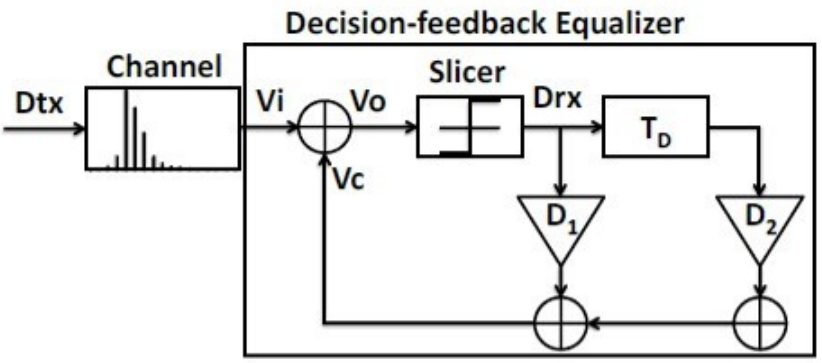


FIGURE 2.4: Decision Feedback Equalization [3]

2.3.3 Continuous Time Linear Equalizer(CTLE)

CTLE, a receiver side equalizer is physically implemented with a differential pair. It is a wideband amplifier as explained in section 2.2. The load resistors R_L set the poles and R_s set the zeros at the required frequency. The circuit is as shown in Figure 2.1. CTLE is used for the smooth channel with comparatively lesser ISI effects. It power-efficient compared to DFE. Hence it is used for this parallel interface project.

2.3.3.1 State-of-the-art Work

The state-of-the-art work has been understood by reading the following papers. A thorough study has been conducted both on parallel links and serial links. Firstly, parallel links are considered. On a 65nm technology, [6] has been implemented. It has a data rate of 16Gbps and channel loss of 15dB with an efficiency of 8 pJ/bit. In [7], there is a channel loss of 15dB for 16/20Gbps data rate. An energy efficiency of 5.3pJ/bit has been achieved on 40nm technology. [8] is designed for a10dB channel loss and 16Gbps data rate, 4.1pJ/bit efficiency has been observed. It is implemented on 40nm technology. 32nm CMOS technology is used in [9] for a data rate of 16Gbps, 11dB channel loss with an efficiency of 1.8pJ/bit. 32nm SOI technology [10] has been used to implement a 16Gbps data rate with 6.2dB loss and 1.8pJ/bit energy efficiency.

The study has been performed to understand the trend of serial links and it is as follows. [4] has a controllable transfer function of a multistage continuous-time linear equalizer (CTLE) has been presented. The whole frequency range into six regions and the value of each is obtained by the inverse transfer function of the channel. There are two applications viz., 6-Gb/s data transfer per channel for high definition multimedia interface (HDMI) 2.0 receiver and 5.4-Gb/s data transfer per channel for DisplayPort (DP) receiver designs. The circuit has been fabricated in a 28-nm ultrathin body and buried oxide fully depleted silicon-on-insulator technology with an area of 0.06-mm2 CTLE. The power consumption is 30 mW. The gain peaking is 28-dB peaking. The total power consumption of complete receiver 55mW having an area of 0.21 mm2, has a power efficiency of 9.2 pJ/bit at 6 Gb/s. The jitter tolerance of 0.7 unit interval (UI) up to 10 MHz for HDMI and 0.42 UI up to 100 MHz for DP, which is superior to their corresponding specifications.

The breach between on-chip and off-chip communication speed has become broader as the IC process technology remains to shrink in order to increase the chip enactment. The speed of on-chip circuit has beaten the off-chip communication speed. But, the legacy of copper cannot support high data rate. As a result, the reliability of the signal is weakened with nonideal effects introduced by the channel. Continuous-Time Linear Equalizer (CTLE) is used at the receiver front-end to compensate the high-frequency losses introduced by the channel. There can be first and second order CTLE as per the requirement. The advantages and disadvantages of both first and second order CTLE have been shown in [11].

The paper [12] a data rate of 10Gbps, the channel loss is compensated by CTLE and 1-tap DFE. The circuit has been implemented on 45nm technology. The cascode structure increases kick-back noise immunity, decreases power consumption by 11%. There is

5GHz clock is driven by proposed PLL with 12.62 pspkpk jitters. The total power consumption is 14.3mW at 1.1V and a channel loss of 15db has been compensated.[13]Two equalizer filter topologies and a combined equalizer/ CDR circuit are described that function at 10 Gb/s in 130nm CMOS technology. Reverse scaling, passive peaking networks, and dual- and triple-loop adaptation techniques help the prototypes adapt to FR4 trace lengths. It is around 24 inches. The equalizer/CDR circuit consumes 133mW at 1.6V. A new CTLE has been implemented in [14]. It is used for low supply voltage with a degenerated differential pair. The data rate is 2Gbps simulated on 90nm 50-m SI-POF. The total power consumption is 2.7mW with 1V of the power supply. [15]The polynomial chaos expansion (PCE) with stochastic testing (ST) is used on three generic CTLEs. The variation in eye-opening has been compared from 2 to 18Gbps and relative impact in closing and opening eye has been measured.

Thus, the low power hungry and efficient equalizer CTLE has been chosen for the design. CTLE can be realized in the first order or second order.

2.3.3.2 Working of CTLE

The architecture of CTLE is as shown in Figure 2.5 and the understanding is as per [4].CML structure of CTLE places the poles and zeros precisely and hence it is used for high-speed design independent of technology.

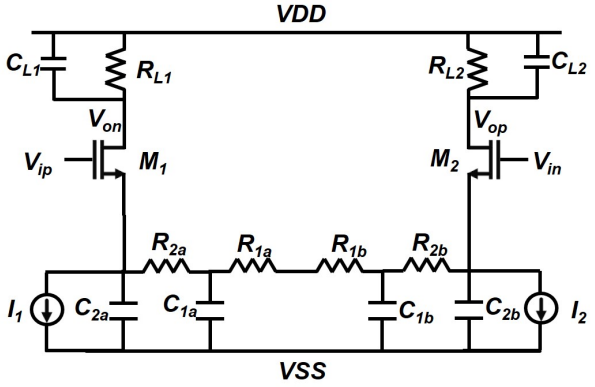


FIGURE 2.5: Circuit schematic of Second Order CTLE

The resistor R_L sets the roll off pole. The resistors R_1 and R_2 along with C_1 and C_2 set zeros. R_1 and R_2 is chosen less than R_L to obtain a dc gain. The point between R_{1a} and R_{1b} acts as ac ground. C_{1a} shorts R_{1a} thus giving a boost and setting a zero. $C_1 \geq C_2$, then C_2 comes into picture to short R_2 to give more boost. The peak of the boost is set by current and g_m of driving transistors. The description can be seen in the Figure 2.6. An approximate small signal model is represented in the Figure 2.7. This

gives small signal model of half symmetric circuit. The analysis of the circuit along with the equation is given in Chapter 3.

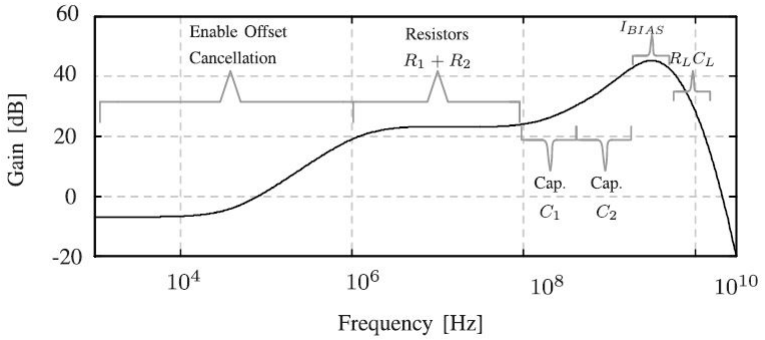


FIGURE 2.6: Frequency response of CTLE [4]

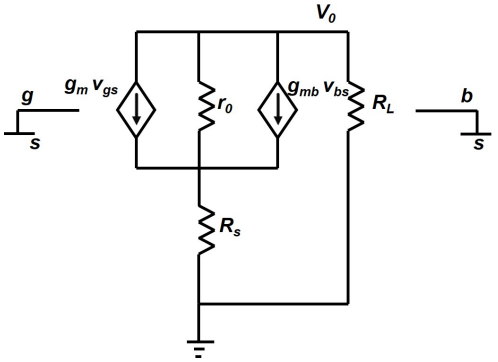


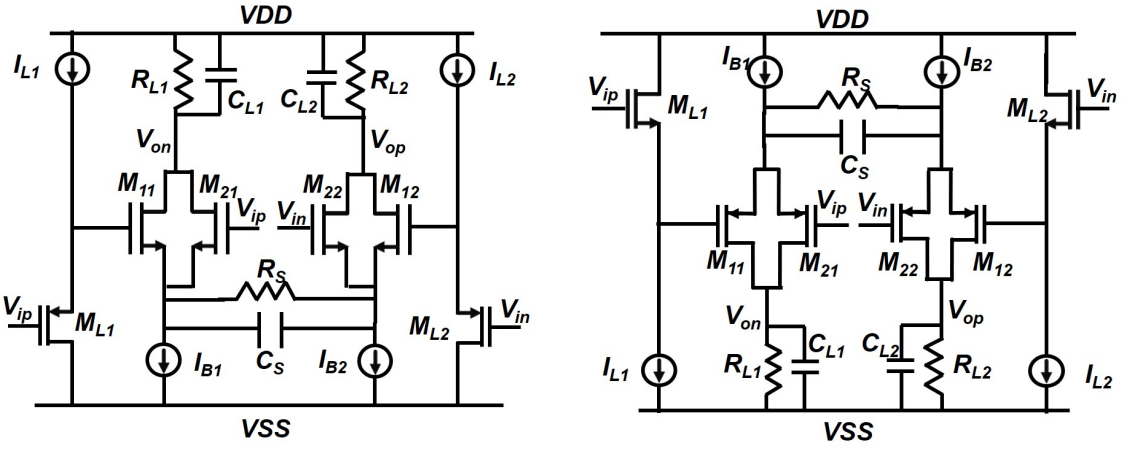
FIGURE 2.7: Small Signal model of CTLE

2.4 Rail to Rail Input Common Mode Amplifiers

Once the CTLE is comprehended, the study has been conducted to support rail to rail ICMR. To attain power consumption of 90W for 1.8V supply voltage, a compacted high-accuracy rail-to-rail CMOS operational amplifier (Op-Amp) is presented. It uses strong inversion techniques. Two complementary differential pair techniques and one-versus-three current mirror compensation techniques are adopted to realize wide input dynamic range, while the output stage provides the rail-to-rail output drive through the use of resistor-compensation circuits (RCC) and self-regular circuits (SRC). The output is simulated and the area is just $0.005mm^2$ and there was also the improvement in THD [16]. TO support rail to rail ICMR, folded cascode with self-bias technique is used in [17]. It is for an ultra-low voltage of 0.5V on 90nm CMOS technology. [18] uses simple architecture such as level shifter to implement constant gm, a folded cascode to combine amplifiers and then a class AB amplifier to obtain a gain. It has been implemented on 130nm CMOS technology, with a 1.5V power supply voltage and consumes just 215W,

and provides a 125dB gain. A pmos and nmos amplifiers, the working principle of [19] consists of comparing the total trans-conductance of a pair of pMOS and nmos with a reference value and then, appropriated tail currents are generated for the complementary input pairs. The input common mode range is from 0 to VDD(3V) on 0.8 mm CMOS technology. The zener diode to implement rail to rail amplifier in [20]. [21] Two novel CMOS differential amplifiers are presented. Both differ from conventional CMOS differential amplifiers in having fully complementary configurations and in being self-biased through negative feedback. The amplifiers have been applied as precision high-speed comparators in commercial VLSI CMOS integrated circuits.

Going through the above papers level shifter has been used to implement rail to rail amplifier as shown in Figure 2.8. But the shortcoming was as shown in Table 2.1. The implementation of the p-level shifter to support lower voltages of n-CTLE has been shown in Figure 2.8 (a). The output becomes independent of input below 300mV. The same case holds with p-CTLE.



(a) N-Based CTLE with Level Shifter (b) P-Based CTLE with Level Shifter

TABLE 2.1: Dead-zone for Level Shifter and Rail to Rail amplifier

CTLE Type	Level-Shifter Type	Non-Operational Vin
N-CTLE	P-level shifter $\leq$ 300mV , output of LS is pulled to VDD	CTLE output is independent of ICMR
P-CTLE	N-level shifter $\geq$ 1V , output of LS is pulled to VSS	CTLE output is independent of ICMR

FIGURE 2.8: CTLE with Level Shifter

Since level shifter implementation did not provide the solution, two different channels for p and n based devices have been kept. A training would be given to system to set ICMR by analyzing the eye measurements by varying the input from rail to rail amplifier. The ICMR cannot be varied dynamically with this architecture. To have a dynamically varying support of ICMR, folded cascode has been implemented and explained in Chapter 3.

2.5 Gain Stage

The gain from the single CTLE stage is not sufficient since the focus in CTLE is to obtain a peaking at high frequency. Hence a gain stage serves the purpose. One of the gain architectures is Operational Trans-conductance Amplifier.

2.5.1 Operational Trans-conductance Amplifier(OTA)

The existing literature has been referred to understand the OTA and its application. The ever-increasing hunt for low power circuits keeping large operational bandwidth has led the design community to opt for Current Mode Techniques for Analog Circuit applications. The design in [22] provides high gain and bandwidth using positive feedback. It is implemented on 90nm CMOS technology with 1V power supply and loaf of 0.5fF. The gain varies from 24dB to 63.3dB gain with increasing the Unity Gain Frequency (UGF) from 8.33 GHz to 11.12GHz.The power consumption is 11.39 W. An adjustable bulk-driven operational transconductance amplifier (OTA) employed at weak inversion region is implemented in [23]. Depending on the traditional positive feedback source degeneration technique, a proposed current-shunt auxiliary amplifier is employed. The proposed architecture improves the UGF by 120% with a negligible increase in power consumption.[24] has been implemented on 45nm having a cascode structure that works in the subthreshold region.OTA in [25] is a single Miller capacitor and an inverting current buffer embedded in the input stage are exploited to implement the frequency compensation network. Additional feed-forward path and a slew rate enhancer are also utilized to improve the large-signal transient response. The dc gain is more than 110dB and also load is 0.5nF.

By understanding the importance and application of OTA, to move further with the circuit as shown in Figure 2.9,the output of CTLE is given to input of OTA. The drivers M_1 and M_2 drive the input , it reflects in M_3 and M_4 mirrored to M_5 and M_6 respectively. Since the current in M_5 and M_7 are same, M_8 gets the mirrored current from M_7. M_6 and M_7 form the AB amplifier stage.

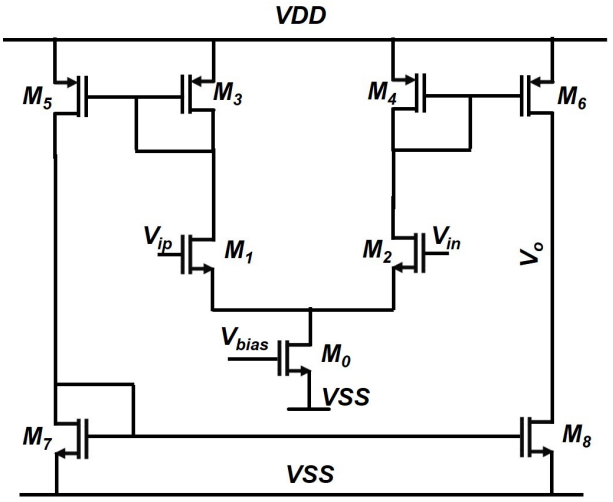


FIGURE 2.9: Operational Trans-conductance Amplifier

Though OTA gives CML to CMOS conversion, the implementation and testing of OTA proved it to be a very power hungry device and with the parallel interface, the current gets multiplied 8 times(for each byte transfer). Hence it has been replaced by another gain stage, latch.

2.5.2 Latch

To obtain an idea of latch following papers were studied. In [26], a new reliable high-resolution and high-speed dynamic latched type comparator with offset cancellation mechanism is presented. The proposed paper presents a 1.25GS/s and achieves 14-bit resolution in presence of 10mV input offset. Also, as simulation results prove that, in the worst-case condition when the V_{DD}=1V, the propagation delay time of the suggested paper is 292ps, meanwhile, while V_{DD}=1.8V, the delay time is decreased 126ps, noticeably. The power consumption of the proposed structure is 342 W with the power supply of 1.8V, as well. Regenerative comparators due to its power efficiency and high-speed finds usage in many high-speed and low-power analog-to-digital converters. In [27], a novel comparator based on double-tail architecture is proposed to improve latch regeneration speed. Upon examining the delay expressions of some prevailing double-tail structures, the structure of latch stage is modified by adding cross-coupled transistors to improve latch regeneration thus augmenting evaluation speed. It has been implemented on 90-nm CMOS technology. [28] uses Adomian Decomposition Method to calculate the non-linear differential equations of the regenerative circuit because circuit simulators like SPICE and Spectre solve the nonlinear differential equations numerically to obtain the time domain behaviour. These numerical solutions neither give a closed form expression of the regeneration time-constant nor they give an expression of time domain behaviour

in closed form. ADM can be used to obtain the complete time-domain behaviour and the regeneration time constant.

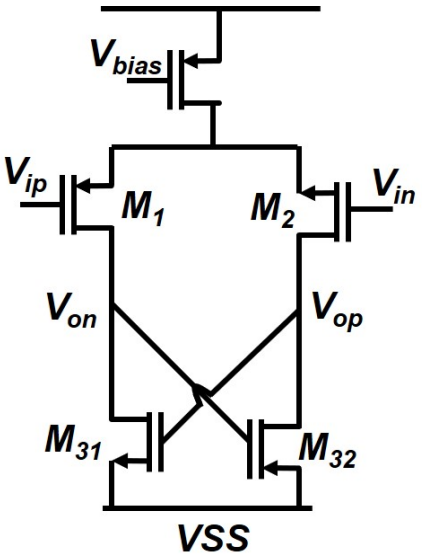


FIGURE 2.10: Latch

The understanding of latch is as follows. The positive feedback owes to high gain and thus the bandwidth is less . Figure 2.10 shows the circuit diagram of the latch. It can be seen that output stage senses the high capacitance seen at gates of M_{31} and M_{32}.In order to move the pole away, resistors are placed such that the output does not see the large capacitance. It might increase the delay since resistance is coming into the picture but the bandwidth improves by carefully placing zeros.

Section 2.1 tells about the requirement of CML to CMOS conversion. The inverter has been implemented for the same.

2.6 Duty Cycle Correction

In order to digitize the signal and to convert from CML to CMOS, series of inverters have been placed at the output of the latch. But the duty cycle was not 50%. Hence the search to fix the duty cycle was carried out.

In [29] a balanced duty cycle is generated by using an edge combiner and also by removing mismatch. It has been implemented on 180 nm and at the frequency of 250 to 625MHz. The duty cycle variation from 30% to 70% is fixed to around 70%. [30] A DLL is implemented on 130nm with a power and area consumption were around 30mW and 0.03mm$\hat{2}$ at 2.5GHz. The jitter is around 14ps. Even this paper uses a unique technique to implement duty cycle correction which has been implemented in the work. [31]

deals with high-speed transmission of signals at 1066MHz and the duty cycle and phase alignment techniques are implemented. A low-cost duty cycle corrector has been implemented in [32], the technique provides 50% duty cycle for a wide range of frequencies.[33] speaks about improving 10% to 90% variation of the duty cycle to 50% implemented on 130nm. The power consumption is around 15mW with 1.5V power supply. Once the different blocks of high-speed design have been comprehended, the effort was conducted to implement it on 16nm FinFET technology, the design has been explained in Chapter 3.

Chapter 3

Proposed Design of the Receiver

After an exhaustive study on different high-speed design techniques, the design was implemented on 16nm FinFET. This chapter gives a complete idea of architecture and design of the receiver.

3.1 Specification

The specification of the design has been shown in the table 3.1. The high-frequency design has been implemented in the thesis on 16nm FinFET.

Table 3.1: Specification

Supply	1.2±10%V
Data Rate	2.8Gbps
Peaking	4dB @ 1.4GHz
DC Gain	10dB
Duty Cycle	50±3%
Input Common Mode Range	Rail to Rail

3.2 Architecture

The receiver architecture involves CTLE to compensate for channel loss. Amplifier/s to provide the gain. CTLE being a CML structure, CML to CMOS converter is required along with a duty cycle corrector. With a 50% duty cycle, the signal digitized and transferred to System-on-Chip(SoC) Figure 3.1 shows the block diagram of the receiver.

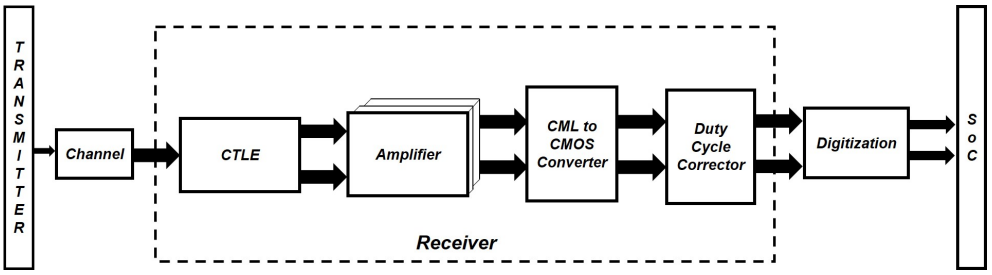


FIGURE 3.1: Architecture of the Receiver

3.2.1 First Order CTLE

Chapter 2 gives the explanation of CTLE. In Figure 3.2, the load resistors R_L set the roll-off pole, R_s and C_s set the zero and the g_m owing to the current in the circuit decides the peaking. From the understanding of CTLE it can be concluded that the value of g_m is comparatively higher to support large current and R_L is comparatively lower to set roll off at high frequency.

In Figure 3.2 the transistors M_1 and M_2 are the driving transistors. The R_s causes source degeneration. C_s sets the zero and R_L rolls off the gain. The first zero is at [11]

$$\omega_z = \frac{1}{R_s C_s} \tag{3.1}$$

The first pole is at

$$\omega_{p1} = \frac{1 + g_m R_s/2}{R_s C_s} \tag{3.2}$$

The role-off pole is at

$$\omega_{p2} = \frac{1}{R_L C_L} \tag{3.3}$$

Here C_L is the capacitance seen by the output.

The gain can be given by

$$A = \frac{g_m R_D}{1 + g_m R_s/2} \tag{3.4}$$

The boost factor is given by

$$K = \frac{\omega_{p1}}{\omega_{p2}} = 1 + g_m R_s/2 \tag{3.5}$$

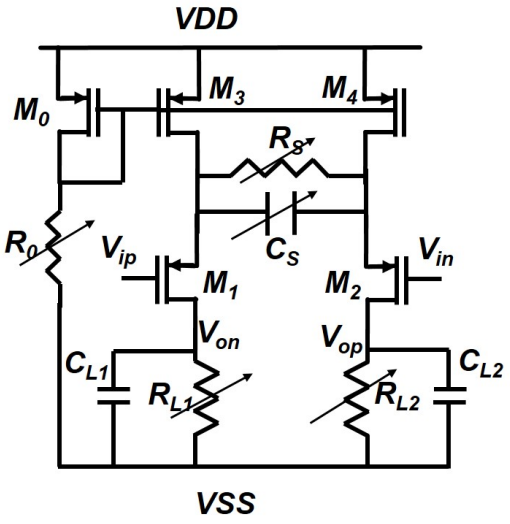


FIGURE 3.2: First Order N-Based CTLE

3.2.2 Biasing

The CTLE has to be biased for proper functioning. The resistance biasing technique is the best for CML structure. In the gain equation above, g_{m1} and $1/R_L$ are comparable to each other. Across corners, if R_L decreases the gain has to decrease but R_0 in resistor biasing also reduces. Thus current through R_0 increases resulting in increase in gain since $g_m \alpha \sqrt{I}$. Thus the gain is balanced with the change in R.

3.2.3 Gain Stage and CML to CMOS Converter

The CTLE is aimed to achieve high bandwidth and the hence gain is targeted is less. There is a trade-off between gain and bandwidth. The gain is achieved from the next stage. A latch is adapted to obtain the gain. The positive feedback of the latch in Figure 2.10 owes to high gain. It can be seen that output stage senses the high capacitance seen at gates of M_{31} and M_{32}.

The output impedance of latch is

$$r_{out} = r_{0m1} || r_{0m31} \tag{3.6}$$

The pole is carefully placed at

$$p_1 = \frac{1}{r_{out} C_{32}} \tag{3.7}$$

where r_{out} is from 3.6.

The swing of CTLE, a CML structure along with latch would not be sufficient to turn off the following CMOS blocks. This increases the static power consumption. The latch improves the gain and thus the swing. The inverter pulls the output from rail to rail, acting as CML to CMOS converter.

CML to CMOS conversion doesn't ensure 50% duty cycle. The parallel interface of the design has 8 data signal and 2 clock signals. The signals must have 50% duty cycle to ensure reliable sampling of the data. The output of CTLE and latch does not have the required duty cycle. Hence a duty cycle corrector circuit has been implemented.

3.2.4 Duty Cycle Correction

The output of differential pair signal is provided as input to Duty Cycle Corrector(DCC) in Figure 3.3. The edges of the output are pulled equally by a differential pair. The transistors associated with clk is on and capacitor at DCCout is charged to VDD. When the signal falls down, clkb is still not high enough to pull DCCout to zero hence the charge on the capacitor is stored. When clkb becomes high, DCCout is pulled down to zero. This process helps to achieve 50% duty cycle.

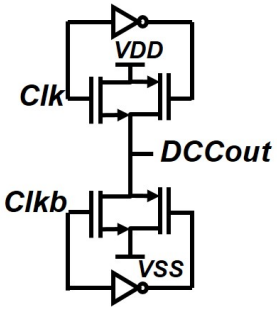


FIGURE 3.3: Duty Cycle Correction

The Figure 3.4 shows the detailed block diagram of the receiver. It has a first order CTLE to boost the gain at 1.4GHz. The latch to increase the dc gain. Inverter acts as CML to CMOS converter. A duty cycle corrector has been used to get a 50% duty cycle. Then the signal is digitised to send it to SoC.

3.2.5 Rail to Rail Input Common Mode amplifier

The other objective is to provide rail to rail support. The level shifter with CTLE in Figure 2.8 could not satisfy the requirement. Hence there are two separate channels for n and p based designs and a training would be given. And an analog MUX can be used to select the channel as shown in Figure 3.5.

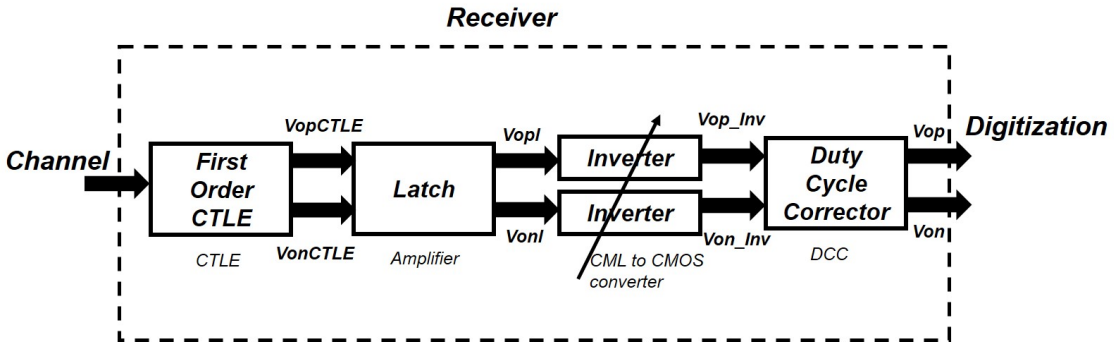


FIGURE 3.4: Detailed Block Diagram of Receiver

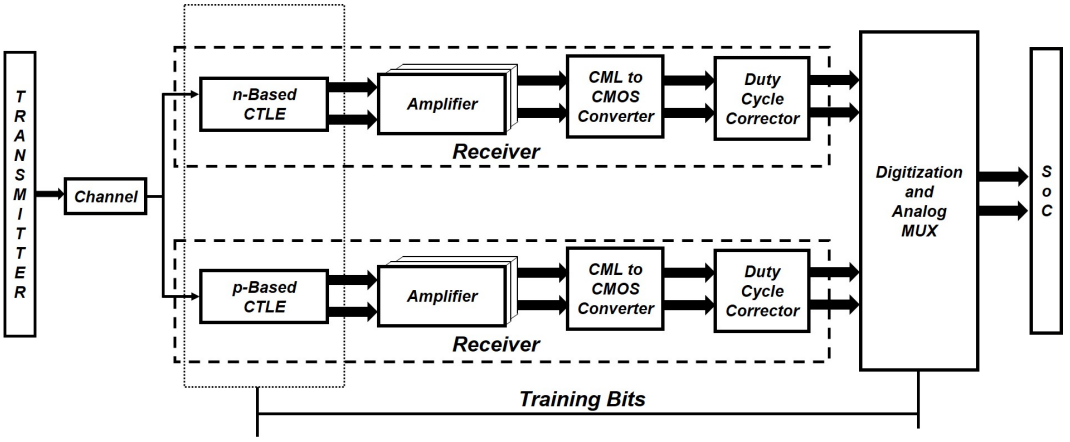


FIGURE 3.5: Receiver with Rail to Rail Input Common Mode

3.2.6 Dynamic Selection of Input Common mode

The architecture in Figure 3.5 does not have dynamically adjustable input common mode range. Two different amplifiers and CML to CMOS converters must be used in order to satisfy the gain for p-based and n-based CTLE. This would be overhead and consumes extra area.

Hence in order to dynamically select the input common mode range a folded cascode structure has been adopted as shown in Figure 3.6. The transistors Mp1-2 and Mn1-2 act as input to the rail to rail support. The transistors Mp3-4 and Mn3-4 are the current sources to the CTLE. The Rs and Cs are used to generate zero at the required frequency.

The zero is placed by either n-based CTLE or p-based CTLE depending on the input common mode range and is given by

$$\omega_z = \frac{1}{R_s C_s} \tag{3.8}$$

R1,2 generate external bias to folded cascode devices. We know that output impedance of folded cascode is large,

$$r_{out} = g_{mn6} r_{on6} (r_{on8} || r_o n2) || g_{mp6} r_{op6} (r_{op8} || r_o p2) \tag{3.9}$$

In order to improve the bandwidth, an inverter with resistive feedback is used. Then the final output impedance along with inverter feedback would be

$$R_{out} = R_3 || r_{out} \tag{3.10}$$

where r_{out} is from Equation 3.9.

Hence the pole is set at

$$\omega_p = \frac{1}{R_{out} C_l} \tag{3.11}$$

where R_{out} is referred from Equation 3.10 and C_l is the capacitance seen by the output of inverter namely, C_{ds} of inverter and C_{gs} of next stage.

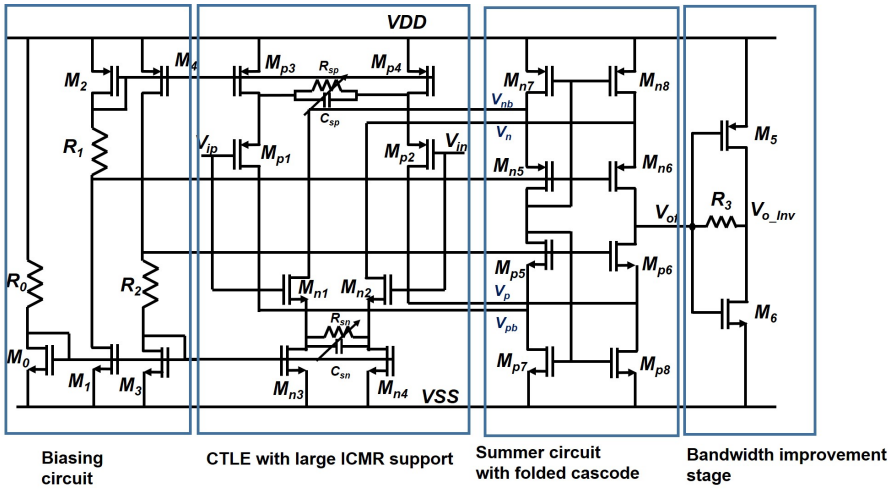


FIGURE 3.6: Proposed CTLE with Folded Cascode to support rail to rail ICMR

The complete architecture with rail to rail input common mode is as proposed in Figure 3.7. Since the gain from the folded cascode is too less because of dropping the output node to R_3, the gain has to be obtained from amplifier stage. The latch is used as the gain stage to increase the gain of the CTLE. The differential signals are generated by using two folded casode blocks and given to duty cycle corrector to improve the duty cycle of the receiver which later is given to digitization block and then to SoC.

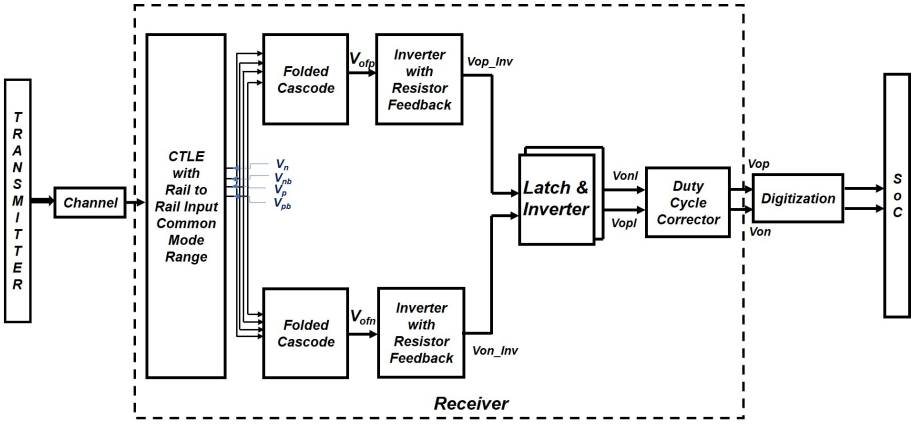


FIGURE 3.7: Complete Architecture of Rail to Rail Input Common Mode Receiver

Chapter 4

Results and Discussion

The simulation results that define the receiver has been presented in the course of this chapter. The schematics are designed in Cadence Virtuoso and in TSMC 16nm FinFET technology.

4.1 Receiver

4.1.1 AC Analysis

The receiver is supposed to provide a gain of 10dB with 4dB peaking at 1.4GHz. The multiple stages help in providing higher gain. The AC response of CTLE is shown in Figure 4.1 which has -0.5dB dc gain. The intention of this stage is to obtain very high operating frequency, hence gain has been intentionally kept less. The peaking is around 4dB at 1.4GHz has been achieved. The phase plot can also be seen in the result. The output of CTLE is given to latch to increase the gain. The gain of 10 dB has been achieved by the latch as shown in Figure 4.1

4.1.2 Transient Analysis

Once the AC analysis is complete, the circuit has been tested for transients. An input to the receiver is 200mV with 40ps slew. The transient analysis has been performed and the result is plotted at every node. Figure 4.2 shows the output of each stage, the second strip shows the output of CTLE with a swing of 265mV. The improvement in the swing is observed at the output of latch with 650mV swing. Then it is given to DCC and digitised finally.

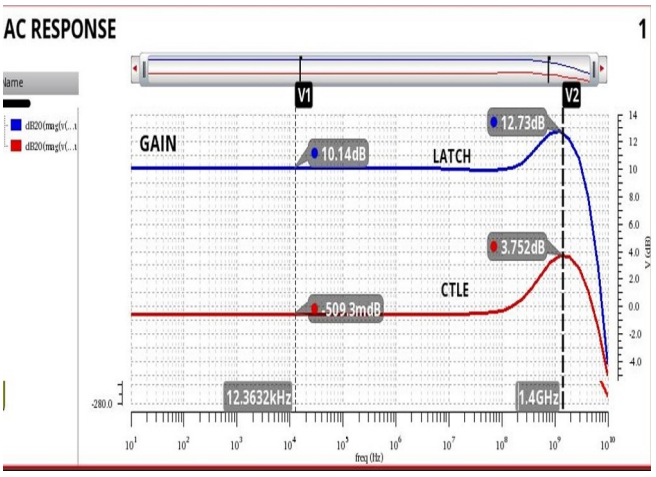


FIGURE 4.1: AC response of the receiver

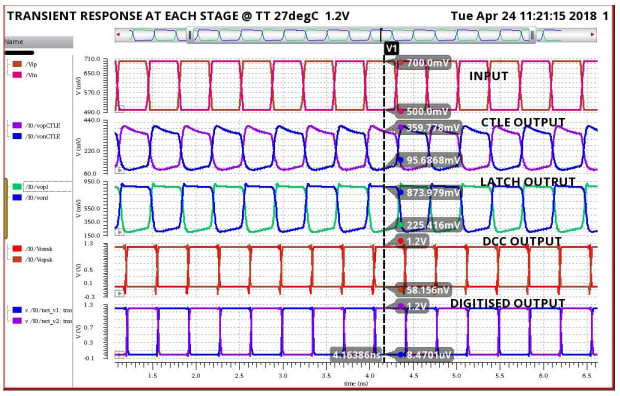


FIGURE 4.2: Transient response of the receiver

To test cross corners, the transient analysis is performed for SS, TT, FF with the temperature variation of -40deg, 27deg and 125deg Celsius and voltage variation of 1.26, 1.2 and 1.14 as shown in Figure 4.3. The output is faithfully swinging from 0 to 1.2V cross corner. The duty cycle that has been a major concern in the receiver has been achieved carefully. The duty cycle corrector corrects the duty cycle the variation is about from 50 ± 1.5% .The maximum current in FF corner with 1.26 VDD is 3.2mA. The power consumption is 4mW. The energy efficiency at 2.8Gbps is 1.4pJ/bit

.

4.2 Folded Cascode

4.2.1 AC Analysis

The gain of the folded cascode has been dropped because of the inverter resistor feedback as shown in Figure 3.7. The gain of folded cascode CTLE with the inverter is -7dB and

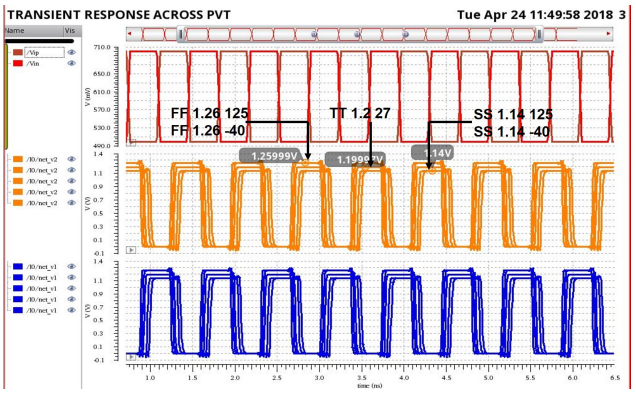


FIGURE 4.3: Transient response across PVT variations

then latch has been used to recover the gain to 5dB is as shown Figure 4.4.

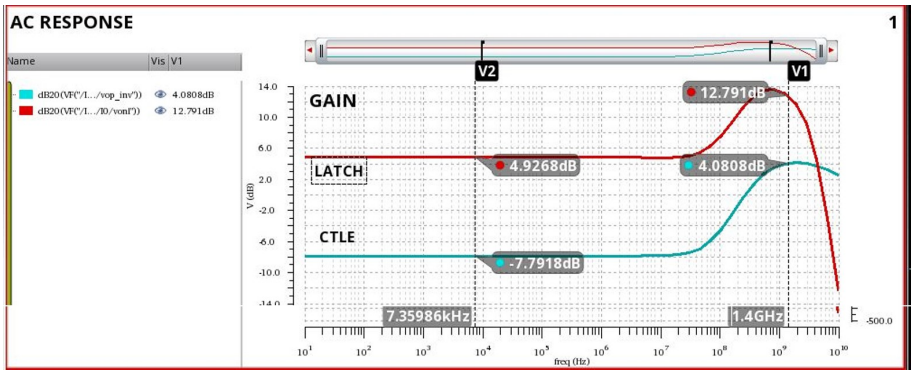


FIGURE 4.4: AC response of Rail to Rail ICMR receiver

4.2.2 Transient Analysis

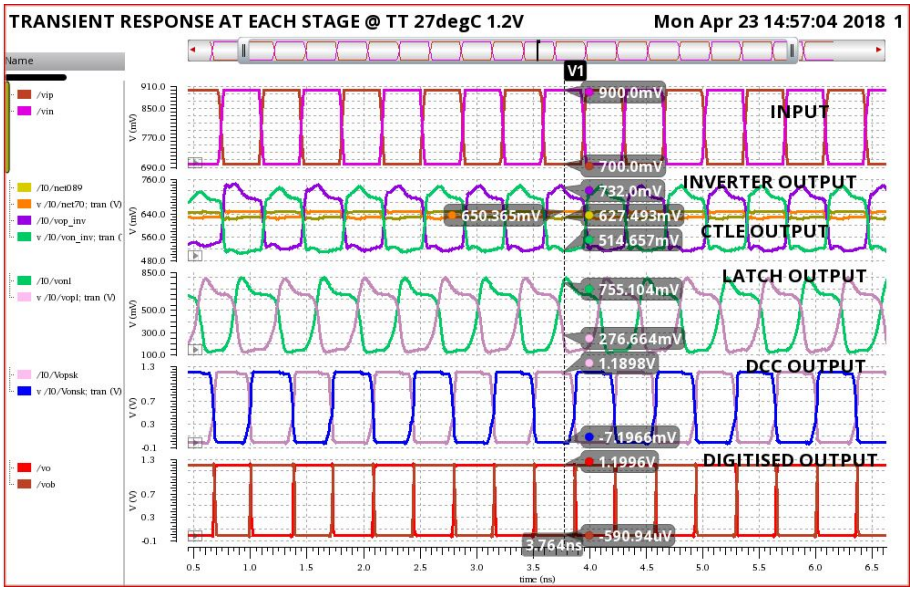


FIGURE 4.5: Transient Response at each stage

To conduct transient analysis on folded cascode architecture, the input of 200mV and the slew of 40ps has been given to the receiver in Figure 3.7. The output of folded cascode CTLE is as shown in Figure 4.5. The gain at the output of folded cascode is too low and it can be seen in the figure. Then the inverter with feedback resistor improves the swing from 22mV to 218mV. The output of the inverter is given to latch, improves the swing to 534mV. Then DCC corrects the duty cycle to 50% and then it is digitized.

The transient analysis is cross corner along with input common mode variation is as shown in Figure 4.6 with the variation of temperature from -40deg, 27deg and 125 deg Celsius with V_{DD} variation of 1.26V, 1.2V and 1.14V across SS, TT, FF corners. The variation is found to be 50 ±1.5%

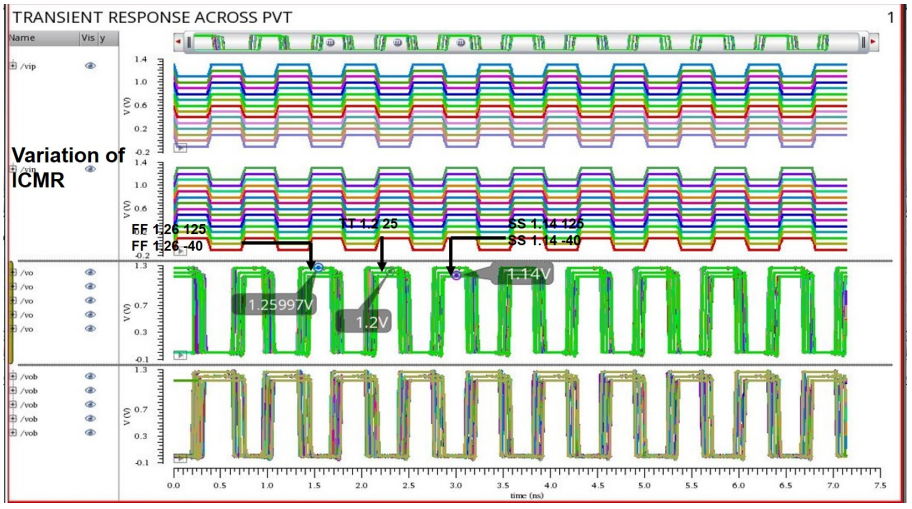


FIGURE 4.6: Transient Response at Cross Corners

The current rating has been shown in Figure 4.7 across PVT. The variation of current is from 3.44mA to 10mA. The power consumption would be 12.6mW and power efficiency would be 4.5pJ/bit

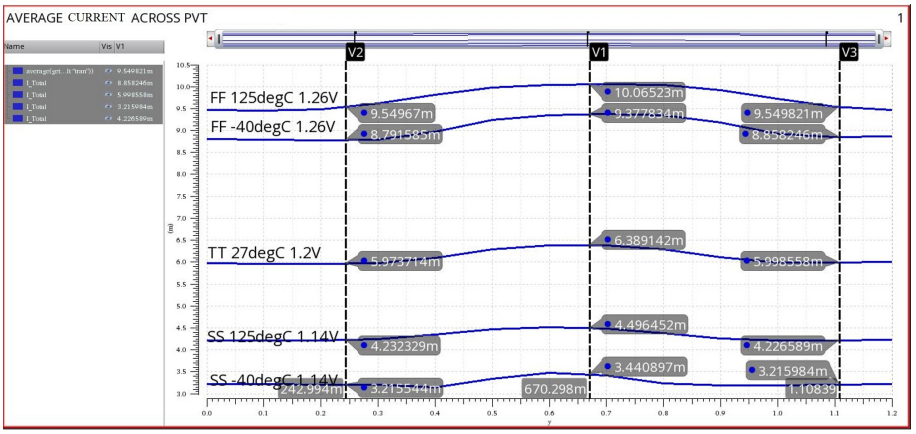


FIGURE 4.7: Current Variation at Corners

4.3 Comparison

Table 4.1 tells about the existing comparison of existing data with the present work. The present work has been power efficient compared to the existing work, it has 1.4pJ/bit of efficiency. Though efficiency of 4.5pJ/bit is low, the architecture is used to support large ICMR. This architecture is the first experiment in the history of CTLE to support rail to rail ICMR.

TABLE 4.1: Comparison with previously reported work

	[6]	[7]	[8]	[9]	[10]	This work
Technology	65nm	40nm	40nm	32nm	32nm SOI	16nm FinFET
Data Rate (Gbps)	16	16/20	16	16	16	2.8
Peaking (dB)	15	15	10	11	6.2	4
Efficiency (pJ/bit)	8	5.3	4.1	2.6	1.8	1.4 ========== 4.5 $\parallel ICMR => 0 - 1.2V$

Chapter 5

Conclusion

A novel architecture has been proposed to support large ICMR between complete rails. This work is successfully able to compensate channel loss at 1.4GHz. All circuits are designed and simulated on 16nm FinFET technology. The circuit performance has been robust against PVT variation and the duty cycle has ±1.5% variation compared to typical value. The proposed design can support next generation ONFI standard. For known ICMR, we were able to achieve 1.4pJ/bit which is much improved compared to the state of art. The energy efficiency is 4.5pJ/bit in order to support rail to rail ICMR.

5.1 Future Work

Though for the fixed ICMR the architecture is better compared to existing systems, for rail to rail variation of input common mode the power consumption is high and it can be reduced by improving the current design or by implementing different architecture. The delay of each block has to be measured and then optimized to obtain the least delay at high speed. The offset cancellation can be easily done off-chip, but an on-chip offset cancellation circuit can be implemented.

Bibliography

[1] URL http://www.onfi.org/.

[2] Shiv Harit Mathur. Design of continuous time linear equalization (ctle) based receiver for gigabit links, bits.

[3] Yue Lu. Energy-efficient equalization circuits for high-speed wireline links,electrical engineering and computer sciences university of california at berkeley. URL http://www2.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-178.html.

[4] P. S. Sahni, S. C. Joshi, N. Gupta, and G. S. Visweswaran. An equalizer with controllable transfer function for 6-gb/s hdmi and 5.4-gb/s displayport receivers in 28-nm utbb-fdsoi. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 24(8):2803–2807, Aug 2016. ISSN 1063-8210. doi: 10.1109/TVLSI.2016.2530680.

[5] Ankit Jain. Equalization in continuous and discrete time for high speed links using 65 nm technology,electrical engineering and computer sciences university of california at berkeley. URL http://www2.eecs.berkeley.edu/.

[6] H. Lee, K. Y. K. Chang, J. H. Chun, T. Wu, Y. Frans, B. Leibowitz, N. Nguyen, T. J. Chin, K. Kaviani, J. Shen, X. Shi, W. T. Beyene, S. Li, R. Navid, M. Aleksic, F. S. Lee, F. Quan, J. Zerbe, R. Perego, and F. Assaderaghi. A 16 gb/s/link, 64 gb/s bidirectional asymmetric memory interface. *IEEE Journal of Solid-State Circuits*, 44(4):1235–1247, April 2009. ISSN 0018-9200. doi: 10.1109/JSSC.2009.2014199.

[7] K. Kaviani, T. Wu, J. Wei, A. Amirkhany, J. Shen, T. J. Chin, C. Thakkar, W. T. Beyene, N. Chan, C. Chen, B. R. Chuang, D. Dressler, V. P. Gadde, M. Hekmat, E. Ho, C. Huang, P. Le, Mahabaleshwara, C. Madden, N. K. Mishra, L. Raghavan, K. Saito, R. Schmitt, D. Secker, X. Shi, S. Fazeel, G. S. Srinivas, S. Zhang, C. Tran, A. Vaidyanath, K. Vyas, M. Jain, K. Y. K. Chang, and X. Yuan. A tri-modal 20-gbps/link differential/ddr3/gddr5 memory interface. *IEEE Journal of Solid-State Circuits*, 47(4):926–937, April 2012. ISSN 0018-9200. doi: 10.1109/JSSC.2012.2185370.

[8] A. Amirkhany, K. Kaviani, A. Abbasfar, S. Fazeel, W. Beyene, C. Hoshino, C. Madden, K. Chang, and C. Yuan. A 4.1-pj/b, 16-gb/s coded differential bidirectional parallel electrical link. *IEEE Journal of Solid-State Circuits*, 47(12):3208–3219, Dec 2012. ISSN 0018-9200. doi: 10.1109/JSSC.2012.2216413.

[9] M. Mansuri, J. E. Jaussi, J. T. Kennedy, T. C. Hsueh, S. Shekhar, G. Balamurugan, F. O'Mahony, C. Roberts, R. Mooney, and B. Casper. A scalable 0.128-to-1tb/s 0.8-to-2.6pj/b 64-lane parallel i/o in 32nm cmos. In *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pages 402–403, Feb 2013. doi: 10.1109/ISSCC.2013.6487788.

[10] T. O. Dickson, Y. Liu, A. Agrawal, J. F. Bulzacchelli, H. Ainspan, Z. Toprak-Deniz, B. D. Parker, M. Meghelli, and D. J. Friedman. A 1.8-pj/bit 16 x00d7;16-gb/s source synchronous parallel interface in 32nm soi cmos with receiver redundancy for link recalibration. In *2015 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–4, Sept 2015. doi: 10.1109/CICC.2015.7338371.

[11] C. H. Lee, M. T. Mustaffa, and K. H. Chan. Comparison of receiver equalization using first-order and second-order continuous-time linear equalizer in 45 nm process technology. In *2012 4th International Conference on Intelligent and Advanced Systems (ICIAS2012)*, volume 2, pages 795–800, June 2012. doi: 10.1109/ICIAS.2012.6306122.

[12] Y. Choi and Y. B. Kim. A 10-gb/s receiver with a continuous-time linear equalizer and 1-tap decision-feedback equalizer. In *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 1–4, Aug 2015. doi: 10.1109/MWSCAS.2015.7282072.

[13] S. Gondi and B. Razavi. Equalization and clock and data recovery techniques for 10-gb/s cmos serial-link receivers. *IEEE Journal of Solid-State Circuits*, 42(9): 1999–2011, Sept 2007. ISSN 0018-9200. doi: 10.1109/JSSC.2007.903076.

[14] C. Gimeno, E. Guerrero, C. Snchez-Azqueta, G. Royo, C. Aldea, and S. Celma. 1-v continuous-time linear equalizer for up to 2 gb/s over 50-m si-pof. In *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1818–1821, May 2015. doi: 10.1109/ISCAS.2015.7169009.

[15] J. B. Preibisch, T. Reuschel, K. Scharff, and C. Schuster. Impact of continuous time linear equalizer variability on eye opening of high-speed links. In *2016 IEEE 20th Workshop on Signal and Power Integrity (SPI)*, pages 1–4, May 2016. doi: 10.1109/SaPIW.2016.7496287.

[16] X. Y. Wang, L. Yu, and L. Wang. A compact high-accuracy rail-to-rail cmos operational amplifier. In *2010 4th International Conference on Bioinformatics and Biomedical Engineering*, pages 1–4, June 2010. doi: 10.1109/ICBBE.2010.5516532.

[17] S. P. G A V and A. K. Saini. A self biased operational amplifier at ultra low power supply voltage. In *2009 16th IEEE International Conference on Electronics, Circuits and Systems - (ICECS 2009)*, pages 152–154, Dec 2009. doi: 10.1109/ICECS.2009.5410958.

[18] L. L. Malavolta, R. L. Moreno, and T. C. Pimenta. A self-biased operational amplifier of constant gm for 1.5 v rail-to-rail operation in 130nm cmos. In *2016 28th International Conference on Microelectronics (ICM)*, pages 45–48, Dec 2016. doi: 10.1109/ICM.2016.7847904.

[19] J. F. Duque-Carrillo, J. M. Carrillo, J. L. Ausin, G. Torelli, and E. Sanchez-Sinencio. Transistor inversion level independent circuit technique for low-voltage rail-to-rail amplifiers. *IEE Proceedings - Circuits, Devices and Systems*, 151(6):565–571, Dec 2004. ISSN 1350-2409. doi: 10.1049/ip-cds:20040136.

[20] R. Hogervorst, J. P. Tero, and J. H. Huijsing. Compact cmos constant-gm rail-to-rail input stages with gm-control by an electronic zener diode. In *Solid-State Circuits Conference, 1995. ESSCIRC '95. Twenty-first European*, pages 78–81, Sept 1995.

[21] M. Bazes. Two novel fully complementary self-biased cmos differential amplifiers. *IEEE Journal of Solid-State Circuits*, 26(2):165–168, Feb 1991. ISSN 0018-9200. doi: 10.1109/4.68134.

[22] S. Rambabu, A. Majumder, and A. J. Mondai. A 90nm gain enhanced modified cascode ota structure with positive feedback. In *2017 2nd International Conference on Communication and Electronics Systems (ICCES)*, pages 203–207, Oct 2017. doi: 10.1109/CESYS.2017.8321266.

[23] Y. Wang, X. Zhao, Q. Zhang, and X. Lv. Adjustably transconductance enhanced bulk-driven ota with the cmos technologies scaling. *Electronics Letters*, 54(5):276–278, 2018. ISSN 0013-5194. doi: 10.1049/el.2017.4435.

[24] E. D. Manolov. Design of cascode current mirror ota in ultra-deep submicron cmos technology. In *2017 XXVI International Scientific Conference Electronics (ET)*, pages 1–4, Sept 2017. doi: 10.1109/ET.2017.8124365.

[25] A. D. Grasso, D. Marano, G. Palumbo, and S. Pennisi. High-performance three-stage single-miller cmos ota with no upper limit of cl. *IEEE Transactions on Circuits and Systems II: Express Briefs*, pages 1–1, 2017. ISSN 1549-7747. doi: 10.1109/TCSII.2017.2756923.

[26] S. Mahdavi, M. Jafarzadeh, M. Poreh, and S. Ataei. An ultra high-resolution low propagation delay time and low power with 1.25gs/s cmos dynamic latched comparator for high-speed sar adcs in 180nm technology. In *2017 IEEE 4th International Conference on Knowledge-Based Engineering and Innovation (KBEI)*, pages 0260–0265, Dec 2017. doi: 10.1109/KBEI.2017.8324983.

[27] R. Jain, A. K. Dubey, V. Varshney, and R. K. Nagaria. Design of low-power high-speed double-tail dynamic cmos comparator using novel latch structure. In *2017 4th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON)*, pages 217–222, Oct 2017. doi: 10.1109/UPCON.2017.8251050.

[28] A. Purushothaman. Analysis of regeneration time constant of dynamic latch using adomian decomposition method. In *2016 20th International Symposium on VLSI Design and Test (VDAT)*, pages 1–6, May 2016. doi: 10.1109/ISVDAT.2016.8064860.

[29] Y. G. Chen, H. W. Tsao, and C. S. Hwang. A fast-locking all-digital deskew buffer with duty-cycle correction. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 21(2):270–280, Feb 2013. ISSN 1063-8210. doi: 10.1109/TVLSI.2011.2182216.

[30] R. J. Yang and S. I. Liu. A 2.5 ghz all-digital delay-locked loop in 0.13 956;m cmos technology. *IEEE Journal of Solid-State Circuits*, 42(11):2338–2347, Nov 2007. ISSN 0018-9200. doi: 10.1109/JSSC.2007.906183.

[31] C. C. Chung, D. Sheng, and S. E. Shen. High-resolution all-digital duty-cycle corrector in 65-nm cmos technology. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 22(5):1096–1105, May 2014. ISSN 1063-8210. doi: 10.1109/TVLSI.2013.2260186.

[32] C. C. Chung, D. Sheng, and C. J. Li. A wide-range low-cost all-digital duty-cycle corrector. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 23 (11):2487–2496, Nov 2015. ISSN 1063-8210. doi: 10.1109/TVLSI.2014.2370631.

[33] Y. Feng, Q. Fan, Y. Tang, Z. Zuo, and J. Chen. A radiation-tolerant dll with fine resolution and duty cycle corrector for memory interface. In *2016 IEEE Dallas Circuits and Systems Conference (DCAS)*, pages 1–5, Oct 2016. doi: 10.1109/DCAS.2016.7791129.

A Voltage Controlled Oscillator Using IGZO Thin-Film Transistors

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***Abstract*—This paper presents a voltage controlled oscillator (VCO) using amorphous Indium Gallium Zinc Oxide (a-IGZO) thin-film transistors (TFTs). This circuit consists of a high-gain OpAmp, a comparator and a relaxation oscillator. The implemented relaxation oscillator shows a power consumption of 700 μW, when it is simulated with a supply rails of $\pm$5 V. It shows a frequency of oscillation range from 327 to 560 Hz, when the tuning capacitance value is in varying from 1.6 to 5 pF. On the other hand, the VCO has a power dissipation of 1.3 mW with frequency ranging from 400 to 556 Hz with a controlling voltage from -5 to 5 V. In-house oxide TFT model is used for circuit simulations in Cadence environment. This circuit would find potential applications in large-area flexible systems, namely smart packaging, biomedical and wearable systems, which needs clocks with different frequencies.**

***Keywords*—Voltage Controlled Oscillator, Relaxation Oscillator, a-IGZO TFTs, comparator with oxide TFTs, positive feedback operational amplifier.**

I. Introduction

Amorphous Indium Gallium Zinc Oxide (a-IGZO) thin-film transistors (TFTs) are gaining significant interest in various real-world applications including smart packaging, biomedical and wearable systems due to their low-temperature fabrication [1], relative high mobility ($>10cm^2$/V.s) and the stability compared to the other competing low-temperature TFT technologies (a-Si:H and organic TFTs). However, these technologies impose challenges in circuit design due to the absence of a stable complementary device.

In order to ensure compact flexible systems, all the circuits need to be on-chip to eliminate external interface problems. On-chip clock generator is one of the important functional block with frequency of oscillation tuning ability. Though many ring oscillators were reported with IGZO TFTs, they have the limitation of inferior swing, very high supply voltages ($\geq$ 15 V) and a single frequency of oscillation [2], [3], [4], [5]. Nevertheless, a ring oscillator with almost full swing is reported with bootstrapping load, this circuit is also limited to a single frequency of oscillation [6].

In order to address the above mentioned challenges, this work proposes a voltage controlled oscillator (VCO) using IGZO TFTs that contains an OpAmp, a comparator and a relaxation oscillator. Since there is an absence of stable and reproducible p-type oxide TFT, CMOS design techniques cannot be adapted directly, and all desired circuit blocks are to be designed only with n-type transistors, which makes designing high performance circuits quite challenging. As a first step, an OpAmp and a comparator are designed and characterized. Then the relaxation oscillator and VCO are implemented and simulated using an in-house oxide TFT model [7] in Cadence environment. It should be noted that the model is capable of predicting the circuit behavior very close to the measured response, when the circuit is fabricated under same conditions as the TFTs, whose data was used for model development [7].

The rest of the paper is organised as follows. Section II demonstrates the proposed circuit design and its operating principle. Section III presents the simulation results and discussions and finally the conclusions are drawn in section IV.

II. Circuit Description

The VCO has been implemented as shown in Fig.1 [8]. It is comprised of a relaxation oscillator, which is implemented with comparator and an OpAmp. The design of all these circuits with only n-type oxide TFTs are explained as follows.

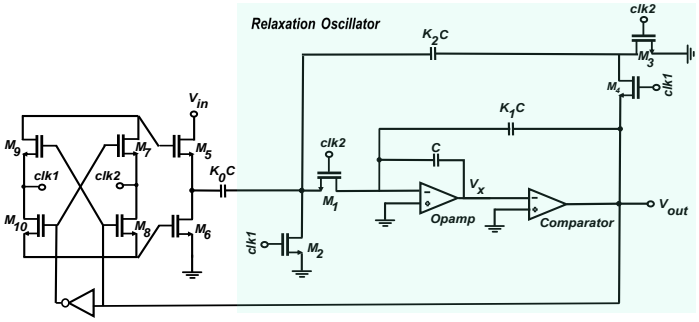

Fig. 1. Circuit diagram of voltage controlled oscillator.

Operational Amplifier: It is an important functional block in the relaxation oscillator circuit and it plays a vital role in minimizing stringent requirements of the comparator design presented in Fig. 1. Circuit schematic of the OpAmp is shown in Fig. 2, where the differential pair formed by transistors M_1-M_4 form a positive feedback loop. The loop gain is A_f as shown in (1). It can be observed that this gain depends on aspect ratios of the transistors forming positive feedback. The aspect ratios of transistors are carefully selected to get the loop gain close to unity. When $A_f \geq 1$, the OpAmp can become

unstable [9]. The transistors M_{11} to M_{14} form a differential to single ended converter, which is followed by a common-drain stage.

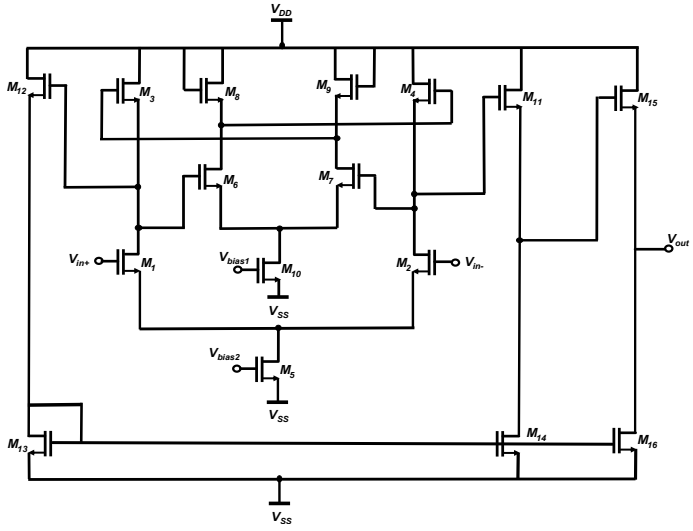

Fig. 2. Circuit diagram of operational amplifier with positive feedback

$$|A_f| = g_{m7}(\frac{1}{g_{m9}||r_{o7}||r_{o9}}) = \frac{g_{m7}}{g_{m9}} \quad (1)$$

The gain of the differential to single ended conversion stage is given by,

$$A_S = g_{m11}(\frac{1}{g_{m11}||r_{o14}||r_{o11}}) \quad (2)$$

and the overall gain of the Opamp is given by,

$$A_v = g_{m1}(\frac{1}{g_{m9}(1-A_f)||r_{o1}||r_{o3}})g_{m11}(\frac{1}{g_{m11}||r_{o11}||r_{o14}}) \approx g_{m1}r_{o1}||r_{o3} \quad (3)$$

Comparator: The architecture of the proposed comparator is shown in Fig.3. In order to ensure faster response, and get rid of clock feed-through and kickback noise, the proposed comparator consists of three preamplification stages and a static latch. Each preamplifier consists of a differential pair with positive feedback as shown in Fig.3a. This stage can ensure high-gain due to the positive feedback even with only n-type transistors, as explained in OpAmp design. A cascade of three such stages relax comparator and latch requirements. A regenerative latch together with preamplification stages can ensure faster response.

A latch is a positive feedback regenerative circuit with cross coupled TFTs as shown in Fig.3b. Its output is a growing exponential function of the differential input as per (4). The outputs of the third preamplification stage are applied as input to the latch. Based on the relative magnitude of these signals and threshold voltage of M_{11} and M_{12}, proper digital rails will be resulted at the output of the latch.

$$V_d(t) = V_d(0).e^{t(g_{m13}-\frac{1}{R_{11}})(\frac{1}{C_{11}})} \quad (4)$$

where V_d(t) is the difference between V_{in-} and V_{in+} of Fig.3b at time t, $V_d(0)$ is initial difference voltage, g_{m13} is transconductance of M_{13} and R_{11} and C_{11} are total resistance and capacitance seen at input of M_{11}.

Relaxation Oscillator: The relaxation oscillator circuit schematic is presented in Fig. 1, which has capacitors K_1C, K_2C and C along with switches, OpAmp and comparator. The switches are controlled by non-overlapping clocks, clk1 and clk2. To understand the working of the oscillator, assume V_{out} is at V_{SS}. A charge of K_2CV_{SS} is stored in capacitor K_2C when clk1 is high. This charge is transferred to capacitor C when clk1 is low and clk2 is high. This makes V_x negative by K_2V_{SS}. If this charge is sufficient enough to drive V_x below zero then the V_{out} is driven to V_{DD}. In the next on-time of clk1, the charge stored on capacitor K_2C is K_2C (V_{SS} + V_{DD}) makes the charge more positive and thus V_x becomes more negative. In the following cycles, the voltage at V_x keeps on charging to zero in the steps of K_2V_{DD}. The frequency of V_{out} is given by (5).

$$f = \frac{K_2}{K_1}\frac{f_{clk}}{2+\frac{V_{SS}}{V_{DD}}+\frac{V_{DD}}{V_{SS}}} \quad (5)$$

where f_{clk} is clock frequency of switching.

Voltage Controlled Oscillator: The relaxation oscillator was used to obtain a VCO as shown in Fig.1. The capacitor K_0C, a feed-in capacitor is controlled in such way that the positive V_{in} adds the charge to C with the same sign of K_2C making V_x reach zero earlier, thus increasing the frequency. With V_{in} the charge added to C has opposite polarity comapared to that of K_2C making V_x reach zero later leading to lower frequency. The frequency of VCO is calculated using (6).

$$f = (\frac{K_2}{4K_1})f_{clk} + V_{in}(\frac{K_0}{4K_1V_{DD}})f_{clk} \quad (6)$$

where V_{in} is voltage that contorls the oscillation of the circuit.

III. Results and Discussion

Using inhouse oxide TFT model the OpAmp, the Comparator, the Relaxation Oscillator and the Voltage Controlled Oscillator have been designed and simulated in Cadence environment with a power supply rails of $\pm$5 V.

The performance of the OpAmp: When the positive feedback operational amplifier shown in Fig. 2 is simulated, it is showing a gain of 61.7 dB. It is stable with a phase margin of 72^0, power consumption of 200 μW and has a unity gain bandwdith of 158 kHz as shown in Fig.4.

The performance of the Comparator: As stated before, the comparator in the work has three preamp stgaes and a latch as shown in Fig. 3. Whereas, Fig.5 shows the gain and phase response of a single-stage preamplifier with a gain of 10 dB and phase margin of 68^o. Fig.6 shows the output response of comparator having a swing of 4.32 to -4.21. Other performance metrics of the comparator are shown in Table I.

The performance of Relaxation Oscillator: The output V_{out} and the intermediate voltage level V_x has been shown in Fig.7. In this response, the output is obtained for a clock

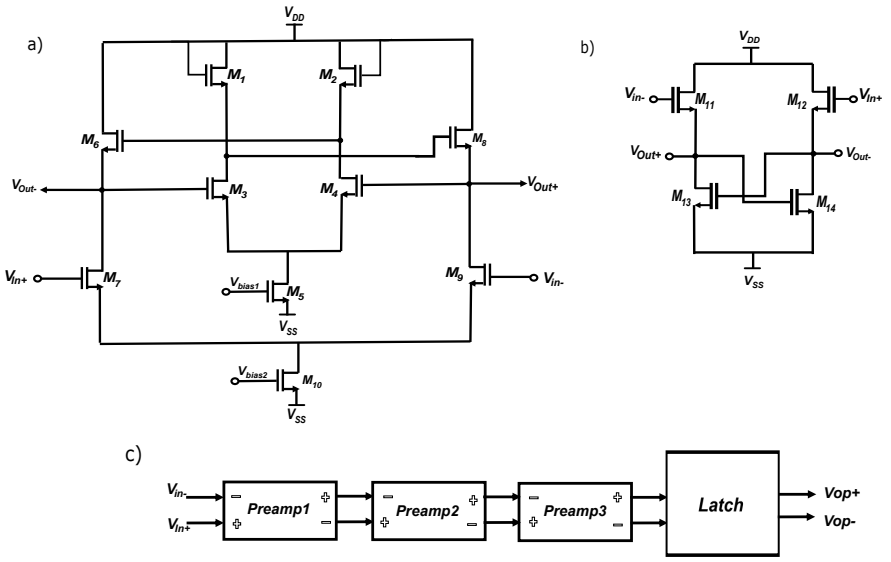

Fig. 3. Circuit diagram of a comparator: a) Preamplifier b) Latch c) Complete Comparator

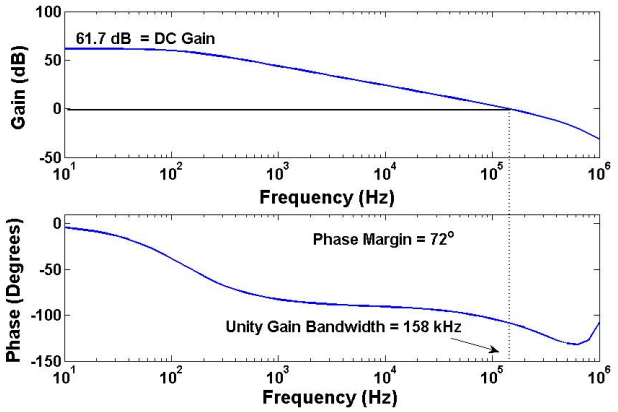

Fig. 4. Response of operational amplifier showing gain and phase plots

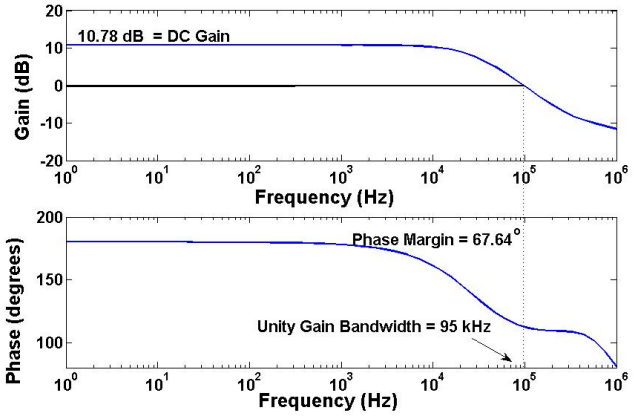

Fig. 5. Response of single stage preamplifier showing gain and phase plots

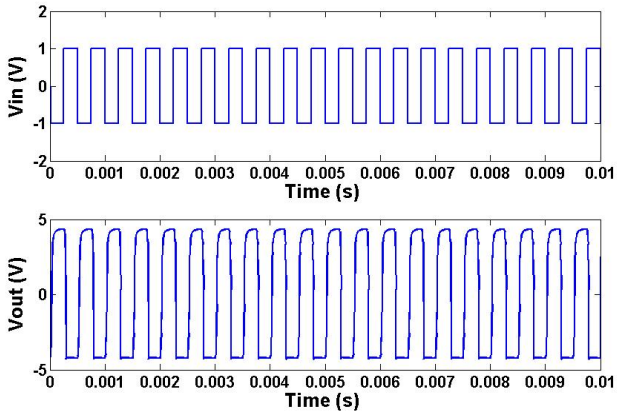

Fig. 6. Output of comparator showing input and output voltages

TABLE I. CALCULATED PARAMETERS OF COMPARATOR

S.NO.	PARAMETERS	VALUES
1.	Systematic offset	60 mV
2.	Slope	22 V/sec
3.	Resolution	50 mV
4.	Power consumption	300 μW

frequency of 10 kHz. The charging and discharging of capacitor C in form of steps with sizes of K_2V_{DD} or K_2V_{SS} can be seen as the voltage V_x.

The relation between the oscillating frequency and capacitor K_2C is linear as shown in (5) from theoretical prediction. The simulated outcome is compared and validated with the expected value in Fig.8. The frequency increases from 327 to 560 Hz with the increase in K_2/K_1 value from 0.08 to 0.24 with K_2C varying from 1.6 to 5 pF and K_1C of 20 pF. There is a slight deviation from predicted frequency because of non-idealities of the opamap and comparator. The proposed

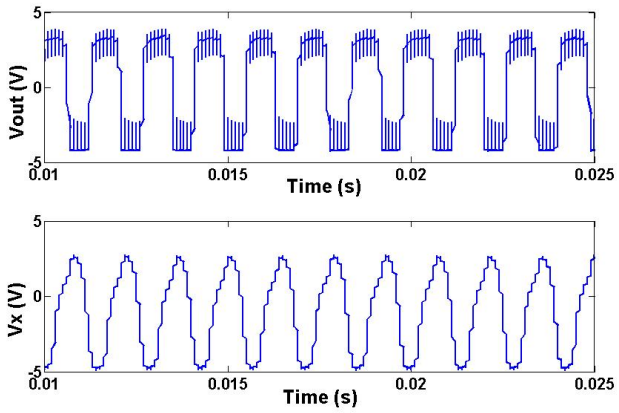

Fig. 7. Output response of relaxation oscillator

relaxation oscillator has a power consumption of 700 μW at 500 Hz. The ratio of clock frequency to oscillation frequency is around 20:1 ratio. With the suitable K_2/K_1 ratio the circuit can also work as frequency divider circuit.

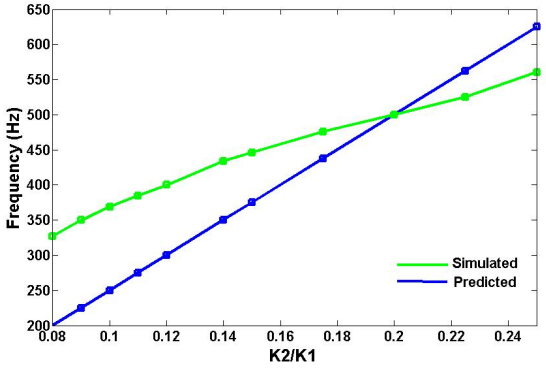

Fig. 8. Plot between the simulated and predicted values of the relaxation oscillator

The performance of the Voltage Controlled Oscillator: The VCO has a power consumption of 1.3 mW. The static power consumption can be reduced by using dynamic circuits. The variation of frequency has a slight deviation from the calculated values, as shown in Fig.9, due to non-idealities of the devices and circuits, such as, inferior gain and non-negligible output impedance of the Opamp due to poor transconductance (or poor mobility), and low resolution of the comparator. The linearity between the input voltage V_{in} of Fig.1 and the frequency of V_{out} is evident from the graph and is in agreement with (6).

It should be noted that the semiconductor is amorphous in nature and the field-effect mobility is around 10 $cm^2/V.s$. This device inferior performance lead to low frequency of oscillation. In addition, the architecture [8] is meant for low frequency, as circuit cannot function at higher frequencies due to phase jitter. Further improvement in the phase noise can be obtained by using design techniques consists of two comparators [10].

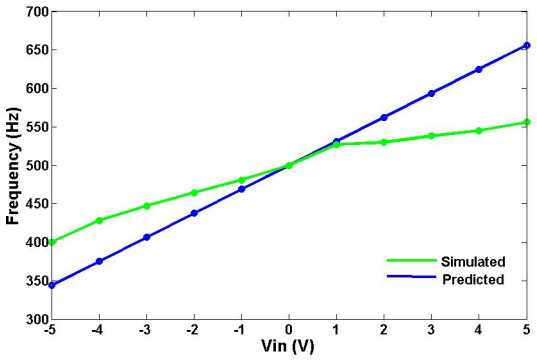

Fig. 9. Plot between the simulated and predicted values of VCO

IV. Conclusions

This paper presented a voltage controlled oscillator with IGZO TFTs for the first time, which is capable of generating variable frequencies by tuning the voltage. The circuit can be used as on-chip oscillator with frequency tuning ability or as frequency divider (refering to relaxation oscillator) in flexible large-area systems, such as, smart packaging, wearable electronics and biomedical applications.

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References

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.

[2] Y. Chen, D. Geng, M. Mativenga, H. Nam, and J. Jang, "High-speed pseudo-CMOS circuits using bulk accumulation a-IGZO TFTs," *IEEE Electron Device Letters*, vol. 36, no. 2, pp. 153–155, 2015.

[3] A. Suresh, P. Wellenius, V. Baliga, H. Luo, L. M. Lunardi, and J. F. Muth, "Fast all-transparent integrated circuits based on indium gallium zinc oxide thin-film transistors," *IEEE Electron Device Letters*, vol. 31, no. 4, pp. 317–319, 2010.

[4] D. Geng, D. H. Kang, and J. Jang, "High-performance amorphous indium–gallium–zinc–oxide thin-film transistor with a self-aligned etch stopper patterned by back-side uv exposure," *IEEE Electron Device Letters*, vol. 32, no. 6, pp. 758–760, 2011.

[5] M. Mativenga, M. H. Choi, J. W. Choi, and J. Jang, "Transparent flexible circuits based on amorphous-indium–gallium–zinc–oxide thin-film transistors," *IEEE Electron Device Letters*, vol. 32, no. 2, pp. 170–172, 2011.

[6] Y. Chen, D. Geng, T. Lin, M. Mativenga, and J. Jang, "Full-Swing Clock Generating Circuits on Plastic Using a-IGZO Dual-Gate TFTs With Pseudo-CMOS and Bootstrapping," *IEEE Electron Device Letters*, vol. 37, no. 7, pp. 882–885, 2016.

[7] P. Bahubalindrun, V. Tavares, P. Barquinha, P. G. De Oliveira, R. Martins, and E. Fortunato, "InGaZnO TFT behavioral model for IC design," *Analog Integrated Circuits and Signal Processing*, vol. 87, no. 1, pp. 73–80, 2016.

[8] K. Martin, "A voltage-controlled switched-capacitor relaxation oscillator," *IEEE Journal of Solid-State Circuits*, vol. 16, no. 4, pp. 412–414, 1981.

[9] Y.-C. Tarn, P.-C. Ku, H.-H. Hsieh, and L.-H. Lu, "An amorphous-silicon operational amplifier and its application to a 4-bit digital-to-analog converter," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 1028–1035, 2010.

[10] P. F. Geraedts, E. van Tuijl, E. A. Klumperink, G. J. Wienk, and B. Nauta, "A 90μW 12MHz Relaxation Oscillator with a-162dB FOM," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*. IEEE, 2008, pp. 348–618.