Improving the Retention Time of a Dopingless 1T DRAM using Gate Engineering

By

Nimish Agarwal

Under the Supervision of Dr. Sneh Saurabh

Indraprastha Institute of Information Technology Delhi

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Nimish Agarwal

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Certificate

This is to certify that the thesis titled **"Improving the Retention Time of a Dopingless 1T DRAM using Gate Engineering"** being submitted by **Nimish Agarwal** to the Indraprastha Institute of Information Technology Delhi, for the award of the *Master of Technology*, is an original research work carried out by him under my supervision. The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

July, 2019

Dr. Sneh Saurabh
Associate Professor
Department of Electronics & Communication Engineering
Indraprastha Institute of Information Technology Delhi
New Delhi, 110020

Abstract

In this thesis, a dopingless 1T DRAM with a high retention time is proposed. The high retention time is achieved by suppressing the diffusion current in the device which is responsible for degrading the "0" state. In the proposed device, a control gate with an appropriate workfunction is added in a region adjacent to the source. The control gate provides the necessary holes that suppress the diffusion current in the "0" state. As a result, 1/0 read current ratio also increases by 3 orders of magnitude. Furthermore, the write/hold/read bias conditions of the device and the array topology is designed such that the proposed DRAM cell can be integrated compactly. Additionally, it is demonstrated that the DRAM cell operates correctly under various disturb conditions.

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List of Abbreviation

DL-DRAM	Dopingless Dynamic Random Access Memory
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
TFET	Tunnel Field-Effect Transistor
BTBT	Band-to-Band Tunneling
RDF	Random Dopant Fluctuations
SM	Sense Margin
RT	Retention time

Chapter 1

Introduction

1.1 Motivation

As the technology is scaled down, there is a need to reduce DRAM size. In conventional 1T-1C DRAMs, capacitor is used as a storage element. However, scaling down capacitor has severe challenges. To overcome these challenges, 1T DRAM was proposed, which has built in storage. However, with scaling down of these 1T DRAMs, new challenges are posed in fabrication. One of them is random dopant fluctuations (RDF). To tackle this problem, recently dopingless DRAMs were proposed. However, these proposed devices have low retention time and designing an array of memories using these proposed devices is difficult. This work is motivated to solve these problems in dopingless 1T DRAM cells.

1.2 Literature survey

With the increase in demand of the large-capacity memories at low cost, dynamic random access memory (DRAM) plays an important role in semiconductor industry. Conventionally, 1T-1C DRAMs have been used for data storage consisting of one transistor and one capacitor. As the technology continued to shrink down with time, a big challenge faced by manufacturers is to shrink the area of basic memory cell. The major problem is scaling down the capacitor, for which complicated structures are used to have sufficient storage [2]. Consequently, capacitor-less single-transistor 1T DRAMs have been proposed containing the built-in storage mechanism. Such 1T DRAM has less area without the

need of fabrication of integrated capacitor as compared to 1T-1C DRAM. Initially, MOSFETs utilizing body charging effects and capacitance of floating body have been offered to form the 1T DRAM [3]. Then, several 1T DRAMs have been evolved with time in order to meet the technology requirements such as Single-Transistor Charge-Trap DRAM (1T CT DRAM) and silicon-with-partially-insulating-layer-on-silicon-on-insulator (SISOI) 1T DRAM [4, 5].

Further reducing gate lengths in 1T DRAM brings certain design and fabrication challenges [6]. One of the major obstructions in device scaling has been due to random dopant fluctuations (RDF) which is defined as variation in the position and number of dopants in the source, channel, and drain regions of a transistor [7, 8].

Recently, a dopingless 1T DRAM having Schottky contact to source/drain regions along with a raised body has been proposed in which thermionic emissions have been used for the generation of holes and electrons [9]. It requires a simpler fabrication methodology because there is no dopant implantation. However, it has a low retention time of 446 ms. Another dopingless 1T DRAM (DL-DRAM) has been proposed based on charge plasma concept [1]. It employs a misaligned double-gate architecture for storing the charge carriers. Similar to the above device it has got a low retention time of 70 ms. Furthermore, with the write/hold/read bias conditions at different terminals reported in [1, 9], it is challenging to design a memory array. These problems are addressed in this thesis, as explained in the following chapters.

Some of the terminologies which are used in this thesis are described below:

- **Read Time:** It is the time required to read a bit i.e. either “0” or “1”.
- **Write Time:** It denotes the time required to write a bit i.e. either “0” or “1”.
- **Current Ratio:** It is calculated as the ratio of read “1” current to read “0” current. It is a parameter that denotes read sensitivity [10].
- **Sense Margin:** It is given by the difference in read “0” and read “1” currents. For high read sensitivity, high sense margin is desired which enables the designing of simpler sensing circuits. Such circuits are used to differentiate the logic states i.e. whether the bit is “0” or “1”.
- **Retention Time:** It is defined as a value of hold time at which sense margin value becomes half of its original one.

1.3 Contribution of this work

The major contribution of this work are as follows:

1. A new design of dopingless DRAM is proposed. In the proposed device, control gate with a suitable workfunction is introduced. As a result, the retention time of the DRAM is considerably improved and the current ratio improved by 3 orders of magnitude.

2. The bias conditions for write/hold/read operations at different terminals are chosen such that the memory array can be designed in a compact manner.

3. It is demonstrated using simulations that the proposed device operates correctly under various disturb conditions.

1.4 Thesis Organization

The thesis is organized as follows:

- **Chapter 2: Device Proposed**
  This chapter proposes a new dopingless DRAM with a control gate such that the retention time is appreciably improved.

- **Chapter 3: Memory Array Design**
  This chapter describes the array design of DRAM implemented using proposed device and investigates various disturb conditions.

- **Chapter 4: Conclusion**
  This chapter concludes the whole thesis and discusses scope for future work.

Chapter 2

Device Proposed

2.1 Device structure and simulation models

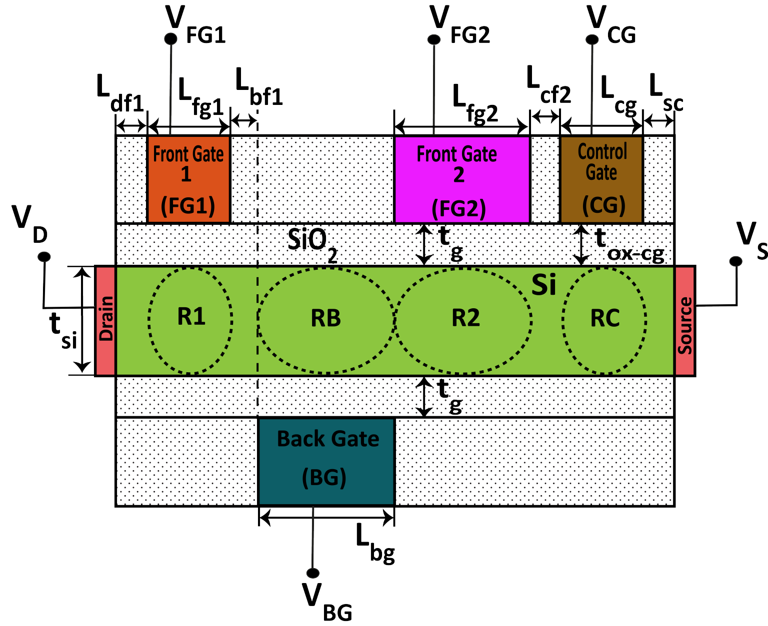

Figure 2.1: Cross-sectional view of the proposed device

The proposed device is shown in Fig. 2.1, with all the device parameters are mentioned in Table 2.1. It has a thin film of intrinsic silicon. The thickness of silicon film t_{si} is smaller than the limit of Debye Length i.e. $L_D = \sqrt{\epsilon V_t / qN}$, where V_t denotes the thermal voltage,

ϵ denotes the dielectric constant of silicon, and N represents carrier concentration in the silicon body [11].

Table 2.1: Device parameters used in simulation of proposed device

Parameter	Value
Silicon film thickness (t_{si})	10 nm
Gate oxide thickness (t_g)	3 nm
control gate oxide thickness (t_{ox-cg})	3 nm
Back-gate/Front-gate1 length (L_{bg}/L_{fg2})	100 nm
Front-gate2 workfunction (ϕ_{fg2})	4.17 eV
Back-gate workfunction (ϕ_{bg})	5.25 eV
Gap between front-gate2 and control-gate (L_{cf2})	15 nm
Gap between back-gate and front-gate1 (L_{bf1})	10 nm
Gap between drain and front-gate1 (L_{df1})	10 nm
Gap between source and control-gate (L_{sc})	10 nm
Front-gate1 workfunction (ϕ_{fg1})	3.9 eV
Control-gate workfunction (ϕ_{fcg})	5.93 eV
Front-gate1/Control-gate Length (L_{fg1}/L_{fcg})	50 nm

The proposed device uses two misaligned gates as used in [1], one at the bottom (back-gate), and other at top (frontgate2). The cross-sectional view of the misaligned gate structure of the dopingless DRAM proposed in [1] is shown in Fig. 2.2 with the device parameters mentioned in Table 2.2. For the proposed device, the workfunction of the control gate is taken as 5.93 eV and the workfunction of source is taken as 3.9 eV. The workfunction of 5.93 eV and 3.9 eV can be obtained by using Platinum and Hafnium, respectively [12]. The workfunction of backgate and frontgate2 are taken as 5.25 eV and 4.17 eV, respectively. These workfunctions can be achieved by p^+ poly and n^+ poly [13]. The workfunctions of source, drain and frontgate1 are taken as 3.9 eV. The workfunctions are chosen such that regions of required hole and electron concentrations are obtained in the intrinsic silicon. The regions with higher workfunction (RB and RC shown in Fig. 2.1) are hole-rich, while regions with lower workfunction (R1 and R2 shown in Fig. 2.1) are electron-rich.

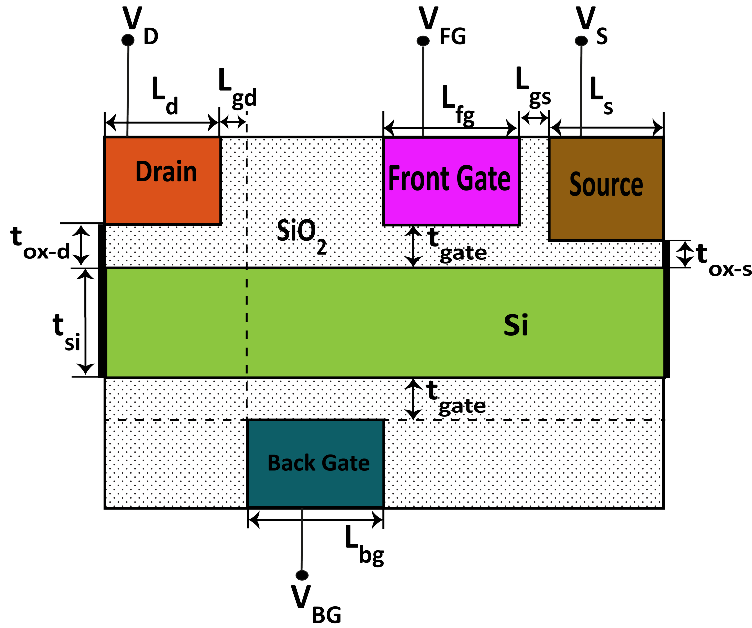

Figure 2.2: Cross-sectional view of the dopingless DRAM proposed in [1]

Table 2.2: Device parameters used in simulation of dopingless DRAM proposed in [1]

Parameter	**Value**
Silicon film thickness (t_{si})	10 nm
Gate oxide thickness (t_{gate})	3 nm
Back-gate/Front-gate length (L_{bg}/L_{fg})	100 nm
Front-gate workfunction (ϕ_{fg})	4.17 eV
Back-gate workfunction (ϕ_{bg})	5.25 eV
Drain–substrate oxide thickness (t_{ox-d})	3 nm
Source–substrate oxide thickness (t_{ox-s})	0.5 nm
Gap between front-gate and source (L_{gs})	15 nm
Gap between back-gate and drain (L_{gd})	10 nm
Drain workfunction (ϕ_d)	3.9 eV
Source workfunction (ϕ_s)	3.9-5.93 eV
Source/Drain Length (L_s/L_d)	50 nm

All the simulations in this work are performed using Silvaco ATLAS version 5.22.1.R. This tool is used in two-dimensional mode keeping width as 1 μm which is the default value [12]. Voltage boundary conditions are used at the contacts whose electrical characteristics are determined by their corresponding workfunctions [12,14]. Lombardi mobility

model is also included to estimate the variations in mobility occurred due to electric field and concentration. Non-local BTBT model is also integrated, which is responsible for tunneling phenomenon noted in various operation modes. A Shockley-Read Hall (SRH) recombination model is also used, which is dependent on concentration [14]. The tunneling model is calibrated by reproducing the results presented in [12] and also validated by simulation model using the results presented in [15].

2.2 Operating mechanism

The bias conditions for various operations at different terminals of the proposed device are shown in Table 2.3. The mechanism of writing and reading are described in the following paragraphs.

Table 2.3: Bias conditions at different terminals

Operation	V_{BG} **(V)**	V_D / V_{FG1} / V_{FG2}**(V)**	V_S/V_{CG} **(V)**
Write "0"	0	-1.1	0
Write "1"	-1.5	1.2	0
Read	1.5	1	0
Hold	-1	0	0

2.2.1 Write operation

The mechanism of writing "1" and "0" is explained below. The write time is taken as 50 ns in this work [1].

Write “1”:

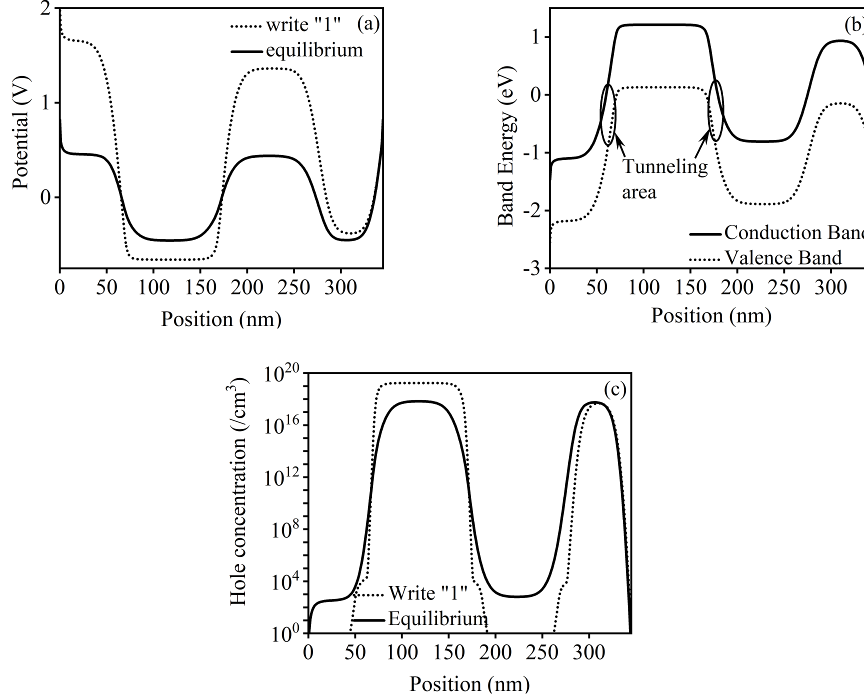

Figure 2.3: Write “1” operation (a) Potential profile at equilibrium and write “1”. Potential well is formed by write “1” operation (b) Conduction and Valance band aligned on both sides of RB region to allow BTBT during write “1” operation (c) Hole concentration in equilibrium and after write “1” operation.

The write “1” is performed by applying V_D = 1.2 V, V_{FG1} = 1.2 V, V_{FG2} = 1.2 V, V_{BG} = -1.5 V, V_{CG} = 0 V, and V_S = 0 V. The negative potential at the backgate and the positive potential at the drain and the frontgates (FG1 and FG2) result in a potential well in RB region enclosed by the two reverse-biased junctions on both the sides, as shown in Fig. 2.3(a). Due to sharp bending of the conduction band and valance band as shown in Fig. 2.3(b), there is an overlap in the energy bands resulting in BTBT. The BTBT causes tunneling of electrons out of the potential well to the drain and the frontgate (FG1 and FG2) regions and accumulation of the holes inside the potential well. The hole concentration increases from $5.6\times10^{17}/cm^3$ to $1.68\times10^{19}/cm^3$ (concentration taken 1nm above the backgate in silicon), after write “1” cycle as shown in Fig. 2.3(c). There is also an increase in the electron concentration in the region RC because of the expelled out electrons from the region R1.

Write "0":

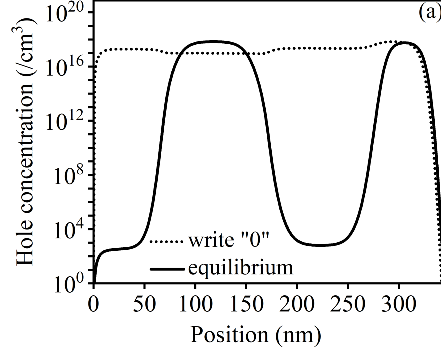

Figure 2.4: Hole concentration in equilibrium and after write "0"

Write "0" is done by applying V_D = -1.1 V, V_{BG} = 0 V, V_{FG1} = -1.1 V, V_{FG2} = -1.1 V, V_{CG} = 0 V, and V_S = 0 V. The negative potential on the drain, FG1, and FG2 disperses holes from the backgate region to the drain, R1, and R2 regions. The hole concentration decreases from $5.6\times10^{17}/cm^3$ to $9.6\times10^{16}/cm^3$ (concentration is observed 1nm above the back gate in silicon) after write "0" cycle as shown in Fig. 2.4. Furthermore, the potential inside the region R1, RB, R2 and near the drain becomes almost the same. This results in the uniform distribution of holes across these regions.

2.2.2 Hold operation

Once the write operation is done, the device has a different hole and electron concentration after write "1" and after write "0". This concentration difference needs to be maintained as long as possible such that during read operation "0" and "1" can be differentiated. Once the hold bias is applied, state "1" (holes captured in region RB) starts to degrade to state "0" (holes escape out from the region RB). Similarly, the state "0" (hole removed from the region RB) starts to degrade to state "1" (concentration of holes start increasing in the region RB). The hold conditions are needed to be chosen such that the process of degradation becomes slow. The bias for hold, in this case, is taken to favor the retention of holes in the state "1". After hold of 175 s, the hole concentration in the state "1" decreases from $1.7\times10^{19}/cm^3$ to $1.4\times10^{19}/cm^3$, while the hole concentration in the state "0" increases from $9.6\times10^{16}/cm^3$ to $1.2\times10^{19}/cm^3$. Under this condition, the difference

between read “1” and read “0” current reduces to 94 μA (which is half of the orignal difference of 187 μA). Therefore, the retention time of the proposed device is taken as 175 s.

2.2.3 Read operation

Read operation is carried out by applying $V_D = 1$ V, $V_{FG1} = 1$ V, $V_{FG2} = 1$ V followed by $V_{BG} = 1.5$ V. The voltage at the other terminals V_{CG} and V_S are kept at ground. The read time is taken $50ns$ [1]. The device behaviour under read “1” and read “0” are described below.

Read “1”:

In the read operation the voltages V_D, V_{FG1}, V_{FG2} are changed to 1 V. As a result there is negligible change in the electron and hole concentration in the device that was established after writing. Thereafter, a positive backgate voltage of 1.5 V is applied. The positive voltage at the drain, FG1, and backgate pushes holes (which are in high concentration in the region RB) towards the source. The hole concentration in the region RC (which is below the control gate) is low enough to allow the diffusion of holes from the region RB (above backgate). The diffusion current is the major component of read “1” current. The excess holes coming from the RB region increase recombination rate and moves recombination center towards the source where the electron concentration is $9.5\times10^{19}/cm^3$ (1 nm in silicon from source). The recombination rate after 50 ns of read operation is $1.7\times10^{25}/cm^3s$. The electrons are in high concentration near the source and R2 region, which drift/diffuse towards the drain and backgate region making the electrons redistribute all over the device.

Read “0”:

In the read “0” operation, voltages V_D, V_{FG1}, V_{FG2} are changed to 1 V. The region RB (above the backgate) has less hole concentration after write “0” compared to write “1”. Therefore, when the positive backgate voltage is applied, there is less diffusion of holes from the region RB towards the drain, R1, and R2 regions. During read “0”, the comparable hole concentrations in the region RC and the region RB leads to negligible diffusion of

holes towards the source. This keeps the transistor in the OFF condition during read "0". A very small current flows due to the recombination of holes and electrons between the regions RB and R2 and band to band tunneling (BTBT) at the junction of regions R2 and RC. The recombination rate is very low ($9.5\times10^{19}/cm^3s$) after 50 ns of read operation.

2.3 Device characteristics

The most salient feature of the proposed device is the control gate. In this work, the impact of control gate on the device characteristics is investigated in detail.

2.3.1 Effect of workfunction

The performance of the proposed device is highly dominated by workfunction. The source and control gate workfunctions are chosen such that state "1" gives high read current, while the read current of state "0" is suppressed.

Source workfunction:

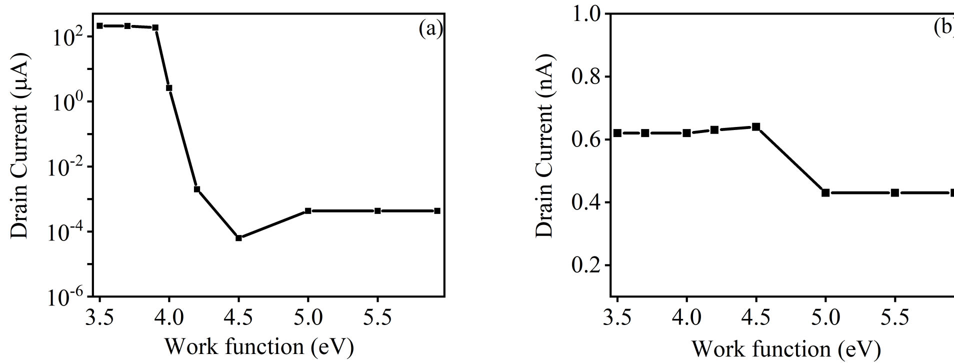

Figure 2.5: Effect of source workfunction is shown for (a) read "1" current and (b) read "0" current

Read "1": The source workfunction is varied from $3.5eV$ to $5.93eV$, as shown in Fig. 2.5(a). As the workfunction of the source is increased, the electron concentration starts to decrease and the hole concentration starts to increase between the region RC and the

source. The diffusion current (the major current component during read “1”) is actually due to very low concentration of holes in between the region RC and the source. As the workfunction increases, the hole concentration starts to increase near the source, which in turn starts degrading the diffusion current. This reduces the diffusion current drastically, as a result, the total read “1” current also decreases greatly. As the source workfunction is increased further, the hole concentration from the region RC to the source increases. As the region R2 has a high electron concentration, the band bending at the junction between the regions R2 and RC starts to increase and more BTBT occurs at the junction.

Read “0”: For the read “0” operation, there is negligible variation in the drain current with the change in the workfunction of the source, as shown in Fig 2.5(b). As the diffusion of holes is already negligible during read “0”, there is not much effect of change in the source workfunction.

Control gate workfunction:

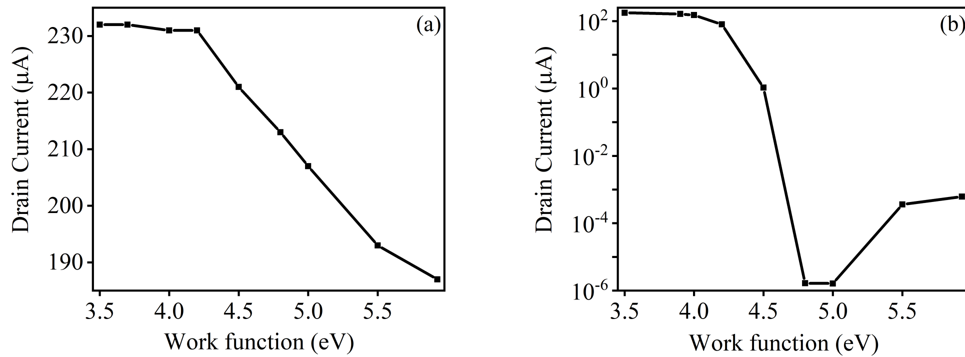

Figure 2.6: Effect of control gate workfunction is shown for (a) read “1” current and (b) read “0” current

Read “1”: In read “1”, as the workfunction of the control gate is increased there is almost continuous decrease in the drain current, as shown in Fig. 2.6(a). However, there is no change in the order of magnitude of the read “1” current. As the workfunction of the control gate increases, there is an increase in the hole concentration in the region RC. As a result the diffusion current is suppressed. However, this concentration is not high enough to suppress the drain current to a large extent.

Read “0”: Fig. 2.6(b) shows drain current variation with varying control gate workfunction for read “0”. In the state “0”, there is a low concentration of hole in the region RB. When the workfunction of the control gate is less then $4eV$, there is a high concentration of electrons and a low concentration holes from the region from R2 to the source. This helps in diffusion of holes towards the source to give diffusion current in micro amperes. As the workfunction is further increased upto $5eV$, the increase in hole concentration in the region RC suppresses the diffusion current. This decreases the drain current drastically. As the workfunction is increased further, there is more band bending at the junction of region R2 and RC, resulting in a small increase in current due to BTBT.

2.3.2 Effect of control gate voltage (V_{CG})

The control gate voltage(V_{CG}) is varied from -1.5 V to 1.5 V in the read operation while keeping all other voltages as mentioned before. The effect of V_{CG} for read “1” and read “0” is discussed below.

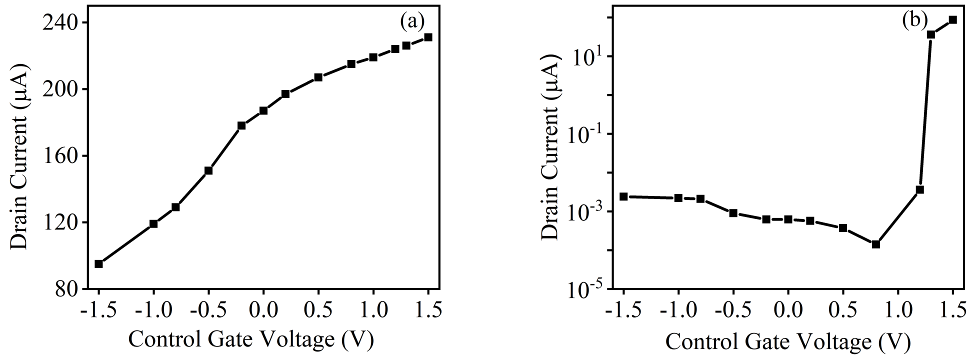

Figure 2.7: Effect of control gate voltage (V_{CG}) is shown for (a) read “1” current (b) read “0” current

Read “1”: Fig. 2.7(a) shows that as control gate voltage increases from -1.5 V to 1.5 V, the drain current also increases, but remains in same order of magnitude. The effect of negative voltage on the control gate is observed to be same as increasing the workfunction of the control gate. As the voltage of control gate becomes more negative, holes starts to accumulate in the region RC. This suppresses the diffusion current. Similarly, as the control gate voltage is changed towards positive voltage, more holes are expelled from the

region RC. As the hole concentration in the region RC decreases, the diffusion current increases.

Read "0": In read "0", when the control gate voltage is varied from -1.5 V to 1 V, there is a negligible change in the drain current. However, for voltage greater then 1 V, drain current starts to rise suddenly as shown in Fig. 2.7(b). This sudden rise is due to the applied high positive voltage removing accumulated holes and decreasing the hole concentration to such a level that it is no longer able to suppress the diffusion current.

2.4 Comparison with other dopingless 1T DRAMs

The comparison of the key figures of merit of the proposed device with the dopingless 1T DRAM proposed in literature is shown in Table 2.4. Clearly, the retention time has increased by order of magnitude.

Table 2.4: Comparison of figures of merit of dopingless DRAMs

S. No.	**Reference**	**Retention time**	**Sense margin**	**Current Ratio**
1	[9]	466 ms	28.7 μA	NA
2	[1]	70 ms	169 μA	3
3	This work	175 s	187 μA	10^3

Chapter 3

Memory Array Design

3.1 Device connections

Table 3.1: Bias during different operations at different terminals

Operation	V_{BG} **(V)**	V_D / V_{FG1} / V_{FG2}**(V)**	V_S/V_{CG} **(V)**
Write “0”	0	-1.1	0
Write “1”	-1.5	1.2	0
Read	1.5	1	0
Hold	-1	0	0

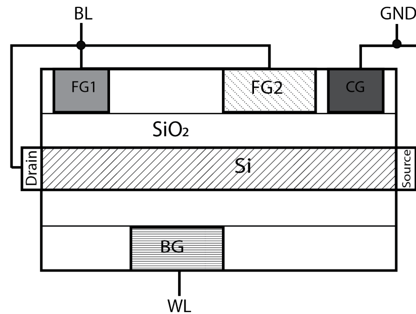

Figure 3.1: Device connections for memory array design (BL connected to the drain, FG1 and FG2. Back gate connected to WL. The source and CG are grounded.)

Bias during different operations at different terminals for the proposed device are given in Table 3.1. For the array design, the backgate terminal is connected to the word line (WL) and the drain, FG1, and FG2 are connected to the bit line (BL), as shown in Fig. 3.1. The source and CG are always grounded. Thus, the number of external connections required for connecting the proposed cell in an array reduces to three. It is worthy to point out that the number of external connections required for dopingless DRAMs proposed in [1] is four, as can be inferred from Table 3.2.

Table 3.2: Bias during different operations at different terminals for the device proposed in [1]

Operation	V_{FG}(V)	V_{BG}(V)	V_D(V)	V_S(V)
Write "0"	0	3	0	0
Write "1"	0	-3	0	0
Read	2	1.1	1	0
Hold	0	-0.8	0	0

Furthermore, designing an array with the bias scheme presented in [1] is challenging. From Table 3.2, it can be noted that the bias of only one terminal (V_{BG}) is varied for writing "1" and writing "0". This makes the selection of a particular cell in an array difficult, during the write operation.

A similar problem exits in the bias scheme used for dopingless DRAM in [9]. Though, the drain voltage during write "0" is not specified in [9], the problem exits if it is taken as 0 V or 1 V (these two are the possible voltages that can be used). In either case, we cannot select a particular cell that needs to be written by different values or are differentiated from the cells that are in hold mode.

For the proposed device the bias scheme are carefully chosen (as shown in table 3.1) to allow easy integration of cells in the form of an array. The write mechanism of the proposed device depends on the two voltage lines which allows a particular cell to be selected using BL and WL. The hold bias condition is selected such that it does not conflict with the read/write bias conditions.

3.2 Transient analysis

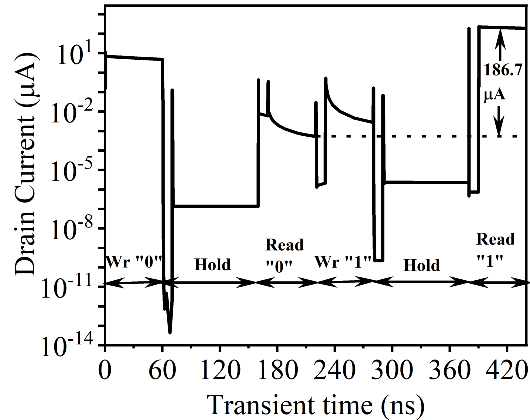

Figure 3.2: Transient analysis showing write/hold/read operations for "0" and "1" state

In a DRAM, bit is written into the memory cell, then the memory cell is taken to the hold state until the data needs to be read. To demonstrate this situation, transient analysis is done for these operations in the sequence of write, hold and read for both "0" and "1" states, as shown in Fig. 3.2. At first "0" is written, then it is held for $100ns$. After that, value is read from the cell and "1" is written on it. This "1" state is held for $100ns$, then read is performed again. The difference between the read "0" current and the read "1" current is found to be 186.7 μA. This demonstrates that the proposed memory cell can correctly perform write, hold and read operations in sequence.

3.3 Analysis under disturb conditions

While writing or reading a particular cell, stored data on other cells sharing the same WL or BL may also get affected. The change in the stored data due to this disturbance from "1" to "0" is called "0" disturb and from "0" to "1" is called "1" disturb [16]. The bias of the WL and the BL for the worst case disturb conditions are shown in Table 3.3.

Table 3.3: "0" and "1" worst disturb conditions

	"1" disturb		"0" Disturb		
Cell	A	B	C	D	E
V_{WL}(V)	-1	-1.5	-1	0	1.5
V_{BL}(V)	1.2	0	-1.1	0	0

3.3.1 "1" Disturb

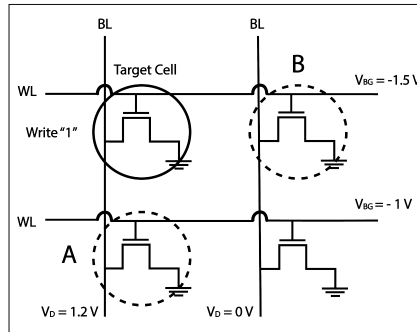

Figure 3.3: Write "1" on target cell creating "1" disturb condition for A and B cells

In Fig. 3.3, "0" is written on A and B cells and are in the hold state. Then write "1" operation is performed on the target cell, which can potentially disturb the stored "0" on A and B cells. After write "1" operation on the target cell, hold and read from A and B cells are done. Due to shared BL with the target cell, the drain, FG1 and FG2 voltages of A cell change from 0 V to 1.2 V. The effect of this change is that the read current rises to 8.6 nA as shown in the Fig. 3.4(a). This current is still very low as compared to the Read "1" current. The WL of B cell is also affected by the write "1" operation on the target cell, which changes the backgate voltage of B cell from -1 V to -1.5 V. This has negligible effect on the read "0" current and it remains close to 0.5 nA, as shown in Fig. 3.4(b). This demonstrates that there is no disturb "1" on the memory cells sharing BL and WL by the write and read operations.

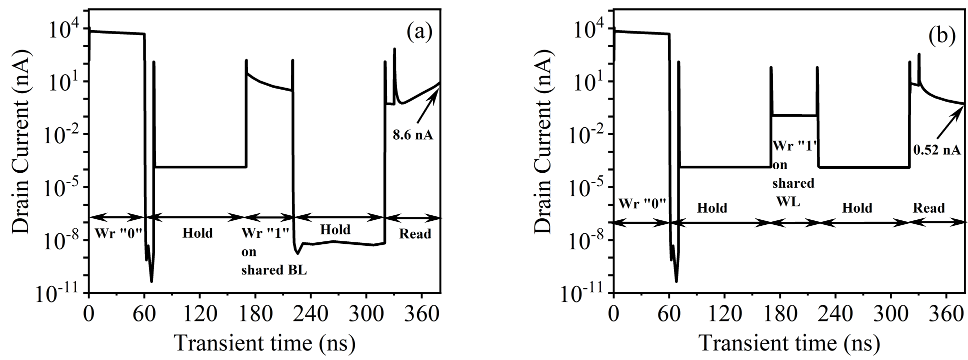

Figure 3.4: Conditions to check for “1” disturb

3.3.2 “0” disturb

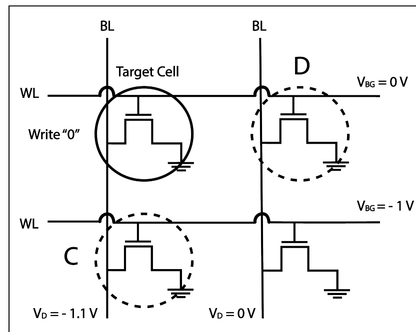

Figure 3.5: Write “0” on target cell creating “0” disturb condition for C and D cells

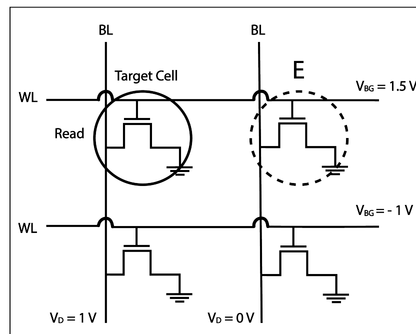

Figure 3.6: Read on target cell creating “0” disturb condition for E cell

Fig. 3.5 and Fig. 3.6 show the scenario for “0” disturb. In Fig. 3.5, write “1” operation is performed on C and D cells, followed by the hold operation. Then, “0” is written on

the target cell to create “0” disturb conditions for A and B cells. Then, read is done after hold from both the cells. For C cell, the BL voltage is changed from 0 V to -1.1 V at the time of write “1” operation on the target cell. In this condition, holes are lost and read “1” current is decreased to 174 μA, as shown in Fig. 3.7(a). Still the current is high enough to be considered as “1”. Fig. 3.7(b) shows the effect on D cell due to shared WL with target cell. Write “1” operation on the target cell changes the backgate voltage of D cell from -1 V to 0 V for time period of “1” write cycle (taken as 50 ns in this work). The read current of D cell is still 186 μA, which demonstrates that there is negligible impact of the disturbance.

Fig. 3.6 shows the effect on the E cell due to read operation on the target cell with shared WL. Backgate voltage is changed from -1 V to 1.5 V. This positive voltage expels the holes from the region RB. As a result, read current of E cell decreases to 156 μA, as shown in Fig 3.7(c). This demonstrates that even after read on the shared WL bits, the cells storing “1” will not have “0” disturb.

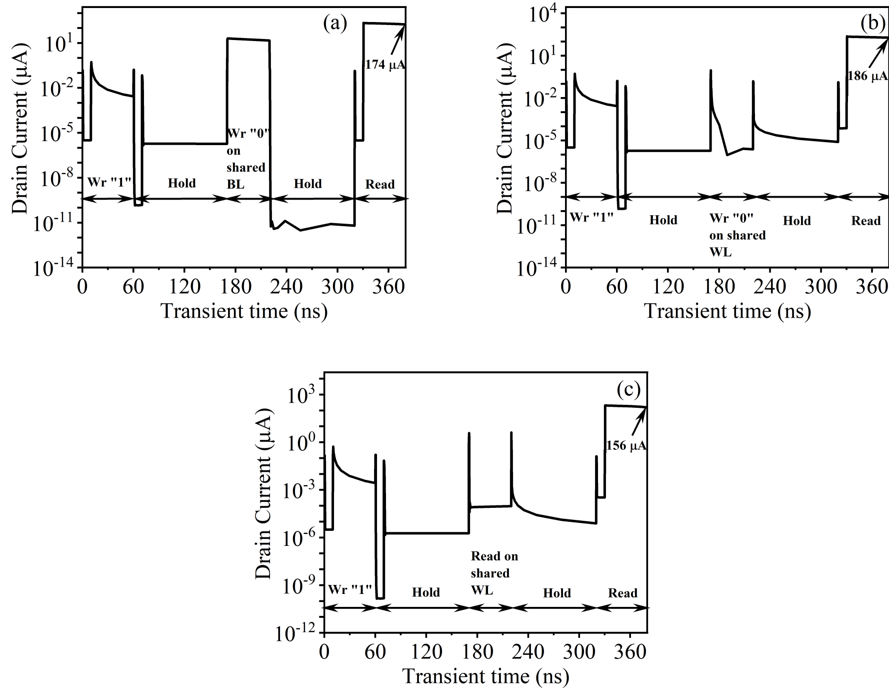

Figure 3.7: Conditions to check for “0” disturb

Chapter 4

Conclusion

4.1 Conclusion

In this work, using gate engineering, an improvement in the retention time of a dopingless 1T DRAM is demonstrated. The device mechanism is studied in detail and the impact of the control gate in improving the electrical characteristics is illustrated. Further, it has been explained how it can be integrated in an array and it has been shown using simulations that it can work as a memory cell. Simulations are done for various disturb conditions to ensure the proper working of device in an array. Future work includes the investigation in improving power consumption and density.

Moreover, dopingless DRAMs can be a solution to the problem of high temperature requirement for annealing process in fabrication of monolithic 3D IC. In IC fabrication, high temperature is required for annealing process to repair damage done by ion implantation [17]. As in some monolithic 3D IC fabrications, the memory is stacked above logic, high temperature to fabricate memory can effect the interconnects and components in logic layer. With the use of dopingless memories, problem of high temperature requirement can be eliminated. This aspect of dopingless DRAM can be investigated in future.

Appendix I

4.2 A1.Sample Input file for write "1" followed by read "1" operation

```
go internal
set Lsd=0.050
set Lgd=0.010
set Lg=0.200
set Lgs=0.015
set startx=0
set dstart=$"startx"
set dend=($"dstart"+$"Lsd"+$"Lgd")
set sstart=($"dend"+$"Lg")
set send=($"sstart"+$"Lsd"+$"Lgs")
set endx=$"send"
set L_back_gate=0.100
set L_front_gate=0.100
set gate_di_thick=0.003
#
set tsi=0.010
set tox=0.009
set starty=0
set endy=($"tsi"+$"tox")

go atlas
#mesh space.mult=1.0
```

```
mesh width=1
x.mesh loc=$"startx"  spac=0.001
x.mesh loc=(($"startx"+$"dend")/2)  spac=0.002
x.mesh loc=($"dend"-$"Lgd") spac=0.001
x.mesh loc=$"dend"  spac=0.001
x.mesh loc=($"dend"+(($"sstart"-$"dend")/2))  spac=0.001
x.mesh loc=$"sstart"  spac=0.001
x.mesh loc=($"sstart"+$"Lgs")  spac=0.001
x.mesh loc=(($"sstart"+$"endx")/2)   spac=0.002
x.mesh loc=$"endx"  spac=0.001

y.mesh loc=($"starty"-$"tox")  spac=0.001
y.mesh loc=($"starty"-$"gate_di_thick")  spac=0.001
y.mesh loc=$"starty"  spac=0.001
y.mesh loc=(($"starty"+$"tsi")/2)    spac=0.0001
y.mesh loc=$"tsi"  spac=0.001
y.mesh loc=($"tsi"+$"gate_di_thick") spac=0.001
y.mesh loc=$"endy"  spac=0.01


region num=1  y.min=($"starty"-$"tox") y.max=$"starty"      material=sio2
region num=2  y.min=$"starty" y.max=$"tsi"       material=silicon
region num=3  y.min=$"tsi" y.max=($"tsi"+$"tox")       material=sio2

electrode name=drain  x.min=$"startx"   x.max=$"startx"  \
y.min=($"starty"-0.003) y.max=$"tsi"
electrode name=gated  x.min=$"startx"   x.max=($"dend"-$"Lgd") \
y.min=($"starty"-$"tox") y.max=($"starty"-0.003)
electrode name=fgate   x.min=($"dend"+$"L_front_gate") x.max=$"sstart" \
y.min=($"starty"-$"tox") y.max=($"starty"-0.003)
electrode name=gates x.min=($"sstart"+$"Lgs")  x.max=$"endx" \
y.min=($"starty"-$"tox")  y.max=($"starty"-0.003)
electrode name=gate x.min=$"dend" x.max=($"sstart"-$"L_front_gate") \
y.min=($"endy"-0.006) y.max=$"endy"
electrode name=source  x.min=$"endx"   x.max=$"endx"  \
```

```
y.min=$"starty" y.max=$"tsi"

qtregion number=1 pts.normal=100 pts.tunnel=((50+($"Lg"*100))*5)  x1=($"dend"-0.040)  \
 y1=$"starty" x2= ($"dend"-0.040)    y2=$"tsi" \
x3=($"dend"+0.025)      y3=$"tsi" x4=($"dend"+0.025)  y4=$"starty"

qtregion number=2 pts.normal=100 pts.tunnel=((50+($"Lg"*100))*5) \
 x1=($"dend"+($"L_back_gate"/2))   y1=$"starty" \
x2=($"dend"+($"L_back_gate"/2))    y2=$"tsi" \
x3=($"sstart"-($"L_front_gate"/2))    y3=$"tsi" x4=($"sstart"-($"L_front_gate"/2)) \
  y4=$"starty"

qtregion number=3 pts.normal=100 pts.tunnel=((50+($"Lg"*100))*5) \
 x1=($"sstart"-0.025) y1=$"starty" \
x2= ($"sstart"-0.025) y2=$"tsi" \
x3=($"sstart"+0.040)    y3=$"tsi" x4=($"sstart"+0.040)  y4=$"starty"

material material=silicon me.tunnel=0.14 mh.tunnel=0.14 region=2

material material=sio2 permittivity=3.9

contact name=fgate N.POLYSILICON common=drain
contact name=gate P.POLYSILICON
contact name=gated workf=3.9 common=drain
contact name=gates workf=5.93 common=source
contact name=drain workf=3.9
contact name=source workf=3.9

 models consrh cvt bbt.nonlocal qtunn.dir=1 bbt.forward print

output charge qfn qfp con.band val.band e.lines J.DRIFT J.DIFFUSION e.field traps
method newton
solve init
save outf=sindhu_dl_1_initial.str
## At equilibrium
```

```
solve vsource=0.0
solve vgate=0.0
solve vdrain=0.0
save outf=sindhu_dl_1_off.str

#write  1 operation
log outf=write_1.log


solve vdrain=1.2 ramptime=5E-10 tstop=10E-9 tstep=1e-10
output val.band con.band charge e.lines J.DRIFT J.DIFFUSION
save outf=consrhoff_read_one_after_0ns_transient_wf_3.9_lifetime_1e-7.str

solve vgate=-1.5 ramptime=5E-10 tstop=60E-9 tstep=1e-10

output val.band con.band charge e.lines J.DRIFT J.DIFFUSION
save outf=test_after_write_one.str

#Read 1 operation. Read taken after 50ns
log outf=consrhoff_wf_3.9_lifetime_1e-7.log

solve vdrain=1 tstop=70E-9 tstep=1e-10
output val.band con.band charge e.lines J.DRIFT J.DIFFUSION
save outf=consrhoff_read_one_after_10ns_transient_wf_3.9_lifetime_1e-7.str


solve vgate=1.5 ramptime=5E-10 tstop=70.5E-9 tstep=1e-10
output val.band con.band charge e.lines J.DRIFT J.DIFFUSION
save outf=consrhoff_read_one_after_10.5ns_transient_wf_3.9_lifetime_1e-7.str
solve vgate=1.5 tstop=71E-9 tstep=1e-10
output val.band con.band charge e.lines J.DRIFT J.DIFFUSION
save outf=consrhoff_read_one_after_11ns_transient_wf_3.9_lifetime_1e-7.str
solve vgate=1.5 tstop=75E-9 tstep=1e-10
output val.band con.band charge e.lines J.DRIFT J.DIFFUSION
save outf=consrhoff_read_one_after_15ns_transient_wf_3.9_lifetime_1e-7.str
```

```
solve vgate=1.5 tstop=100E-9 tstep=1e-10
output val.band con.band charge e.lines J.DRIFT J.DIFFUSION
save outf=consrhoff_read_one_after_40ns_transient_wf_3.9_lifetime_1e-7.str
solve vgate=1.5 tstop=110E-9 tstep=1e-10
output val.band con.band charge e.lines J.DRIFT J.DIFFUSION
save outf=consrhoff_read_one_after_50ns_transient_wf_3.9_lifetime_1e-7.str

solve vgate=1.5 tstop=120E-9 tstep=1e-10
output val.band con.band charge e.lines J.DRIFT J.DIFFUSION
save outf=consrhoff_read_one_after_60ns_transient_wf_3.9_lifetime_1e-7.str

quit
```

Bibliography

[1] A. James and S. Saurabh, “Dopingless 1T DRAM: Proposal, Design and Analysis,” *IEEE Access*, June 2019. doi: 10.1109/ACCESS.2019.2925525.

[2] N. Rodriguez, F. Gamiz, and S. Cristoloveanu, “A-ram memory cell: Concept and operation,” *IEEE Electron Device Letters*, vol. 31, pp. 972–974, Sep. 2010.

[3] S. Okhonin, M. Nagoga, J. Sallese, and P. Fazan, “A capacitor-less 1T-DRAM cell,” *IEEE Electron Device Letters*, vol. 23, pp. 85–87, Feb 2002. doi: 10.1109/55.981314.

[4] M. Gunhan Ertosun, K.-Y. Lim, C. Park, J. Oh, P. Kirsch, and K. C. Saraswat, “Novel Capacitorless Single-Transistor Charge-Trap DRAM (1T CT DRAM) Utilizing Electrons,” *IEEE Electron Device Letters*, vol. 31, pp. 405–407, May 2010. doi: 10.1109/LED.2010.2043634.

[5] W. Lee and W. Y. Choi, “A Novel Capacitorless 1T DRAM Cell for Data Retention Time Improvement,” *IEEE Transactions on Nanotechnology*, vol. 10, pp. 462–466, May 2011. doi: 10.1109/TNANO.2010.2046743.

[6] J. A. Mandelman, R. H. Dennard, G. B. Bronner, J. K. DeBrosse, R. Divakaruni, Y. Li, and C. J. Radens, “Challenges and future directions for the scaling of dynamic random-access memory (DRAM),” *IBM Journal of Research and Development*, vol. 46, pp. 187–212, March 2002. doi: 10.1147/rd.462.0187.

[7] Y. Li, C. H. Hwang, and T. Y. Li,, “Random-Dopant-Induced Variability in Nano-CMOS Devices and Digital Circuits,” *IEEE Transactions on Electron Devices*, vol. 56, pp. 1588–1597, August 2009. doi: 0.1109/TED.2009.2022692.

[8] R. Rao, N. DasGupta, and A. DasGupta, “Study of Random Dopant Fluctuation Effects in FD-SOI MOSFET Using Analytical Threshold Voltage Model,” *IEEE Trans-*

actions on Device and Materials Reliability, vol. 10, pp. 247–253, June 2010. doi: 10.1109/TDMR.2010.2044180.

[9] J.-T. Lin, W.-T. Sun, H.-H. Lin, Y.-J. Chen, N. Navlakha, and A. Kranti, "Raised Body Doping-less 1T-DRAM With Source/Drain Schottky Contact," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 276–281, January 2019. doi: 10.1109/JEDS.2019.2896412.

[10] Li Wei, Liu Hongxia, Wang Shulong, Chen Shupeng, and Wang Qianqiong, "The Programming Optimization of Capacitorless 1T DRAM Based on the Dual-Gate TFET," *Nanoscale Research Letters*, vol. 12, p. 524, Sep 2017. doi: 10.1186/s11671-017-2294-3.

[11] R. J. E. Hueting, B. Rajasekharan, C. Salm, and J. Schmitz, "The charge plasma p-n diode," *IEEE Electron Device Letters*, vol. 29, pp. 1367–1369, Dec 2008.

[12] M. J. Kumar and S. Janardhanan, "Doping-Less Tunnel Field Effect Transistor: Design and Investigation," *IEEE Transactions on Electron Devices*, vol. 60, p. 3285–3209, Oct 2013. doi: 10.1109/JPROC.2010.2070470.

[13] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-/spl kappa//metal-gate stack and its mosfet characteristics," *IEEE Electron Device Letters*, vol. 25, pp. 408–410, June 2004.

[14] Silvaco(2015). http://www.silvaco.com. Atlas User Manual.

[15] N. Navlakha, J. Lin, and A. Kranti, "Retention and scalability perspective of sub-100-nm double gate tunnel fet dram," *IEEE Transactions on Electron Devices*, vol. 64, pp. 1561–1567, April 2017.

[16] E. Yoshida and T. Tanaka, "A capacitorless 1T-DRAM technology using gate-induced drain-leakage (GIDL) current for low-power and high-speed embedded memory," *IEEE Transactions on Electron Devices*, vol. 53, pp. 692–697, April 2006.

[17] M. S. Ebrahimi, G. Hills, M. M. Sabry, M. M. Shulaker, H. Wei, T. F. Wu, S. Mitra, and H. . P. Wong, "Monolithic 3d integration advances and challenges: From technology to system levels," in *2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, pp. 1–2, Oct 2014.

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Brief Biography of the Author

Nimish Agarwal has completed his B.Tech. from North-Eastern Hill University (NEHU), Shillong in the department of Electronics & Communication Engineering. He is doing his M.Tech. from Indraprastha Institute of Information Technology (IIIT), Delhi with the specialization in VLSI and Embedded Systems. He is specifically interested in digital design domain. He is going to join as an Engineer in Qualcomm. He can be contacted at **nimish17104@iiitd.ac.in** or **nimish0808@gmail.com**.