Flexible Electronics Based Efficient Front-End Circuits for Noninvasive Continuous Health Monitoring in Biomedical Wearable Devices

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To

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Dedicated to my husband, loving parents and my grand parents . . .

Certificate

This is to certify that the thesis titled **"Flexible Electronics Based Efficient Front-End Circuits for Noninvasive Continuous Health Monitoring in Biomedical Wearable Devices"** being submitted by **Ms. Nishtha** to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of Doctor of Philosophy, is an original research work carried out by her under our supervision. In our opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

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Dr. Sujay Deb (IIIT Delhi)

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Abstract

With the new habits of lifestyle, new health problems are arising and demands continuous health monitoring. Wearable technology will revolutionize our lives in the upcoming years. To enable widespread usage of such devices, it is important to maximize their functionality while minimizing manual intervention, with extended life time, flexibility and at low-cost. The advancement of miniature and flexible devices has fostered a dramatic growth of interest in this technology. Currently, most of the wearable biomedical systems are c-Si based, which are typically rigid, bulky (due to battery size), expensive in terms of fabrication cost and requires some external interface. They limit mobility and comfort of the wearer. Typically in hospitals, in order to monitor ECG signals, which is a part of routine for the cardiovascular patients, is done through ECG measurement equipment with many electrodes and long wires, which limits the patient's mobility. In the same way, BP measurement using cuffs is very inconvenient when frequent measurements need to be recorded. Both these approaches need human interaction. Though some commercial wearable devices are available for biomedical monitoring, which are confined to few biological signal monitoring that includes ECG, EEG, temperature sensor or for the measurement of pulse rate. Compact, reliable and light weight systems, that can monitor the variety of biological signals is still an open challenge. Researchers have been actively seeking for innovative solutions and new technologies that could improve the quality of patient care meanwhile reduce the cost through early detection of serious health problems.

In order to address these issues, this work targets to build a self-contained noninvasive flexible real-time health monitoring front-end, which is compact and do not limit the wearer's mobility. The proposed system can be successfully used by many people ranging from infants, sportsman, elderly people and post-hospitalized patients, where, continuous health monitoring is vital. Further the idea can be extended to store the biological signals over a time period so that doctor can have complete record of the patient's health condition.

In order to bring the proposed biomedical wearable front-end into a reality, many signal conditioning and processing circuits need to be developed with oxide TFT technology (a-IGZO), as it can facilitate fabrication of circuits on flexible substrates. The circuits that are included are on-chip power supply (bootstrapping circuit), clock generators (ring oscillators), pre-amplifier to amplify biomedical signals for pre-processing, low-pass filters (anti-aliasing filter) and ADC (Analog-to-Digital Converter). The biological signals (output of the bio-sensors) need to be processed through these analog and mixed signal blocks in order to transmit the data to the server/smart phone so that in case of an emergency, an alert can be sent to the doctor/wearer in order to provide immediate medical assistance. This type of remote monitoring of the important biological signals in real-time data can significantly minimize health risks.

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Chapter 1

Introduction

1.1 Introduction and Background

Ongoing advances in small gadgets, just as versatile and pervasive processing, have fostered a dramatic growth of interest for wearable technology. Wearable sensors and systems have developed to the point that they can be viewed as ready for clinical application [1]. This is expected not exclusively to the colossal increment in research endeavors committed to this territory in the previous years but to the huge number of organizations that have started investing in the advancement of wearable products for clinical applications [2, 3]. Stable patterns indicating a development in the utilization of this innovation recommends that soon wearable systems will be essential for routine clinical assessments.

Wearable technology in health care applications are predicted to revolutionize many aspects of our human living and social habits. These systems are most intelligent systems that are used to provide high quality health care monitoring [4, 5]. They are quite helpful in preventive healthcare paradigm. These wearable sensing devices are gaining importance due to its ability to monitor day to day activities and also for the continuous health diagnostics that includes critical biological signal monitoring. Today in hospitals, monitoring of biological signals are done by nurses, which includes, blood pressure (BP), heart rate (HR), respiratory rate (RR), blood oxygen saturation and core temperature [6, 7]. The enthusiasm for wearable systems begins from the need for checking patients over extensive periods of time. This case emerges when doctors need to monitor people whose chronic condition incorporates danger of unexpected intense functions or on the other hand people for whom mediation's should be evaluated in the home and outside climate. If observations over one or two days are satisfactory, ambulatory systems can be used to gather physiological information [1]. An obvious example is the use of ambulatory systems for ECG monitoring, which has been part of routine assessment of

cardiovascular patients for nearly thirty years. However, these systems are not appropriate when monitoring has to be accomplished over period of several weeks or months, as it is required in various clinical applications. In addition, the transportation of the clinical instruments required for the monitoring of these signals is not easy and requires medical personnel for its configuration and manipulation [8].

Wearable systems are absolutely non-obtrusive devices that permit doctors to defeat the constraints of ambulatory technology and provide a response to the need for monitoring the individuals over weeks or even months [1, 9]. It provides efficient and cost-effective alternative to on-site clinical monitoring by staying at home. They ordinarily depend on wireless, miniature sensors that are enclosed in patches or bandages,or on the items which can be worn, such as a ring or a shirt. They take favorable advantage of hand-held units to briefly store physiological information and afterward occasionally transfer that information to an information base through a wireless local area network (LAN) or a support that permits Internet connection [10]. The informational sets that are recorded using these systems are then handled to distinguish functions prescient of conceivable worsening of the patient's clinical circumstance or they are investigated to assess the effect of clinical mediation's.

1.2 Problem Statement

The commercial devices that are available are confined to only few biological signal monitoring i.e. either they can monitor ECG or EEG or temperature or pulse rate [11, 12]. For example in reference [13], proposes a touch-based system in order to measure ECG combined with Impedance CardioGram (ICG), in which the main objective was early detection of Congestive Heart Failure (CHF). In another example [14], the eyeglass was developed for PPG acquisition system, which can be used to obtain HR and pulse transit time (PTT). This device also does not uses any external ECG or PPG finger clip. All these system are crystalline-Silicon (c-Si) based [11, 12, 15], which typically have rigid substrates. Also, these all work proposes different solutions for the acquisition of the biological signals. These devices does not allow flexibility, cannot be fabricated at room temperature and are very expensive.

The need of monitoring patient's health condition in regular intervals of time is very important as it will help in detecting the onset of illness in the early stage, leading to the increased quality of life. To enable widespread usage of such devices, it is important to maximize their functionality while requiring minimum intervention from the users, with extended life time, flexibility and cost [16]. This enables physicians to monitor individuals whose chronic condition includes risk of sudden acute events or individuals for whom interventions need to be assessed in the home and outdoor environment. Keeping this in mind, there is a need of a

device, which is compact, reliable, flexible and light weight. Also, different biological signals should be acquired using a single device that do not interfere the user activity. These systems are most intelligent systems that are used to provide high quality health care monitoring. This type of device can be successfully used by many people ranging from infants, sports person, elderly people and post-hospitalized patients, where continuous monitoring plays a vital role.

1.3 State of Art Work

Several portable systems have been developed to measure bio-signals in recent years. For example, in present scenario, ECG monitoring, which is a part of routine for the cardiovascular patients, is done through ECG measurement equipment with many electrodes and long wires, which limits the patient's mobility [17, 18]. In the same way, BP measurement using cuffs is very inconvenient when frequent measurements need to be recorded [19, 20]. Both these approaches need human interaction. Till date, most of the wearable biomedical devices are c-Si based that are rigid, bulky and expensive [21–24]. Today, researchers have been actively seeking for innovative solutions and new technologies that could improve the quality of patient care meanwhile reduce the cost through early detection. It is the need of the today's world that the future health-care system should be preventive, predictive, pre-emptive, personalized, pervasive, participatory, patient-centered and precise, i.e., p-health system [25]. This p-health system requires acquisition, transmission, processing, storage, retrieval, and use of different types of health and biomedical information so that immediate medical assistance can be provided to the patient in-order to minimize health risk.

The typical architecture of a wearable system for continuous health monitoring is presented in Fig. 1.1. In this the patient carries a mobile phone in his/her pocket, which serves as data logger (i.e., the mobile phone talks to the sensors (on the flexible chip) situated on the body) and as an entryway for remote access to the subject's information. Admittance to the subject's information is accomplished through a phone's network or via a wireless LAN. Information is then transferred through the Internet to emergency personnel, a family member or a doctor, which responds immediately to the emergency situations, evaluate the subject's status, and plan clinical intercessions. This health care system is divided in two parts. One is Analog Front-end (AFE) and the other is the communication part. AFE is the most critical block of this biomedical wearable system [26, 27]. In order to implement flexible electronics for this wearable Noninvasive biomedical system, oxide TFT technology is a perfect choice among other semiconductor technologies that allow flexible electronics [28]. The biomedical devices should be such that they are minimally invasive and which can be worn or implanted. Crystalline silicon technology does not allows flexible electronics and also its fabrication

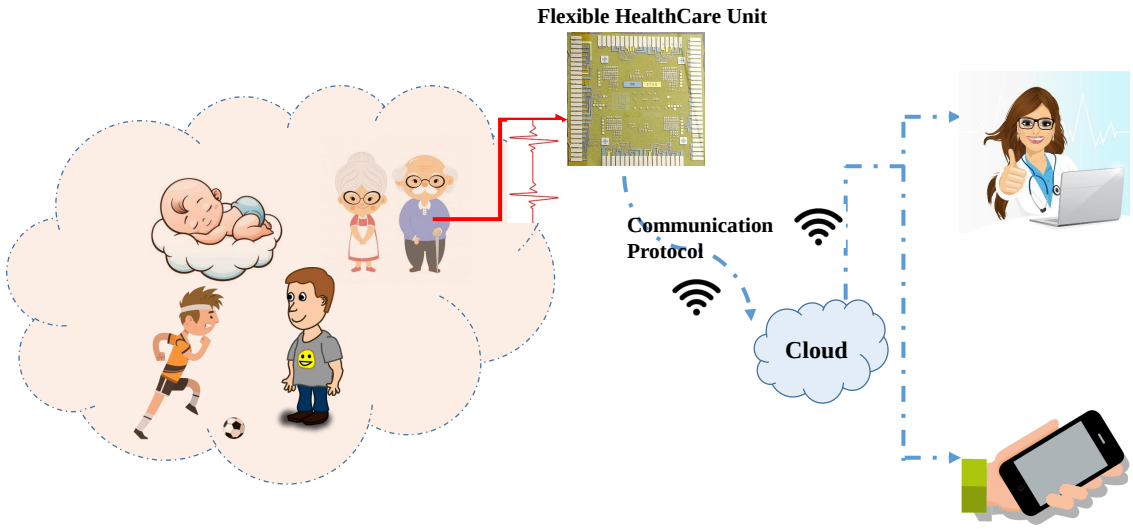


Figure 1.1: Architecture of Wearable Health Care System.

temperature is very high. The other TFT technologies such as a-Si:H and organic TFT has the disadvantage in terms of the low mobility. Because of this limitation oxide TFT technology has been used in this work. The attractive feature of a-IGZO technology is relative high mobility, which is one order (>10 cm^2/V.sec) greater than the other low-temperature compatible TFT technologies [29]. In addition, these devices (IGZO TFTs) are relatively stable and compatible with low-cost fabrication techniques like ink-jet printing. However, this technology imposes several limitations on circuit design. In order, to implement flexible electronics, one of the major challenge is the lack of stable and reproducible p-type oxide TFT. Therefore, CMOS circuit design techniques cannot be adapted directly and forcing to investigate novel design techniques to circumvent this problem.

Fig.1.2 illustrates the evolution of sensing technologies, mainly for electrocardiogram (ECG). They have evolved from water buckets [30] and bulky vacuum tubes [31, 32], bench-top [33] and portable devices [34] with discrete transistors, to the recent clothing and small gadgets based wearable devices with integrated circuits (standard CMOS technology) [15, 35]. The limitations with these systems are, they are bulky (due to battery weight), rigid and requires some external interface [18, 36]. Further, past implementations have disadvantage as it restricts patient's mobility and also continuous data cannot be stored. There is active research going on to evolve these biomedical wearable devices into flexible and stretchable devices [37, 38]. Carbon

Figure 1.2: Timelines of medical devices for ECG measurement

nanotube (CNT) [39] or graphene are one of the candidate in this race. But the drawback with them is fabrication cost is very high. The other technologies are a-Si:H and organic TFTs. Since they have resulted poor mobility ($\sim 1\ cm^2$/Vs) [40], so they are not best choice for biomedical applications. On the other hand, oxide based semiconductor (a-IGZO) thin-film transistor (TFT) technology is showing almost one order higher mobility by retaining all the advantages of other low-cost semiconductor technologies (a-Si:H and organic) that allow flexible electronics. Many a-IGZO TFT based circuits have been reported on flexible substrates [41–49]. The fundamental limitation is that, only individual circuits have been reported instead [50]. In order to implement flexible biomedical system, the IGZO TFT is a good option. However, till date very scarce work is reported for complete system implementation. This is due to the limitation in the circuit design, that are, absence of p-type transistor and also the mobility is one order lower than the c-Si technology. Till date, no such systems have been reported. Now in order to address this issue, this work proposes a low cost self-contained biomedical wearable front-end for real time health monitoring, which guarantee's user comfort. This type of system can be successfully used by all generations ranging from infants, sports person, elderly people and post hospitalized patients, where continuous health monitoring over an extensive period of time plays a vital role. In case of any emergency, an alert can be sent to the doctor/wearer for immediate medical assistance to minimize health risks.

Table 1.1: Frequency Range of Biological Signals

Biological Signals	Frequency Range (Hz)
Electroretinagram	0.5-20
Electronystagmogram	0.6-20
Pneumogram	0.5-40
ECG	0.5-100
EEG	0.5-100
Electromyogram	100-200
Sphygmomanogram	0.25-200

1.4 Objective of the work

In this thesis, we propose a noninvasive wearable biomedical front-end using flexible electronics for continuous health monitoring with oxide TFTs. Currently in literature no such system has been proposed with TFTs. This is the first time we are proposing this biomedical wearable system with the oxide TFTs. A general block diagram of biomedical acquisition front-end is shown in Fig.1.3.

In order to build this front-end, signal processing and mixed-signal blocks are required so that biological signals can be pre-processed and digitized before sending it to the next stages. The proposed systems can work with many bio-sensors (for ECG, EEG or PPG signals), whose output signals are in the order of few mV with a frequency range of 100 mHz to 700 Hz. Table 1.1 shows various biological signals and their frequency ranges.

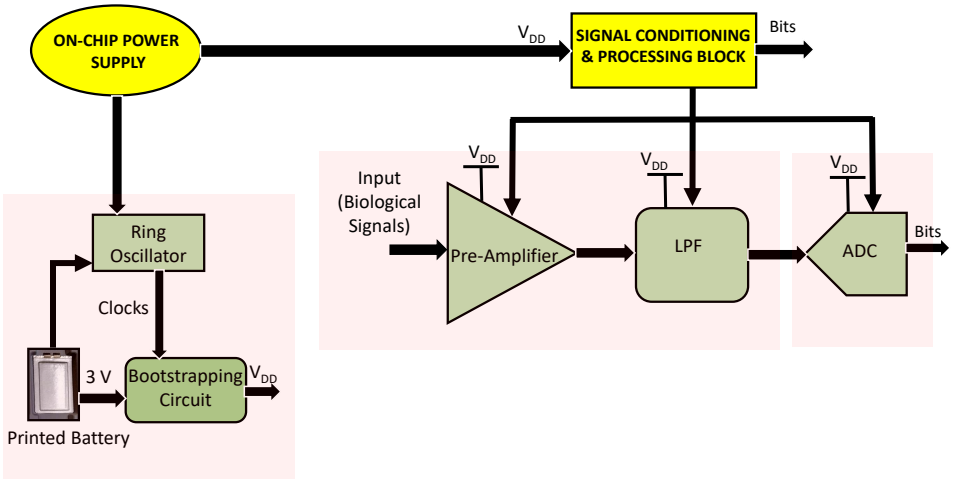


Figure 1.3: A biomedical acquisition front-end with on-chip power supply

1. To build complete analog front-end following signal processing blocks are required:

- **On-chip power Supply** - To make the complete system on-chip, these on-chip power supplies are required. It is comprised of printed batteries (in this work we are using commercial thin-film batteries), Bootstrapping (BS) circuit or charge pumps to boost the DC voltage and to generate required supply voltage to drive on-chip pre-processing and mixed-signal blocks and timing signal generators to generate on-chip clocks.
- **Pre-amplifier** - These are used to amplify bio-sensors output. These designs should ensure low power consumption, robustness (V_{th} insensitive), high CMRR, PSRR, SR, Stability and low input referred noise.
- **Low Pass Filter(LPF)** - Filters are used to filter out unwanted signals.
- **ADC** - Analog to Digital converters are required to convert analog signal into digital bits which can be transmitted to the server.

2. Finally the communication part is needed, which can be Bluetooth or any wireless technology. The complete communication part is to be implemented to have the prototype ready. This part once done, the digital bits can be successfully transmitted to the either mobile or server so that health monitoring of the patient can be done and health risks can be minimized.

1.5 Document Outline

The remaining of the dissertation is organized as follows:

- **Chapter 2**: Related Prior Works with Oxide TFTs
- **Chapter 3**: Introduces a-IGZO TFT technology and characterization, main advantages and challenges imposed for circuit design, fabrication information, device operation and impact of contact resistance.
- **Chapter 4**: Introduces the on-chip power supply, which is required in order to built the complete compact system. This block is implemented with printed battery, ring oscillator (RO) (comparative study of the ROs with a-IGZO TFT is considered) and a bootstrapping circuit (novel circuit with a-IGZO TFTs). The circuit design techniques, functionality of these blocks, schematic diagrams, simulation and measured results are presented in this chapter.

- **Chapter 5**: This chapter illustrates design and implementation of signal conditioning block, which is comprised of pre-amplifiers and switched capacitor filters (novel block), along with their schematic diagrams, simulation results and measurement results.
- **Chapter 6**: Two types of Delta-Sigma ADCs (novel designs) are presented in this chapter, where one is passive and the other is active. The main component of these ADCs are comparators. Five different novel comparators have been designed and the best one is selected in order to implement ADC.
- **Chapter 7**: In this chapter complete wearable biomedical analog front-end using oxide TFTs (novel design) is presented from simulation.
- **Chapter 8**: Conclusions and future work is presented in this chapter.

1.6 List of Publications

- **JOURNAL**:
  (a) **Wadhwa N**, Bahubalindruni PG, Pedda S, Deb S, Gupta M, Mahato P, Gupta D and Tripathi A, "Switched Capacitor Low-Pass Filter with a-IGZO TFTs on Flexible Substrate," *Electron. Lett.*, 2021, https://doi.org/10.1049/ell2.12144.
  (b) **Wadhwa N**, Bahubalindruni PG, Chapagai K, Goes J, Deb S, Barquinha P., "Sixth-order Differential Sallen-and-Key Switched Capacitor LPF using a-IGZO TFTs," *International Journal of Circuit Theory and Applications (Wiley)*, 47(1), pp: 32-42., 2019, https:// doi.org/10.1002/cta.2576.
  (c) **Nishtha Wadhwa**, PG Bahubalindruni, Sujay Deb, Joao Goes and Pedro Barquinha, "High Performance Comparators Using a-IGZO TFTs for Flexible Electronic Systems," submitted in *Circuits, Systems, and Signal Processing Journal (Springer)*.
  (d) **Nishtha Wadhwa**, Ana Coerrila, PG Bahubalindruni, Sujay Deb, Joao Goes and Pedro Barquinha, " Active Δ-Σ ADC with a-IGZO TFTs For Biomedical Applications," will be submitting in *IEEE Transaction in Circuits and System I (TCAS-I)*.
- **CONFERENCES**:
  (a) **Nishtha Wadhwa**, PG Bahubalindruni, Ana Coerrila, John Melo, Joao Goes, Sujay Deb and Pedro Barquinha, "Mostly Passive Δ-Σ ADC with a-IGZO TFTs for Flexible Electronics," accepted in *IEEE International Symposium on Circuits and Systems (ISCAS), 2021*.

(b) **N. Wadhwa**, P. G. Bahubalindruni, S. Deb and P. Barquinha, "Bootstrapping Circuit with IGZO TFTs for On-Chip Power Supply Generation," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, 2019, pp. 1-5, doi: 10.1109/ISCAS.2019.8702356.

(c) **Wadhwa N.**, Bahubalindruni P.G., Deb S., "A PVT Insensitive Low-Power Differential Ring Oscillator". In: Rajaram S., Balamurugan N., Gracia Nirmala Rani D., Singh V. (eds) *VLSI Design and Test. VDAT 2018*, Communications in Computer and Information Science, vol 892. Springer, Singapore, https://doi.org/10.1007/978-981-13-5950-7_7.

(d) Rai N., Agarwal V., **Wadhwa N.**, Tiwari B., Bahubalindruni P.G., "Temperature Insensitive Low-Power Ring Oscillator Using only n-type Transistors," In: Rajaram S., Balamurugan N., Gracia Nirmala Rani D., Singh V. (eds) *VLSI Design and Test. VDAT 2018*, Communications in Computer and Information Science, vol 892. Springer, Singapore. https://doi.org/10.1007/978-981-13-5950-7_3.

(e) Shukla S., Tiwari B., **Wadhwa N.**, Bahubalindruni P.G., Barquinha P., "Low-Power Switched Operational Amplifier Using a-InGaZnO TFTs," In: Rajaram S., Balamurugan N., Gracia Nirmala Rani D., Singh V. (eds) *VLSI Design and Test. VDAT 2018*, Communications in Computer and Information Science, vol 892. Springer, Singapore. https://doi.org/10.1007/978-981-13-5950-7_32

(f) **N. Wadhwa**, J. Martins, P. Bahubalindruni, S. Deb and P. Barquinha, "A Comparitive Study of On-Chip Clock Generators Using a-IGZO TFTs for Flexible Electronic Systems," *International Flexible Electronics Technology Conference (IFETC)*, Ottawa, ON, Canada, 2018, pp. 1-6, doi:10.1109/IFETC.2018.8583926.

(g) T. Keragodu, B. Tiwari, **Nishtha**, P. Bahubalindruni, J. Goes and P. Barquinha, "A Voltage Controlled Oscillator Using IGZO Thin-Film Transistors," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018, pp. 1-5, doi: 10.1109/ISCAS.2018.8351175.

(h) K. Chapagai, P. Bahubalindruni and **Nishtha**, "2nd Order Sallen Key Switched Capacitor LPF with N-type Transistors," *31st International Conference on VLSI Design and 17th International Conference on Embedded Systems (VLSID)*, Pune, India, 2018, pp. 319-324, doi: 10.1109/VLSID.2018.83.

Chapter 2

Related Prior Work with Oxide TFTs

2.1 Introduction

As discussed in chapter 1, that currently available biomedical devices are c-Si based, which are typically rigid, bulky and expensive. The main target of this work is to built a system, which is compact, reliable, flexible and light weight. a-IGZO TFTs are the perfect choice in order to built such systems. Very limited work has been done with the oxide TFT technology in reference to the biomedical application.

2.2 Prior Work with a-IGZO TFTs for Biomedical Applications

In the literature, a 52 μW heart-rate measurement interface for wearable application has been reported [51]. The circuit has been fabricated on flexible foil with a-IGZO TFT. A cascaded diode connected load amplifier has been used with a gain of 22 dB and bandwidth of 3 kHz. The output is a binary Pulse Width Modulation (PWM) waveform that can be send to the reader device using some wireless communication. The power that is consumed by this circuit is 0.052 mW. In addition to this, it consists of some passive elements (resistors and capacitors), in order to cancel out input referred noise. The disadvantage of this system is that it can only measure HR and consumes high power compared to the work proposed in this thesis.

The other biopotential front-end circuit is also reported in the literature with a-IGZO on flexible substrate [52]. It is composed of an input chopper that helps in noise reduction and frequency multiplexing. The proposed circuit is mainly for the EMG (Electromyography)

signals, which is mainly a drawback as it cannot be used to process the other biological signals. In addition pre-amplifier is only amplifying the signal.

2.2.1 Individual blocks with oxide TFT technology

Various blocks have been reported using oxide TFT technology in the state of art work. Such as different ROs, bootstrapping circuits, amplifiers, filters and ADCs.

The first block in this analog front end is the on-chip power supply, which consists of printed battery, BS circuit and a RO. With oxide TFT, this work proposes a novel bootstrapping circuit. DC-DC converters that have been reported before can boost DC voltage but the drawback with them is that they employ inductors [53, 54], whose fabrication is the challenging part. Also, some complex circuitry needs to be added in order to get the accurate voltage. The other block used is the RO. This work presents a comparative study of four different types of ROs that are diode connected, BS circuit, pseudo-CMOS and pseudo-CMOS BS, which are simulated under similar condition. In literature different ROs have been reported with oxide TFT technology [43, 46, 55–57]. The details of this will be discussed further in chapter 4. The main drawback is that there is no such work in the literature, where these all four ROs have been reported under similar conditions, so that the functionality of these ROs can be properly studied and the best design can be chosen according to the application.

The low amplitude biological signals are being sensed by the pre-amplifier, which amplifies the signal for the further pre-processing. In order to have a simple circuitry with oxide TFT technology, a simple positive feedback pre-amplifier has been used in this work [45, 58]. Some of the complex designs of this amplifier has also been presented in the literature with oxide TFT [50]. In this work, double gate oxide TFT has been fabricated, which makes it complex in terms of fabrication. The gain reported in this paper is less for the biomedical application. In this work a simple positive feedback amplifier has been used, which boosts the signal by the gain of 40 dB. The rest of the details is mentioned in the later Chapter.

The limited work has been reported with TFTs towards filter design. Till now, in literature a RC biquad was demonstrated using a−Si:H TFTs with a power supply of 25 V [59]. In order to overcome the disadvantage of RC filter, this work proposes SC biquad for the first time at relatively low supply voltage, as its performance is a function of ratio of capacitance instead of RC time constants, that suffers from huge absolute process variations. The main advantage of this antialising filter with respect to the state of art in flexible electronics [59], is in terms of power consumption, cut-off frequency and area, as this design is purely a resistor-less based.

The last block that is used is ADC. The work done towards ADC design with oxide TFTs is very limited, though they are critical functional blocks to implement systems of practical importance. Since the mobility of the oxide TFTs are one order lower as compared to crystalline-

Si based transistors and due to absence of complementary device, it is quite challenging to achieve a reasonable resolution. It can be noticed from the state of the art, with Nyquist ADCs ENOB is limited to 9 bits [60–63]. The oversampling converters (Δ-Σ (Delta-Sigma ADC)) ensures better resolution due to noise shaping ability. It is worth to note that the work reported on Δ-Σ ADC with oxide TFTs is scarce [64–66]. ENOB of 9 bits [64], 4.1 bits [65] and 5.2 bits [66] were reported. Since practical applications need higher ENOB, this work proposed a novel passive delta-sigma ADC with improved FOM. In the proposed design, important active block is comparator, which is implemented with preamplifier, latches and full rail-to-rail logic gates. Since the ADC reported in this work can ensure ENOB $>$ 11 bits and able to operate at few kHz frequency range, it is suitable for the real world applications.

The complete detail description (advantages and disadvantages) of the each of these block in accordance with the state of art work has been discussed in subsequent chapters.

Chapter 3

Oxide TFT Technology for Flexible Electronics

This chapter presents a brief introduction to the low-temperature compatible thin-film transistor (TFT) technologies that can facilitate flexible electronics. This chapter only gives information regarding the technology that is used for designing all the circuits that has been presented in this thesis. The layouts of transistors and circuits have been designed using this technology.

In also highlights the advantages of Amorphous Indium Gallium Zinc Oxide (a-IGZO) TFT technology. Which is followed by different TFT device structures, working principle and electrical characterization of devices considered in this work. Fabrication details of these devices are also presented. Finally, oxide TFT technology limitations for circuit design is discussed.

3.1 Thin-Film Transistor Technology

The most common choice for the low-temperature compatible TFT semiconductor material was hydrogenated amorphous silicon (a-Si:H) to facilitate low-cost flexible electronics [67]. However, the disadvantage with this technology is low carrier mobility ($\sim$1 cm^2/Vs) and non-transparency in visible spectrum [68]. The other low-temperature compatible (typically < 180 degrees) TFT technology is organic semiconductor based. These organic TFTs, despite exhibiting great potential for flexible and large area electronics, have shown poor mobility in the same order as a-Si:H TFTs. Then amorphous oxide semiconductor (AOS) based TFTs were reported in 2004 [69], which preserves all the advantages of a-Si:H and organic TFTs. Further, a-IGZO can show relatively higher mobility (> 10 cm^2/Vs) with good optical transparency (86%) of the semiconductor in the visible spectrum [70, 71]. Among other AOS materials, IGZO is

a successful multi-component oxide till date within the industry and academic research [71–75]. This technology allows fabrication of circuits or devices on different substrates like glass, plastic and papers facilitating flexible electronics [76, 77]. Further, IGZO TFTs allow large-area uniformity due to absence of grain boundaries unlike poly-silicon and ZnO based TFTs [78]. Its low-cost and low-temperature manufacturing methods such as solution processes and printing techniques are the main factors that foster the commitment of research groups and companies towards this technology.

3.2 TFT Device Structure, Operation and Characteristics

3.2.1 TFT Device Structure

A typical oxide TFT has gate, source and drain electrodes together with an insulating/dielectric layer that isolates gate and active material (semiconductor). The most common structures are staggered top-gate, staggered bottom-gate, co-planar top-gate, co-planar bottom-gate, as can be noticed in Fig. 3.1.

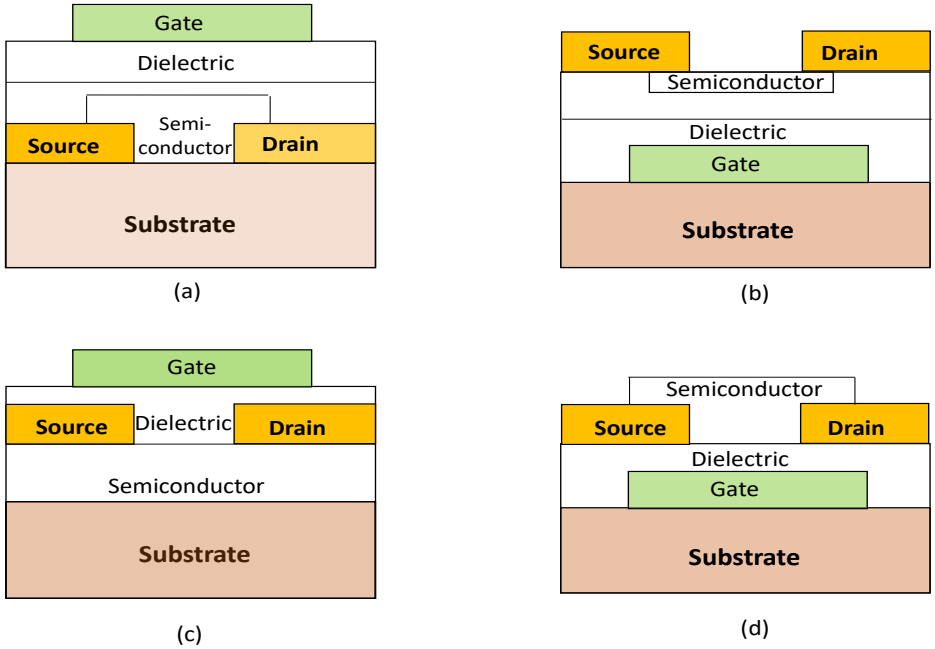


Figure 3.1: Common structures of a-IGZO TFTs: (a) Staggered top-gate, (b) Staggered bottom-gate, (c) Co-planar top-gate and (d) Co-planar bottom-gate.

In order to minimize the parasitic due to overlap between gate to source/drain, self-aligned structures can be employed. The thickness of the semiconductor layer [79], dielectric [80],

source and drain electrodes [81] and fabrication conditions [82] show significant impact on the TFT electrical performance.

3.2.2 Operating Principle of IGZO TFT

Despite metal oxide semiconductor field effect transistor (MOSFET) and a-IGZO TFT being structurally different, both are Field-effect transistors (FETs). In both the FETs, the drain current is controlled by the bias voltage (V_{GS} and V_{DS}). In CMOS, for the long channel devices, V_{th} corresponds to the V_{GS} value at which inverted charge carrier concentration is equal to the bulk carrier concentration [44]. From this, it is said that the moderate to strong inversion channel is created between the source and the drain terminals just below the dielectric. Whereas, in the case of oxide TFTs, the source and drain electrodes are not deposited in the bulk unlike MOSFETs. The bulk is a pure insulator in these devices and no inversion layer is formed in the channel. In IGZO TFTs the semiconductor is amourphous in nature and is inherently n-type material. Generally, in the case of oxide TFTs definition of V_{th} (threshold voltage) is not very clear. Whereas, the term V_{on} is used, which corresponds to the V_{GS} value at which there is a significant increase in the drain current (I_D).

Currently in the literature, the complete device physics for carrier transportation mechanism is not yet clearly understood. Therefore, small signal models of MOSFETs corresponding to level 1 equations are being used for circuit design. However, it should be understood that the MOSFETS models cannot predict the behaviour of a-IGZO TFTs to good accuracy because MOSFETS employs crystalline-silicon, whereas, IGZO is an amorphous semiconductor. Further, the conduction mechanism in MOSFETS are due to inversion, whereas, in IGZO the channel is formed due to accumulation. Other differences between these two transistors are device structure, materials and fabrication processing conditions. Though a-Si:H TFT employs amorphous semiconductor, this model also cannot be directly adopted to IGZO TFT. This is because of the distinctive property of the amorphous semiconductor oxides, where the localized charge carriers are less than the free charge carriers, unlike a-Si:H TFT [83, 84].

3.2.2.1 Device Operation

Consider a a-IGZO TFT biased with a positive gate voltage as shown in Fig. 3.2 If V_{th} is positive then the TFT is enhancement type. Whereas, if it is negative then it is depletion type.

The different regions of operation of the device can be defined as follows.

When V_{GS} is less than V_{on}, there is no channel in the semiconductor and hence no current can flow in the device, then the device is said to be in cut-off (see Fig. 3.2(a)).

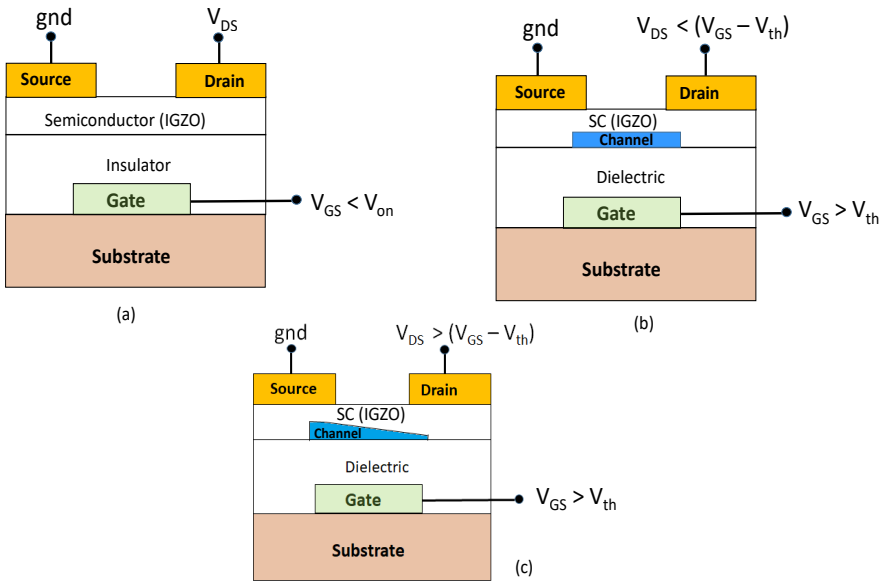


Figure 3.2: Operating regions of TFT: (a) Cut-off, (b) Linear, (c) Saturation.

When $V_{on} < V_{GS} < V_{th}$, channel is formed with weak accumulation and results in very low drain to source current. Then the device is said to be in the sub-threshold region of operation. As V_{GS} is further increased above V_{th}, a conductive channel is formed with strong accumulation. As V_{DS} is increased, the charge carriers are drifted towards the drain electrode. The current flow is then detected in the opposite direction of the charge carriers i.e. from drain to source. When, $V_{DS} < V_{GS}$ - V_{th}, the device is said to be in linear region of operation and a uniform conductive channel is formed near the dielectric and semiconductor interface as shown in Fig. 3.2(b). In the linear mode of operation, the relation between the drain current (I_{DS}) and the bias voltages (V_{DS} and V_{GS}) are given as (as per Level-I MOSFET equations):

$$I_{DS} \approx \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}] \tag{3.1}$$

where:

μ is the mobility; $\frac{W}{L}$ is the aspect ratio; C_{ox} is the oxide capacitance per unit area.

When, $V_{DS} \geq V_{GS}$ - V_{th}, then the channel is pinched off near the drain electrode as shown in Fig. 3.2(c). This is due to the weaker vertical electrical field that is created near the drain end as $V_{GD} < V_{th}$.The drain to source current equation is of quadratic form given as:

$$I_{DS} \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2 \tag{3.2}$$

Since the mobility of a-IGZO TFT is less than the c-Si, so the drain current is also significantly small for same size and voltages of the devices used. These approximations from equation (3.1) and (3.2) are considered for the sake of circuit design.

3.2.3 Device Modelling

There are almost 70 models [85] of the MOSFETs that addresses derivative discontinuity, geometry effects, self heating, negative conductance, bulk charge effect on current, velocity saturation, hot carriers and impact ionization. Some of these models are empirical, some are semi-empirical and others are physical. In the case of CMOS, Level 1 SPICE model is the simplest and fastest but does not meet the industrial needs in the case of sub-micron technologies [86]. However, it is used for circuit design and hand calculations due to its simplicity. a-IGZO TFTs are still in its emerging phase, as international standards and different fabs are employing different device structures, materials and fabrication conditions resulting in different electrical performance of the device.

In this work, an equivalent circuit (EC) empirical modeling approach with ANNs is adopted [44, 45]. These models are accurate, simple, continuous and it can effectively characterize all the properties of the device in the complete region of operation because ANNs are universal approximators [87]. This model is developed from measured characteristics of the device and it can predict static and dynamic behavior of the device. The model was implemented in Verilog-A and ported to Cadence Virtuoso to simulate the circuits.

3.3 Fabrication of a-IGZO TFT based circuits

Circuit fabrication using IGZO TFT technology has been carried out at two fabs; (i) CENIMAT, Portugal and (2) NCFlexe, IIT Kanpur. Fabrication details from these labs are detailed below together with electrical characteristics of individual devices.

3.3.1 CENIMAT

A 60 nm thick Mo gate electrode is sputtered on a 125m thick PEN substrate. Then, a 180 nm thick multilayer/multicomponent dielectric is co-sputtered without intentional substrate heating, using SiO_2 and Ta_2O_5 targets, followed by dry etching process in SF6 atmosphere. A 20 nm thick semiconductor layer is then deposited without intentional substrate heating, using ceramic IGZO target (In:Ga:Zn atomic ratio of 2:1:2) and Ar+O_2 atmosphere and patterned by liftoff. Source and drain electrodes are sputtered with 60 nm thick Mo. Gate, dielectric and source/drain patterning is done by dry etching process in SF_6 atmosphere. The interlevel

dielectric is 1μm thick parylene layer, patterned using a dry etching process in O_2 atmosphere. On top of this layer, metal 3 is deposited: by sputtering 400 nm thick Mo, followed by dry etching process in SF_6 atmosphere. The devices were annealed at 180°C for 1 hour in air before source/drain deposition and at the end of the process [29, 44, 45, 49, 88]. The cross sectional schematic view of the IGZO TFT and interconnects are presented in Fig. 3.3(a). In order to minimize the parasitics due to interconnects (overlap of gate to source/drain) and to further improve the yield of the process for circuits operation with this technology, metal 3 (400 nm thick Mo) is being used. This brings the additional advantage of achieving IGZO back channel surface passivation with the inter-level dielectric, i.e., no extra processing steps are required to assure robust operation of the TFTs. Inset of Fig. 3.3(b) shows a PEN substrate containing isolated TFTs and various circuits. It also demonstrates linear transfer characteristics of the TFT with W = 320μm and L = 15μm. These devices are showing a turn-on voltage of 0.5V, mobility of 12 cm^2/V.s and on-off ratio exceeding 10^7. Small clockwise hysteresis, with charge trapping phenomena at dielectric/semiconductor interface, is noticed from the plot. Transistor performance is unaffected by bending radius of down to 15mm [48].

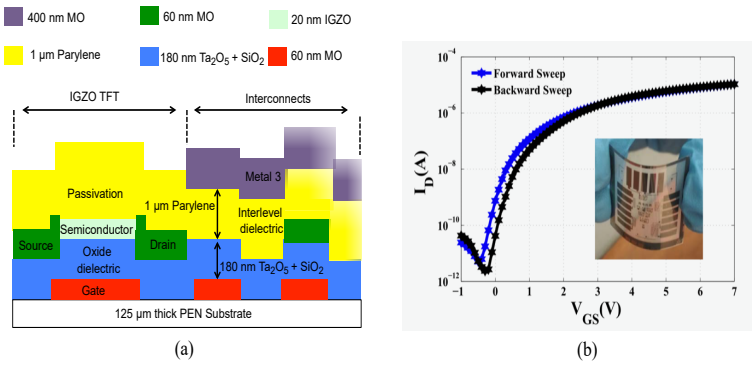
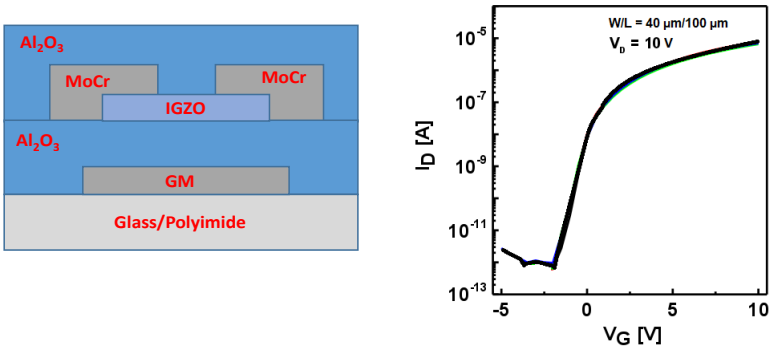


Figure 3.3: (a) Cross sectional view of the TFT and interconnects adopted in this work (b) Linear transfer characteristics of a single TFT with W = 320 μm and L = 15 μm at V_{DS} = 0.1 V.

3.3.2 FLEXI LAB

TFTs were fabricated on a glass substrate coated with a polyimide film. First, polyimide precursor solution from Fujifilm (Duramide 115A) was spin coated on an Eagle XG glass substrate. After drying, precursor film was cured at 400°C in order to achieve a smooth polyimide film on glass substrate. A buffer layer of ALD Al_2O_3 was deposited at 250°C. 80 nm thick Mo film was sputtered and gate electrodes were patterned by photo-lithography and wet-etching. Subsequently, 80 nm thick Al_2O_3 layer was deposited at 150°C using atomic layer deposition. Via holes were opened using standard photo-lithography and wet-etching.

Approximately 25 nm thick IGZO film was sputtered from In:Ga:Zn (1:1:1) target under Ar with 2% O_2 at a process pressure of 1 mTorr. Semiconductor islands were defined by wet-etching of IGZO film. Approximately 80 nm thick Mo source-drain was applied by the lift-off process.



(a) (b)

Figure 3.4: (a) Cross sectional view of the TFT, (b) Transfer Characteristics of TFTs on polyimide substrate.

Eventually, the whole device was passivated by 80 nm thick ALD Al_2O_3 film and subsequently annealed at 150°C for 2 hours on a hotplate under ambient conditions. The cross sectional view and output characteristics of a fabricated TFT through this process is shown in Fig. 3.4 (a) and (b), respectively. for the width (W) of 40 μm and length (L) of 100 μm respectively. At a drain voltage (V_D) of 10 V, the turn on voltage and the mobility of the transistor are observed to be $\approx$ -1.8 V and $\approx$ 8.2 cm^2/Vsec, respectively.

3.3.3 Difference in Cenimat & Flexi Lab TFT

Below Table 2.1 shows clearly the difference between in the fabrication process and the electrical characteristics of both the TFTs. The only limitation with the Flexi Lab TFT is that its turn on voltage is negative i.e. when -1.8 V is applied then only the TFT will start operating.

Table 3.1: Comparison between both sets of oxide TFTs used

S.No.	Characteristic	Cenimat	Flexi Lab
1.	Thickness of Mo Layer	60 nm	80 nm
2.	Dielectric	$SiO_2 + Ta_2O_5$	Al_2O_3
3.	Mobility	12 cm^2/Vs	8.2 cm^2/Vs
4.	On-Off Ratio	10^7	$> 10^7$
5.	Turn-On Voltage	0.5 V	-1.8 V
6.	Substrate	PEN/Glass	Polyimide/Glass

3.4 Challenges in Circuit Design

Following are the challenges for the circuit design:

- The most important challenge is the lack of stable and reproducible complementary device (p-type transistor) [89], poor mobility compared to crystalline silicon [90] and gate bias stress susceptibility [91]. Due to these reasons new design techniques needs to be investigated for the circuit design with a-IGZO TFTs.
- There are no commercial device models that can be used for circuit simulations. In addition, the nonexistence of the standardized libraries make the circuit design quite challenging.

Next chapters in this work focuses on design details of the individual blocks that are employed in the analog biomedical front-end system (see Fig.1.3).

Chapter 4

On-Chip Power Supply Generation for the Biomedical Analog Frond-End

Proposed biomedical wearable front-end block diagram with oxide TFTs is presented in Fig. 4.1. The first important block is the on-chip power supply, which is meant for generating V_{DD} for the rest of the pre-processing blocks. This block is implemented with thin-film printed battery, clock generators and bootstrapping circuits in order to generate required DC supply voltage for the pre-processing blocks. Complete design details, implementation and characterization of individual circuits in this block are presented in the chapter.

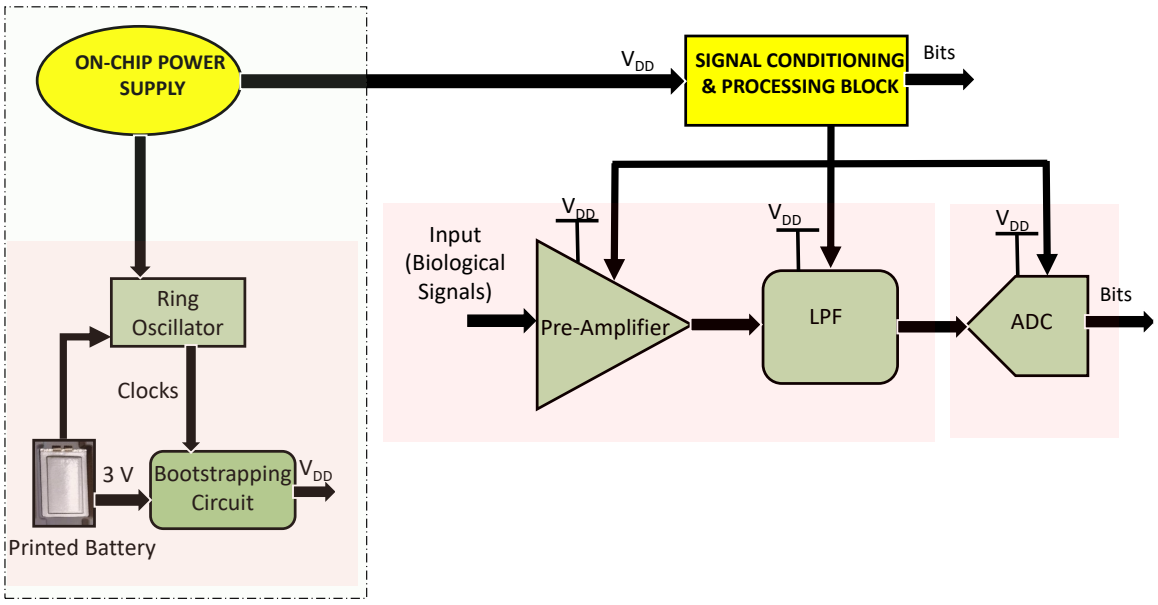


Figure 4.1: Biomedical front-end block diagram with on-chip power supply (highlighted).

4.1 Printed Battery

BrightVolt PME (Polymer Matrix Electrolyte) is employed in this work. These commercial printed batteries typically generate an output voltage around 3 V and flexible electronics with IGZO TFTs typically needs a power supply $>$ 5 V (depending on the dielectric) [44, 92, 93].

In-order to supply 10 V to these circuits, at-least three printed batteries need to be placed in series, which can occupy significant active area, as single battery size is approximately 2 cm*2 cm [94]. In order to circumvent this problem, on-chip DC boosters are going to be employed in this work together with a single thin-film battery to generate required power supply voltage for the circuits.

4.2 Proposed Bootstrapping Circuit

The next important circuit of the on-chip power supply generation is the DC voltage boosters, to boost the DC voltage from the thin-film battery. Though DC/DC converters can boost the DC voltage, they employ inductors [53, 54]. Fabrication of high performance inductors is a challenging task. In-order to overcome this problem, charge pumps are used to boost the input voltage [95]. The main drawback with this topology is that, in order to get the accurate precision in voltage levels at the output, complex topologies like switched capacitors [96] are needed. Another possible way is to use thin-film printed batteries, whose fabrication is compatible with printed techniques. But as mentioned before, printed batteries occupy huge die area.

In order to address these challenges, this work proposed on-chip power supply generation with a single thin-film battery, bootstrapping (BS) circuit (developed first time with IGZO TFTs) and on-chip clock generator (as shown in Fig. 4.1), to ensure a compact system. The proposed BS circuit with IGZO TFTs can generate 2*V_{DD} and 3*V_{DD} with the printed batteries output voltage of around 3 V ($\approx V_{DD}$) and this circuit plays a vital role in the on-chip supply generation for wearable biomedical front-end.

These bootstrap circuits can work with different loading conditions along with the clock generators that can be successfully implemented with the IGZO TFTs [46, 97], leading to complete self-contained system without complex interfacing. This circuit occupies very less active area and consumes low power, which is an optimal choice for compact biomedical wearable applications. The proposed circuit design analysis simulations are carried out using in-house a-IGZO TFT model [44, 88].

4.2.1 Circuit Description

Proposed boostrapping circuit schematic is shown in Fig. 4.2(a). In this circuit switches are implemented with n-type transistor (a-IGZO TFT) due to absence of complementary p-type device. ϕ_1 and ϕ_2 are two complementary clocks and C_1, C_2, C_3 and C_4 are of equal value.

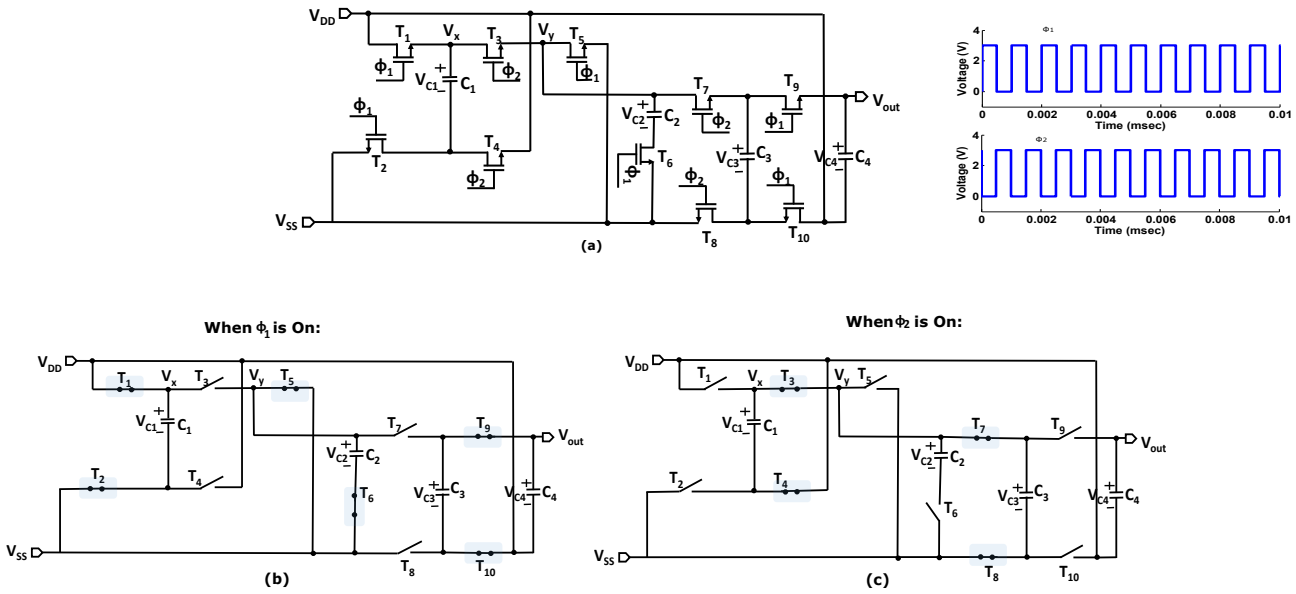


Figure 4.2: (a) Proposed Bootstrap circuit schematic with a-IGZO TFTs (b) Equivalent circuit when ϕ_1 is enabled, (c) Equivalent circuit when ϕ_2 is enabled.

The clocks ϕ_1 and ϕ_2 can be generated using on-chip clock generators (Ring Oscillators(RO)) as shown in Fig. 4.3(a). In this RO, inverters are designed by the combination of Pseudo-

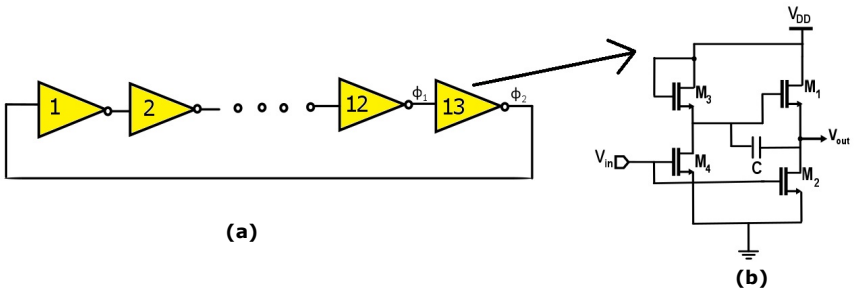


Figure 4.3: (a) Ring oscillator for on-chip clock generation, (b) Circuit schematic of Pseudo-CMOS Bootstrapped inverter for RO.

CMOS and Bootstrapped techniques, shown in Fig. 4.3(b), in order to obtain full swing at the output [56] (Discussed in detail in Section 3.3). ϕ_1 and ϕ_2 are obtained from the 12^{th} and 13^{th} stage of this RO.

When ϕ_1 is enabled as shown in Fig. 4.2(b), capacitor C_1 will hold the voltage that is given by 4.1.

$$V_{C_1} = V_{DD} - V_{SS} \tag{4.1}$$

where, voltage V_{SS} is the voltage of ground potential and V_{DD} serves as the input voltage.

In the same way at the capacitor C_2, the voltage is given as:

$$V_y = V_{C_2} = V_{SS} \tag{4.2}$$

When ϕ_2 is enabled as shown in Fig. 4.2(c), Capacitor C_1 is already holding the voltage equal to

$$V_x = V_{DD} - V_{SS} \tag{4.3}$$

where,

$$V_x = V_{C_1} \tag{4.4}$$

and V_y is given as:

$$V_y = V_{C_2} = V_x + V_{DD} \tag{4.5}$$

$$= V_{DD} - V_{SS} + V_{DD} \tag{4.6}$$

$$V_{C_2} = 2V_{DD} - VSS \tag{4.7}$$

$$\approx 2V_{DD} \tag{4.8}$$

So, Capacitor C_2 now holds the voltage V_{C_2}, which is further transferred and bootstrapped by the similar 2^{nd} half of the circuit to the voltage given by V_{C_3}. The final output that is acquired is given by 4.9.

$$V_{out} = 3V_{DD} - 2V_{SS} \tag{4.9}$$

$$\approx 3V_{DD} \tag{4.10}$$

The capacitor C_4 holds the charge in order to provide constant voltage at the output when ϕ_2 is enabled again. From equation 4.10 it can be noticed that the circuit bootstrapped the input voltage to three times of V_{DD} value. This simple circuit can be effectively used for on-chip biomedical wearable health monitoring system to provide the supply voltage for the proper functioning of all the analog and mixed signal blocks. This circuit is tested with the input spanning from 2 to 10 V.

4.2.2 Simulation Results

Using oxide TFT model, for the first time the bootstrapping circuit has been designed and simulated in Cadence environment. The circuit has been tested at various frequencies of the two complementary clocks (ϕ_1 and ϕ_2) upto 1 MHz. For the complete system-on-chip, these two clocks can be generated from the Pseudo-CMOS BS RO as shown in Fig. 4.4. By using this circuit, complete rail to rail timing signals can be obtained even with 3 V power supply.

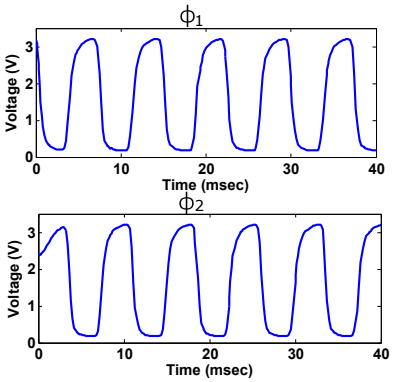


Figure 4.4: Simulation results of ring oscillator for generation of two inverting clock pulses (a) ϕ_1 and (b) ϕ_2.

The simulation results of the bootstrapping circuit at different clock frequencies with a load of 2 MΩ is shown in Fig. 4.5. It can be noticed that it takes approximately 50 μsec to settle

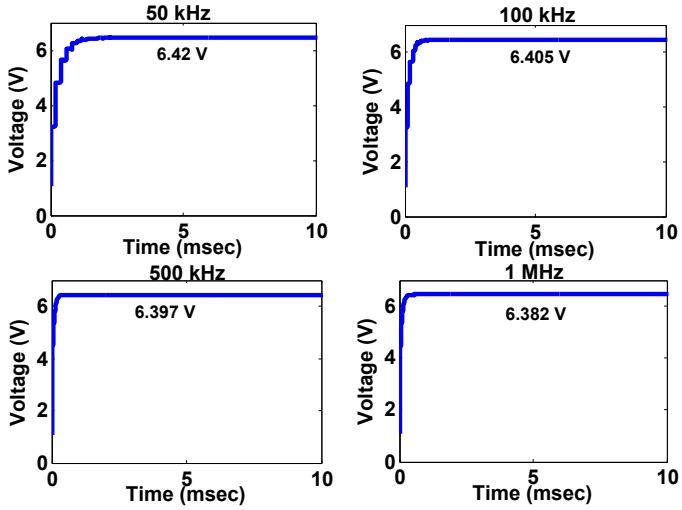


Figure 4.5: Simulation results of bootstrapping circuit at clock frequency of 50 kHz, 100 kHz, 500 kHz and 1 MHz with input voltage of 3 V at 2 MΩ load.

down to the final value. This is due to the finite non-zero on-resistance of the switches and the parasitics of the transistors. Generally, a high TFT on-resistance increases the settling time. Assuming a constant channel length, narrow TFTs results in high on-resistance, whereas too wide TFT results in non-negligible charge injection. As a trade off between these two factors proper dimensions of the TFTs have been chosen to implement switch. It can be noticed that with the input voltage of 3 V, the resulted output is $>$ 5 V. Irrespective of the frequency of the clocks, output is same i.e. approximately equal to 6.4 V for 2 MΩ loading condition. This constant voltage can serve as V_{DD} for the rest of the low power signal processing blocks in order to build complete system on-chip. In addition to this, the circuit consumes very low power equal to 24.9 μW for 2 MΩ load, which is a good fit for flexible biomedical applications.

In order to test the robustness of the bootstrapping circuit, PVT analysis have been carried out, which shows 2.3%, 1.2% and 10% of variation against temperature, voltage and process in 180 nm CMOS technology (since oxide TFT models for statistical simulations are not available, PVT analysis was done using only NMOS devices). With this, it can be inferred that this circuit is an optimal choice for the real world applications.

Fig. 4.6, presents the output voltage of the proposed circuit when the input is varying between 2 to 10 V at loading conditions 2 MΩ and 5 MΩ respectively. This circuit response at other loading conditions are presented in Table 4.1.

Table 4.1: Output voltage and current with different loads with input voltage of 3 V

S.No.	Loads (MΩ)	Voltage (V)	Current (μA)
1.	**1**	**5.2**	**5.2**
2.	**2**	**6.4**	**3.2**
3.	**5**	**7.9**	**1.58**
4.	**10**	**8.3**	**0.83**
5.	**25**	**8.8**	**0.352**
6.	**50**	**8.99**	**0.179**

It can be noticed that the output voltage is less than 3*V_{DD} because of non-idealities of switches, such as threshold voltage drop and finite on-resistance.The output voltage is also function of the load resistance. With the maximum load of 50 MΩ, it can generate voltage upto 3*V_{DD}. This circuit is capable of generating a supply voltage, which is sufficient to drive other analog pre-processing circuits with oxide TFTs and consumes low power. The micrograph of the bootstrapping circuit is shown in Fig. 4.7. The overall area that is occupied by the bootstrap circuit is approximately equal to 25 $(\mu\text{m})^2$, which is very low, compared to the printed batteries size, when multiple batteries are used in series connections to get the desired voltage. By using this circuit the system can be made compact.

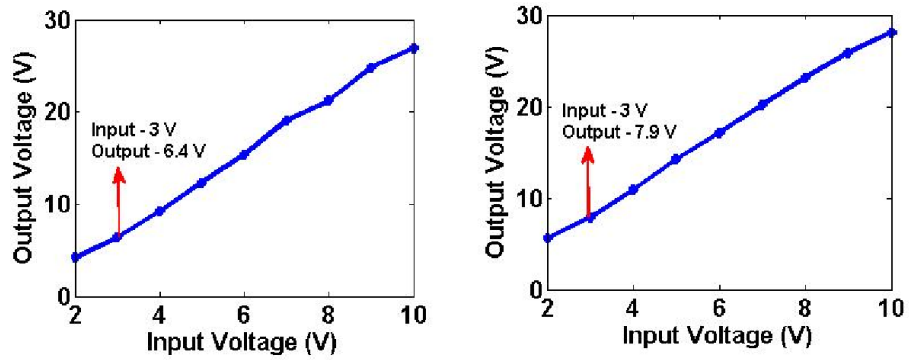


Figure 4.6: Simulation results of bootstrapping circuit at clock frequency of 1 MHz with different loading conditions (a) 2 MΩ and (b) 5 MΩ.

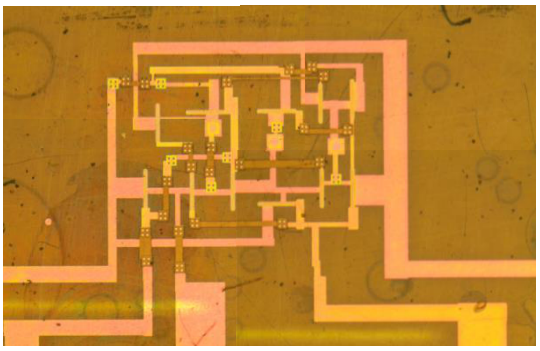


Figure 4.7: Micrograph after fabrication of the boostrapping circuit with a-IGZO TFT.

4.3 Ring Oscillators with Oxide TFT

The proposed Bootstrapping circuit requires clocks (ϕ_1 and ϕ_2 as shown in Fig. 4.2(a)), which can be generated using proposed Ring Oscillators (RO). This section discusses four different types of ROs that are implemented with different inverter topologies using IGZO TFTs, which includes Diode connected load, Capacitive bootstrapping (BS), Pseudo-CMOS and Pseudo-CMOS bootstrapping architectures. These topologies have been simulated using in-house IGZO TFT models under similar conditions using different power supplies (10 V, 15 V and 20 V) in cadence environment. In addition, measured results of these ROs are also presented when they are tested with thin-film batteries (with the supply voltages ranging from 3-9 V).

Many ROs have been reported till date with a-IGZO TFTs [43, 46, 55–57]. Absence of complementary devices lead to poor noise margin [98], which results in the degradation of output voltage swing when such multiple stages are used in cascade [99]. In addition, this also leads to high static power consumption. Many designs using monotype TFTs have been proposed to address above challenge (mainly output swing), such as, depletion load [100, 101],

dual gate [47, 98], dual V_{th} TFTs [102]. These techniques have limited applicability due to the requirement of dedicated TFT characteristics, additional masks and fabrication processing steps. It is very challenging to achieve CMOS characteristics with these Amorphous Oxide Semiconductors (AOS) [103, 104]. In addition, some of the hybrid structures have also been proposed with n-type AOS and p-type organic/carbon nanotube TFTs [105]. However, it is relatively expensive and complicated to fabricate these hybrid structures due to different processing conditions [47, 106, 107]. It should also be noted that, even if the circuits are implemented only with n-type oxide TFTs, it is hard to compare the circuit performance as there is no international standardization for oxide TFT technology unlike standard CMOS. For this technology different Fabs use different processing steps, device structures and materials [29, 46, 57, 97]. Therefore, for a given application it is hard to choose the most suitable on-chip clock generator (RO) architecture that can give the desired performance. The main topologies that are considered in this study to implement RO are with diode connected load [108, 109] capacitive bootstrapping [46], Pseudo-CMOS [43, 97] and the combination of Pseudo-CMOS together with capacitive bootstrapping [56, 57]. All the circuits have been simulated using in-house TFT models at different power supply ranging from 10-20 V [88, 110]. This work also presents a comparitive study of ROs with a-IGZO TFTs that are implemented under same conditions using different inverter topologies.The measured results have also been reported of these ROs in the later sections.

4.3.1 Circuit Description

A ring oscillator is comprised of an odd number of inverters connected in a ring fashion, which leads to oscillations [111]. The conventional CMOS based RO consists of both PMOS and NMOS transistors, while in current work, all designs have been implemented with a-IGZO TFTs, which are inherently n-type in nature. A 5-stage RO has been considered in this work (keeping in mind the area constraints of the system) as shown in Fig. 4.8, where an inverter is an essential block. This inverter design dictates overall performance of the ring oscillator. Therefore, different implementations of inverters based on only n-type transistors are discussed below, as a first step.

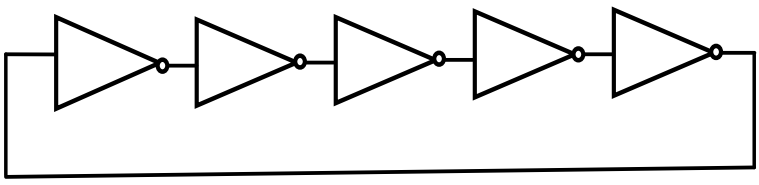


Figure 4.8: A 5-stage Ring Oscillator.

1. **INVERTER WITH DIODE CONNECTED LOAD:** The circuit schematic with diode load inverter is presented Fig. 4.9(a). Here both M_1 and M_2 have same channel length,

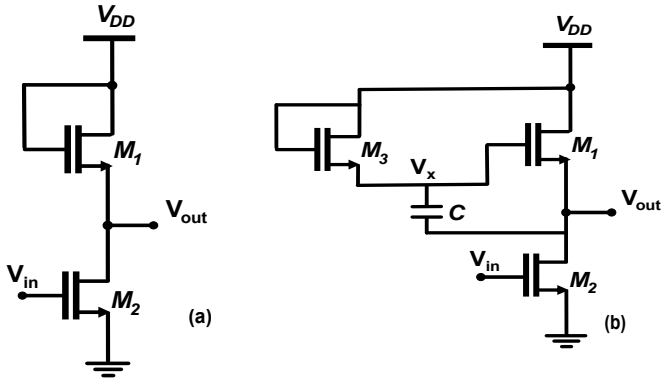


Figure 4.9: Inverter with (a) Diode connected load and (b) Capacitive Bootstrapping Load.

while $W_{M2} > W_{M1}$ to favour voltage swing. In this circuit, if the input voltage (V_{in}) is set to a low value, M_2 is almost turned off and nearly no current flows through the device. Consequently, the output voltage (V_{out}) approaches to V_{DD}-V_{th_1}. As V_{in} increases, the drain current increases, thus the voltage drop across M_1, which results in a lower V_{out}. In this case V_{out} is given by (4.11).

$$V_{out} \approx V_{DD} - \frac{1}{g_{m1}} I_D \tag{4.11}$$

Full swing cannot be achieved through this topology. From small signal analysis low frequency gain of Fig. 4.9(a) is given by (4.12).

$$A_v = \frac{g_{m2}}{g_{m1} + g_{ds1} + g_{ds2}} \tag{4.12}$$

If $g_m >> g_{ds}$, then

$$A_v \approx \sqrt{\frac{W_2}{W_1}} \tag{4.13}$$

Analysis of (4.13) reveals that to achieve a high gain (sharp transition between V_{OH} and V_{OL} in voltage transfer characteristics) the width of the driver transistor should be high as shown in Table 4.2, giving rise to large parasitics that decrease the operation frequency mainly due to miller capacitance (C_{gd} of M_2) formed by considerable overlap between gate to drain.

2. **INVERTER WITH CAPACITIVE BOOTSTRAPPING LOAD:** Another topology that can be used with a-GIZO TFTs is based on capacitive bootstrapping load as shown

Table 4.2: Dimensions of Transistors for the different inverter topologies

S.No.	Inverter Topology	Transistors	W(μm)	L(μm)
1.	**Diode connected**	M1	20	20
		M2	320	20
2.	**BS**	M1,M2	160	20
		M2	20	20
3.	**Pseudo CMOS**	M1,M2	160	20
		M3	20	20
		M4	20	20
4.	**Pseudo-CMOS BS**	M1,M2	160	20
		M3	20	20
		M4	20	10

in Fig. 4.9(b). In this circuit a bootstrapping capacitor C is added between the source and gate electrodes of transistor M_1. The value of C should be relatively greater than the parasitics introduced by TFTs in the circuit to ensure proper bootstrapping operation. In this topology, M_3 always operates in cut-off, as there is no low impedance path to drive current.

When input goes high, M_2 conducts and V_{out} settles at V_{OL}.

$$V_{out} = V_{OL} \tag{4.14}$$

Voltage at node V_x is given by (4.15).

$$V_x = V_{DD} - V_{GS_3} \approx V_{DD} \tag{4.15}$$

When input goes low, M_2 is off and V_{out} increases towards V_{DD}. Due to the bootstrapping:

$$V_x \approx 2V_{DD} - V_{GS_3} - V_{OL} \tag{4.16}$$

This topology is widely used to improve the V_{OH} by pulling up the gate voltage of load TFT (M_1) to levels higher than V_{DD}. Frequency of operation is a function of bootstrapping capacitor and aspect ratios of the transistors for a given technology. The disadvantage of this topology is that, $V_{OH} \approx V_{DD}$ but poor $V_{OL} > 0$ V.

3. **INVERTER WITH PSEUDO-CMOS LOAD:** Third topology is the Pseudo-CMOS inverter as shown in Fig. 4.10(a). This topology can replicate the behaviour of the CMOS inverter. Two additional TFTs M_3 and M_4 are added to apply inverted signals to M_1 and

M_2, so that CMOS inverter behavior can be replicated. When the input is low, M_1 is on and M_2 is off. The output voltage V_{out} is given by (4.16).

$$V_{out} \approx V_{DD} - 2V_{th} \tag{4.17}$$

When the input is high, M_1 is off and M_2 is on, making $V_{out} \approx V_{SS}$. The advantage of this inverter is that it improves the output swing mainly V_{OL} by making M_2 and M_1 on and off, respectively. This helps to reduce the static current through M_1 and M_2 branch, resulting in low power consumption compared to bootstrapping RO by employing smaller dimensions for M_3 and M_4 in Fig. 4.10(a).

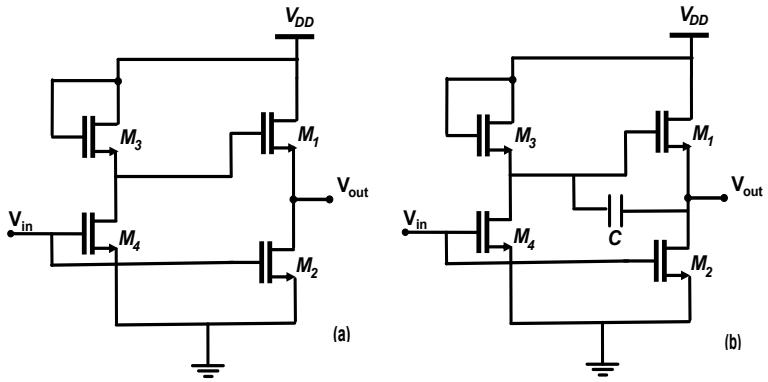


Figure 4.10: Circuit schematic formed with (a) Pseudo-CMOS configuration and (b) Pseudo-CMOS Bootstrapped configuration.

4. **PSEUDO-CMOS BOOTSTRAPPED INVERTER:** By combining the advantages of both pseudo-CMOS and bootstrapped inverters, Pseudo CMOS Bootstrapped inverter is designed as shown in Fig. 4.10(b). By incorporating Pseudo-CMOS topology, it can replicate the behavior of CMOS inverter by adding two additional TFTs (M_3 and M_4) in front of load TFT (M_1) which helps to improve V_{OL} by reducing the static current through the driving TFT (M_2). The bootstrapped capacitor helps to improve V_{OH}. When input goes from low to high, M_1 is turned off due to inverted gate signal while M_2 is turned on. This will connect the output node to $V_{SS} \approx V_{OL} \approx 0$. When input goes from high to low, M_1 is turned on and M_2 is turned off. At the same time, output voltage also rises, pulling up the gate voltage of M_1 by bootstrapping through C.

   The bootstrapped high gate voltage at M_1 can set V_{OH} close to V_{DD}. It keeps the advantages of both (Pseudo-CMOS and Capacitive BS) which means $V_{OH} \approx V_{DD}$ and $V_{OL} \approx 0$. Almost full output voltage swing can be obtained by this topology without significantly compromising power and frequency.

4.3.2 Simulation and Measured Results

4.3.2.1 Simulation Results

A 5-stage RO is formed by different inverter topologies which are discussed in previous section. As a first step individual inverter performance from circuit simulation are presented in Fig. 4.11 with Diode connected, Bootstrapping, Pseudo-CMOS and Bootstrapped Pseudo-CMOS inverters at V_{DD} = 10V.

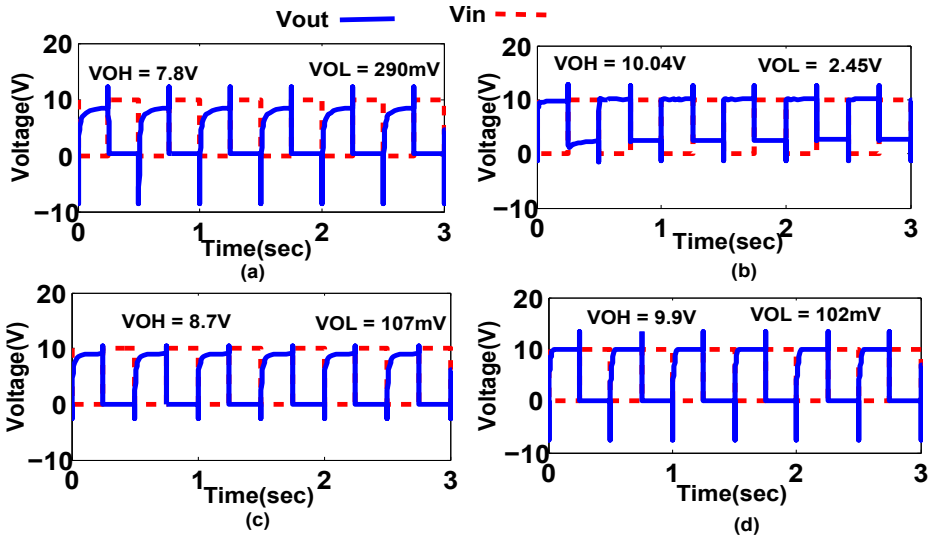


Figure 4.11: Simulation outcomes of different inverter topologies with power supply of 10 V, (a) Diode connected load inverter, (b) Capacitive BS load inverter, (c) Pseudo-CMOS inverter, (d) Pseudo-CMOS BS inverter.

Diode connected inverter does not provide full swing due to design limitations. BS inverter topology provides $V_{OH} \approx V_{DD}$ but poor V_{OL}. Whereas, Pseudo-CMOS provides $V_{OL} \approx 0$ but poor V_{OH}. By combining both these topologies i.e. Pseudo-CMOS and bootstrapped full swing is obtained (98% of V_{DD}). This topology can be used for various applications where full swing is needed.

By using all these inverters topologies RO have been designed and simulated in Cadence environment with the power supply voltage rails of 10 V, 15 V and 20 V under no load condition.

1. **Diode Connected RO:** Simulation outcome of RO formed with inverters using diode connected load is shown in Fig. 4.12. It can be noticed that the output voltage swing is 55% of V_{DD}. Poor swing makes the circuit unsuitable for clock generation. The driver transistor M_1 is much wider than load (Table 4.2), which leads to large parasitic capacitance in turn limiting the frequency of oscillations.

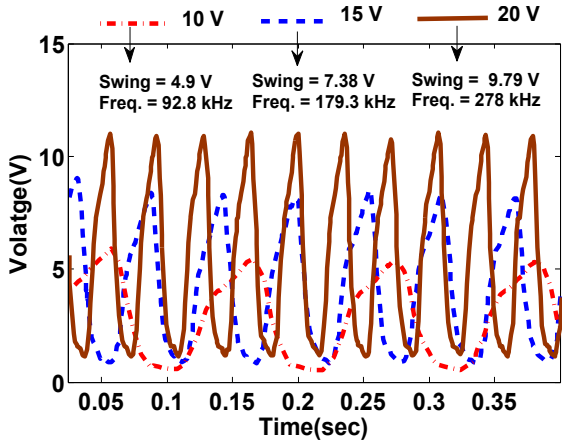


Figure 4.12: Simulation outcome of RO formed with diode connected load.

2. **Capacitive Bootstrapping RO:** Fig. 4.13 shows the output response of capacitive bootstrapping RO. It can be inferred from the figure that the output is 82% of V_{DD} i.e. provides better swing than diode connected RO. In this, capacitance C is in the same order as C_{gs} of transistor, which makes it operate at high frequency in the range of MHz. The drawback with this topology is poor V_{OL}. To nullify this drawback value of C should be increased, which in turn increases the output swing but decreases the frequency of oscillations.

3. **Pseudo-CMOS RO:** Fig. 4.14 shows the output characteristics of Pseudo-CMOS RO. From the figure it can be noticed that V_{OH} is highly compromised due to V_{th} drop in each stage. However V_{OL} is improved, reaching closer to V_{SS} as it imitates the CMOS inverter behaviour.

4. **Pseudo-CMOS Bootstrapped RO:** Fig. 4.15 shows the output characteristics of Pseudo-CMOS Bootstrapped RO. The V_{OH} and V_{OL} of the circuit is improved i.e. $V_{OH} \approx V_{DD}$ and $V_{OL} \approx V_{SS}$. The output voltage swing with this topology is 95% of V_{DD}.

   Table 4.3 presents the performance metrics of various ROs with a-IGZO TFTs that are implemented and simulated in this work. Values reported in literature are also included for comparison. It can be seen that bootstrapping RO provides high frequency (F) of operation in the order of MHz with improved figure of merit or PDP (Power Delay Product) compared to other RO topologies. Whereas, Pseudo-CMOS can provide low power consumption with respect to bootstrapping and Pseudo-CMOS Bootstrapped RO. The advantages of both these topologies are noticed in Pseudo-CMOS bootstrapped RO which provides high voltage swing peak-to-peak (V_{PP}) with reasonable figure of merit

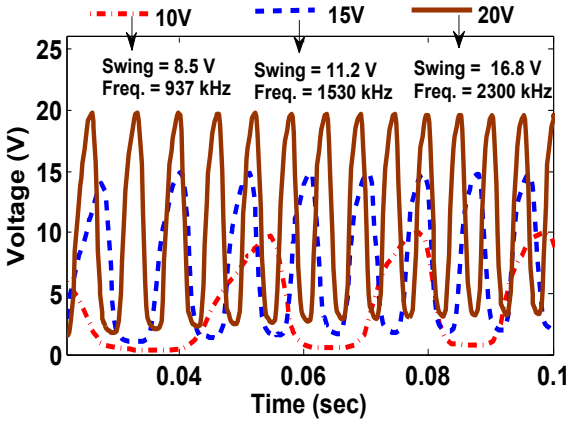


Figure 4.13: Simulation outcome of RO formed with capacitive BS load.

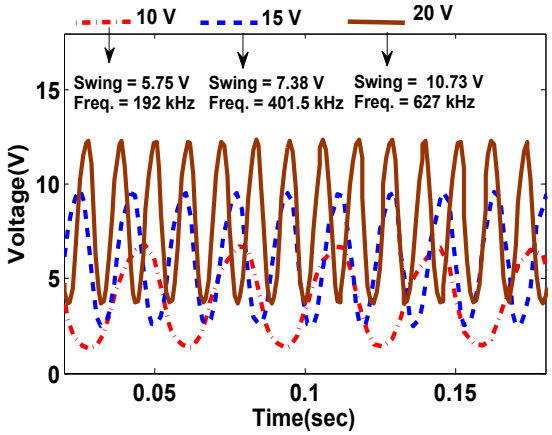


Figure 4.14: Simulation outcome of RO Pseudo-CMOS inverter topology.

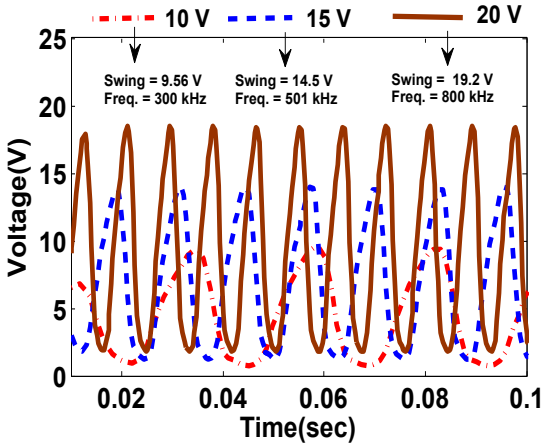


Figure 4.15: Simulation outcome of RO formed with Pseudo-CMOS BS inverter topology.

Table 4.3: Performance Matrices of Various ROs with a-IGZO for flexible electronics

This Work							**Previous Work**				
S. No.	**Inverter Topology**	V_{DD} **(V)**	**Voltage Swing (V)**	**F (kHz)**	**Power (mW)**	**PDP (nJ)**	**Type of Device**	**F (kHz)**	**T (°C)**	**PDP (nJ)**	**Voltage Swing (V)**
1.	**Diode Connected**	10	4.9	92.8	0.342	0.73	-	-	-	-	-
		15	7.38	179.3	1.36	1.5	-	-	-	-	-
		20	9.79	278	3.6	2.5	Single Gate (on PET [108])	94.8	<200	-	12
2.	**BS**	10	8.6	937	2.8	0.5	Bottom Gate [46]	10650	300	-	8
		15	11.2	1530	10.1	1.3	-	-	-	-	-
		20	16.8	2300	26	2	-	-	-	-	-
3.	**Pseudo CMOS**	10	5.75	192	0.6	0.62	Metal-oxide TFT [57]	300	230	7.56	8.7
		15	7.89	401.5	2.97	1.4	Metal-oxide TFT [57]	500	230	15	12
		20	10.73	627	8.17	2.6	Metal-oxide TFT [57]	650	230	28	15.6
4.	**Pseudo CMOS BS**	10	9.56	300	0.59	0.39	Top Gate TFT [56]	70	-	**-**	8.5
		15	14.5	501	2.2	0.87	Top Gate TFT [56]	200	-	**-**	11.7
		20	19.2	800	3.5	0.8	Top Gate TFT [56]	272	-	**-**	18

or PDP (Power Delay Product) implemented under same conditions. In addition, the performance of ROs in terms of frequency of operation, device structures and annealing temperature are compared with the state of art. Since all the simulations are carried out under similar conditions, the user can choose the topology based on the given application. For high frequency of operation-capacitive bootstrapping technique can be used, for low power applications- Pseudo-CMOS can be used and for high voltage swing-the combination of both i.e. Pseudo-CMOS bootstrapped can be used. In addition, all these circuits presented in this work can be fabricated at room temperature (T) compared to the state of the art work.

4.3.2.2 Measured Results

The ring oscillators were fabricated at CENIMAT and tested at 3, 6 and 9 V, which are generated using printed batteries. These voltages have been chosen because a single printed battery that is used can generate a maximum voltage of 3 V. The micrographs of five-stage RO with diode-connected inverter and with Pseudo-CMOS Bootstrapped inverter topologies are presented in Fig. 4.16 and Fig. 4.17 respectively. The measured results of diode connected RO and Pseudo-CMOS BS RO is shown in Fig. 4.18 and Fig. 4.19 at 3 V, 6 V and 9 V respectively, with a load of 15 pF ‖ 10 MΩ.

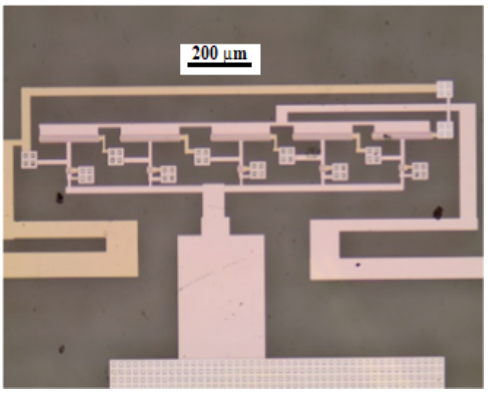


Figure 4.16: Micrograph of five-stage Diode Connected Ring Oscillator.

From the Table 4.4 it can be observed that there is a drop in the voltage swing of the ROs. This is mainly due to less number of stages that are present in the RO. It can be inferred from the table that Pseudo-CMOS BS RO is best suited for this biomedical application as it can provide 6.09 V of voltage swing when V_{DD} of 9 V is applied using printed batteries and the required frequency range for the given application. Frequency of operation can be further improved by using on-chip buffers and swing can be improved by employing more number of

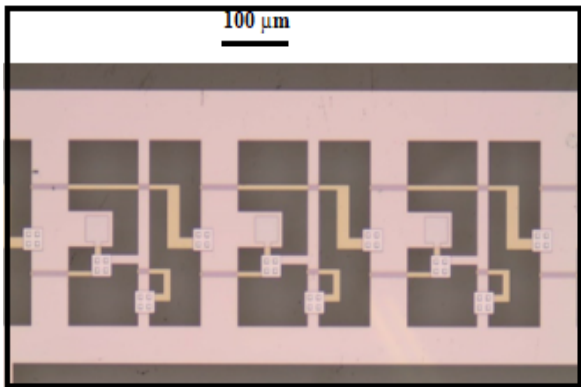


Figure 4.17: Micrograph of five-stage Pseudo-CMOS Bootstrapped Ring Oscillator.

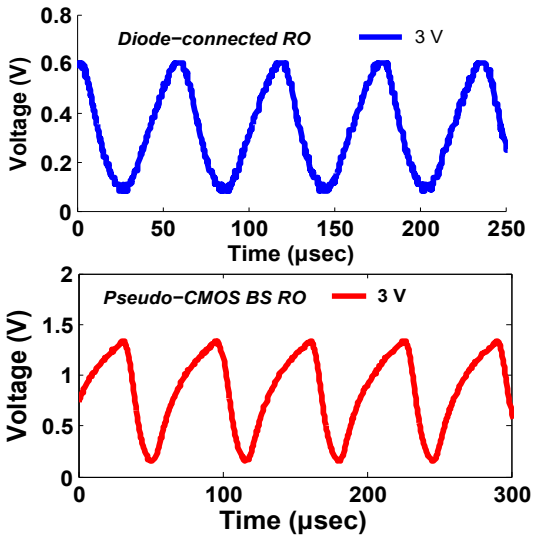


Figure 4.18: Measured results of Diode connected RO and Pseudo-CMOS BS RO with single thin-film battery at V_{DD} of 3 V.

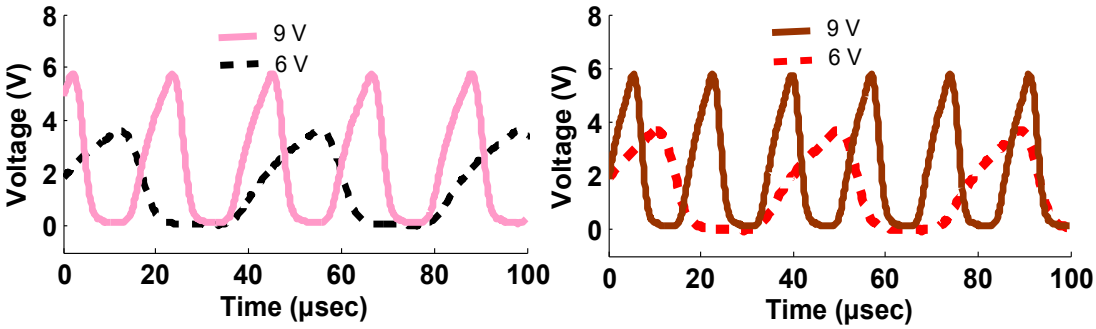


Figure 4.19: Measured results of (a) Diode connected RO and (b) Pseudo-CMOS BS RO at V_{DD} of 6 V and 9 V respectively.

Table 4.4: Measured Results of Ring Oscillators.

S.No.	RO TOPOLOGY	V_{DD} (V)	VOLTAGE SWING (V)	FREQUENCY (kHz)
1.	**Diode-Connected**	3	0.6	4.2
		6	3.78	24.46
		9	5.71	56.34
2.	**Pseudo-CMOS BS**	3	1.4	5.65
		6	3.99	28.7
		9	6.09	60

stages. In order to verify the impact of number of stages in the RO on the voltage swing, circuit simulations have been carried out with 13 stages at 3 V power supply.

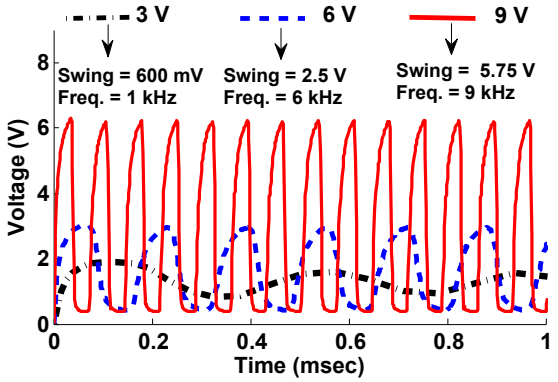


Figure 4.20: Simulation outcome of thirteen stage RO formed with diode connected load.

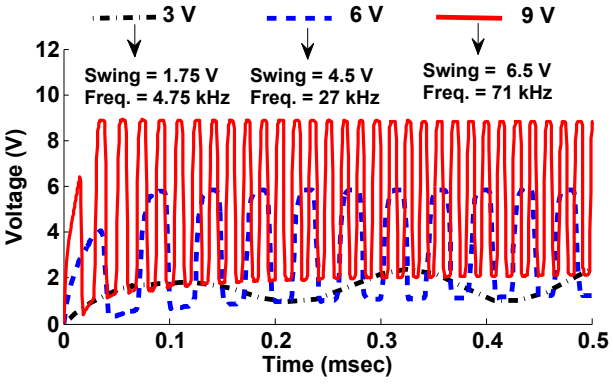


Figure 4.21: Simulation outcome of thirteen stage RO formed with capacitive bootstrapping load.

The simulation results of these ROs with the load of 15 pF ‖ 10 MΩ) are presented in Fig. 4.20, Fig. 4.21, Fig. 4.22 and Fig. 4.23. It can be noticed from the figures that approximately

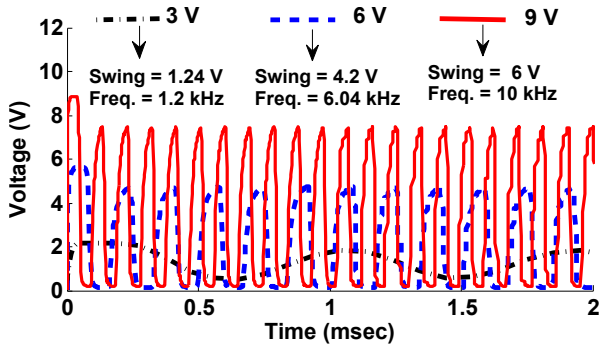


Figure 4.22: Simulation outcome of thirteen stage RO formed with pseudo-CMOS load.

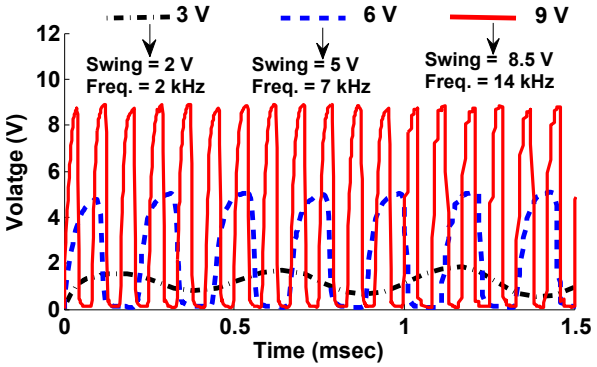


Figure 4.23: Simulation outcome of thirteen stage RO formed with pseudo-CMOS BS load.

full swing ($\approx 95\%$) at the output can be obtained with Pseudo-CMOS BS RO. Because of this advantage, it can be successfully used as clock generators for bootstrapping circuit.

4.4 Conclusions

This chapter deals with a novel bootstrapping circuit and different ROs with the oxide TFT technology. The novel bootstrapping circuit using IGZO TFTs for the first time, generates power supply > 5 V with $I_{DD} > 5.2\ \mu$A to drive signal processing blocks in a wearable biomedical system.

The ROs are implemented with different inverter topologies using IGZO TFTs under similar conditions. It can be inferred, for high frequency of operation capacitive BS can be preferred, for low power Pseudo-CMOS and diode-connected topologies can be used and if a particular application demands full swing, Pseudo-CMOS Bootstrapping circuit can be used without much compromising with the figure of merit. Because of this Pseudo-CMOS BS RO has been

adapted in this work to built the on-chip clock generators, as it is best suited for the targeted application, which has been verified from the measured results. Both of these circuits opens a window for self-contained flexible electronics in various other applications as well.

Chapter 5

Pre-Processing Blocks for Bio-medical Front-End

This chapter covers design and implementation details of pre-processing blocks (see Fig. 5.1), which consists of an amplifier that can amplify low amplitude signals and a novel LPF to remove unwanted signals.

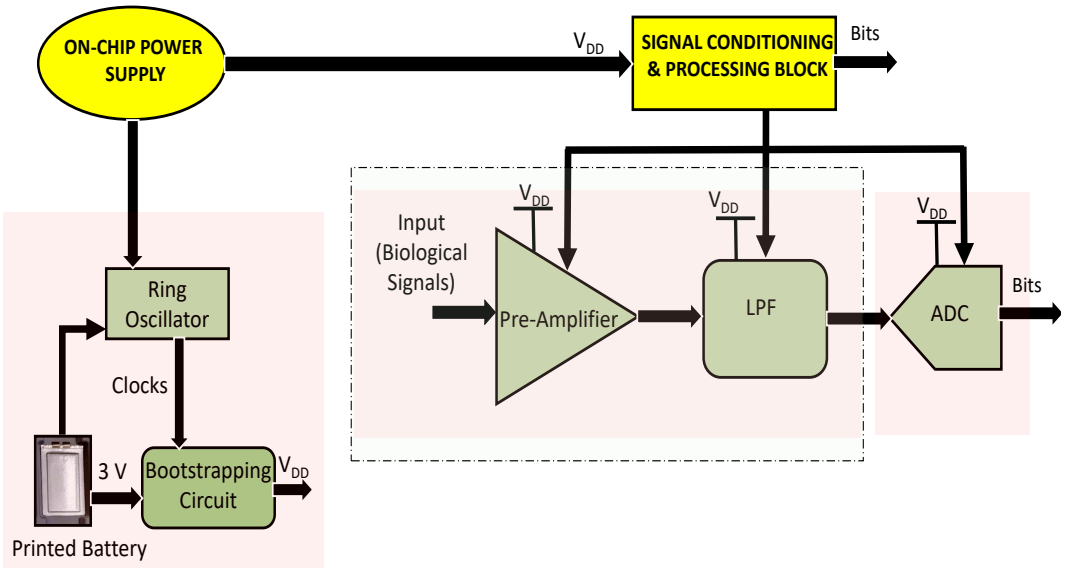


Figure 5.1: Biomedical analog front-end with pre-processing block (highlighted).

5.1 Pre-amplifiers

The bio-Sensors output is typically in the order of few mV with a frequency range of 100 mHz to 200 Hz that are subjected to pre-amplification in the analog domain. In this work positive feedback amplifier is considered in order to have minimum complexity so as to obtain better yield.

5.1.1 Positive Feedback Amplifier

5.1.1.1 Introduction

The design and implementation of high-gain amplifier using only n-type transistors with a-IGZO TFTs impose major limitations due to the absence of complementary (p-type) device and lower mobility of the amorphous semiconductor. Since CMOS design techniques cannot be adapted directly, new design methods need to be investigated to overcome the technology challenges for circuit design.

One of the most important parameter in designing of an amplifier is the gain. Gain enhancement techniques using NMOS transistors have been adapted by various TFTs technologies that have unipolar device [112, 113]. With a-Si:H TFTs, a common source (CS) amplifier with positive feedback technique has been implemented in the literature, which consists of only n-type transistors [68] and presents the gain of around 10 dB. In addition to this, positive feedback technique with a-IGZO TFTs has also been reported in the literature [45, 114, 115]. This amplifier topology is employed in this work due to its simplicity.

5.1.1.2 Circuit Description

To explain the positive feedback technique, let us consider first the gain enhancement techniques with the CS amplifiers. Load impedance of the CS amplifier dictates overall gain. Possible CS amplification topologies with only n-type transistors are shown in Fig. 5.2.

- **CS amplifier with Resistive Load**

  Assuming the channel length modulation is neglected, the CS amplifier gain with the resistive load (see Fig. 5.2(a)) is given by:

$$A_{v1} = -g_{m1} * R_D \tag{5.1}$$

  The gain of the amplifier is limited by the value of load resistor (R_D) and trans-conductance of the driving transistor (g_{m1}) that is directly proportional to the aspect ratio of the driving

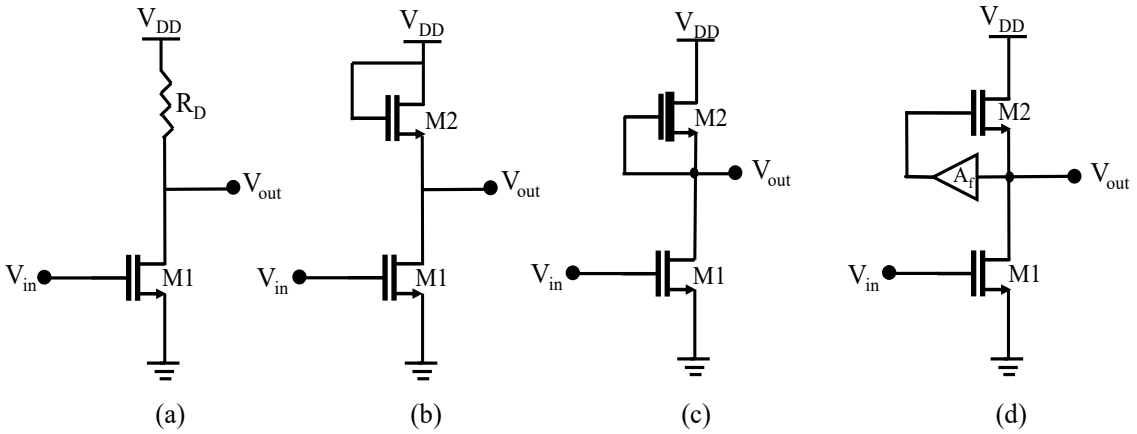


Figure 5.2: CS amplifier with only N-type transistors with (a) Resistive load (b) Diode connected load (c) Depletion load (d) Positive feedback for g_m cancellation of the load.

transistor and the overdrive voltage. Large load resistors are difficult to implement since they occupy large area, increases power consumption, sensitive to process variations and also increases the parasitic.

- **CS amplifier Diode connected transistor**

  The load resistor can be replaced by the transistors working in either saturation or triode region. One of the implementation is diode connected load as shown in Fig. 5.2(b). The gain of this circuit is

$$A_{v2} = -\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \tag{5.2}$$

  If $g_m \gg g_{ds}$, then the gain of this amplifier will be equal to the square root of the aspect ratios of the two transistors.

$$A_{v2} \approx -\sqrt{\frac{(W/L)_1}{(W/L)_2}} = -\sqrt{\frac{W_1}{W_2}} \tag{5.3}$$

  Above equation shows that the gain is proportional to the widths of the transistors when they have same channel lengths. In order to have high gain, width of the driver transistor should be larger than the load transistor. Larger widths can give rise to large parasitic and can limit the bandwidth due to miller capacitance.

- **CS amplifier with Depletion load**

  The depletion load can improve the gain of the amplifier, which can be done by connecting the gate of the load transistor to the source that eliminates the effect of g_m. The circuit

diagram of CS amplifier with depletion load is shown in Fig. 5.2(c). The gain of the amplifier is

$$A_{v3} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}} \tag{5.4}$$

This gain resembles the gain of a CMOS common-source amplifier and is significantly higher than CS amplifier with diode load. However, it consumes more overhead in fabrication since more number of masks are required to fabricate the semiconductor for depletion and enhancement transistors.

- **CS amplifier with feedback**

  In order to enhance the gain (A_{v4}) of the CS amplifier, impact of g_m of load transistor M2 (see Fig. 5.2(d)) can be minimized by making the the feedback network gain (A_f) close to unity as shown in (5.6) [45].

$$A_{v4} = -\frac{g_{m1}}{(1 - A_f)g_{m2} + g_{ds1} + g_{ds2}} \tag{5.5}$$

  The overall gain of the feedback circuit can be made close to 1 by properly sizing the transistors and biasing circuit such that (1-A_f) $g_{m2} \approx 0$ and the gain of the amplifier becomes:

$$A_{v4} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}} \tag{5.6}$$

  This is almost half the intrinsic gain of the input transistor, which can be maximized if the trans-conductance of the driving transistor is maximized while minimizing the output conductance or maximizing output resistance with proper biasing techniques.

- **GAIN ENHANCEMENT TECHNIQUE USING POSITIVE FEEDBACK**

  The feedback method in the previous section can be accomplished using two feedback techniques. Both are positive feedback such that, it enhances the overall output impedance of the network by cancelling the g_m component of the load as described above. The two methods include, using cascaded inverters or a bootstrapping capacitor for the feedback. The details are discussed in below.

  Gain Enhancement Technique with cascade of inverters (method I)

  One of the most commonly used method is cascading of inverters [68] as shown in Fig. 5.3(a) to obtain in phase signals at the source and gate of M2. The feedback circuit (formed by M3 to M6) shows a gain of:

$$A_f = \frac{g_{m3} * g_{m5}}{g_{m4} * g_{m6}} \tag{5.7}$$

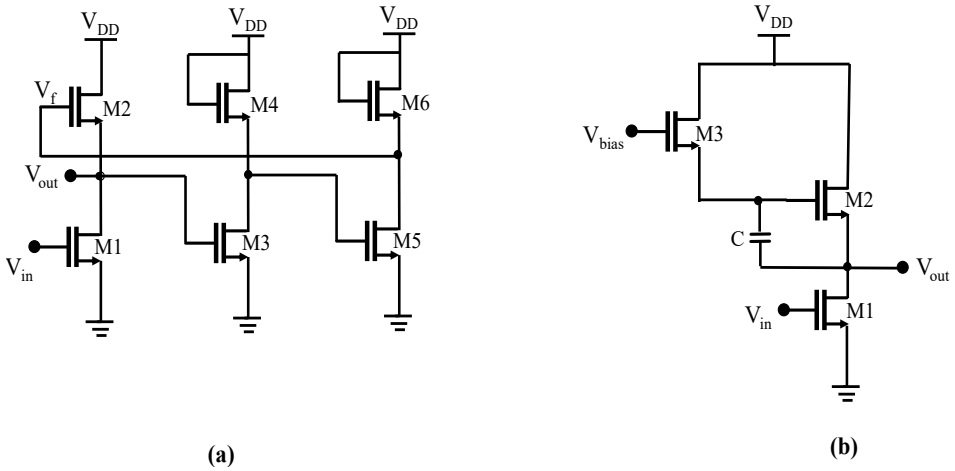


Figure 5.3: Gain enhancement technique with positive feedback using (a) cascading of inverters technique (method I), (b) Capacitive bootstrapping technique (method II).

The feedback gain (A_f) can be made close to 1 by carefully choosing the aspect ratio of the feedback transistors and the biasing currents. Then,

$$V_f = A_f * V_{out} \tag{5.8}$$

and V_{GS} of M2 is

$$V_f - V_{out} = (A_f - 1)V_{out} \tag{5.9}$$

which is approximately equal to zero, when A_f = 1. This results in high active load resistance equal to the output resistance of the transistor and leading to high gain as shown in (5.6).

Gain enhancement with capacitive bootstrapping (method II)

A gain enhancement technique with capacitive bootstrapping [116] is shown in Fig. 5.3(b). The feedback path consists of a bootstrapping capacitor C and a biasing transistor M3. The basic idea is to increase the equivalent active load value to a point, where the global gain gets very close to the gain achieved by standard CMOS based single stage common source amplifier. For proper operation, the transistor M1 and M2 will operate in saturation region while transistor M3 is cutoff. The gain of this circuit is given by [117] the equation:

$$A_{v4} = \frac{-g_{m1}}{g_{m2}(1-A_f)+g_{ds1}+g_{ds2}} \tag{5.10}$$

where, A_f is given by:

$$A_f = \frac{C}{C+C_{eq}} \tag{5.11}$$

where C_{eq} is the parasitic capacitance of the feedback transistor given by:

$$C_{eq} = C_{gs3}+C_{gd2} \tag{5.12}$$

Therefore, the overall gain of the amplifier is directly dependent on the value of the feedback capacitor and the aspect ratio of the feedback transistor. One of the uniqueness of the amplifier with bootstrapped load is that the response shows a bandlimited/bandpass response. i.e. it has both lower and higher cutoff frequencies and the lower cutoff frequency value can be controlled by the aspect ratio of biasing transistors (M5/M6) and the bootstrapping capacitance (C).

- **Proposed high gain amplifier**

  The amplifier that has been used in this work is the positive feedback amplifier because the bootstrapping amplifier shows the bandlimited/bandpass response, which is not suitable for the application that has been focused in this work. Gain enhancement technique with positive feedback using cascading of inverters is used in differential amplifier as shown in Fig. 7.1. The pre-amplifier is self compensated and self biased circuit with common mode feedback (CMFB) as dipicted by M6-M8 and M14-M16. Transistors M1-M4 form a first differential pair. Transistors M5 & M6 and M13 & M14 are the self biasing mirrored transistors with voltages V_{CM1} and V_{CM2} respectively, carrying the currents $I_5 = I_6$. These biasing currents are direct functions of $V_{CM1} = V_{GS5} = V_{GS6}$. V_{CM1} is proportional to the common-mode voltage at nodes A and A', aspect ratios of common-mode sensing and mirror transistors. The gate-drain voltage of mirrored biasing transistors is the source voltage of sensing transistor. This gives rise to a negative feedback system such that any change in output common mode signal variations will be compensated by the biasing circuit. The internal transistors M9-M12 form a positive feedback network while M13 and M14 are the biasing transistors for the feedback network. The common-mode feedback based biasing and compensation of this feedback circuit uses same theory as in the first stage.

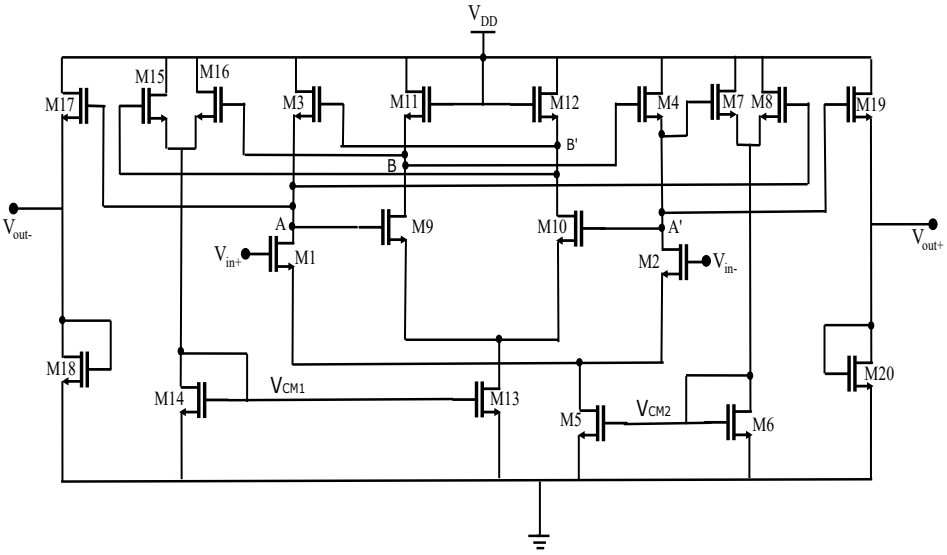


Figure 5.4: Pre-amplifier with positive feedback gain enhancement technique.

From the small signal analysis the gain of the two stages are given by :

$$StageI : A_1 = \frac{g_{m1}}{g_{m3}(1-A_f)+g_{ds1}+g_{ds3}} = \frac{g_{m2}}{g_{m4}(1-A_f)+g_{ds2}+g_{ds4}} \tag{5.13}$$

$$FeedbackStage : A_f = \frac{g_{m9}}{g_{m11}+g_{ds9}+g_{ds11}} = \frac{g_{m10}}{g_{m12}+g_{ds10}+g_{ds12}} \tag{5.14}$$

Transistors M17 & M18 and M19 & M20 forms a source follower in order to have low output impedance and isolate impact of load on the circuit performance. While optimizing for the gain of the amplifier the frequency response and phase should also be taken care to ensure stability (phase margin > 60°). The dominant pole that is presented at the output is due to improved active load resistance with the positive feedback technique.

5.1.1.3 Simulation Results

The simulations of the above mentioned positive feedback amplifier has been done with the in-house IGZO TFT models. The frequency response of the amplifier is shown in Fig. 5.5. The circuit has shown the gain of around 40 dB with Unity Gain-Bandwidth (UGB) of 93 kHz and Common-Mode Rejection Ratio (CMRR) of 80 dB. This bandwidth is more than sufficient for the biomedical analog front end that has been proposed in this work. In addition the circuit consumes 323 μW of power at the power supply of 10 V. The circuit shows the phase margin of 89° and hence ensures good stability. This amplifier is able to amplify the low amplitude

biomedical signals, which can be further processed by other pre-processing blocks even near DC.

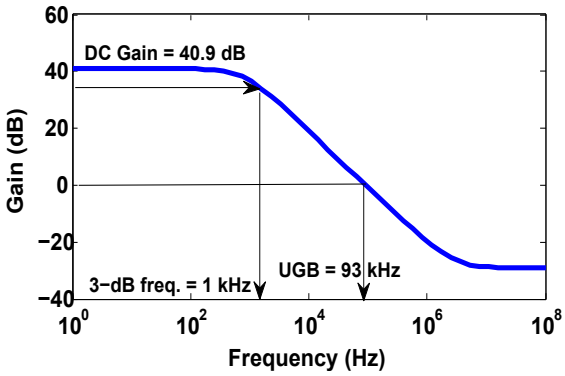


Figure 5.5: Frequency response of positive feedback amplifier.

5.2 Proposed Low Pass Filters

The next pre-processing block is the LPF as shown in Fig. 5.1. LPF or an antialising filter is an important block, as it helps to suppress the high frequency signals. In this section sixth-order fully differential active low pass Resistor-Capacitor (RC) and switched-capacitor (SC) filters using IGZO thin-film transistors are presented for the first time with a-IGZO TFTs. As a first step, a low-gain amplifier using a diode-connected load and a fully differential amplifier is designed with positive feedback based on capacitor bootstrapping. These amplifiers are employed to realize biquads, with which a sixth-order Sallen-Key low-pass RC and SC filters are implemented.

Conventional active filters consist of resistors and capacitors with either transistors or OpAmp(s). Active RC filters are sensitive to temperature and process variations. Further, on-chip resistors occupy huge die area. These drawbacks can be overcome by SC filters, since their performance is a function of ratio of capacitance instead of RC time constants, which are robust against process variations. Although active RC and SC filters have been extensively studied and implemented in CMOS technology [118–120], the work done for filter design is very scarce using oxide TFTs.

Till now, in literature RC biquad was demonstrated using a−Si:H TFTs with a power supply of 25 V [59]. In order to overcome the disadvantage of RC filter, this work proposes 6^{th} order SC biquad at relatively low supply voltage with respect to the state of art work. Differential-Difference Amplifier (DDA) with both high gain and low gain topologies has been used in order to implement 6^{th} order sallen-and-key SC LPF. The circuit simulations have been

carried out in Cadence Virtuoso using in-house IGZO TFT models. In addition, measured results of 2^{nd} order SC biquads with high gain and low gain DDA is also presented.

5.2.1 Circuit Description

5.2.1.1 Active RC Filter

Sallen-and-Key architecture is most widely used since it has a very good gain accuracy. A fully differential architecture has been used for implementing the filter. The main advantage of using differential architecture is that, it provides higher output swing, immunity to common mode noise and reduced even order harmonics[121].

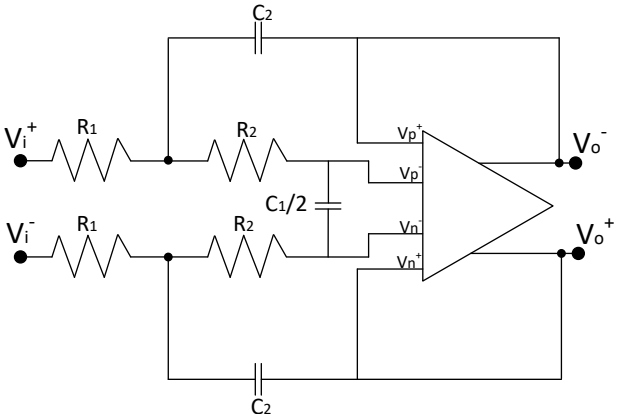


Figure 5.6: Active Differential Sallen-and-Key RC Biquad.

The transfer function of fully differential sallen-and-key RC LPF (see Fig. 5.6) is given by:

$$A = \frac{A_0}{1 + a_i s + b_i s^2} \tag{5.15}$$

where, A_0 is the DC gain, a_i and b_i are the filter coefficients of the biquad, and at unity gain, the coefficients are given by:

$$a_i = \omega_c C_1 (R_1 + R_2) \tag{5.16}$$

$$b_i = \omega_c^2 C_1 C_2 R_1 R_2, \tag{5.17}$$

where, $\omega_c = 2\pi f_c$ and f_c being cutoff frequency of the filter.

A direct design is used for the single-ended filter circuit to determine the value of the resistors upon suitable choice of capacitance by solving the quadratic expression in the denominator of equation 5.15. Feed-forward difference method is used in this work, in order to have a simple architecture with minimal complexity. Capacitances have been chosen in such a way that they do not overload the amplifier. The values are adapted from the single-ended section into fully

differential with an exception for the capacitor C_1, whose value is now halved considering the potential across it is twice that of the single-ended section [120]. The quadratic equation (5.15) is compared to a standard Butterworth polynomial of same order to determine the Butterworth coefficients a and b for a given filter order. The filter coefficients of a standard Butterworth polynomial can be found in Fig. 5.7 [122].

n (order)	Normalized Denominator Polynomials in Factored Form
1	$(1+s)$
2	$(1+1.414s+s^2)$
3	$(1+s)(1+s+s^2)$
4	$(1+0.765s+s^2)(1+1.848s+s^2)$
5	$(1+s)(1+0.618s+s^2)(1+1.618s+s^2)$
6	$(1+0.518s+s^2)(1+1.414s+s^2)(1+1.932s+s^2)$
7	$(1+s)(1+0.445s+s^2)(1+1.247s+s^2)(1+1.802s+s^2)$
8	$(1+0.390s+s^2)(1+1.111s+s^2)(1+1.663s+s^2)(1+1.962s+s^2)$
9	$(1+s)(1+0.347s+s^2)(1+s+s^2)(1+1.532s+s^2)(1+1.879s+s^2)$
10	$(1+0.313s+s^2)(1+0.908s+s^2)(1+1.414s+s^2)(1+1.782s+s^2)(1+1.975s+s^2)$

Figure 5.7: Normalized Butterworth polynomial for low pass filters.

The same can be done for all filter types by comparing the transfer function equation with the characteristic polynomials and its coefficients. This quadratic can be solved for a given value of capacitor satisfying the given condition such that the solution of quadratic is positive real. The condition for the roots to be real is given by:

$$C_2 \geq C_1 \frac{4b_1}{a_1^2} \tag{5.18}$$

Using these values of capacitor values of the resistors are found as below:

$$R_{1,2} = \frac{a_1 C_2 \pm \sqrt{a_1^2 C_2^2 - 4b_1 C_1 C_2}}{4\pi f_0 C_1 C_2} \tag{5.19}$$

Also, the Q-factor of this filter can be calculated as:

$$Q = \frac{w_o}{2\alpha} = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \tag{5.20}$$

where, $w_o = 2\pi f_o$. The filter coefficients, calculated resistors, and capacitor values are presented in Table 5.1.

Higher order filters can be implemented by cascading the individual biquads in increasing order of their Q values such that there is minimum loading in the previous block or to the input of the subsequent filter (see Fig. 5.8). The reason is that, with cascading two or more

Table 5.1: Filter section parameters and Butterworth coefficients

Stages	a_i	b_i	**Q**	f_c **(Hz)**	R_1 **(MΩ)**	R_2 **(MΩ)**	C_1 **(pF)**	C_2 **(pF)**	C_{eq1} **(pF)**	C_{eq2} **(pF)**
I	1.932	1	0.52	500	9.8	51.6	10	20	2.55	0.48
II	1.414	1	0.71	500	13.8	61.2	6	20	1.81	0.41
III	0.52	1	1.93	500	40.9	124	1	20	0.61	0.20

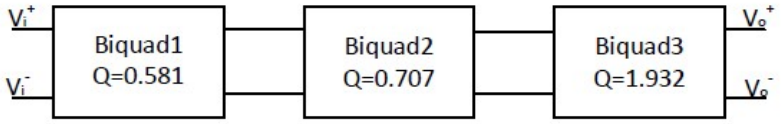


Figure 5.8: Sixth-order filter implementation with a cascade of three biquads.

biquads, the result will no longer resemble Butterworth and results in a cutoff at -6 dB, which can be compensated by considering different Q values. These can be directly derived from the butterworth polynomials (refer Fig. 5.7) to achieve for example, a sixth order butterworth filter with its denominator equation of the form:

$$H(s) = \frac{1}{S^2 + 0.5176s + 1} \frac{1}{s^2 + 1.414s + 1} \frac{1}{s^2 + 1.9319s + 1} \tag{5.21}$$

Each bi-quadratic can be solved to give a filter section with different Q-values. The resistor and capacitor values are calculated for each biquads by solving the quadratic in the butterworth polynomial. Each of these biquads are then implemented with resistor and capacitors with the low-gain and high-gain DDAs. These biquads are cascaded in increasing order of their Q-value to obtain higher order filter. A switched capacitor equivalent of the RC implementation is generated by forward eulers transformation with parasitic insensitive configuration.

5.2.1.2 Active SC Biquad

The transformation from RC to SC is done by a forward difference transformation of the continuous time active RC filter by replacing the resistors with parallel equivalent switched capacitor as shown in Fig. 5.9, in order to have a simple architecture with minimal complexity. The resulted differential SC biquad is presented in Fig. 5.10. It consists of a parallel capacitor with two switches controlled by non-overlapping clocks ($\phi 1$ and $\phi 2$). By properly sizing the capacitor, switch and clock frequency, very large values of resistors can be implemented. The switched capacitor equivalent of the resistor is dependent on the resistor and the clock frequency by T_{clk} = RC.

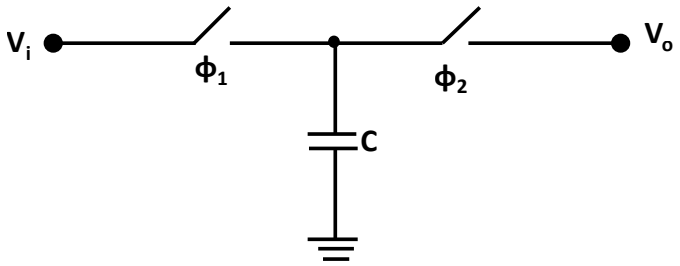


Figure 5.9: Switched-capacitor equivalent of resistor.

The design of switches used in the SC filter plays an important role in the overall performance of a filter. Switches should be designed in such a way that, its resistances should be close to that of an ideal switch.i.e., zero ON resistances and infinite OFF resistance. However, practically we would be able achieve finite resistance when the switch is either 'on' or 'off'. One major drawback of switches in the TFT technology is the unavailability of its complementary device hence switches are implemented with transistor operating in linear region. Due to low mobility, it is challenging to achieve high frequency of operation. Further, these switches tend to show non-linear on-resistance as it is function of V_{in}. Other limitation of the switch includes non-negligible charge injection, clock feed though and compromised output voltage swing due to V_{th} drop. R_{ON} for a MOS transistor in linear region is given by:

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{in} - V_{th})} \tag{5.22}$$

This variable resistance leads to non-linearity in the output. The voltage dependent resistance problem of the NMOS switch along with its swing limit can be overcome by using a transmission gate as a switch, which uses two control signals (normal and its complementary signal). It consists of a NMOS and PMOS transistors connected in parallel. However this is not possible in IGZO technology. Though linear switch can be designed using bootstrapping approach, it leads to increased complexity. Considering yield of the process, the circuit is designed with minimal complexity by trading off with the accuracy or precision of the electrical performance.

5.2.1.3 Fully Differential Amplifiers with IGZO TFTs

1. **Low Gain DDA**

   Fig. 5.11 shows the circuit schematic of low-gain fully differential amplifier with diode-connected load. This circuit provides very low gain as compared with high-gain DDA, which is dictated by the aspect ratios of the driving (M_1 to M_4) and load transistors (M_5

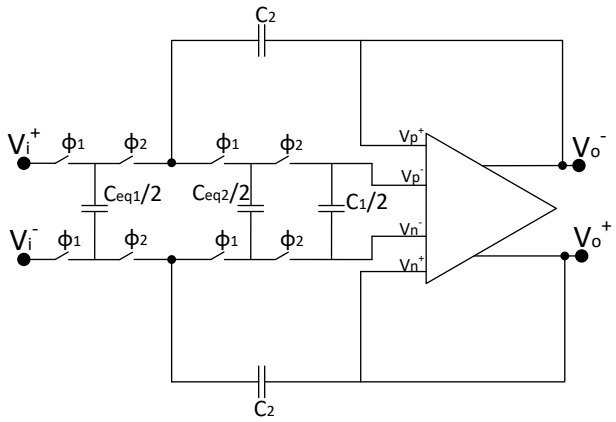


Figure 5.10: Fully differential switched capacitor biquad.

and M_6). Since the Sallen-Key SC filter is independent of the gain of the OpAmp, it is expected to provide similar results with both high-gain and low-gain DDAs. Low-gain DDA consists of three stages. Transistors M_1-M_6 forms differential pair, M_7-M_9 forms the common mode feedback in order to reduce common mode variations, and M_{11}-M_{14} forms a unity gain buffer.

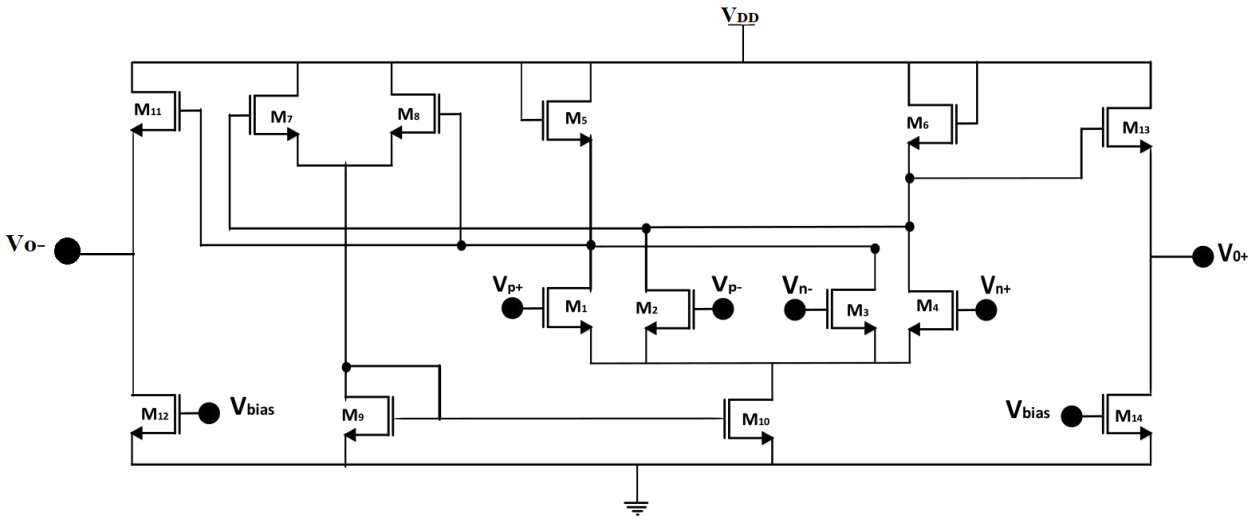


Figure 5.11: Circuit schematic of low- gain differential difference amplifier.

The gain of the amplifier shown in Fig. 5.11 is given by

$$A_v = \frac{g_{m1,2} + g_{m3,4}}{g_{m5,6} + g_{ds1,2} + g_{ds3,4} + g_{ds5,6}} \tag{5.23}$$

2. **High Gain DDA**

The improvement of the low-gain DDA is the high-gain DDA, which is formed by simply replacing the diode-connected load with the capacitive bootstrapping load. A fully differential amplifier circuits based on bootstrapping capacitor is presented in Fig. 5.12, which is used as an active element in the filter. In this amplifier, capacitor C and transistors M_7-M_8 form the positive feedback. For proper operation, transistors M_7 and M_8 operate in cutoff, whereas, other

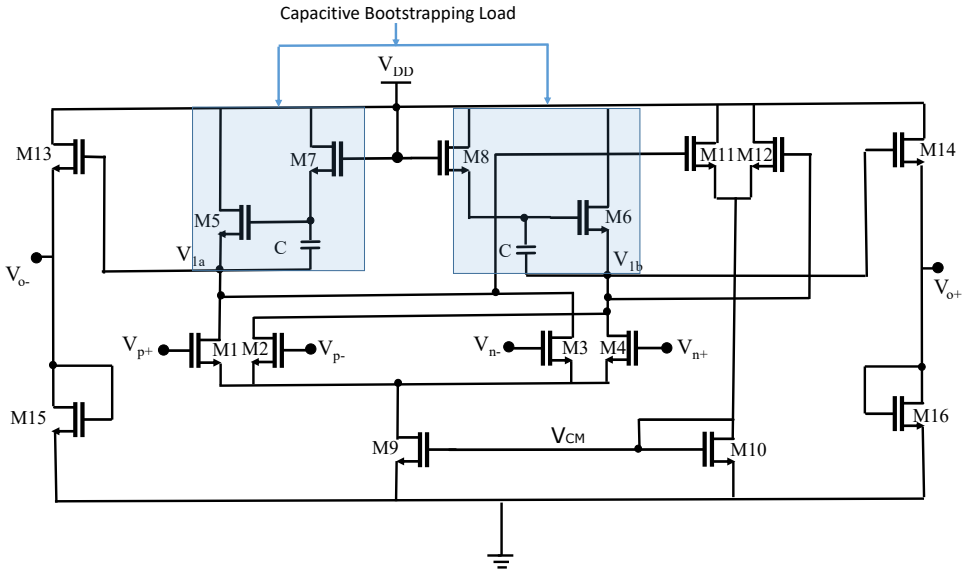


Figure 5.12: Circuit Schematic of High Gain DDA.

transistors are in saturation. A common-mode feedback (CMFB) (shown by M11 and M12 transistors in Fig. 5.12) is to minimize variations in the common mode level of the differential pair output. This gives rise to a negative feedback such that the biasing network will compensate any change in the output common-mode level of the first stage, under ideal conditions or large gain, from the differential difference amplifier (DDA).

$$V_p^+ - V_p^- = V_n^+ - V_n^- \tag{5.24}$$

However, the gain of the DDA is given by:

$$A_v = \frac{V_o^+ - V_o^-}{[(V_p^+ - V_p^-) - (V_n^+ - V_n^-)]} \tag{5.25}$$

For the circuit above the gain of the first stage is:

$$A_v = \frac{g_{m1,2} + g_{m3,4}}{g_{m5,6}(1 - A_f) + g_{ds1,2} + g_{ds3,4} + g_{ds5,6}} \tag{5.26}$$

Table 5.2: Comparison of high-gain and low-gain DDA electrical performance

A. LOW-GAIN DDA		**B. HIGH-GAIN DDA**	
Parameter	**Value**	**Parameter**	**Value**
V_{DD}	**10 V**	V_{DD}	**10 V**
Gain	**5.03 dB**	**Gain**	**53 dB**
GBW	**450 kHz**	**GBW**	**175 kHz**
Power	**0.127 mW**	**Power**	**0.191 mW**

where, the gain of the feedback path A_f as given by :

$$A_f = \frac{C}{C + C_{eq}} \tag{5.27}$$

where, C_{eq} is the parasitic capacitance of the feedback transistor given by:

$$C_{eq} = C_{gs7,8} + C_{gd5,6} \tag{5.28}$$

For DC, the bootstrapping capacitance C acts as an open circuit, and the gate current of $M_{5,6}$ is very small and there is a high impedance path. Therefore, $M_{7,8}$ are being operated in cutoff. In equation 5.8 C_{eq} depends on aspect ratio of the biasing transistors (M7 and M8). This circuit shows a band-limited/band-pass response, i.e, it has both lower and higher cutoff frequencies. The lower cutoff frequency is due to the high-pass filter action formed by the biasing transistors (M_7 and M_8) and bootstrapping capacitors (C); however, this lower cutoff frequency can be set close to zero by employing large C and biasing TFTs of small dimensions. By comparing equations 5.23 and 5.26, it can be clearly noticed that the gain provided by the capacitive bootstrapped amplifier is higher as compared with low-gain DDA.

5.2.2 Simulation and Measured Results

5.2.2.1 Simulation Results

The circuit simulations have been carried out using in-house models [42, 48]. For the **Low-Gain DDA** (see Fig. 5.11), the frequency response is shown in Fig. 5.13. The gain provided by this amplifier is 5.03 dB. CMRR obtained for this amplifier is around 65 dB. The amplifier performance metrics are shown in Table 5.2, which shows low-gain but higher GBW. However, it consumes less power as compared with high gain DDA as it does not consist of gain enhancement topology.

For the amplifier topology **High-Gain DDA** (see Fig. 5.12), the first differential gain stage contributes high gain as well as the dominant pole. Therefore, the design is aimed at optimizing

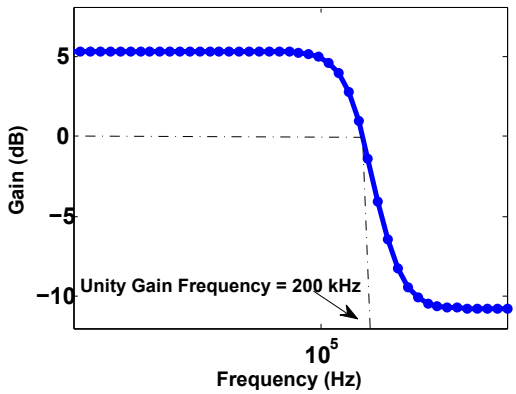


Figure 5.13: Frequency response of low gain DDA with diode connected load.

the gain, phase, and gain bandwidth (by changing the widths of C and M7/M8 transistors) at this stage. The second stage is a buffer with slightly less than unity gain, which is meant for isolating loading effect on the amplifier response. The frequency response of the amplifier is shown in Fig. 5.14, which shows a gain around 53 dB. CMRR obtained for this amplifier is around 83 dB. The amplifier performance metrics are presented in Table 5.2. It can be inferred

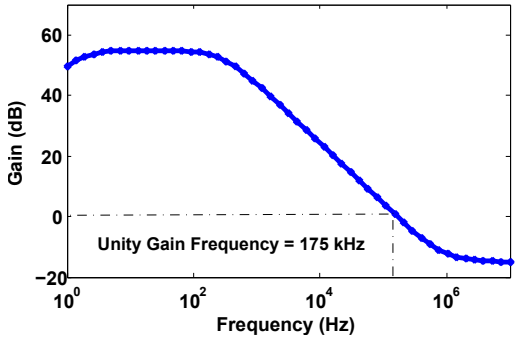


Figure 5.14: Frequency response of differential amplifier with capacitor bootstrapping load.

from the Table 5.2 that the capacitive bootstrapped load increases the gain of the amplifier but it decreases BW, which is mainly arising due to the high active load impedance, which places the dominant pole close to origin.

These amplifiers are employed in the sixth-order Sallen-Key RC and SC low-pass filter, which is presented in Fig. 5.6 and Fig. 5.10. The design of the filter follows standard design steps for a sixth-order Butterworth response. The Butterworth coefficients along with the calculated resistors and capacitors are shown in Table 5.1. There is a trade-off among resistance, capacitance, and clock frequency for the SC implementation. The values are properly chosen in order to maintain the clock frequency much larger than the signal or 3-dB cutoff frequency of the filter.

The frequency response of **RC and SC biquads with low-gain DDA** is presented in Fig. 5.15 (a) and (b) respectively. Their corresponding spectrum is shown in Fig. 5.15 (c) and (d). Similarly frequency response of **RC and SC biquads with high-gain DDA** is presented

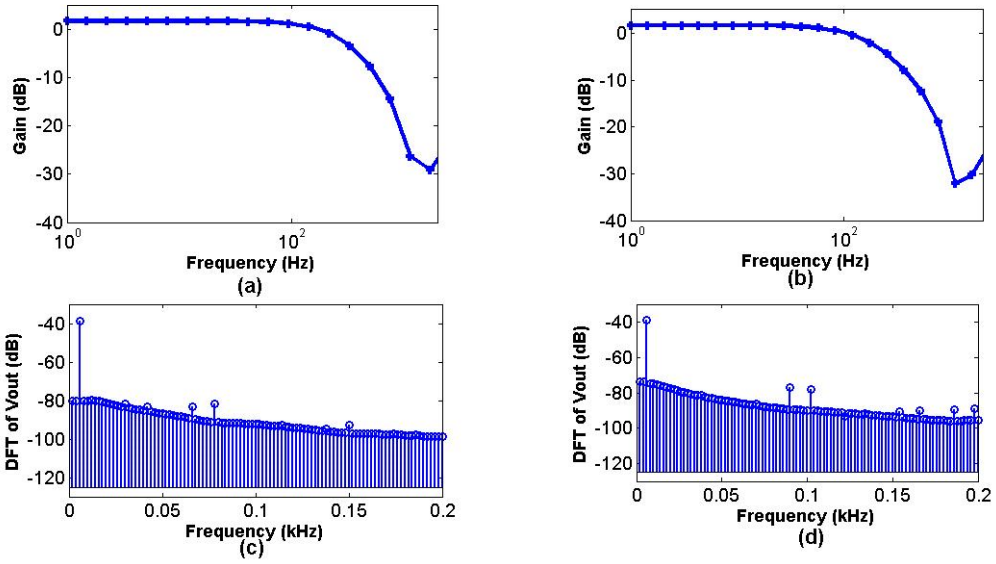


Figure 5.15: Response of biquads with low-gain DDA (a) RC frequency response (b) SC frequency response (c) RC DFT plot (d) SC DFT plot.

in Fig. 5.16 (a) and (b) with the corresponding spectrum in Fig. 5.16 (c) and (d) respectively.

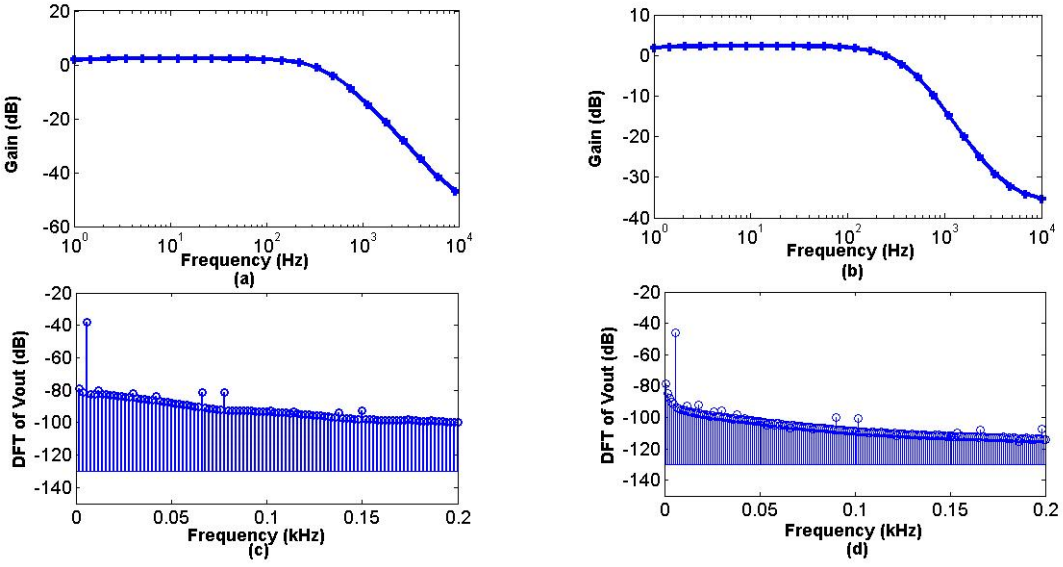


Figure 5.16: Response of biquads with high-gain DDA (a) RC frequency response (b) SC frequency response (c) RC DFT plot (d) SC DFT plot.

Similar responses for sixth-order filter with low-gain and high-gain DDA are presented in Fig. 5.17 and Fig. 5.18, respectively.

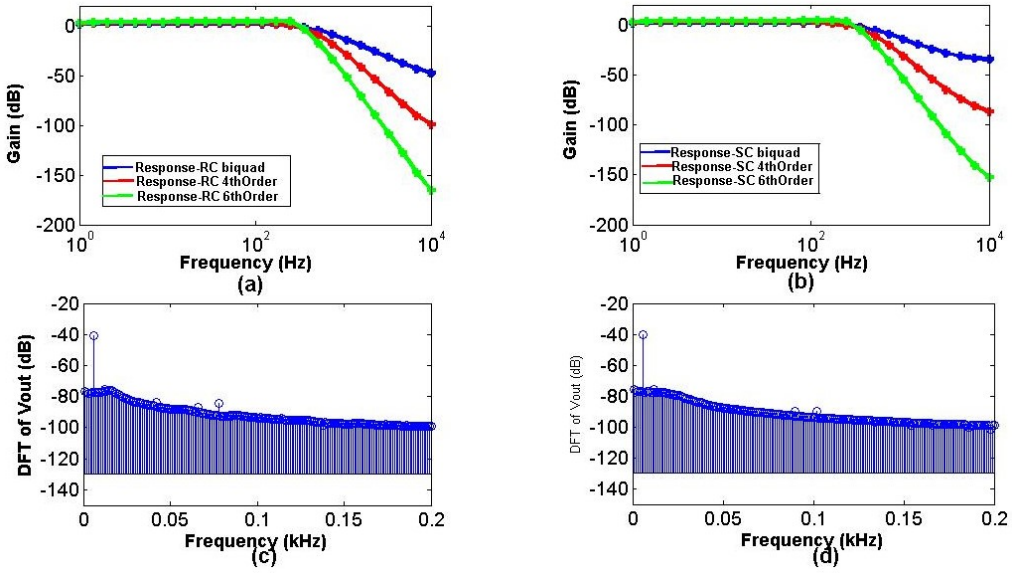


Figure 5.17: Response of sixth-order section (low gain) (a) RC frequency response (b) SC frequency response (c) RC DFT plot (d) SC DFT plot.

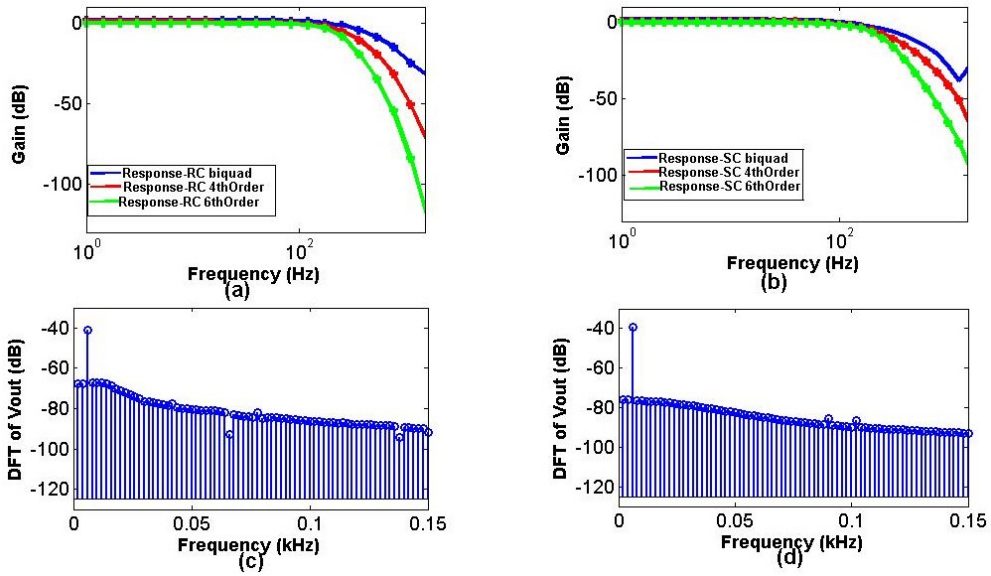


Figure 5.18: Response of sixth-order section (high gain) (a) RC frequency response (b) SC frequency response (c) RC DFT plot (d) SC DFT plot.

From these figures, an increment in the roll off of the gain with respect to the increasing order of the filter can be noticed. There is a gradual increment in the harmonic distortion

from the biquad to sixth-order section due to non-linearity of the devices, as it can be noticed from Fig. 5.15 (c), (d), Fig. 5.16 (c), (d), Fig. 5.17 (c), (d) and Fig. 5.18 (c), (d) with both the OpAmps. Cutoff frequencies obtained for all these filters (biquad and six-order) with low-gain and high-gain DDA can be observed from Table 5.3. It is worth to notice that these cutoff frequencies are different from the expected value (500 Hz), which is due to non-idealities of the opamps and NMOS switches, These circuits have been tested with an input frequency of 60 Hz. It can be noticed from the DFT spectrum that the maximum amplitude is achieved at the input frequency of the filters (Biquad and sixth-order) response from circuit simulations are presented in Table 5.3, when they are implemented with low-gain and high-gain DDA. Switching from the RC filter topology to a switched capacitor filter has shown slight improvement in terms of linearity as evident from Table 5.3, which is due to absence of resistor that gives thermal noise and are sensitive to process variations. The filter parameters obtained from PSS, PAC, and transient analysis simulations of the circuits are shown in Table 5.3 for low-gain and high-gain DDA.

The 3-dB frequency, THD (Total Harmonic Distortion), and SFDR (Spurious Free Dynamic Range) of both the filters are nearly same, when they are implemented with low-gain and high-gain OpAmps, as Sallen-Key filter response is almost independent of the amplifier gain. The power consumption of RC and SC biquad is almost same because of the presence of same active components, i.e., amplifier with capacitive bootstrapping in both the circuits, which consumes most of the power. This is true for the low-gain DDA with diode-connected load, which consumes less power when compared with the high-gain DDA. It should be noticed that the last column in this table has presented simulation results [59] for a fair comparison with the current work. It can be inferred from the table that current designs are able to work with relatively low power supply voltage compared to [59], resulting in reduced power consumption. Further, better THD and SFDR are also observed, implying superior performance in terms of linearity.

Table 5.4 shows the simulation results with respect to PVT variations. The electrical performance variations of SC biquad has been compared with RC biquad. It can be noticed from the table that SC (RC) biquads show variation in the cutoff frequency of 8% (75%) with process corners, 6% (15%) variations with power supplies variations and 13% (50%) variations with temperature. Clearly, it can be observed that SC biquad shows robust performance compared to RC counterpart. In order to make SC biquad further insensitive to PVT variations, more complex techniques need to be investigated and adapted in the circuit, which can increase the complexity and power consumption [123, 124].

Table 5.3: Outcome of filters and comparison

Parameter Technology	**RC Biquad (Low Gain)**	**RC Biquad (High Gain)**	**SC Biquad (Low Gain)**	**SC Biquad (High Gain)**	**RC Sixth-order (Low Gain)**	**SC Sixth-order (Low Gain)**	**RC Sixth-order (High Gain)**	**SC Sixth-order (High Gain)**	**Other work [59]**
TFT Technology	IGZO (20 μm)	IGZO (20 μm)	IGZO (20 μm)	IGZO (20 μm)	IGZO (20 μm)	IGZO (20 μm)	IGZO (20 μm)	IGZO (20 μm)	a-Si:H (8 μm)
V_{DD} **(V)**	10 V	10 V	10 V	10 V	10 V	10 V	10 V	10 V	25 V
Pass-band Gain (dB)	-0.07	-0.1	-0.12	-0.19	-0.15	-0.5	-0.17	-0.65	-0.12
f-3 dB (Hz)	200	312	186	285	220	273	218	272	150
THD (dB)	-40.1	-40.98	-40.9	-41.52	-30.2	-31.35	-30.92	-31.41	-28.48
SFDR (dB)	39.9	40.92	40.1	40.57	29.89	30.08	30.12	32.24	28.5
Power (mW)	0.154	0.191	0.154	0.191	0.456	0.537	0.456	0.537	3.7

Table 5.4: PVT variations of Biquads

VARIATIONS	**PROCESS**			**VOLT. (V)**			**TEMP. (C)**		
PARAMETERS	**TT**	**SS**	**FF**	**9.5**	**10**	**10.5**	**15**	**25**	**85**
RC BIQUAD	329 Hz	233 Hz	567 Hz	371 Hz	329 Hz	297 Hz	275 Hz	329 Hz	587 Hz
SC BIQUAD	295 Hz	276 Hz	320 Hz	312 Hz	295 Hz	287 Hz	261 Hz	295 Hz	321 Hz

5.2.2.2 Measured Results

1. SC Biquad with High Gain DDA

Fig. 5.19 shows the micrograph of SC biquad with high gain DDA. Fig. 5.20 shows both the

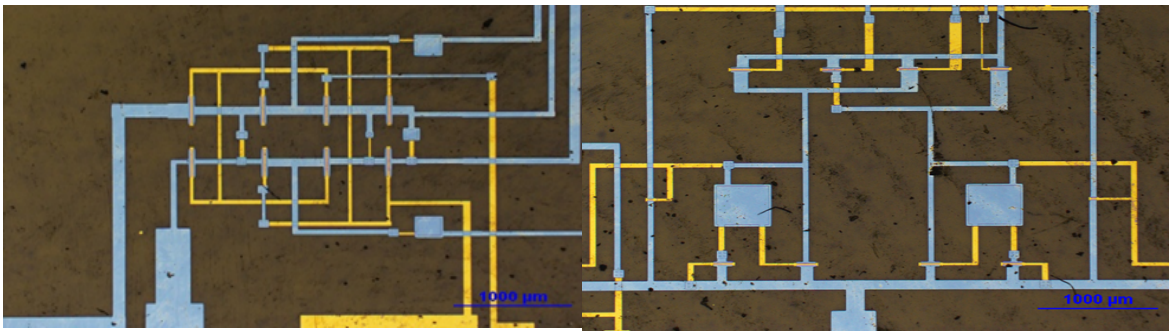


Figure 5.19: Micrograph of SC biquad with high-gain DDA.

simulated and measured results of SC sallen-and-key LPF with high gain DDA. The sampling frequency of the circuit is 40 kHz and input signal frequency has been swept from 10 Hz to 15 kHz. The circuit has shown a power consumption of 336 μW with a supply voltage of 10 V. From measurements under normal ambient conditions the 3-dB frequency was observed to be 155 Hz, which makes it suitable for biomedical applications. It can be observed from Fig. 5.20 that the roll off rate and 3-dB frequency are decreased as compared to simulation results. The differences in simulated and measured response could be due to the non-ideal effects of switches, such as, charge feed through/clock feed through problem, parasitics due to interconnects, non-linear on resistance of the switch and limitation in the measurement setup, especially at low output voltage.

It is worth to note that these IGZO TFTs are not showing significant degradation in the electrical performance, when the bending radius is $\geq$ 15 mm [48]. Since the electrical performance is not changing for individual devices under these conditions, the cut-off frequency of the proposed circuit is expected to remain almost the same.

Only one work has been proposed with oxide TFT in the case of sallen-and-key biquadr [59]. Table 5.5 shows the comparison of the proposed work with the state of art work from measurements. It can be noticed from the table that there is a significant improvement in 3-dB frequency and power consumption is almost one order lower [59]. In addition, the proposed circuit eliminates the disadvantage of using resistors, which occupy large active area. Though the V_{DD} is relatively high, it should be noted that the current levels of the devices (oxide TFTs) are low due to low mobility ($< 30cm^2$/V.S). Therefore the circuit contributes relatively low

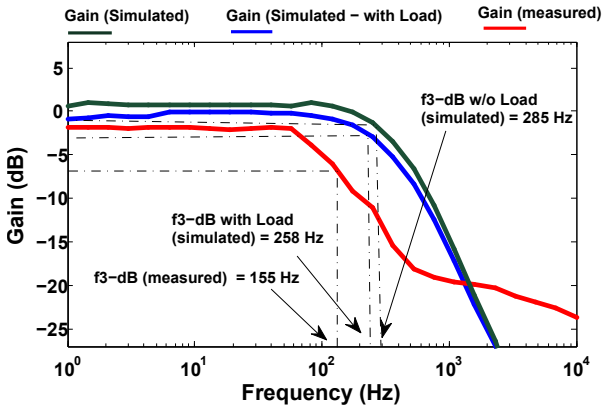


Figure 5.20: Simulated and Measured response of SC biquad with high-gain DDA.

Table 5.5: Comparison with the state of art work

S.No.	Parameters	Previous Work (RC Biquad)[59]	This work (SC Biquad)
1.	TFT Technology	a-Si:H TFT	a-IGZO TFT
2.	VDD (V)	25 V	10 V
3.	Passband Gain (dB)	4.9	-1.98
4.	f-3dB (Hz)	0.3	155
5.	Power (mW)	9.5	0.336

power (V_{DD}*I_{DD}), making oxide TFT based circuits to open a window for wearable bio-medical applications. However, low-power design techniques needs to be investigated and the design needs to be modified to minimize the power consumption further.

2. SC Biquad with Low Gain DDA

Fig. 5.21 shows the micrograph of SC biquad with low gain DDA.

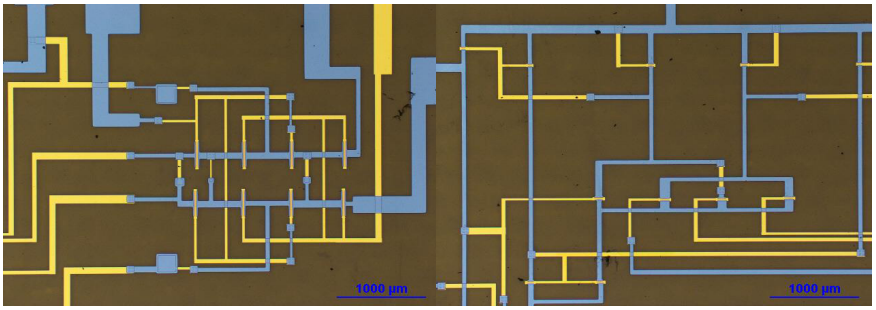


Figure 5.21: Micrograph of SC biquad with Low-gain DDA.

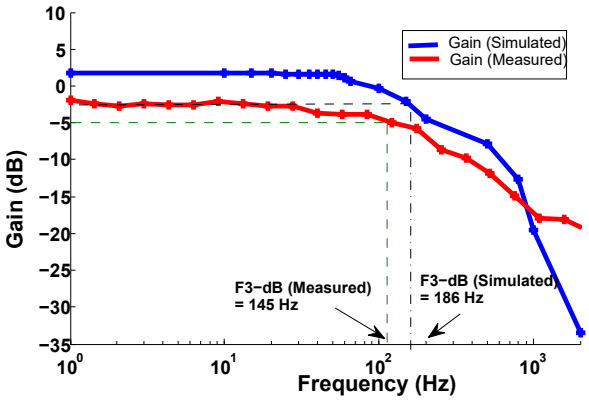


Figure 5.22: Simulated and Measured response of SC biquad with low-gain DDA.

Fig. 5.22 shows both the simulated and measured results of SC sallen-and-key LPF with low gain DDA. The circuit has been tested with the clock frequency of 40 kHz. The TFTs in this batch have a turn on voltage of -6 V. Because of this the amplitude of clock has been chosen from -6 to 4 V. The input is swept from 1 to 30 kHz during the measurement. The power consumption of this circuit is 435 μW. Similar to the SC biquad with high gain DDA, the roll off rate and 3-dB frequency are decreased as compared to simulation results due to the same non-idealities as explained for high-gain DDA based design.

5.3 Conclusions

The pre-processing block consists of two circuits. One is pre-amplifier and other is LPF. In this chapter different pre-amplifiers have been highlighted with oxide TFT technology and the novel SC filter has been proposed.

The positive feedback pre-amplifier has been successfully used in this work in order to amplify the low amplitude biological signals with common mode feedback to make the circuit performance robust against process variations.

On the other hand, a sixth-order Sallen-Key RC and SC low-pass filters with Butterworth response are illustrated for the first time using a-IGZO TFTs with a power supply of 10 V. Design of amplifiers (low-gain DDA with diode-connected load and fully differential amplifier configuration with capacitive bootstrapping) in the filter is also presented. The low-gain DDA provides the gain of about 5 dB while the fully differential amplifier (DDA) is accomplished to give gain above 40 dB. Using these OpAmps, a sixth-order RC and SC filter is designed and simulated. The response of these filters is nearly same, as Sallen-Key topology response is almost independent from the amplifier gain. It is worth to notice that the sixth-order LPFs

have shown low power consumption when they employed low-gain amplifier compared with high-gain amplifier-based design, without compromising on other performance metrics.

In addition, measured results of sallen-and-key LPF with high gain and low gain DDA is also presented in this work for the first time. It can also be noticed that the biquad have shown cut-off frequency of 200 Hz (with high gain DDA) and 145 Hz (with low gain DDA), with the power consumption of 336 μW and 435 μW respectively, without compromising on the performance metrics. The proposed filters would find potential applications in large area flexible electronics, mainly in biomedical systems.

Chapter 6

Novel Analog-to-Digital Converters for Biomedical Applications

After pre-processing of the biological signals, the next important block in the biomedical front end is Analog to Digital Converter (ADC) as shown in Fig. 6.1. ADC helps to convert the analog signal to the digital bit-streams, which can be further transferred through a communication protocol (Bluetooth or Zigbee or Wifi) to a mobile or server so that the biological signals can be monitored in real-time.

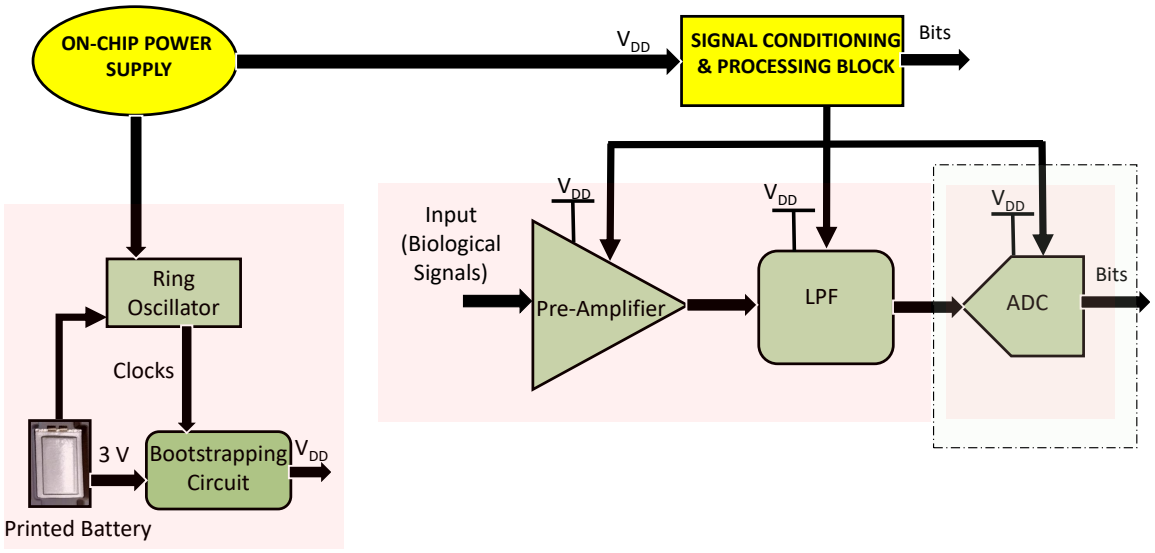


Figure 6.1: Biomedical analog front-end with ADC (highlighted).

The mobility of the oxide TFTs are one order lower as compared to CMOS. Further, complementary device is not available for circuit design. Therefore it is quite challenging to achieve a reasonable resolution ($\geq$ 11 bits) for biomedical applications [62, 125] with Nyquist ADCs. A few examples can be found, such as a four-bit counting type ADC [126], a six-bit SAR (the digital logic is implemented in FPGA) [127] with complementary organic TFTs, a five-bit flash ADC with n-type a-Si:H TFTs [128].As it can be noticed from the state of the art [64, 65], ENOB is limited to 9 bits, which is not sufficient for biomedical applications. In oder to address this challenge, current work employed oversampling data converter (delta sigma ADC). This architecture can ensure better resolution due to noise shaping ability. This work proposed two delta sigma ADCs to obtain a resolution $\geq$ 11 bits. In these designs, comparators are critical blocks that dictates the overall performance. Therefore, this work proposed five novel comparators. The design and implementation details of all these circuits (comparators and ADCs) are explained in the following sections.

6.1 Delta Sigma ADC

In this section a brief introduction to the oversampling ADC, namely, delta sigma (Δ-Σ) ADC is discussed. These converters combine an analog sigma delta modulator with a more complex digital filter.

6.1.1 Working of ADC

The block diagram of first order delta-sigma ADC is shown in Fig. 6.2 [129]. The name first order comes from the fact that there is only one integrator in the feed-forward path. The input signal x(t) is applied into the modulator via a summing junction, which is then passed through the integrator and applied to a comparator that acts as a one-bit quantizer. The comparator output is then fed back to the input summing junction via a one-bit digital-to-analog converter (DAC). When the comparator output is positive, the DAC feeds back a positive reference signal, which is subtracted from the input signal in order to change the integrator output to the negative direction. Similarly, when the comparator output is negative, the DAC feeds back the negative reference signal, which is added to the incoming signal. The integrator accumulates the difference between the input and the quantized output signals and tries to maintain the integrator output around zero [111, 130].

Following are the two main important features in Δ-Σ ADC's operation:

- **Oversampling:** According to the sampling theorem, the sampling frequency of the signal must be at least twice the signal frequency in order to reconstruct the sampled signal

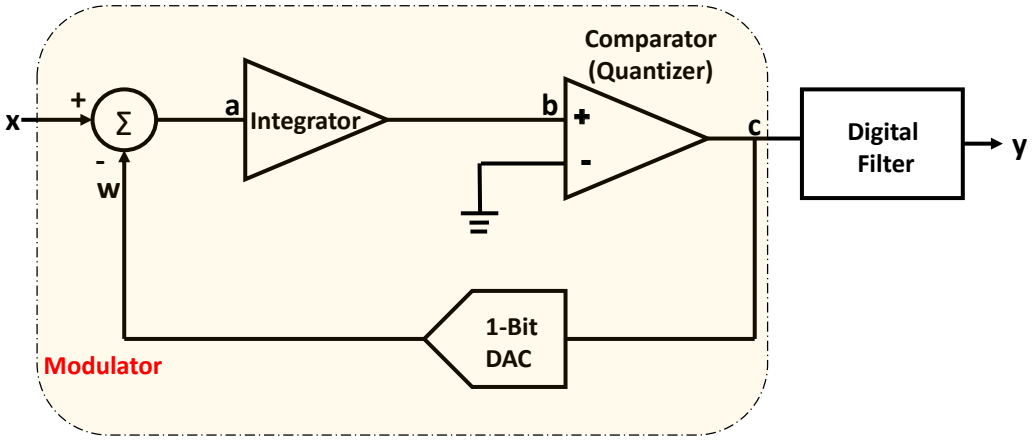


Figure 6.2: Block diagram of first order Δ-Σ ADC.

[129, 131]. When the signal is sampled its input spectrum is mirrored around integer multiples of sampling frequency (f_S). Fig. 6.3(a) shows the spectrum of the sampled signal when the sampling frequency $f_S < 2f_N$ (where, f_N is input signal bandwidth). The shaded area shown in the plot is referred as aliasing. When the signal is reconstructed from this aliasing, the resultant signal is always distorted. To avoid this aliasing effect, the sampling frequency should be much higher than the Nyquist rate, which can be achieved by oversampling the signal [132]. The oversampling process ensures the entire input bandwidth to be less than $f_S/2$ and avoids the aliasing trap as shown in Fig. 6.3(b) [129, 133].

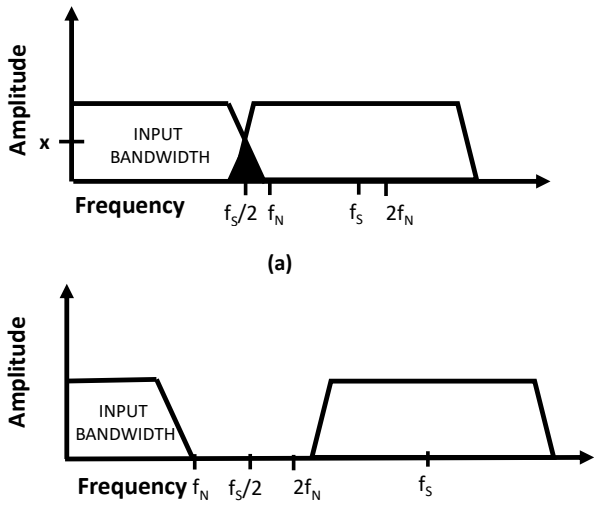


Figure 6.3: Spectrum of (a) under-sampled signal, (b) over-sampled signal.

- **Noise Shaping:** The quantization noise or the quantization error ilimits the dynamic range of an ADC [134]. This error occurs during quantization process, when the signal amplitude level is the rounded-off. For, example consider a 2-bit ADC with a 3 V full scale value. The inputs applied to the ADC are 0 V, 1 V, 2 V and 3 V, whose corresponding outputs are 00, 01, 10 and 11 respectively. If an input of 1.75 V is applied to this ADC, the resultant output will be 10, which actually corresponds to an input of 2 V. The 0.25 V error that occurs during the quantization process is called as quantization error. This error can be treated as random or white noise. Therefore, the quantization noise power and RMS quantization voltage of an A/D converter are given by the following equations [135, 136]:

$$e_{RMS} = \frac{q}{\sqrt{12}}[\mathrm{V}] \tag{6.1}$$

where q is the quantization interval or LSB size.

A quantized signal sampled at frequency f_S has all of its noise power folded into the frequency band of $0 \leq \mathrm{f} \leq f_S/2$. The spectral density of the noise is given by:

$$E(f) = e_{RMS}(\frac{2}{f_S})^{\frac{1}{2}}[\frac{\mathrm{V}}{\sqrt{\mathrm{Hz}}}] \tag{6.2}$$

Converting this to noise power by squaring it and integrating over the bandwidth of interest (f_N), the following result is obtained:

$$n_0 = e_{RMS}(\frac{2f_N}{f_S})^{\frac{1}{2}}[\mathrm{V}] \tag{6.3}$$

where, n_0 is the in-band quantization noise. The quantity $f_S/(2f_N)$ is the Oversampling Ratio (OSR). It is important to note that equation (6.3) shows that oversampling reduces the in band quantization noise by the square root of the OSR.

Δ-Σ ADC Quantization Noise: The above sampling and noise theory can be used to show how Δ-Σ modulator shapes the quantization noise. From the Fig. 6.4 the difference equation for the output of the modulator is given by by [129, 133, 137]:

$$y_i = x_{i-1} + (e_i - e_{i-1}) \tag{6.4}$$

The output of the modulator is equal to the input plus the quantization noise ($e_i - e_{i-1}$). This formula shows that the quantization noise is the difference between the current quantization error (e_i) and the previous quantization error (e_{i-1}).

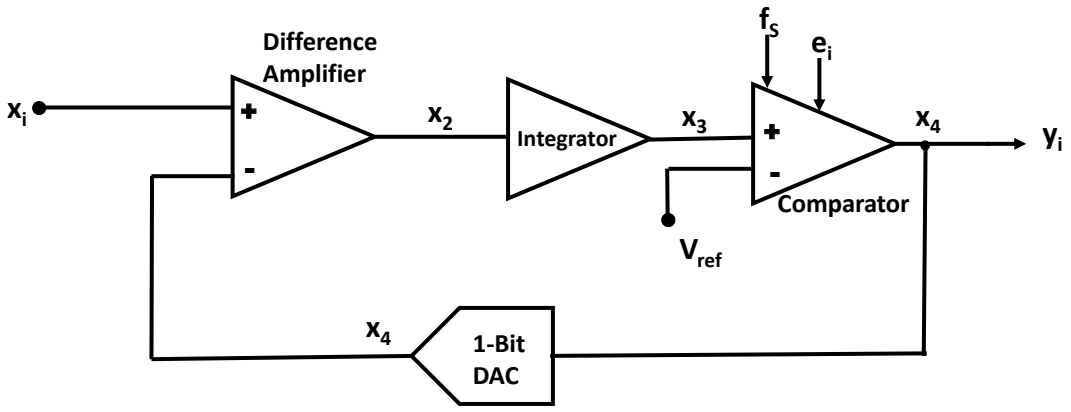


Figure 6.4: Block diagram of sampled data equivalent of first orderΔ-Σ ADC.

Assuming the input signal is active enough to treat the error as white noise, the spectral density of the noise (n_i = e_i - e_{i-1}) can be expressed as:

$$N(f) = E(f) \mid (1 - e^{(-jw/f_S)}) \mid = 2e_{RMS}(\frac{2}{f_S})^{\frac{1}{2}} sin(\frac{w}{2f_S}) \tag{6.5}$$

The noise power in the bandwidth of interest is given by:

$$n_0^2 = e_{RMS}^2 \frac{\pi^2}{3}(\frac{2f_N}{f_S})^3 [\mathrm{V}^2] \tag{6.6}$$

Or,

$$n_0 = e_{RMS} \frac{\pi}{\sqrt{3}}(\frac{2f_N}{f_S})^{\frac{3}{2}} [\mathrm{V}] \tag{6.7}$$

From the above equation it can be inferred that by increasing f_S (which increases OSR) by a factor of 2 will decrease the in-band noise by 9 dB.

Similarly, for the second order delta sigma modulator the noise is:

$$= e_{RMS} \frac{\pi^2}{\sqrt{5}}(\frac{2f_N}{f_S})^{\frac{5}{2}} [\mathrm{V}] \tag{6.8}$$

and that increasing f_S by a factor of 2 decreases the in band noise by 15 dB. Noise for M_{th} order modulator is given by,

$$n_0 = e_{RMS}^2 \frac{\pi^M}{\sqrt{2M+1}}(\frac{2f_N}{f_S})^{M+\frac{1}{2}} [\mathrm{V}] \tag{6.9}$$

From above it can be noticed that doubling the OSR will decrease the in-band quantization noise by 3(2M+1) dB.

Fig. 6.5 [129, 134] presents the relation between signal-to-noise ratio (SNR) and OSR for 1st, 2nd and 3rd order modulators. As it can be noticed, higher order modulators and OSR improve SNR and hence resolution of the ADC, as per((6.9)). However, higher order delta sigma ADCs lead to increased complexity. As a tradeoff, this work focus on second order ADC with a OSR of 100 for active Δ-Σ ADC and 66 for passive Δ-Σ ADC.

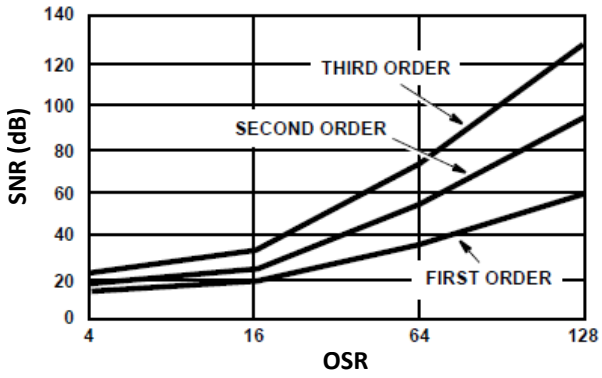


Figure 6.5: Graph between SNR vs OSR of delta sigma modulator.

The noise spectrum of the nyquist type ADC is shown in Fig. 6.6(a) [129, 133]. The SNR of these converters is given by:

$$SNR = (6.02N + 1.76)dB \tag{6.10}$$

where, N denotes effective number of bits or resolution of the ADC.

Fig. 6.6(b) shows the effect of oversampling. It can be seen that $f_S/2$ is much greater than f_N and the quantization noise is spread over a wide spectrum. The total quantization noise is still the same but the quantization noise in the bandwidth of interest is greatly reduced. The SNR of the oversampled ADC is given by:

$$SNR = (6.02N + 1.76) + 10Log_{10}(\frac{f_S}{2f_N})dB \tag{6.11}$$

where, f_N is the maximum frequency of interest.

The quantization noise of the oversampled Δ-Σ modulator is shown in Fig. 6.7 [111, 129, 130]. The total quantization noise of the converter is still the same as in Fig. 6.6(a), but the in-band quantization noise is greatly reduced. Therefore the oversampling converter can ensure better resolution than nyquist converter.

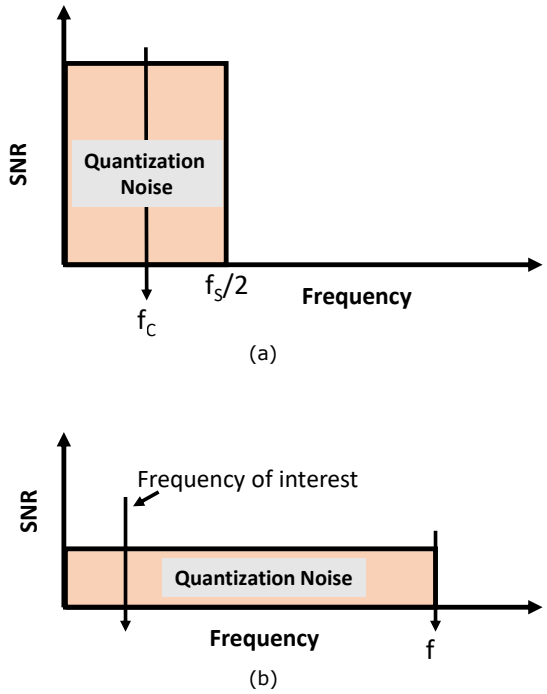


Figure 6.6: Spectrum of quantization noise of (a) Nyquist converter. (b) Oversampled Converter.

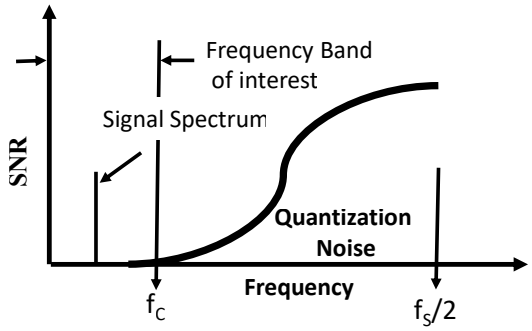


Figure 6.7: Spectrum of quantization noise of oversampled 1^{st} order delta sigma modulator.

Comparator is an important block in the Δ-Σ ADC, which dictates the overall performance of the converter. Consequently, various novel comparators have been designed and implemented, which are able to show beyond state-of-the-art performance. Then, one comparator among the proposed designs with optimum performance is chosen to implement the ADC. The next section presents design details of comparator circuits.

6.2 Comparator Designs

Comparator design with TFTs are scarce [138–140]. Work reported in [138] shows a comparator with oxide TFTs, operating at 20 V power supply with poor output swing (logic 1 and logic 0 around $V_{DD}/2$ and 5 V, respectively) and significant power consumption. Whereas, [140] shows simulation results of comparator with limited swing at the output of around 8 V. On the other hand, [139] presents a comparator with organic TFTs operating at very low clock frequencies of around 500 Hz and significant power consumption ($\approx$ 0.15 mW) with a power supply of 20 V.

It should be noted that the circuits for biomedical applications should consume low power and are able to work at relatively low power supply voltages. There is a big gap in the literature [138, 139] to meet these requirements. Then, this work proposes novel high performance dynamic comparator designs, which are specially designed for flexible biomedical applications. Being the most relevant and active block of delta-sigma ADC, five different types of comparators are designed and the best one has been used in the ADC.

Following are the details of all the five comparators that are designed with a-IGZO TFTs:

1. **Comparator 1** - It consists of one pre-amplification stage, one regenerative flip flop and a NAND based SR latch.

2. **Comparator 2** - Change in this comparator as compared to comparator 1 is the addition of one pre-amplification stage. It consists of two positive feedback Pre-amplifier, positive feedback latch with reset and SR latch.

3. **Comparator 3** - This circuit employs a novel latch with built-in pre-amplifier to obtain low-power consumption. Typically dynamic comparators employ two phase clocks in order to perform reset and latching operation. The proposed comparators uses only a single clock to perform both these operations.

   The main difference between the rest three proposed comparators (comparator 4 and 5) is in the inverter topologies, which is used for the latching operation. Comparator 3 uses conventional NMOS diode load based inverter topology.

4. **Comparator 4** - Employs Pseudo-CMOS based inverter topology to obtain better voltage swing.

5. **Comparator 5** - Employs Pseudo-CMOS Bootstrapped based inverter topology to obtain almost complete rail-to-rail swing.

6.2.1 Circuit Design

The complete circuit description of all the comparators are explained below.

6.2.1.1 Comparator 1 and Comparator 2

The mobility of the oxide TFTs are low compared to CMOS leading to very low-speed designs. In order to address this limitation, a high-speed architecture is used, which typically employs a pre-amplifier to build up the input change to a sufficiently large value and a latch to discriminate levels through positive feedback. Typically, just usage of pre-amplifier alone is not sufficient to ensure the desired output. Similarly usage of only latch takes long time for decision making,

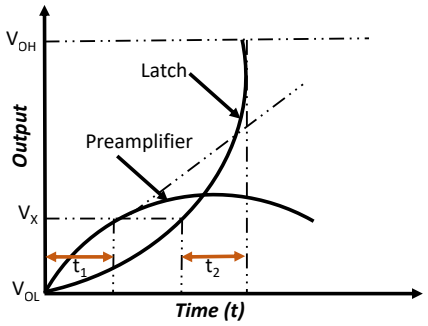


Figure 6.8: Pre-amplifier and latch step response.

especially when the differential input signal values are low in amplitude, resulting in low speed operation as it can be noticed in Fig. 6.8 [130]. In order to address this issue, in high speed design, it is common practice to use latches preceded by pre-amplifier so that the pre-amplifier boosts the signal level to a reasonable value (V_x in time t_1), where the positive feedback in the latch can be effective to to discriminate states (V_{OH}/V_{OL} in time t_2). There the effective response time is reduced to $t_1 + t_2$.

Comparator 1 (Fig. 6.9(a)) is composed of one positive feedback preamplifier, a positive feedback latch and a SR latch, whereas Comparator 1 together with an additional preamplifier forms the Comparator 2 (Fig. 6.9(b)). The micrograph of Comparator 1 is presented in (Fig. 6.9(c)). The detailed discussion of each block is presented in the next sub sections.

1. **Preamplifier:**

   Due to the lack of a reproducible and stable p-type oxide TFTs, the comparator is designed considering only n-type devices (IGZO TFTs). The pre-amplifier circuit (with positive feedback) schematic and the micrograph are presented in Fig. 6.10, which is extensively discussed in the literature [45, 68, 115, 117].

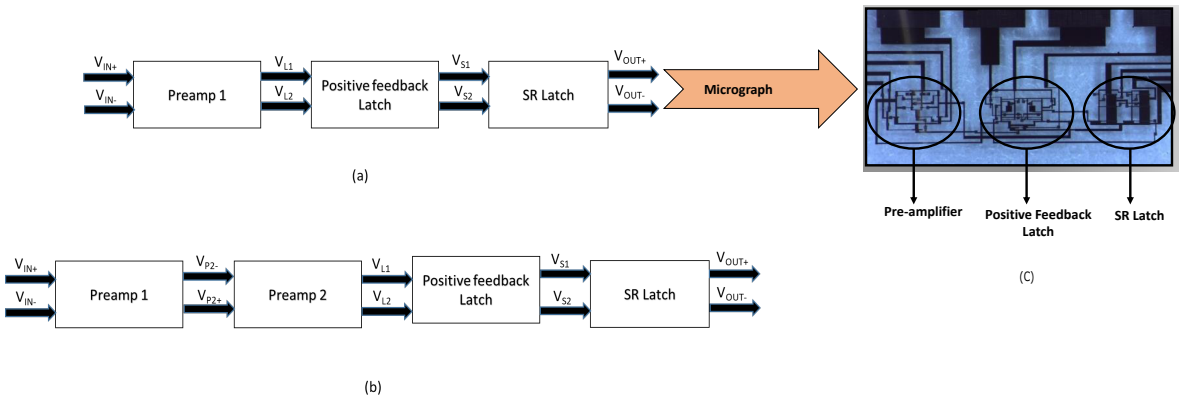


Figure 6.9: Block diagram of proposed (a) Comparator 1 (b) Comparator 2 (c) Micrograph of proposed Comparator 1 showing pre-amplifier, positive feedback latch and SR latch.

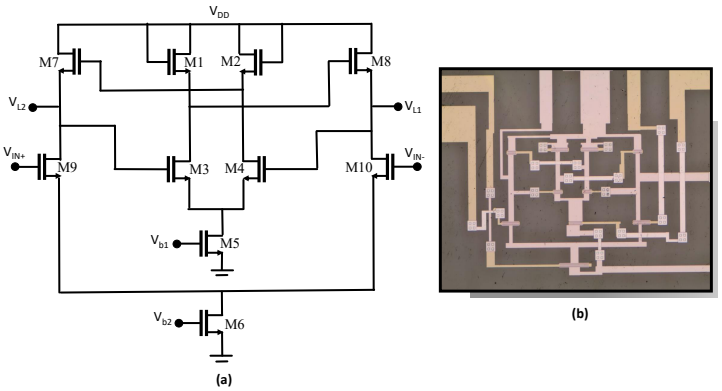


Figure 6.10: Preamplifier employed in the proposed comparator (a) Circuit schematic (b) Micrograph.

In this transistors M6-M10 forms a differential amplifier. It has overall gain (discussed in detail in Chapter 4, Section 4.1):

$$StageI : A_1 = \frac{g_{m9,10}}{g_{m7,8}(1-A_f) + g_{ds9,10} + g_{ds7,8}} \tag{6.12}$$

Where,

$$A_f = \frac{g_{m3,4}}{g_{m1,2} + g_{ds3,4} + g_{ds1,2}} \tag{6.13}$$

One pre-amplification stage has been used in order to design comparator 1 and two pre-amplification stages are used for designing of comparator 2 in order to enhance frequency of operation. These pre-amplification stage help to relax the design constraints

of the latch by increasing the input signal level to large value before applying it to the latch.

2. **Positive Feedback Latch:**

   Latch is an important block in high speed comparators. In the proposed comparator, positive feedback regenerative latch is used as shown in Fig. 6.11, whose operation is divided into two states (Reset and Compare/Regeneration). The state of 'Clk' determines the mode of operation.

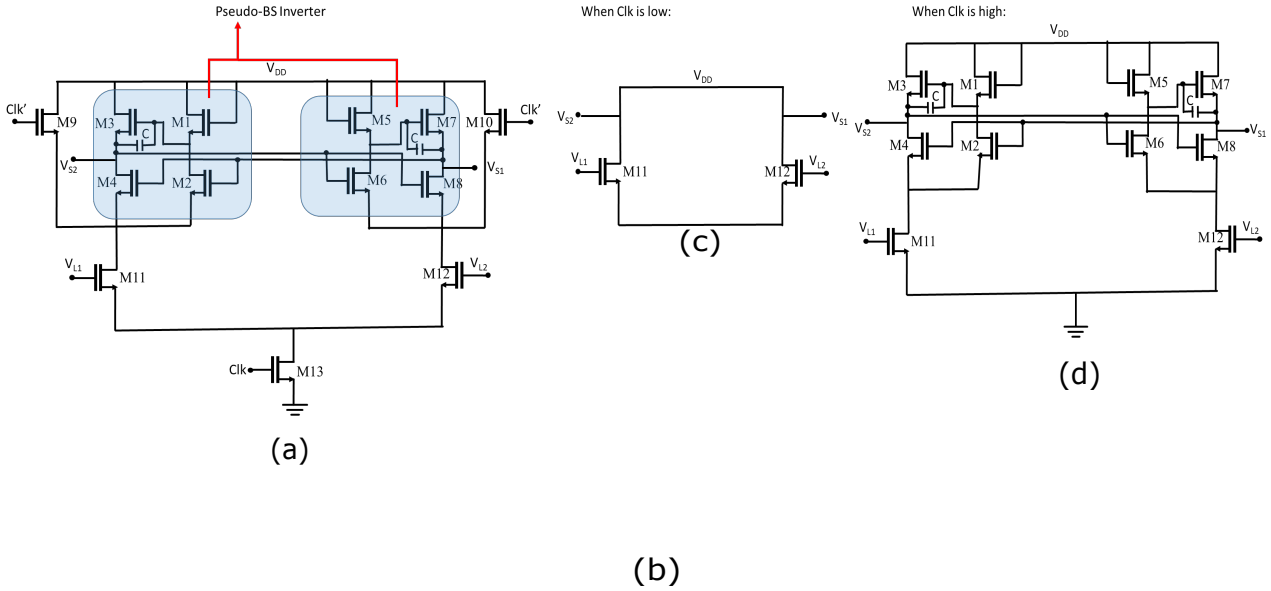


Figure 6.11: Novel positive feedback latch (a) Circuit schematic (b) Micrograph.

It consists of two high performance Pseudo-CMOS Bootstrapped (BS) inverters (discussed in Chapter 3), where C is the bootstrapping capacitance. This Pseudo CMOS BS inverter topology is used instead of conventional diode load based inverter, in order to achieve full swing at the output. Therefore, the overall performance of the comparators can be significantly improved. M11 and M12 form the differential pair that receives the differential voltages (V_{L1} and V_{L2}) arriving from the preamplifiers. M9 and M10 gates are applied with clk' and M13 gate is applied with Clk.

The operation of the latch is divided into two phases. First "Reset Phase, when the Clk is Low", M9 and M10 TFTs are in on-state and M13 is in off-state, therefore, no biasing current will exist and all the transistors are off. The outputs V_{S1} and V_{S2} are being connected to approximately equal to V_{DD}.

The second phase is the "Regeneration/Readout stage, when the clock is High." During this state, M9 and M10 are off and M13 is turned on. The current starts flowing through M13, differential pair and Pseudo CMOS BS inverter. The current that flows between the differential pair and the Pseudo CMOS BS inverters are different depending on the input voltages levels. The regeneration between the cross-coupled inverters perform the latching operation and determines the final output voltage. The time response of the dynamic latch is given by [130]:

$$\Delta V_S(t) = e^{(t/\tau_L)} \Delta V_s \tag{6.14}$$

The equation (6.14) gives the difference between the latch output voltages, $\Delta V_S(t)$, at the time t after enabling the latch. The voltage ΔV_s is the difference between the latch output voltages, before the latch is enabled. τ_L is the time constant of the latch, which is given by:

$$\tau_L = 0.67 C_{ox} \sqrt{\frac{WL^3}{2K'I}} \tag{6.15}$$

Where, C_{ox} is the oxide capacitance, W and L are the width and length of the latching transistors, I is the latch DC biasing current and K' is the trans-conductance parameter equal to $\mu_0 \, C_{ox}$. By using Pseudo CMOS BS inverters, full swing at the output can be achieved. After the regeneration mode, one of the output goes high and the other goes low, based on the input amplitude level.

3. **SR Latch:**

The SR latch drives the full complementary output levels at the end of the regenerative mode and remains in the previous state during reset mode [141]. NAND based SR Latch [142] is used at the output stage of the comparator as shown in Fig. 6.12.

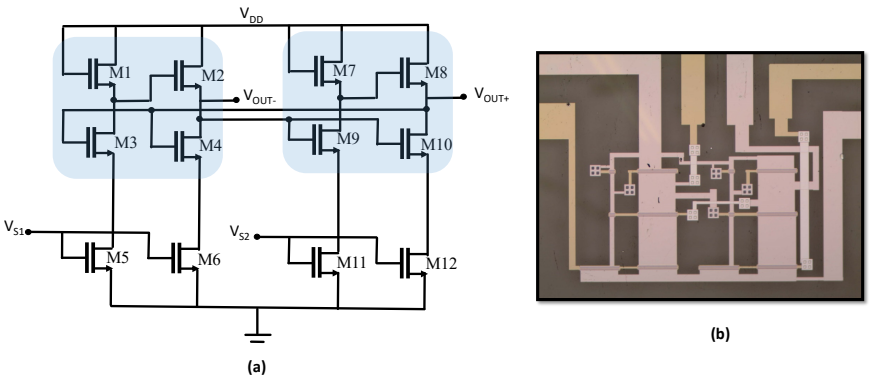


Figure 6.12: NAND based SR latch (a) Circuit schematic (b) Micrograph.

Instead of conventional NMOS diode load based inverters, Pseudo CMOS inverter topology (M1-M4 and M7-M10) is used in this SR latch for better voltage swing.

The other three proposed comparators are fully dynamic in nature. They have in-built pre-amplifier and employs a single phase clock. The advantage of using a single phase clock is reduced complexity of the circuit and less active area. Detailed description of each of these comparators are presented below.

6.2.1.2 Comparator 3

The circuit schematic and micrograph of comparator 3 are shown in Fig 6.13(a) and (b). This type of comparator is built on the principle of sense amplifier. Sense amplifier circuits accept small input signals and amplify them to generate rail-to-rail swings [143]. It can be noticed from the comparator circuit that a single phase clock is sufficient to perform both reset and regeneration operation. This comparator uses a conventional NMOS diode load based inverters (M1, M2 and M3, M4) to perform the latching operation. A low impedance switch is inserted between the two output nodes.

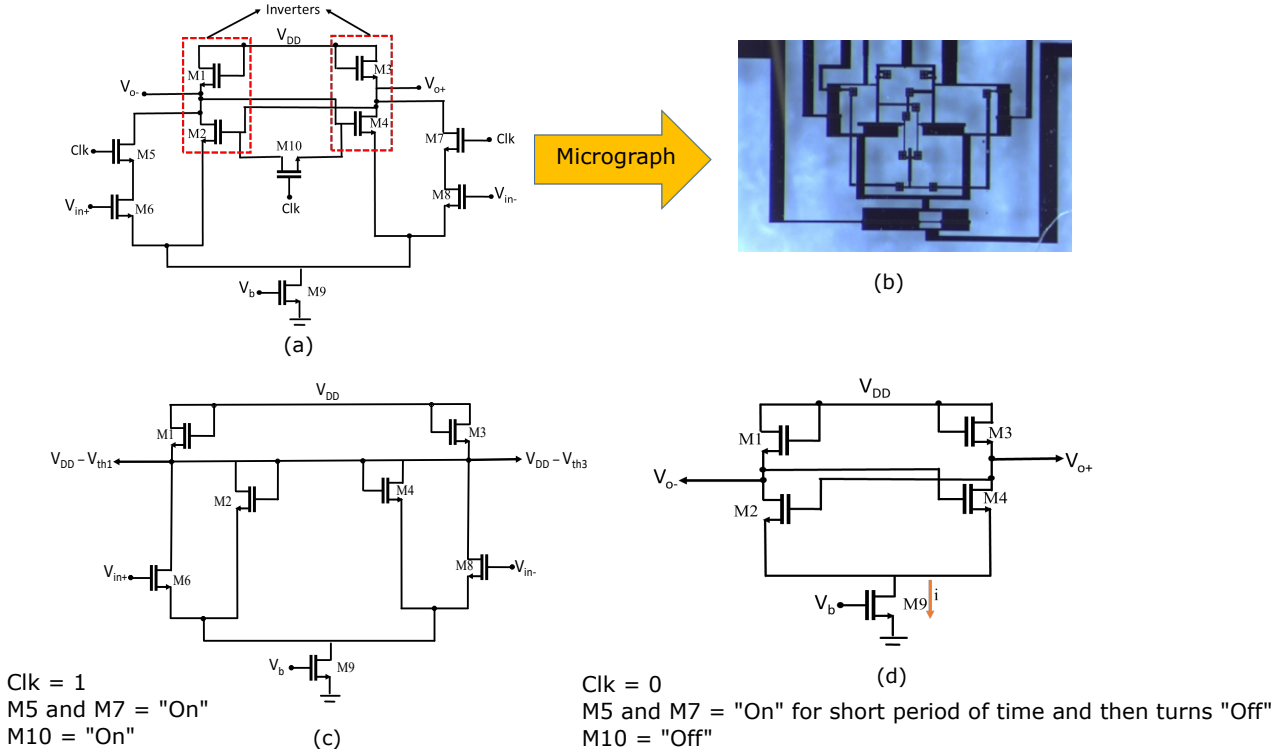


Figure 6.13: Proposed comparator 3 (a) Circuit schematic (b) Micrograph (c) Equivalent circuit during reset phase (d) Equivalent circuit during regeneration phase.

The working principle of the comparator can be understood in two phases as described below:

During "Reset Mode", when Clk is '1' (high), the reset switch is turned on, which shorts the two output nodes as shown in Fig 6.13(c). Due to shorting of the two output nodes, the resulted output voltage obtained is V_{DD} - $V_{th1/3}$.

During "Regeneration Mode", when Clk is '0' (Low) as shown in Fig 6.13(d), M5 and M7 transistors take some time to turn off due to their high on resistance compared to M10 transistor. This causes difference in current levels in the two branches of latch, where this difference is corresponding to the input signal levels. The cross coupled inverters (M1 and M2, M3 and M4), steer the tail current (i) through M9 transistor. This current is responsible in altering the output voltages of the comparator according to the input levels sensed by the latch and the comparator outputs (V_{o+} and V_{o-}) settles towards supply rails voltages.

6.2.1.3 Comparator 4

The circuit schematic and micrograph of comparator 4 are shown in Fig 6.14. Similar to comparator 3, it also uses a single phase clock.

The only difference between the comparator 3 and comparator 4 is the replacement of the conventional NMOS diode load based inverter by pseudo-CMOS inverter topology (as discussed in Chapter 3). The working principle of the comparator 4 is similar to comparator 3. The advantage of using pseudo-CMOS inverter topology over conventional NMOS diode load inverter is to obtain high output voltage swing and during the reset operation, it can reset the value of the latch to approximately half of the V_{DD}. This topology can replicate the behavior of the CMOS inverter and improves the output swing mainly V_{OL}. This helps to reduce the static current through M2 and M1 branch and M7 and M8 branch, resulting in low power consumption.

6.2.1.4 Comparator 5

The circuit schematic and micrograph of comparator 5 is shown in Fig 6.15. Similar to comparator 3 and comparator 4, it also uses a single phase clock. The difference between the comparator 4 and comparator 5 is replacing pseudo-CMOS inverter topology by pseudo-CMOS bootstrapped inverter topology (as discussed in Chapter 3). The working of this comparator is similar to comparator 3. Pseudo-CMOS BS inverter can retain complete rail-to-rail voltage swing, without significantly compromising on the power consumption. The presence of bootstrapping capacitor slows down the speed of operation.

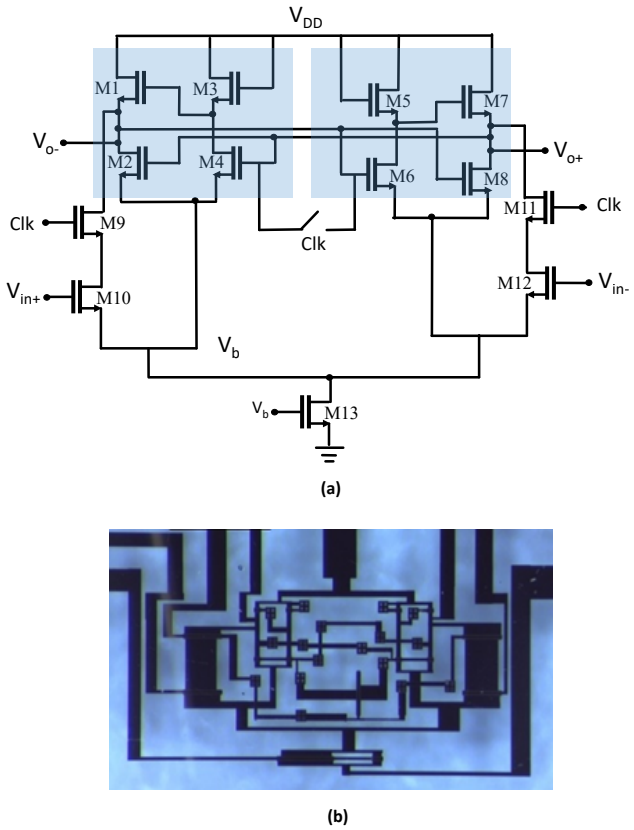


Figure 6.14: Proposed comparator 4 (a) Circuit schematic (b) Micrograph.

6.2.2 Simulation and Measured Results

Using in-house oxide TFT model the complete comparator have been designed and simulated in Cadence environment with a power supply of 10 V.

6.2.2.1 Simulation Results of Comparators

The performance of Preamplifier: By using the positive feedback topology in the preamplifier, a gain of 17.46 dB is achieved as shown in Fig. 6.16. The 3-dB frequency of 15 kHz and unity gain frequency of 100 kHz were noticed. The power consumed by this pre-amplifier is 110 μW with the phase margin of 79°.

The performance of Positive feedback latch: The performance of positive feedback latch is shown in Fig. 6.17, when the input and clock frequencies are 500Hz and 10kHz, respectively. The circuit is tested with a differential input amplitude of 5 $\pm$ 0.25 V. It can be observed that almost full rail-to-rail output is achieved. During the reset phase the outputs settles at V_{DD}. Whereas, during the regeneration phase, depending on the input voltages, voltage levels (V_{OH} $\approx$ 9.5 V and V_{OL} $\approx$ 870 mV are obtained.

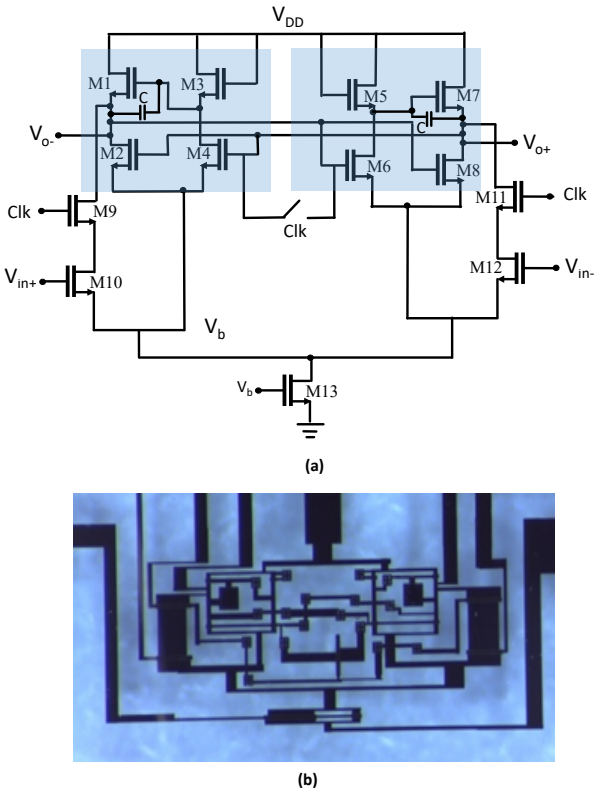


Figure 6.15: Proposed comparator 5, (a) Circuit schematic, (b) Micrograph.

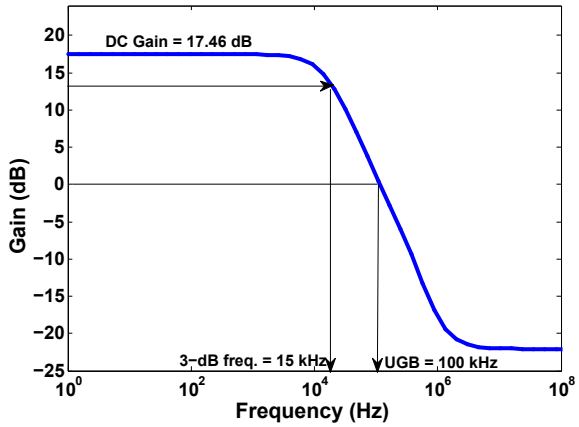


Figure 6.16: Frequency response of differential amplifier gain plot.

The performance of SR latch: The performance of a NAND based SR latch is shown in Fig. 6.18. The input voltage of 5 V is applied as logic high value for the SR latch and 0 V as the logic low with the input frequency of 500 Hz. The main functionality of this SR latch in the comparator is to provide full swing complementary digital outputs.

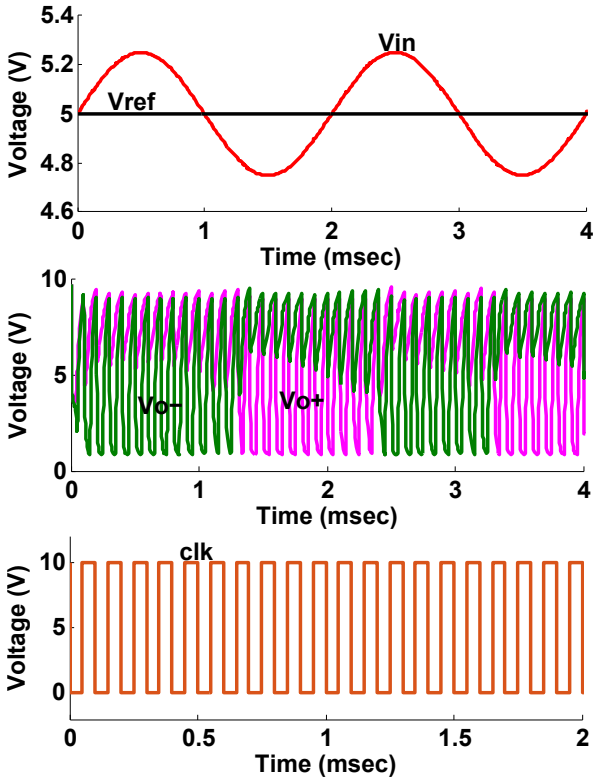


Figure 6.17: Transient response of positive feedback regenerative latch.

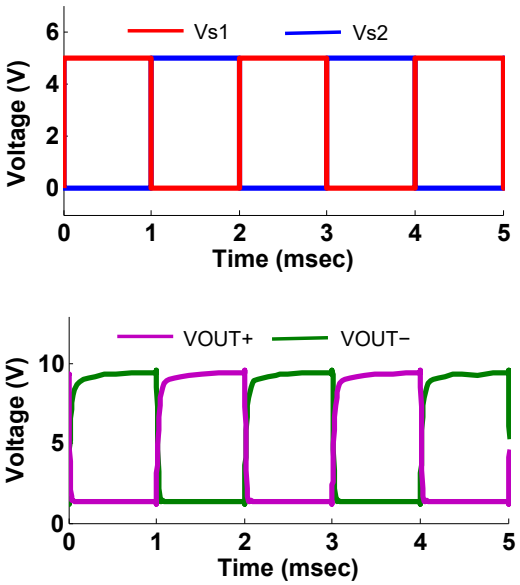


Figure 6.18: Transient response of NAND based SR latch.

The performance of Comparator 1: The comparator 1 is comprised of one preamplifier, a positive feedback latch and a SR latch. The performance of this comparator is shown in Fig. 6.19 at a clock frequency of 10 kHz. The comparator has been tested with an input voltage of 5 $\pm$ 0.06 V and frequency of 500 Hz.

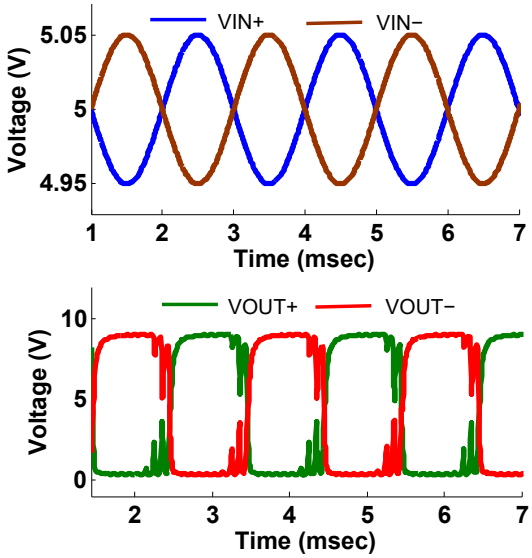


Figure 6.19: Transient response of Comparator 1 with a clock frequency of 10 kHz.

A differential signal with successive possible worst-case inputs are applied as shown in Fig. 6.20. As it can be observed, the proposed comparator always decides correctly, within a worst-case regeneration time less than 100 μsec. It can be noticed that the comparator gives accurate output when the differential input is $\geq$ 60 mV and digital output is valid in the falling-edge of Clk (after half clock cycle delay). In addition, 497 μW of power is consumed by comparator 1 at 10 V of power supply.

The performance of Comparator 2: The comparator 2 is comprised of two preamplifiers, a positive feedback latch and a SR latch. The performance of this comparator is shown in Fig. 6.21 at a clock frequency of 15 kHz. The comparator has been tested with the input voltage of 5 $\pm$ 0.02 V and frequency of 500 Hz.

Similar to comparator 1, comparator 2 is also tested for sequence of worst case input combinations as shown in Fig. 6.22. It can be observed that this comparator gives an accurate output when the differential input is $\geq$ 20 mV. In addition, 528 μW of power is consumed at 10 V power supply.

The Performance of Comparator 3:

The response of comparator 3 is shown in Fig. 6.23. This comparator works at sampling frequency of 2 kHz with input signal frequency of 100 Hz. The comparator has been tested

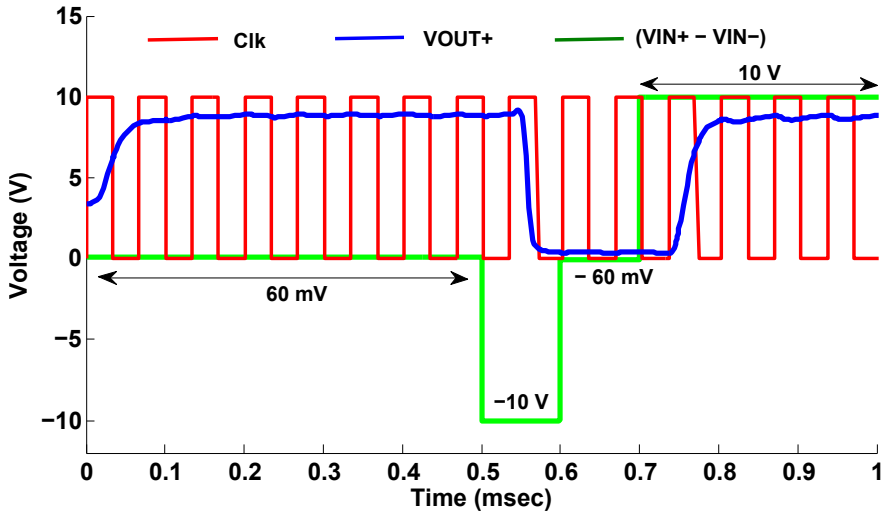


Figure 6.20: Performance of comparator 1 under successive worst case inputs.

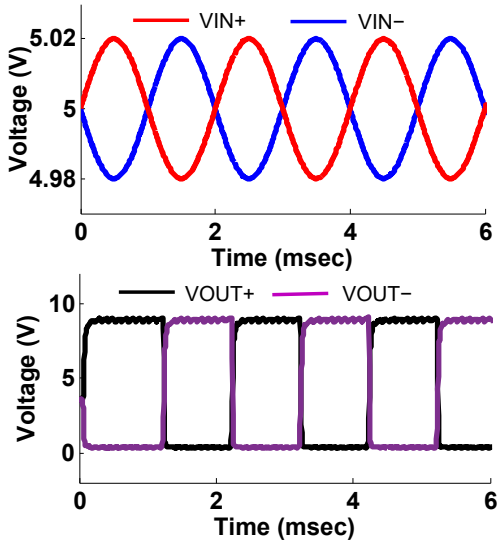


Figure 6.21: Transient response of Comparator 2 with clock frequency of 15 kHz.

with the input voltage of 5±0.5 V. Since it uses conventional NMOS diode load based inverters for the latching operation, so full swing at the output is not achieved. Resulted V_{OH} is 8 V and its V_{OL} value is 1.4 V.

A differential signal with successive possible worst-case inputs are applied as shown Fig 6.24. It can be noticed from the figure that the comparator gives the accurate output when the input is $\geq$ 500 mV. Its digital output is valid in the falling-edge of C_{lk} (after half clock cycle delay). The power consumed by this comparator is approximately 205 μW with the supply voltage of 10 V.

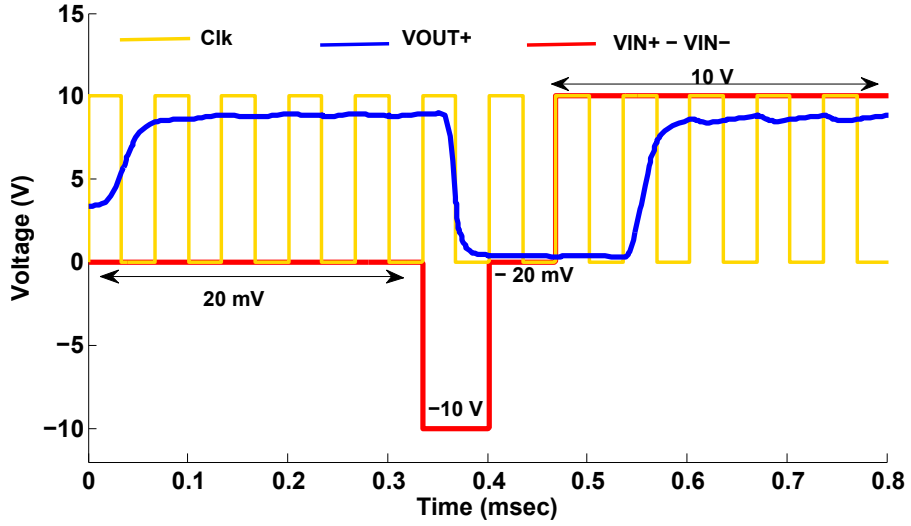


Figure 6.22: Performance of comparator 2 under successive worst case inputs.

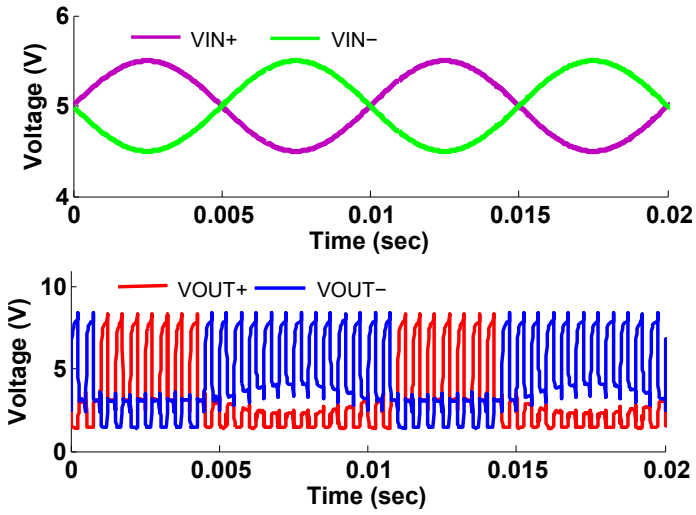


Figure 6.23: Transient response of Comparator 3 with clock frequency of 2 kHz.

The Performance of Comparator 4:

The response of comparator 4 is shown in Fig 6.25, when it is tested with a sampling frequency of 2kHz, input signal frequency of 100Hz and an input amplitude of 5±0.4 V. Pseudo-CMOS based inverters is used instead of conventional inverters for the latching operation, in order to improve the comparator swing at the output. The resulted output levels are V_{OH} of 9.2 V and V_{OL} of 0.5 V. Because of using pseudo-CMOS based inverter, both the high level and low levels voltage are improved compared to Comparator 3, without compromising on the speed and resolution.

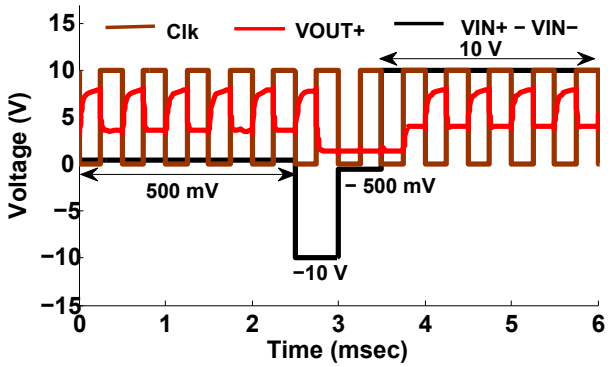


Figure 6.24: Performance of comparator 3 under successive worst case inputs.

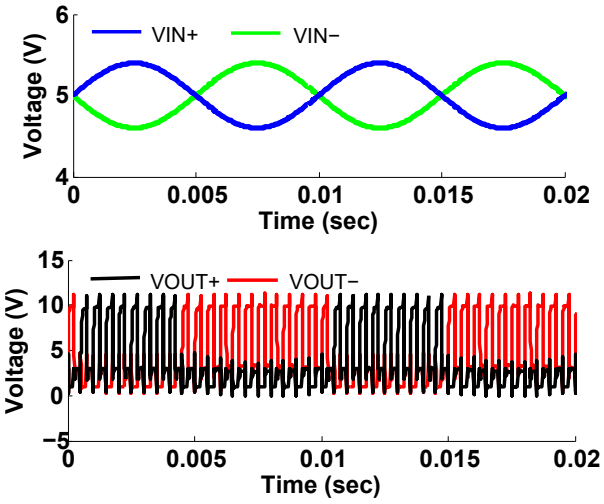


Figure 6.25: Transient response of Comparator 4 with clock frequency of 2 kHz.

Similar to comparator 3, comparator 4 is also tested for sequence of worst case input combinations as shown in Fig 6.26. It can be observed from the figure that the comparator gives an accurate output when the input is $\geq$ 400 mV. It can be noticed that the digital output is valid in the falling-edge of Clk (after half clock cycle delay). The power consumed by this comparator is approximately 129 μW with the supply voltage of 10 V. Further this design ensured low power consumption as the static current is inverter branches are significantly low unlike diode load based inverters.

The Performance of Comparator 5:

The response of comparator 5 is shown in Fig 6.27. This comparator also works at sampling frequency of 2 kHz with an input signal frequency of 100 Hz. The comparator has been tested with the input voltage of 5$\pm$0.4 V. Pseudo-CMOS bootstrapped based inverters are used instead

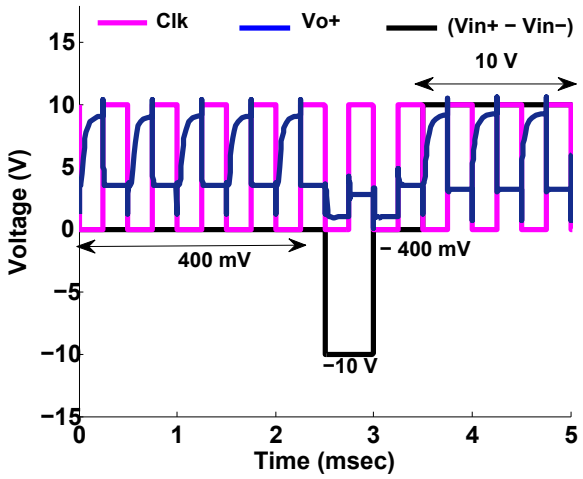


Figure 6.26: Performance of comparator 4 under successive worst case inputs.

in this design to improve the comparator output voltage swing. The V_{OH} value is improved to 9.95 V and V_{OL} is 321 μV. Almost full swing at the output of the comparator is achieved by this topology.

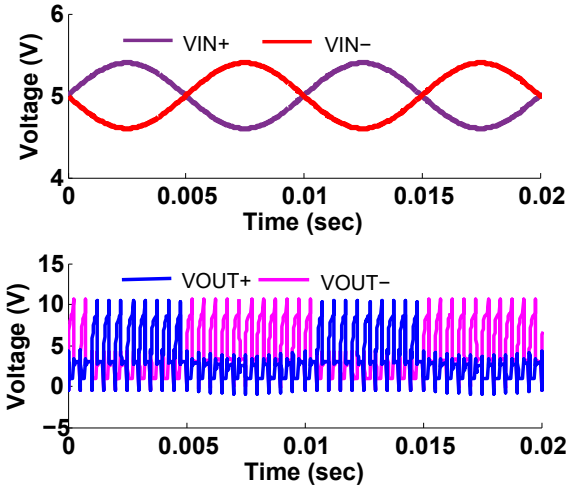


Figure 6.27: Transient response of Comparator 5 with clock frequency of 2 kHz.

Similar to other comparators, comparator 5 is also tested for sequence of worst case input combinations as shown in Fig 6.28. It can be observed from the figure that the comparator gives an accurate output when the input is $\geq$ 400 mV. It can be noticed that the digital output is valid in the falling-edge of Clk (after half clock cycle delay). The power consumed by this comparator is approximately 125 μW with the supply voltage of 10 V.

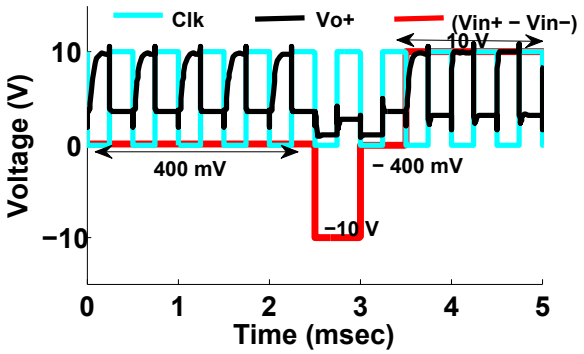


Figure 6.28: Performance of comparator 5 under successive worst case inputs.

Table 6.1: Comparison of the proposed comparators with the state of art work

S.No.	Designs	Fs (Hz)	Vin,min (V)	Power (W)	VOH (V)	VOL (V)	VDD (V)
1.	Comparator 1	10 k	60 m	497 μ	9.2	350 m	10
2.	Comparator 2	15 k	20 m	528 μ	9	300 m	10
3.	Comparator 3	2 k	500 m	205 μ	8	1.4	10
4.	Comparator 4	2 k	400 m	120 μ	9.2	0.5	10
5.	Comparator 5	2 k	400 m	129 μ	9.95	321 m	10
6.	Comparator IGZO [138]	30	2	-	10.5	5.5	20
7.	Comparator Organic [139]	500	-	1.5 m	14	8	20
8.	Comparator IGZO [140]	50 k	40 m	1.5 m	8.1	1.2	10

Performance of proposed comparators are being compared with the state of art work in TFTs as shown in Table 6.1.

The difference between comparator 1 and 2 is the addition of one preamplification stage. Due to which comparator 1 consumes low power as compared to comparator 2. Comparator 2 shows the advantage in terms of high frequency of operation and better resolution. This is because, by the addition of one more preamplifier, the total time t_1 (due to two preamplifiers) + t_2 (due to regenerative latch) (as shown in Fig. 6.8) will be less in order to reach the final desired output value as processing time is minimized, due to which comparator 2 works at high frequency with respect to comparator 1. However, this improvement in the speed of operation comes with a cost of power consumption in the second preamplifier.

In addition, it can be noticed that the Comparator 5 is superior in terms of providing full swing at the output as compared to other designs, due to use of pseudo-CMOS BS inverter topology for the latching operation, which makes $V_{OH} \approx V_{DD}$ and $V_{OL} \approx 0$. Comparator 4 provides the advantage in terms of the power consumption with respect to state of art work. This is mainly due to minimizing static current.

It can also be observed that the proposed comparators gives beyond the state of the art performance in terms of operating speed, output voltage swing and power consumption. The comparators that are reported in this work are suitable for the targeted application, since they all provide the advantage in terms of power consumption which is an important factor for biomedical application. These comparators can be successfully used for the designing of ADC for biomedical front end.

6.3 Passive Delta Sigma ADC

In this section a 2^{nd} order continuous time passive Δ-Σ ADC is presented with a-IGZO TFTs. The only active component in this ADC is the comparator. It is assumed that the digital decimation filter will be implemented in the digital-signal processor (DSP) available in the targeted application.

6.3.1 Circuit Description

Consider the 2^{nd} order CT Δ-Σ M (Continuous Time Delta Sigma Modulator) with feed-forward structure as shown in Fig. 6.29 [144]. In this figure, the feed forward path (highlighted)

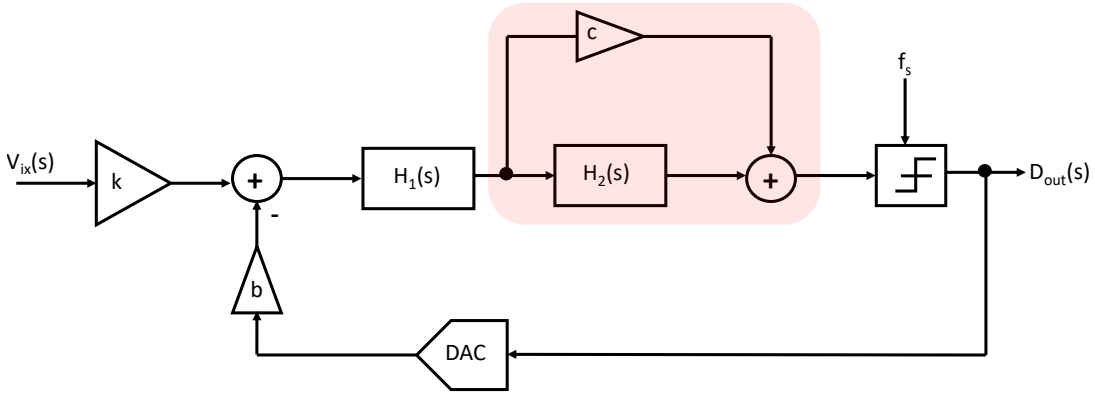


Figure 6.29: Block diagram of the 2^{nd} order CT Δ-Σ M with feed-forward structure.

introduces zero in the transfer function of the system and it improves stability of the closed loop. In order to reduce the quantization noise/error, the negative fedback path compares the quantized signal with the input signal. This process can only work if there is a sufficent gain in the feedback loop of the ADC. The main component of the gain in this ADC is from the comparator. Howerver, to achieve the stability in the loop with only one feedback path, it is necessary to add a zero to the loop gain. This can be done by placing a resistor in series with

the capacitor in the 2^{nd} RC circuit of the ADC as shown in Fig. 6.30. The obtained transfer function is given by [145]:

$$H_{RC2}(s) = \frac{sR_5C_2 + 1}{s(R_4 + R_5)C_2 + 1} \tag{6.16}$$

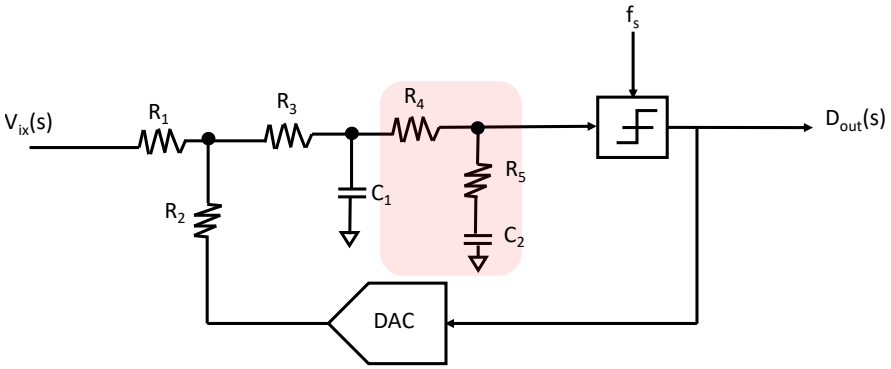


Figure 6.30: Circuit schematic of the 2^{nd} order CT ΔΣM with feed-forward structure.

Comparing both the highlighted parts of the Fig. 6.29 and Fig. 6.30, it is possible to match an equivalent signal path of the passive RC network as an integrator in parallel with a feed-forward. At high frequencies, gain is given by:

$$c = \frac{sR_5C_2}{s(R_4 + R_5)C_2 + 1} \approx \frac{R_5}{R_4 + R_5} \tag{6.17}$$

Whereas, at low frequencies, it behaves like an integrator with the gain less than unity given as:

$$H_2(s) = \frac{1}{s(R_4 + R_5)C_2 + 1} \approx \frac{1}{s(R_4 + R_5) + C_2} \tag{6.18}$$

For the first integrator (formed by R_3 and C_1), equation can be written as:

$$H_1(s) = \frac{1}{sR_3C_1 + 1} \tag{6.19}$$

In order to design ΔΣM, GA (Genetic Algorithm) tool has been used [144, 146, 147]. This tool is responsible to improve the modulator's overall dynamic performance. The optimization process takes into account all the characteristics such as the stability required for the circuit and the comparator's delay, which affects directly the modulator. The exact transfer function was also analyzed by the tool to evaluate the circuit behaviour.

Fig. 6.31 shows differential second-order continuous time Δ-Σ modulator that has been used in this work. This transfer function of the circuit is analyzed including loading effect

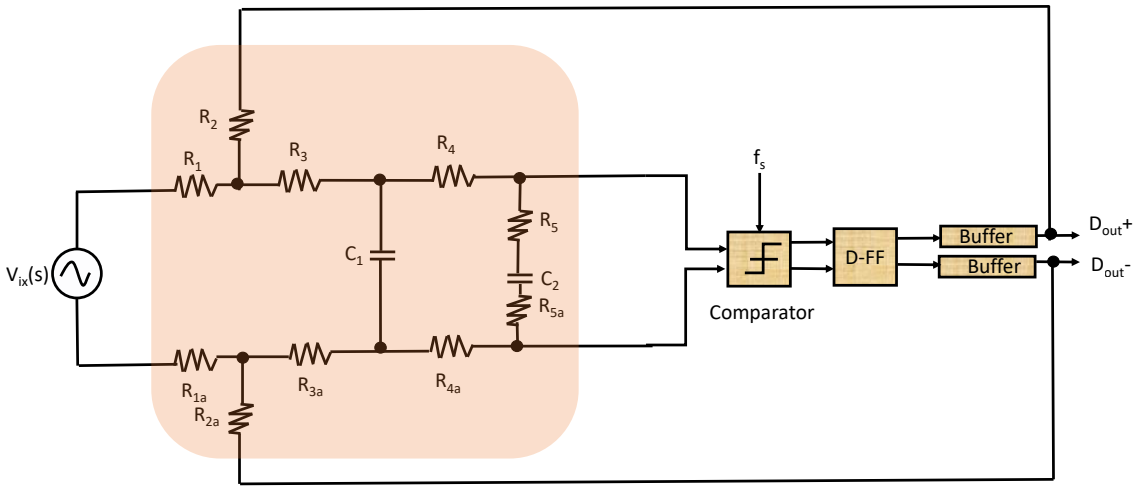


Figure 6.31: Block diagram of the 2^{nd} order CT ΔΣM.

Table 6.2: Sizing of passive components obtained using MATLAB/SIMULINK tool

Optimized Passive Components	**Values**
R_1	30 kΩ
R_2	64 kΩ
R_3	0
R_4	256 kΩ
R_5	26 kΩ
C_1	235 nF
C_2	23.5 nF

in SIMULINK in order understand circuit's functionality [64]. The analog loop filter is composed of cascade connection of the two fully passive RC type integrators, which are mainly responsible to implement 2^{nd} order noise shaping transfer function. Optimized values of the passive components in the ADC are presented in Table 6.2 at a sampling frequency of 2 kHz, where the optimization took place using GA tool.

In this ADC, comparator 1 is employed , as it is able to meet operating speed of the ADC (sampling frequency > 2kHz), and relatively provides low power consumption. After the comparator, master-slave configuration of D-Flip flop [148] and a buffer (two back to back Pseudo-CMOS BS inverter has been used as shown in Fig. 4.10(b)) has been used as shown in Fig. 6.32. The DFF is made up of Pseudo-CMOS BS inverters and two non overlapping clocks (Clk and Clk'). Switches in this circuit are implemented with IGZO TFTs. The two

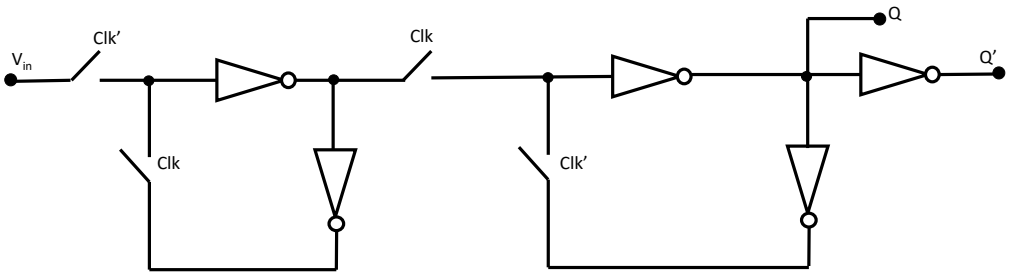


Figure 6.32: Schematic of master-slave DFF.

complementary outputs (Q and Q') of this DFF are fed into the buffer. The main advantage of using flip flop and buffer is to reduce the influence of the jitter noise. They guarantee constant delay, which means that the logic value is always sampled at the same time instant. Buffers provide proper driving capability to the circuit.

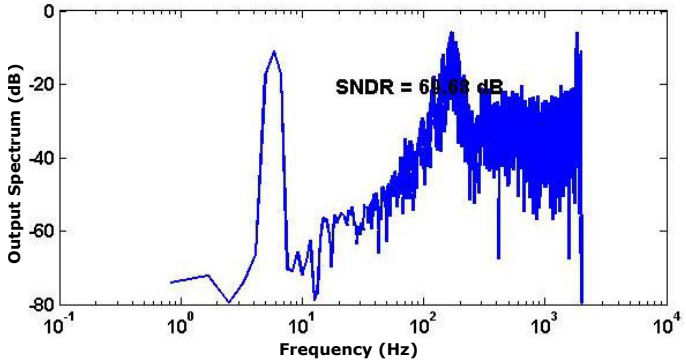


Figure 6.33: Spectrum of the proposed passive Δ-Σ ADC with a input signal frequency of 5 Hz from simulation.

6.3.2 Simulation Results

The circuit simulations of the passive delta sigma modulator has been carried out using in-house TFT model. The complete ADC has been tested with a sampling frequency of 2 kHz and an input signal frequency of 5 Hz. Spectrum of the proposed passive delta sigma ADC with an input signal frequency of 5 Hz from simulation is presented in Fig. 6.33. It exhibits the slope of 40 dB/dec, which is compatible with the 2^{nd} order noise shaping system. It can be seen that the SNDR (Signal to noise distortion ratio) obtained for this ADC is 69.68 dB with an ENOB (Effective number of bits) of 11.2 bits. The performance metrics of this ADC are shown in Table 6.3. The FOM (Figure of Merit) of this ADC is 0.15 μJstep. It can be clearly noticed

Table 6.3: Simulated performance parameters of passive delta sigma ADC

S.No.	Characteristic	Value
1.	Sampling Frequency	2 kHz
2.	Input signal Frequency	5 Hz
3.	Input signal amplitude	5 Vdiff
4.	OSR	100
5.	B.W.	10 Hz
6.	SNDR	69.68 dB
7.	Power supply	10 V
8.	Power consumption	2 mW
9.	FOM	0.15 μJ/conversion step

from the table that is ADC consumes very low power and provide high ENOB compared to the state of the art work (see Table 6.5), which can be sucessfully used for the targetted application.

6.4 Active Delta Sigma ADC

The ADC that has been discussed above is the passive delta sigma ADC, in which only comparator is the active element. The disadvantage of this ADC is that, we need an extra PCB (Printed circuit board) in order to use the passive RC components. In order to avoid this extra circuitry, this work proposes a complete on chip delta sigma ADC, in which all the components are active in nature.

6.4.1 Circuit Description

The block diagram of second order active delta sigma ADC is shown in Fig. 6.34. This

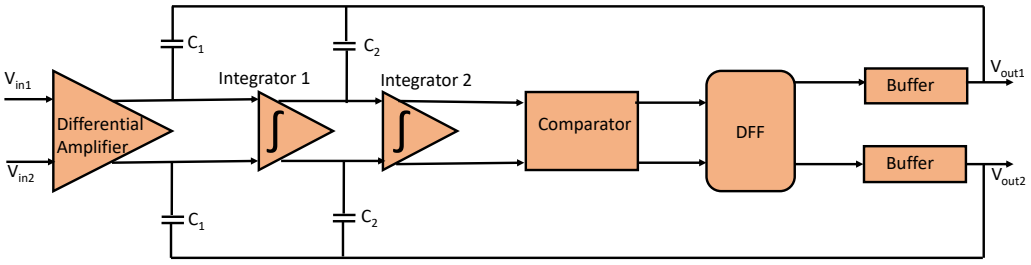


Figure 6.34: Block diagram of the 2^{nd} order CT active Δ-ΣM.

ADC consists of differential amplifier (same as discussed in section 6.2.1.1), two RC based integrators, comparator 1 (as in passive ADC), DFF and two buffers. This active delta sigma is obtained by replacing the passive integrators with active counter parts in Fig. 6.31.

Integrators : RC based integrators (see Fig. 6.35) [149, 150]. have been used in this design due to minimal complexity of the circuit, which can ensure better process yield. The output

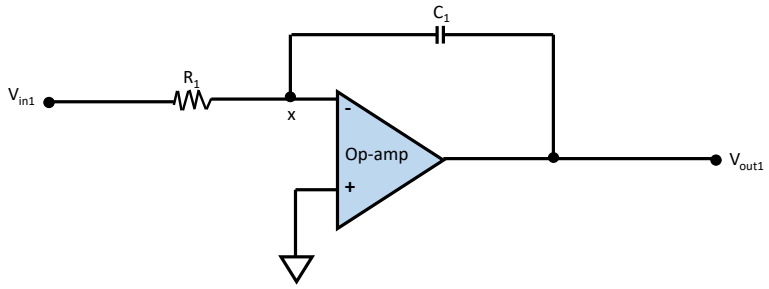


Figure 6.35: Circuit diagram of an opamp based integrator.

voltage (V_{out1} of this integrators given by:

$$V_{out1} = \frac{-1}{j\omega RC} V_{in1} \tag{6.20}$$

Where, $\omega = 2\pi f$ and the output voltage V_{out1} is a constant 1/RC times the integral of the input voltage V_{in} with respect to time. Thus the circuit has the transfer function of an inverting integrator with the gain constant of -1/RC. The minus sign (–) indicates a 180° phase shift because the input signal is connected directly to the inverting input terminal of the operational amplifier.

Since resistors occupy huge area in the chip, they are replaced with diode connected transistors. The block diagram of the integrator is shown in Fig. 6.36. A positive feedback operational amplifier (discussed in section 5.1) has been used in this integrator circuit. The resistance is equal to $1/g_m$. Since the mobility of the devices are low, g_m values is typically in the order of μS and helps to implement huge resistance with minimal active area. The circuit functionality almost remain the same as the previous design (see Fig. 6.35).

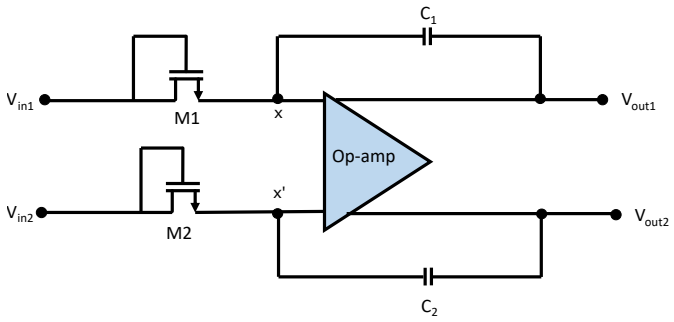


Figure 6.36: Circuit diagram of an integrator.

6.4.2 Simulation Results

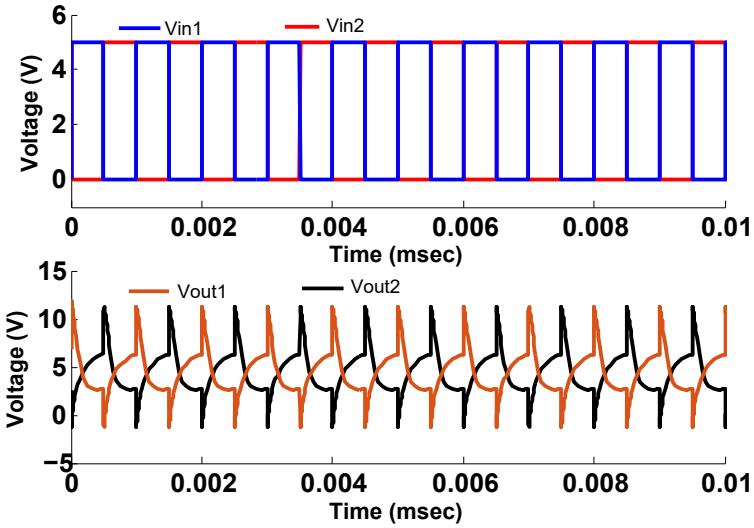


Figure 6.37: Simulation result of differential integrator circuit.

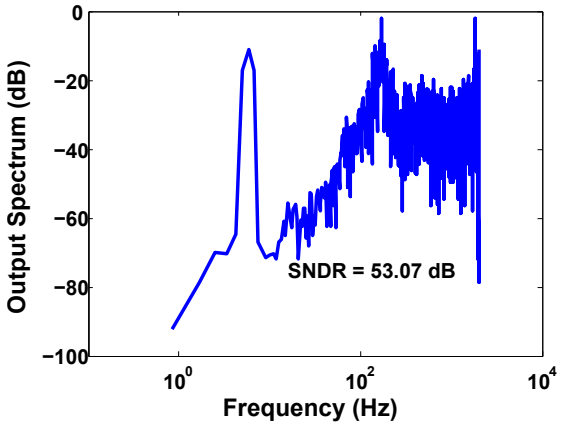


Figure 6.38: Spectrum of the proposed active Δ-Σ ADC with a input signal frequency of 5 Hz from simulation.

The simulation of active Δ-Σ ADC has been done using in house a-IGZO TFT model. The output of the integrator circuit is shown in Fig. 6.37 and and expected behavior can be noticed. The spikes in the output are due to the non-idealities of the switches in the circuit.

Spectrum of the proposed active Δ-Σ ADC with an input signal frequency of 5 Hz from simulation is presented in Fig. 6.38. ADC has been tested with a sampling frequency of 10 kHz and an input signal frequency of 5 Hz. The SNDR obtained for this ADC is 53.07 dB with

Table 6.4: Simulated performance parameters of active ΔΣ ADC

S.No.	Characteristic	Value
1.	Sampling Frequency	10 kHz
2.	Input signal Frequency	5 Hz
3.	Input signal amplitude	5 V_{diff}
4.	OSR	66
5.	B.W.	75 Hz
6.	SNDR	53.07 dB
7.	Power supply	10 V
8.	ENOB	8.5 bits
9.	FOM	0.0315 μJ/conversion step

Table 6.5: Comparison of ADCs with the state of art work

S.No.	ADC Design	f_S (kHz)	f_M (Hz)	$B.W.$ (Hz)	OSR	SNDR (dB)	ENOB (Bits)	FOM (μJ/ conversion step)	V_{DD} (V)
1.	**Passive Delta sigma ADC**	2	5	10	100	69.68	11.2	0.15	10
2.	**Active Delta sigma ADC**	10	5	75	66	53.07	8.5	0.0315	10
3.	Delta sigma with organic TFT [65]	0.5	10	15.6	16	26.8	4.1	3.6	15
4.	Delta sigma with a-IGZO TFT [64]	128	101.5	500	128	57	9	6.7	10
5.	a-IGZO asyn-chronous Delta sigma [66]	1	50	300	-	40	6.2	0.39	20

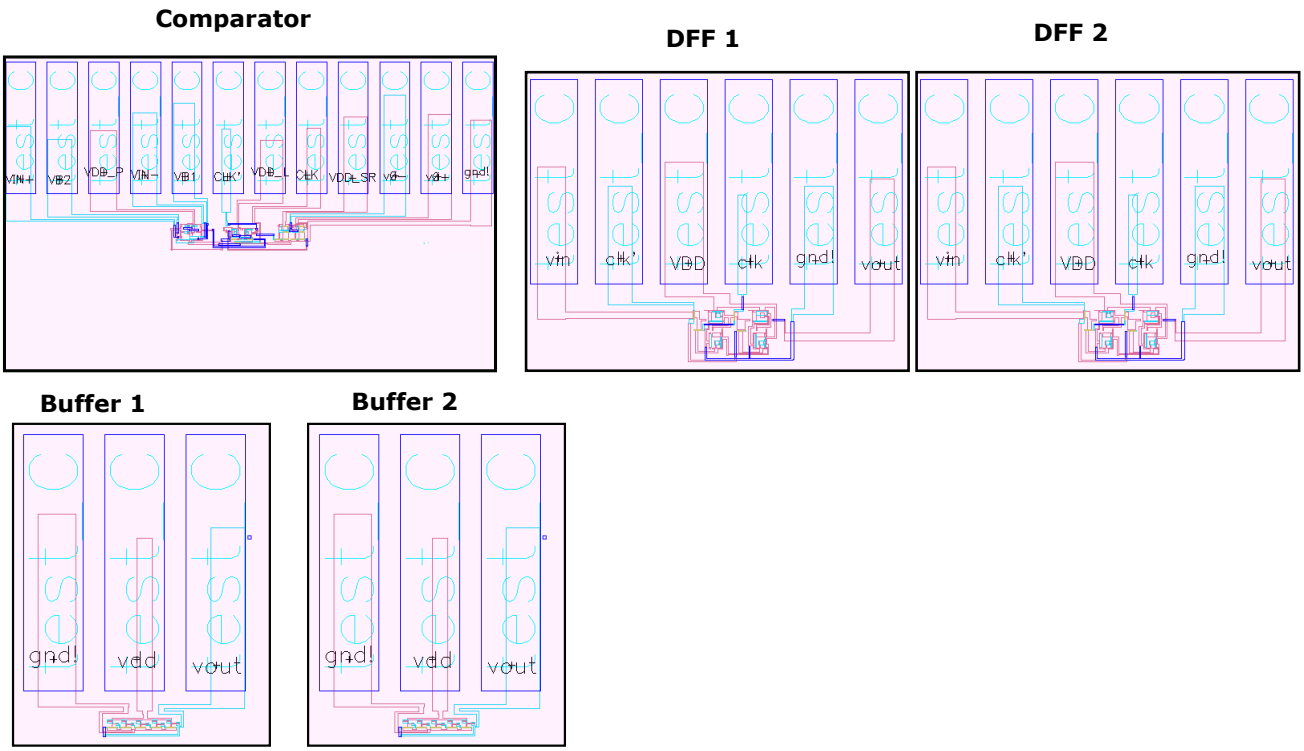


Figure 6.39: Layout of passive Δ-Σ ADC.

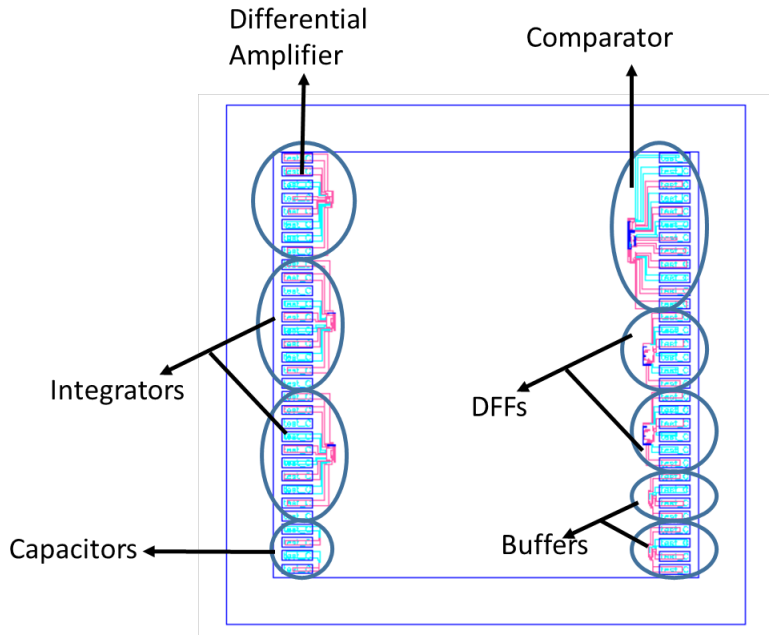


Figure 6.40: Layout of active Δ-Σ ADC.

the ENOB of 8.5 bits. The reason behind this poor ENOB is due to the non-idealities of the opamps that are present in the differential amplifier and the integrator circuits. The operating speed is high as the active components (differential amplifier, integrators and comparators) has the unity gain bandwidth more than 20 kHz, which makes active Δ-Σ ADC to work at high speed. The ADC performance metrics are presented in Table 6.4. In addition both the ADC has been compared with the state of art work in Table 6.5. It can be noticed that passive delta sigma produces high ENOB (as only comparator is the active element) and active delta sigma ADC has the advantage in terms of FOM (Figure Of Merit), which is 0.0315 μJ/conversion step as compared to the state of art work. These both ADC can be successfully used for the biomedical acquisition analog front-end block.

6.5 Layouts of ADCs

For both these ADCs layouts has been designed. Since the yield of the TFTs is low, the layouts of the individual blocks are designed and placed in one chip as shown in Fig. 6.39 and Fig. 6.40. During the measurement, the connections will be done externally in order to see the complete functionality of the ADC. In the case of passive ΔΣ ADC, a PCB of passive elements are created using eagle tool. Both these ADCs are under fabrication, because of which measured results are presented in this work.

6.6 Conclusions

In this chapter, five novel high performance comparators are proposed. Simulation results have shown that the proposed circuits are able to work at several tens of kHz. The five comparators that are reported gives an advantage in-terms of high speed and low power consumption in the order of μW, which is a stringent requirement for biomedical application. Due to some fabrication issues (finite isolation between pads), measured results could not be reported. However, next batch is under fabrication and these circuits are expected to be characterized once they are fabricated.

In order to built passive Δ-Σ ADC, comparator 1 has been chosen from all the five comparators. This ADC provides the advantage with the ENOB. Since, ENOB is the stringent requirement for this biomedical system, passive delta sigma ADC has been chosen in the complete system simulation results.

Similar to passive Δ-Σ ADC, active Δ-Σ ADC also uses Comprator 1 out of other five comparators. By replacing all the passive components (integrators, differential amplifier, DAC), which were used in passive ADC with the active components, this ADC has been designed.

This ADC gives the advantage in terms of low power consumption compared to the passive Δ-Σ ADC.

Chapter 7

Complete System Implementation

Chapter 4 to 6 in this thesis described design details of individual blocks in biomedical front-end. This chapter presents the complete proposed system response.

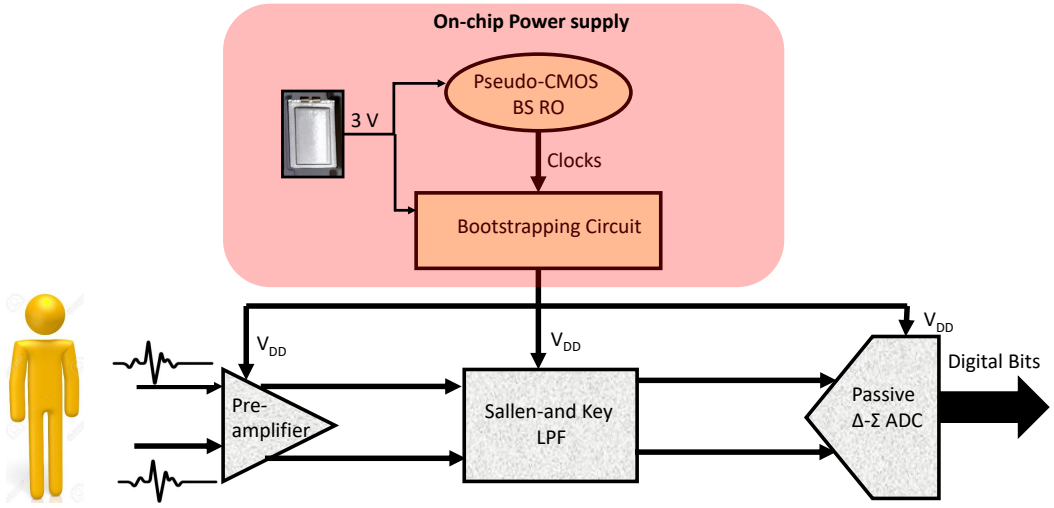


Figure 7.1: Block diagram of complete analog front-end.

The complete system block diagram is shown in Fig. 7.1. It consists of an on-chip power supply, which generates power supply (V_{DD}) for the pre-processing blocks. BrightVolt printed battery is used in this work to generate on-chip power supply. It can be fabricated with solution process techniques [151]. They are ultra-thin, flexible, and do not contain volatile liquids—eliminating the potential for combustion.

The other components used to generate on-chip power supply is the Psuedo-CMOS BS RO. This RO has been used because it provides full swing at the output. The clocks generated by

this is used by the bootstrapping circuit in order to generate V_{DD} for rest of the pre-processing blocks.

The biological signals are being sensed with the use of bio sensors from the human body and are send to pre-amplifier for further pre-processing. The positive feedback preamplifier has been used to design this analog front-end. The next important block is the LPF. 2^{nd} order SC sallen-and-key LPF has been used in this work. This filter acts as an antialiasing filter, which helps to block the unwanted signal. After the filter, ADC has been used in this work, which generates digital bit streams that can be transmitted by communication means. The ADC that has been considered is the passive delta sigma ADC as it generates highest number of bits, which is the key requirement for such biomedical systems.

7.1 Simulation Outcome

The complete system simulation has been carried out using in-house a-IGZO TFT model. Various biological signals inputs are presented in Table 1.1. For the system simulation, the input amplitude of the signal has been chosen to 5 mV and a frequency of 100 Hz (by keeping in mind the ECG signals). The supply voltage generated by the on-chip power supply circuitry is approximately equal to 10 V, which is fed to rest of the pre-processing and signal conditioning blocks. The main challenge in designing of this complete analog front-end is the loading effect. This is reduced by changing the aspect ratios of some transistors in order to get the required output. The output after the pre-amplification stage is shown in Fig. 7.2. Very less degradation

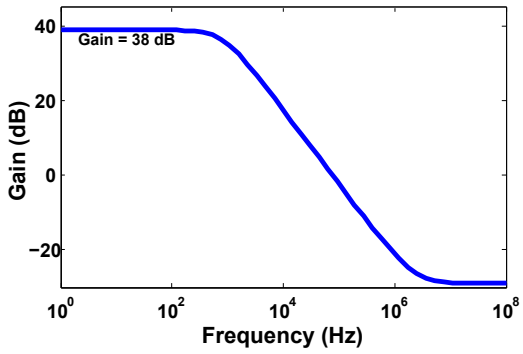


Figure 7.2: The frequency response of pre-amplifier after the pre-amplification stage.

in the gain is observed after this stage as it is the 1st stage of the complete block and suffers less loading condition. The main degradation in the output can be seen after the LPF as shown in Fig. 7.3. The 3-dB frequency is degraded much (i.e. instead of 0 dB it is now 3 dB). This is

mainly due to the loading effect of the subsequent block that is the pre-amplifier stage. This degradation in the output has a direct effect in the resolution of the ADC.

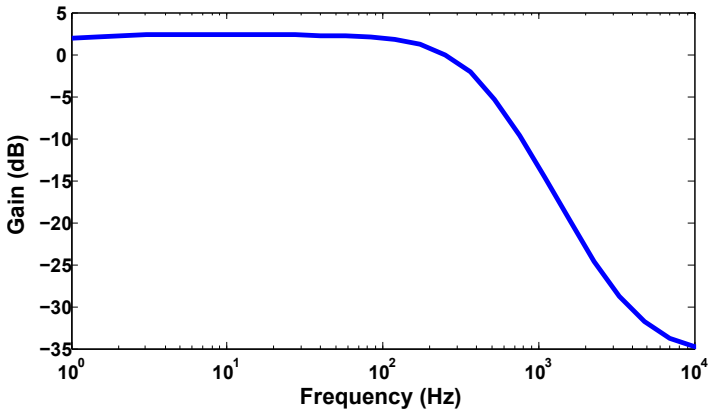


Figure 7.3: The frequency response of SC Biquad with high gain DDA after the filtering block.

The spectrum of ADC is shown in Fig. 7.4 from the complete system, when it is tested with a typical bio-signal from simulations. It can be seen that the ADC output exhibits a slope of 40 db/dec and the SNDR of 56.47 dB. This gives the ENOB of 8.9 bits. The degradation in the ENOB in the complete system is due to the non-idealities, of various components (opamps, switches, clock generators and comparators) and also due to loading effect. By using proper communication protocol this digital bitstream can be transmitted to either mobile or server and it needs to converted into a readable form. The power consumed by the complete system is 3.5 μW.

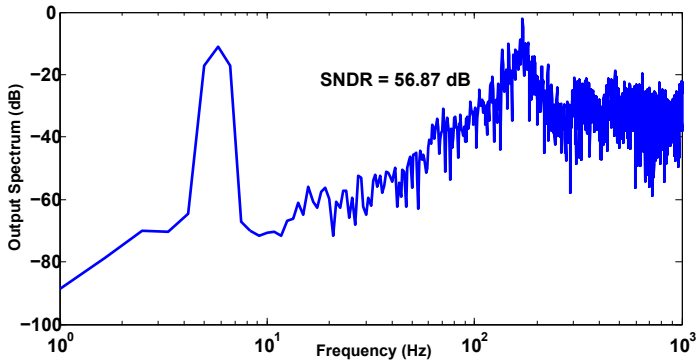


Figure 7.4: Spectrum of the output of ADC in complete system simulation.

7.1.1 Conclusions

This work presents complete biomedical wearable analog front-end for the first time with the oxide TFT technology. The complete system is able to show an ENOB of 8.9 bits, which is a reasonable resolution to reconstruct signals.

Chapter 8

Conclusion and Future Work

This chapter presents the conclusions on the work developed for the PhD. dissertation, It also focuses on the future directions of this work in order to improve the effectiveness of circuit design with a-IGZO TFTs and to improve the overall system performance.

8.1 Conclusions

The main goal of this Ph.D is to design biomedical wearable analog front-end with the a-IGZO TFT. For the first time, a complete biomedical analog front-end has been designed and implemented in this work. The main target of the work is to built the self-contained non-invasive flexible real-time health monitoring system that can be used by variety of people in this whole world. In order to make this system various individual pre-processing and signal conditioning blocks are required along with the on chip power supply.

The printed batteries that are used in this work supplies 14 mA current per hour. The amplifier which is the next block requires 300 μA current, which can be easily driven by the printed battery that is used in this biomedical wearable front end. For considering the decay in the battery voltage discharge, simulations of few of the above block have been carried out by taking into consideration 30% decay in the voltage variations in the power supply that has been used. It has been observed that not much decay in the performance has been observed for the above circuits. Initially as a first step, the circuit has been designed by considering the mA rating of the battery. Since, the work is targeted to built low cost electronics, so the battery that is used is disposable kind. The higher nominal capacity of the battery will be considered in the future work. In addition the other possibility is to use the battery less system e.g for energy harvesting.

The proposed blocks has been successfully implemented in this work for biomedical acquisition front-end. **Pseudo-CMOS BS RO** has been used after comparing with other ROs with oxide TFT technology. The **bootstrapping circuit** has been proposed in this work for the first time, so that the area of the system can be minimised and to make the complete system on chip. The next important block is the **pre-amplifier**, which is used to amplify the low amplitude signal. A simple architecture of the pre-amplifier is used so that area of the system can be minimised. In addition to this, since oxide TFT is completely a new technology, fabrication of the complex circuit is very critical due to poor yield. So, a simple architecture of positive feedback amplifier has been used in this work, which serves the purpose for the application targetted. The other important block is the **antialising filter or LPF**. SC Sallen-and-Key LPF (upto 6^{th} order) has been proposed in this work first time in order to filter out unwanted parts. The measured results of this filter has also been reported in the thesis. The next important block is the **ADC**. This is the most important block in biomedical analog front-end. The heart of the ADC is the comparator. Five types of different comparators have been proposed in this work. The dynamic comparators has been proposed. The best comparator 1 has been chosen out of five different comparators. Two types of ADCs have been proposed. One is Passive Δ-Σ ADC and the other is active Δ-Σ ADC. The simulation results of both the ADCs have been presented, which shows better ENOB and FOM compared to the state of art work. And, finally all the proposed blocks (Pseudo-CMOS BS RO, bootstrapping circuit, 2^nd order SC Sallen-and-key LPF, active Δ-Σ ADC) above have been combined together in order to make **complete biomedical front-end** with the commercially available printed battery. The simulation result of this analog front end is presented and it shows ENOB of 8.9 bits, which is higher than the state of art work.

8.2 Future Directions

- Device noise modeling and noise characterization of circuits need to be carried out, as flicker noise play an important role at low frequencies (especially for the application under consideration).
- By enhancing the Opamp performance (obtaining near ideal response), various circuits performance can be improved further, mainly LPF and comparator.
- ADC circuit layouts are ready and they are under fabrication. Once these circuits are fabricated, they need to be characterized from measurements.
- After the digital bits are generated, they need to be transmitted through the communication means, which can be Bluetooth or any wireless technology. The complete communication

part is to be implemented to have the prototype ready. Once the communication system is developed, the digital bits can be successfully transmitted to the either mobile or server for continuous health monitoring of the wearer.

Appendix A

Other works during Ph.D.

A.1 A PVT Insensitive Low-power Differential Ring Oscillator

In this a novel low-power seven stage differential ring oscillators (see Fig. A.1), which are robust against PVT variations is considered. The work proposes two different circuits, namely, current

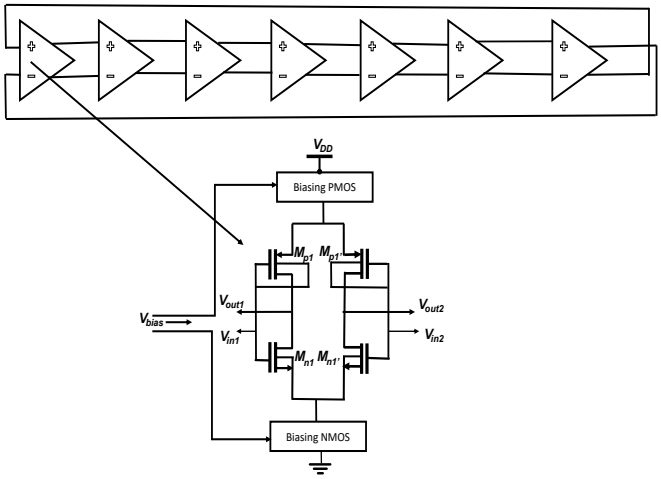


Figure A.1: Proposed Differential 7-stage RO circuit

starved (see Fig. A.2(a)) and negative skewed PMOS ring oscillators(see Fig. A.2(b)). Power consumption is minimized in these circuits by employing DTMOS (below 0.6V) technique that adjusts the threshold voltage of the PMOS transistor in a dynamic way (see Fig. A.3(a)). In addition, circuit performance is made robust against PVT variations by using a self biased compensation technique(see Fig. A.3(b)).

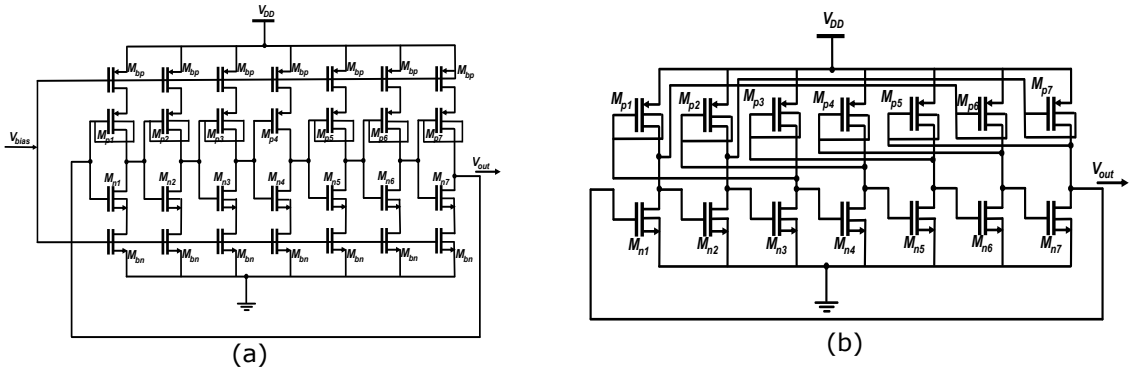


Figure A.2: (a) 7-stage current starved ring oscillator(CSRO) employing DTPMOS technique, (b) Circuit schematic of single ended negative skewed PMOS RO with DTPMOS Technique

The biasing circuit changes the control voltage of the differential ring oscillator to maintain a constant frequency. Circuits simulations are carried out in standard 65 nm technology with a supply voltage of 0.5 V. The simulation results are shown in Fig. A.4.

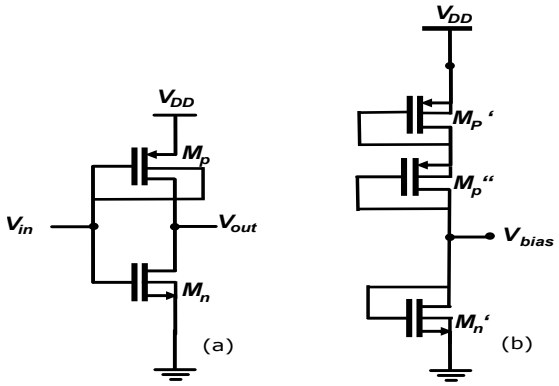


Figure A.3: (a) Circuit schematic of a simple inverter using DTPMOS (M_p), (b) Circuit schematic of proposed self-compensated biasing circuit only with MOSFETs

The worst case variation in frequency of oscillation is $< 4\%$ over a temperature range of -75°C to 150°C. Process corners have resulted in 2% variation compared to the nominal, on the other hand 1% relative variation is observed when power supply is with in the range of 5% of nominal value. Proposed current starved and skewed PMOS ring oscillators show a power consumption of 186 nW at 41 MHz and 4.2 μW at 1.5 GHz, respectively, from the simulations. Both these circuits maintains the power delay product of 0.2 fJ. Given the robust performance against PVT, these circuits can find the potential applications in IoT devices.

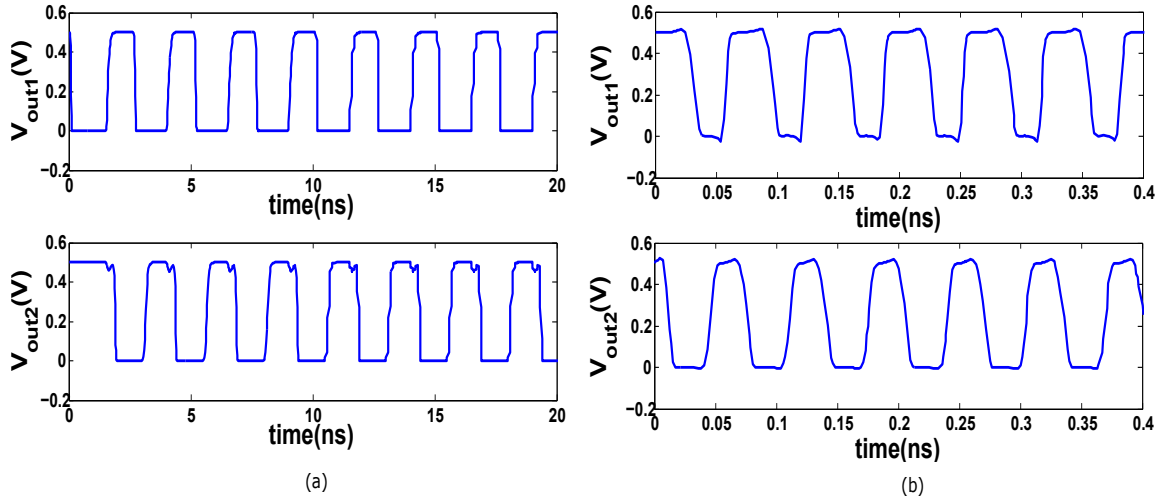


Figure A.4: Proposed Design I and Design II response

A.2 Temperature Insensitive Low-Power Ring Oscillator using only n-type Transistors

A low-power five stage current starved ring oscillator (see Fig. A.5) which is robust against temperature variations is being presented in this work. The proposed work has been designed

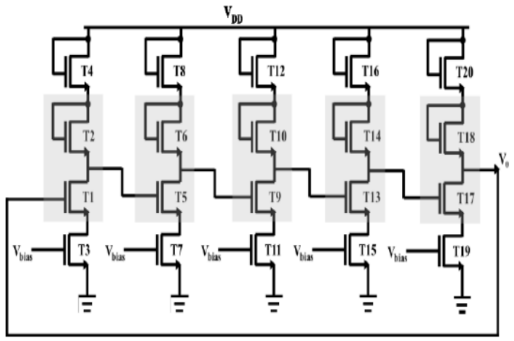


Figure A.5: Circuit schematic of proposed work where V_{bias} is generated by temperature compensation bias circuit

using only n-type transistors and therefore, can easily be adapted to amorphous oxide TFTs which have unstable p-type transistors. The ring oscillator uses temperature compensation biasing circuit (as shown in Fig. A.7), which contains a novel bootstrap op-amp (shown in .

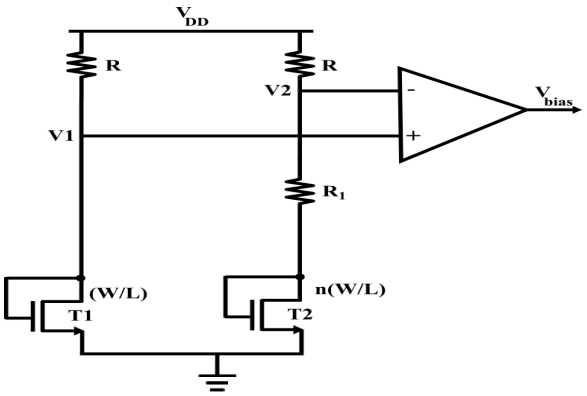


Figure A.6: Generation of temperature independent bias voltage

The biasing circuit generates constant bias voltage to make current starved ring oscillator insensitive to temperature variations. The proposed circuit simulations were done in Cadence Virtuoso on standard 180nm CMOS technology with a supply voltage of 1.8 V. The output

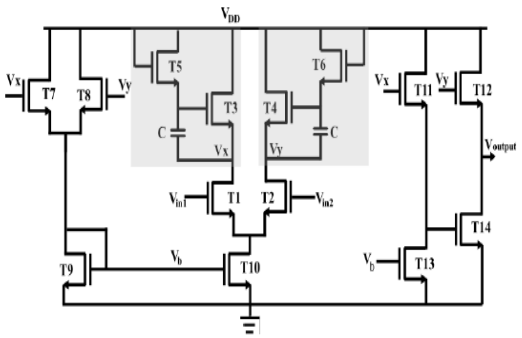


Figure A.7: Circuit schematic of op-amp with capacitive bootstrapping and common mode feedback used

response of the opamp and the temperature insensitive RO is shown in Fig. A.8(a) and (b) respectively. This circuit has shown a frequency of oscillation around 235.8 MHz and a power delay product of 0.139 pJ. The phase noise of designed ring oscillator is -98.532 dBc/Hz. It shows 3.73% variations in frequency over a temperature range from -40°C to 125°C. Since oxide TFT's are also n-type FET's (Field Effect Transistors), the proposed design can be directly adapted to this emerging post-silicon technology, which finds potential applications in smart packaging, bio-medical and wearable systems.

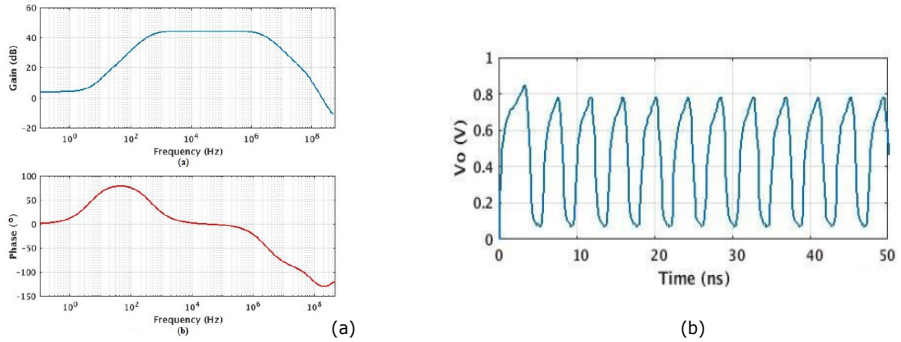


Figure A.8: (a) Frequency Response of proposed op-amp (a)Gain plot, (b)Phase plot, (b) Proposed ring oscillator oscillations

A.3 A Voltage Controlled Oscillator Using IGZO Thin-Film Transistors

A voltage controlled oscillator (VCO) using amorphous Indium Gallium Zinc Oxide (a-IGZO) thin-film transistors (TFTs) is presented as shown in Fig. A.9. This circuit consists of a high-

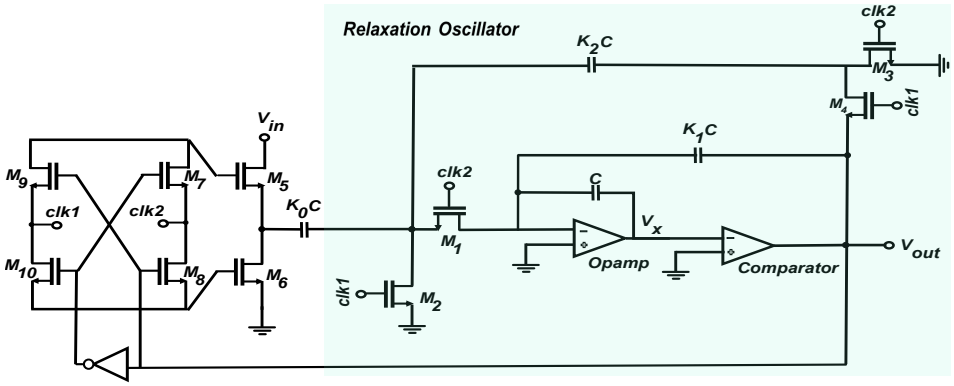


Figure A.9: Circuit diagram of voltage controlled oscillator

gain OpAmp (positive feedback opamp is used as shown in Fig. A.10), a comparator (three preamplifier and a latch as shown in Fig. A.11) and a relaxation oscillator.

The implemented relaxation oscillator shows a power consumption of 700 μW, when it is simulated with a supply rails of $\pm$5 V as shown in Fig. A.12. It shows a frequency of oscillation range from 327 to 560 Hz, when the tuning capacitance value is in varying from 1.6 to 5 pF. On the other hand, the VCO has a power dissipation of 1.3 mW with frequency ranging from 400 to 556 Hz with a controlling voltage from -5 to 5 V. In-house oxide TFT model is used for circuit simulations in Cadence environment. This circuit would find potential applications in

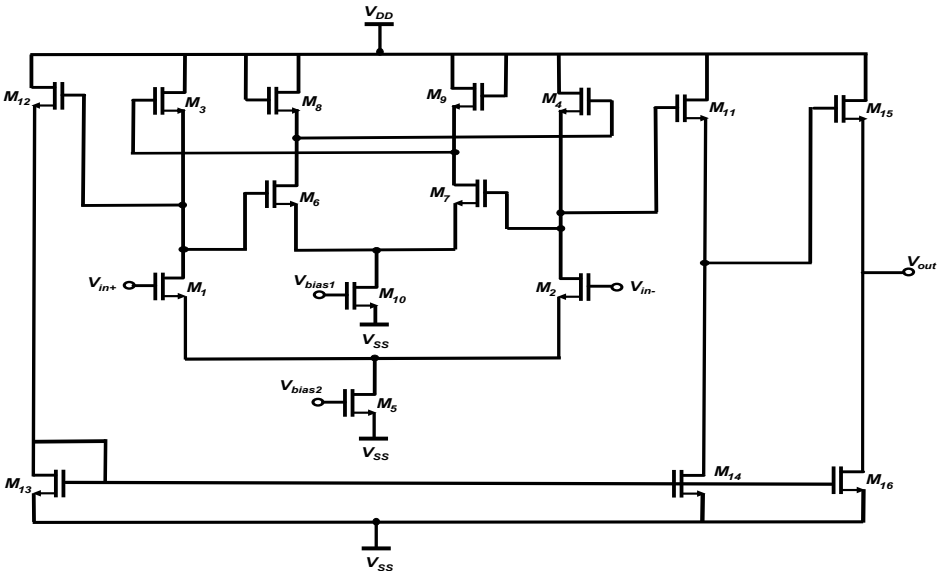


Figure A.10: Circuit diagram of operational amplifier with positive feedback

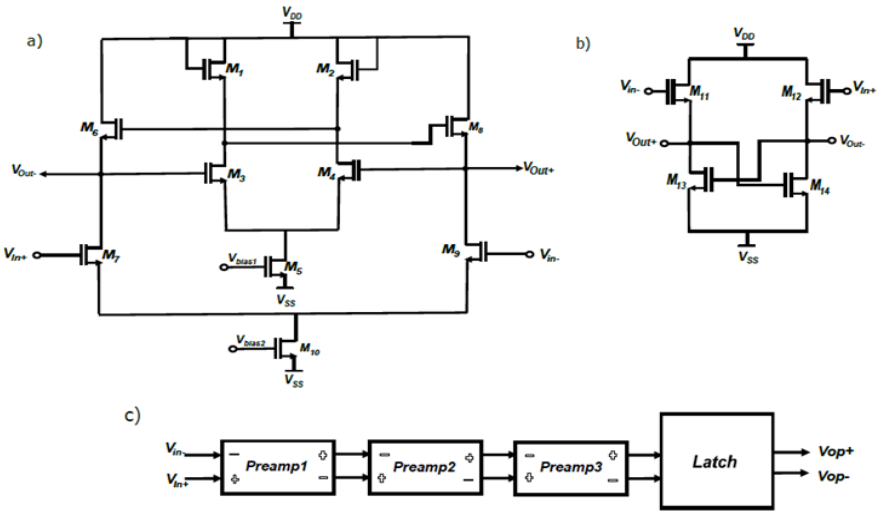


Figure A.11: Circuit diagram of a comparator: a) Preamplifier b) Latch c) Complete Comparator

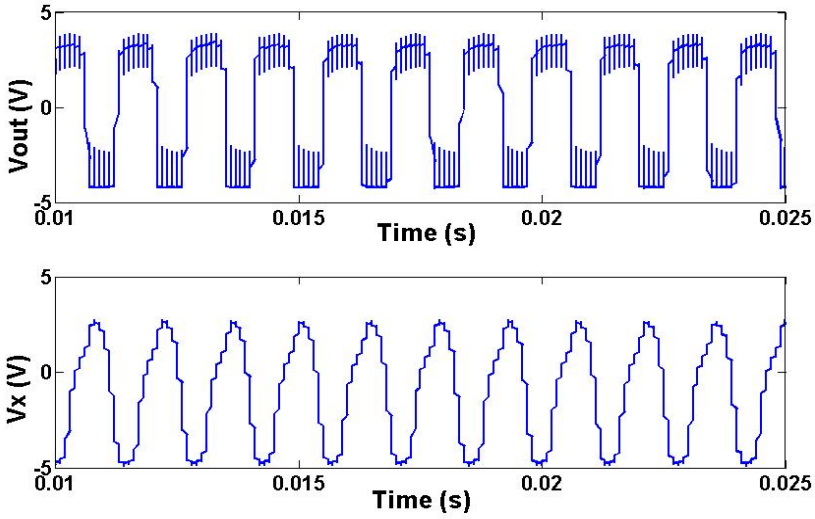


Figure A.12: Output response of relaxation oscillator

large-area flexible systems, namely smart packaging, biomedical and wearable systems, which needs clocks with different frequencies.

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