Innovative Augmentation of Impedance Transformation in the Design of Highly Flexible Multifunctional RF/Microwave Circuits and Components

By

Rahul Gupta

under the guidance of

Dr. Mohammad S. Hashmi

Professor, IIIT-Delhi

Indraprastha Institute of Information Technology, Delhi

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Dr. Mohammad S. Hashmi

Professor, IIIT-Delhi

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To my loving Krishna, parents, wife, and brother ...

Certificate

This is to certify that the thesis titled ***Innovative Augmentation of Impedance Transformation in the Design of Highly Flexible Multifunctional RF/Microwave Circuits and Components*** being submitted by **Rahul Gupta** to the Indraprastha Institute of Information Technology-Delhi, for the award of the degree of **Doctor of Philosophy**, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

July 2021
Dr. Mohammad S. Hashmi
Professor
Thesis Supervisor

Department of Electronics and Communication Engineering
Indraprastha Institute of Information Technology-Delhi
New Delhi-110020

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"*The only way to do great work is to love what you do!*"
"*It is strange that only extraordinary men make the discoveries, which later appear so easy and simple.* "

– Georg C. Lichtenberg

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Abstract

The burgeoning of a multi-standard wireless communication system (WCS) with the multitude of emerging applications has been permeating the design and development of radio frequency (RF) circuits and components of the front-end subsystem. To support multiple standards, the design and development of the multi-band RF and Microwave circuits and components are highly desirable. This is due to the fact that these wireless standards are operating at multiple frequencies, and therefore, the multi-band architectures reduce system size, cost, power consumption, etc., rather than the conventional approach of using individual subsystems for the individual frequencies. Furthermore, the multi-functional RF components eliminate the redundant uni-functional components and associated interconnections between the uni-functional components of a communication system by exhibiting all the features inherently. This further reduces the system size/volume, power consumption, insertion loss, etc.

However, it should be noted that the design and development of such multi-band multi-functional components are found to be very challenging. The key constraints are the achievable frequency ratios, achievable impedance transformation ratios, and increased design complexities. For example, the literature is replete with the dual-band impedance transformers, but the range of frequency ratios and impedance transformation ratios is limited. More importantly, the concurrent operation of high impedance transformation ratios at high frequency ratios is much limited. One of the possible reasons is the limited design flexibility at the expense of increased functionality. Subsequently, the requirement of multi-functional characteristics affects the design flexibility further. Furthermore, the development on the domain of multi-band multi-functional components is not explored much in the literature. Therefore, this thesis aims

to investigate and address the existing lacunae on the design and development of multi-band multi-functional components.

Firstly, the challenges associated with the impedance transformers for high impedance transformation ratios at high frequency ratios are discussed and addressed. Also, the concurrent high frequency ratios and high impedance ratios are accomplished.

Secondly, the RF and Microwave components exhibiting multiple inherent features like impedance transformation, DC blocking, differential phase shifts, balanced-to-unbalanced signal conversion, etc., are investigated. In addition, the multi-functional architectures, inherently exhibiting more than one feature, with dual-band operations are addressed. More specifically, the developed architectures for operation at high impedance transformation ratios and high frequency ratios, even concurrently, are accomplished.

Thirdly, this thesis addresses the challenges associated with the arbitrary impedance environments, varying with the design frequencies. The architectures for dual-band impedance transforming power divider with frequency-dependent complex port impedances at two arbitrary design frequencies are presented. No such feature from a dual-band power divider or combiner is presented in the literature.

Finally, it should also be noted that the reported design architectures are simplified and uni-planar and are supported by sound and systematic analytical design solutions, which is rare in the literature. The closed-form equations with innovative design strategies make the designs re-configurable for the wide range of design specifications, and thus the enhanced microstrip compatibility is attained. The closed-form design equations not only make it easy to calculate the design parameters but also enables the quick prototyping of the circuits and components.

Overall, the contributions are within the realm of simplifying the design strategies and rapid prototyping backed by the closed-form design equations for multi-frequency communication circuits and systems. In brief, this research work has the potential to significantly advance the current state-of-the-art that may eventually lead to a paradigm shift in the way such systems are designed. This thesis also paves a new dimension of the applications of multi-functional components, which leads to a unified PCB solution for the RF front end of a communication system. The future directions and possible improvements are also reported.

Author's Publications

Peer-Reviewed Published Journal Articles

J[1] **R. Gupta**, B. Gabdrakhimov, A. Dabarov, G. Nauryzbayev, and, M. S. Hashmi, "Development and Thorough Investigation of Dual-Band Wilkinson Power Divider For Arbitrary Impedance Environment", IEEE Open Journal of the Industrial Electronics Society, doi: 10.1109/OJIES.2021.3072151.

J[2] **R. Gupta**, M. S. Hashmi and M. H. Maktoomi, "An enhanced frequency ratio dual band balun augmented with high impedance transformation," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 12, pp. 2973-2977, Dec. 2020, doi: 10.1109/TCSII.2020.2984787.

J[3] **R. Gupta**, M. S. Hashmi and M. A. Chaudhary, "Flexible design scheme for a simple dual-band ultra-high impedance transformer and its application in a balun," IEEE Access, vol. 8, pp. 125745-125754, July 2020, doi: 10.1109/ACCESS.2020.3008046.

J[4] **R. Gupta**, M. H. Maktoomi, V. V. Singh, and M. S. Hashmi, "High impedance transforming dual-band balun with isolation and output ports matching," Progress In Electromagnetics Research Letters, Vol. 81, pp. 121-126, 2019, doi:10.2528/PIERL18111604.

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J[6] M. H. Maktoomi, **R. Gupta**, M. A. Maktoomi and M. S. Hashmi, "A Novel Wideband Phase Shifter Using T- and Pi- Networks," Journal of Progress in Electromagnetics Research (PIER), Vol. 71, 29-36, 2017, doi:10.2528/PIERL17080202.

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UR[2] **R. Gupta**, B. Gabdrakhimov, and M. S. Hashmi, "Investigation of a Versatile Impedance Transforming Power Divider for Single- and Dual-Band Operations,"

UR[3] **R. Gupta**, B. Gabdrakhimov, and M. S. Hashmi, "Filtering Dual-band Power Divider with Inherent Impedance Transformation Feature."

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C[1] **R. Gupta**, S. Kairatova, and M. S. Hashmi, "A Dual-Band Balun Architecture With Unequal Port-Terminations", IEEE 50th European Microwave Week (IEEE EUMW), Netherlands, Jan 2021.

C[2] **R. Gupta**, M. A. Chaudary, and M. S. Hashmi, "Dual-Frequency Out-Of-Phase Power Divider with Integrated Impedance Transformation", IEEE Asia-Pacific Microwave Conference (APMC), Hong Kong, Dec 2020.

C[3] **R. Gupta**, V. V. Singh and M. Hashmi, "A Power Divider Utilizing Stepped Impedance Transformers for Real/Complex Port Terminations," IEEE Asia-Pacific Microwave Conference (APMC), Singapore, pp. 312-314, 2019, doi: 10.1109/APMC46564.2019.9038196.

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2. K. Dautov, M. Hashmi, S. Verma, and **R. Gupta**, "Highly-efficient Compact Size DGS-based Wireless Power Transfer for Low-Power Sensor Nodes", IEEE International Microwave and RF Conference (IMaRC), India, Dec 2019.

3. M. S. Hashmi, Kassen Dautov, and **R. Gupta**, "Investigation of an Enhanced Efficiency Class-E Power Amplifier with Input Wave Shaping Network", IEEE International Conference on Advanced Networks and Telecommunications Systems, Dec 2018.

4. A. Saxena, D. Banerjee, **R. Gupta**, and M. S. Hashmi "Design of pi-Structure Dual-Band Matching Network With Unequal Susceptance Cancellation Stubs" IEEE International Microwave and RF Conference (IMaRC), India, Nov 2018.

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6. **R. Gupta**, A. P. Yadav and M. S. Hashmi, “Symmetric Tri-band Balun Architecture with a Systematic Design Procedure,” in NCC2017, Madras, India, Mar 2017.

7. **R. Gupta**, M. A. Maktoomi and M. S. Hashmi, "A new high frequency balun with simplified impedance matching technique," IEEE Asia-Pacific Microwave Conference (APMC), New Delhi, pp. 1-4, 2016.

8. M. A. Maktoomi, **R. Gupta**, M. H. Maktoomi, and M. S. Hashmi, "A Generalized Multi-Frequency Impedance Matching Technique," in MMS2016, Abu Dhabi, UAE, Nov 2016.

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List of Abbreviations

1G	1st Generation Wireless Standard
2G	2nd Generation Wireless Standard
3G	3rd Generation Wireless Standard
4G	4th Generation Wireless Standard
5G	5th Generation Wireless Standard
ADS	Keysight Advanced Design System
AI	Amplitude Imbalance
BW	Bandwidth
CAD	Computer Aided Design
CCL	Complex Conjugate Load
CI	Characteristic Impedance
DBB	Dual-Band Balun
DBITPD	Dual-Band Impedance Transforming Power Divider
DBPD	Dual-Band Power Divider
DC	Direct Current
EDA	Electronic Design Automation
EL	Electrical Length
EM	Electromagnetic Momentum
FBW	Fractional Bandwidth
FDCL	Frequency Dependent Complex Load
FM	Frequency Modulation

FoM	Figure of Merit
FR1	frequency range 1 for 5G standards
FR2	frequency range 2 for 5G standards
GaN	Gallium Nitride
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HEMT	High Electron Mobility Transistor
IMN	Input Matching Network
IoT	Internet of Things
ISM	Industrial Scientific and Medical Band
ITR	Impedance Transformation Ratio
ITPD	Impedance Transforming Power Divider
ITB	Impedance Transforming Balun
LNA	Low Noise Amplifier
LTE	Long Term Evaluation
MATLAB	Matrix Laboratory
mMIMO	massive Multiple Input Multiple Output
MN	Matching Network
NR	New Radio frequency bands of 5G standards
OC	Open Circuit
OMN	Output Matching Network
PA	power amplifier
PCB	Printed Circuited Board
PD	Power Divider
PhD	Phase Difference
PI	Phase Imbalance
SC	Short Circuit
SDR	Software Defined Radio
SIW	Substrate Integrated Waveguide
SMD	Surface Mounted Devices

TL	Transmission Line
TSTL	Two-section Transmission Line
TTS	T-Type Structure
UMTS	Universal Mobile Telecommunications Service (3G Broadband)
VNA	Vector Network Analyzer
vs	Versus
WCS	Wireless Communication System
WCDMA	Wideband Code Division Multiple Access
WiFi	Wireless Fidelity
WLAN	Wireless Local Area Network
WPD	Wilkinson Power Divider
w.r.t.	With respect to

List of Symbols

ε_r	Dielectric Constant of Material
μ	micro
ρ	Coupling factor of a coupled line
$\tan\delta$	Loss Tangent
B	Susceptance
f_0	Frequency of Operation
G	Conductance
k	Impedance Transformation Ratio
r	Frequency Ratio
R	Resistance
θ	Electrical Length
T_{even}	Transmission parameter in even-mode
X	Reactance
Y	Characteristic Admittance
Z	Characteristic Impedance
Z_{even}	Even-mode input impedance
Z_e	Even-mode impedance of a coupled line
Z_L	Load Impedance
Z_{odd}	Odd-mode input impedance
Z_o	Odd-mode impedance of a coupled line
Z_S	Source Impedance

Chapter 1

Introduction

1.1 Motivation

The confluence of a wireless communication system (WCS) along with the emerging applications such as internet of things (IoT) systems, cognitive radio systems, multiple-input multiple-output (MIMO) antenna systems, 5G, and compatible applications has been permeating the broader consumer electronics space at a rapid pace in the past few years. It has essentially turned WCS into a ubiquitous entity in the larger scheme of technology. A block diagram of a conventional WCS, depicted in Fig. 1.1, can readily aid in visualizing the overall system concept. It is apparent that the three vital elements of a WCS are the transmitter section, the receiver section, and the communication channel. The transmitter section processes an information signal for transmission purposes, which is transmitted through an antenna, whereas the receiver section receives the transmitted signal through an antenna and processes it for analysis or display purposes. Here, the communication channel serves as a medium for the signal flow from the transmitter to the receiver antenna. At the transmitter, a high-frequency carrier signal is used to modulate, i.e., to scale up the frequency, the information signal in a WCS to increase the transmission range and energy of the transmission signal. The handling of the high-frequency signals is done by the circuitry present at the transmitters (receivers) after its up-conversion from (before its down-conversion to) the base-band signal, i.e., the information signal. This set of circuits or components is referred to as a radio frequency (RF)

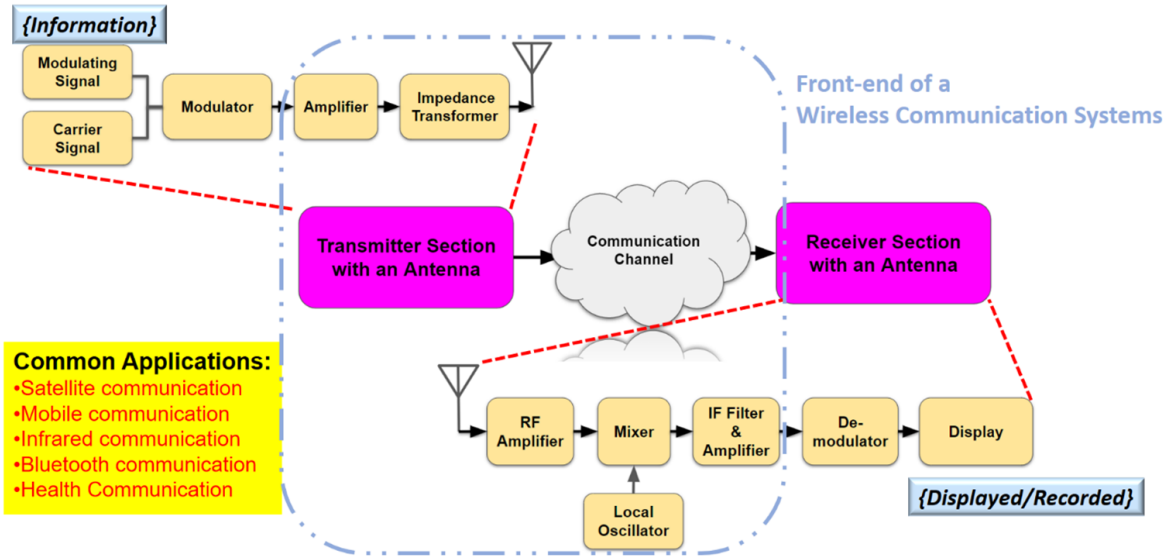


Figure 1.1: A generalized wireless communication system with Front-end subsystem.

front-end subsystem of a WCS. The RF front-ends at the transmitter and receiver are encircled in blue, as depicted in Fig. 1.1.

To reiterate, the perpetual emergence of wireless standards from earlier 1G to current 5G has also led to significant advancements in WCS infrastructure, including the RF front-ends and associated peripheral circuits and components. It has resulted in the facilitation of earlier only voice-type applications to more recent applications such as advanced mobile communications, satellite communications, internet services, WiFi, IoT networks, digital health, internet of things (IoT) devices, massive multiple-input multiple-output (MIMO) systems, energy harvesting, wireless power transfer, etc. [5, 8–31]. Moreover, the design and development of the evolving 5G front-end subsystem altogether with the existing infrastructure would be an added advantage, at least for the developing nations. It is due to the fact that the infrastructural setup of the existing communication technologies harmonizes with the FR1 frequency regime of 5G new radio (NR) bands and therefore stands out as a cost-savvy approach with minimal infrastructural amendments. All of these applications have necessitated the innovation in RF front-end components to seamlessly transition the infrastructure to satiate the requirements of the emerging wireless standards. For example, a conventional RF front-end of a radio receiver is required to support multiple wireless standards like a cellular network, WLAN, GSM, UMTS, Bluetooth, FM radio, GPS, etc. [28]. All of these standards operate at

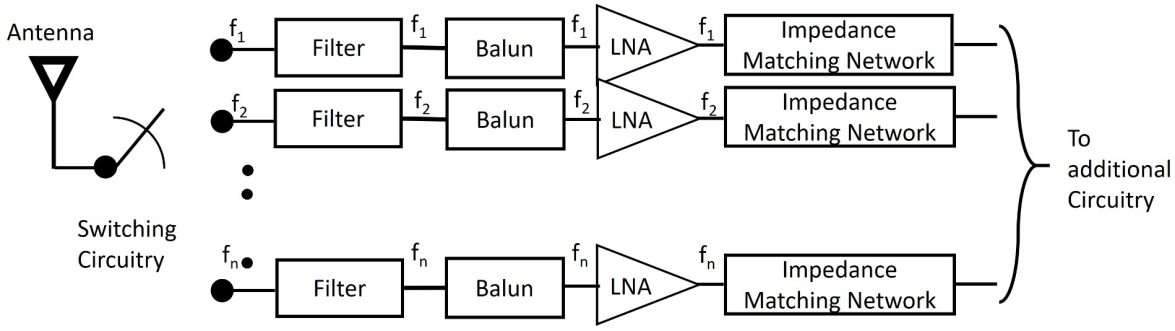


Figure 1.2: An example of conventional radio terminal with multiple devices for various RF inputs.

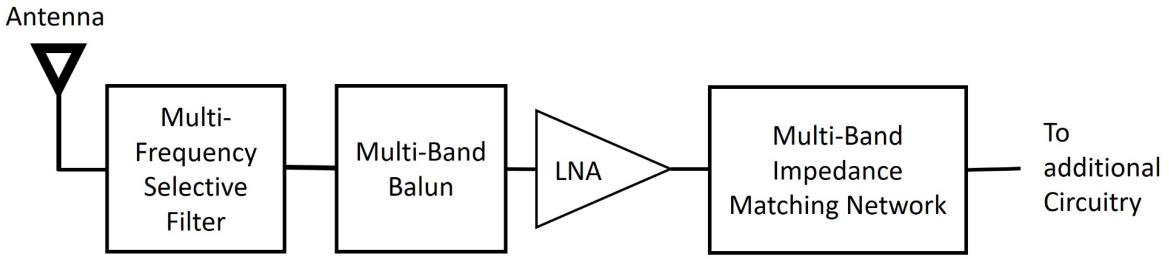


Figure 1.3: Proposed RF front-end incorporating multi-band components.

different frequencies individually, and therefore the front-end subsystem must be able to support these multiple frequencies. The conventional approach to design such systems for multiple frequencies is depicted in Fig. 1.2. Here, "n" different frequencies require "n" different filters, "n" different baluns, "n" different LNA, and "n" different impedance transformers in addition to other circuitry of the system, each working at an individual frequency. However, this solution will demand more circuit area, more cost, more power consumption due to transmission losses, more design complexity, etc. Alternatively, as depicted in Fig. 1.3, we propose to use just one set of multi-band front-end components that operate at the three distinct frequencies concurrently. This analogy is further elaborated in this thesis. Various configurations and architectures of the multi-functional RF front-end components are investigated, which are capable of performing distinct functionalities at distinct frequencies simultaneously. This has the potential to provide compactness, higher efficiency, cost-effectiveness as well as a single prototype solution to the burgeoning domain of front-end subsystems [29–31].

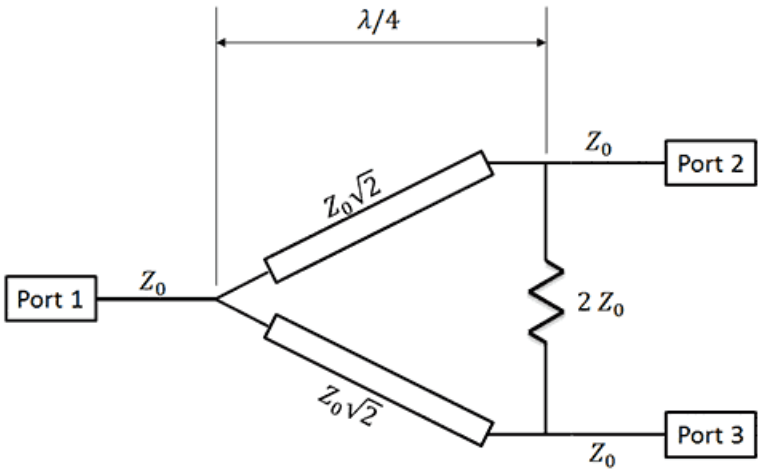
It is pertinent to convey that an ideal design entails RF front-end circuits to operate at a wide range of frequencies to support multiple wireless standards. Therefore, a wideband circuit can be a solution at the same time; however, achieving wideband operation is constrained by the well-known Bode-Fano criterion [32–34]. Also, the new 5G standards have two different bands spaced far apart, namely FR1 (450 MHz – 6 GHz) and FR2 (24.25 GHz – 52.6 GHz) [35]. As a consequence, the design of wideband components is not practically possible for the situation when the intended bandwidth covers two distinct communication standards far apart in terms of their carrier frequencies. In such situations, dual-band or multi-band matching could be extremely useful, considering that they can provide an optimum solution over a limited range of bandwidth around the chosen carrier frequencies of operation [36]. It can thus be inferred that the proposed innovative concept and the development of multi-band multi-functional circuits and systems would be able to facilitate the practical realization of existing and upcoming WCS standards and protocols.

1.2 Key Observations

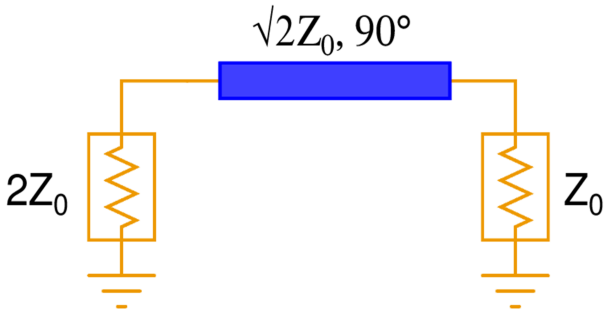
The recent developments in the design of RF and Microwave front-end components of a WCS are studied. The literature is replete with several techniques for the dual-band circuits and therefore provides the agreement on the cost-effectiveness over the conventional approach as depicted in Fig. 1.2. Moreover, some key observations highlight the attributes to support the motivation of the development of multi-functional components, which are articulated below.

1.2.1 Components of Wireless Communication System (Power Dividers as an example)

A Wilkinson power divider (WPD), key component of an RF front-end, is shown in Fig. 1.4. This configuration is used to distribute (or combine) the power at the output (input) port/s equally. The even-mode equivalent circuit of this power divider, depicted in Fig. 1.4(b) reveals that the transmission line (TL) is connected between the ports of different impedances of Z_0 and $2Z_0$. This TL acts as an quarter-wave impedance transformer with the characteristic



(a)



(b)

Figure 1.4: (a) A Wilkinson power divider and its (b) Even-mode half circuit.

impedance of $\sqrt{Z_0 * 2Z_0} = \sqrt{2 * Z_0}$ for the impedance matching [37]. The idea is, therefore, to explore this impedance transformation on the front-end circuits and components for variety of port terminations and not to limit it to just Z_0 to $2Z_0$.

1.2.2 Antenna Feedline

An antenna at the receiver or transmitter is used to either receive or transmit a signal, respectively. An antenna which can receive a signal as well as transmit a signal, is usually referred as transceiver antenna. These antennas are further connected to the front-end components for the RF signal generation and analysis purposes. For the maximum power transfer, it is made sure to minimize the return losses at the ports using impedance matching (transformation)

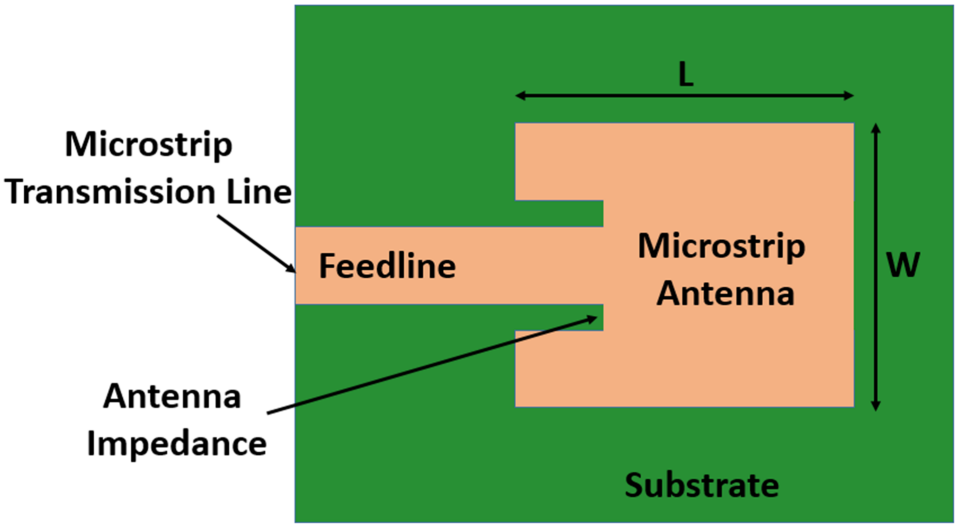


Figure 1.5: Patch antenna with feedline.

techniques. A feedline is generally used for the purpose. An example of a patch antenna with the feedline configurations is shown in Fig. 1.5.

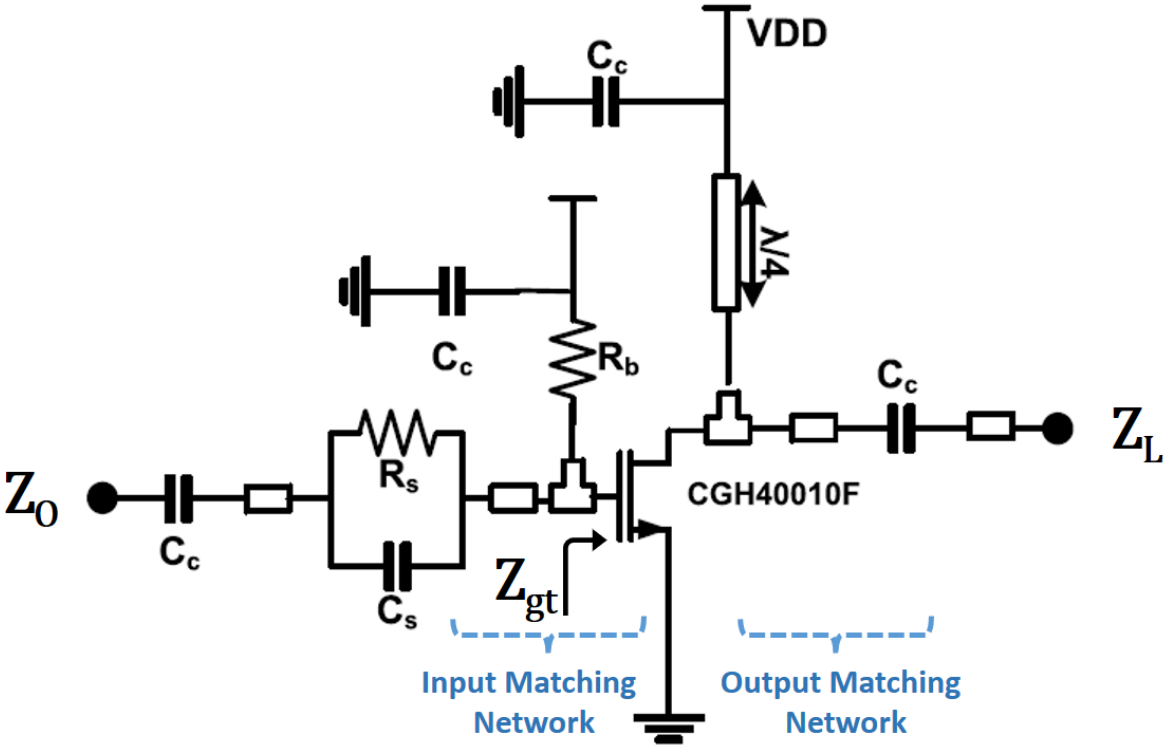


Figure 1.6: RF/Microwave single stage amplifier. Input and output matching networks are essential components [1].

1.2.3 RF Power Amplifiers

In previous examples, it has been seen that the impedance transformation is widely utilized techniques in Front-end subsystem. Not only for interconnections but design the individual RF component also incorporate the impedance transformers. The same has been attributed in an example configuration of an RF/microwave amplifier and is depicted in Fig. 1.6, where the input matching network (IMN) and output matching network (OMN) are required to match the complex impedance of the amplifier at the terminals with the port terminations, for e.g., Z_0 and Z_L. Just to reiterate, the impedances at the transistor terminals (Z_{gt}) can either be real or complex. The complex impedance may also be variable with the frequency in nature for the multi-frequency operations. For the dual-band amplifier the respective matching networks at the input and output must exhibit dual-band matching at the two frequencies of operations.

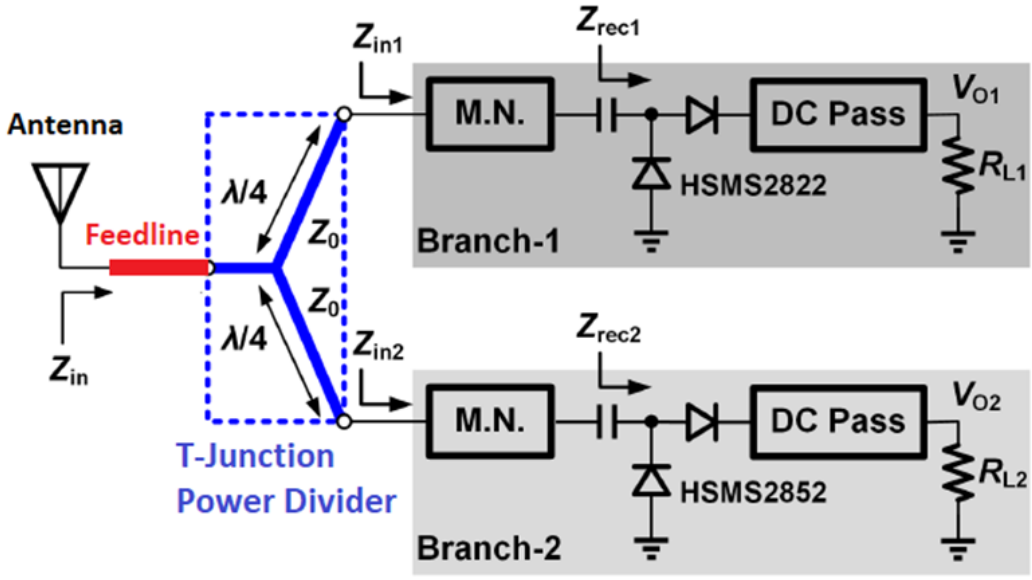


Figure 1.7: The example of a receiver architecture for the wireless power transfer.

1.2.4 Interconnections of a Wireless Communication System

Now, it is well justified that an impedance transformer is an ubiquitous block of a WCS and is used to provide the impedance matching between the ports of the front-end components for maximum power transfer and high efficiency purposes. Moreover, its omnipresence can be

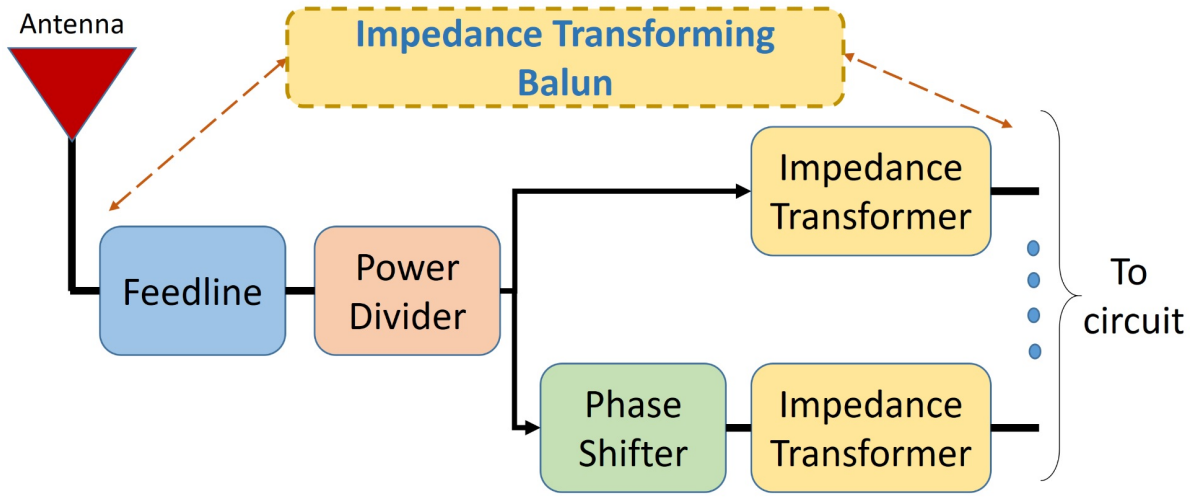


Figure 1.8: Example of a Front-end transceiver subsystem for a WCS.

further attributed in an RF front-end subsystem. For example, a situation can be visualized in Fig. 1.7, where a T-junction power divider is connected between an antenna and a dual-branch rectifier circuitry at its ports. The antenna uses a feedline while the circuitry has matching networks (M. N.) as the impedance transformer for the maximum power transfer.

1.2.5 Multi-functional Components of a Communication System

Similarly, we propose to obtain multiple inherent features in the RF circuits or components. For example, an impedance transforming Balun can be used instead of using five different components in a front-end subsystem as illustrated in Fig. 1.8. Moreover, a multi-band impedance transforming Balun reduces the circuit size multi-fold for the respective system. Not only the architecture with inherent features makes a system compact, but it also reduces the losses associated with the bigger circuit size to make the communication system more efficient. Further, the multi-feature component can also be integrated with the antenna to be fabricated on a single printed circuit board (PCB).

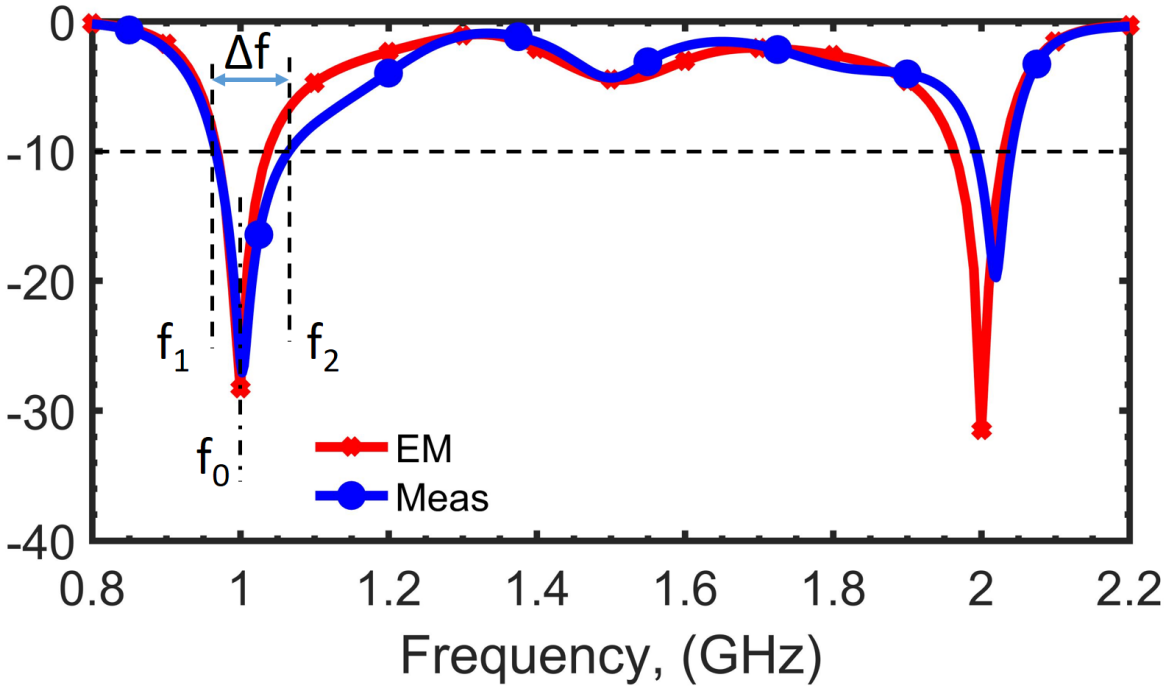


Figure 1.9: Fractional Bandwidth

1.3 Key Terminologies

Before discussing further, the relevant terminologies used in this thesis are articulated here, in brief. These terminologies are mentioned below:

1.3.1 Fractional Bandwidth

The fractional bandwidth (FBW) is the measure of the bandwidth at a frequency band. To understand, Fig. 1.9 can be followed. The term f_0 is depicting the design frequency and Δf is the difference between the higher cut-off frequency (f_2) and the lower cut-off frequency (f_1).

Then the fractional bandwidth can be defined as (1.1). The FBW is generally mentioned in percentage and that can be expressed as (1.2).

$$\text{FBW} = \frac{f_2 - f_1}{f_0} = \frac{\Delta f}{f_0} \tag{1.1}$$

$$\text{Percentage FBW} = \frac{(f_2 - f_1) * 100}{f_0}\% = \frac{(\Delta f) * 100}{f_0}\% \tag{1.2}$$

Figure 1.10: Impedance Transformation Ratio

1.3.2 Frequency Ratio

This is a vital performance measuring metric in any multi-band circuits and systems. In the domain of the dual-band circuits and system, frequency ratio refers to the ratio of the higher frequency of the two frequency bands in the domain of dual-band circuits to the lower frequency (f_1). The frequency ratio is denoted by r throughout this thesis.

$$\text{Frequency Ratio}(r) = \frac{f_2}{f_1} \tag{1.3}$$

Where the term f_1 is the lower frequency in Hz and f_2 is the higher frequency in Hz.

1.3.3 Impedance Transformation Ratio

The impedance transformation ratio is a vital characteristic of the impedance transforming architectures. The impedance transformation refers to the ratio of the load impedance to the source impedance and vice-versa.

In this thesis, the impedance transformation ratio of a component, as depicted in Fig. 1.10, refers to the ratio of the load impedance (Z_L) to the source impedance (Z_S), unless defined specifically. The impedance transformation ratio is denoted by k throughout this thesis.

$$\text{Impedance Transformation Ratio}(k) = \frac{Z_L}{Z_S} \tag{1.4}$$

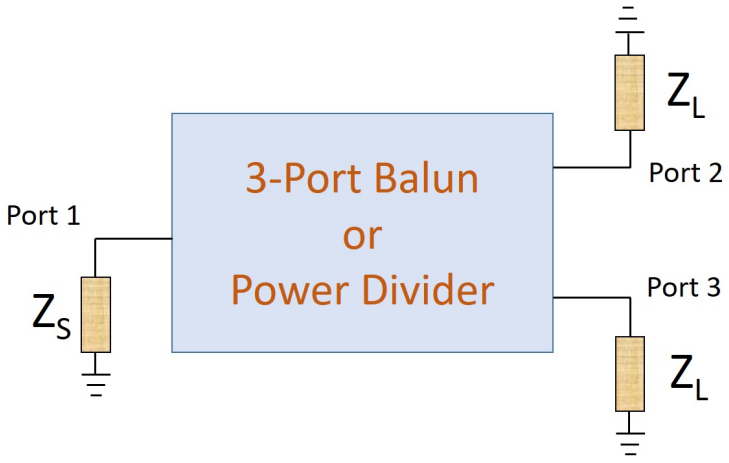


Figure 1.11: Amplitude and Phase Imbalance for a 3-Port Component

1.3.4 Amplitude Imbalance

In the context of a power divider or Balun, as depicted in Fig. 1.11, the amplitude imbalance is the difference between the amplitude of the output signals. The amplitude imbalance is a figure of merit for the power divider and balun architectures.

$$\text{Amplitude Imbalance} = \|S_{21} - S_{31}\| dB \tag{1.5}$$

1.3.5 Phase Imbalance

In the context of a power divider or Balun, as depicted in Fig. 1.11, the phase imbalance can be defined as the deviation in the phase from the required phase difference between the two output ports. The required phase difference is 180° for the balun architectures. For the power divider architectures, it may vary with the requirements; however, within the scope of this thesis, the required phase difference for the power dividers is 0°.

The phase imbalance is also a figure of merit for the power divider and balun architectures.

$$\text{Phase Imbalance } (^\circ) = \|\text{required phase difference} - (\angle S_{21} - \angle S_{31})\| \tag{1.6}$$

1.3.6 Microstrip Compatibility

The term microstrip compatibility is related to the realization of a microstrip transmission line on a printed circuited board (PCB). There are fabrication challenges associated with the PCB manufacturing machines and processes to design a TL of specific dimensions on a PCB board. The microstrip dimensions are calculated based on the design theory associated with the RF and Microwave circuits and components.

Therefore, a circuit is said to have high microstrip compatibility if the realizable design parameters can be computed for the wide range of design specifications.

1.4 Thesis Objectives

During the course of investigations, a number of problems associated with the existing designs and corresponding design techniques are identified. The proposed concept envisages a unified space rather than developing and assembling additional connecting lines and individual components. The solutions have the potential to bring the paradigm shift in the approach such systems are designed. The proposed architectures and the design techniques in this thesis provide an initial design report for the development of future communication systems.

The key objective of this thesis is to investigate the multi-functional circuits and components to eliminate the redundant impedance transformers and other uni-functional devices [29–31]. Moreover, the developed design analysis should also provide a first pass solution while enabling the quick prototyping. The proposed developments have the potential to reduce the circuit and system complexities of the WCS by bringing a paradigm shift. Overall, the objectives of this thesis can be listed as:

- Enhancement of Frequency Ratios.
- Enhancement of Impedance Transformation Ratios.
- Inherent impedance transformation with concurrent Impedance Transformation and Frequency Ratios.
- Design and development of Multi-functional Circuits and Components.

- Planar and simplified architectures of the WCS circuits and components.
- Systematic design analysis backed by sound and simple analytical formulations to enable quick prototyping.
- Innovative design strategies to obtain high microstrip compatibility (re-configurable architectures).

1.5 Major Research Contributions

Based on the set objectives of the thesis, several architectures of the circuits and components of a WCS are developed to provide novel solutions. These solutions contribute to addressing the existing design challenges. The major contributions of this thesis are summarized below, along with the relevant publications.

1.5.1 Development of Impedance Transformers

The design and development of the RF and Microwave circuits and components are provided. Initially, the impedance transformers are investigated considering the omnipresence in any communication system. The impedance transformers with very high impedance transformation ratios are provided. Moreover, this thesis contributes to the dual-band impedance transformers working at two arbitrary frequencies with concurrent ultra-high impedance transformations.

1.5.2 Inherent Impedance Transformation in the RF Circuits and Components

The impedance transformers are the ubiquitous components of a WCS which are used to transform the impedance of a circuit or component to its source and load ports. This highlights the omnipresence of an impedance transformer in a communication system. It is, therefore, investigated to integrate the RF components with the impedance transformation capability to eliminate the very common impedance transformers from the system. Several impedance transforming architectures with very high inherent impedance transformation is provided in

this thesis. The developed components also exhibit dual-band performance with high and arbitrary frequency ratios.

1.5.3 Multi-functional Circuits and Components

The motivation section of the thesis articulates the need and advantages of multi-functional circuits and components. It should be noted that the increased requirement of features from a single component limits the design flexibility, and therefore, the literature is deficient with the concurrent impedance transformation and frequency ratio. If available, the range of achievable impedance transformation and frequency ratio is very limited, specifically. One of the contributions is to provide the dual-band power divider with inherent impedance transformation for the arbitrary impedance environment at the source and load. No such feature from a dual-band power divider or combiner is present in the literature.

The list of inherent features within the scope of this thesis are listed below:

1. High impedance transformation ratio.
2. High frequency ratio.
3. Concurrent high impedance transformation ratio and high-frequency ratio.
4. Real, complex, and frequency-dependent complex impedance transformations.
5. DC blocking or DC Isolation.
6. Balanced to unbalanced signal transformation and vice-versa.
7. Differential phase shifts.

1.5.4 Simplified Architectures with Analytical Design Analysis

Though several research focuses on the design and development of the RF and Microwave components with the capabilities of frequency ratios, impedance transformation ratio, and multi-functional features in the literature, they lack with the simplified uni-planar architectures. Moreover, it is not very common to find the mathematical formulations on the proposed

technique. One of the major contributions of this thesis is the development of simplified architectures backed with sound and simple analytical formulations. The design analysis also articulates the closed-form equations and the systematic design procedure to calculate the design parameters easily, which enables the designers with the quick prototyping of the circuits and components.

1.5.5 Innovative Design Strategy for the Enhanced Design Flexibility and Reconfigurability

Finally, the design analysis intuitively strategies the provided design procedure to obtain the high microstrip compatibility. This is due to the fact that the design analysis provides the independent design variables and choice of the architecture configuration. The independent design variables can be set freely within the realizable span of microstrip compatibility, which relaxes the design parameters which are bounded by the mathematical formulations. Moreover, the intuitive variation of electrical lengths and choice of short- and open-stub configurations are used to enhance the design flexibility or reconfigurability of the proposed circuits and components for the wide range of design specifications.

1.6 Organization and Presentation of the Thesis

The major contributions of this thesis can be broadly categorized into three parts. Firstly, the improvement on the individual features of the RF and Microwave components are addressed and accomplished. Secondly, which is the major part of this thesis, the multi-functional components with single- and dual-band of operations are discussed. Specifically, the challenge of achieving concurrent high impedance transformation ratios and frequency ratios is addressed. Finally, the impedance transforming power dividers for arbitrary varying impedance environments at the two arbitrary frequencies are discussed and addressed. These concepts are further elaborated in the respective chapters as described.

Chapter 2 of the thesis provides an intense literature review on the design and developments of the components of the wireless system. Initially, the designs of impedance transformers are

studied and investigated for the achievable impedance transformations and frequency ratios. Further, the investigations on the multi-functional components are elaborated. Specifically, these components are studied for the two attributes, namely frequency ratio and impedance transformation ratio.

Chapter 3 illustrates the microstrip transmission lines and their characteristics for some of the design conditions. The microstrip line is further utilized to develop the designs of phase shifters for wideband performance.

Chapter 4 presents the design and development of the dual-band impedance transformers. The impedance transformers are also investigated for the high impedance transformation ratio. The application of the impedance transformation property is also discussed in the design of the dual-band Power Divider.

Chapter 5 delves into the design of multi-functional components. These multi-functional components are articulated for the additional but inherent features. The DC isolation, useful for the DC feeds in the application of power amplifiers and unbalanced to balanced signal transformation useful for the antenna feeds, are discussed. Further, in addition to DC isolation, inherent phase shifting, and balanced to unbalanced signal transformation, the attributes of frequency ratio and impedance transformation ratio are investigated in detail. The components with concurrent high-frequency ratio and impedance transformation ratio are discussed in detail.

Finally, Chapter 6 illustrates the application scenario of the impedance transforming components where the impedance varies with the variation of frequency. The frequency-dependent complex loads are discussed, and subsequently, the impedance transforming power dividers are proposed for real, complex, and frequency-dependent complex impedances.

In the end, the achievements of the thesis are concluded in Chapter 7. This chapter also highlights both the immediate as well as long term future research possibilities in this area.

Chapter 2

Literature Review

A wireless communication system (WCS) is everywhere nowadays and is a key part of our lives. It is one of the fastest-growing technology with most of the applications including our day – to – day life such as mobile communications, Wi-Fi communications, Bluetooth, internet of things (IoT) devices, smart home automation, wireless radios, digital health, 5G new radio (NR), massive multiple-input multiple-output (MIMO) systems, energy harvesting, wireless power transfer, etc. [5, 8–31]. The design and development of the ever-advancing WCS has necessitated the design and development of the front-end circuits and components such as impedance transformers, power dividers, phase shifters, couplers, baluns, RF power amplifiers, filters, etc. capable of operating at multiple frequencies or wideband frequency spectrum [2, 3, 21, 36, 38–62].

2.1 A Review on Impedance Transformers

In an RF front-end sub-system of a communication system, there are several circuits and components connected all together to establish the communication. The interconnects are made up of transmission lines to handle the RF signal flow (propagation). Conventionally, the impedance of these transmission lines is selected to be universal 50 Ω as a compromise between the minimum attenuation and maximum power capacity [37]. Therefore, all the circuits and components are also transformed to 50 Ω at its connection ports using an impedance transformer if possessing different impedances for the uniform connection purposes. The role

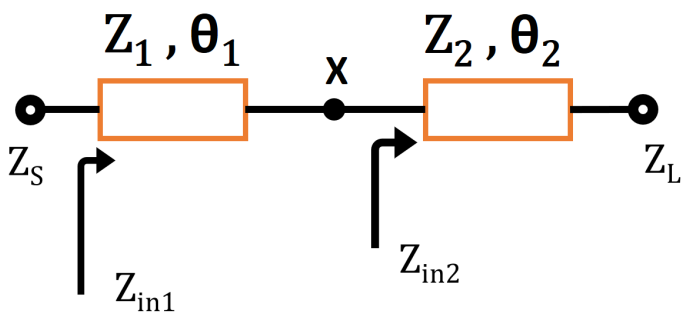


Figure 2.1: Two section transmission line impedance transformer [2]

of RF impedance transformers is more significant in RF and Microwave circuits and systems considering the premium attached with the available power at high frequencies [63–65]. The discussion also indicates the importance and omnipresence of impedance transformers in the front-end of a WCS. Therefore, the impedance transformers are selected as first choice to investigate for the existing developments and find out the scope of improvement on the state-of-the-art.

2.1.1 Real-to-Real Impedance Transformation

Impedance matching or transformation is one of the key aspects often required in electronic circuits and systems for matching unequal impedance environments at the ports. All of these impedance transformers have their existent as a dominant component in various applications of the WCS such as RF front-end [66, 67], wireless power transfer [13–15], energy harvesting applications [16–18], and antenna feed applications [18, 68, 69] to indicate a few. In RF circuits and systems, micro-strip transmission line impedance transformers are the most popular ones considering the ease of fabrication for the prototyping purposes. There have been reports of many matching techniques to address the needs of a variety of applications [70–73], and these can be broadly categorized into single-band and multi-band impedance transformation approaches [2, 4, 57, 59, 60, 74–82]. A quarter-wave impedance transformer is widely appreciated conventional design for the impedance transformation for real-to-real impedances. However, it is limited for the single band of operation only [37]. The last decade has seen emerging wireless applications with multiple wireless standards and hence resulted

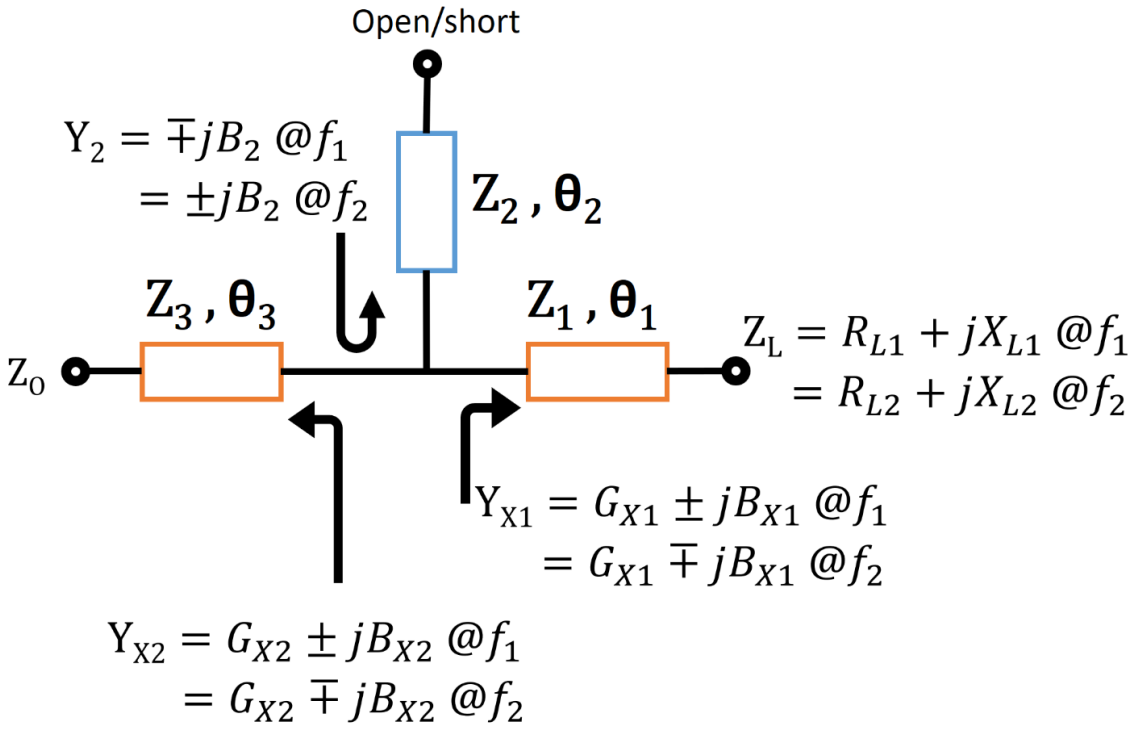


Figure 2.2: T-type impedance transformer for FDCL loads [3]

in the requirements of multi-band transformation techniques [2, 4, 48, 50, 57, 59, 60, 74–77]. For the dual-band of operation, one of the most cited impedance transforming architecture with two stepped-transmission lines was proposed almost two decades ago [2]. Though the proposed architecture was able to provide very high k and r theoretically, a case study reveals that this impedance transformer faces fabrication challenges on FR4 substrate for k beyond 8.0 at $r = 3$. Other popular impedance transformers include L-type network [83] and the coupled-line based design [48] to match real source and load impedances at two arbitrarily selected design frequencies. Recently, a real-to-real dual-band impedance transformer [59] was reported which utilizes slow-wave architectures to achieve the impedance transformation at two arbitrary design frequencies.

2.1.2 Real and Complex Impedance Transformation

Some of the recent designs report innovative techniques to achieve a high impedance transformation ratio (k) and high frequency ratio (r) so that they can find usefulness in the design

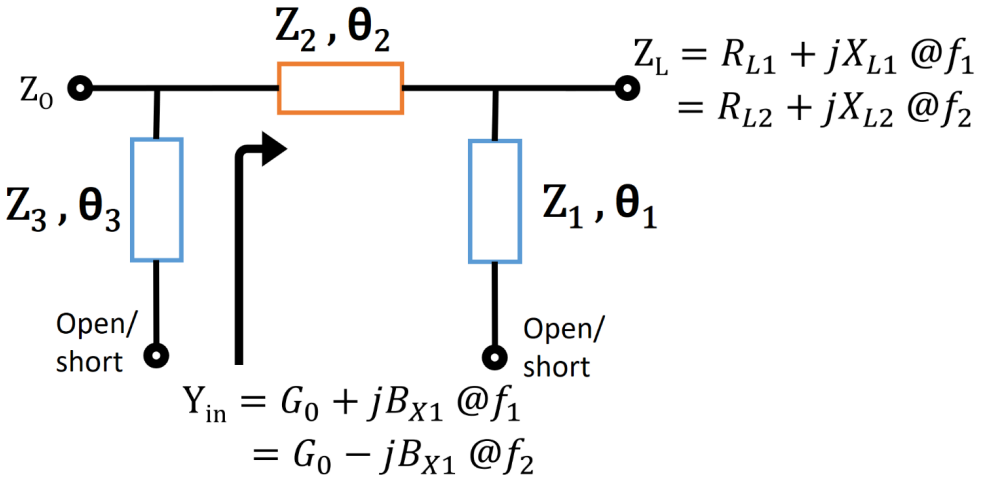


Figure 2.3: π-type impedance transformer for FDCL loads [4]

of modern wireless communication system components. Though the designs provide real-to-real impedance transformation [79, 84–87] and real-to-complex impedance transformations [3, 4, 75, 76, 88], but these are limited with either single-frequency operation or lesser frequency ratio. The microstrip compatibility is often found limited with the reported structures for concurrent high k and high r. Several short- and open-stubs based architecture were also reported recently to mitigate the high impedance transformation challenges [3, 4, 75, 76]. The short-/open- circuited stubs, used at the ports of a single transmission line (TL), provide the dual-band complex impedance transformation [3, 4]. The T-type structure (TTS) [3] is depicted in Fig. 2.2 while the π-type structure (PTS) [4] is depicted in Fig. 2.3, respectively. These structures transform the frequency-dependent complex impedance to real impedance at the two arbitrary frequencies. Other examples with similar stub based architectures are of three stepped transmission line with three short- or open-circuited shunt stubs [75], and three stepped transmission line with two short-/open-circuited shunt stubs [76]. In these designs, the role of the stubs is to provide a transmission zero in addition to the required impedance matching. A ladder based network for the impedance transformation can be used for the multi-band impedance transformation, but it suffers from increased size and design complexities with the increasing number of bands [77]. In [87], a broadband IT with an impedance transformation ratio of 5 based on the 4:1 Guanella-transformer has been demonstrated. In [85], a matching network for transforming ratio of 5 has been designed using coupled-line and shunt open-stub.

Table 2.1: List of Impedance Transformers with High Impedance Transformation Ratios [*Calculated as the ratio of real parts of the port impedances, **Calculated as the ratio of the maximum to minimum operating frequency]

Ref	Venue	Technique	Maximum r	Maximum k
[2]	TMTT 2003	Two Section Stepped TL	7	20
[40]	MOTL 2011	Planar TL with a coupled-line	2.5	15.36*
[4]	MWCL 2015	Planar TL with stubs	1.5	5*
[76]	TCPMT 2016	Planar TL with stubs	1.94	4
[75]	MWCL 2017	Planar TL with stubs	1.66	1.35*
[57]	TCAS II 2017	T-Type network with load healing	2.5	5*
[60]	MWCL 2017	Dual-Transmission Line	5.2	10
[77]	EL 2018	Coupled-line with ladder network	1.5**	9.13*
[59]	ECTC 2019	Coupled-lines	3.88	4

Two-section parallel coupled-lines have been employed to design a UHTR IT in [79]. This UHTR IT achieves a transforming ratio of 10 with a fractional bandwidth of 8.27%. In [84], two UHTR ITs have been developed based on the short-ended coupled-line sections for a transforming ratio of 20. An IT has been designed using a modified coupled-line structure for the transforming ratio of 5 [88]. The concurrent high-frequency ratios and high impedance transformation ratios are proposed by the recent impedance transformer circuits [60, 89, 90] but the achievable transformation is less though good for the intended applications. Moreover, most of the designs either lack with the systematic design procedure with analytical solutions for the quick prototyping or the detailed investigation on the range of impedance transformations and frequency ratios.

In order to summarize the lacunae on the available literature, the two important attributes of some high-performance impedance transformers are listed in Table 2.1. The impedance transformation ratio for the complex impedance transformations signifies the ratio of the real part of the load impedance to source impedance. It should be noted that the maximum achiev-

able r or k of the available impedance transformers are limited with most of the impedance transformers. If the individual impedance transformer provides high k, the achievable r is quite low [40, 77]. Only, [2] claims to provide the high r and k concurrently. However, a case study reveals that this impedance transformer faces fabrication challenges on FR4 substrate (with substrate thickness 1.5 mm and permittivity of 4.7) for k beyond 8.0 at $r = 3$. To clarify it further, the TL width is calculated to be 0.1 mm for the mentioned specifications (k = 8.0 at r = 3.0). Therefore, dual-band impedance transformers with high frequency separations, simultaneously, are of much interest to explore and improve the state-of-the-art while providing the high microstrip compatibility.

2.2 A Review on Power Dividers

More often, the RF signals propagating through the RF and microwave circuits and interconnects are distributed to other branches (or path) of the system or combined to a single path for the signal analysis and conditioning purposes. This operation is performed by the power dividers or combiners (or couplers) in the communication system. The power dividers are also one of the popular key passive components in the RF/Microwave system. The researchers have focused on the innovations in the domain of PD considering that it is sort of *sine qua non* in communication infrastructure [36, 45, 91–99]. The plethora of applications of a PD can be found in such as antenna feeder networks, push-pull amplifiers, mixers, baluns, I/Q vector modulators, antennas transceiver systems, and phase arrays for signal-division or combination [36, 36, 45, 45, 92, 93, 95, 96, 98, 99, 99, 99–105]. Furthermore, the development of multi-band wireless components with multiple inherent features is a win-win situation as it significantly aids in size miniaturization, cost reduction, reduced power requirements, and ease of design and fabrication. These innovations have the potential to bring a paradigm shift in the design of circuits and systems for a myriad of applications ranging from rectenna, wireless power transfer, energy harvesting, and internet of things as they will bring reduction in both the size as well as conservation in RF/microwave energy [14, 16]. Several recent reports [7, 36, 96, 99, 103–106, 106, 106–114] have presented the dual- and multi-band operation of a power divider in detail where miniaturized size, low insertion loss, good isolation, wide

band-ratio, and high impedance transformation ratio is the center of interest. The WPD [106] consists of a complex isolation structure with lumped components though demonstrating good performance. In dual-band WPDs, the dual-frequency quarter wave-length equivalent blocks are used to provide the dual-band operation, but it is limited in band-ratio [108]. The reports [106, 109, 110] demonstrate the improved performance at the expense of complex isolation with lumped components, which restricts the operation at higher frequencies. The coupled lines are also used in the reports [111, 112] for the possibility of the miniaturization and its advantage of having an additional degree of freedom in terms of even- and odd-mode impedances. The report [113] utilizes the port matching concept to enhance the performance, but the limitation is with the isolation resistor which is eventually a continuous function of the band-ratio. A design based on extended port [103] delivers the enhanced performance in terms of port matching and isolation. Furthermore, the isolation resistor, here, is not dependent on the band-ratio.

2.3 Multi-functional RF/Microwave Components Augmented with Impedance Transformation

Moreover, the rapid advancement in multi-band/multi-standard RF/Microwave communication systems encourages the design and development of re-configurable and multi-functional components [115–117]. Subsequently, there has been an increased interest in the design and development of multi-functional components [29, 62, 79, 98, 117–124]. These components demonstrate that the more than one functionalities are achieved inherently in a multi-functional circuit without any compromise in its performance. There is a vast scope of development in plethora of such areas for example inherent filtering [29, 117, 123], dc isolation [117, 119], impedance transformation ratio [118, 119, 124], balanced to unbalanced transformation [118, 125, 126], antenna element [116], phase shifting [125], frequency ratio [29, 127], etc. In support to this thesis contributions, the power dividers and baluns with high frequency ratio, high impedance transformation ratio, balanced to unbalanced transformation, phase shifting, and isolation are further reviewed.

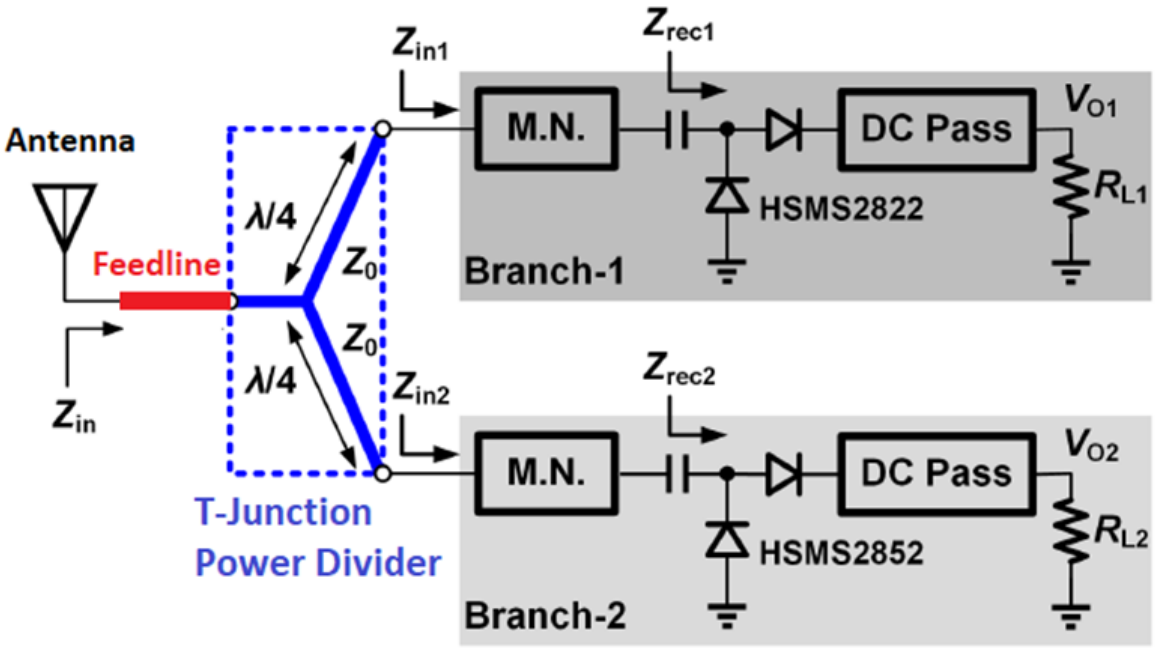


Figure 2.4: A generic depiction of wireless power transfer front-end [5].

The literature review on the designs of PDs is introduced in section 2.2. The emergence of advanced wireless technology has also seen a recent surge in impedance transforming PDs [5, 36, 45, 95, 97–99, 105, 128]. This has been necessitated by the fact that often there exists a wide impedance variation between the ports of PDs and interconnecting circuit blocks. At first, the inherent impedance transformation is an interesting feature for the front-end components as they discard the need for additional impedance transformers. Furthermore, the multi-functional component provided such benefits up to a greater extent. For example, a glimpse of such applications is visualized in Fig. 2.4 where a PD is connected with an antenna at the input port, and a dual-branch rectifier circuitry at the output ports [5]. The antenna has a feedline, and the rectifier circuitry has a matching network (M.N.) for the necessary impedance transformation for the maximum power transfer. Apparently, an impedance transforming power divider (ITPD) in such cases has the potential to bring a paradigm shift in the way such systems are designed. At the outset, it is pertinent to mention that, irrespective of the multi-frequency or single-frequency circuits or systems, often the practical situations entail complex, real, or combination of these port impedances and PDs are no different [91, 95, 96].

Many of these designs have addressed the inherent impedance transformation issues but often find limited usefulness emanating from complex design schemes, non-planar architecture, incorporated reactive elements, variable nature of impedance environments at the ports, capability in achieving higher frequency ratios (r) and impedance transformation ratios (k), etc. There are a few reports of ITPDs with varied nature of real and complex impedance scenarios at the ports, but these can operate at a single frequency only [94–98]. The impedance transformation in a PD with dual-band operation is also reported, but it suffers from very low k [99]. Another dual-band PD (DBPD) with inherent impedance transformation has a little improvement on k, but the achievable r is limited [45]. The r is improved significantly in [36], but the k is again limited. Additionally, the design utilizes an admittance inverter to replace the conventional TL, which has resulted in a large architecture. The validation of the impedance transformation from the fabricated prototype is also absent. In addition to all the limitations within the reported dual-band ITPDs, all of these are exposed to the real port terminations only. Unfortunately, neither of the reported designs explore the varied nature of impedance environments, such as frequency-dependent complex loads (FDCLs), at their respective ports. There is one recent report on dual-band PD which utilizes the complex load for the matching purposes [129]. Here, the PD consists of a combination of reactive components to obtain the complex load, but it is a port of the circuit and not any impedance transformation at any port. There is no dual-band ITPD that can handle the arbitrary frequency-dependent complex loads (FDCLs) at both the input and output ports. It is thus clear that literature is rarely available with the design techniques to achieve the dual-band impedance transformation for varying impedance environment, and there is an emergent need for the design and performance evaluation of such PDs with benchmarking of isolation, amplitude, and phase performance.

Again, to summarize the lacunae on the literature of impedance transforming and dual-band components, Table 2.2 is provided on the basis of two attributes, i.e., r and k. Additionally, the individual contributions are compared with the state-of-the-art in this thesis. While discussing the impedance transforming components, it should be noted that the impedance transformation is an inherent attribute of a component here, unlike the impedance transformers, which are only intended to provide the impedance transformation. These inherent capabilities may reduce the design flexibility, which is apparent in the reduced ranges of the r and k of the listed components

Table 2.2: Maximum Achievable Frequency Ratios and Impedance Transformation Ratios of Impedance Transforming and Dual-Band Components

Reference	**Venue**	**Component**	**Maximum r**	**Maximum k**
[130]	TMTT 2001	Balun	NA	3.2
[131]	TCPMT 2014	Coupler	NA	2
[105]	MWCL 2014	Power Divider	0.34-3	2
[99]	MWCL 2015	Power Divider	2.32<r<6.01 2.44<r<7.31	80/120 (k=0.67) 100/130 (k=0.77)
[41]	Access 2016	Balun	2.58<r<4.61 2.75<r<4.22 2.91<r<3.87	50/50 (k=1) 75/50 (k=1.5) 100/50 (k=2)
[132]	MWCL2017	Balun	4.6	NA
[133]	MWCL2017	Crossover	1.76-3.50	NA
[58]	TCAS-II 2018	Power Divider	1-7	NA
[98]	TMTT 2018	Unbalanced-to-balanced Power Divider	NA	4
[134]	TMTT 2018	Power Divider	>7 for higher θ	NA
[135]	MWCL 2018	Coupler	NA	5
[136]	Access 2019	Balun	2.16	6

in Table 2.2. It can be seen that if a component has high r, the maximum achievable k of the component is either not discussed or is very less [58, 99, 134]. Similarly, if the maximum achievable k is high, the r is limited [135, 136]. Though it is not very common in the literature to provide the individual r and k more than five each, the concurrent high r and k is very rare. Furthermore, there is no impedance transforming architecture which can cater to the arbitrary frequency-dependent complex loads (FDCLs) at both the input and output ports.

2.4 A Summary of the Literature Review

There have been several advancements in the domain of single- and multi-band passive components with the rich and vast literature. It is also administered that many existing lacunae have been addressed over the years through the valuable research outcomes. However, an extensive literature survey on the specific domain of single- and dual-band multi-functional architectures,

some of the shortcomings and research gaps are identified to cope up the ever-advancing growth of the WCS. These are summarized below:

1. **Frequency Ratio is Limited:** As explained, the requirement with multi-faceted multi-standard communication system requires operation at multiple frequencies simultaneously. For example, the literature is limited to provide a design of RF component operating at GSM downlink (900 MHz) and WiFi-LTE (5.8 GHz) due to wide band separation. Therefore, the components with arbitrarily high frequency ratios are very effective in handling such scenarios. The Tables 2.1 and 2.2 demonstrate the limited ranges of the frequency ratio in the available literature.

2. **Impedance Transformation Ratio is Limited:** Another important aspect is impedance transformation, which is widely discussed above. The impedance transformation ratio with an impedance transformer or the inherent impedance transformation with an RF and Microwave component is limited as per the literature. Most of the available designs are limited to a fixed reference port impedance (e.g., 50 Ω). One of the major contributions of this thesis is in the improvement of the impedance transformation ratios of the RF and Microwave components of the front-end system. The Tables 2.1 and 2.2 demonstrates the limited ranges of the impedance transformation ratio from the available literature. Furthermore, the concurrent operation of k and r put a high trade-off, and therefore the ranges with concurrent operations are very limited.

3. **Multi-band Multi-Functional Components are Advantageous:** The cost-effective solutions are always of high interest. The proliferation of the growing wireless market has necessitated the development of multi-band multi-functional RF circuits and components to reduce the transmission losses and size of the communication system. Other than multi-functional performance, the thesis highlights the r and k attributes of the multi-band multi-functional components.

4. **Re-configurability can be improved:** The reconfigurability of the circuits and components is highly desirable for cost-effective solutions. The reconfigurability of a circuit enables it to work for a wide range of design specifications. The literature is rarely

available for high r and k concurrently. This is due to the inability of these architectures to follow the realizable limits of the design parameters. The reported work of this thesis, however, provides independent design variables and choices in the reported configurations to achieve high reconfigurability and thus the improved micro-strip compatibility for the circuits.

5. **Simplified Architectures with Systematic and Analytical Design Solutions are very effective:** It is also rare in the literature to find the closed-form mathematical solutions. The analytical solutions for the proposed circuits and components play a major role in order to enable the quick prototyping. From the designers' point of view, it is effective to develop the circuits with the aid of mathematical formulations rather than much emphasis on the EDA tools and optimization algorithms.

Chapter 3

Transmission Lines based Components: Phase Shifters as example

3.1 Transmission Lines

A transmission line is a two conductor system used for the propagation of the electromagnetic signals. ***The effects of a transmission line becomes significant when the length of the transmission line is comparable or higher than the wavelength of the signal frequency.*** Some common examples of a transmission line are coaxial cables, twin-line cable, microstrip line, stripline, etc [37]. In this thesis, the microstrip line is used for the design and development of the circuits and components of the WCS. And therefore, the microstrip line is elaborated further in this section.

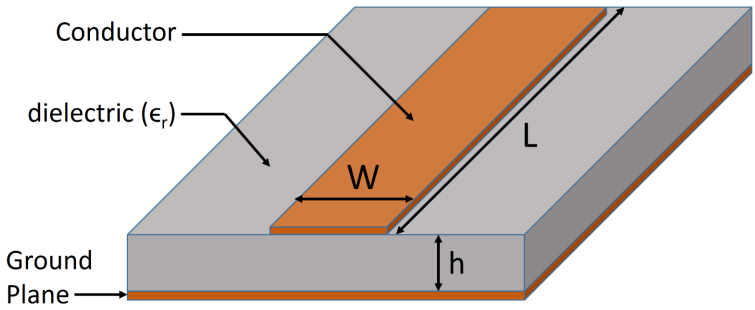


Figure 3.1: Microstrip Transmission Line

Figure 3.1 depicts a microstrip transmission line where a conductor is separated from a ground plane by a dielectric substrate having permittivity (ε_r). The example resembles a two-sided printed circuit board (PCB) where the conductor layer and the ground plane are shown. The length and width of the conductive transmission line are depicted as "L" and "W". The dielectric substrate is also depicted with thickness "h". Usually, both the layers are of conductive material, and one of the layers is used to design the circuit (while other acts as ground plane). The microstrip transmission line structures are one of the most convenient options for the prototyping purposes and have been widely used [91–94].

3.1.1 Characteristic Impedance

The characteristic impedance (Z_0) is a critical parameter of a transmission line and can be defined as ***the input impedance of a transmission line when its length is infinite***. For the microstrip transmission line, the characteristic impedance is a function of the ratio of the height of the substrate to the width of the transmission line [37].

3.1.2 Lossless Transmission Lines

Figure 3.2 depicts a lossless TL, generally referred as ideal TL, terminated in an arbitrary load impedance Z_L. The input impedance of the transmission line can be expressed as (3.1) [37].

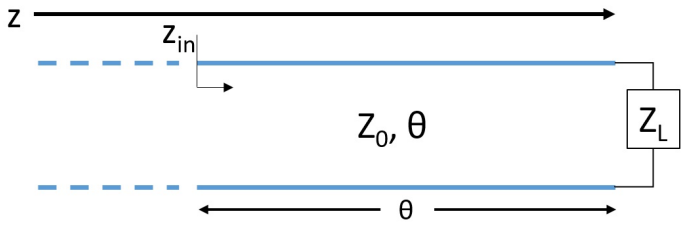


Figure 3.2: Transmission line terminated with load

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan\theta}{Z_0 + jZ_L \tan\theta} \tag{3.1}$$

Subsequently, the input impedance expressions for the specific load conditions are deduced in further sections below:

3.1.2.1 Case 1: Short-Circuited Line

In the short-circuited condition, the transmission line is terminated at a *short circuit* which is $Z_L = 0$. Putting $Z_L = 0$ in (3.1), the input impedance reduces to (3.2).

$$Z_{in} = jZ_0 \tan\theta \tag{3.2}$$

3.1.2.2 Case 2: Open-Circuited Line

In the open-circuited condition, the transmission line is terminated to a *open-circuit* which is $Z_L = \infty$. Putting $Z_L = \infty$ in (3.1), the input impedance reduces to (3.3).

$$Z_{in} = -jZ_0 \cot\theta \tag{3.3}$$

3.1.2.3 Case 3: Matched Condition

The matched load condition signifies that the transmission line is terminated with the characteristic impedance of the transmission line which can be written as $Z_L = Z_0$. Putting $Z_L = Z_0$ in (3.1), the input impedance for the matched condition reduces to (3.4).

$$Z_{in} = Z_0 \tag{3.4}$$

And therefore, the input impedance of a transmission line terminated with its characteristic impedance is equal to the characteristic impedance irrespective of the transmission line length.

3.2 Application of the Microstrip Transmission Line

As defined above, a transmission line is just a conductive medium for the propagation of the electromagnetic signals when the length of the transmission line is comparable or higher than the wavelength of the signal frequency. This effect is significant at RF/microwave frequencies and therefore the microstrip line circuits are well established for the design and development of the RF/microwave circuits and components. Some of the examples of these circuits include impedance transformer, balun, power divider, phase shifter, etc. [2, 4, 8, 9, 21, 36, 45, 48, 50, 53–55, 59–61, 65, 75–77, 79, 95–99, 137].

As an example, phase shifters are designed using the microstrip transmission line. Two different architectures of the microstrip phase shifters are proposed and discussed in the next section. Phase shifters are key components in WCS applications such as power dividers, band pass filters, phase-array antennas, mobile satellite systems, etc. [138, 139]. The initial and very popular phase shifter designed using coupled line, called Shiffman phase shifter [54], exhibited a bandwidth of approximately about 80% with a phase ripple of 10°. Two proposed phase shifters are discussed in this chapter. One phase shifter utilizes the loaded transmission line while another phase shifter utilizes T- and Pi- Networks for the desired phase shift. The WCS applications does require variable phase shifts too and one of the proposed wideband phase shifters is useful for such situations.

3.3 A brief Literature Review for Phase Shifters

Phase Shifters are critical component in many RF and Microwave systems that are used to vary the phase of an incoming signal. The most significant application of the phase shifters is in phased array antennas where the antenna beam is steered.

A phase shifter is introduced by Schiffman [54] which has a main line built around a shorted coupled line and a simple transmission line serves as the reference line. However, it was based on a stripline that for specific bandwidth requirements, often necessitated very tight coupling. Various improvements over the Schiffman phase shifter using cascade and parallel combination of shorted coupled line have been introduced [140–142], but again, tight coupling is still required. The implementation of a phase shifter using selectively etching the underneath of the coupled lines and placing material of different permittivity to change the even and odd mode impedance values is an interesting idea [143]. A return loss better than 10 dB and a bandwidth up to 70% have been achieved by doing so, but this phase shifter requires a longer procedure. Phase shifters reported in [144, 145] provide wide bandwidth, but these designs also require a multilayer fabrication process which increases their fabrication cost and may not be compatible with other parts of the circuit. A design using stub loaded line reported in [146] has relatively smaller insertion loss and could provide bandwidth up to 82%. Some other interesting designs have been reported in the literature as well [147–150] and their

performance is given at the end of this chapter in the comparison section; majority of them rely on multilayer processing. A technique to utilize single reference line and multiple main lines to achieve different phase shifts was reported in [151], and can provide 45% bandwidth with a phase deviation of 5° and with an insertion loss up to 0.9 dB. While in [152] the main line is formed by changing the position of the stubs and could attain a bandwidth of 55.6% with a return loss up to 0.7 dB considering a phase deviation of 8°, the multilayer technique reported in [153] achieves a bandwidth of 112%. A modified version of the Shiffman phase shifter with the reference line also comprising of a coupled line was reported in [43], while [154] is limited to providing only 180° phase shift.

3.4 Design of L-Shaped Phase Inverter

The proposed phase shifter has two lines, as shown in Fig. 3.3. The lower transmission line having characteristic impedance Z_M and electrical length θ_M is the reference line for the main line i.e. upper line. The main line includes two sections of transmission line which are loaded with a short stub to form an L-shape. The respective characteristic impedances and electrical lengths of the transmission line sections and stubs are Z_1, Z_2, and Z_S and θ_1, θ_2, and θ_S, respectively. The transmission line sections are assumed to be non-dispersive, and hence, its characteristic impedance is assumed to be frequency independent.

3.4.1 Design Analysis of the Proposed Phase Shifter

The ABCD parameters of the main line can be written as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta_1 & jZ_1\sin\theta_1 \\ jY_1\sin\theta_1 & \cos\theta_1 \end{bmatrix} \begin{bmatrix} \cos\theta_2 & jZ_2\sin\theta_2 \\ jY_2\sin\theta_2 & \cos\theta_2 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_{in} & 1 \end{bmatrix} \tag{3.5}$$

Where $Y_{in} = jb = -jY_S\cot\theta_S$. Furthermore, if the transmission line sections are assumed to be of same electrical length i.e., $\theta_1 = \theta_2 = \theta$ then:

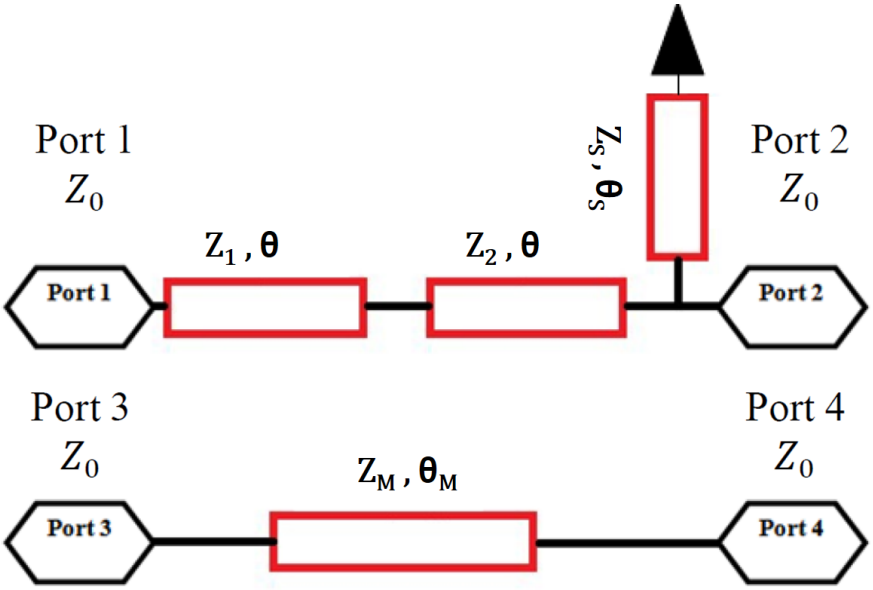


Figure 3.3: Proposed structure of phase inverter

The simplification of (3.5) results into:

$$A = \cos^2\theta - Z_1 Y_2 \sin^2\theta + \frac{jb(Z_1+Z_2)\sin 2\theta}{2} \tag{3.6a}$$

$$B = \frac{j(Z_1+Z_2)\sin 2\theta}{2} \tag{3.6b}$$

$$C = j[\frac{Y_1 + Y_2 sin2\theta}{2} + b(cos^2\theta - Y_1 Z_2 sin^2\theta)] \tag{3.6c}$$

$$D = cos^2\theta - Y_1 Z_2 sin^2\theta \tag{3.6d}$$

The relevant scattering parameters of the main line in terms of ABCD parameters can be expressed as:

$$S_{11} = \frac{Z_0 A + B - Z_0^2 C - Z_0 D}{Z_0 A + B + Z_0^2 C + Z_0 D} \tag{3.7a}$$

$$S_{21} = \frac{2Z_0}{Z_0 A + B + Z_0^2 C + Z_0 D} \tag{3.7b}$$

Where Z_0 is impedance of all the ports.

Equations (3.6) and (3.7) can be further simplified to achieve the following expressions:

$$S_{11} = \frac{E + jF}{G + jH}\ ; \quad S_{21} = \frac{2}{G + jH} \tag{3.8}$$

Where,

$$E = (Y_1Z_2 - Z_1Y_2)sin^2\theta - \frac{b(Z_1+Z_2)sin2\theta}{2} \tag{3.9a}$$

$$F = \frac{\frac{Z_1+Z_2}{Z_0} - Z_0(Y_1+Y_2)}{2}sin^2\theta - Z_0b(cos^2\theta - Y_1Z_2sin^2\theta) \tag{3.9b}$$

$$G = 2cos^2\theta - (Y_1Z_2 + Z_1Y_2)sin^2\theta - \frac{b(Z_1+Z_2)sin2\theta}{2} \tag{3.9c}$$

$$H = \frac{\frac{Z_1+Z_2}{Z_0} + Z_0(Y_1+Y_2)}{2}sin^2\theta + Z_0b(cos^2\theta - Y_1Z_2sin^2\theta) \tag{3.9d}$$

$$\tag{3.9e}$$

Now for the phase shifter to be operating ideally, $S_{11} = 0$ and S_{21} should satisfy the following.

$$S_{21} = \|S_{21}\|e^{j\phi} = 1.e^{j\phi} \tag{3.10}$$

Where, ϕ is the phase shift through the main line. Now using the condition of $S_{11} = 0$ in the simplification of (3.8) results in E=0 and F=0, simultaneously. For this to hold true, following condition should be met:

$$\tan\theta = \frac{b(Z_1+Z_2)}{Y_1Z_2 - Z_1Y_2} = \frac{bZ_1Z_2}{Z_2 - Z_1} \tag{3.11}$$

Eventually, the relationship between Z_1 and Z_2 can be deduced by simplification of (3.8) and (3.11).

$$(Z_2^2 - Z_1^2)(Z_1Z_2 - Z_0^2) = Z_0^2\{(Z_2 - Z_1)^2 - b^2Z_1Z_2^3\} \tag{3.12}$$

Furthermore, (3.8) and (3.10) can be solved to find a generic expression for phase shift through the main line as:

$$\tan\phi = \frac{Z_0^2b(1 - Y_1Z_2tan^2\theta) + tan\theta\{Z_1 + Z_2 + Z_0^2(Y_1+Y_2)\}}{2Z_0(1 - Y_1Z_2tan^2\theta)} \tag{3.13}$$

Eventually, insertion loss can be calculated from S_{21} and S_{11} and the phase shift, $\Delta\delta$, at the design frequency can be calculated as [146]:

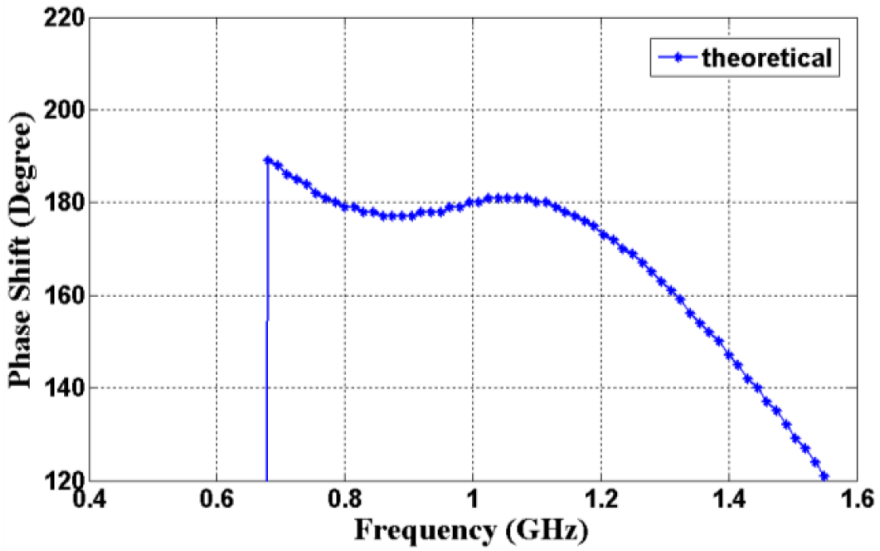


Figure 3.4: Calculated phase response of the proposed phase shifter

$$\Delta\delta = \phi - phase(S_{43}) \tag{3.14}$$

The equations (3.11)-(3.14) are the design equations for the proposed phase inverter.

3.4.1.1 Calculation of Phase difference

For achieving ϕ=90° from the main line, the expression in equation (3.13) simplifies to:

$$tan^2\theta = \frac{Z_1}{Z_2} \tag{3.15}$$

If the electrical length of the two transmission line segments in the main line is selected as θ=60° and substituted in (3.15) then we obtain:

$$Z_1 = 3Z_2 \tag{3.16}$$

The equations (3.11) and (3.16) can be further solved to obtain the relationship between the stub susceptance, b and the transmission line impedance, Z_1, as:

$$b = (\frac{-2}{\sqrt{3}})\frac{1}{Z_2} \tag{3.17}$$

The values of impedances Z_1 and Z_2 for achieving ϕ = 90° through the main line, of electrical length θ = 60°, can be obtained by solving (3.12), (3.16), and (3.17). The calculated

Table 3.1: Dependence of bandwidth on the stub electrical parameters

Z_S (Ω)	θ_S (°)	**Bandwidth Ratio**
29.79	40	1.549:1
25	45	1.603:1
20.97	50	1.657:1

values are Z_1 = 86.6 Ω and Z_2 = 28.868 Ω. From (3.17), the calculated susceptance comes out to be b = -0.04. There can be multiple values of stub electrical parameters Y_S ($1/Z_S$) and θ_S for achieving this value of susceptance. For example, if we choose $\theta_S = 45°$ then the impedance of the stub should be Z_S = 25 Ω. Now, the characteristic impedance of the reference line should be chosen as Z_M = 50 Ω for achieving match at ports 3 and 4. For the ideal scenario, theoretically the phase shift through the reference line should be 270°, that is, $\theta_M = 270°$ for this design to work as phase inverter as conveyed by (3.14). Then, the phase difference provided by the phase shifter is $\Delta\delta$ = 90°-(-90°) = 180°.

If all the transmission line segments are considered ideal, then from the above calculations, the achieved phase shifter performance at the chosen design frequency of 1 GHz is depicted in Fig. 3.4. The phase shifter performance is calculated near the design frequency and it can be seen that the phase shifter provides the required phase inversion at the design frequency of 1 GHz, i.e., phase shift of 180°. Moreover, considering the phase inversion tolerance of 4° into account, the proposed phase shifter has the potential to achieve the phase inversion over a bandwidth ratio of 1.6035:1, i.e., f_u/f_l:1. Here, f_u is the higher cutoff frequency and f_l is the lower cutoff frequency for the accepted tolerance.

3.4.1.2 Discussion on Effect of Stub Parameters on Bandwidth

From theoretical derivation, it can be seen that the electrical parameters of stub can be varied using b= - 0.04 = - $Y_S \cot\theta_S$ without affecting the matching condition at the ports. The achieved bandwidth for a set of Y_S and θ_S is given in Table 3.1.

It is apparent that the bandwidth ratio can be increased by increasing the electrical length of the stub. However, in the proposed design, the electrical length cannot be increased beyond 50° because of the sharp increase in the phase error in the phase inversion.

Table 3.2: Electrical Parameters of Design

Impedance	**Value (Ω)**	**Electrical Length**	**Value (°)**
Z_1	86.6	θ_1	60
Z_2	28.86	θ_2	60
Z_S	20.97	θ_S	50
Z_M	50	θ_M	270

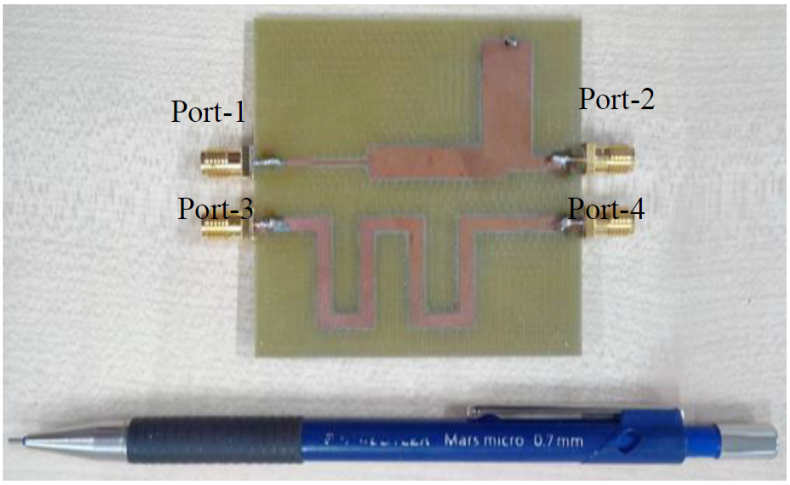


Figure 3.5: The developed prototype of the proposed phase inverter

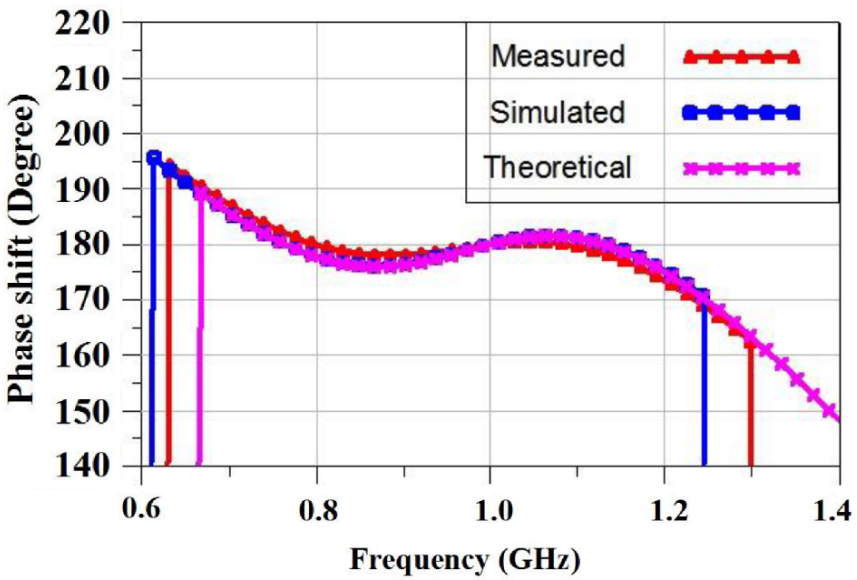


Figure 3.6: Comparison of measured, theoretical, and simulated phase shift performance

Table 3.3: Measurement of the Phase Inverter

Parameter	Simulated Value	Measured Value
Phase Shift (°)	180	180
S_{11} (dB)	-85	-45
S_{12} (dB)	-0.2	-0.3
Phase Error (°)	4	4
Bandwidth Ratio	1.7:1	1.5:1

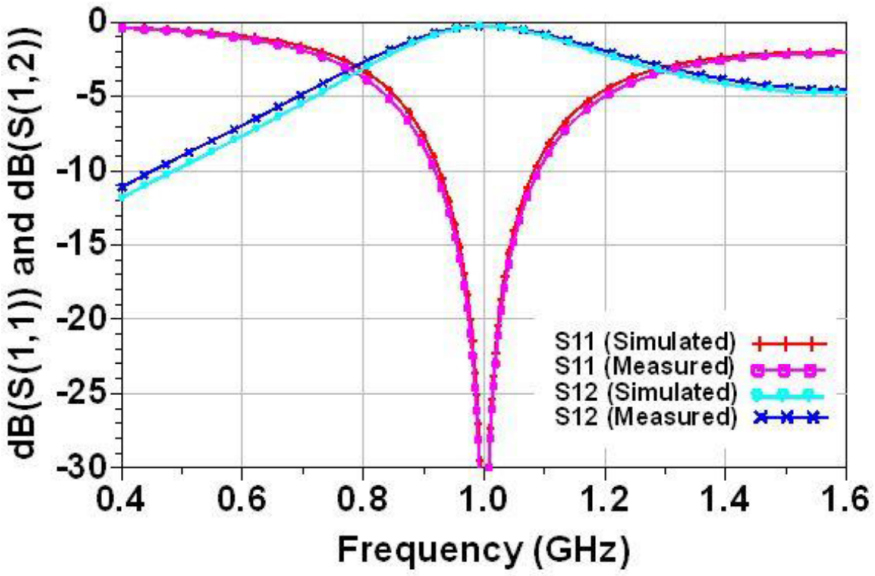


Figure 3.7: Comparison of measured and simulated S_{11} and S_{12}

3.4.2 Design Examples and Discussion

For validation purposes, all the port impedances of 50 Ω at design frequency of 1 GHz are selected. From Table 3.1, it is apparent that the best performance can be achieved for Z_S=20.97 Ω while other design parameters are kept same. For easy references, all the design parameters are summarized in Table-3.2. For these parameters, the corresponding simulated performance is given in Table-3.3.

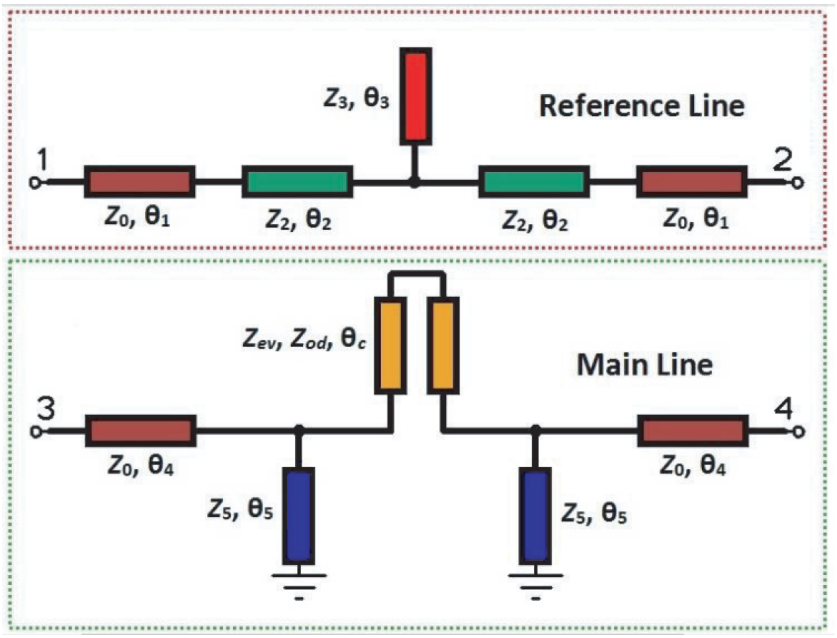


Figure 3.8: Schematic diagram of the proposed phase shifter.

3.4.3 Fabrication of the Proposed Phase Shifter and Measurement Results

Subsequently, a prototype, shown in Fig. 3.5, was developed on FR4 substrate with substrate thickness 1.524 mm and $\varepsilon = 4.7$. The measured phase performance along with the theoretical and simulated values, is depicted in Fig. 3.6. Here, theoretical results are the calculated values from the design equations (3.11)-(3.14) which are derived following the ideal TL theory. The simulated results are the optimized EM simulation performance of the circuit on a EDA tool, i.e., Keysight ADS for this case. Finally, the measured results are the results from the fabricated prototype when measured using a Vector Network Analyzer (VNA). It is apparent that the measured results match well with the theoretical and simulated results. In addition, it is also evident that for a tolerance of 4° in the phase shift, phase inversion over a bandwidth of approximately 430 MHz can be achieved around the design frequency of 1 GHz.

Finally, in order to check the matching /transmission at port-1 to understand the potential return/insertion loss, measurement and simulation was carried out for S_{11} and S_{12}. The result depicted in Fig. 3.7 verifies a very good matching and insertion loss performance at the chosen design frequency of 1 GHz.

3.5 Phase Shifter with Improved Bandwidth

The schematic of the proposed phase shifter is depicted in Fig. 3.8. To illustrate how we arrive at the proposed phase shifter configuration, it is pertinent to recall that there are normally two lines in a differential phase shifter, the main line and the reference line. For example, in [147] a Pi-network is used as the main line, and a simple transmission line (TL) serves as the reference line. In contrast, a T-network is used in [146] as the main line. It implies that the T- and Pi-networks have similar phase responses. Though a simple transmission line is utilized as the reference line in these reports, theoretically, any two-port network can be chosen as the reference line. The important requirement is that both the main two-port network and the reference two-port network, must have the same phase slope ($d\angle S_{21}/df$) [152]. We, therefore, present a novel phase shifter that uses a Pi-network as the main line and a T-network as the reference line. In addition, since coupled lines give extra degrees of design freedom due to their even and odd mode characteristic impedance parameters, the middle transmission line section in the Pi-network is replaced with shorted coupled lines. The coupled lines have even- and odd-mode impedances z_{ev} and z_{od}, respectively, and an electrical length of θ_c. The arms of Pi-network has a characteristic impedance z_5 and electrical length θ_5. An extra TL section having characteristic impedance z_2 and length θ_2 has been added in the T-network to compensate for any small imbalances in the phase response, return loss or transmission coefficient by varying its parameters. The open stub of T-network having characteristic impedance z_3 and electrical length θ_3 provides an extra degree of freedom, where θ_3 independently makes the design procedure more flexible. The terminating TL sections at the ports have characteristic impedance z_0 and the electrical lengths θ_1 and θ_4 in the reference and the main line, respectively.

3.5.1 The Design Analysis

The required differential phase is the difference between the phases of the main and the reference networks:

$$\Delta\phi = \angle s_{43} - \angle s_{21} \tag{3.18}$$

In addition, it is required that there must no insertion loss in both the paths and all the four ports must be matched, and therefore, the following conditions exist:

$$\|s_{21}\| = \|s_{12}\| = \|s_{43}\| = \|s_{34}\| = 1 \tag{3.19}$$

$$\|s_{11}\| = \|s_{22}\| = \|s_{33}\| = \|s_{44}\| = 0 \tag{3.20}$$

$$s_{11} = s_{22} = \frac{(j+\tan\theta_1)\{z_2^3\tan^2\theta_2 + 2(z_0^2 - z_2^2)z_3\tan\theta_2\cot\theta_3 + z_0^2 z_2\}}{(\tan\theta_1 - j)(z_0 + jz_2\tan\theta_2)\{z_0(2z_3\tan\theta_2\cot\theta_3 + z_2) + jz_2(z_2\tan\theta_2 - 2z_3\cot\theta_3)\}} \tag{3.21}$$

$$s_{21} = s_{12} = \frac{j2z_0z_2z_3(j+\tan\theta_1)\cot\theta_3\sec^2\theta_2}{(\tan\theta_1 - j)(z_0 + jz_2\tan\theta_2)\{z_0(2z_3\tan\theta_2\cot\theta_3 + z_2) + jz_2(z_2\tan\theta_2 - 2z_3\cot\theta_3)\}} \tag{3.22}$$

$$s_{33} = s_{44} = -\frac{(\tan\theta_4 + j)\{z_0^2(z_{ev}\cot\theta_5\cot\theta_c - z_5)(z_5\cot\theta_c + z_{od}\cot\theta_5) + z_5^2 z_{ev}z_{od}\cot\theta_c\}}{(\tan\theta_4 - j)\{z_0z_5 - z_{ev}\cot\theta_c(z_0\cot\theta_5 + jz_5)\}\{z_0(z_5\cot\theta_c + z_{od}cot\theta_5) + jz_5z_{od}\}} \tag{3.23}$$

$$s_{43} = s_{34} = \frac{jz_0z_5^2(\tan\theta_4 + j)(z_{ev}\cot^2\theta_c + z_{od})}{(\tan\theta_4 - j)\{z_0z_5 - z_{ev}\cot\theta_c(z_0\cot\theta_5 + jz_5)\}\{z_0(z_5\cot\theta_c + z_{od}cot\theta_5) + jz_5z_{od}\}} \tag{3.24}$$

$$\begin{aligned}\angle s_{21} = \tan^{-1}\frac{\tan\theta_1\cot\theta_3\sec^2\theta_2)}{-\cot\theta_3\sec^2\theta_2} \\ -\tan^{-1}\frac{\begin{array}{r}\theta_1\{z_2\tan\theta_2 + z_3\cot\theta_3(\tan^2\theta_2 - 1)\} - 2z_0^2(2z_3\tan\theta_2\cot\theta_3 + z_2) \\ + 2z_2^2\tan\theta_2(z_2\tan\theta_2 - 2z_3\cot\theta_3)\end{array}}{\begin{array}{r}z_2\tan\theta_2 + z_3\cot\theta_3(\tan^2\theta_2 - 1) + 2z_0^2\tan\theta_1(2z_3\tan\theta_2\cot\theta_3 + z_2) \\ - 2z_2^2\tan\theta_1\theta_2(z_2\tan\theta_2 - 2z_3\cot\theta_3)\end{array}}\end{aligned} \tag{3.25}$$

$$\begin{aligned}\angle s_{43} = \tan^{-1}\frac{z_0z_5^2\tan\theta_4(z_{ev}\cot^2\theta_C + z_{od})}{-z_0z_5^2(z_{ev}\cot^2\theta_C + z_{od})} \\ -\tan^{-1}\frac{\begin{array}{r}z_0^2(z_{ev}\cot\theta_5\cot\theta_C - z_5)(z_5\cot\theta_C + z_{od}\cot\theta_5) - z_5^2z_{ev}z_{od}\cot\theta_C \\ + z_5z_0\tan\theta_4\{z_5(z_{od} - z_{ev}\cot^2\theta_C) - 2z_{ev}z_{od}\cot\theta_5\cot\theta_C\}\end{array}}{\begin{array}{r}z_5z_0\{z_5(z_{od} - z_{ev}\cot^2\theta_C) - 2z_{ev}z_{od}\cot\theta_5\cot\theta_C\} \\ + z_0^2\tan\theta_4(z_5 - z_{ev}\cot\theta_4\cot\theta_C)(z_5\cot\theta_C + z_{od}\cot\theta_5) + z_5^2z_{ev}z_{od}\tan\theta_4\cot\theta_C\end{array}}\end{aligned} \tag{3.26}$$

Since both the lines are symmetric and thus the even-odd mode analysis is invoked and the resulting S-parameters are obtained as mentioned in Eqs. (3.21) - (3.26). In order that both the

networks' phase variations are similar with frequency, an additional condition on the phase slope of both the networks holds true [152]:

$$\frac{d\angle s_{43}}{df} = \frac{d\angle s_{21}}{df} \tag{3.27}$$

For a required differential phase, Eqs. (3.18), (3.19), (3.20) and (3.27) are solved using MATLAB with the help of the closed-form S-parameters obtained in Eqs. (3.21) - (3.26). It is noted that some of the design parameters can be chosen independently. It is also important to note that for a required differential phase, there could be overwhelming computational burden while enforcing the conditions set by Eqs. (3.19), (3.20), and (3.27), and we may even get some unrealizable design parameters. Since, normally achieving 10–20 dB return loss is adequate for all practical purposes, it is justified to relax $|S_{11}|$ requirement (from its ideal value of ∞ dB) to enhance the computational speed. Similarly, 0.5 dB–1 dB insertion loss is common over a wide bandwidth, relaxing $|S_{21}|$ form its ideal value of 0 dB a bit helps speed up the computation. Thus, it is recommended that rather than solving for the ideal return and insertion losses, we can, for example, allow a VSWR of 1.1 to 1.3 and a transmission loss of 0.04 to 0.06 to obtain a realistic solution with considerable ease. As an alternate the optimization techniques available with EDA tools can be utilized with such relaxations. Yet another constraint is placed on the characteristic impedances of various microstrip lines in the proposed phase shifter as for a physically realizable design these values must line between 20 Ω and 140 Ω. Finally, since in a design incorporating coupled lines their gap may constrain the fabrication; the minimum coupled lines gap in this work is assumed to be 0.25 mm, which further helps the choice of z_{od}.

3.5.2 Variation on the Differential Phase Shifts

Following these guidelines, variation of the design parameters with the required phase shift is obtained. Fig. 3.9 shows this variation for the differential phase ranging from 45° to 120°. It must be noted that this curve is not unique as z_{od}, z_2, and θ_3 are independent variables and they can assume any value as far as the design constraints are satisfied. The current plot is obtained considering these parameters to be 36 Ω, 50.5 Ω, and 7.5°, respectively. This choice is motivated noting that z_2 cannot be much far from 50 Ω and length of its stub should be as

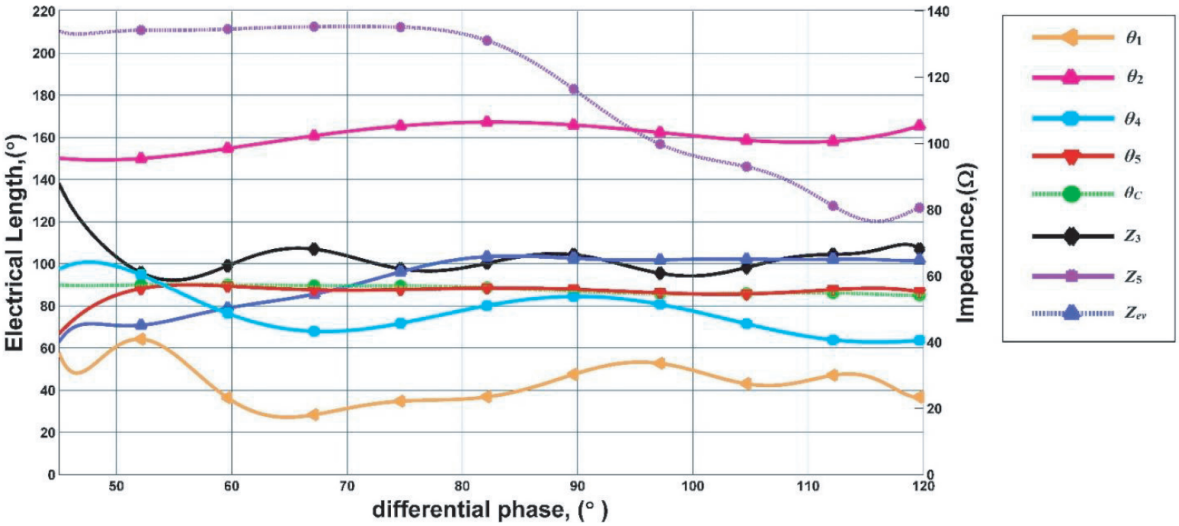


Figure 3.9: Design parameters of the proposed phase shifter for different phase shifts.

Table 3.4: The design parameters of the proposed phase shifter (θ_i in (°) and Z_i in (Ω))

Parameters	**Phase Shift**					
	120°	105°	90°	75°	60°	45°
θ_1	37.2	42	48	32.40	30.2	58
θ_2	167	158	164	168	154	150
Z_3	67	65	64	63.5	66	132
θ_4	63.3	65	84.4	75.8	65.9	97.4
θ_5	86.8	87	86.8	88.7	88.3	88
Z_5	80.8	94	118	135	135	134
θ_C	85.1	86.1	86.1	89.1	90.2	90
Z_{ev}	65	65	40	62	50	40

small as possible considering that ports 1 and 2 of the reference T-network are to be matched. Furthermore, z_{od} is considered on a lower side to achieve a practically realizable design as it has a relationship with z_{ev} in terms of $\rho = z_{ev}/z_{od}$, and typically for ease of fabrication ρ lies between 1 and 4 [155].

The values of various design parameters can easily be read from Fig. 3.9 and the Table 3.4, for example, list these parameters for the phase variation from 45° to 120° at an interval of 15°. The design examples listed in Table 3.4 are simulated using the Keysight Advanced Design System (ADS) and the results are depicted in Figs. 3.10, 3.11, 3.12, 3.13, and 3.14. Fig. 3.14 shows the variation of differential phase shifts with the frequency for different simulation examples. The wideband characteristic of the proposed phase shifter for all the

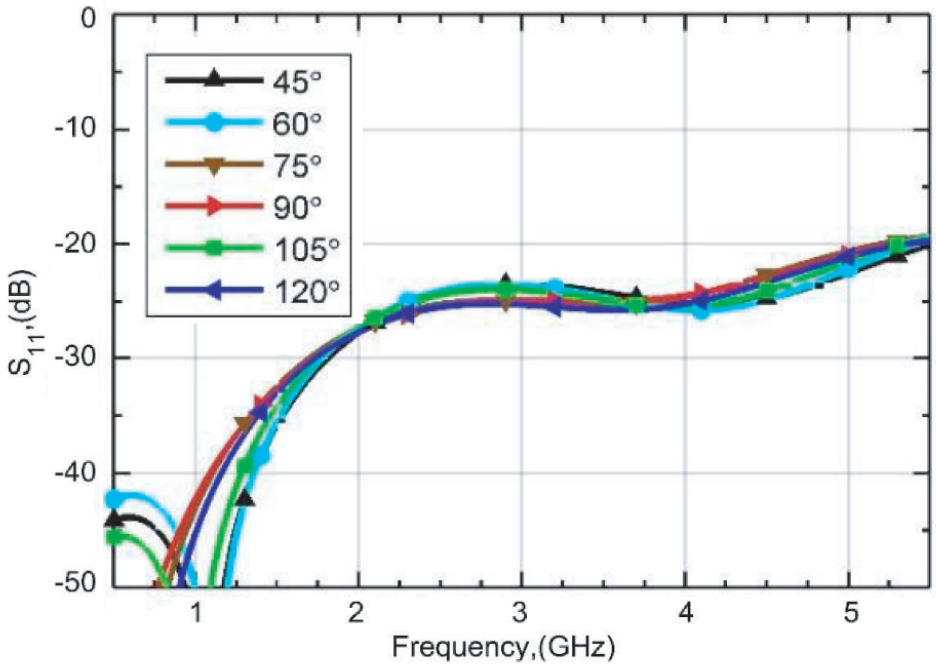


Figure 3.10: Simulated S_{11} of design cases listed in Table 3.4.

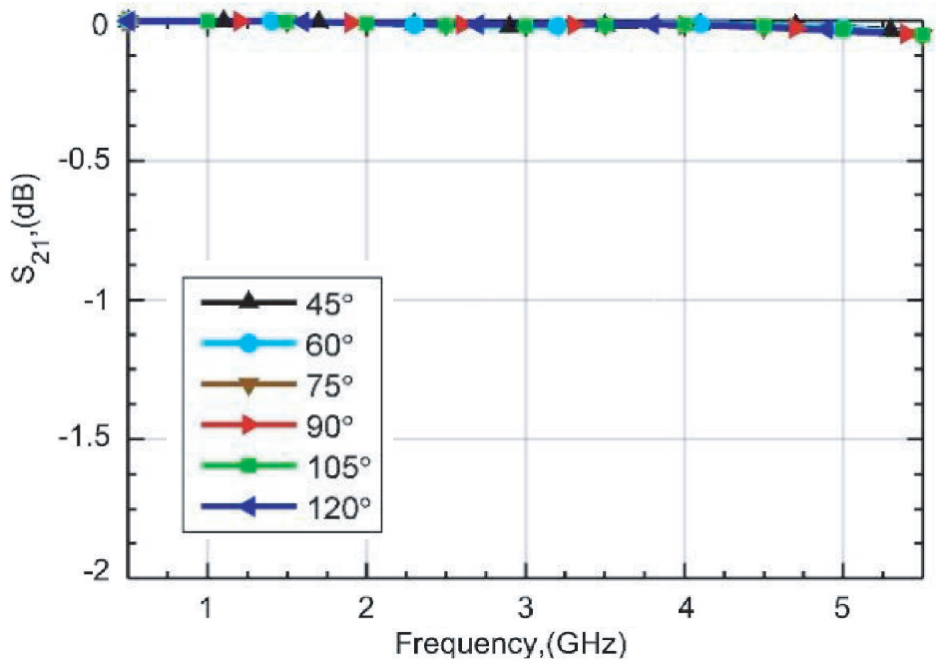


Figure 3.11: Simulated S_{21} of design cases listed in Table 3.4.

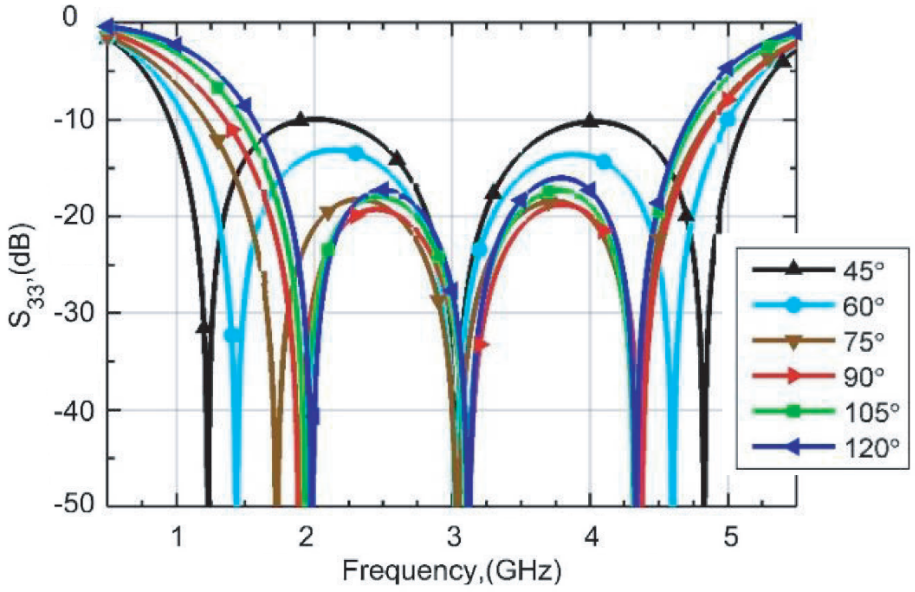


Figure 3.12: Simulated S_{33} of design cases listed in Table 3.4.

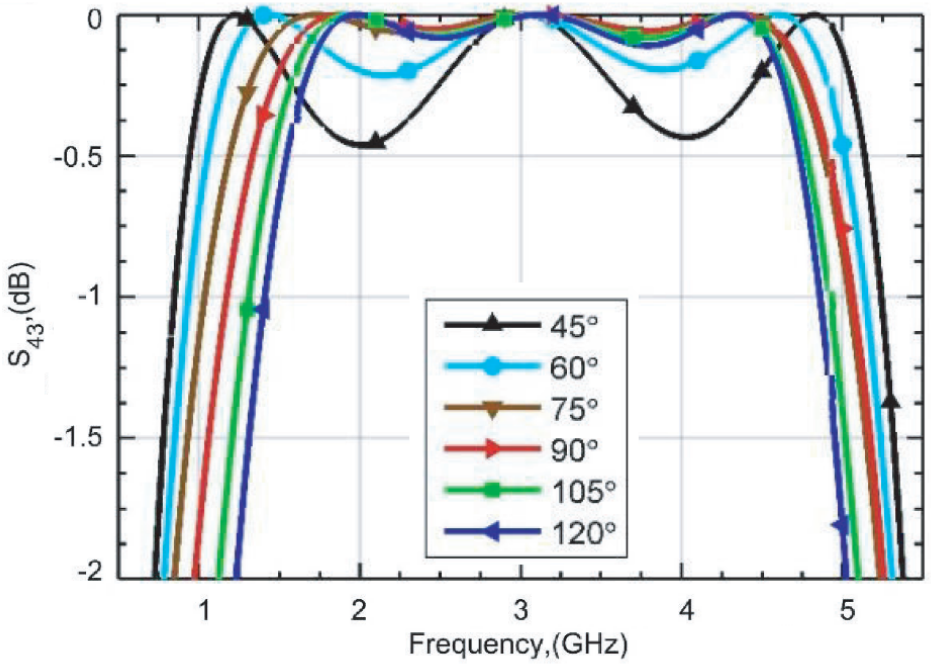


Figure 3.13: Simulated S_{43} of design cases listed in Table 3.4.

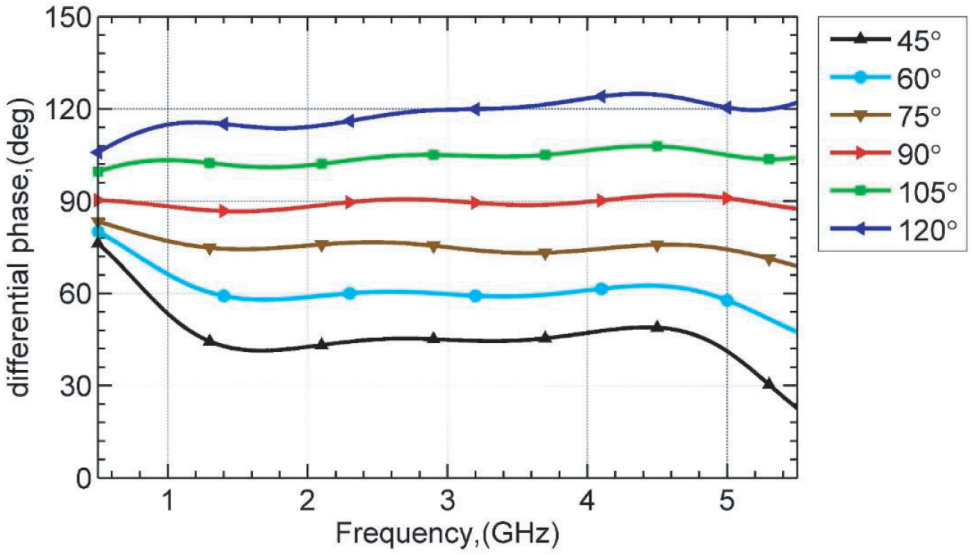


Figure 3.14: Simulated differential phase shift of design cases listed in Table 3.4.

mentioned phase shifts is clearly evident. The simulation results of return and insertion losses of these examples are depicted in Figs. 3.10, 3.11, 3.12, and 3.13, which reflects remarkable performance of the proposed phase shifter. It is to be noted that these near ideal results are obtained due to the application of ideal transmission line elements during the simulations.

3.5.3 Design Prototype and Measurement Results

The momentum electromagnetic (EM) simulation engine of the Keysight ADS is used to verify and optimize the formulated design. The substrate used is the Rogers RT/Duroid 5880 with $\varepsilon_r = 2.2$, loss tangent 0.0009 and substrate thickness of 1.575 mm and 35 μm copper on both sides. To validate the proposed idea, a 90° phase shifter at 3 GHz is designed, simulated, fabricated and measured. The ideal design parameters are given in Table 3.4. Since there are multiple bends and junctions emanating during the layout of the phase shifter, the final design is obtained after optimization to compensate for their effects. Since reducing the coupled lines gap normally improves the bandwidth performance, the initial gap of 0.33 mm was optimized to a final value of 0.25 mm due to the availability of a good fabrication facility. Fig. 3.15 and Fig. 3.16 shows the implemented prototype and measurement setup along with the dimensions marked in mm, respectively. The measurement of the prototype is carried out using an E5063A

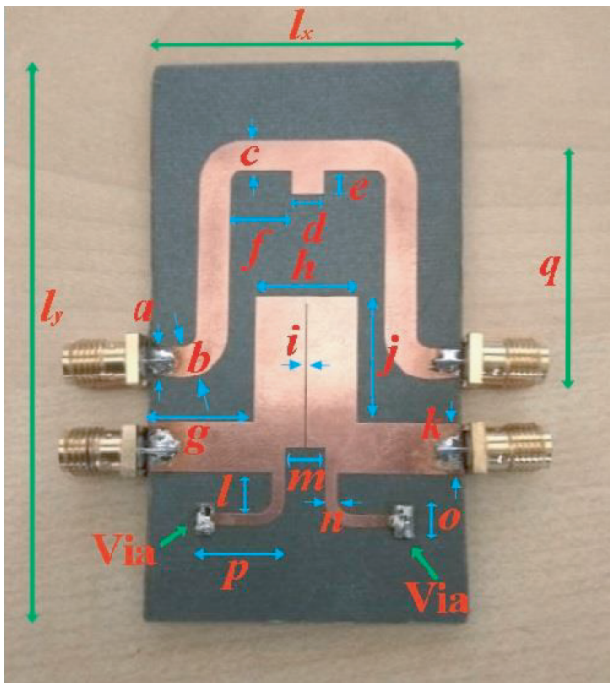


Figure 3.15: The prototype. The proposed prototype has the following dimensions (in mm): a = 3.55, b = 4.19, c = 3.94, d = 3.94, e = 3.05, f = 8.01, g = 13.2, h = 12.7, i = 0.255, j = 16.25, k = 6.35, l = 5.08, m = 5.08, n = 1.53, o = 4.06, p = 11.17, q = 31.11, lx = 39.75, and ly = 86.21.

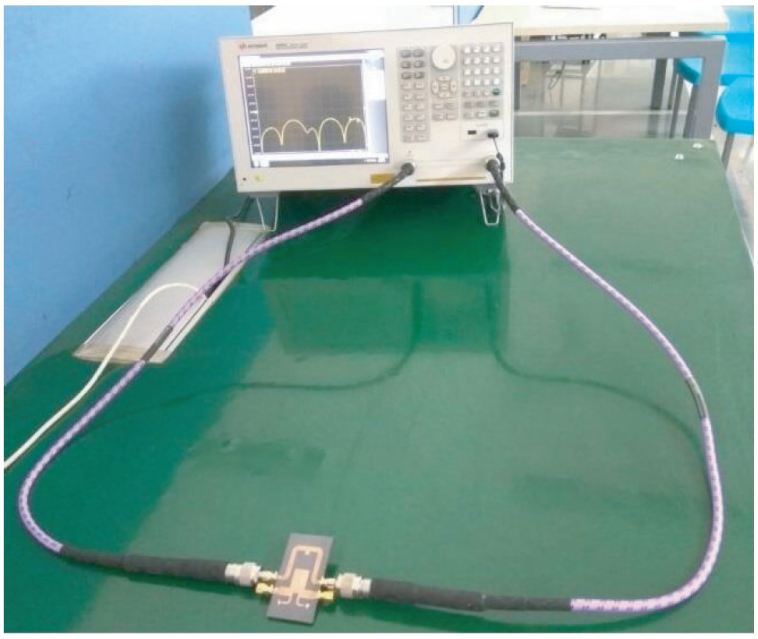


Figure 3.16: The measurement setup. An E5063A vector network analyzer from Keysight Technologies is used for the measurement.

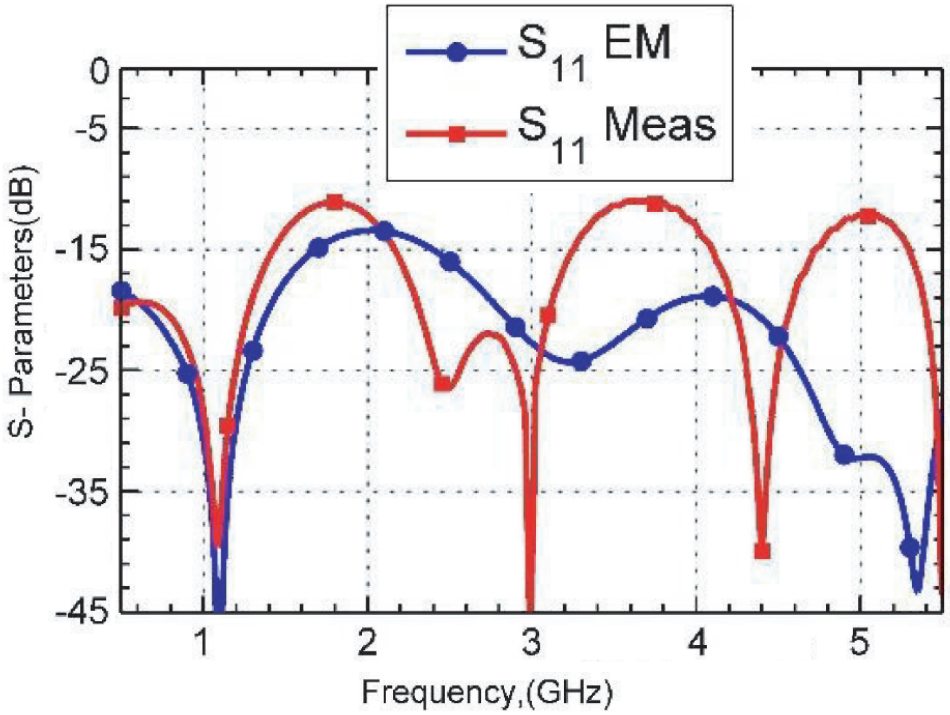


Figure 3.17: EM simulation vs Measured S_{11} of the fabricated prototype.

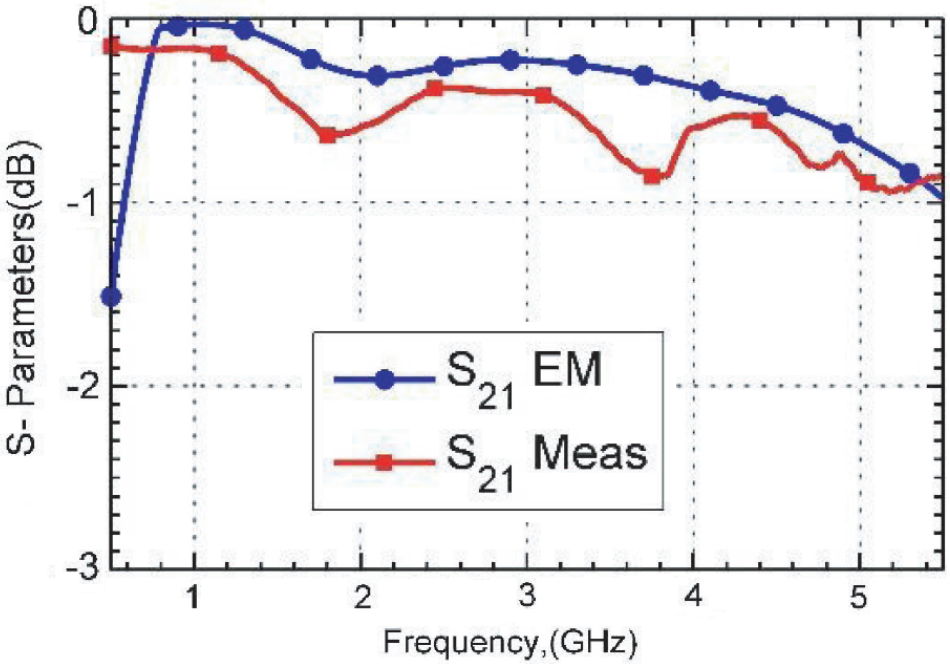


Figure 3.18: EM simulation vs Measured S_{21} of the fabricated prototype.

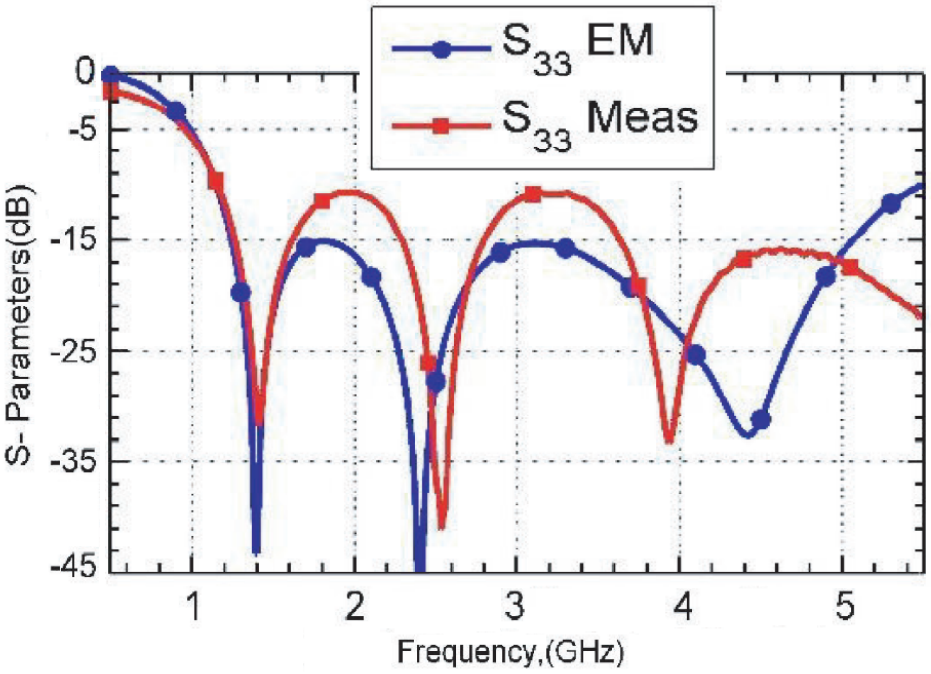


Figure 3.19: EM simulation vs Measured S_{33} of the fabricated prototype.

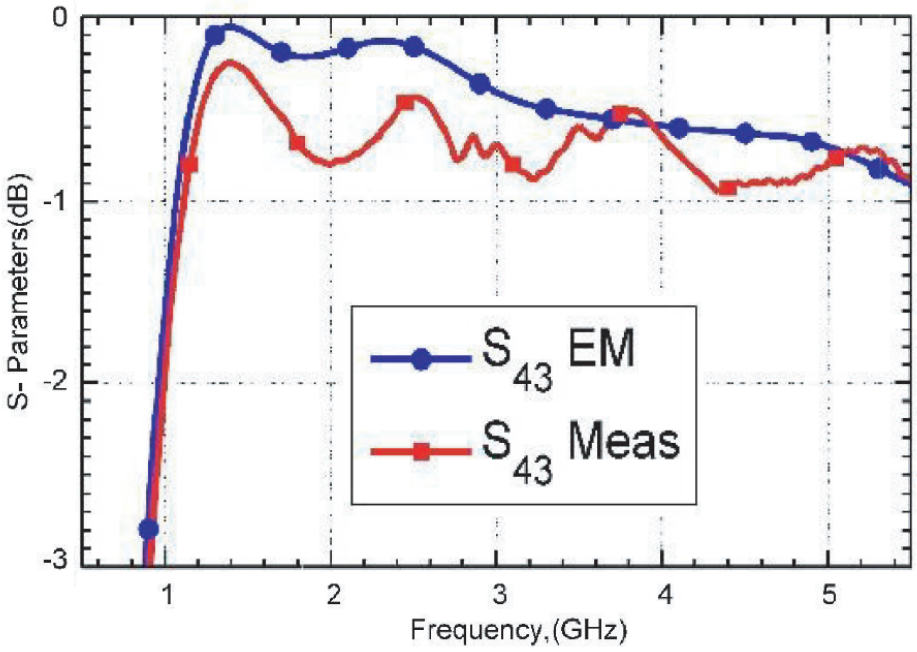


Figure 3.20: EM simulation vs Measured S_{43} of the fabricated prototype.

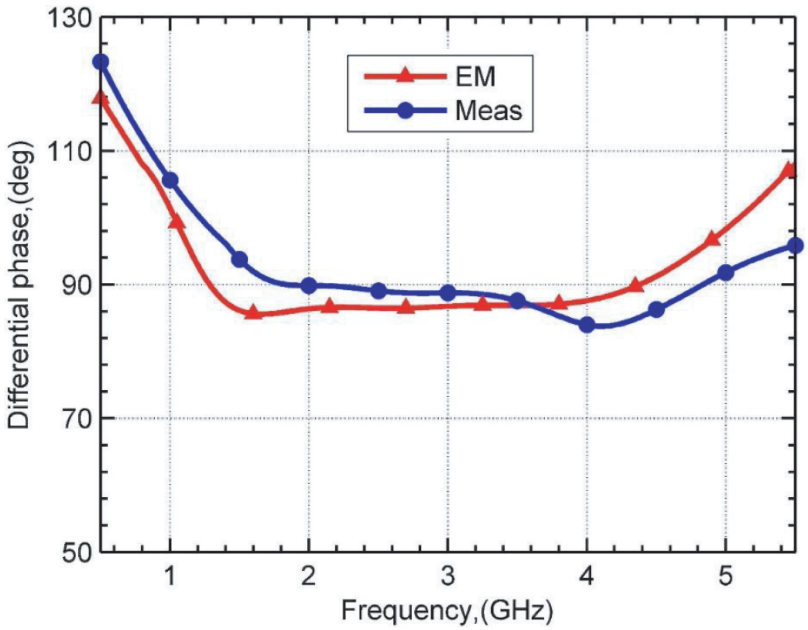


Figure 3.21: EM simulation vs Measured differential phase shift of the fabricated prototype.

vector network analyzer (VNA) from the Keysight Technologies. Please note that the similar setup is followed for all the measurements in this thesis.

The comparison of EM simulated and the measured S-parameters are depicted in Figs. 3.17, 3.18, 3.19, and 3.20. The EM simulated and the measured differential phase are also shown in Fig. 3.21. It is apparent that there is a good agreement between the EM simulated and the measured results. It is apparent from Figs. 3.17, 3.18, 3.19, and 3.20 that both the networks have better that 10 dB return losses and better than 1 dB insertion losses over a wide frequency span. Specifically, if we consider a phase error up to $\pm 7^{\circ}$ in Fig. 3.21, a return loss better than 10 dB, and an insertion loss less than 1 dB as the performance indicators, the minimum fractional bandwidth (FBW) is for S_{33}, which is around 142% at the centre frequency of 3 GHz. An anomaly between the EM simulated and measured results can potentially be due to the higher losses associated with the real substrate as well as fabrication and measurement tolerances. In addition, junction discontinuities also contribute to the parasitics, which might not have been exactly represented during the EM simulation. Nevertheless, the measurement results clearly show the outstanding performance of the fabricated prototype.

Table 3.5: Comparison with previous reported Phase Shifters.

Reference	Frequency (GHz)	Diff. Phase (°)	Phase Deviation (°)	Insertion Loss (dB)	Return Loss (dB)	FBW (%)	Layers
[143]	1.5 - 3.1	90	5	0.5	12	70	2
[144]	3.1 - 10.6	45	3	1	10	109	3
[145]	3.1 - 10.6	180	7	1.4	10	109	3
[146]	2.3 - 5.5	90	6.4	0.6	10	82	1
[147]	3.1 - 10.6	45	4.5	0.3	13.4	109	1
[148]	3.1 - 10.6	90	9.02	0.96	10	109	1
[149]	2.2 - 9.8	90	6	1.8	10	126.7	3
[150]	3 - 11	90	3	0.4	15	114	2
[151]	2.24 - 3.55	135	5	0.9	10	45	1
[152]	2.6 - 4.6	135	7.8	0.7	10	55.6	1
[153]	3.1 - 11	90	3	0.4	15	114	2
[This Work]	1.18 - 5.44	90	7	0.97	10.4	142	1

3.5.4 Comparison Report

A comparison between the proposed design and some of the previously reported phase shifters is made in Table 3.5. It is apparent that the proposed design is a single layer implementation (i.e., a design is only on the top side of microstrip) and provides an excellent FBW of 142%.

3.6 Conclusion

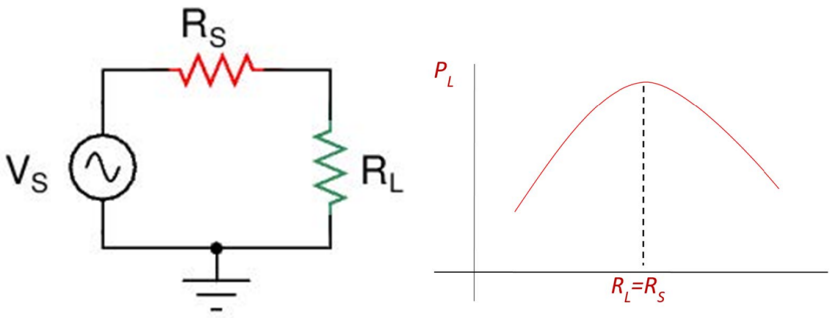
The basic characteristics of the microstrip transmission lines have been revisited in this chapter. The transmission lines are utilized to design the microstrip phase shifters as an example. Though the design, analysis, and investigations of the phase shifters have been provided in ideal or lossless TL in detail, the phase shifters have been validated through the microstrip prototype. It has been shown that the proposed developed designs exhibit good performance with limited phase ripples. The reported architectures are simple structures with closed form analytical solutions for the achieved performance of the phase shifters. The variable phase shifting over the wide range has also been obtained.

Chapter 4

Concept of Impedance Transformation and Its Applications

4.1 Impedance Transformer

Impedance transformation or matching is a paramount requirement for the maximum power transfer in all the circuit and system applications. As per the maximum power transfer theorem, the load resistance (R_L) in Fig. 4.1 should follow $R_L = R_S^*$ for the maximum power to be delivered to the load. Here, symbol "*" denotes complex conjugate function. The plot in Fig. 4.1(b) depicts the variation of the delivered load power with the variation of load resistance.



(a) (b)

Figure 4.1: (a) Voltage source connected to a load resistance and (b) Power delivered to the load versus the load resistance value.

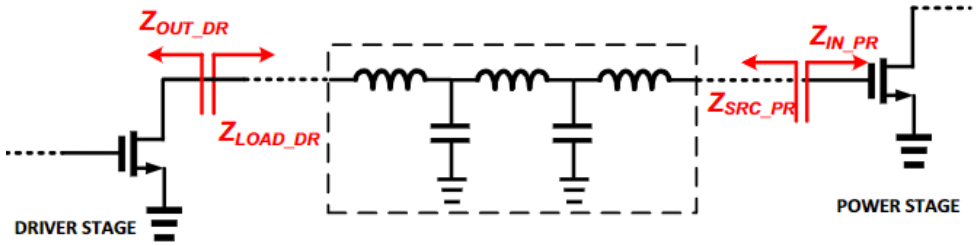


Figure 4.2: Example of complex to complex inter-stage matching methodology [6]

An individual component used for the impedance transformation is known as "impedance transformer" or an "impedance matching network". An RF impedance transformer is used to mitigate the reflections between two RF components by providing the impedance matching. Impedance transformers are the most ubiquitous block of any RF/Microwave communication system and are present ***almost everywhere*** in the WCS. The impedance transformers offer various ports matching for the WCS circuits and components for various source/load conditions. In general, the impedance transformation can be broadly classified into three different aspects i.e.

- **Real to Real Impedance Transformer** for example in power dividers [83],
- **Real to Complex Impedance Transformer** for example in amplifiers [156], and
- **Complex to Complex Impedance Transformer** for example in multi-stage amplifiers and RF circuit systems [157]. An example of a dual-stage power amplifier is depicted in Fig. 4.2 [6].

4.2 A Dual-Frequency Impedance Transformer

The proposed dual-band impedance transformer is depicted in Fig. 4.3. It utilizes a coupled line with the open-/short-circuited stubs. These stubs are utilized in such a way that they enhance the design flexibility. This statement is elaborated and clarified in the provided design analysis. The reported architecture is distributed in two sections, i.e., Section 1 and Section 2, and are

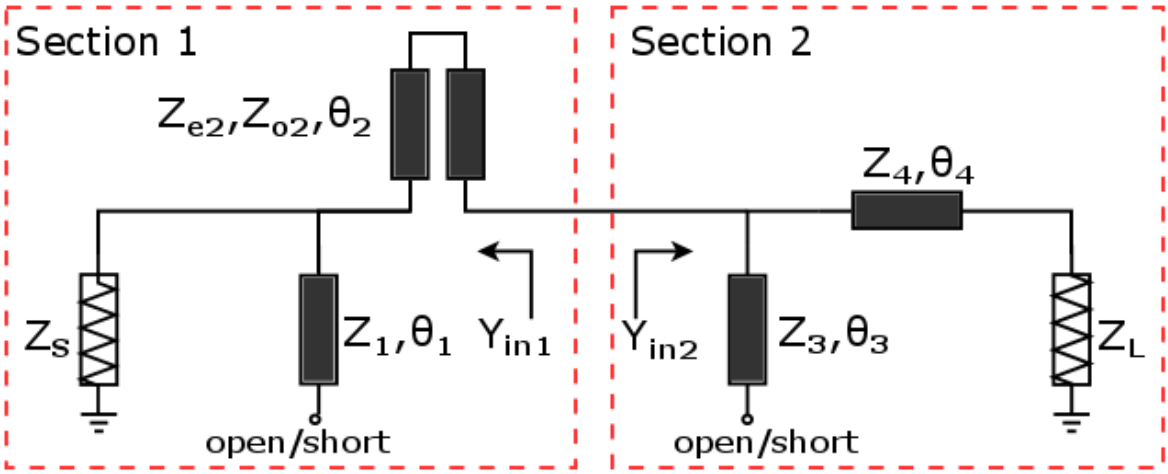


Figure 4.3: Schematic of the reported UHITR impedance transformer.

marked accordingly in Fig. 4.3. The respective characteristic impedance and electrical length of the transmission lines and coupled lines are mentioned, respectively. The term Y_{in1} and Y_{in2} are the respective admittances looking towards the marked directions.

4.2.1 Mathematical Design Analysis of the Reported Impedance Transformer

4.2.1.1 Derivation of Y_{in1} for "Section 1"

The reported impedance transformer is analyzed using transmission parameters (T-parameters). For section-1, the respective transmission parameters of the ideal transmission lines and the admittance Y_{in1} can be expressed as (4.1) and (4.2), respectively. The open and short conditions are expressed separately in (4.1).

$$\begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix}_{Z_{1,open}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{j}{Z_1} tan\theta_1 & 1 \end{bmatrix}$$
$$\begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix}_{Z_{1,short}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{-j}{Z_1} cot\theta_1 & 1 \end{bmatrix} \tag{4.1}$$

$$Y_{in1} = \frac{Z_S C_1 + D_1}{Z_S A_1 + B_1} \tag{4.2}$$

$$here, \quad A = D = \frac{Z_{e2}cot\theta_2 - Z_{o2}tan\theta_2}{Z_{e2}cot\theta_2 + Z_{o2}tan\theta_2} \tag{4.3}$$

$$B = \frac{2jZ_{e2}Z_{o2}}{Z_{e2}cot\theta_2 + Z_{o2}tan\theta_2} \tag{4.4}$$

$$C = \frac{2j}{Z_{e2}cot\theta_2 + Z_{o2}tan\theta_2} \tag{4.5}$$

4.2.1.2 Derivation of Y_{in2} for "Section 2"

Similarly, expressions for section-2 are written in (4.6) and (4.7).

$$\begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix}_{Z_{3,open}} = \begin{bmatrix} 1 & 0 \\ \frac{j}{Z_3}tan\theta_3 & 1 \end{bmatrix} \begin{bmatrix} cos\theta_4 & jZ_4sin\theta_4 \\ \frac{j}{Z_4}sin\theta_4 & cos\theta_4 \end{bmatrix}$$
$$\begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix}_{Z_{3,short}} = \begin{bmatrix} 1 & 0 \\ -\frac{j}{Z_3}cot\theta_3 & 1 \end{bmatrix} \begin{bmatrix} cos\theta_4 & jZ_4sin\theta_4 \\ \frac{j}{Z_4}sin\theta_4 & cos\theta_4 \end{bmatrix} \tag{4.6}$$

$$Y_{in2} = \frac{Z_L C_2 + D_2}{Z_L A_2 + B_2} \tag{4.7}$$

4.2.1.3 Formulation of Z_3 and Z_4

Now, Y_{in1} and Y_{in2}, can be represented into its real and imaginary parts. It can be inferred from (4.3)-(4.5) that A and D are real, whereas, B and C are imaginary. Assuming K and L as (4.8) and (4.9) respectively, the real and imaginary parts of Y_{in1} and Y_{in2} are expressed in (4.10)-(4.17).

$$K = Z_s(A - jBcot\theta_1/Z_1) \tag{4.8}$$

$$L = Z_s(A + jBtan\theta_1/Z_1) \tag{4.9}$$

$$Re[Y_{in1,open}] = \frac{LD - Z_S(C + jDtan\theta_1/Z_1)B}{L^2 - B^2} \tag{4.10}$$

$$Im[Y_{in1,open}] = -\frac{Z_S L(jC - Dtan\theta_1/Z_1) - jBD}{L^2 - B^2} \tag{4.11}$$

$$Re[Y_{in2,open}] = \frac{Z_L + Z_L tan^2\theta_4}{Z_L^2 + Z_4^2 tan^2\theta_4} \tag{4.12}$$

$$Im[Y_{in2,open}] = \frac{tan\theta_3}{Z_3} + \frac{-Z_4 tan\theta_4 + Z_L^2 tan\theta_4/Z_4}{Z_L^2 + Z_4^2 tan^2\theta_4} \tag{4.13}$$

$$Re[Y_{in1,short}] = \frac{KD - Z_S(C - jDcot\theta_1/Z_1)B}{K^2 - B^2} \tag{4.14}$$

$$Im[Y_{in1,short}] = -\frac{Z_S K(C - jDcot\theta_1/Z_1) - BD}{K^2 - B^2} \tag{4.15}$$

$$Re[Y_{in2,short}] = \frac{Z_L tan^2\theta_3(1 + tan^2\theta_4)}{(Z_L tan\theta_3)^2 + (Z_4 tan\theta_3 tan\theta_4)^2} \tag{4.16}$$

$$Im[Y_{in2,short}] = \frac{(\frac{Z_L^2}{Z_4} - Z_4)tan\theta_4 - \frac{Z_L^2 - Z_4^2 tan^2\theta_4}{Z_3 tan\theta_3}}{Z_L^2 + (Z_4 tan\theta_4)^2} \tag{4.17}$$

Now if both the stubs are open-circuited, the following conditions should be satisfied for impedance matching of the source and load impedances.

$$Re[Y_{in1,open}] = Re[Y_{in2,open}] \tag{4.18}$$

$$Im[Y_{in1,open}] = -Im[Y_{in2,open}] \tag{4.19}$$

Solving (4.18) and (4.19), the design parameters Z_4 and Z_3 are derived as (4.20) and (4.24) respectively. Z_1, Z_{e2}, Z_{o2} are considered as independent variables here as can be chosen between [20-150] for the micro-strip line prototyping.

$$Z_4 = \frac{\sqrt{-Z_L Z_S(AD - BC)(Z_{4,num_1} + Z_{4,num_2})}}{ADZ_1 Z_S tan\theta_4 - BCZ_1 Z_S tan\theta_4} \tag{4.20}$$

where,

$$N = 1 + tan^2\theta_4 \tag{4.21}$$

$$Z_{4,num_1} = (B^2(Z_1^2 + Z_S^2 tan^2\theta_1) - A^2 Z_1^2 Z_S^2)N \tag{4.22}$$

$$Z_{4,num_2} = (AD - BC)Z_1^2 Z_L Z_S - 2jABZ_1 Z_S^2 tan\theta_1 N \tag{4.23}$$

$$Z_3 = -\frac{tan\theta_3 M}{\frac{Z_L^2 tan\theta_4}{Z_4} + \frac{jZ_{3,den}M}{Z_S^2(A + jBtan\theta_1/Z_1)^2 - B^2} - Z_4 tan\theta_4} \tag{4.24}$$

Table 4.1: Calculated values of design parameters of the reported ultra-high impedance transformer

case	r	k	Z_L	Z_1	θ_1 **(open/ short)**	Z_{e2}	Z_{o2}	θ_2	Z_3	θ_3 **(open/ short)**	Z_4	θ_4
1	2	10	500	100	$\pi/3$ (short)	120	60	$\pi/3$	33.6	$\pi/3$ (short)	106.9	$\pi/3$
2	2	50	1	60	$\pi/3$ (short)	150	90	$\pi/3$	66.57	$\pi/3$ (open)	19.3	$\pi/3$
3	4	5	10	30	$\pi/5$ (open)	100	60	$\pi/5$	21.64	$\pi/5$ (open)	63.6	$\pi/5$
4	7	4	200	150	$2\pi/8$ (short)	150	90	$\pi/8$	146.1	$\pi/8$ (open)	87.2	$\pi/8$

where,

$$Z_{3,den} = BD - (A + \frac{jBtan\theta_1}{Z_1})(C + \frac{jDtan\theta_1}{Z_1})Z_S^2 \tag{4.25}$$

$$M = Z_4^2 tan^2\theta_4 + Z_L^2 \tag{4.26}$$

Similarly, expressions for other open/short configurations of the two stubs can be derived. The electrical length for all the transmission lines and stubs should follow the condition (4.27) for dual-band operation (at f_1 & f_2) [2, 158]. Here, n is chosen 1 for the transmission lines for the miniaturized size, however, it is scaled to higher values for the open/short stubs only for the desired admittance. A simplified expression for all the θ w.r.t. frequency ratio ($r = f_2/f_1 \geq 1$) is mentioned in (4.28).

$$\theta(f_1) + \theta(f_2) = n\pi; \quad n \in [1,2,3,..,n] \tag{4.27}$$

$$\theta = \frac{n\pi}{1+r}; \qquad n \in [1,2,3,..,n] \tag{4.28}$$

4.2.2 Design Examples

Based on the analytical expressions, the design parameters of four different cases with very high impedance transforming ratio ($k = Z_L/Z_S$ or Z_S/Z_L to keep $k \geq 1$) and frequency ratio (r) are calculated. Here, Z_S is fixed to 50 Ω for all the cases. These design parameters are mentioned in Table 4.1 and are within the microstrip realizable range, which demonstrates the

Table 4.2: Comparison of Possible Impedance Transformation (k)

Ref	**r**	**k (range of Z_L in Ω)**
[2]	1<r<7	8<Z_L<450
[159]	1<r<7	10<Z_L<500
[60]	Case 1: 2<r<5 Case 2: 3<r<7	Case 1: 1<Z_L<56.25 Case 2: 1.5<Z_L<84.38
[This Work]	1<r<10	1<Z_L<500; Z_L >500 for lesser r

effectiveness of the reported design. To emphasize, case 1 in Table 4.1 explicitly specifies the design example with a very high impedance transformation ratio. Case 2 demonstrates the example for even higher k and with low impedance values. Case 3 and case 4 shows the ability of the reported design to achieve high k at higher r.

4.2.3 Fabrication and Measurement Results

Based on the available lab facilities, case 3 from the Table 4.1 is chosen for the prototyping of the reported design. The design is fabricated on Rogers RO4003C substrate with substrate thickness 1.52 mm, permittivity 3.38, and loss tangent 0.0021. The laminate has copper cladding of 35 μm on both sides of the substrate. The prototype is shown in Fig. 4.4. The measurement is done on Keysight E5063A VNA and the return loss results (S_{11} in dB) are plotted in Fig. 4.5. The measured results demonstrate a good return loss of over -20 dB with a slight deviation from the design frequencies. This possible cause of this deviation could be the transmission line discontinuities and the soldering errors. The fabricated prototype has a good 10 dB measurement (simulation) bandwidth of 0.30 GHz-0.41 GHz (0.344 GHz - 0.434 GHz) and 1.52 GHz - 1.62 GHz (1.56 GHz - 1.66 GHz). This demonstrates that the measurement results are in good agreement with the simulation results and thus validate the presented concept.

The ultra-high impedance transformation capability at high-frequency ratios of the prototype is also compared in Table 4.2 with the recently published reports on impedance transformers. The k of as high as 10 can be achieved using the reported prototype. The much interesting characteristic of this transformer to note is the value of load impedance, which can be transformed.

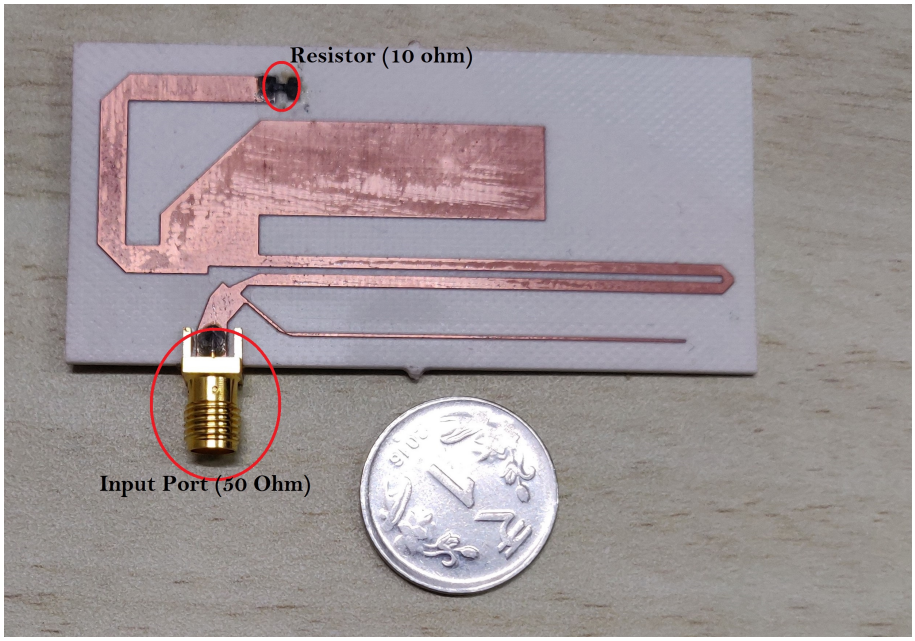


Figure 4.4: The fabricated prototype (R=10 Ω, Dimension: 70 mm x 28 mm).

4.3 Impedance Transformer with Improved Performance

The modified impedance transformer, shown in Fig. 4.6, consists of a simple architecture with one coupled-line and two open-/short-circuited stubs. The modified circuit is reduced by a TL now (the TL with characteristic (Z_4, θ_4) in Fig. 4.3 is eliminated from the circuit). These two stubs in Fig. 4.6 have the characteristic impedance and electrical length as Z_a (in Ω), θ_a (in °) and Z_b (in Ω), θ_b (in °) respectively. The coupled-line has even and odd mode impedances as Z_e (in Ω) and Z_o (in Ω), respectively and the electrical length is θ_c (in °). Terms Y_a, Y_b, and Y_c denote the respective admittances.

4.3.1 Design Theory and Expressions

The expressions for Y_a, and Y_c are deduced following the TL theory and are mentioned in (4.29) and (4.30), respectively [37]. The electrical lengths follow the expression (4.34) for the dual-band operation at two arbitrary frequencies where r is the frequency ratio [56].

$$\begin{aligned} Y_a &= \frac{1}{Z_L} + \frac{1}{\mathrm{j}Z_a \tan\theta_a} \quad \text{for short circuit} \\ Y_a &= \frac{1}{Z_L} + \frac{\mathrm{j}\tan\theta_a}{Z_a} \quad \text{for open circuit} \end{aligned} \tag{4.29}$$

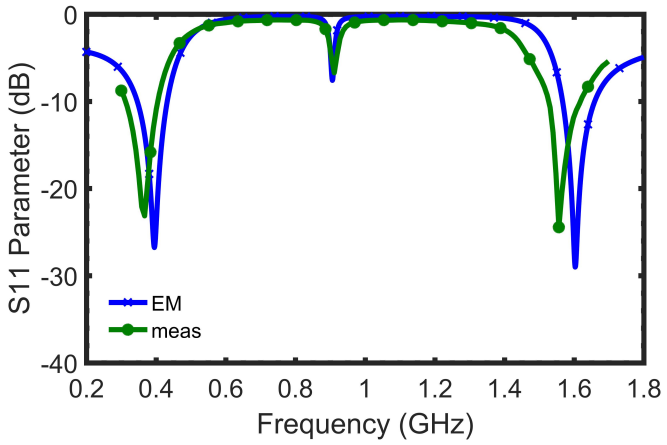


Figure 4.5: EM Simulation versus Measurement Results of the prototype.

$$Y_c = \frac{C + DY_a}{A + BY_a} \tag{4.30}$$

here,

$$A = D = \frac{Z_e \cot\theta_c - Z_o \tan\theta_c}{Z_e \cot\theta_c + Z_o \tan\theta_c} \tag{4.31}$$

$$B = \frac{2\mathrm{j} Z_e Z_o}{Z_e \cot\theta_c + Z_o \tan\theta_c} \tag{4.32}$$

$$C = \frac{2\mathrm{j}}{Z_e \cot\theta_c + Z_o \tan\theta_c} \tag{4.33}$$

$$\theta_i = \frac{(1+n)\pi}{1+r};\ n \in (0,1,2,..);\ i \in [a,b,c] \tag{4.34}$$

The real and imaginary parts of Y_c are equated with $1/Z_S$ and negative of Y_b respectively for the required impedance transformation. These two conditions are expressed in (4.35) and (4.36), and the solution of these provide the design parameters of the modified impedance transformer. To solve (4.35), any two variables from Z_e, Z_o, and Z_a can be considered to be independent as per the suitability and can be chosen in the range of [20 Ω - 150 Ω] for the realizable design parameters.

$$\mathrm{Re}[Y_c] = \frac{1}{Z_S} \tag{4.35}$$

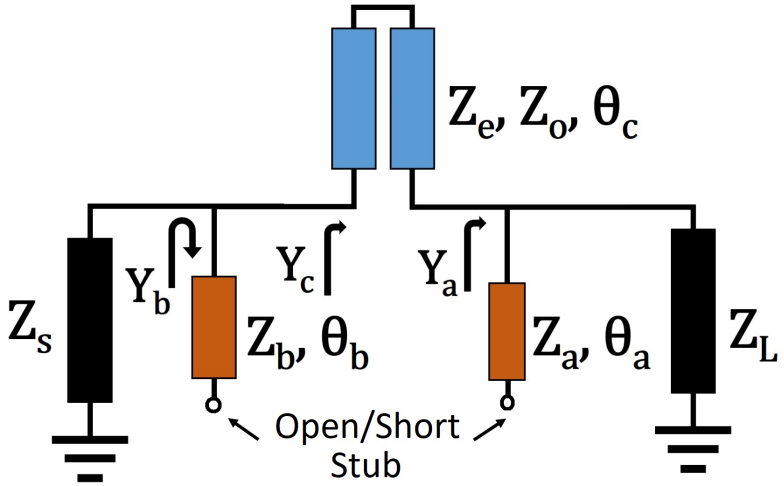


Figure 4.6: modified circuit for the dual-band impedance transformer.

$$\mathrm{Im}[Y_c] = -Y_b \tag{4.36}$$

where,

$$\begin{aligned} Y_b &= \frac{1}{\mathrm{j}Z_b \tan\theta_b} \quad \text{for short circuit} \\ Y_b &= \frac{\mathrm{j}\tan\theta_b}{Z_b} \quad \text{for open circuit} \end{aligned} \tag{4.37}$$

4.3.2 Design Flow Chart and Case Studies

4.3.2.1 Design Flow Chart

To enable quick prototyping of the modified impedance transformer, a design flow chart is provided in Fig. 4.7. The design flow chart is summarized below for a better understanding of the design procedure.

1. Compute r and k based on specified frequencies of operations and port terminations Z_L and Z_S.

2. Calculate electrical lengths θ_a and θ_c using (4.34). Initially, keep $n = 0$ for minimized architecture. Assume any combination of open/short-circuited stubs.

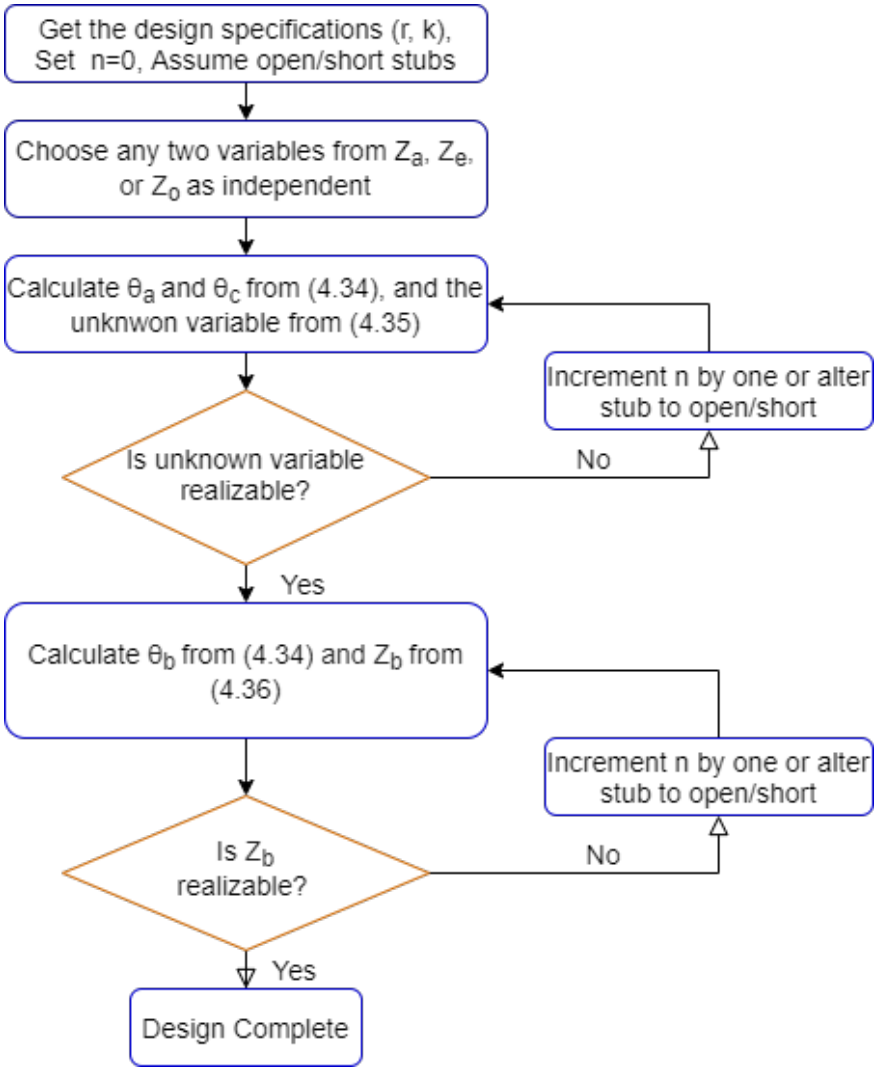


Figure 4.7: Flow chart for the quick prototyping of the modified IT.

3. Use (4.35) to find the unknown design parameter. Here, any two variables out of Z_a, Z_e, and Z_o can be chosen as independent variables. However, the selection of Z_e and Z_o may be opted with high coupling coefficient for the wider bandwidth [160].

4. In case the calculated parameter is not realizable, increment n in step 2. The selection of open- (or short-) circuited stub (Z_a, θ_a) can also be altered.

5. Further, calculate electrical length θ_b, keeping $n = 0$. Solve (4.36) to calculate Z_b.

6. In case Z_b is not realizable, increment n in step 5. Again, the selection of open- (or short-) circuited stub (Z_b, θ_b) can also be altered.

Table 4.3: Design Examples With Variation in r (k = 2, Z_S = 50 Ω is fixed for all cases) [Var*: Design parameters, S: short-circuited, O: open-circuited]

Var*	$r = 2$ **(case 1)**	$r = 4$ **(case 2)**	$r = 6$ **(case 3)**	$r = 8$ **(case 4)**	$r = 10$ **(case 5)**	$r = 15$ **(case 6)**	$r = 20$ **(case 7)**	$r = 30$ **(case 8)**
$Z_a(\Omega)$	65.8	105	65	46.9	35.3	23.6	133.8	40.4
$\theta_a(^\circ)$	60(S)	36(O)	25.7(O)	20(O)	16.4(O)	11.25(O)	77.1(S)	46.4(O)
$Z_e(\Omega)$	86	94	107	121	140	160	55.6	67
$Z_o(\Omega)$	56	67	84	95	109	140	37.3	54.2
$\theta_c(^\circ)$	60	36	25.7	20	16.4	11.25	34.3	5.8
$Z_b(\Omega)$	45.5	98	103	144	143.8	126.3	86.4	128.7
$\theta_b(^\circ)$	60(S)	36(O)	25.7(O)	20(O)	16.4(O)	11.25(O)	34.3(S)	11.6(S)

The modified design and the flow chart envisages the following important aspects: 1) the modified design has two stubs with the choices of being open- or short-circuited, 2) the design analysis demonstrates that there are two independent design variables, 3) the choice of selecting two independent design variables out of three Z_a, Z_e, and Z_o, and, 4) the independent selection choices of n for θ_a, θ_b, and θ_c in (4.34). Owing to the possibilities in computing the design parameters, the design procedure validates the enhanced design flexibility of the modified impedance transformer. It makes the modified design extremely suitable for a very wide range of design specifications in terms of r and k.

4.3.2.2 Case Studies: Impedance Transformer at Various Frequency Ratios

It has been explained in the last sub-section that the design procedure is very flexible. Now, a variety of case studies are discussed in order to show its effectiveness and design flexibility in practical scenarios. In essence, the modified impedance transformer is assessed and evaluated for a wide range of possible k for varied values of arbitrarily selected r.

At first, the impedance transformer is designed for the varying r for a fixed k of 2. This example enables evaluation of the design for the identification of possible extreme values of r for a fixed value of k. A number of design examples mimicking this situation are listed in Table 4.3 along with the corresponding design parameters. It is clear that all the design parameters are realizable for cases varying from $r = 2$ to $r = 30$. The circuit simulation results for all these design cases are plotted in Fig. 4.8. The results for the cases 7 and 8 are depicted only around the design frequencies for clarity purposes. It is now safe to comprehend from these results

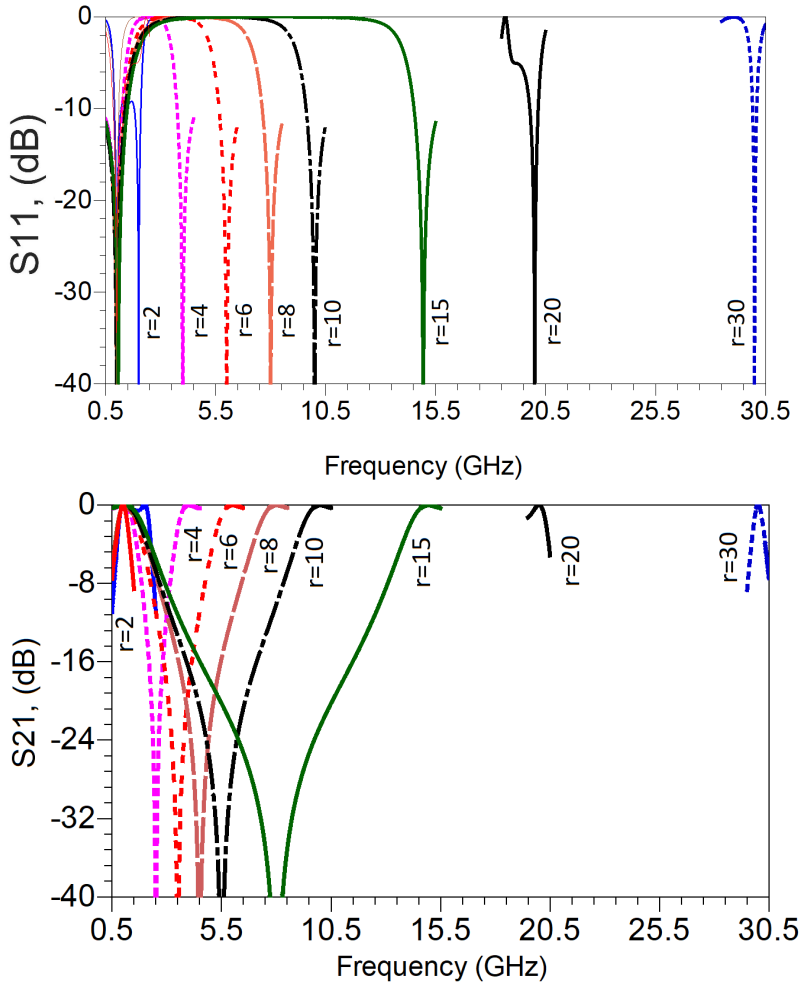


Figure 4.8: Simulation performance of the design examples of Table 4.3.

that the impedance transformer achieves excellent performance for the values of r up to 30. Furthermore, the modified impedance transformer is capable of achieving fractional bandwidth (FBW) in excess of 100% at the first frequency for all the cases except cases 7 and 8. The FBW for case 7 is 38%, however, it is reduced to only 19% for case 8 at the first frequency. Apparently, the enhanced design flexibility makes it possible to have the realizable design parameters at such high values of r. But it should be noted that there is a trade-off between the achievable r and the FBW as can be seen from the deteriorating FBW of only 2% at the second frequency, i.e. 20 GHz, in the design case 7. However, this constraint can be circumvented and r of more than 30 can also be achieved if the chosen design frequencies are at the lower RF spectrum (for example, 200 MHz and 6 GHz).

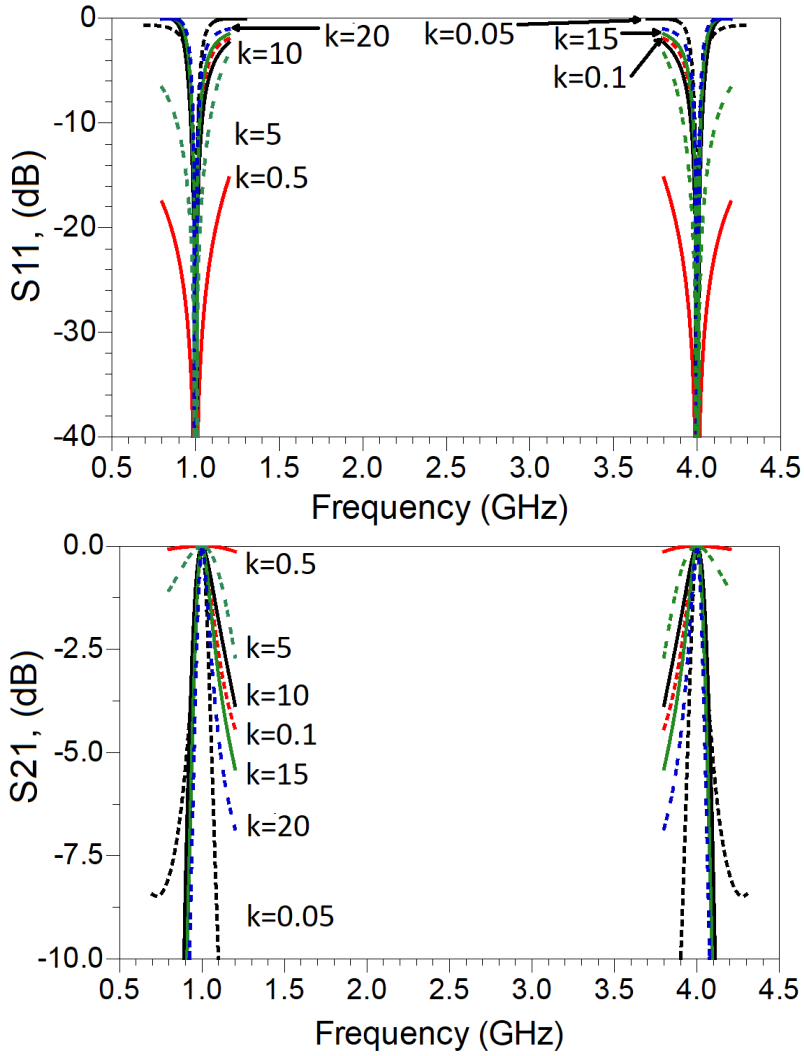


Figure 4.9: Simulation performance of the design examples of Table 4.4.

4.3.2.3 Case Studies: Impedance Transformer at Various Impedance Transformation Ratios

Now, the effectiveness and design flexibility of the modified impedance transformer is evaluated for varying k for a fixed r of 4. The r is fixed at 4 to assess the concurrent impedance transformation at two distinct frequencies. Multiple design examples are listed in Table 4.4 with the calculated design parameters. Again, all the design parameters are realizable for the cases varying from $k = 0.1$ to $k = 20$. The circuit simulation results of the design examples are also depicted in Fig. 4.9. These results demonstrate the excellent performance of the impedance transformer at all the k. It should be noted that the operational FBW, as per required reflection

Table 4.4: Design Examples With Variation in k ($r = 4$, f_1 = 1 GHz is fixed for all cases) [Var*: Design parameters, S: short-circuited, O: open-circuited]

Var*	$k = 0.05$ **(case 9)**	$k = 0.1$ **(case 10)**	$k = 0.5$ **(case 11)**	$r = 5$ **(case 12)**	$k = 10$ **(case 13)**	$k = 15$ **(case 14)**	$k = 20$ **(case 15)**
$Z_a(\Omega)$	154.9	84.9	120.5	94.2	93.7	98.7	97.2
$\theta_a(^\circ)$	144(O)	108(O)	36(O)	36(O)	108(S)	108(S)	108(S)
$Z_e(\Omega)$	20	27	52	120	156	150	141.5
$Z_o(\Omega)$	19	25.3	31	87	80	85	85.5
$\theta_c(^\circ)$	108	72	36	36	36	36	36
$Z_b(\Omega)$	46.1	62.6	68.9	38.3	62.5	46.3	36.6
$\theta_b(^\circ)$	72(O)	108(O)	36(O)	36(O)	216(S)	216(S)	216(S)

coefficient (Γ_m), of the modified impedance transformer reduces at the higher k following the conventional theory (4.38) [37]. Here, $\Delta f/f_o$ is the FBW and f_o is the first frequency of operation. Again, the enhanced design flexibility enables the impedance transformer to have the realizable design parameters at higher k but, for an FBW of 3%, impedance transformer is operable for k varying from as low as 0.1 to as high as 20. However, employing any bandwidth enhancement technique [161–163] will further enhance the range of achievable impedance transformation and frequency ratios. It is also practically evaluated that the different combinations of the open-/short-circuited stubs in the modified design have the potential to improve the bandwidth of the modified design.

$$\frac{\Delta f}{f_o} = 2 - \frac{4}{\pi}\cos^{-1}\left[\frac{\Gamma_m}{\sqrt{1-{\Gamma_m}^2}}\frac{2\sqrt{Z_S Z_L}}{|Z_L - Z_S|}\right] \tag{4.38}$$

4.3.2.4 Case Studies: Complex Impedance Transformation

Furthermore, the capability of the modified impedance transformer for the complex loads is also tested at the two operating frequencies simultaneously. The complex impedance transformation and the proposed architecture to handle such environments are discussed in detail later in this thesis. However, a glimpse of the complex impedance transformation is also demonstrated here through an example in Table 4.5. A design example working at a high r of 4 and a widely separated complex port impedance of 150+j20 Ω at the load is evaluated. The design example with design parameters is provided in case 16 of Table 4.5.

Table 4.5: Arbitrary Design Examples [*Calculated as the ratio of real parts of the port impedances, S: short-circuited, O: open-circuited]

Design Parameters	$r = 4; k = 5^*$ **(case 16)**	$r = 5; k = 8.04$ **(case 17)**	$r = 15, k = 20$ **(case 18)**
$Z_L(\Omega)$	150+j20	402	1000
$Z_S(\Omega)$	30	50	50
f_1(GHz)	1	0.8	0.3
f_2(GHz)	4	4.0	4.5
$Z_a(\Omega)$	149.8	106.1	89.8
$\theta_a(^\circ)$	288(S)	30(O)	22.5(O)
$Z_e, Z_o(\Omega)$	78, 45	126, 71	105, 70
$\theta_c(^\circ)$	36	30	33.75
$Z_b(\Omega)$	77.7	66.7	97.4
$\theta_b(^\circ)$	36(S)	120(O)	11.25(S)

The design cases 17 and 18 are also listed to demonstrate the design flexibility at concurrent very high design specifications, i.e., r, k = 5, 8.04 and r, k = 15, 20, respectively. So many design examples with arbitrarily high design specifications, as per authors' knowledge, are very rare in the reported literature. For example, a dual-band stepped impedance transformer [2] provides very high r and k, but working at higher k and r simultaneously brings inherent fabrication challenges in this design. Designing of this well-known stepped impedance transformer for the design specifications of r = 4, source impedance 50 Ω, and load impedance 500 Ω (i.e. k = 10) results in characteristic impedances of 119.6 Ω and 209.1 Ω for the TLs in this design. However, the calculated characteristic impedance of 209.1 Ω is practically not realizable in microstrip technology. On the other hand, for the modified impedance transformer at the same $k = 10$, the characteristic impedances are within the realizable range of the microstrip technology i.e. within [20 Ω, 150 Ω] for a very high r as can be seen in case 13 in Table 4.4. All the design parameters listed in Tables 4.3, 4.4, and 4.5 for the three cases are within the microstrip TL realizable limits.

4.3.3 Fabrication and Measurement

To validate the working of the modified impedance transformer, two different prototypes working at very high design specifications, i.e. cases 17 and 18, are fabricated. The first

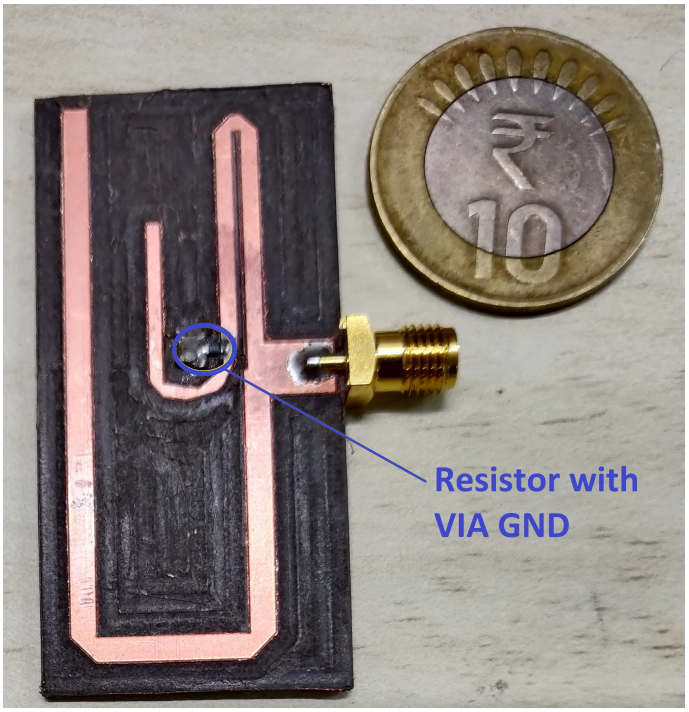


Figure 4.10: Fabricated prototype of the impedance transformer with $r = 5$ and $k = 8.04$.

prototype, i.e., case 17, working at 0.8 and 4.0 GHz (i.e., $r = 5$) is fabricated on Rogers RO5880 substrate with a substrate thickness of 1.57 mm, ε_r of 2.2, loss tangent of 0.0009, and copper cladding of 35 μm on both sides of the substrate. The source and load impedances of the impedance transformer are kept 50 Ω and 402 Ω (i.e., $k = 8.04$), respectively. The design parameters of the impedance transformer are calculated and provided in Table 4.5. The load of the impedance transformer is a 402 Ω resistor CRCW0603402RFKEA which is shorted to ground through a via on the printed circuited board (PCB) and a 50 Ω SMA connector is soldered at the source. The size of the fabricated prototype is 0.018 λ_g^2. The second prototype, i.e., case 18 for demonstration of extreme r and k, is specified to operate at 0.3 and 4.5 GHz (i.e., $r = 15$) and is fabricated on Rogers RO4350B substrate with a substrate thickness of 1.524 mm, ε_r of 3.66, loss tangent of 0.0037, and copper cladding of 35 μm on both sides of the substrate. The source and load impedances are chosen to be 50 Ω and 1000 Ω (i.e. $k = 20$), respectively. The design parameters of the impedance transformer are calculated and provided in Table 4.5. The load of the impedance transformer is a 1000 Ω resistor CRCW04021K00FKED shorted to ground through a via on the printed circuited board (PCB), whereas SMA connector mimics the 50 Ω source impedance. The size of the fabricated second prototype is 0.0026 λ_g^2.

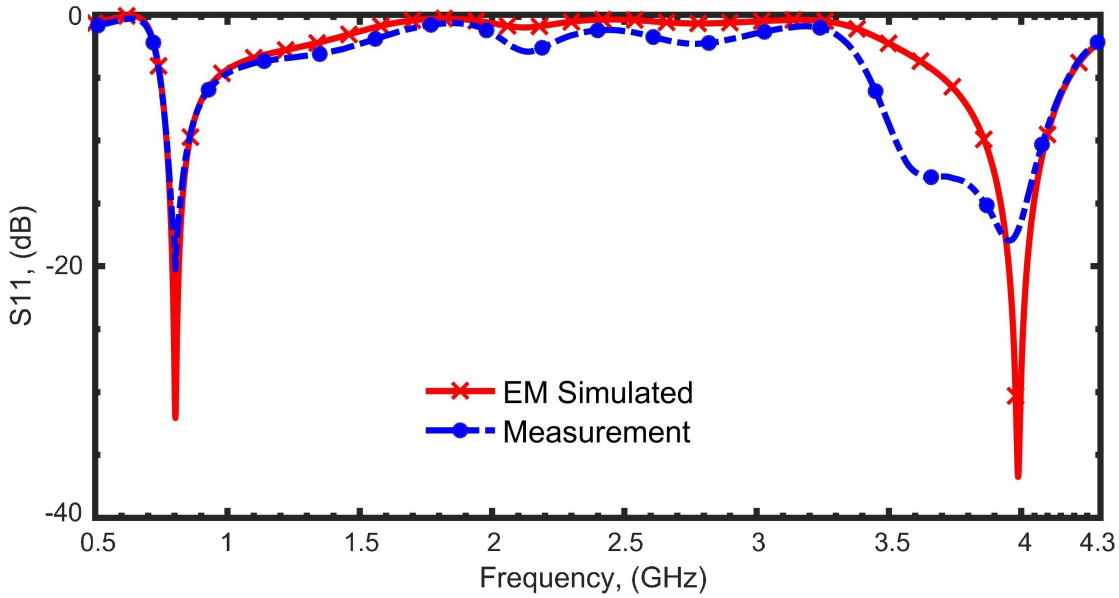


Figure 4.11: Measurement results of the fabricated prototype for $r = 5$ and $k = 8.04$.

These prototypes for cases 17 and 18 are depicted in Figs. 4.10 and 4.12, respectively. The corresponding measurement and EM simulated results are depicted in Figs. 4.11 and 4.13. An excellent agreement between the simulation and the measurement results validate the modified design along with the design process. Apparently, the measured return losses (S_{11}) of -20.5 dB at 0.8 GHz (-26.3 dB at 0.292 GHz) and -18.5 dB at 4.0 GHz (-23.5 dB at 4.468 GHz) for the first (second) prototype demonstrate good performances at the chosen frequencies for the respective designs. The unwanted resonance frequencies may be observed in Fig. 4.13 due to the multifold electrical lengths (i.e., n $\geq$ 1) and can be easily filtered by the existing frequency selective multiband systems. It is imperative to note that any design example in Tables 4.3, 4.4, and 4.5 or any other example conforming to extreme cases can be prototyped for validation of the presented concept, but here, the selected example for prototyping is regulated by the available lab resources. However, the modified circuit is discussed within the scope of microstrip technology and can achieve the highest operable frequencies with some precautions [164].

Table 4.6 compares the features of the modified impedance transformer with the recently reported highly featured architectures. Despite utilizing the planar TL, coupled-lines, and stubs combinations by most of the recently published reports [4, 59, 75–77], it is apparent that the

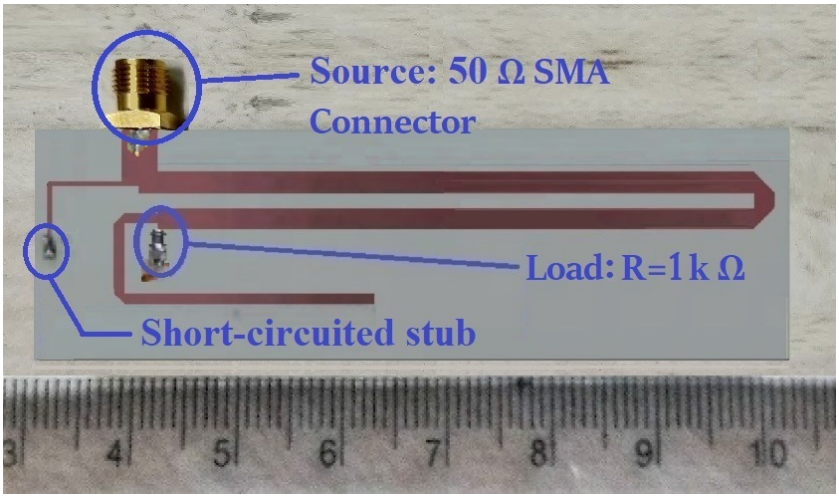


Figure 4.12: Fabricated prototype of the impedance transformer with $r = 15$ and $k = 20$.

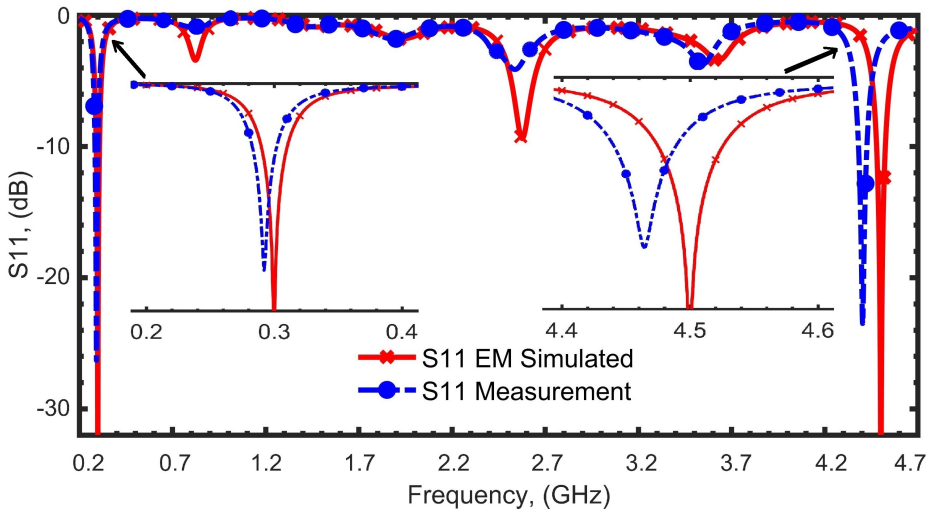


Figure 4.13: Measurement results of the fabricated prototype for $r = 15$ and $k = 20$.

Table 4.6: Comparison with State-of-the-art Impedance Transformers capable of High k and r [*Calculated as the ratio of real parts of the port impedances, **Calculated as the ratio of the maximum to minimum operating frequency]

References	**Technology**	**Max. r of examples**	**Max. k of examples**	**Specifications of the fabricated prototype (f_2 GHz/f_1 GHz, k)**
This Work	Coupled line with stubs	**20**	**20**	(**4.5/0.3, 20**), (4.0/0.8, 8.04)
[2]	Two Section Stepped TL	7	20	Not Provided
[59]	Coupled-lines	3.88	4	(2.4/0.9, 2)
[60]	Dual-Transmission Line	5.2	10	(2.8, 10), (5.2/1.0, 10)
[4]	Planar TL with stubs	1.5	5*	(3.6/2.4, 5*)
[75]	Planar TL with stubs	1.66	1.35*	(1.5/0.9, 1.35*)
[76]	Planar TL with stubs	1.94	4	(2.1/0.9, 2.02*)
[77]	Coupled-line with ladder network	1.5**	9.13*	(3.0/2.0**, 9.13*)
[57]	T-Type network with load healing	2.5	5*	(2.0/1.0, 1.86*)
[40]	Planar TL with a coupled-line	2.5	15.36*	(2.61/1.45, 15.36*)

modified design has extended the range of realizable design specifications significantly. Several modifications in the architectures are reported to achieve very high k [4, 57, 60] and very high r [59, 60]. However, achieving the concurrent high k and r have been rare in the reported literature. Though the load healing concept presented in [57] can enhance the range of k to some extent, but it was able to achieve only marginal improvement. The modified circuit not only enhances the k and r individually but also leads to significantly enhanced concurrent k and r are also made possible. A design example of concurrent r, k of 15, 20 is fabricated, depicted in Fig. 4.12 and the measurement results are demonstrated to validate the design flexibility of the modified impedance transformer. Moreover, all the design cases given in Tables 4.3, 4.4, and 4.5 demonstrate that the modified impedance transformer is capable of providing a) real and complex impedance transformations, b) very high k, c) very high r, and, d) very high k and r concurrently in comparison to the recently reported impedance transformers in Table 4.6. It is, therefore, safe to convey that the modified impedance transformer has the ability to achieve the highest k and r reported so far and thus enhances the existing state-of-the-art significantly.

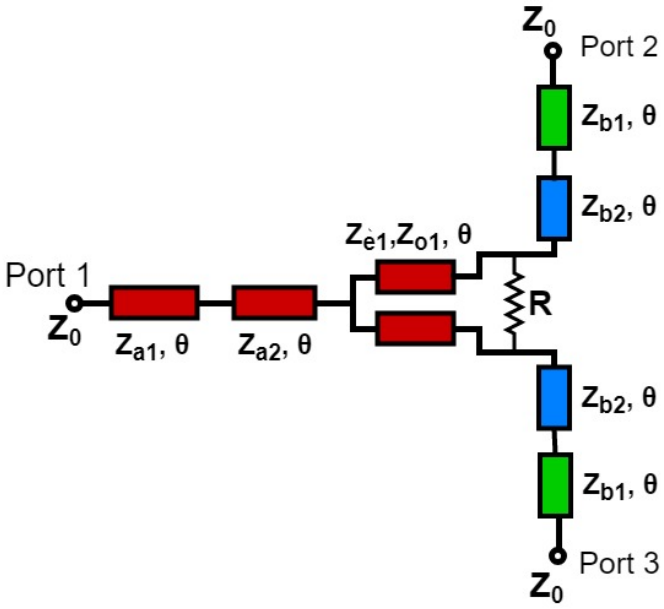


Figure 4.14: The proposed dual-band Power Divider

4.4 Application of Impedance Transformation

The modified impedance transformers demonstrate the high design flexibility and have high microstrip compatibility for the realizability in microstrip technology. These impedance transformers are omnipresent in a WCS and its applications are not limited to ports and interconnects only. Even the individual components of a WCS utilize the concept of impedance transformation. The same is illustrated in the design of a new power divider in the subsequent section of this chapter.

4.5 Impedance Transformation in Proposed Architecture of Power Divider

A coupled-line based dual-band Power Divider (PD) is depicted in Fig. 4.14. It consists of a coupled line, with odd- and even-mode impedances Z_{e1} and Z_{o1} respectively, and an isolation resistor, R, as the PD core. All the three ports are extended using two section transmission line (TSTL) [52]. The characteristic impedance (C.I.) of the left- (right-) side TSTLs are denoted

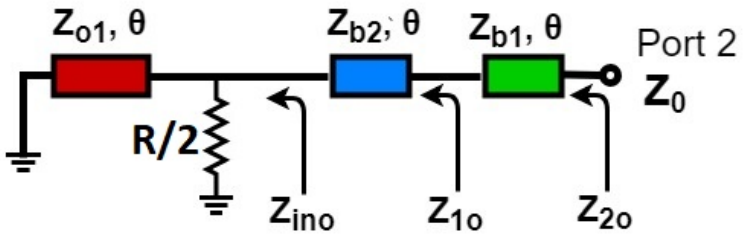


Figure 4.15: Odd-mode equivalent circuit of the proposed Power Divider

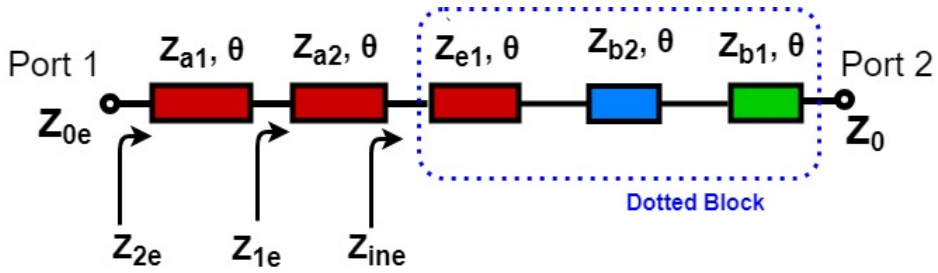


Figure 4.16: Even-mode equivalent circuit of the Power Divider

as Z_{a1} and Z_{a2} (Z_{b1} and Z_{b2}). All the electrical lengths (E.L.) are same and denoted as θ and are defined at the first frequency f_1.

4.5.1 Design Analysis

The even-odd mode analysis is employed to deduce the closed from design equations for all the design parameters. It is also demonstrated, subsequently, that the impedance matching is an requirement to provide the matching in the even- and odd-mode analysis.

Under the odd-mode analysis, the equivalent circuit of the PD core, in Fig. 4.15, is the combination of a resistor (R/2) shorted to ground and a short circuited stub with C.I. Z_{o1}. The equivalent impedance Z_{ino} of this combination can be written as:

$$Z_{ino} = R_{ino} + jX_{ino} \tag{4.39}$$

$$R_{ino} = \frac{(R/2)Z_{o1}^2\tan^2\theta}{(R/2)^2 + Z_{o1}^2\tan^2\theta} \tag{4.40}$$

$$X_{ino} = \frac{(R/2)^2 Z_{o1}\tan\theta}{(R/2)^2 + Z_{o1}^2\tan^2\theta} \tag{4.41}$$

The TSTL on the right-side, provides impedance matching to the load impedance (Z_0) of the PD. Here, impedance Z_{1o} and Z_{2o} can be expressed as (4.42) and (4.43), respectively.

$$Z_{1o} = Z_{b2}\frac{(R_{ino} + jX_{ino}) + jZ_{b2}\tan\theta}{Z_{b2} + j(R_{ino} + jX_{ino})\tan\theta} \tag{4.42}$$

$$Z_{2o} = Z_{b1}\frac{(Z_{1o}) + jZ_{b1}\tan\theta}{Z_{b1} + j(Z_{1o})\tan\theta} \tag{4.43}$$

It has been shown in [137] that ($Z_{1o}@f_1$) = (Z_{1o} @f_2)* and (Z_{2o} @ f_1) = ($Z2o$ @ f_2)* holds true if θ has the form given in (4.44).

$$\theta = n\pi/(1+r), r = f_2/f_1 \tag{4.44}$$

Invoking Z_{2o} = Z_0 in (4.43) to obtain the impedance matching, and then simplifying (4.42) and (4.43) gives (4.45) and (4.46) with a = tanθ [52].

$$Z_0a^2Z_{b2}^2 + [Z_0X_{ino}a + Z_{b1}(R_{ino} - Z_0)]Z_{b2} + [Z_{b1}Z_0X_{ino}a - Z_{b1}^2R_{ino}a^2] = 0 \tag{4.45}$$

$$Z_{b1}aZ_{b2}^2 + [Z_{b1}X_{ino} - R_{ino}Z_0a + Z_{b1}^2a]Z_{b2} - [Z_{b1}Z_0R_{ino}a + Z_{b1}^2X_{ino}a^2] = 0 \tag{4.46}$$

Elimination of Z_{b2} from (4.45) and (4.46) yields a 4th order equation in Z_{b1}:

$$AZ_{b1}^4 + BZ_{b1}^3 + CZ_{b1}^2 + DZ_{b1} + E = 0 \tag{4.47}$$

Where

$$A = \frac{R_{ino}^2a^4}{Z_0} - p_1(R_{ino} - Z_0)\frac{R_{ino}a}{Z_0} - R_{ino}p_1^2a^2 \tag{4.48}$$

$$B = p_1X_{ino}(R_{ino} - Z_0)(1+a^2) + p_1^2Z_0X_{ino}a - p_1X_{ino}R_{ino}a^2 - 2X_{ino}R_{ino}a^3(1+a^2) \tag{4.49}$$

$$C = Z_0X_{ino}^2a^2(1+a^2)^2 - 2Z_0R_{ino}^2a^4 + 2p_1Z_0R_{ino}^2a^3 + R_{ino}^2(R_{ino} - Z_0)a^2 + p_1Z_0X_{ino}^2a(1+a^2) + p_1R_{ino}Z_0(R_{ino} - Z_0)a \tag{4.50}$$

$$D = 2Z_0^2R_{ino}X_{ino}a^3(1+a^2) + R_{ino}^2X_{ino}a^3 - Z_0R_{ino}X_{ino}(R_{ino} - Z_0)a(1+a^2) - p_1Z_0^2R_{ino}X_{ino}a^2 \tag{4.51}$$

$$E = Z_0^3R_{ino}^2a^4 - Z_0^2R_{ino}X_{ino}^2a^2(1+a^2) - Z_0^2R_{ino}^2(R_{ino} - Z_0)a^2 - Z_0^2R_{ino}^3a^4 \tag{4.52}$$

$$p_1 = a + \frac{1}{a}(1 - \frac{R_{ino}}{Z_0}) \tag{4.53}$$

Now (4.47) can be solved for Z_{b1}, and subsequently, Z_{b2} can be obtained from (4.45) and (4.46) as:

$$Z_{b2} = \frac{Z_0 R_{ino} a Z_{b1} + X_{ino}(1+a^2)Z_{b1}^2 - \frac{R_{ino}a}{Z_0} Z_{b1}^3}{p_1 Z_{b1}^2 - Z_0 R_{ino} a} \tag{4.54}$$

Here Z_{e1}, Z_{o1}, and R are considered as independent variables. Once the design parameters in the odd-mode are computed, the even-mode equivalent circuit of the proposed PD, shown in Fig. 4.16, is analyzed afterward to compute the unknown parameters i.e. Z_{a1}, and Z_{a2}. Here, the port impedance Z_{0e} =2Z_0. And the impedance Z_{ine} is the effective impedance offered by the dotted block, i.e. computed/known parameters, in combination with the port impedance Z_0. As the term Z_{ine} is known and can be written in the form of $R_{ine} \pm jX_{ine}$, it resembles the effective circuit as in odd-mode analysis and, therefore, the design parameters can be computed similarly. Terms Z_{b1}, Z_{b2}, R_{ino}, and X_{ino} in (4.42) - (4.54) should be replaced with Z_{a1}, Z_{a2}, R_{ine}, and X_{ine}, respectively.

4.5.2 Simplified Design Procedure

This Section summarizes the design steps to be followed for a PD operating at two arbitrary frequencies:

- Choose a value of Z_{e1}, Z_{o1} and R in the realizable range of 20-150 Ω. These parameters are independent variable here while R is independent of the frequency ratio too.
- All the electrical lengths (θ) are calculated from (4.44) for a desired frequency-ratio (r). Here, value of n is chosen to be 1 for the miniaturized size.
- R_{ino} and X_{ino} are evaluated from (4.40) and (4.41) as the real and imaginary parts of Z_{ino}.
- Subsequently, Z_{b1} and Z_{b2} of the right-side TSTL are computed from (4.47)-(4.54). The negative values and the values out of range [20-150] of Z_{b1} and Z_{b2} should be omitted due to the TL realization in the micro-strip technology.

Table 4.7: Design Parameters at Different Frequency Ratios (All parameters in Ω if not marked)

Cases	**Frequency Separation (r)**	**Design Parameters**							
		Z_{e1}	Z_{o1}	R	Z_{a1}	Z_{a2}	Z_{b1}	Z_{b2}	θ
Case 1	1.1	120	70	150	94.5	128.3	72	87.1	85.71°
Case 2	2.0	145	100	150	96.6	69.5	70.8	62.1	60°
Case 3	4.7	127	96	100	51.7	20	66.5	26.7	31.58°

- Repeat Step 3-4 for the even-mode design parameters where R_{ino}, and X_{ino} (Z_{b1}, and Z_{b2}) should be replaced with R_{ine}, and X_{ine} (Z_{a1}, and Z_{a2}). The parameters Z_{a1} and Z_{a2} can easily be computed now.

4.5.3 Design Examples

Three design examples of the proposed dual-band PD based on the design procedure, are presented in this section. The port impedances are Z_0 = 50 Ω at all the three ports and the first design frequency is kept 1 GHz in all the cases. The second design frequency is varied from case to case basis to 1.1 GHz, 2 GHz, and 4.7 GHz to demonstrate the working and realizable design parameters at these various frequency ratios. The electrical lengths of all the transmission lines are 85.71°, 60°, and 31.58° for the dual-band operation of the design for three different cases respectively. All the C.I. and the E.L. for these design cases are listed in Table 4.7. The C.I. of the coupled line, Z_{e1} and Z_{o1}, and the isolation resistor R are chosen independently. The simulation results of the respective cases are demonstrated in Fig. 4.17.

4.5.4 Prototype and results

The design example of case 2, in Table 4.7, working at f_1 = 1 GHz and f_2 = 2 GHz is fabricated on Rogers RO4003C substrate with height 1.5 mm, copper cladding 35μm (both the sides) and permittivity (ε) = 3.55. The isolation resistor (R) of 150 Ω, 0603 size SMD package is used in the prototype. The fabricated prototype with its measurement setup are shown in Fig. 4.18.

The obtained measurement results are compared with the EM simulated results in Figs. 4.19, 4.20, and 4.21. It is imperative to note that the design is not optimized here for maximum matching at the design frequencies which is usually done to cater the junction discontinuities

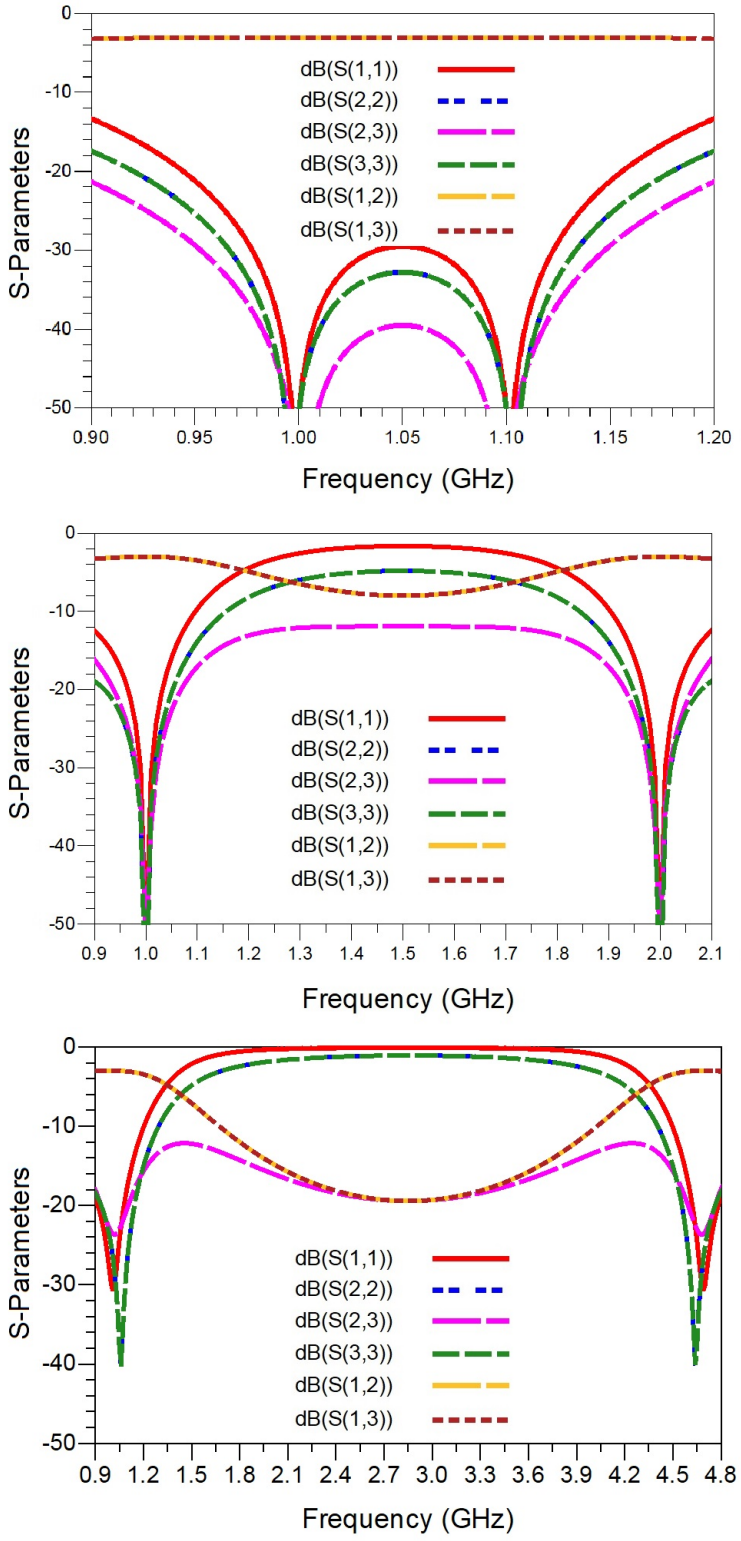


Figure 4.17: Simulation results for $r = 1.1$ (top), $r = 2.0$ (middle), and $r = 4.7$ (bottom)

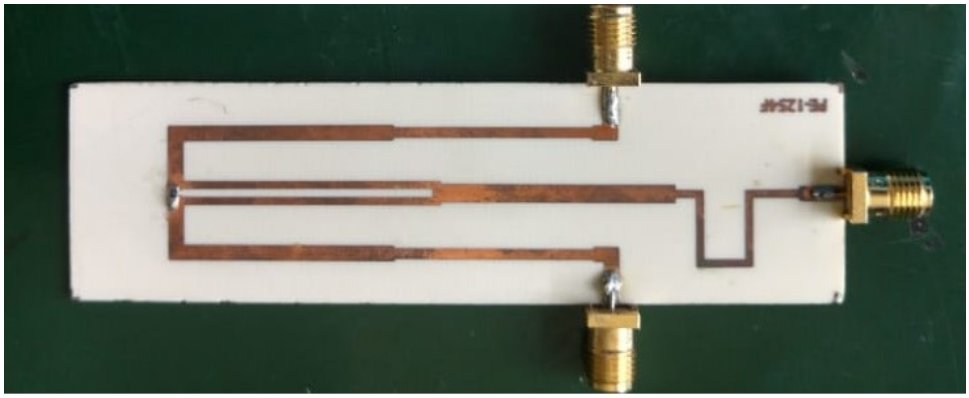


Figure 4.18: Fabricated prototype

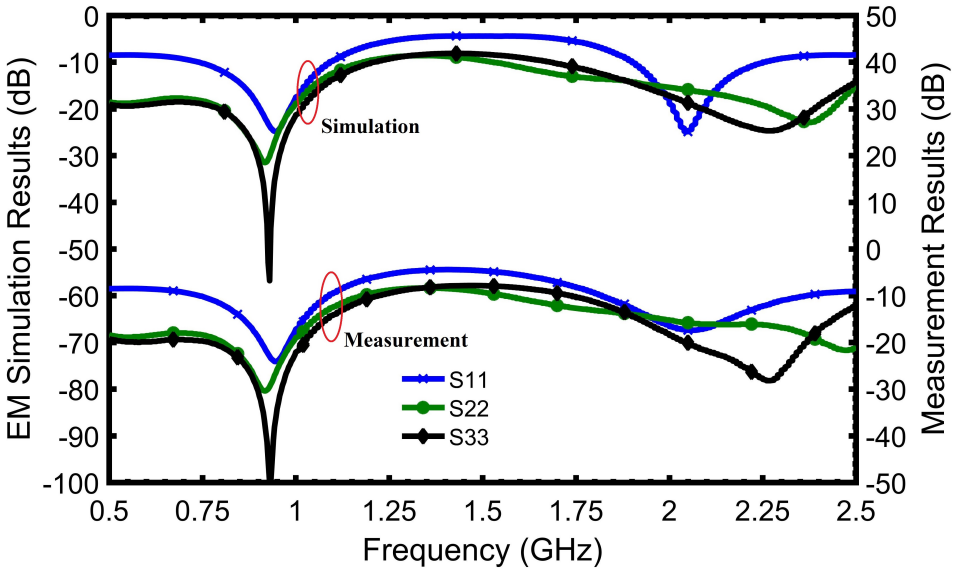


Figure 4.19: Measurement results for all ports matching

and resistor gap in the design. Instead, the optimizations is done for the wider bandwidths. The design is slightly optimized for the meandering and bends of the microstrip line and the resistor gap which is created due to the lumped resistor. The wider bandwidth at the second frequency can also be attributed to the associated dispersion, meandering, discontinuities, etc.

Apparently, the measurement results show a good return loss which is better than -17 dB at both the design frequencies (<-10 dB from 0.74 - 1.1 GHz @f_1 and 1.9 - 2.25 GHz @f_2). The isolation (S_{23}) between output ports is very good (>25 dB) at both the frequencies (<-10 dB for the whole bandwidth from 0.69 - 2.36 GHz). The output port matching S_{22} (S_{33}) are < -10 dB from 0.5 - 1.18 GHz @f_1 and 1.56 - 2.5 GHz @f_2 (0.5 - 1.23 GHz @f_1 and 1.73 - 2.5

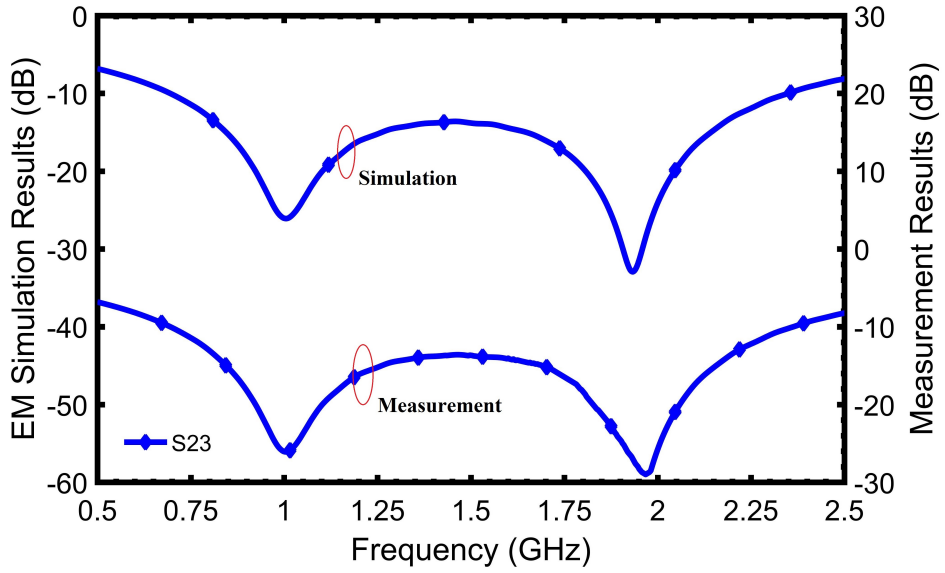


Figure 4.20: Measurement results for isolation

GHz @f_2). Moreover, the measured S_{21} and S_{31} are almost equal to -3.6 dB @f_1 /-3.7 dB @f_2. The corresponding EM simulated values of these parameters are -3.5 dB @f_1 /-3.7 dB @f_2. The measured phase difference between the output ports are $< 1.0^\circ$ @f_1 and $< 2^\circ$ @f_2. The amplitude imbalance is < 0.5 dB for a wide range of 0.5 - 2.5 GHz, and the phase imbalance is $<5^\circ$ from 0.5 - 2.45 GHz. Overall the fabricated prototype exhibits good agreement.

4.5.5 Comparison with the state of the art Power Dividers

A comparison with some recently reported dual-frequency PD is summarized in Table II. Compared to [106] and [103], the proposed PD has better band-ratio. The isolation resistor is not the continuous function of the band-ratio. As compared to [106, 109], the proposed design has independent isolation element, i.e., only one resistor, for the different band-ratios. Apparently, the design in [109] is better than the proposed PD from band-ratio view-point but, again, it needs a resistor, inductor, and capacitor which vary continuously with the band-ratio. The proposed design is advantageous considering the requirement of only one lumped element which is frequency independent isolation component too. Three design examples are discussed to support the proposed concept. The measurement results validate the design principle. There are a few independent design variables to support the flexible operation of the design.

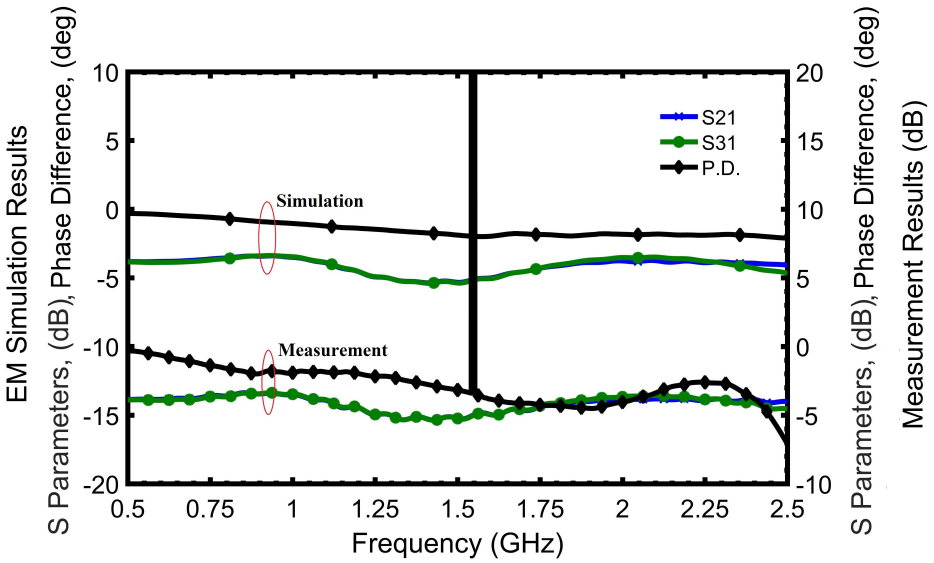


Figure 4.21: Measurement results for power division and phase difference

4.6 Conclusion

In this chapter, an impedance transformer has been proposed for the high impedance transformation. The impedance transformation is further improved by another impedance transformer. The architecture is a modification of the earlier proposed impedance transformer and is simplified by eliminating a TL. The proposed improved dual-band impedance transformer has been demonstrated to obtain an ultrahigh impedance transformation. The proposed architecture, with high design flexibility, has three main advantages: 1) the design is realizable for high k, 2) the design is realizable at a very high r, and 3) the design is realizable at very high k and r simultaneously. The presented design theory is supported by a number of design examples. Furthermore, a power divider is proposed for the dual-band operation as an example of the wireless communication system. The coupled-line based PD offers wide band-ratio capabilities. The analytical design analysis has been provided with the closed-form design equations for the quick prototyping. A few independent design variables are also present to support the flexible operation of the proposed design. The prototypes have also been fabricated to validate the design theory. The EM simulation results have been found in good agreement with the measurement results to validate the design performance.

Table 4.8: Comparison With State-Of-The-Art Techniques [Ph. D: Phase Difference, NA: Not Applicable]

Ref.	**Frequency** f_1/f_2 **GHz**	S_{11} **dB** f_1/f_2	S_{21}, S_{31} **dB** f_1/f_2	S_{23} **dB** f_1/f_2	**Ph.D** $^\circ$ f_1/f_2	**Isolation Element**	**Band Ratio**
[109]	0.5/2.0	-47/-26	-3.1/-3.3	-34/-40	NA	1 Resistor, 1 Capacitor, 1 Inductor	1-10
[106]	0.7/1.96	-40/-26	-3.1/-3.2	-30/-25	NA	1 Resistor, 1 Capacitor, 1 Inductor	1-3.5
[103]	0.9/3.5	-16/-31	-3.1/-3.2, -3.4/-3.6	-26/-24	0.4/1.2	1 Resistor	1.5-4.0
This Work	1.0/2.0	-19/-17	-3.78/-3.71	-26/-28	1.0/1.8	1 Resistor	1-4.7

Chapter 5

Multi-functional RF/Microwave Components

The proliferation of the growing wireless market has developed a profound interest in the design and development of the RF circuits and components to dramatically increase their functionality. In a WCS, multiple subsystems, for example, transmitters, receivers, and other associated components, supporting multiple RF circuits are connected altogether. These systems are supposed to be confined within a limited volume for the increased cost-effectiveness. To solve this problem, the development of multi-functional circuits and components is seems to be the potential solution. As the name suggests, a multi-functional RF component provides more than one feature in its operation in the communication system. Within the scope of this thesis, several features of an RF component can be listed as inherent impedance transformation, dual-band operation, DC isolation, balanced to unbalanced signal transformation, phase shifts, etc. The impedance transformation, dual-band operation, and phase shift operation are already explained in the previous chapters. "DC isolation" and "Balanced to Unbalanced signal transformation" functions are defined, subsequently, in this chapter. In this chapter, all the major objectives of the design and development of multi-functional components can be listed below:

- more features than the intended feature of a component.
- performance enhancement with high r.
- performance enhancement with high k.

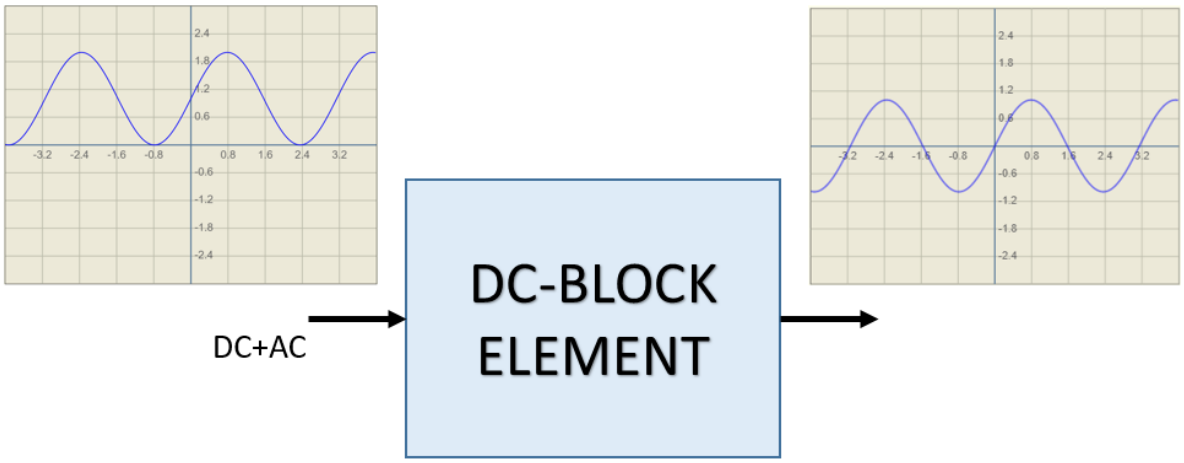


Figure 5.1: Functioning of a DC blocking element

- flexible and re-configurable design architectures.
- systematic design procedure to facilitate the quick prototyping.
- innovative design strategies to improve the design flexibility for high ranges of r and k.

5.1 DC Block or DC Isolation

The role of an ideal dc blocking element is to offer high series impedance to the frequency of 0 Hz and separate dc signals along a transmission line. An illustration of the functioning of DC blocking element is depicted in Fig. 5.1. A sinusoidal wave with some DC offset is present in the input. On passing through a DC blocking element, only the sinusoidal element is passed through while the DC component (DC offset) is blocked by the element.

5.2 Impedance Transformer with Inherent DC Blocking

A parallel coupled line can be utilized as an example of a dc-block element in the design of RF/Microwave components [47]. The reported impedance transformer, therefore, incorporates a coupled-line in its design along with other transmission line sections. A dual-band real to real impedance transformer, consisting of three sections to match the source impedance Z_S with the load impedance Z_L, is depicted in Fig. 5.2. Section 1 of the design is comprised of a

coupled-line having even- and odd-mode impedances of Z_e and Z_o, and electrical length θ_1. The section 2 is a two-section transmission line having equal electrical lengths θ_2, where (θ_2=θ_1), but distinct characteristic impedances Z_1 and Z_2, while the section 3 is a stub possessing characteristic impedance of Z_3 and electrical length, θ_3. Here, all the electrical lengths are defined at the first frequency i.e, f_1. The terms Y_{in1}, Y_{in2}, Y_{in3} in Fig. 5.2 are the respective admittance identified by the arrow directions. Analysis of each section that results into design equations is provided subsequently.

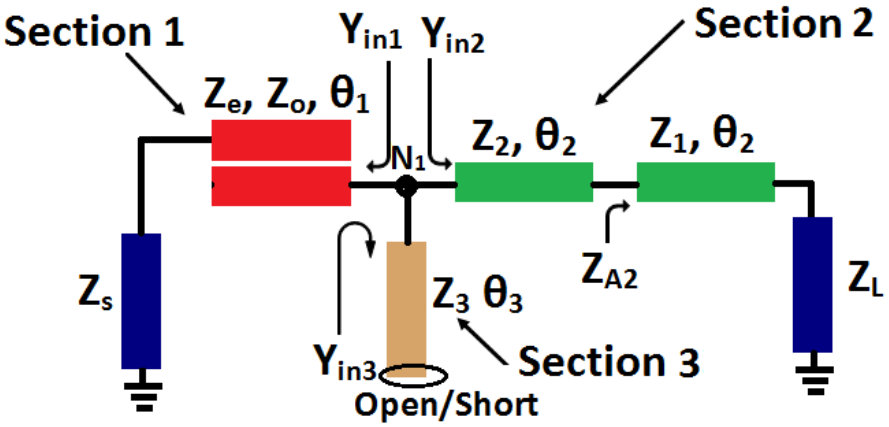


Figure 5.2: A Dual-band Impedance Transformer

5.2.1 Analytical Design Analysis

5.2.1.1 Design of Section 1

The admittance Y_{in1} is given by [48]:

$$Y_{in1} = G_{in1} + jB_{in1} \tag{5.1}$$

Where, G_{in1} and B_{in1} are expressed by (5.2) and (5.3), respectively. The term ρ (=Z_{e1}/Z_{o1}) is the coupling factor of a coupled-line i.e. ratio of the even and odd mode impedance of the coupled-line. Apparently, all the frequency dependent terms in (5.2) and (5.3) have squared magnitude i.e. always positive except the numerator of (5.3). Subsequently, a simplified expression for θ_1 can be deduced for the complex conjugate of B_{in1}.

$$G_{in1} = \frac{4(\rho-1)^2 Z_S sec^2\theta_1}{4(\rho+1)^2 Z_S^2 + 16\rho^2 Z_o^2 cot^2\theta_1 + (\rho-1)^4 Z_o^2 tan^2\theta_1 - 8\rho(\rho-1)^2 Z_o^2} \tag{5.2}$$

$$B_{in1} = \left(\frac{\rho+1}{Z_o}\right) \frac{tan\theta_1 \left[8Z_S^2 - 2(\rho-1)^2 Z_o^2 + 8\rho Z_o^2 cot^2\theta_1\right]}{4(\rho+1)^2 Z_S^2 + 16\rho^2 Z_o^2 cot^2\theta_1 + (\rho-1)^4 Z_o^2 tan^2\theta_1 - 8\rho(\rho-1)^2 Z_o^2} \tag{5.3}$$

$$\theta_1 = \frac{(n+1)}{(r+1)}\pi \tag{5.4}$$

Where, the term r is the frequency ratio f_2/f_1 and n is an integer. Furthermore, for dual-band operation, the value of θ_1 needs to satisfy $Y_{in1}|f_1 = \overset{*}{Y_{in1}}|f_2$ [165].

5.2.1.2 Design of Section 2

First, the term Z_{A2} can be defined as the input impedance of the transmission line having characteristic impedance Z_1 and electrical length θ_2, i.e. equals to θ_1.

$$Z_{A2} = Z_1 \frac{Z_L + jZ_1 tan\theta_1}{Z_1 + jZ_L tan\theta_1} \tag{5.5}$$

Then the admittance Y_{in2} can be given by:

$$Y_{in2} = 1/\left[Z_2 \frac{Z_{A2} + jZ_2 tan\theta_1}{Z_2 + jZ_{A2} tan\theta_1}\right] \tag{5.6}$$

Now, the expression in (5.6) can be simplified as $Y_{in2} = G_{in2} + jB_{in2}$, with the terms G_{in2} and B_{in2} expressed by (5.7) and (5.8) respectively. Once again, for dual-band operation, $Y_{in2}|f_1 = \overset{*}{Y_{in2}}|f_2$ with θ_1 following expression (5.4). Now, for the matching, $\mathrm{Re}(Y_{in1}) = Re(Y_{in2})$ at the node N_1 and this essentially means $G_{in1} = G_{in2}$. The simplifications lead to the expression (5.9) for the odd-mode impedance Z_o in terms of free variable ρ, the ratio of even-mode and odd-mode impedances, of the coupled-line.

$$G_{in2} = \frac{Z_L^2 (Z_1^2 (1 + tan^2\theta_1)^2}{Z_L^2 (Z_1 - Z_2 tan^2\theta_1)^2 + Z_1^2 (Z_1 + Z_2)^2 tan^2\theta_1} \tag{5.7}$$

$$B_{in2} = \frac{Z_1^2 (Z_1 - Z_2 tan^2\theta_1) - Z_1^2 (Z_2 - Z_1 tan^2\theta_1}{Z_1^2 (Z_1 - Z_2 tan^2\theta_1)^2 + Z_1^2 (Z_1 + Z_2)^2 tan^2\theta_1} (1 + \frac{Z_1}{Z_2}) tan\theta_1 \tag{5.8}$$

$$Z_o = \sqrt{\frac{4Z_S[(\rho+1)^2-4\rho+(\rho-1)^2 tan^2\theta_1][Z_L^2(Z_1-Z_2 tan^2\theta_1)^2+Z_1^2(Z_1+Z_2)^2 tan^2\theta_1] - 4Z_S^2 Z_L Z_1^2(\rho+1)^2(1+tan^2\theta_1)^2}{[Z_L Z_1^2(1+tan^2\theta_1)^2]\left[(\rho-1)^4 tan^2\theta_1+16\left(\frac{\rho^2}{tan^2\theta_1}\right)-8\rho(\rho-1)^2\right]}} \tag{5.9}$$

5.2.1.3 Design of Section 3

This section cancels the net imaginary part during the matching, i.e, $Y_{in1} = Y_{in2}$, at node N_1. At this node, $jIm(Y_{in1}+Y_{in2}) = j(B_{in1}+B_{in2})$ @ f_1 and $jIm(Y_{in1}+Y_{in2}) = -j(B_{in1}+B_{in2})$ @ f_2. This cancellation can be achieved using a dual-band short or open-stub at this node [165]. The expressions (5.10) and (5.11) can be simplified to determine the values of Z_3 and θ_3 for dual-band operations.

$$\theta_3 = \frac{(n+1)}{(r+1)}\pi, n \in I \tag{5.10}$$

$$Z_3 = -tan\theta_3/(B_{in1}+B_{in2}) \tag{5.11}$$

5.2.2 Design Procedure

For a given load and source impedances of Z_L and Z_S, the design starts with section 1. The odd-mode characteristic impedance Z_o of the coupled-line is determined using (5.9). During this stage, ρ, Z_1, and Z_2 are considered free variables whereas θ_1 is dependent on the frequency ratio r and is calculated using (5.4). For example, the values of Z_o for ρ = 3 and $r = 3$ are depicted in Figs. 5.3 and 5.4. The results in Fig. 5.3 provide the values of Z_o for Z_L varying from 10 to 40 Ω, whereas Fig. 5.4 shows the range of Z_o for Z_L varying from 60 to 260 Ω. The curves apparently give the realizable values of odd mode impedance (Z_o) for the chosen frequency and transformation ratios. The free variables Z_1 and Z_2 can be varied to develop realizable matching between higher values of Z_L and the source impedance while also maintaining the realizability of Z_o as shown in Fig. 5.4. Now, all the required parameters to design section 1 and section 2 of the impedance matching network is available and therefore the net imaginary impedance at node N_1 can be cancelled using the stub (section 3) that is used

Table 5.1: Case Studies and Design Examples

Case	Freq-uencies, (GHz)	Z_L, (Ω)	Section 2 Z_1 (Ω), Z_2 (Ω), θ_2 (°)	Section 1,(for ρ =2.298) Z_e (Ω), Z_o (Ω), θ_1 (°)	Section 3 Z_3 (Ω), θ_3 (°) (open/short)	10dB BW,(MHz) @f_1, f_2
Case 1	f_1 1 f_2 = 2	60	Z_1= 80, Z_2 = 80, θ_2=60	Z_e = 133.56, Z_o = 58.12, θ_1=60	Z_3 = 66.61, θ_3=120 (O)	130, 130
Case 2	f_1= 1 f_2 = 2	100	Z_1= 100, Z_2 = 100, θ_2=60	Z_e = 155.16, Z_o = 67.52, θ_1=60	Z_3 = 86.6, θ_3=120 (O)	100, 100
Case 3	f_1= 1 f_2 = 2	200	Z_1= 100, Z_2 = 104, θ_2=60	Z_e = 57.45, Z_o = 25, θ_1=60	Z_3 = 46.81, θ_3=120 (O)	60, 60
Case 4	f_1= 1 f_2 = 2	300	Z_1= 80, Z_2 = 80, θ_2=60	Z_e = 113.33, Z_o = 49.32, θ_1=60	Z_3 = 72.17, θ_3=60 (S)	100, 100
Case 5	f_1= 1 f_2 = 2	10	Z_1= 38, Z_2 = 40, θ_2=60	Z_e = 153.01, Z_o = 69.55, θ_1=60	Z_3 = 54.13, θ_3=120 (O)	60, 60
Case 6	f_1= 1 f_2 = 1.8	10	Z_1= 29, Z_2 = 35, θ_2=64.28	Z_e = 95.59, Z_o = 43.45, θ_1=64.28	Z_3 = 26.69, θ_3=128.5 (O)	60, 400

to nullify this imaginary impedance. The electrical length and characteristic impedance of the stub can be computed using (5.10) and (5.11), respectively.

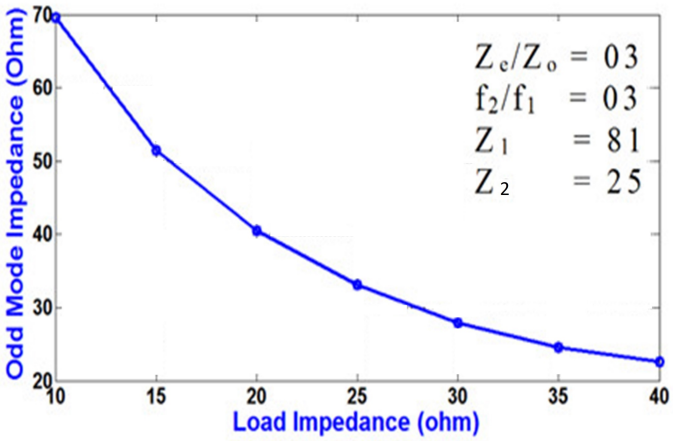


Figure 5.3: Realizable Range of Load Impedances

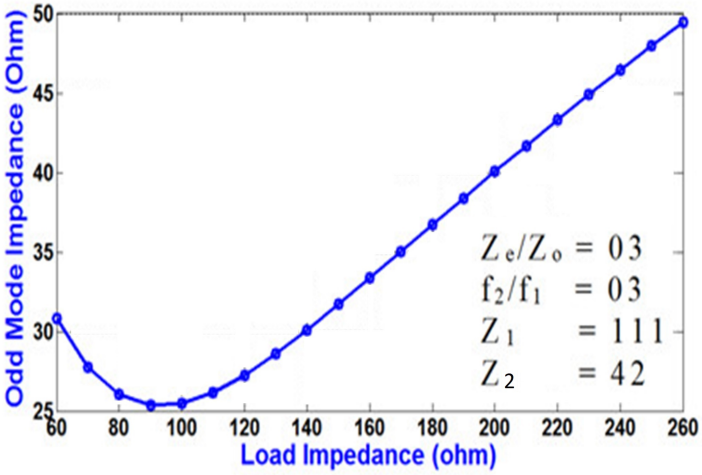


Figure 5.4: Realizable Range of Load Impedances

5.2.3 Case Studies and Design Examples

Several case studies for varying transformation ratios (here its assumed that the Z_S=50 Ω and Z_L is varied) are given in Table 5.1. It is evident that the values of various parameters for all the three sections of the reported impedance transformer are realizable. The chosen values of Z_L demonstrate that the reported technique can cover the matching over whole of smith chart i.e. when the load impedance is inside the 1+jX circle (case 1 for example) and outside of the 1+jX circle (case 5 for example). As the value of impedances can vary on X-axis (on the real line of smith chart) only, the values are chosen accordingly (here, case 1 and case 5).

Subsequently, the design parameters for the examples given in Table 5.1 has been taken to assess the performance of the reported technique. The obtained S_{11} (in dB) for all the cases depicted in Fig. 5.5 show extremely good performance. Eventually, the insertion loss (dB) for all the cases plotted in Fig. 5.6 demonstrate the effectiveness of the strategic impedance matching scheme.

Furthermore, case 3 in Table 5.1 is also simulated to verify the DC blocking property of the proposed impedance transformer. The transmission parameter S_21 is plotted and depicted in Fig. 5.7 which demonstrates that the dB amplitude of S_21 at DC (0 GHz) is zero and therefore indicating that no transmission is happened.

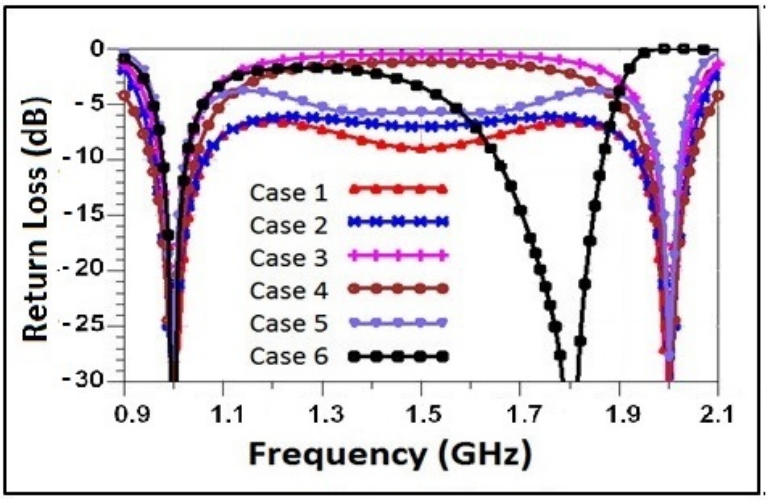


Figure 5.5: S_{11} response of simulated cases

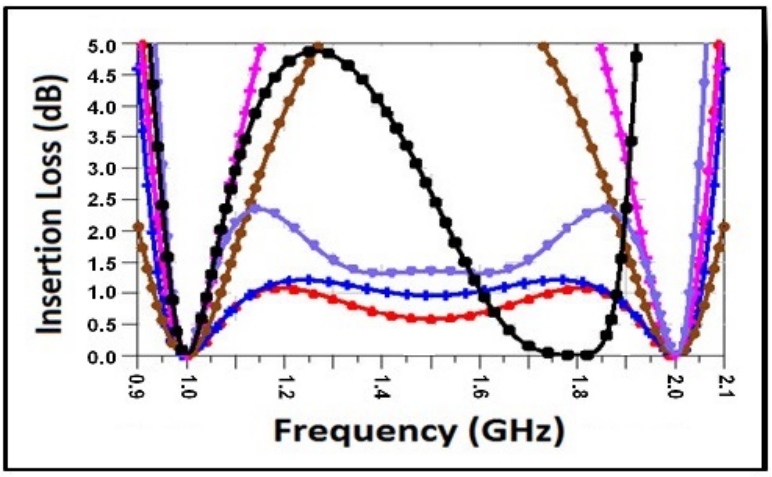


Figure 5.6: Insertion Loss of simulated case

5.2.4 Fabrication and Measurement

A prototype, given in Fig. 5.8, has been developed on RO4350B with substrate height of 1.524 mm, copper thickness 35 μm, and permittivity (ε_r) = 3.66. The chosen frequencies are f_1 = 1 GHz and f_2 = 2 GHz and this prototype essentially is the case 3 in Table 5.1. The measured return loss, depicted in Fig. 5.9, compare favorably to the EM simulated and theoretical values, and thus validate the effectiveness of the reported impedance transformer. The EM simulated results are optimized to compensate the paracitic/losses occurred due to the use of a lumped resistor as a load, transmission line discontinuities and in-house fabrication. Furthermore, the performance can be enhanced by utilizing better substrates and better fabrication technique.

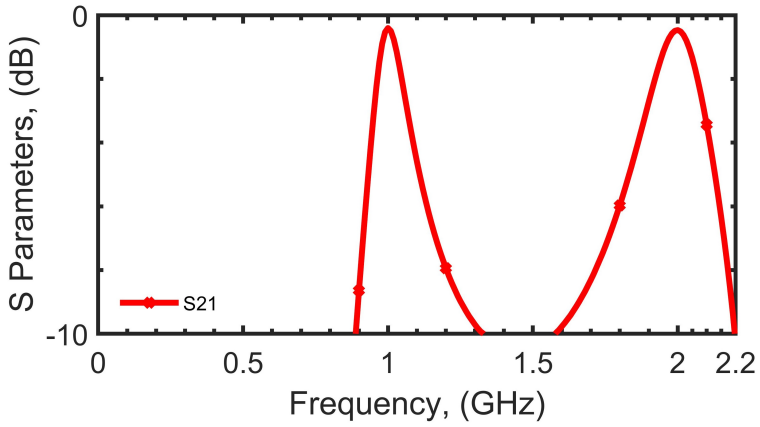


Figure 5.7: Simulated performance of the proposed DC blocking impedance transformer

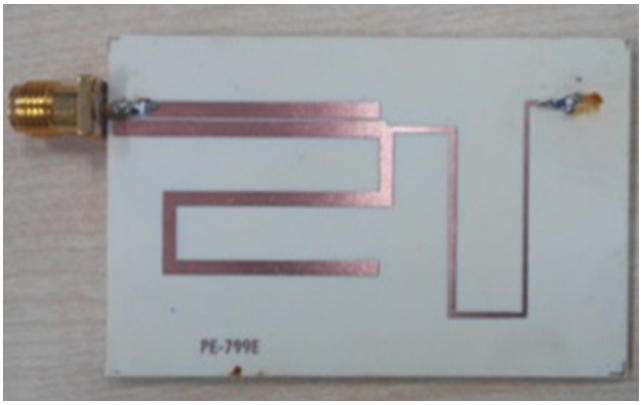


Figure 5.8: Designed prototype on RO4350 [case 3]

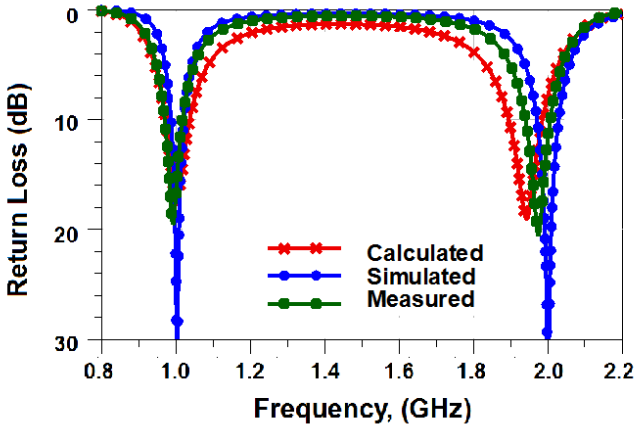


Figure 5.9: S_{11} of the prototype [case 3]

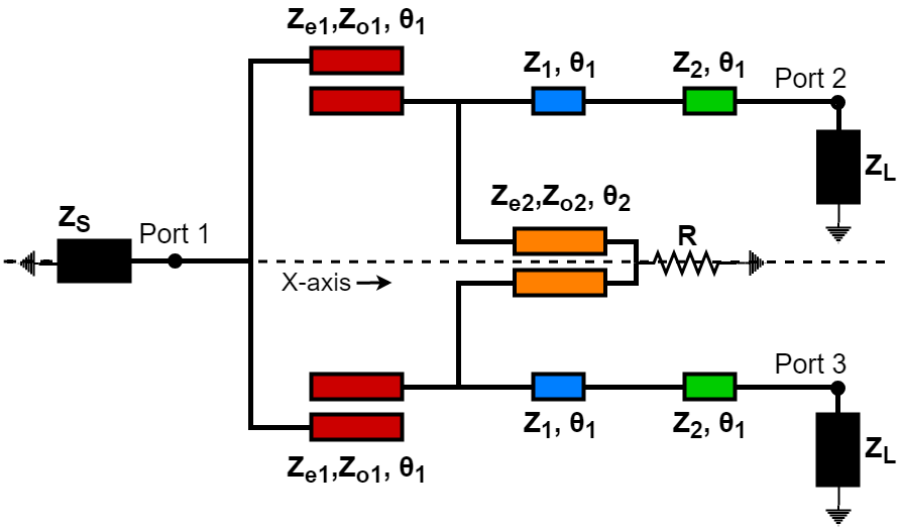


Figure 5.10: The proposed Multi-functional Power Divider

5.3 Dual-Band Multi-Functional Power Divider

Figure 5.10 shows the proposed dual-band PD architecture with different input and output ports impedances. Here, port 1 is the input port, with port impedance Z_S, and port 2 and port 3 are the output ports, with equal port impedance Z_L. The power division at the output ports is achieved using two coupled-lines with Z_{e1} and Z_{o1} as the even-odd mode impedances, respectively, and two TSTLs with impedances Z_1 and Z_2. The electrical length for the coupled-lines and the TSTLs is θ_1. Another coupled-line, with Z_{e2} and Z_{o2} as the even-odd mode impedances respectively and θ_2 as the electrical length, is used along with a resistor R for the isolation between the output ports. The coupled line, here, provides a degree of freedom due to its even- and odd-mode impedances. All the characteristic impedances, in Ω, and the electrical lengths, in degrees °. Here all the electrical lengths are defined at first frequency, i.e., f_1.

5.3.1 Even-mode Analysis

Owing to the symmetry property of the proposed circuit, the even-odd mode analysis is utilized here to analyze the proposed circuit. The even-mode equivalent circuit is demonstrated in Fig. 5.11. In the even-mode analysis, the resistor across the X-axis is shorted to ground whereas the coupled-line is reduced to a TL with effective characteristic impedance Z_{e2}, the even-mode impedance of the coupled-line. The equivalent circuit resembles like the DC blocking

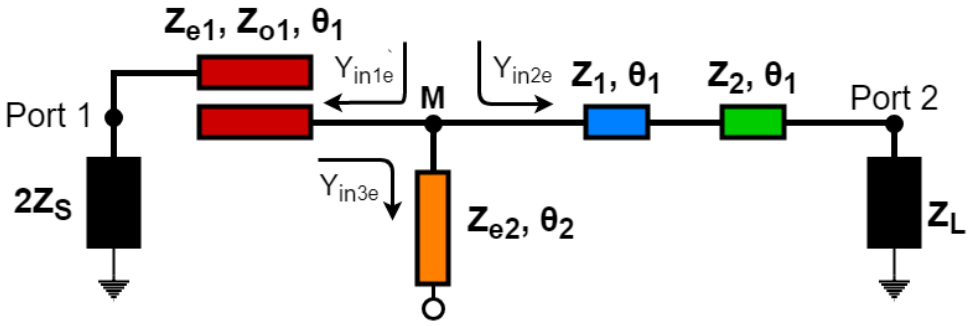


Figure 5.11: Even-mode equivalent circuit

impedance transformer circuit depicted in 5.2. Therefore, following the same analysis, the design parameter Z_{o1} can be expressed as:

$$Z_{o1} = \sqrt{\frac{4Z_S\left[(\rho+1)^2-4\rho+(\rho-1)^2tan^2\theta_1\right]\left[{Z_L}^2(Z_1-Z_2tan^2\theta_1)^2+{Z_1}^2(Z_1+Z_2)^2tan^2\theta_1\right]}{\left[Z_L{Z_1}^2(1+tan^2\theta_1)^2\right]\left[(\rho-1)^4tan^2\theta_1+16\left(\rho^2tan^2\theta_1\right)-8\rho(\rho-1)^2\right]}} * \sqrt{\frac{-4{Z_S}^2Z_L{Z_1}^2(\rho+1)^2(1+tan^2\theta_1)^2}{\left[Z_L{Z_1}^2(1+tan^2\theta_1)^2\right]\left[(\rho-1)^4tan^2\theta_1+16\left(\rho^2tan^2\theta_1\right)-8\rho(\rho-1)^2\right]}} \quad (5.12)$$

$$\begin{aligned}\mathrm{Im}\left(Y_{in3e}\right) &= j\left(B_{in1e}+B_{in2e}\right) = j\left(1/Z_{e2}\right)tan\theta_2 f_1 \\ &= -j\left(B_{in1e}+B_{in2e}\right) = j\left(1/Z_{e2}\right)tan\left(r\theta_2\right)f_2 \end{aligned} \quad (5.13)$$

Furthermore, the short or open-stub with characteristic impedance Z_{e2} is used to cancel the effective imaginary admittance at node M (in Fig. 5.11), i.e. $j(B_{in1e}+B_{in2e})@f_1$ and f_2. The expressions of design parameters are provided in (5.14) and (5.15).

$$\theta_2 = \left(\frac{n+1}{r+1}\right)\pi;\ n \in I \quad (5.14)$$

$$\mathrm{Z_{e2}} = \frac{tan\theta_2}{\left(B_{in1e}+B_{in2e}\right)} \quad (5.15)$$

5.3.2 Odd-mode Analysis

The odd-mode equivalent circuit of the PD is demonstrated in Fig. 5.12. The resistor across the X-axis is effectively R/2 now, and the coupled-line is reduced to a TL with effective

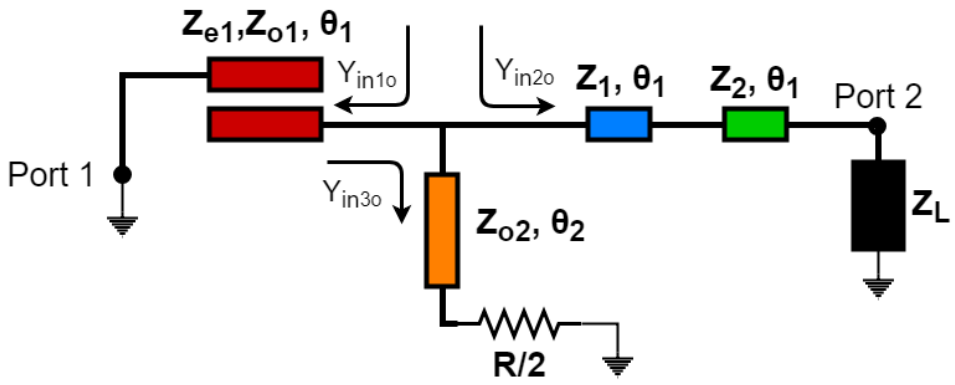


Figure 5.12: Odd-mode equivalent circuit

characteristic impedance Z_{o2}, the odd mode impedance of the coupled line. The respective input admittance are mentioned as Y_{in1o}, Y_{in2o}, and Y_{in3o}. Here, Z_{o2} and R are the only unknown design parameters to be computed.

The admittances Y_{in1o} and Y_{in2o} can be derived similarly as Y_{in1e} and Y_{in2e} in the even-mode analysis and can be written as (5.16) and (5.17) respectively, where $G_{in1o} = 0$ and B_{in1o} is expressed in (5.18).

$$Y_{in1o} = G_{in1o} + \mathrm{j}\, B_{in1o} \tag{5.16}$$

$$Y_{in2o} = Y_{in2e} = G_{in2e} + \mathrm{j}\, B_{in2e} \tag{5.17}$$

$$B_{in1o} = \left(\frac{\rho+1}{Z_o}\right)\left(\frac{8\rho {Z_{o1}}^2 cos^3\theta_1/sin\theta_1 - (\rho-1)^2 {Z_{o1}}^2 sin^2\theta_1}{(\rho-1)^4 {Z_{o1}}^2 sin^2\theta_1 - 8\rho(\rho-1)^2 {Z_{o1}}^2 cos^2\theta_1 + 16\rho^2 {Z_{o1}}^2 cos^4\theta_1/sin^2\theta_1}\right) \tag{5.18}$$

Now the effective admittance due to the combination of Y_{in1o} and Y_{in2o}, should be matched with the effective admittance offered by Y_{in3o}, which can be expressed as (5.19).

$$Y_{in3o} = G_{in3o} + \mathrm{j}\, B_{in3o} \tag{5.19}$$

Where,

$$G_{in3o} = \frac{(R/2)(1+\tan^2\theta_2)}{(R^2/4)+Z_{o2}^2\tan^2\theta_2} \tag{5.20}$$

Table 5.2: Various Design Cases For The Proposed PD

Cases	k = Z_L/Z_S	r	Z_{e1}/ Z_{o1} (Ω)	$\theta_1(^\circ)$	Z_1 (Ω)	Z_2 (Ω)	Z_{e2}/ Z_{o2} (Ω)	θ_2°	R(Ω)
1	1.66(50/30)	2	87.7/57.4	60	135	35	84.7/71.0	120	3.64k
2	50(500/10)	2	87.6/58.3	60	100	60	108.7/100.6	120	4.04k
3	10(50/5)	2	87.3/55.3	60	135	30	69.4/67.6	120	4.71k
4	0.1(5/50)	2	81.6/60.2	60	90	35	114.0/57.5	120	4.79k
5	2(100/50)	3	139.8/45.0	45	150	150	78.3/42.9	135	0.89k
6	0.5(25/50)	3	97.2/52.2	45	150	125	73.7/63.3	135	3.02k

$$B_{in3o} = \frac{\left((R^2/4) - Z_{o2}^2\right) \tan\theta_2}{(R^2/4) + Z_{o2}^2 \tan^2\theta_2} \tag{5.21}$$

Following (5.22) and (5.23) the design parameters R and Z_{o2} can easily be computed.

$$G_{in3o} = G_{in1o} + \mathrm{G}_{in2e} \tag{5.22}$$

$$B_{in3o} = \text{-}(\mathrm{B}_{in1o} + B_{in2e}) \tag{5.23}$$

5.3.3 Systematic Design Procedure

The systematic design procedure of the proposed PD is elaborated in this section as follows:

- At first the independent design parameters Z_1, Z_2 and ρ are chosen. The source and load impedances Z_S and Z_L are as per the design requirement. Also, the electrical length θ_1 is calculated accordingly for the required frequency ratio.
- The design parameter Z_{o1} is computed from (5.12).
- Subsequently, Z_{e2}, and θ_2 are calculated from (5.14) and (5.15) respectively.
- Finally, R and Z_{o2} are computed by solving (5.22) and (5.23).

Furthermore, case 1 is also simulated to verify the DC blocking property of the proposed power divider. The transmission parameter S_21 is plotted and depicted in Fig. 5.13 which demonstrates that the dB amplitude of S_21 is zero at DC (0 GHz) and therefore indicating that no transmission is happened.

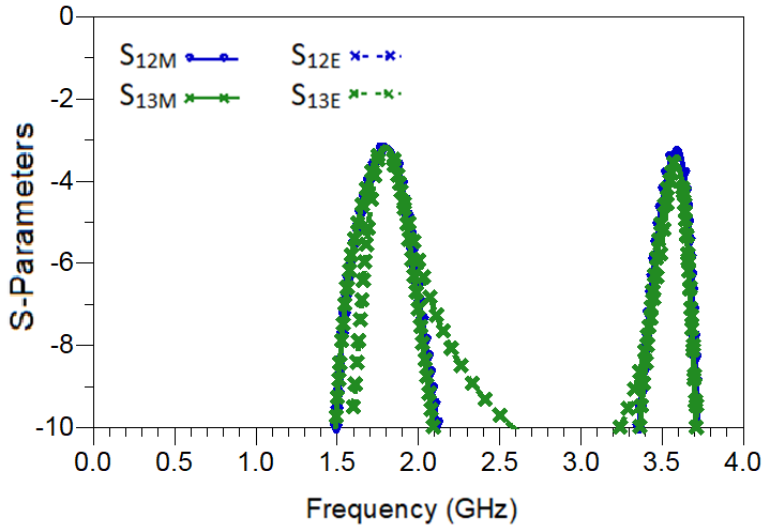


Figure 5.13: Simulated performance of the proposed DC blocking power divider

5.3.4 Design Cases

To validate the proposed design and design analysis, a few design cases are provided in Table 5.2 with varying frequency ratio ($r = f_2/f_1$) and impedance transformation ratio ($k = Z_L/Z_S$). The design parameters are computed following the design procedure. It is apparent in Table 5.2 that the design has realizable parameters for a wide range of frequency ratio and the impedance ratio. The point of interest is the possibility of the extreme impedance ratios as the design can match the impedances as high as 500 Ω (case 2) and as low as 5 Ω (case 3 and case 4). This demonstrates the inherent impedance transformation capability of the design for energy harvesting and wireless power transfer applications [14].

5.3.5 Fabrication and Measurement

To validate the design concept and inherent impedance transformation of the design, Case 1 from Table 5.2 is prototyped with input port impedance 30 Ω and the output ports impedance 50 Ω. The prototype, working at f_1=1.8 GHz and f_2=3.6 GHz is fabricated on RO5880 substrate with height 1.575 mm, copper cladding 35 μm on both the sides and permittivity (ε_r) 2.2. The dissipation factor (tan δ) for the substrate is 0.0009. The fabricated prototype is shown in fig. 5.14. The effective PD is of dimension 7.1 $\times$ 6.6 cm^2 only which is extended with a redundant stepped impedance transformer [2] at the input port for the commercially available

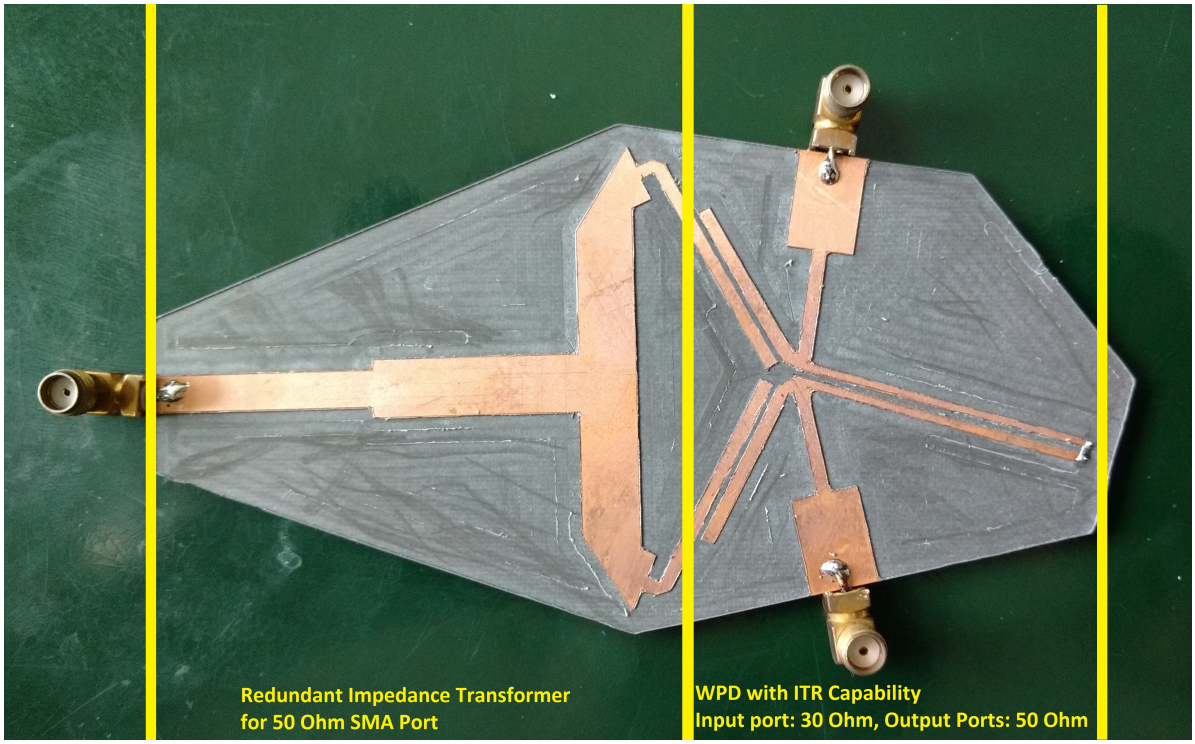
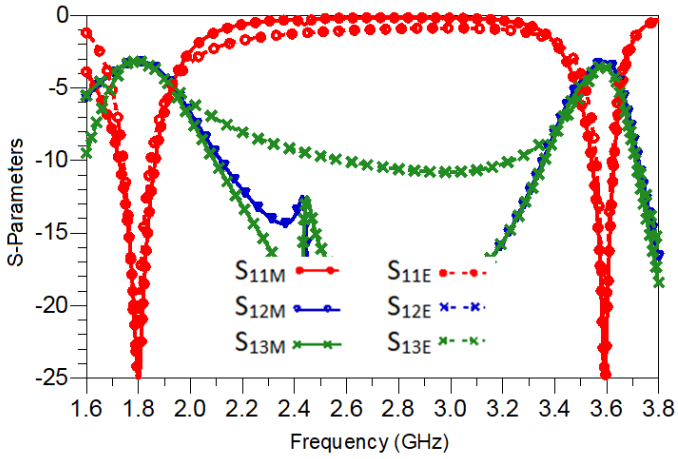
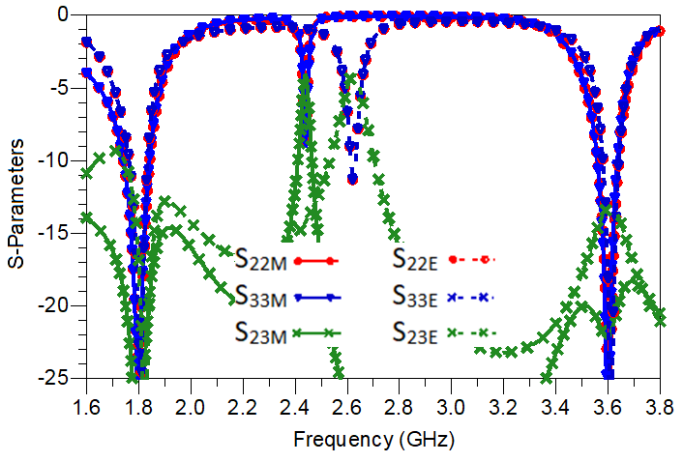


Figure 5.14: The fabricated Power Divider with redundant impedance transformer

50 Ω connector for the measurement purpose. The design is simulated on Keysight ADS tool and the design parameters are optimized due to TL discontinuities and the commercially available resistor, i.e. R. The measurement results in comparison with the EM simulation results are demonstrated in figs. 5.15 and 5.16. The matching at all three ports is approximately measured to be better than -10 dB for 1.73 - 1.86 GHz @f_1 and 3.54 - 3.63 GHz @f_2. The measured isolation performance is below -10 dB at almost all the frequencies. The phase difference between the two output ports and the amplitude imbalance is less than 3° and 0.5 dB respectively for more than 100 MHz (1.6 - 2.03 GHz @f_1 and 2.92 - 3.62 GHz @f_2) of bandwidth. These measurement result matches very well with the EM Simulation results and hence validates the proposed design. The performance metrics of the designed prototype is mentioned in Table 5.3 where the design is compared with the recently published PDs.



(a)



(b)

Figure 5.15: EM Simulation (E) vs Measurement results (M): S-Parameters.

5.4 Balanced to Unbalanced Signal Transformation

A balanced signal can be defined as the set of two signals with equal amplitude but opposite direction of propagation. It actually signifies that both the signals have a phase difference of 180° in reference to each other. Therefore, these are also called differential signals. However, the unbalanced or single-ended signal has a ground plane as a reference.

A component that transforms an unbalanced signal to a balanced signal or vice-versa is known as *Balun*, depicted in Fig. 5.17. Most commonly, RF baluns are used with many antennas and their feeders to transform a balanced feedline to an unbalanced one. Other applications include balanced mixers, push-pull amplifiers, local oscillator, etc. Additionally,

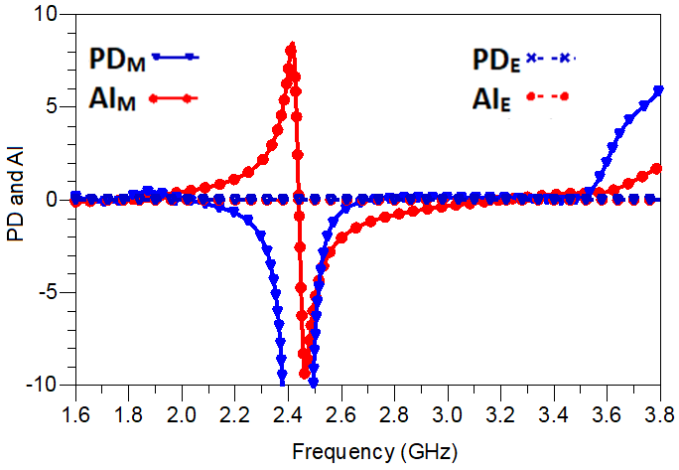


Figure 5.16: EM Simulation (E) vs Measurement results (M), PD and AI: Phase Difference and Amplitude Imbalance between output ports

Table 5.3: Comparison With State-Of-The-Art Techniques [*As per the test cases provided, ^Case (a) in [7], NA: Not Available, AI: Amplitude Imbalance, PI: Phase Imbalance]

Ref.	Frequency f_1/ f_2 (GHz)	S_{11} @ f_1/ f_2 (dB)	S_{22}, S_{33} @f_1/f_2 (dB)	S_{23} @f_1/ f_2 (dB)	AI @ f_1/f_2 (dB)	PI @f_1/ f_2 (°)	r	k
[105]	1.5/2.4	-28/-37	-18/-14, NA	-15/-16	<0.8	<5	1.1- 2.9 (dB)	1.5
[99]	0.5/3.65	-38/-16	-3.1/-3.2	-30/-25	<0.5	<5	2.44- 7.31 (dB)	2
[7]	1.0^	-20	-20, -20	-23	<0.5	<5	Single -band (dB)	2
This Work	1.8/3.6	-19/-17	-3.78/-3.71	-26/-28	<0.5	<3	1.5 3.0	>(0.1 -50)

the all port matching and the isolation between the balanced ports of a balun is extremely important [41]. A simplified and symmetric balun architecture with significantly improved isolation and output port-matching is discussed.

5.5 Simplified Multi-Functional Power Divider with Inherent Balanced to Unbalanced Transformation

A multi-functional power divider structure is provided in this section. The power divider provides the following functions inherently:

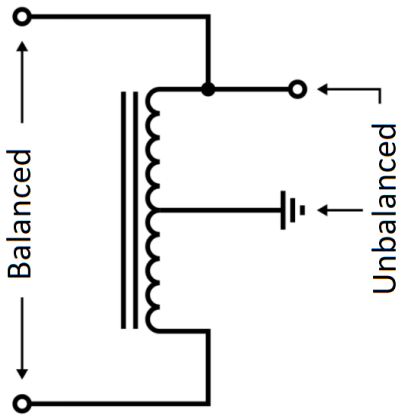


Figure 5.17: A Balun Transformation

- Power division from the input port to the output ports.
- Power combiner for the power available at the output ports to the input port.
- Balanced to unbalanced signal transformation and vice-versa.
- Impedance Transformation.

A power divider with inherent property of balanced to unbalanced signal transformation (or vice-versa) is known as balun [99, 166, 167]. Therefore the provided architecture is named as balun in this section. The reported balun, shown in Fig. 5.18, is symmetric network along the xx'-axis. Here, the Z_i (in Ω) are transmission line characteristic impedances and θ_i ($^\circ$) are the electrical lengths, where $i = \{1,2,..,5\}$, and the port impedances are Z_0 Ω. The incorporation of resistor $R/2$ aids in achieving high isolation at the design frequency without increasing the design complexity.

For successful balun operation, the conditions in (5.24) that is, no signal flows from the input port in the even-mode and the odd-mode input impedance must be twice to that of the input port impedance must be satisfied [41]. Here, T_{even} is the transmission parameter in the even-mode and Z_{Odd} is the odd-mode input impedance of the balun circuit.

$$T_{even} = 0 \ \text{ and } \ Z_{odd} = 2Z_0 \tag{5.24}$$

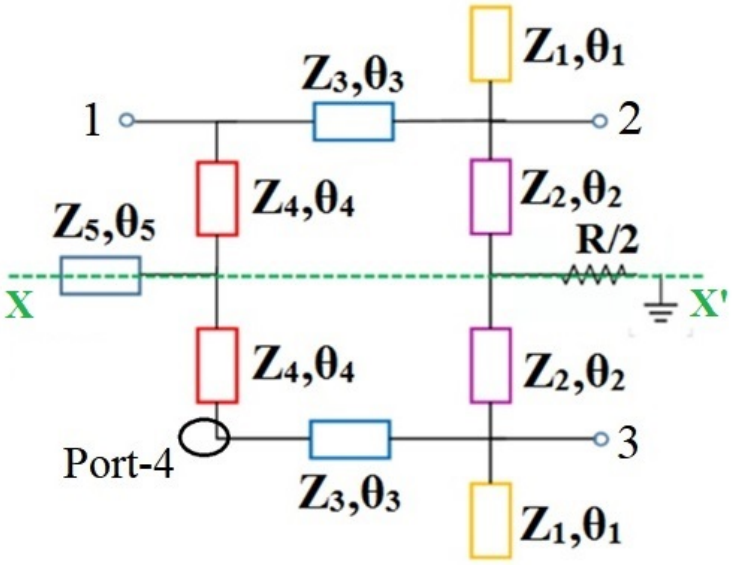


Figure 5.18: The reported architecture of balun

5.5.1 Design Analysis

5.5.1.1 Odd-Mode Analysis

The odd-mode equivalent circuit, in Fig. 5.19(a), is obtained when all the junctions along the xx'-axis are short circuited. The term Z_{odd} is the impedance looking towards node a_1 from the port 1 (input).

At node a_2, the open-circuited stub having admittance Y_a cancels the effect of the short-circuited stub with admittance Y_b and this requires enforcement of (5.25).

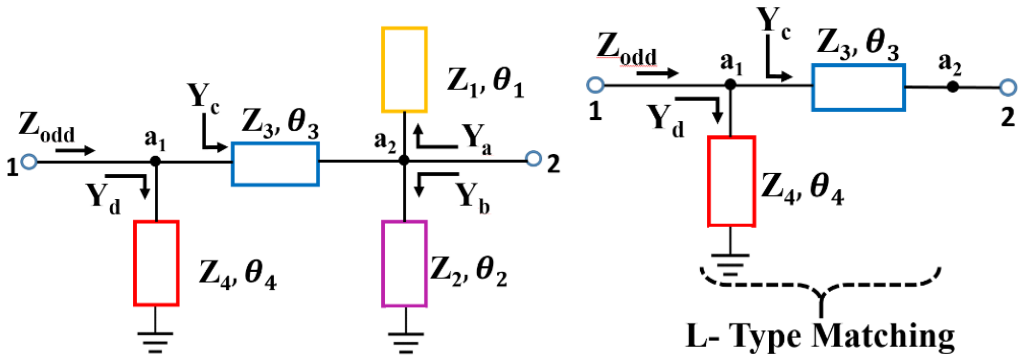
$$Z_1 = Z_2 \tan^2 \theta \quad [for \theta_1 = \theta_2 = \theta] \tag{5.25}$$

After cancellation, the eventual odd-mode circuit can be analyzed as an L-network impedance transformer [49] in Fig. 5.19(b). Furthermore, the admittance Y_C can be represented as:

$$Y_C = G_C + jB_C \tag{5.26}$$

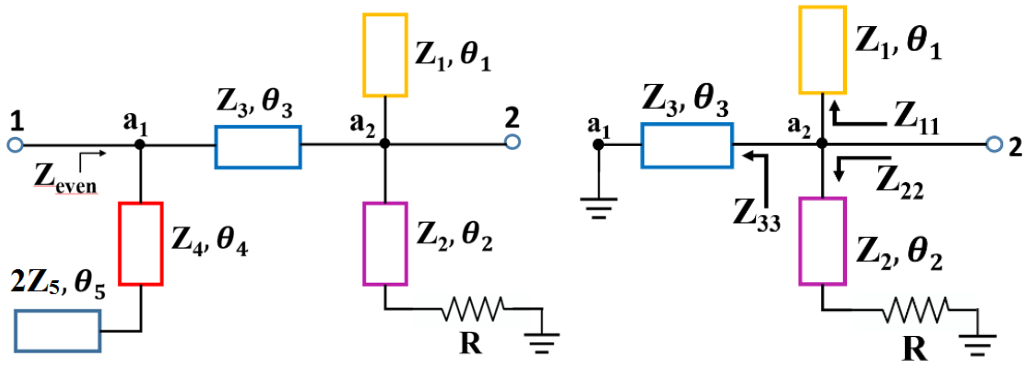
The term B_C is cancelled by short-stub of impedance Z_4 as represented by (5.27).

$$Z_4 = \cot \theta_4 / B_C \tag{5.27}$$



(a) (b)

Figure 5.19: (a) Odd-mode equivalent circuit of the reported balun and (b) Simplified circuit of the odd mode equivalent.



(a) (b)

Figure 5.20: (a) Even-mode equivalent circuit and (b) Simplified circuit of the even-mode equivalent

In order to fulfill (5.24), the odd-mode impedance must meet the condition $G_C = 1/2Z_0 = 1/Z_{odd}$ and this results in expression (5.28).

$$Z_3 = \sqrt{\frac{Z_0^2(1+2\tan^2\theta_3)}{\tan^2\theta_3}} \tag{5.28}$$

5.5.1.2 Even-Mode Analysis

In the even-mode circuit, shown in Figure 5.20(a), obtained by opening the nodes along xx'-axis, the term Z_{even} is the impedance looking towards node a_1 from port 1. In order to satisfy $T_{even} = 0$, conditions $\theta_4 + \theta_5 = (2n+1)\pi/2$ and $Z_5 = Z_4/2$ are imposed to achieve a virtual ground at node a_1 ($Z_{even} = 0$) and this results in an equivalent circuit as shown in Figure 3B.

Now, the symmetry of the reported balun that is, S_{33} = 0 and S_{23} = 0, requires S_{22e} = 0. A simple solution for meeting this condition is the incorporation of resistor R/2 as shown in the reported balun in Figure 5.18.

Now, matching at output port 2 leads to (5.30), with Z_{11}, Z_{22}, and Z_{33} being the respective input impedances.

$$S_{22e} = 0 \tag{5.29}$$

$$\frac{1}{Z_0} = \frac{1}{Z_{11}} + \frac{1}{Z_{22}} + \frac{1}{Z_{33}} \tag{5.30}$$

Analysis of Fig. 5.20(b) in conjunction with (5.30) and by assuming $\theta_1 = \theta_2 = \theta_3 = \theta$ gives the expressions for R and Z_2.

$$Z_2 = \pm \frac{\sqrt{R(Z_0 - R + Z_0 \tan^2 \theta)}}{\tan \theta} \tag{5.31}$$

$$R = \pm Z_2 \tan \theta \sqrt{\frac{Z_2}{Z_3 - Z_2 + Z_3 \tan^2 \theta}} \tag{5.32}$$

The value of isolation resistor R and Z_2 can be computed using Equations (5.31) and (5.32). Either positive or negative sign can be omitted for practical values once computed.

5.5.2 Case Studies and Design Examples

The design could be categorized in two categories and the respective design analysis is discussed in detail.

5.5.2.1 Case 1: $\theta_1 = \theta_2 = \theta_3 = \theta$

- Choose any value of θ. Calculate Z_3 from (5.28) to satisfy (5.24) (to match the real part of Z_{odd} with the twice of the impedance at port 1).
- Compute Z_4 from (5.27) by selecting value of θ_4 to mitigate the imaginary part of Z_{odd}.
- Use (5.31) and (5.32) to calculate R and Z_2 and then determine Z_1 from (5.25).

Table 5.4: Special Feature Of Higher Impedance Ratios [D. P.: Design Parameter]

Impedance ratio: 5/50				**Impedance ratio: 500/50**			
D. P.	**Value**	**D. P.**	**Value**	**D. P.**	**Value**	**D. P.**	**Value**
Z_1	125.1	θ_4	160	Z_1	80	θ_4	15
Z_2	27.2	Z_5	33.2	Z2	138.6	Z_5	33
Z_3	70.7	θ_5	110	Z_3	34.9	θ_5	75
Z_4	66.4	$R/2$	77.4	Z_4	65.9	$R/2$	493.4
θ_1 = 10, θ_2 = 87.8, θ_3 = 18				θ_1 = 30, θ_2 = 45, θ_3 = 63.72			

- Calculate the values of Z_5 and θ_5 by considering $Z_5 = Z_4/2$ and $\theta_5 = \pi/2 - \theta_4$. For positive θ_5, $\theta_4 + \theta_5 = (2n+1)\pi/2$ is followed, where, $n \in I$. This is to keep the sum equal to the odd multiple of a quarter wavelength transmission line.

A design example for equal electrical lengths is considered to demonstrate the effectiveness of the provided technique. Here, the ports are considered to be terminated with 50 Ω while the electrical lengths θ_1, θ_2 and θ_3 are assumed to be 45° at the design frequency. The calculated value of Z_3 is 86.6 Ω and it is within the realizable limit. Subsequently, $\theta_4 = 120°$ is chosen and it yields Z_4 = 100 Ω and hence Z_5 = 50 Ω and $\theta_5 = 150°$. The computed values for Z_2 and Z_1 comes out to be 43.3 Ω for both. The determination of Z_2 and Z_3 enables the computation of $R/2$ which is equals to 12.5 Ω.

5.5.2.2 Case 2: $\theta_1 \neq \theta_2 \neq \theta_3$

The inherent impedance transformation capability of the architecture is apparent once it is analysed for different electrical lengths. The varied range of impedance transformation ratio finds usefulness in design of circuits for various applications [41, 130, 131]. In this case, the design steps are similar to case-I with the only change being different electrical lengths (such as (5.25) becomes $Z_1 = Z_2\ tan\theta_1 tan\theta_2$). Table 5.4 provides two extreme scenarios for the impedance transformation ratios of as low as 1/10 and as high as 10 along with the design parameters (D.P.). It is apparent that the D.P.s are within the realizable limits of 20 Ω and 140 Ω. The value of $R/2$ can be optimized (or recalculated) for the nearby available values subsequently.

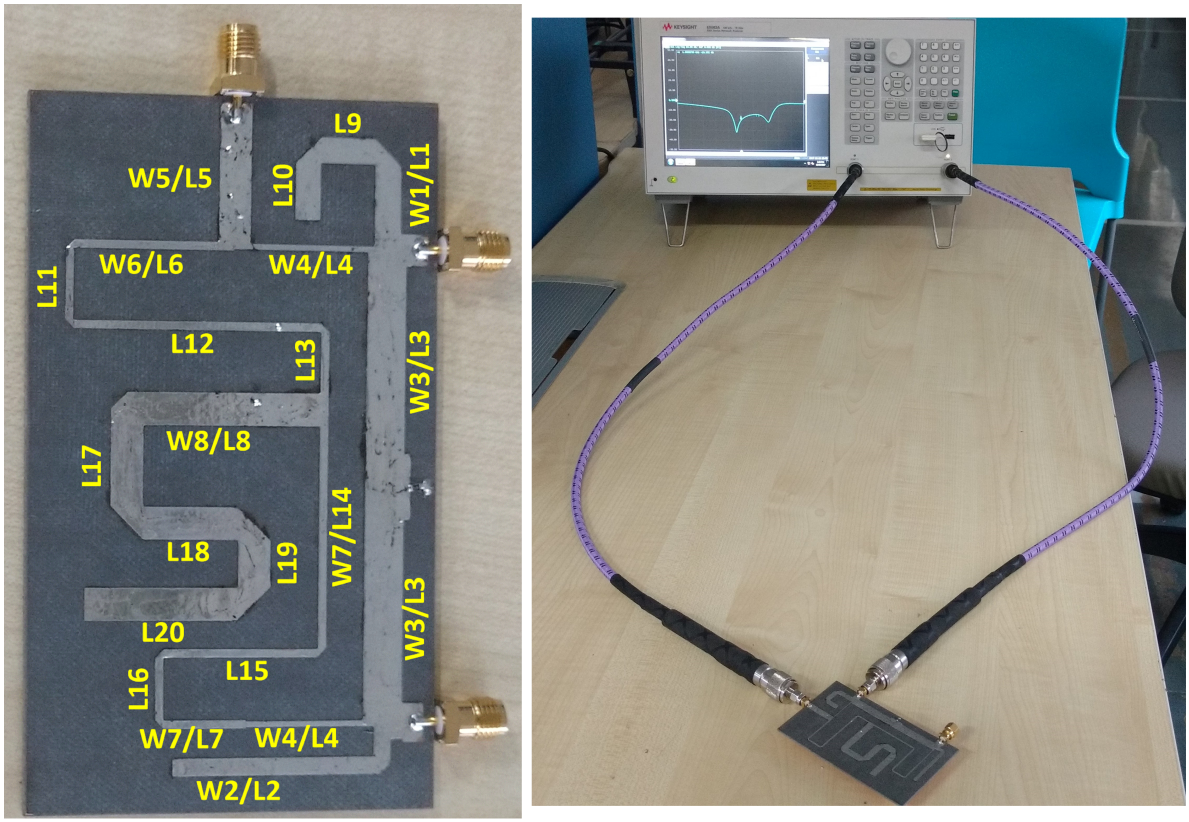


Figure 5.21: The balun prototype and the measurement setup. Dimensions (mm): W1 = 3.4, W2 = 2.9, W3 = 6, W4 = 1, W5 = 4.8, W6 = 1.2, W7 = 1, W8 = 4.7, L1 = 9.6, L2 = 29.6, L3 = 27.1, L4 = 17.2, L5 = 19.7, L6 = 20.6, L7 = 12, L8 = 25.6, L9 = 7.9, L10 = 8.2, L11 = 10, L12 = 35.9, L13 = 8.8, L14 = 32.1, L15 = 22.5, L16 = 9.5

5.5.3 Fabricated Prototype

After the determination of the D.Ps., Keysight ADS was used to carry out the simulation at 1.0 GHz to evaluate the performance of the reported design. Subsequently, for validation of the reported approach, a prototype has been developed on a 62 mil thick RT/duroid 5880 substrate with the dielectric constant of 2.2 and the loss-tangent of 0.0009. The copper-cladding on both the sides of the substrate is 35 μm. The fabricated prototype, with an overall dimensions of 95 $\times$ 53 mm^2, along with the measurement setup is shown in Fig. 5.21. It is important to note that the final design requires some optimization in the ADS to compensate for the effects of junctions at the nodes and airgap of the isolation resistor.

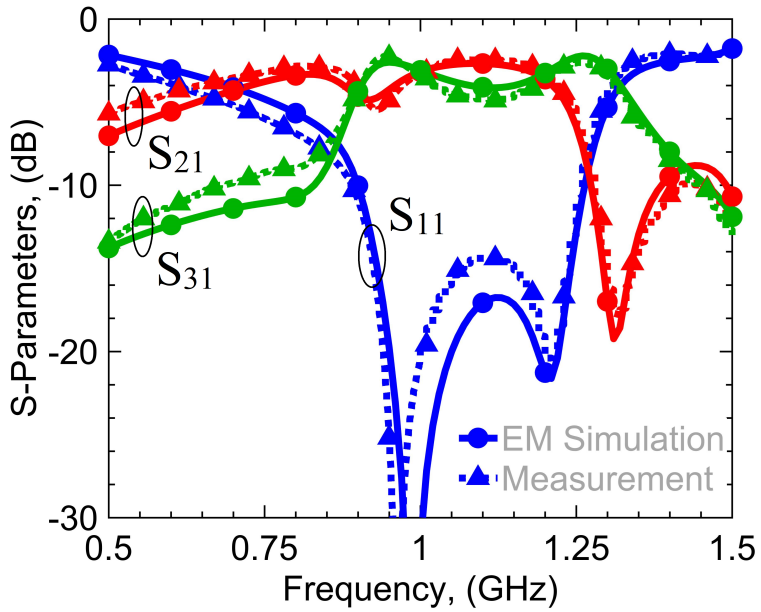


Figure 5.22: EM simulated vs measurement results of the prototype: return loss and insertion loss

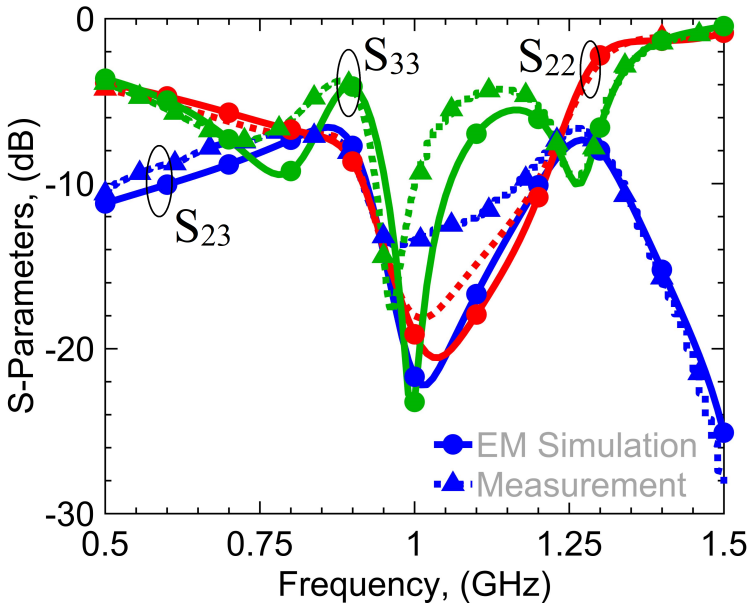


Figure 5.23: EM simulated vs measurement results of the prototype: output ports matching and isolation between the output ports

5.5.3.1 Simulation And Measurement Results

The plots in Figs. 5.22-5.25 provide the input port matching and insertion loss of the design, isolation along with the matching at its output ports, the phase difference between the signal at

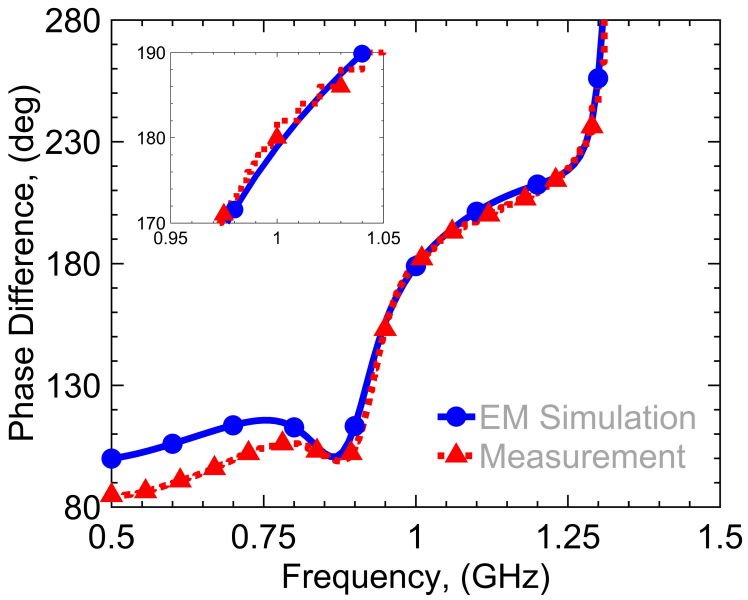


Figure 5.24: EM simulated vs measurement results of the prototype: phase difference

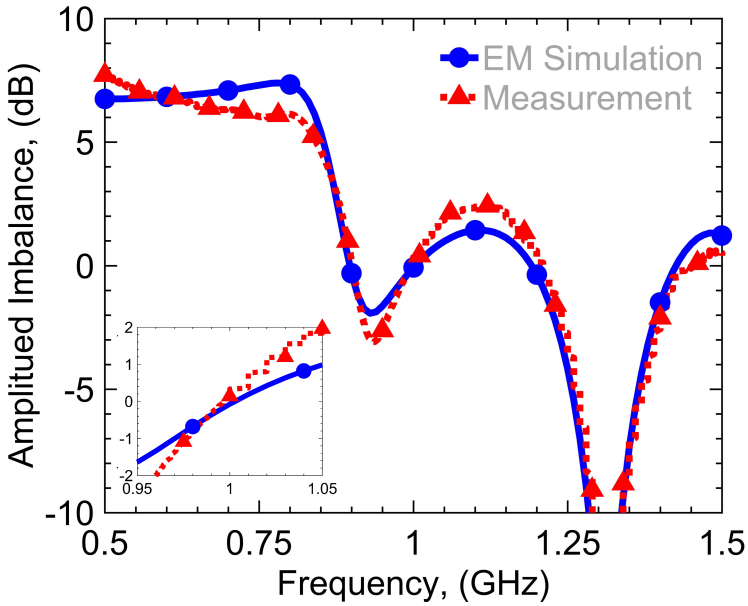


Figure 5.25: EM simulated vs measurement results of the prototype: amplitude imbalance

the output ports, and the amplitude imbalance of the balun. The respective measured values of S_{11}, S_{22}, S_{33}, S_{23}, S_{21}, and S_{31} are -31 dB, -18.0 dB, -17.1 dB, -14.1 dB, -3.28 dB, and -3.42 dB near the design frequencies whereas the phase difference (S_{21}-S_{31}) is 180° (for a bandwidth of 8%). It is also apparent that the measured and EM simulated are in good agreement with slight anomaly in S_{23} and S_{33} values which could be attributed to the mutual coupling between

Table 5.5: Comparison With Previously Reported Designs [[a]Planar architecture with coupled lines, [b]Planar architecture, [c]Non-planar, NA: Not Available]

Ref	F_0 GHz/ FBW (%)	Amplitude/ phase Imbalance (dB))	IL/RL (dB))	Isolation (dB))	k	Design Analysis)	Layout Complexity
[41]	1/29, 2.6/10	1/5	3.5±1.0 /10	–25	0.28-1.96	Analytical	a
[168]	1/11	0.8/±5	3.0±0.0 /10	No	No	Analytical	b
[107]	2.42/2	0.8/±4	3.0±1.7 /10	–13	No	Empirical	b
[165]	4/31	0.6/±8	3.0±2.0 /10	No	No	Empirical	c
[85]	2.6/28	0.8/±9	3.0±0.8 /10	–18	No	Analytical	b
[169]	2.4/5.8	0.37/±5	3.0±1.6 /10	No	No	Analytical	b
[131]	2/37.6	1/±1	4±1.0 /10	No	0.57-2	Analytical	a
[130]	1.2/40	0.5/±5	3.5±0.5 /10	-10	0.8-3.2	Analytical	a
[This Work])	1.0/8	2/±10	3.0±0.5 /10	-20	0.1-10.0	Analytical	b

the TLs near port 3, in-house fabrication and soldering errors. Furthermore, the reported balun is able to provide an amplitude and phase imbalance of 0.14 dB and 0°, respectively at the design frequency of 1.0 GHz.

Finally, performance of the reported design is compared with the existing state-of-the-art in Table 5.5. It is clear that the reported architecture compares favorably with recent designs and also provides enhanced features such as high impedance transformation ratios, output port matching, and isolation between output ports with minimum structural complexity.

5.6 Multi-Functional Power Divider

Again, the power divider is integrated with the inherent property of balanced to unbalanced signal transformation and the component is referred as a Balun. The architecture of the

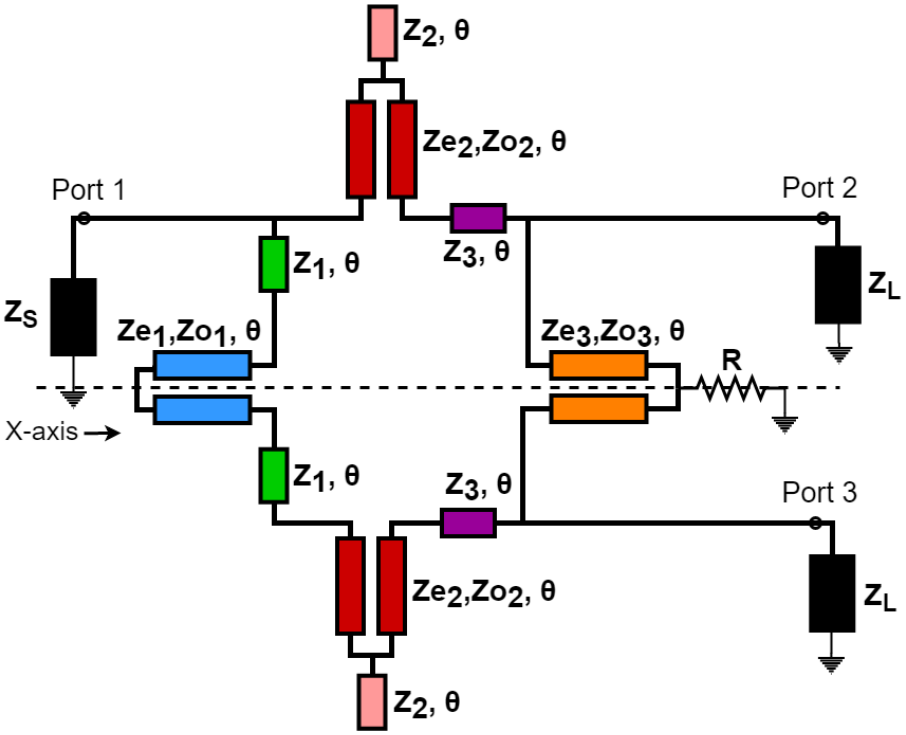


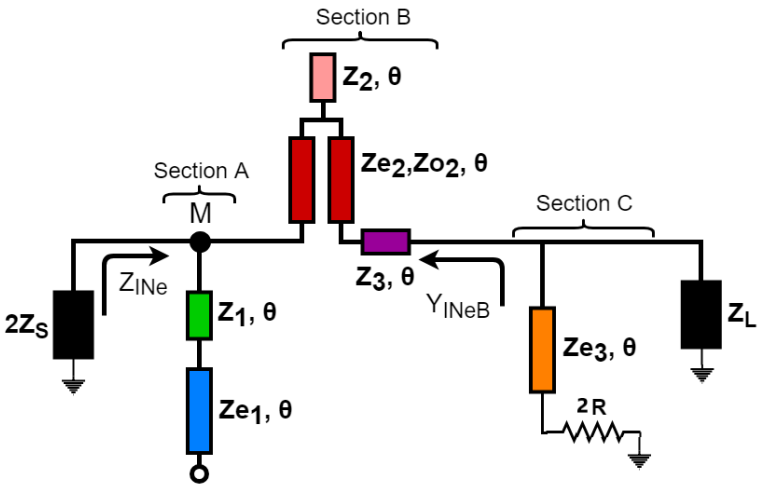
Figure 5.26: The proposed Dual-Band Balun architecture

proposed DBB, in Fig. 5.26, is symmetric to the X-axis and consists of port 1 as input port and ports 2 and 3 as output ports. It incorporates stubs to short the two coupled-line sections perpendicular to the X-axis. An isolation resistor R (Ω) provides isolation between the output ports. The characteristic impedances denoted by Z and the electrical lengths denoted by θ of all the transmission lines (TL) are in Ohms (Ω) and degrees ($^\circ$) respectively. Apparently, even-odd mode analysis can be carried out to simplify the design process. Here, the even mode (e) and odd-mode (o) parameters must satisfy conditions in (5.33) for a balun architecture to ensure matching at all the ports, balanced outputs, and good isolation between the output ports.

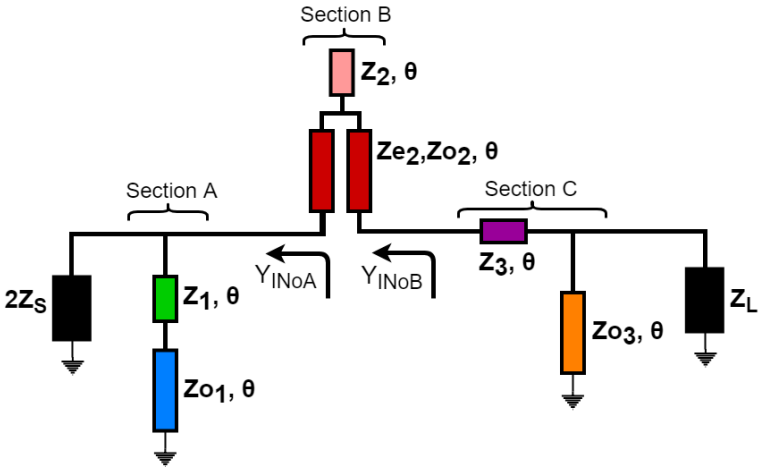
$$S_{21e} = 0; S_{22e} = 0; S_{11o} = 1/3 \tag{5.33}$$

5.6.1 Design Analysis and Procedure

All the TL are considered ideal in the analysis stage. In the even mode circuit, Fig. 5.27 (top), no signal flows in from port 1 and this is ensured by achieving $Z_{INe} = 0$.



(a)



(b)

Figure 5.27: (a) Even-mode and (b) Odd-mode equivalent circuit.

For this, the node M should be short-circuited and this results in (5.34). Here, Z_1 is an independent variable and should be chosen in the range of [20 Ω - 150 Ω] so that all the design parameters are realizable. Here, the electrical length follows $\theta = \pi/1+r$ and r being the desired frequency ratio.

$$Z_{e1} = Z_1 \tan^2\theta \tag{5.34}$$

In the odd mode circuit, Fig. 5.27 (bottom), the term Y_{INoB} is of the form $R_{Bo} \pm jX_{Bo}$. It is the combined admittance of Z_S, section A, and section B looking towards section B. It is matched by an L-type impedance transformer, the section C having Z_{e2}, Z_{o2}, Z_2 as independent

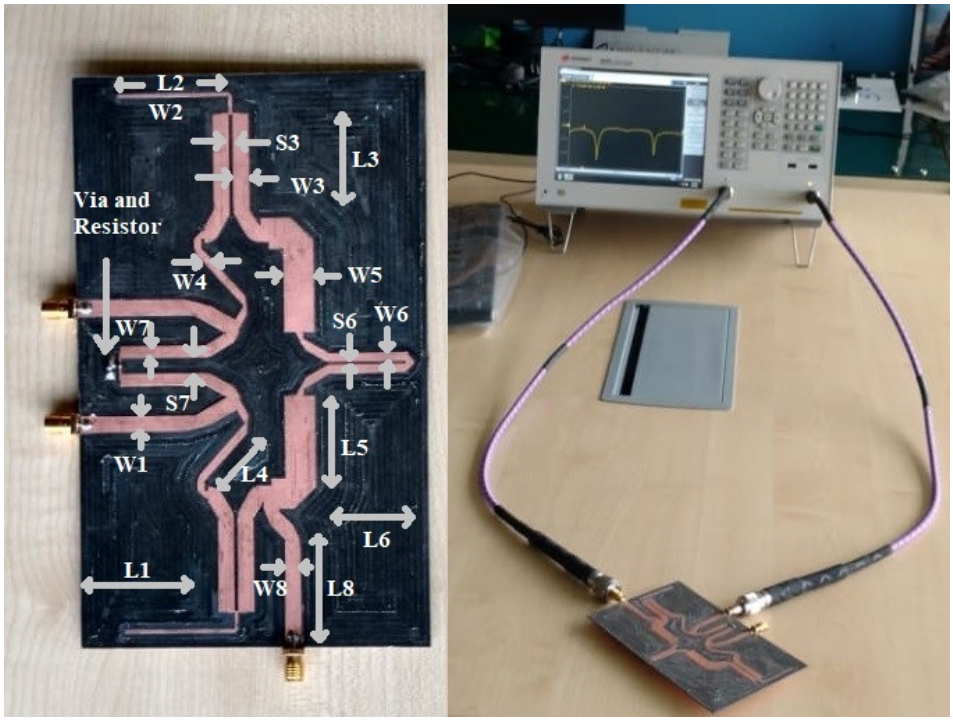


Figure 5.28: The fabricated prototype (left) and measurement setup (right)

variables, which is considered good for high ITR [97]. Subsequently, the dependent parameters are computed from (5.35) and (5.36).

$$Z_3 = \frac{-1 \pm \sqrt{1 - \left({R_{Bo}}^2 + {X_{Bo}}^2 - Z_o R_{Bo} - Z_o R_{Bo} \tan^2\theta\right)}}{\tan\theta} \tag{5.35}$$

$$Z_{o3} = \frac{{Z_3}^3 \tan^2\theta + 2{Z_3}^2 \tan\theta + Z_3 {R_{Bo}}^2 + Z_3 {X_{Bo}}^2}{Z_3 X_{Bo}\left(\tan^2\theta - 1\right)\tan\theta + \left({R_{Bo}}^2 + {X_{Bo}}^2 - {Z_3}^2\right)\tan^2\theta} \tag{5.36}$$

Furthermore, for the matching at the output ports and for isolation between the output ports, the sufficient condition in even mode is $S_{22e} = 0$. Here, node M is shorted and hence the input impedance Y_{INeB}, in the form $0 \pm jX_{Be}$, in parallel with the section C can be matched using the calculated values of Z_{e3} and R as outlined in (5.37) and (5.38).

$${Z_{e3}}^2\left(2{Z_L}^2 R + 2{X_{Be}}^2 R \mp Z_L {X_{Be}}^2\right) + Z_{e3}\left(2{Z_L}^2 R + 2R{X_{Be}}^2 \mp \frac{4R^2 Z_L X_{Be}}{Z_{e3}}\right)\tan^2\theta = 0 \tag{5.37}$$

$${Z_{e3}}^2\left({Z_L}^2 X_{Be} - {Z_L}^2 \tan\theta - {X_{Be}}^2 \tan\theta\right) + 4R^2 \tan\theta\left({Z_L}^2 X_{Be}\tan\theta - {Z_L}^2 - {X_{Be}}^2\right) = 0 \tag{5.38}$$

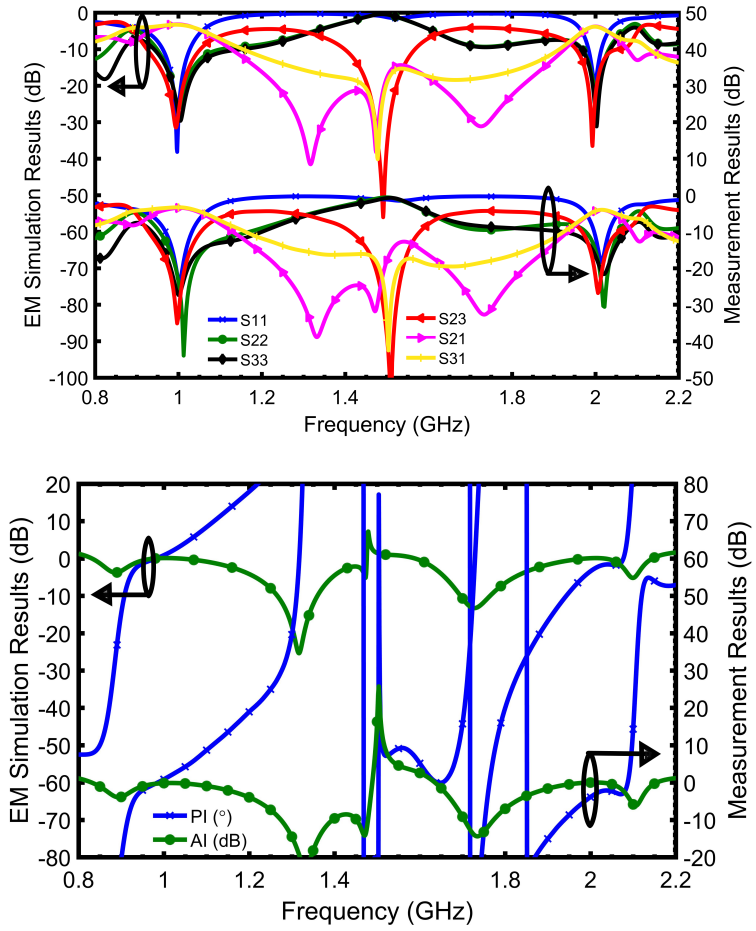


Figure 5.29: S-parameters (top), Amplitude Imbalance (AI) and Phase Imbalance (PI) (bottom) results of the fabricated prototype.

5.6.2 Fabrication and Measurement

A prototype working at 1 and 2 GHz is designed on Rogers RO5880 to validate the presented concept. The source (load) impedance is taken as 50 Ω so that they gel with the impedances of the SMA connectors and discard the need of an additional impedance transformer. The design equations are used to determine the design parameters as (units: Ω) $Z_1 = 30$, $Z_{e1} = 90$, $Z_{o1} = 62.1$, $Z_2 = 118.7$, $Z_{e2} = 58.4$, $Z_{o2} = 41.3$, $Z_3 = 74.5$, $Z_{e3} = 57.5$, $Z_{o3} = 52.9$, and $R = 55.4$. Electrical lengths of all the TL are chosen as 60° for the dual-band operation. The EM simulations are carried out in CAD tool and the design parameters are optimized for the TL discontinuities and substrate losses. The prototype with the optimized parameters is shown in Fig. 5.28 with dimensions as (units: mm) $W_1 = 185$, $L_1 = 1227.4$, $W_2 = 45$, $L_2 = 1276.7$, $W_3 = 190$, $S_3 = 40$, $L_3 = 1076.7$, $W_4 = 91.7$, $L_4 = 739.8$, $W_5 = 350$, $L_5 = 960.1$, $W_6 = 95$,

Table 5.6: Design Parameters for various cases of ITR

ITR $(Z_L/Z_S) = 20/50$				**ITR** $(Z_L/Z_S) = 200/50$			
Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
Z_1	40	Z_2	105	Z_1	29.1	Z_2	149.8
Z_{e1}	120	Z_3	35.7	Z_{e1}	87.3	Z_3	89
Z_{o1}	87.6	Z_{e3}	22.2	Z_{o1}	79	Z_{e3}	117
Z_{e2}	75.2	Z_{o3}	20.2	Z_{e2}	47.5	Z_{e3}	112
Z_{o2}	57.6	R	14.5	Z_{o2}	29	R	377.7

$L_6 = 861.2$, $S_6 = 30$, $W_7 = 140$, $S_7 = 185$, $L_7 = 992.1$, $W_8 = 185$, $L_8 = 1208.1$, and $R = 56.2$. The EM simulation results and the measurement results are shown combinely in Fig. 5.29. The EM results confirm equal power distribution and matching at all the ports along with good isolation for a broad range of frequencies at both the chosen bands. The measured response for the amplitude (phase) imbalance is 0.1 dB (0.8°) at 1.0 GHz and 0.0 dB (-3.6°) at 2.0 GHz, the matching response S_{11},S_{22}, and S_{33} is -23.4 dB (-18.9 dB), -44 dB (-30.6 dB), -27.8 dB (-22.2 dB) respectively at 1.0 GHz (2.0 GHz). The insertion losses S_{21} and S_{31} are better than -3.4 dB (-4.5 dB) at the operating frequency of 1.0 GHz (2.0 GHz). Extremely good isolation of -35.1 dB (-26.8 dB) at 1.0 GHz (2.0 GHz) is also achieved in the proposed DBB.

Moreover, the 10 dB bandwidth for S_{11} (S_{22}, S_{33} and S_{23}) at 1 GHz is 0.969 - 1.034 GHz (0.95 - 1.17 GHz, 0.94 - 1.20 GHz, and 0.927 - 1.06 GHz) and at 2 GHz is 1.99 - 2.04 GHz (1.97 - 2.06 GHz, 1.94 - 2.08 GHz, and 1.96 - 2.06 GHz). The amplitude (phase) imbalance of 1 dB (5°) is also achieved for a bandwidth of 0.95 - 1.1 GHz (0.929-1.06 GHz) at 1 GHz and of 1.92-2.06 (1.98 - 2.10 GHz) at 2 GHz. These results apparently match very well with the simulation results and thereby validate the design concept.

5.6.3 Application for Impedance Transformation

An added feature of the proposed DBB is its potential to operate at wide range of distinct load and source impedances. For example, the design parameters (units: Ω) of the DBB for two design cases of maximum achievable ITR of 0.4 and 4.0 are given in Table 5.6. Electrical lengths of the TL are again 60° for its dual-band operation at 1/2 GHz. The simulation results, in Fig. 5.30, for these cases also demonstrate the effectiveness of the proposed technique. The two figures on the top demonstrate the performance of the balun for ITR 0.4. One figure, on the left,

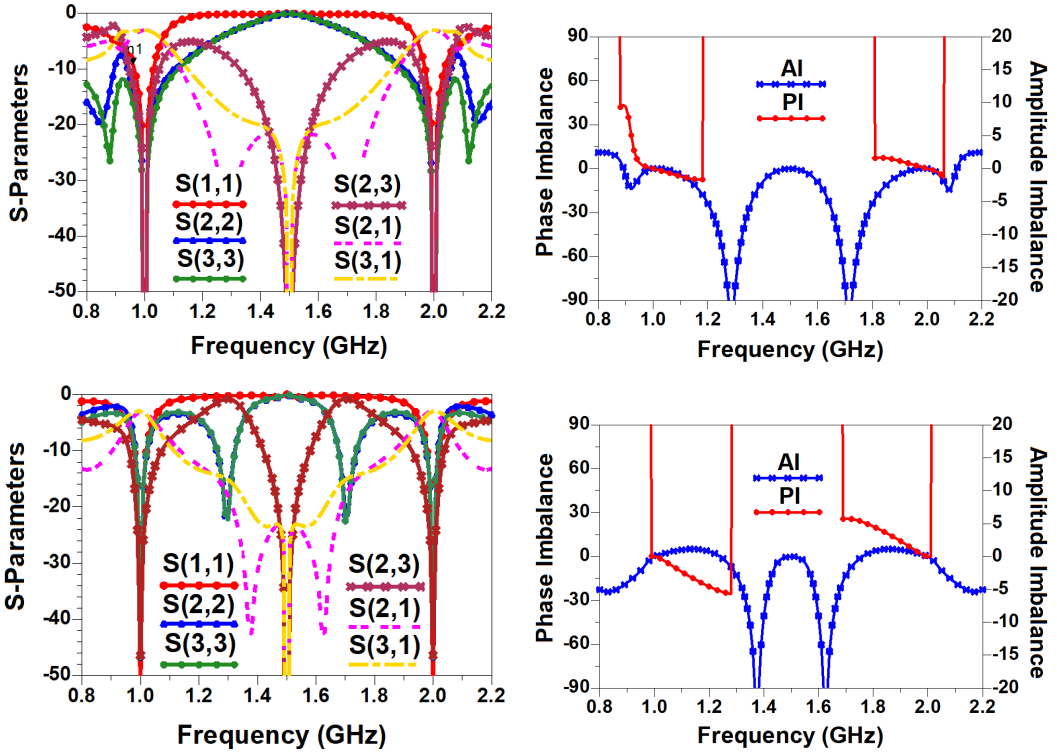


Figure 5.30: Simulation Results of the design for ITR as 0.4:1 (top two) and ITR as 4.0:1 (bottom two)

demonstrates the return loss at all the three ports, i.e., S_{11}, S_{22}, and S_{33}, isolation between the two output ports S_{23}, and the insertion loss for the two output ports, i.e., S_{21}, and S_{31}. Another figure, on the right, demonstrates the amplitude difference between the two output ports, i.e., amplitude imbalance (AI) and the deviation in the phase from the required phase difference of 180° between the two output ports, i.e., phase imbalance (PI). Similarly, the bottom two figures of Fig. 5.30 demonstrate all the performance parameters for ITR 4.0. These results, therefore, confirm the capability of the design to provide inherent impedance transformation integrated with the operation of a balun for a wide range of impedance transformation ratios.

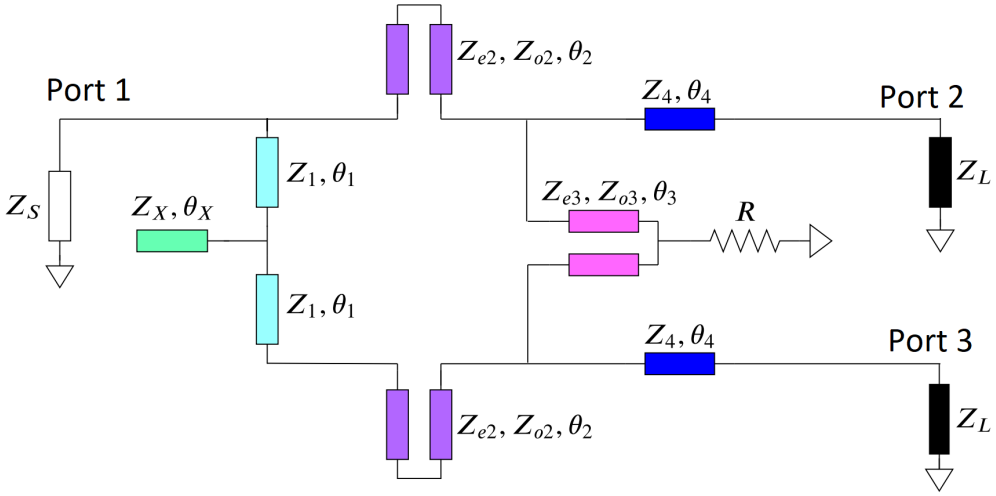


Figure 5.31: The proposed impedance transforming balun.

5.7 Dual-Band Baluns For Concurrent High Impedance Transformation and High Frequency Ratios

5.7.1 Architecture 1

Fig. 5.31 shows the architecture of the proposed impedance transforming dual-band balun. The respective characteristic impedances and electrical lengths of the transmission lines and the coupled lines are also depicted. The source at port 1 (an input port) of the balun has an impedance of Z_S and the load at ports 2 and 3 (output ports) of the balun has an impedance of Z_L. Since the proposed circuit is symmetric, the even-odd mode analysis is used to derive the analytical expressions for the design variables. The balun operation is achieved by satisfying the following expressions (5.39) and (5.40) [97]:

$$T_{even} = 0 \tag{5.39}$$

$$Z_{odd} = 2Z_s \tag{5.40}$$

$$Z_{even} = 0 \tag{5.41}$$

Equation (5.39) states that the input signal must not flow in the even-mode. This can be achieved by forcing a virtual ground at the source using (5.41).

5.7.1.1 Mathematical Design Analysis

1. **Odd-mode analysis:**

The odd-mode decomposition of the proposed balun is demonstrated in Fig. 5.32 and obtained by shorting the nodes at symmetry line. The coupled line (Z_{e3}, Z_{o3}, and θ_3) is reduced to a transmission line (TL) with its odd-mode equivalent characteristic impedance Z_{o3}. However, the electrical length remains unchanged as θ_3. The terms Y_m and Y_n denote the respective admittances and are expressed in (5.42).

$$Y_m = \frac{Z_S C_1 + D_1}{Z_S A_1 + B_1} \quad , \quad Y_n = \frac{Z_L C_2 + D_2}{Z_L A_2 + B_2} \tag{5.42}$$

here,

$$\begin{aligned} \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix}_{Y_m} &= \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} 1 & 0 \\ -\frac{j}{Z_1} Cot\theta_1 & 1 \end{bmatrix} \\ &= \begin{bmatrix} A - j\frac{B}{Z_1} Cot\theta_1 & B \\ C - j\frac{D}{Z_1} Cot\theta_1 & D \end{bmatrix} \end{aligned} \tag{5.43}$$

$$\begin{aligned} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix}_{Y_n} &= \begin{bmatrix} 1 & 0 \\ -\frac{j}{Z_3} Cot\theta_3 & 1 \end{bmatrix} \begin{bmatrix} Cos\theta_4 & jZ_4 Sin\theta_4 \\ -\frac{j}{Z_3} Sin\theta_4 & Cos\theta_4 \end{bmatrix} \\ &= \begin{bmatrix} Cos\theta & jZ_4 Sin\theta_4 \\ -\frac{j}{Z_3} Cos\theta_4 Cot\theta_3 + \frac{j}{Z_4} Sin\theta_4 & \frac{Z_4}{Z_3} Sin\theta Cot\theta_3 + Cos\theta \end{bmatrix} \end{aligned} \tag{5.44}$$

and

$$A = D = \frac{Z_{e2} Cot\theta_2 - Z_{o2} Tan\theta_2}{Z_{e2} Cot\theta_2 + Z_{o2} Tan\theta_2} \tag{5.45}$$

$$B = \frac{2jZ_{e2}Z_{o2}}{Z_{e2} Cot\theta_2 + Z_{o2} Tan\theta_2} \tag{5.46}$$

$$C = \frac{2j}{Z_{e2} Cot\theta_2 + Z_{o2} Tan\theta_2} \tag{5.47}$$

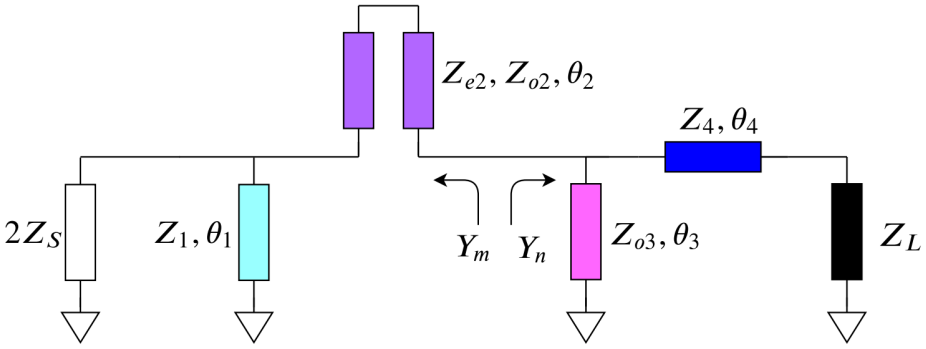


Figure 5.32: Odd-mode equivalent circuit of the proposed balun.

For the dual-band operation, the electrical lengths must follow the expression:

$$\theta_i = \frac{(1+n)\pi}{1+r} \; ; \;\; i \in [1,2,3,4], n \in I \tag{5.48}$$

To ensure the impedance matching of the odd-mode equivalent circuit, the following equations must be true:

$$Re[Y_m] = Re[Y_n] \tag{5.49}$$

$$Im[Y_m] = -Im[Y_n] \tag{5.50}$$

The expressions of the real and imaginary parts of Y_m and Y_n are provided in Eqs. (5.51)-(5.54).

$$Re[Y_m] = \frac{KD - Z_S(C - jDCot\theta_1/Z_1)B}{K^2 - B^2} \tag{5.51}$$

$$Im[Y_m] = -j\frac{Z_S K(C - jDCot\theta_1/Z_1) - BD)}{K^2 - B^2} \tag{5.52}$$

$$Re[Y_n] = \frac{Z_L Tan^2\theta_3(1 + Tan^2\theta_4)}{(Z_L Tan\theta_3)^2 + (Z_4 Tan\theta_3 Tan\theta_4)^2} \tag{5.53}$$

$$Im[Y_n] = -\frac{Tan\theta_3(\frac{Z_4^2}{Z_3} + \frac{Z_L^2}{Z_3 Tan^2\theta_4} - \frac{(Z_L^2 - Z_4^2)Tan\theta_3}{Z_4 Tan\theta_4})}{Z_L^2 + Z_4^2 Tan^2\theta_3} \tag{5.54}$$

here,

$$K = Z_S(A - jBCot\theta_1/Z_1) \tag{5.55}$$

The Eqs. (5.49)-(5.50) are solved substituting Eqs. (5.51)-(5.54) to deduce the design parameters Z_4 and Z_{o3} of the proposed balun. The expressions of Z_4 and Z_{o3} are derived and represented as in Eqs. (5.56)-(5.57). Here, Z_1 is an independent variable. It should also be noted that $\theta_2 = \theta_4 = \theta$ is considered here for the simplification of the expressions.

$$Z_4 = \frac{1}{W_1}\sqrt{Z_L Z_s(2Z_1^2 Z_{o2}^2 Z_s^2 + Cot\theta(Z_1^2 Cot\theta W_2 + W_3))} \tag{5.56}$$

$$Z_{o3} = -\frac{Cot\theta_3(Z_L^2 + Z_4^2 Tan^2\theta)}{Z_4 Tan\theta - Z_L^2 Tan\theta/Z_4 + X} \tag{5.57}$$

where variables W_1, W_2, W_3 and X are expressed as:

$$W_1 = Z_1 Z_S(Z_{o2} + Z_{e2}Cot^2\theta) \tag{5.58}$$

$$\begin{aligned} W_2 = Z_{o2}(2Z_{e2}^2 Z_{o2} - 4Z_{e2}Z_s^2 + Z_{o2}Z_s(2Z_s - Z_L)) + \\ Z_{e2}(-2Z_{o2}Z_s(2Z_s + Z_L) + Z_{e2}(2Z_{o2}^2 + Z_L Z_s))Cot^2\theta \end{aligned} \tag{5.59}$$

$$\begin{aligned} W_3 = Z_{e2}Z_s(-Z_1^2 Z_{e2}(Z_L - 2Z_S)Cot^3\theta \\ - 8Z_1 Z_{o2}Z_s(Z_{o2} - Z_{e2}Cot^2\theta)Cot\theta_1 \\ + 8Z_{e2}Z_{o2}^2 Z_s Cot\theta Cot^2\theta_1)Csc^2\theta \end{aligned} \tag{5.60}$$

$$\begin{aligned} X = (Z_L^2 + Z_4^2 Tan^2\theta)(2Z_1^2 Z_{e2}Z_{o2}M - \\ 2Z_s N(2Z_1 - MCot\theta_1)/(4Z_1^2 Z_{e2}^2 Z_{o2}^2 + N^2) \end{aligned} \tag{5.61}$$

M and N in Eqs. (5.58)-(5.61) are given by:

$$M = Z_{e2}Cot\theta - Z_{o2}Tan\theta \tag{5.62}$$

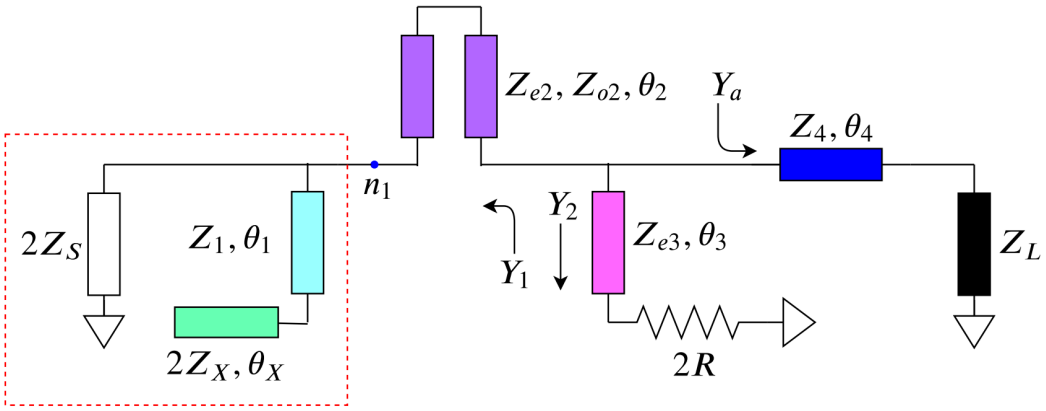


Figure 5.33: Even-mode equivalent circuit of the proposed balun.

$$N = 2Z_s(Z_1 Z_{e2} Cot\theta + 2Z_{e2} Z_{o2} Cot\theta_1 - Z_1 Z_{o2} Tan\theta) \tag{5.63}$$

2. **Even-mode analysis:**

Unlike the odd-mode equivalent circuit, the even-mode equivalent circuit of the proposed balun is obtained by open-circuiting the nodes at the symmetry line and depicted in Fig. 5.33. The coupled line (Z_{e3}, Z_{o3}, and θ_3) is reduced to a TL with its even mode equivalent characteristic impedance Z_{e3}. The respective input admittances are also shown by Y_1, Y_2, and Y_a. According to the condition (5.41), the input impedance is virtually shorted so that the node n_1 is shorted to the ground. Subsequently, the combination of stubs with impedance Z_1 and $2Z_X$ are shorted to ground which results in Z_X as in (5.64). The term Z_1 is known from the odd-mode analysis.

$$Z_X = \frac{1}{2} Z_1 Tan\theta_1 Tan\theta_X \tag{5.64}$$

The admittances Y_1, Y_2, and Y_a are as follows:

$$Y_1 = \frac{Z_{e2} Cot\theta_2 - Z_{o2} Tan\theta_2}{2jZ_{e2} Z_{o2}} \tag{5.65}$$

$$Y_2 = \frac{Z_{e3} + 2jRTan\theta_3}{Z_{e3}(2R + jZ_{e3} Tan\theta_3)} \tag{5.66}$$

$$Y_a = \frac{Z_4 + jZ_L Tan\theta_4}{Z_4(Z_L + jZ_4 Tan\theta_4)} \tag{5.67}$$

Table 5.7: Design parameters of the proposed balun for two design examples with extreme design specifications

Case	r	k	$Z_1(\Omega)$ θ_1°	Z_{e2} (Ω), Z_{o2} (Ω) θ_2°	Z_{e3} (Ω), Z_{o3} (Ω) θ_3°	Z_4 (Ω) θ_4°	Z_X (Ω) θ_X°	Z_S (Ω)	Z_L (Ω)
1	5	10	95, $2\pi/6$	100, 60, $2\pi/6$	37.7, 21.7, $\pi/6$	36.8, $2\pi/6$	142.5, $2\pi/6$	500	50
2	5	6	120, $\pi/6$	100, 60, $2\pi/6$	91.79, 73.51, $2\pi/6$	143.92, $2\pi/6$	20, $\pi/6$	25	150

Again, to obtain the impedance matching, the following conditions must be satisfied.

$$Re[Y_2] = Re[Y_1 + Y_a] \tag{5.68}$$

$$Im[Y_2] = -Im[Y_1 + Y_a] \tag{5.69}$$

where the real and imaginary components of Y_2 and $Y_1 + Y_a$ ($Y_1 + Y_a = Y_b$) are as follows:

$$Re[Y_2] = \frac{2R}{(4R^2 - Z_{e3}^2)Cos^2\theta_3 + Z_{e3}^2} \tag{5.70}$$

$$Im[Y_2] = \frac{(-Z_{e3}^2 + 4R^2)Tan\theta_3}{Z_{e3}(4R^2 + Z_{e3}^2 Tan^2\theta_3)} \tag{5.71}$$

$$Re[Y_b] = \frac{Z_L}{(Z_L^2 - Z_4^2)Cos^2\theta_4 + Z_4^2} \tag{5.72}$$

$$Im[Y_b] = \frac{(-Z_4^2 + Z_L^2)Tan\theta_4}{Z_4(Z_L^2 + Z_4^2 Tan^2\theta_4)} - \frac{Z_{e2}Cot\theta_2 - Z_{o2}Tan\theta_2}{2Z_{e2}Z_{o2}} \tag{5.73}$$

The solution of the Eqs. (5.68) and (5.69) using Eqs. (5.70) - (5.73), provides the expressions for the unknown design variables Z_{e3} and R in Eqs. (5.74) and (5.75), respectively. The terms $Re[Y_b]$ and $Im[Y_b]$ are known due to the design parameters calculated in the odd-mode analysis and denoted as G_b and B_b, respectively.

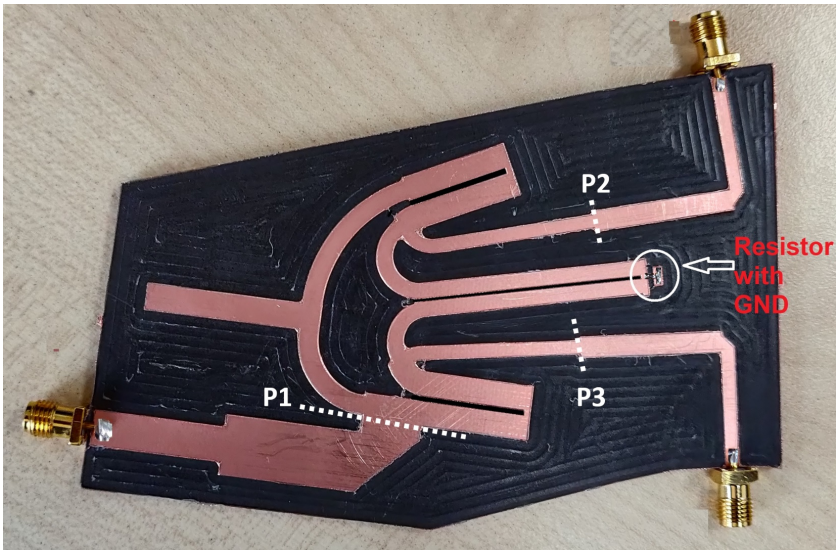


Figure 5.34: Fabricated prototype of the proposed balun. Size:0.086 λ_g^2.

$$Z_{e3} = \frac{B_b Cos2\theta_3 + \sqrt{B_b^2 + G_b^2 Sin^2 2\theta_3}}{(B_b^2 + G_b^2) Sin2\theta_3} \tag{5.74}$$

$$R = \frac{4G_b^2 + B_b(2B_b - \sqrt{2}\sqrt{2B_b^2 + G_b^2 - G_b^2 Cos4\theta_3})}{8G_b(B_b^2 + G_b^2)Cos^2\theta_3} \tag{5.75}$$

5.7.1.2 Circuit Fabrication

A design example with design specifications as source impedance 25 Ω and load impedance 75 Ω working at 1 GHz and 2.6 GHz is fabricated to verify the operation of the proposed balun. The design parameters for the provided specification are calculated using the design analysis in previous section and are as follows: Z_X = 21.3 Ω, Z_1 = 30 Ω, Z_{e2} = 40 Ω, Z_{o2} = 30 Ω, Z_{e3} = 65.4 Ω, Z_{o3} = 37.9 Ω, Z_4 = 68.6 Ω, $\theta_X = \theta_1 = \theta_2 = \theta_3 = \theta_4 = 50°$, and R = 28.1 Ω. In addition, the design parameters of the two design examples with extreme specifications, i.e., r & k = 5 & 10 and r & k = 5 & 6 are also calculated and listed in Table 5.7. These examples demonstrate that the proposed balun is realizable at very high r and k. Case 1 also demonstrates the operation at concurrent high k and r which is very rare in the literature. The fabrication of the prototype is done on RT/duroid 5880 substrate with the dielectric constant of 2.2, and loss-tangent of 0.0009. The substrate has a thickness of 1.575 mm and the copper cladding of

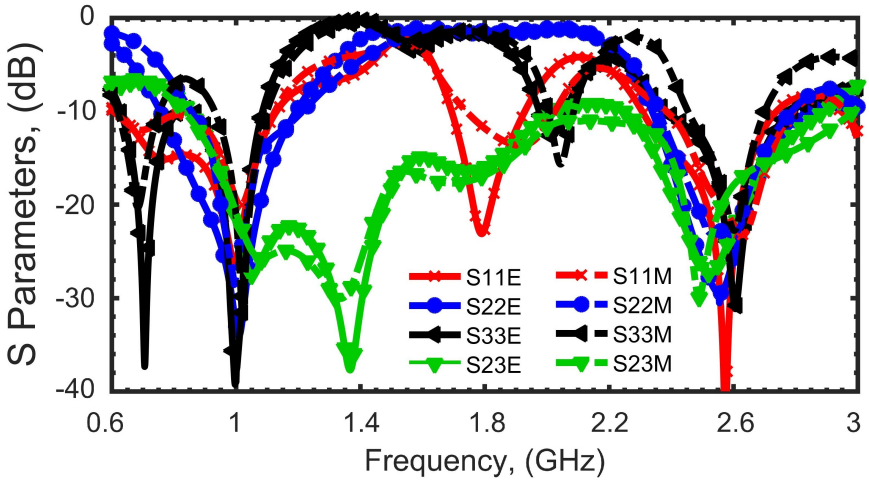


Figure 5.35: All ports matching and isolation between the balanced output ports

35 μm on both the sides of the substrate. The fabricated prototype has an overall dimension of 50 mm $\times$ 73 mm (0.086 λ_g^2) and is shown in Fig. 5.34. The unbalanced port (P1) and balanced ports (P2 and P3) are indicated with a dashed-line on the fabricated prototype. All the ports are extended with an impedance transformer to transform the port impedances to 50 Ω for the measurement environment. However, these impedance transformers would not be needed in a communication system for the required arbitrary impedance terminations. The isolation resistor CRCW040228R0FKED is shorted to ground by soldering. Some optimizations are also performed to compensate the effects of the curves and junctions in the design of the prototype.

5.7.1.3 Measurement Results

The prototype is then evaluated and the measurement results along with the EM simulation results are compared and plotted in Figs. 5.35 and 5.36. The letter 'E' is suffixed for EM simulation results whereas letter 'M' is suffixed for the measurement results. Fig. 5.35 depicts the all ports matching and isolation between the balanced ports of the balun. The isolation along with the matching at the output ports of the balun is better than -20 dB at both the operating frequencies. The overall operating 10 dB bandwidth, considering all ports matching and isolation of the balun, is 170 MHz (0.93 GHz - 1.1 GHz) at 1 GHz and 250 MHz (2.45 GHz - 2.7 GHz) at 2.6 GHz. The insertion losses and phase difference between the two output ports of the balun are also depicted in Fig. 5.36. The insertion loss through port 2 (port 3) is

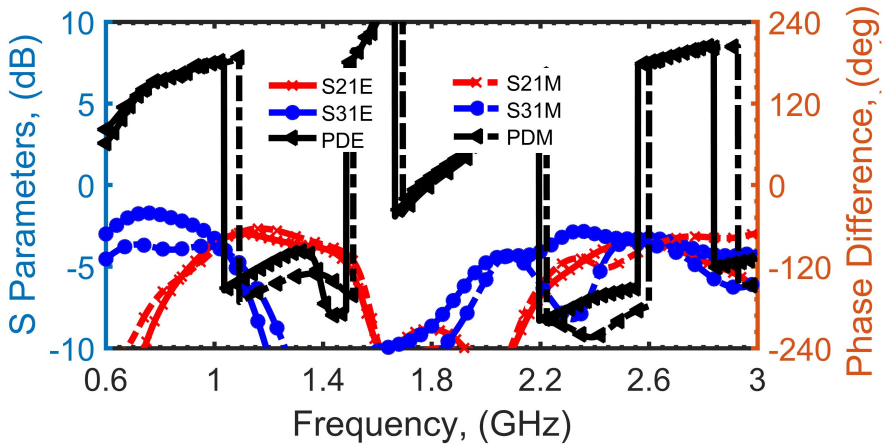


Figure 5.36: Insertion losses and phase difference between the balanced ports

-3.9 dB (-3.8 dB) at 1 GHz and -3.8 dB (-3.6 dB) at 2 GHz. It should be noted here that the measured insertion loss includes the effect of redundant impedance transformers at all the ports. The measured phase difference is 178.8° at 1 GHz and 179.3° at 2.6 GHz. The measurement results are are in good agreement with the EM simulation results and therefore validates the proposed design and methodology.

The capabilities of the proposed architecture are also compared in Table 5.8 with the recently published baluns. The wideband isolation is better than -15.8 dB for the working bandwidth of the proposed balun which is evident from the measured results in Fig. 5.35. The balun provides maximum frequency ratio of 5 and the maximum impedance ratio of 10 which is much higher than other recently reported baluns. And, therefore, the proposed balun advances the state-of-the-art with its design flexibility for a wide range of design specifications.

5.7.2 Architecture 2

The proposed dual-band balun shown in Fig. 5.37 has the source (input port) and the load (output ports) impedances of Z_S Ω and Z_L Ω respectively. Here, all the electrical lengths are denoted by θ_i where i=x,1,2,3. Apparently the balun is symmetric around AA' axis (blue dotted line) in Fig. 5.37 and, therefore, can be analyzed using its equivalent odd- and even-mode circuits shown in Figs. 5.38 and 5.39, respectively.

Table 5.8: Specifications comparison with the earlier reported baluns

Ref.	Frequency ratio, r	k (=Z_L/Z_S)	Isolation
[61]	r=2	0.4<k<5	S23<-12.3 dB (measured)
[170]	1<r<4.37	0.25<k<2.5	No such function
[99]	2.32<r<6.01 2.44<r<7.31	80/120 (k=0.67) 100/130 (k=0.77)	S23<-16 dB (measured)
[41]	2.58<r<4.61 2.75<r<4.22 2.91<r<3.87	50/50 (k=1) 75/50 (k=1.5) 100/50 (k=2)	S23<-10 dB (measured)
[136]	r=2.17	150/50 (k=3) 1<k<6	S23<-26 dB (measured)
This work	1.6<r<5.0 r=2 r=4	1<k<7 k=8,9,10 k=9	S23<-15.8 dB (measured)

5.7.2.1 Design Analysis

The balun operates successfully if the conditions in (5.76) are met [97]. Moreover, the network consisting of a stub of electrical length θ_4 loaded with a resistor R is used to achieve isolation between the output ports. In addition, electrical lengths for dual-band designs are regulated by expression (5.77) [171]. Here, the term Z_{odd} is the odd-mode impedance at the input port, T_{even} is the transmission coefficient of signal in the even-mode, $r = f_2/f_1 \geq 1$, and $n \in I$.

$$Z_{odd} = 2Z_S \quad \text{and} \quad T_{even} = 0 \tag{5.76}$$

$$\theta = \frac{(1+n)\pi}{1+r} \tag{5.77}$$

5.7.2.2 Odd-Mode Analysis

In the odd-mode equivalent circuit, Fig. 5.38, the transmission lines (TLs) with electrical length θ_1 and θ_3 are shorted to ground. Terms Y_{ino3} and Y_{ino2} in (5.78) and (5.79) can be deduced respectively. The subsequent expressions represent the terms in these expressions. It is important to note that all the electrical lengths are assumed equal, i.e, $\theta_1 = \theta_2 = \theta_3 = \theta$, for simplifications of these expressions.

$$Y_{ino3} = \frac{1}{Z_L} + \frac{1}{jZ_{o3}\tan\theta_3} \tag{5.78}$$

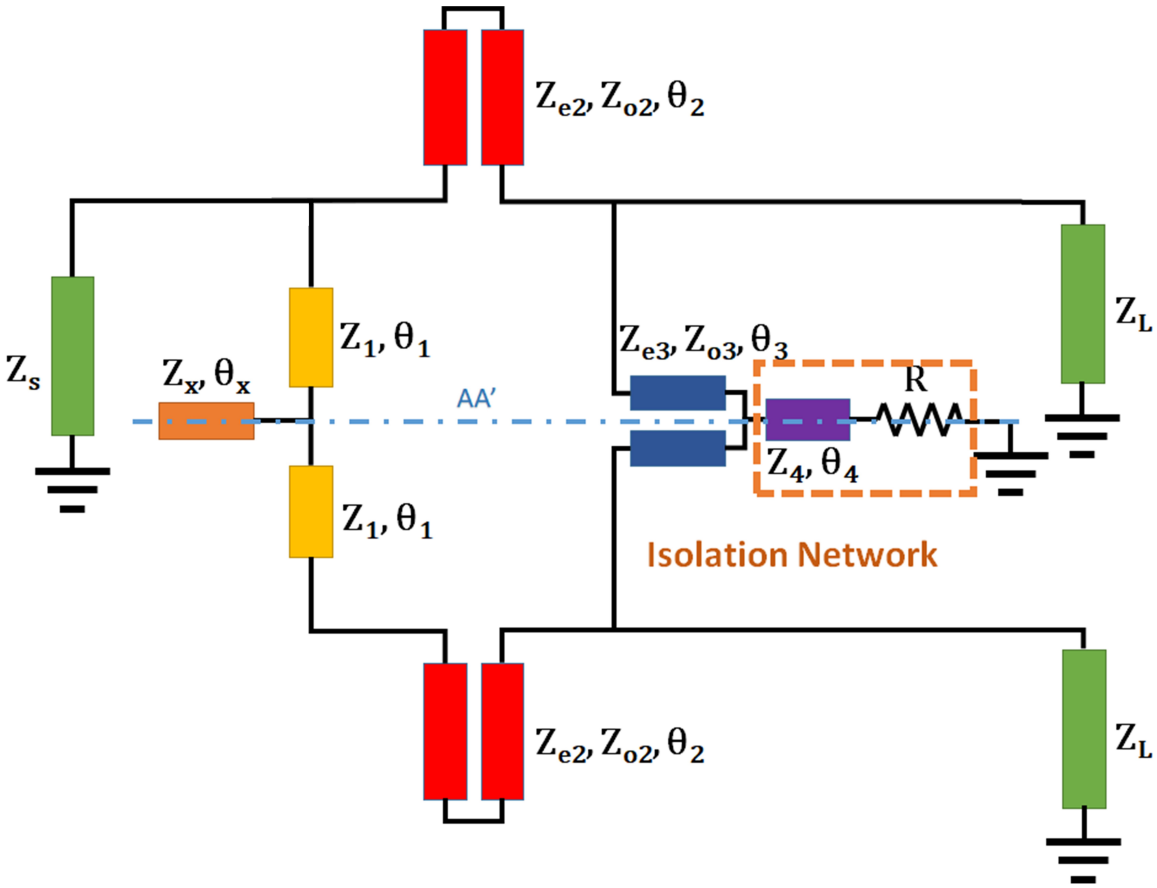


Figure 5.37: Proposed dual-band balun architecture

$$Y_{ino2} = G_{ino2} + jB_{ino2} \tag{5.79}$$

$$G_{ino2} = \frac{Z_L Z_{o3}^2 \left(Z_{o2}\tan^2\theta + Z_{e2}\right)^2}{4Z_L^2 \tan^2\theta\,(A)} \tag{5.80}$$

$$B_{ino2} = \frac{(B-C)}{(D+E)} \tag{5.81}$$

$$A = \frac{Z_{e2}^2 Z_{o2}^2 + Z_{e2}^2 Z_{o2} Z_{o3}}{\tan^2\theta} + \frac{Z_{e2}^2 Z_{o3}^2}{4\tan^2\theta} - Z_{o2}^2 Z_{e2} Z_{o3} - \frac{Z_{o3}^2 Z_{e2} Z_{o2}}{2} + \frac{4Z_{o3}^2 Z_{e2}^2 Z_{o2}^2}{Z_L^2} + \frac{Z_{o2}^2 Z_{o3}^2 \tan^2\theta}{4} \tag{5.82}$$

$$B = \left(Z_{o2}\tan^2\theta - Z_{e2} + 2Z_{o3}\tan^2\theta\right) \frac{\left(2Z_{e2}Z_{o2} + Z_{e2}Z_{o3} - Z_{o2}Z_{o3}\tan^2\theta\right)}{Z_{o3}^2 \tan\theta \left(Z_{o2}\tan^2\theta + Z_{e2}\right)^2} \tag{5.83}$$

$$C = \frac{2Z_{e2}Z_{o2}\tan\theta\left(Z_{e2} - Z_{o2}\tan^2\theta\right)}{Z_L^2 \left(Z_{o2}\tan^2\theta + Z_{e2}\right)^2} \tag{5.84}$$

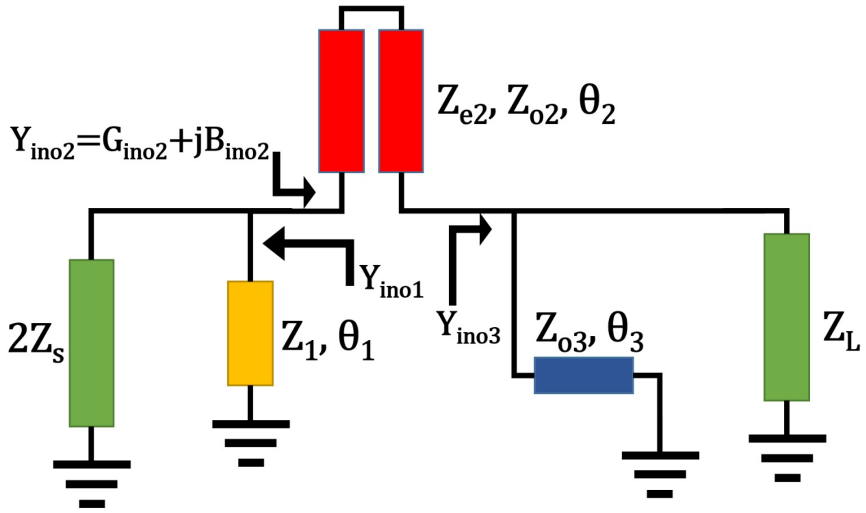


Figure 5.38: Odd-mode equivalent circuit of the proposed balun

$$D = \frac{\left(2Z_{e2}Z_{o2} + Z_{e2}Z_{o3} - Z_{o2}Z_{o3}\tan^2\theta\right)^2}{Z_{o3}^2\left(Z_{o2}\tan^2\theta + Z_{e2}\right)^2} \tag{5.85}$$

$$E = \frac{4Z_{e2}^2Z_{o2}^2\tan^2\theta}{Z_L^2\left(Z_{o2}\tan^2\theta + Z_{e2}\right)^2} \tag{5.86}$$

The real and imaginary parts of Y_{ino2} are equated with $1/2Z_S$ and negative of Y_{ino1} to satisfy (5.76) respectively to get the design parameters Z_{o3} and Z_1, expressed in (5.87), for given values of Z_{e2} and Z_{o2}. The terms Z_{e2} and Z_{o2} are independent variables here and can be chosen in the range of [20-160] Ω for the realizable Z_{o3} and Z_1.

$$Z_{o3} = \frac{2Z_LZ_{e2}Z_{o2}\,(F)}{G} \qquad Z_1 = \frac{H+I}{J-K} \tag{5.87}$$

Where,

$$F = \sqrt{2}\sqrt{Z_SZ_LZ_{o2}^2 - \frac{2Z_{e2}^2Z_{o2}^2}{\tan^2\theta} + \frac{Z_SZ_LZ_{e2}^2}{\tan^4\theta} + \frac{2Z_SZ_LZ_{e2}Z_{o2}}{\tan^2\theta}} \pm \left(\frac{Z_LZ_{e2}}{\tan^2\theta} - Z_LZ_{o2}\right) \tag{5.88}$$

$$G = -\frac{Z_L^2Z_{e2}^2}{\tan^2\theta} + 2Z_L^2Z_{e2}Z_{o2} - Z_L^2Z_{o2}^2\tan^2\theta + \frac{2Z_SZ_LZ_{e2}^2}{\tan^2\theta} + 4Z_SZ_LZ_{e2}Z_{o2} + 2Z_SZ_LZ_{o2}^2\tan^2\theta - 4Z_{e2}^2Z_{o2}^2 \tag{5.89}$$

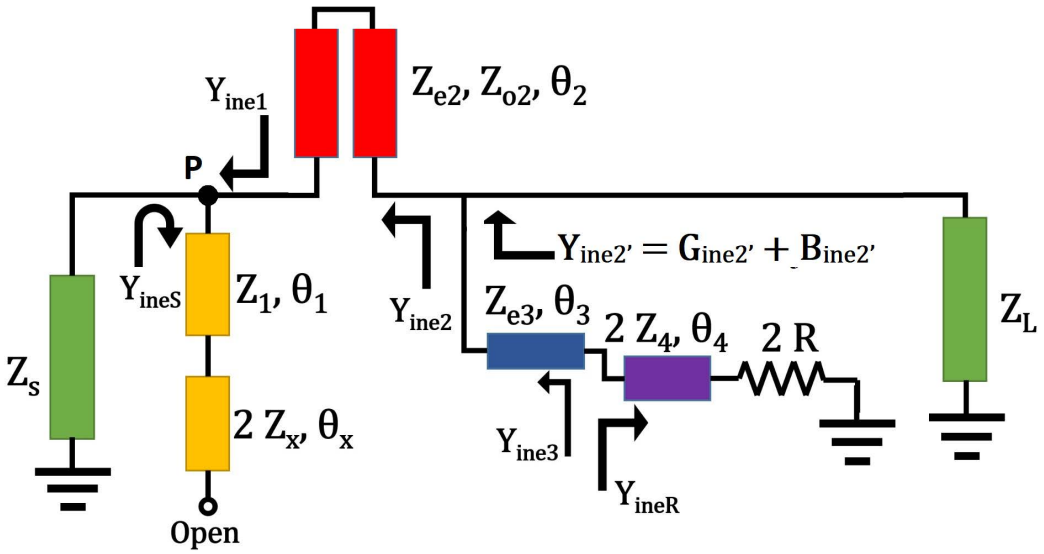


Figure 5.39: Even-mode equivalent circuit of the proposed balun

$$H = \frac{\left(2Z_{e2}Z_{o2} + Z_{e2}Z_{o3} - Z_{o2}Z_{o3}\tan^2\theta\right)^2}{Z_{o3}^2\left(Z_{o2}\tan^2\theta + Z_{e2}\right)^2} \tag{5.90}$$

$$I = \frac{4Z_{e2}^2Z_{o2}^2\tan^2\theta}{Z_L^2\left(Z_{o2}\tan^2\theta + Z_{e2}\right)^2} \tag{5.91}$$

$$J = \left(Z_{o2}\tan^2\theta - Z_{e2} + 2Z_{o3}\tan^2\theta\right)\frac{\left(2Z_{e2}Z_{o2} + Z_{e2}Z_{o3} - Z_{o2}Z_{o3}\tan^2\theta\right)}{Z_{o3}^2\left(Z_{o2}\tan^2\theta + Z_{e2}\right)^2} \tag{5.92}$$

$$K = \frac{2Z_{e2}Z_{o2}\tan^2\theta\left(Z_{e2} - Z_{o2}\tan^2\theta\right)}{Z_L^2\left(Z_{o2}\tan^2\theta + Z_{e2}\right)^2} \tag{5.93}$$

5.7.2.3 Even-Mode Analysis

The notations in even-mode equivalent circuit in Fig. 5.39 carry standard meaning. Here, condition in (5.76) can be satisfied by creating a virtual ground at the node P in Fig. 5.39, and this leads to $Y_{ine1} = Y_{ineS} = \infty$ for $\theta_1 = \theta_X = \theta$. $Y_{ineS} = \infty$ results in Z_X expressed in (5.94). Furthermore, the matching at the output ports can be achieved by enforcing $Y_{ineR} = Y_{ine3}{}^*$ [37] which can be solved to obtain Z_4 and R, given in (5.95) and (5.99), as functions of Z_{e2}, Z_{o2}, Z_{e3}, and θ. The independent design variable Z_{e3} in (5.104) can be calculated for the realizable coupling factor (ρ) while all the electrical lengths are assumed equal, i.e, $\theta_1 = \theta_2 = \theta_3 = \theta_4 = \theta$.

$$Z_X = \frac{1}{2}\left(Z_1 \tan^2\theta\right) \tag{5.94}$$

$$Z_4 = -\frac{\begin{array}{r}2B_{ine2'}Z_{e3}^2 + Z_{e3}^3 \sin 4\theta - \sqrt{2}Z_{e3} * \sqrt{(a)\cos 4\theta + (b)\sin 4\theta + c} + 2B_{ine2'}Z_{e3}^2 \cos 4\theta \\ - B_{ine2'}^2 Z_{e3} \sin 4\theta - G_{ine2'}^2 Z_{e3} \sin 4\theta\end{array}}{\begin{array}{r}4(B_{ine2'}^2 + G_{ine2'}^2 + Z_{e3}^2) * \sin 2\theta - 4B_{ine2'}Z_{e3} + 2(Z_{e3}^2 - B_{ine2'}^2 - G_{ine2'}^2)\sin 4\theta \\ + 4B_{ine2'}Z_{e3}\cos 4\theta\end{array}} \tag{5.95}$$

$$a = -G_{ine2'}^4 - Z_{e3}^4 - B_{ine2'}^4 + 6B_{ine2'}^2 Z_{e3}^2 - 2G_{ine2'}^2 Z_{e3}^2 - 2B_{ine2'}^2 G_{ine2'}^2 \tag{5.96}$$

$$b = 4B_{ine2'}Z_{e3}^3 - 4B_{ine2'}^3 Z_{e3} - 4B_{ine2'}G_{ine2'}^2 Z_{e3} \tag{5.97}$$

$$c = B_{ine2'}^4 + G_{ine2'}^4 + 2B_{ine2'}^2 G_{ine2'}^2 + Z_{e3}^4 + 2B_{ine2'}^2 Z_{e3}^2 + 2G_{ine2'}^2 Z_{e3}^2 \tag{5.98}$$

$$R = Z_4\sqrt{\frac{d}{e(\tan\theta)}} \tag{5.99}$$

$$\begin{aligned} d = -B_{ine2'}^2 Z_{e3} + 2Z_4 B_{ine2'}^2 \tan^2\theta - B_{ine2'}Z_{e3}^2 \tan\theta + \frac{B_{ine2'}Z_{e3}^2}{\tan\theta} - 4Z_4 B_{ine2'}Z_{e3}\tan\theta - G_{ine2'}^2 Z_{e3} \\ + 2Z_4 G_{ine2'}^2 \tan^2\theta + Z_{e3}^3 + 2Z_4 Z_{e3}^2 \end{aligned} \tag{5.100}$$

$$\begin{aligned} e = B_{ine2'}^2 Z_{e3}\tan\theta + 2Z_4 B_{ine2'}^2 \tan\theta + B_{ine2'}Z_{e3}^2 \tan^2\theta - B_{ine2'}Z_{e3}^2 - 4Z_4 Z_{e3} B_{ine2'} + Z_{e3}G_{ine2'}^2 \tan\theta \\ + 2Z_4 G_{ine2'}^2 \tan\theta - Z_{e3}^3 \tan\theta + \frac{2Z_4 Z_{e3}^2}{\tan\theta} \end{aligned} \tag{5.101}$$

Here,

$$G_{ine2'} = \frac{4\,\mathrm{Z_L}\,{\mathrm{Z_{e2}}}^2\,{\mathrm{Z_{o2}}}^2\tan^2\theta}{{\mathrm{Z_L}}^2\left(\mathrm{Z_{e2}} - \mathrm{Z_{o2}}\tan^2(\theta)\right)^2 + 4\,{\mathrm{Z_{e2}}}^2\,{\mathrm{Z_{o2}}}^2\tan^2\theta} \tag{5.102}$$

$$B_{ine2'} = \frac{2\,{\mathrm{Z_L}}^2\,\mathrm{Z_{e2}}\,\mathrm{Z_{o2}}\,\tan(\theta)\,\left(\mathrm{Z_{e2}} - \mathrm{Z_{o2}}\tan^2(\theta)\right)}{{\mathrm{Z_L}}^2\left(\mathrm{Z_{e2}} - \mathrm{Z_{o2}}\tan^2(\theta)\right)^2 + 4\,{\mathrm{Z_{e2}}}^2\,{\mathrm{Z_{o2}}}^2\tan^2\theta} \tag{5.103}$$

$$Z_{e3} = \rho Z_{o3} \tag{5.104}$$

5.7.2.4 Case Studies

1. **Case Studies: Frequency Ratio:** In order to estimate maximum r, the electrical length (θ) in (5.87), (5.94), (5.95), and (5.99) are varied as per (5.77) for the determination

of the required design parameter Z_{o3}, Z_1, Z_X, and Z_4 within the realizable range for a micro-strip TL. The design parameters are then calculated and plotted in Fig. 5.40 as a function of variables Z_{e2}, Z_{o2}, and Z_{e3} for a range of r. Apparently, these parameters are realizable for frequency ratio up to 5.1. A design example, case 1 at $r = 4.7$ in Table 5.9, clearly conveys that the calculated design parameters are within the micro-strip TL realizable limits.

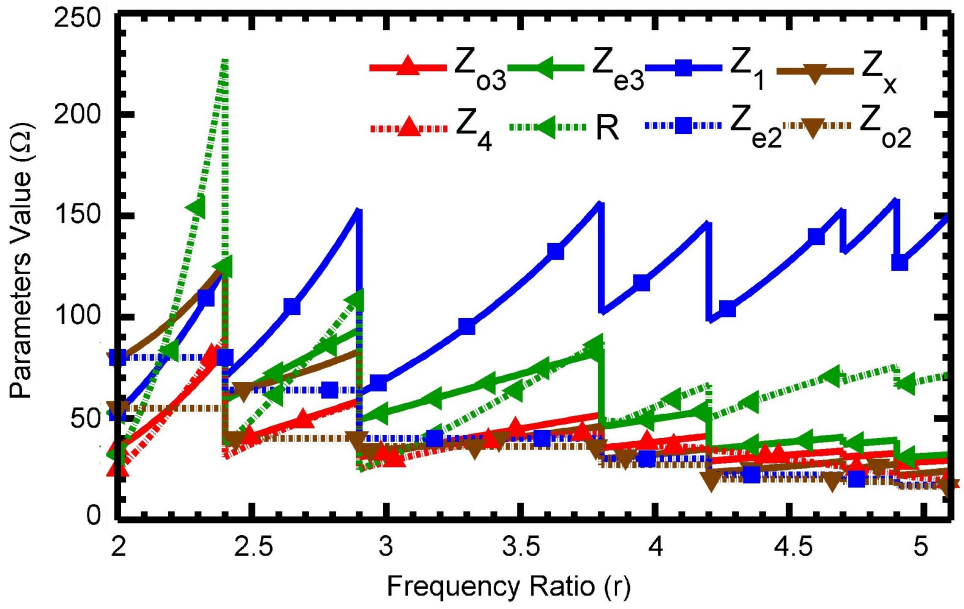


Figure 5.40: parameter values vs frequency ratio for the proposed balun

Table 5.9: Design Cases for the reported balun at different frequency and impedance transformation ratios (*: unequal electrical lengths)

Cases	r	k	**Parameters**					
			Z_1, θ_1	Z_X, θ_X	Z_{e2}, Z_{o2}, θ_2	Z_{e3}, Z_{o3}, θ_3	Z_4, θ_4	R
1	4.7	1	153, 31.6	28.9, 31.6	22, 20, 31.6	40.7, 33.9, 31.6	26, 31.6	72
2*	10	1	55, 49.09	36.6, 49.1	42.4, 33, 49.1	121.1, 100, 49.1	33, 16.4	78
3	2	8	31.9, 60	47.9, 60	140, 110, 60	168.6, 80.3, 60	29.7, 60	39
4	2	20	20, 60	29.3, 60	140, 110, 60	196.7, 93.7, 60	22.75, 60	49
5*	5	5	42.12, 60	63.19, 60	138, 104, 60	140.3, 76.1, 60	28.5, 30	32
6*	6	4	25, 51.4	19.7, 51.4	50.4, 46, 51.4	132, 116.6, 25.7	71, 25.7	33

Furthermore, the maximum $r = 5.1$ is achieved when all the TL segments are assumed equal i.e. $\theta_1 = \theta_2 = \theta_3 = \theta_4$. However, it has been identified that unequal TL segments can significantly enhance r. For example, θ_1 is varied by considering higher n in (5.77)

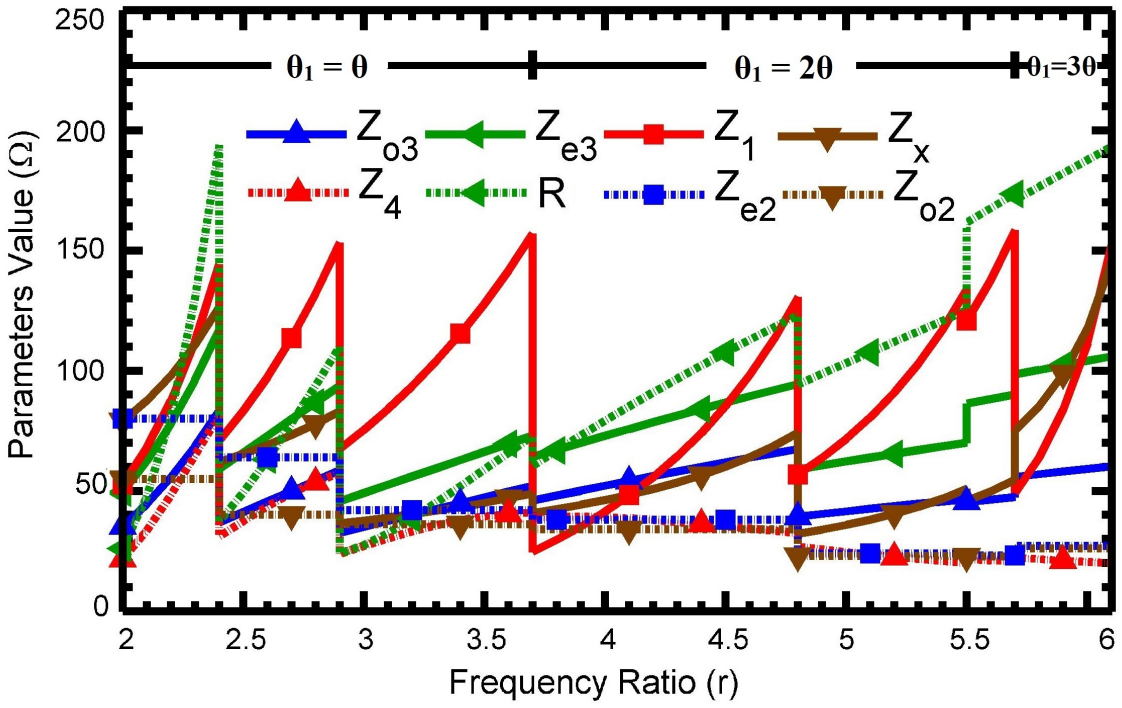


Figure 5.41: Design parameters vs frequency ratio for different multiples of θ_1

while keeping all other TLs equal i.e., $\theta_2 = \theta_3 = \theta_4$, and the outcome is plotted in Fig. 5.41. It can be observed that just changing θ_1 has the potential to enhance r to 6.1. It could be further enhanced by choosing a greater n in (5.77) for varying θ_1, but it may come at the cost of increased size and design complexity. It is safe to mention that r can be greatly enhanced by varying other electrical lengths i.e. $\theta_1, \theta_2, \theta_3, or\ \theta_4$ or a combination of them. An example using unequal TLs, case 2 in Table 5.9, clearly show that even r = 10 is achievable while keeping the design parameters realizable.

2. **Case Studies: Impedance Transformation Ratio:** Once again all the electrical lengths are kept equal for various k i.e. (Z_L/Z_S) and the design parameters are calculated. For example, Fig. 5.42 depicts that a balun with $r = 2$ is realizable upto k = 20 considering that all the design parameters are within the realizable limit as mentioned in case 4 of Table 5.9. The plots in Fig. 5.43 convey that concurrent high k and r is also achievable using the proposed design though it comes with a trade-off where maximum achievable k is reduced to 2.2. However, unequal electrical lengths can support concurrent high k

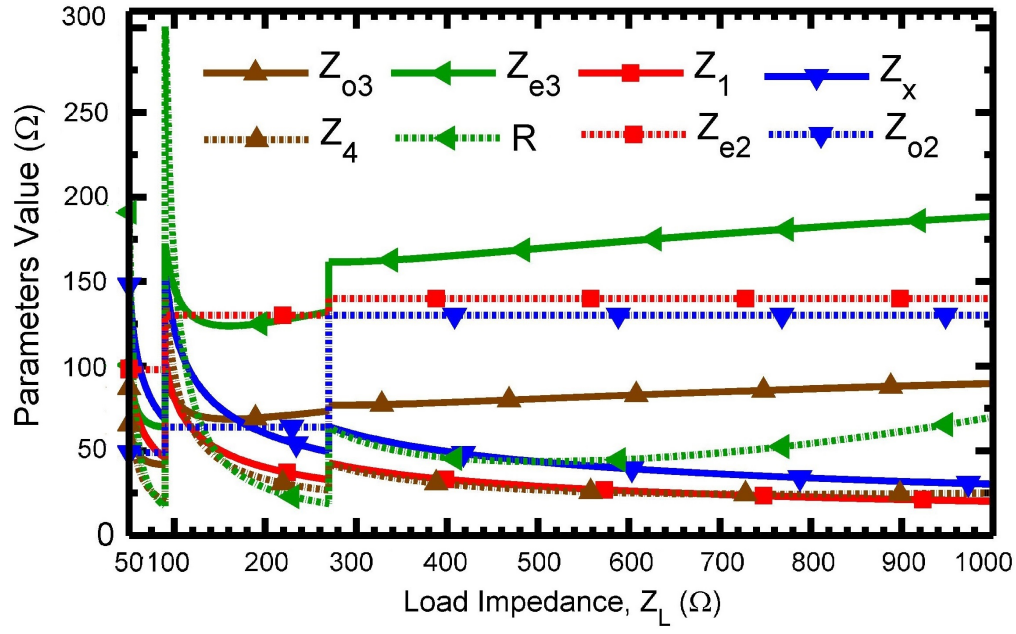


Figure 5.42: Design parameters of the balun vs the impedance ratio for r=2

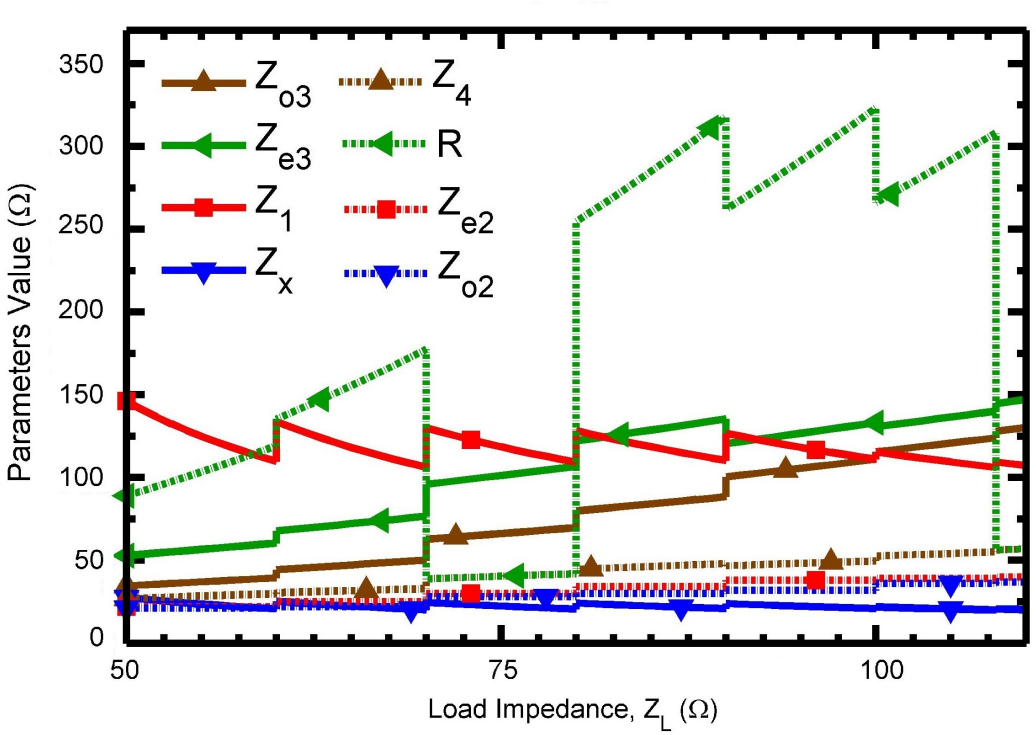


Figure 5.43: Design parameters of the balun vs the impedance ratio for r=4.7

and r as mentioned in design examples in cases 5 and 6 in Table 5.9. As per authors' knowledge, baluns with such an ultra high k as well as concurrent high k and r are being reported for the first time.

5.7.2.5 Systematic Design Procedure

The design steps are summarised below:

1. Compute r and k based on specified frequencies of operations and port terminations Z_L and Z_S.
2. Calculate θ using (5.77), and choose the independent design variables Z_{e2} and Z_{o2}.
3. Then calculate Z_{o3} and Z_1 using (5.87). If any of these are not realizable then follow step-2 by keeping their realizability in perspectives.
4. If required, a higher value of n in (5.77) can be selected to satisfy the realizability of the design parameters.
5. Now, use (5.94) to calculate Z_X for the calculated Z_1. If Z_X is not realizable then repeat steps 2 and 3.
6. Choose Z_{e3} and use (5.95) and (5.99) to calculate Z_4 and R. If Z_4 is not realizable then repeat step 5.

A total of 9 cases and their corresponding design parameters are included in Table 5.9 to demonstrate the capability of the design for wide range of r and k. For example, case 2 lists the design parameters for high r while case 5 provides design parameters for high k for same electrical lengths of TL. Similarly, case 6 corresponds to very high k while case 3 is for very high r for unequal electrical lengths of TL. It is also imperative to note that simultaneous enhancements in both k and r, cases 7 to 9, can be obtained if TL segments of unequal electrical lengths are used.

5.7.2.6 Fabrication, Measurement and Discussion

To evaluate the effectiveness of the proposed design, two design cases from Table 5.9 are considered for the development of prototypes. These are case 4 $(r,k) = (2,8)$ for extremely high k and case 7 with $(r,k) = (5,5)$ for simultaneous high k and r. These choices are influenced by the fabrication facilities available in the lab. The source impedance, Z_S, at the input port in all the cases is 50 Ω and the load impedances, Z_L, at both the output ports are regulated according to the chosen k. Thus the impedance at all the ports is Z_S = 50 Ω & Z_L = 250 Ω for case 7, and Z_S = 50 Ω & Z_L = 400 Ω for case 4. Three design cases are designed at frequencies of 1.0/5.0 GHz and 1.0/2.0 GHz, respectively and then the simulation was carried out using Keysight ADS. It is important to note here that both the cases make use of additional impedance transformers at the output ports to create 50 Ω environment for measurement purposes. The substrate chosen for these designs is RO5880 with the thickness of 1.575 mm, the permittivity of 2.2, loss tangent of 0.0009, and copper cladding of 35 μm on both sides of the substrate. There were requirements of appropriate optimization to account for the non-idealities such as discontinuities, gaps, and losses associated with the TL segments. The prototypes, with the marked dimensions, along with the corresponding measurement setups are depicted in Figs. 5.44, 5.48. Just to reiterate, the prototypes are smaller in actuality as the additional impedance transformers, used for measurement purposes, will not be required in the intended applications.

The measured results for case 4 depicted in Figs. 5.45, 5.46, and 5.47. Apparently, return loss better than -21 dB at both the design frequencies demonstrates good matching at all the ports. The 10dB matching bandwidths in this case are better than 130 MHz @ 1 GHz and 2 GHz. Measured S_{21} is -3.5 dB @ f_1 and -3.8 dB @ f_2 whereas measured S_{31} is -3.3 dB @ f_1 / -3.8 dB @ f_2 in Fig. 5.45 indicates good performance. Furthermore, a high S_{23} of -26 dB is achieved at both the design frequencies as shown in Fig. 5.46. Finally, a good phase relationship is observed in both the simulated and measured results as depicted in Fig. 5.47.

The measured and EM simulated results for case 7 are compared in Figs. 5.49-5.51. The results in Fig. 5.49 demonstrate excellent matching at the input port. The measured (simulated) return loss is smaller than -30 dB (-26 dB) at both the design frequencies and the

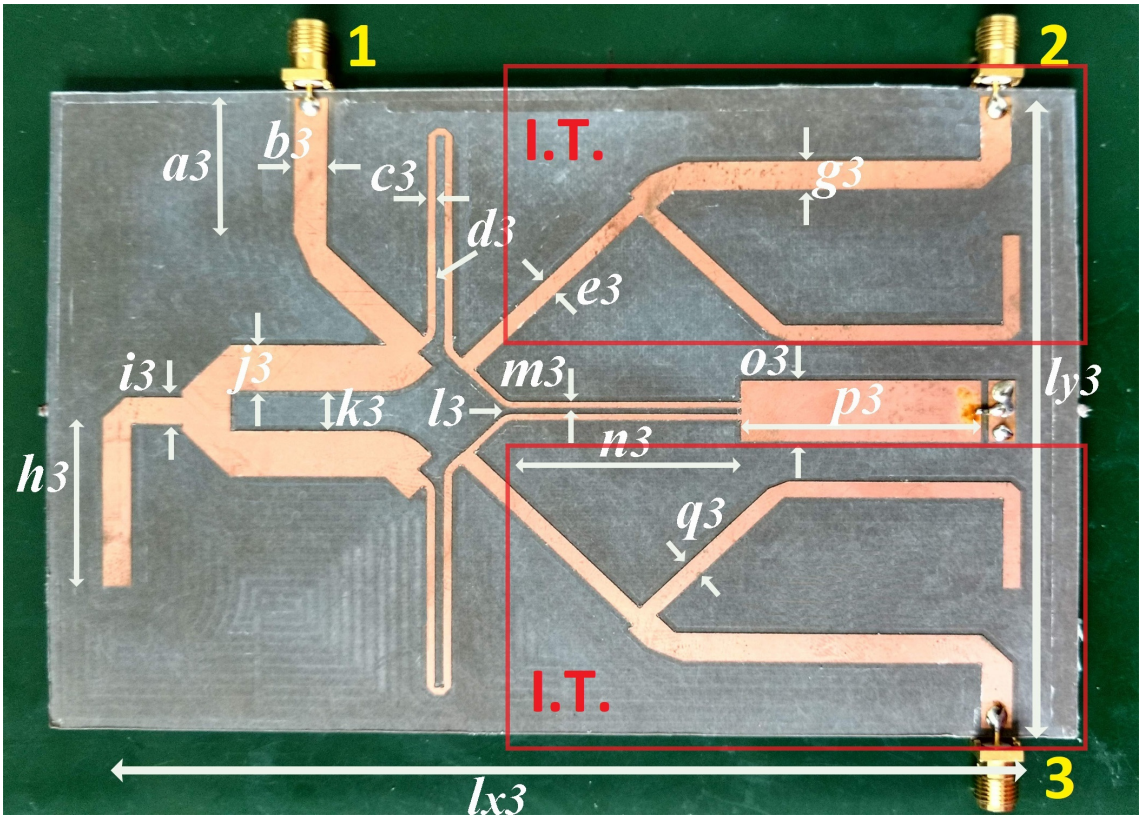


Figure 5.44: Fabricated balun prototype for r=2 and k=8. [a3=21.25, b3=4.77, c3=1.14, d3=1.28, e3=2.46, g3=4.36, h3=25.60, i3=163.94, j3=7.13, k3=6.47, l3=1.02, m3=0.86, n3=33.12, o3=9.53, p3=34.24, q3=2.42, ly3=98.05, lx3=133.35 (all in mm)] (includes two redundant impedance transformers (I.T.) in red boxes).

10 dB matching bandwidth is better than 110 MHz @ 1 GHz (11%) and 600 MHz @ 5 GHz (12%). These bandwidths readily meet the requirements of practical applications such as IEEE 802.11b/g/n (2.412 - 2.472 GHz, 2.5%), IEEE 802.11j (4.9-5.0 GHz, 2%), and narrowband IoT. The measured (simulated) insertion loss S_{21} is -3.66 dB (-3.20 dB) @ 1 GHz / -4.95 dB (-4.75 dB) @ 5 GHz, and S_{31} is -3.44 dB (-3.27 dB) @ 1 GHz / -4.17 dB (-4.03 dB) @ 5 GHz. These results include the affect of redundant impedance transformers at the output ports. Furthermore, the output port matching and isolation are also promising as can be seen in Fig. 5.50. In addition, the amplitude and phase relationships between the output ports are depicted in Fig. 5.51. The measurement results are in good agreement with the EM simulation results. Overall, the presented design achieves very good performance in terms of isolation, matching, and bandwidth.

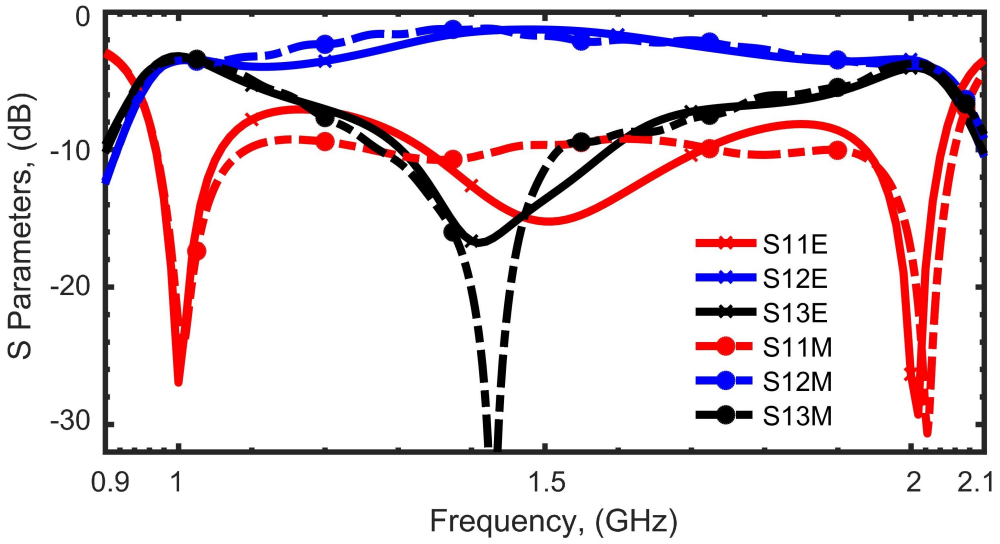


Figure 5.45: EM Simulated vs Measurement results for S_{11}, S_{12}, and S_{13} for $r = 2$ and $k = 8$, E: EM simulation results and M: Measurement Results

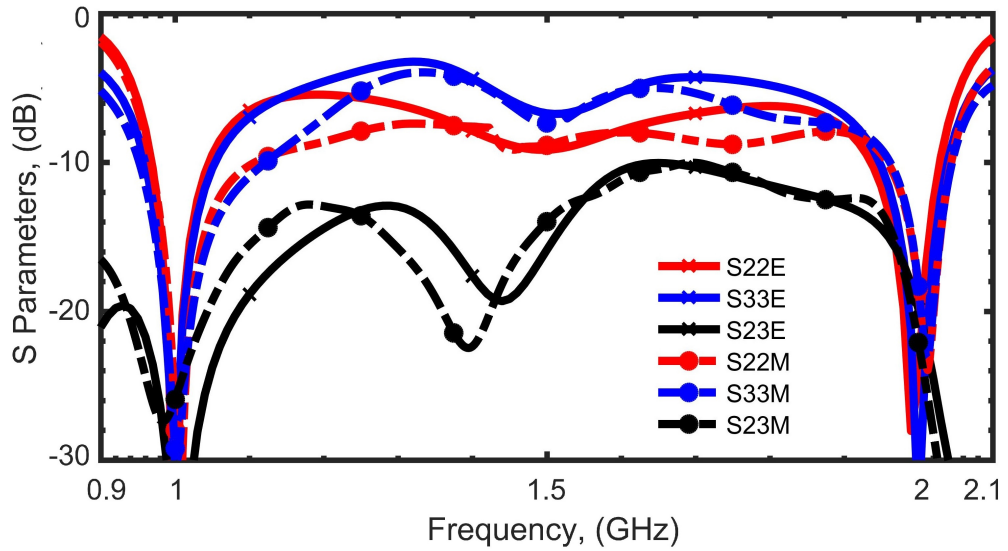


Figure 5.46: EM Simulated vs Measurement results for S_{22}, S_{33}, and S_{23} for $r = 2$ and $k = 8$, E: EM simulation results and M: Measurement Results

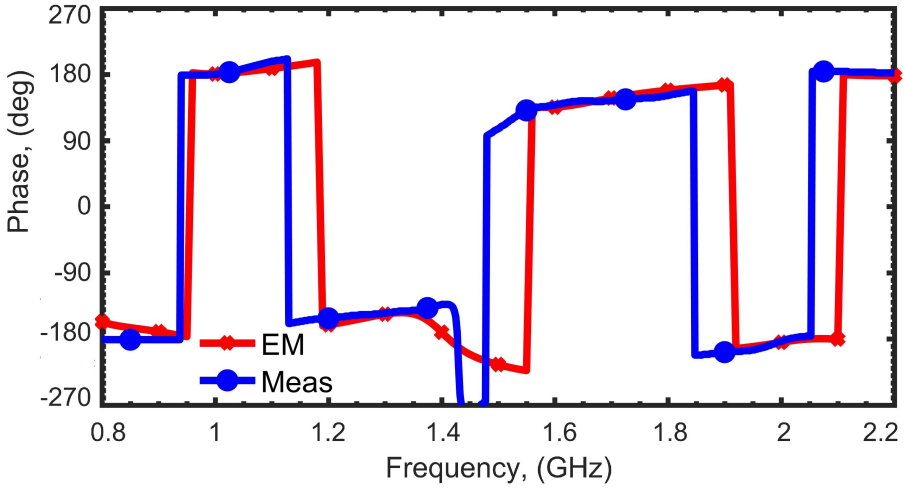
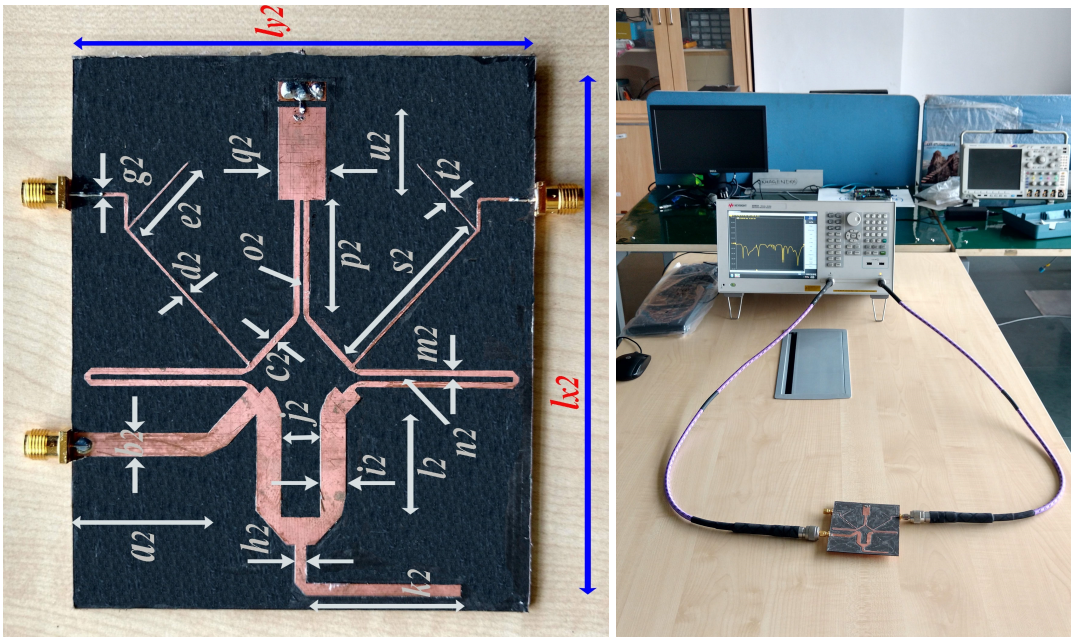


Figure 5.47: EM Simulated vs Measurement results for Phase Difference (PD) for $r = 2$ and $k = 8$, E: EM simulation results and M: Measurement Results



(a) (b)

Figure 5.48: (a)Fabricated Prototype with dimensions 101.4x98.9 mm^2 and (b) measurement setup for r=5 and k=5. [a2=29.30, b2=4.77, c2= 1.37, d2=0.69, e2= 18.33, g2=0.83, h2=2.43, i2=5.56, j2=8.12, k2=33.78, l2=19.14, m2= 1.38, n2= 0.91, o2= 0.69, p2= 22.22, q2=10.35, s2=37.19, t2= 0.38, u2=18.18, ly2=98.94, lx2=101.47]

Finally, the recent developments related to the dual-band baluns and impedance-transforming baluns are compared with the proposed architecture in Table 5.10. It is apparent from Table 5.10

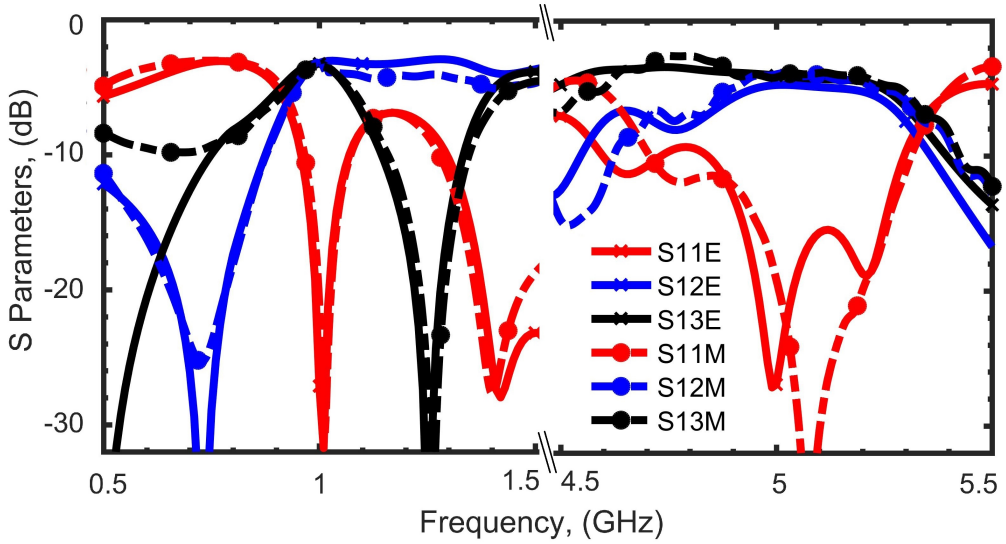


Figure 5.49: EM Simulated vs Measurement results for S_{11}, S_{12}, and S_{13} for $r = 5$ and $k = 5$, E: EM simulation results and M: Measurement Results

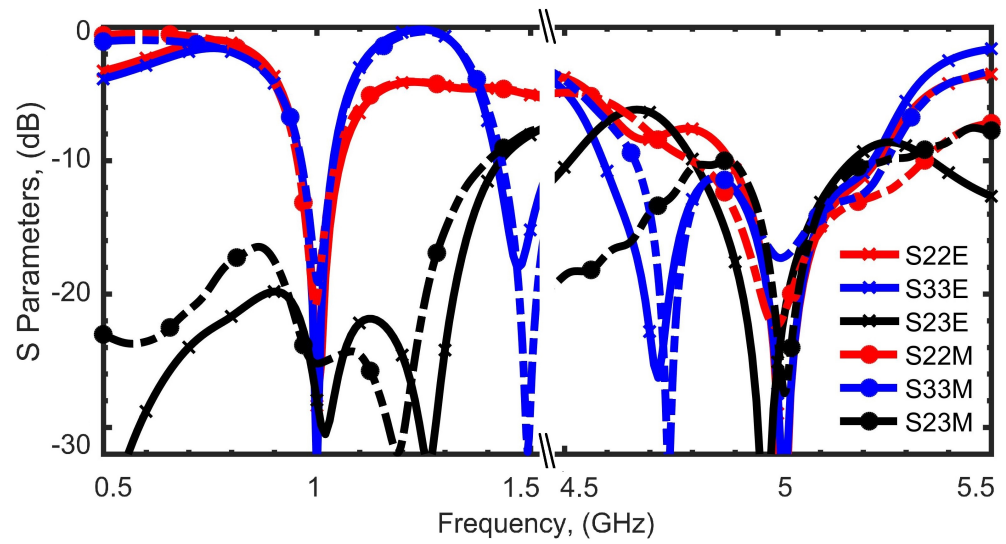


Figure 5.50: EM Simulated vs Measurement results for S_{22}, S_{33}, and S_{23} for $r = 5$ and $k = 5$, E: EM simulation results and M: Measurement Results

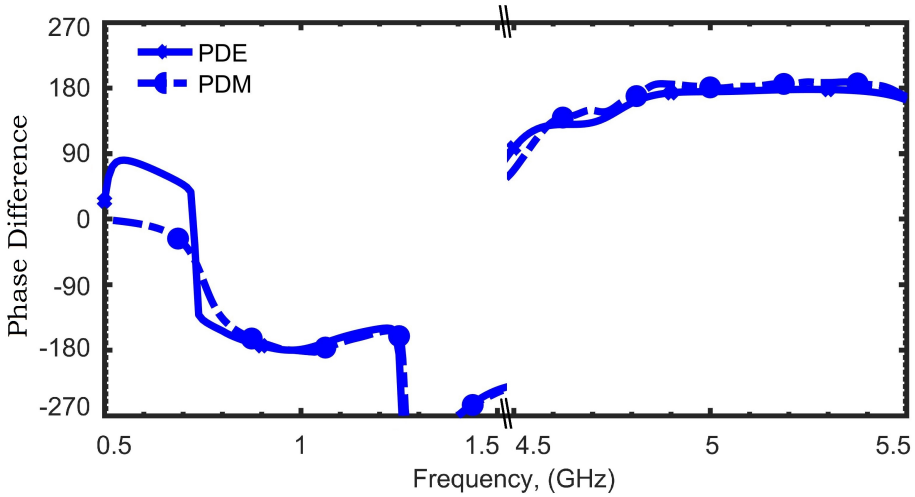


Figure 5.51: EM Simulated vs Measurement results for Phase Difference (PD) for r = 5 and k = 5, E: EM simulation results and M: Measurement Results

that the design reported in [41] is terminated with 50 Ω port impedances and hence not possible to understand impedance transformation ability. Another design [99] reports good performance at high r but is limited with k. A very recent balun architecture [136] demonstrates concurrent performance for $k = 3$ and $r = 2.13$ but at the expense of layout complexity considering the possibility of longer T-junction coupled line. The proposed design, on the other hand, possesses a simple layout and exhibits favorable performance with significantly enhanced concurrent k and r, as can be seen in the comparison Table 5.10. These k and r are substantially higher as compared to the existing state-of-the-art. Therefore, it is safe to convey that the presented design advances the dual-band balun technology as it is capable of achieving simultaneous high k and r, exhibits excellent isolation between output ports, and possesses very good port matching.

5.8 Conclusion

The measures to improve the cost-effectiveness of WCS with the design and development of the multi-functional components have been discussed in this chapter. Initially, an impedance transformer is integrated with an inherent DC isolation feature is reported. Then, multiple architectures of multi-functional power dividers and balun have been proposed and analyzed in

Table 5.10: Comparison With STATE-OF-THE-ART Baluns With High Frequency And Impedance Transformation Ratios

[Ref]	r (f_1/f_2) **(GHz)**	k (Z_L/Z_S)	S_{11} **(dB)**	S_{21} **(dB)**	S_{31} **(dB)**	S_{23} **(dB)**	**Percent Bandwidth** (S_{11})
[41]	1/2.6	Exist but prototype uses 50Ω/50Ω	<-16	-3.5/-3.8	-3.5/-4	<-21	29.7%/ 10.5% (<-10 dB)
[58]	1.0/5.0	NA	-36/-31	-3.24/-3.68	-3.24/-3.68	-29/-32	40%/5.71% (<-10 dB)
[99]	0.5/3.65	100Ω/ 130Ω	-37/-16	-4/-3.7	-3.7/-4	-26/-32	13.9%/2.8% (<-15 dB)
[136]	2.39/5.1	150Ω/ 50Ω	-36/-25	-3.5/-4.2	-3.5/-4.2	-28/-26	9.2%/4.5% (<-15 dB)
[This Work]	**1.0/2.0**	**400Ω/ 50Ω**	-21/-21	-3.5/-3.8	-3.3/-3.8	-31/-26	10%/10% (<-10 dB)
[This Work]	**1.0/5.0**	**250Ω/ 50Ω**	-29/-21	-3.6/-3.9	-3.4/-4.1	-25/-27	11%/12% (<-10 dB)

this chapter. The architectures are emphasized on the impedance transformation, and frequency ratio features specifically while providing the DC isolation or balanced to unbalanced signal transformation features additionally. While providing the multi-functional, these reported architectures are uniplanar and easy to fabricate. These simplified architectures are also backed by the analytical solutions with systematic design procedures which help in the quick prototyping of the proposed architectures. More specifically, the microstrip compatibility for a wide range of impedance transformations has been demonstrated through the design examples. Moreover, it has been shown that the proposed design scheme is versatile owing to the presence of independent design variables. Finally, the performance of the proposed circuits has been demonstrated through the fabricated prototypes which exhibit decent performance. It is envisaged that the proposed architecture and design technique will be extremely useful for upcoming applications such as 5G arrays, energy harvesting, dual-band RF amplifiers, wireless power transfer, energy harvesting, etc.

Chapter 6

Impedance Transforming Power Dividers for Frequency Dependent Complex Loads

The diversity and multi-standard nature of the existing and future wireless communication system have necessitated the operations of the wireless communication system for multiple frequencies or frequency bands concurrently. Modern WCS, such as mobile communication network (5G) new radio (NR), massive multiple-input multiple-output (MIMO) antenna systems, 5G, and compatible IoT applications, offer challenges on the front-end sub-systems to support multiple circuits connected all together and operating at different frequency bands. At the outset, it is pertinent to mention that, irrespective of the multi-frequency or single-frequency circuits or systems, often the practical situations entail complex, real, or combination of these port impedances [91, 95–97]. And in the multi-frequency scenarios, these impedances become arbitrary in nature due to their variation along with the frequency.

6.1 Frequency Dependent Complex Impedance

As discussed, impedance matching is an extremely important attribute in a WCS. The interconnects and circuits of the communication system offer arbitrary nature of impedances. Under multi-frequency operations, the frequency-dependent complex impedances vary with the frequency. For example, a microstrip line with microstrip width (W) of 50 mils and microstrip length (L) of 100 mils is simulated in an EDA tool (Keysight ADS) from a frequency of 1 GHz

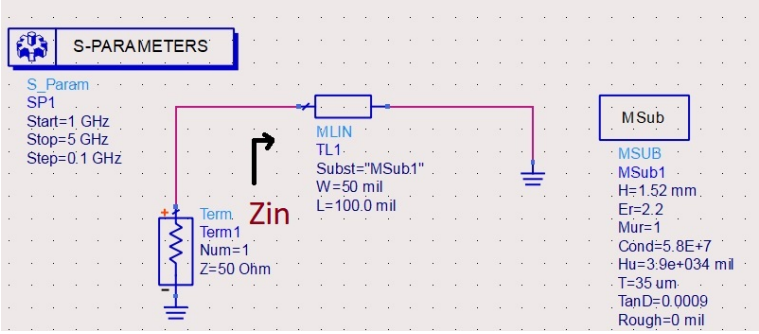
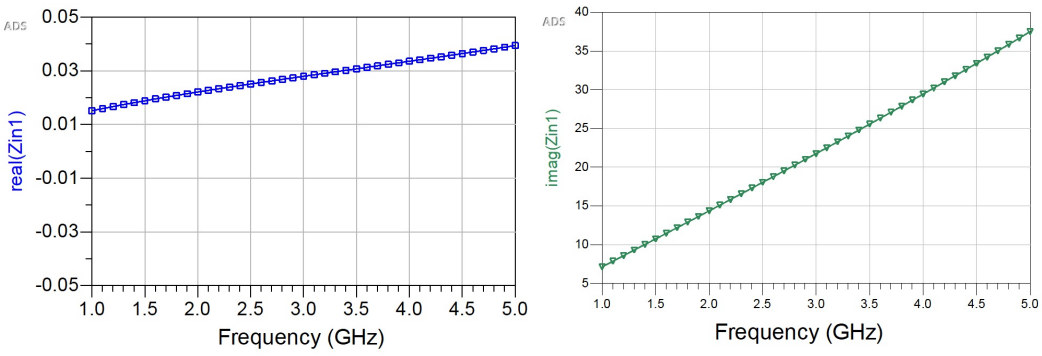


Figure 6.1: An example MLIN in Keysight ADS



(a) (b)

Figure 6.2: (a) The real part and (b) The imaginary part of the input impedance for Fig. 6.1

to 5 GHz. The schematic from the EDA tool is depicted in Fig. 6.1 with input impedance as Z_{in}. The real and imaginary parts of Z_{in} are plotted in Figs. 6.2(a) and 6.2(b), respectively. The variation of the real and imaginary part of Z_{in} over the frequencies are apparent, and it should be noted that the impedance may vary arbitrarily depending on the combinations of circuits and components of the system.

An application scenario is also illustrated in Fig. 6.3 where the multiple amplifier stages have respective input matching networks (IMN) and output matching networks (OMN) [1]. The application also demonstrates the use of a power divider, which is cascaded between the amplifier stages. This application scenario is a good example to understand the importance of inherent impedance transformation for the arbitrary impedance environment. For the multiband operation, the impedance transforming power divider can easily replace the output matching network of the first stage amplifier and the input matching network of the second stage amplifier.

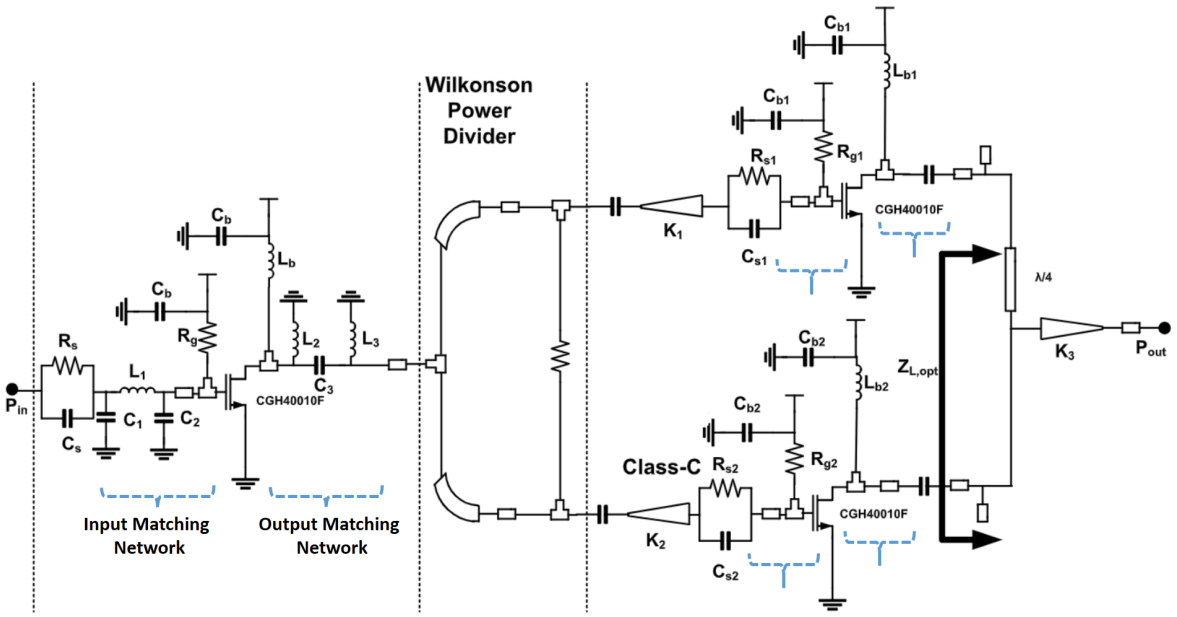


Figure 6.3: Multi-stage amplifier circuit [1]

One of the contributions of this thesis is a prominent solution to such situations and is described in this chapter in the subsequent sections.

Taking all the above discussions into perspective, there is a clear need to investigate the design of a dual-band PD with FDCL impedance transformations at widely separated arbitrary frequencies to meet the requirements of emerging communication applications. In this chapter, the solution to such issues is provided by proposing three different architectures of a power divider. The power divider circuit is taken as an example for the inherent impedance transforming capability. The power dividers are also providing the solutions to the uncorrelated complex impedances at two distinct arbitrary design frequencies. The literature is empty with such architecture where a power divider can provide the inherent impedance transformation at two arbitrary design frequencies concurrently. The frequency-dependent complex impedance can either be at the source or at the loads, or at both the source and load. For the first time, a dual-band frequency dependent complex impedance transforming PD with the systematic design procedure is presented to address some of the above constraints. Overall, the proposed architectures have the following objectives:

1. Real and complex impedance transformations.

2. Frequency-dependent complex impedance transformations.

3. High impedance transformation ratio.

4. High arbitrary frequency ratio.

5. High concurrent impedance transformation ratio and high frequency ratio.

6. Systematic and flexible design methodology.

7. Absence of reactive elements for any nature of port terminations.

8. High microstrip compatibility.

9. Simple, planar, and compact architecture.

6.2 Power Divider For Real and Complex Port Terminations

The power divider proposed in Chapter 4 demonstrates how the RF and Microwave components utilize the concept of impedance transformation in the design analysis. This is also a key observation from this work that influences the further development and improvement on the multi-functional components. However, the design analysis is kept simple and elaborates on the real-to-real impedance transformation, only. Here, the same architecture of the power divider circuit is reused, intentionally, to demonstrate its capability for the complex impedances at both the source and load ports.

The architecture of the proposed PD, shown in Fig. 6.4, comprises the same coupled line with an isolation resistor, R, as core of the power divider. The respective odd- and even-mode impedances and the electrical length of the coupled-line are Z_{o3}, Z_{e3}, and θ_3. The core of the PD then consists of TSTL, marked by respective Z and θ, at all the three ports. To maintain X-axis symmetry, the TSTLs at ports 2 and 3 have similar electrical properties. This enables a simplified even-odd mode analysis of the proposed PD structure. During the analysis, it will be shown that the input (port 1) and output (ports 2 and 3) impedances could be distinct over a wide range of complex and real values.

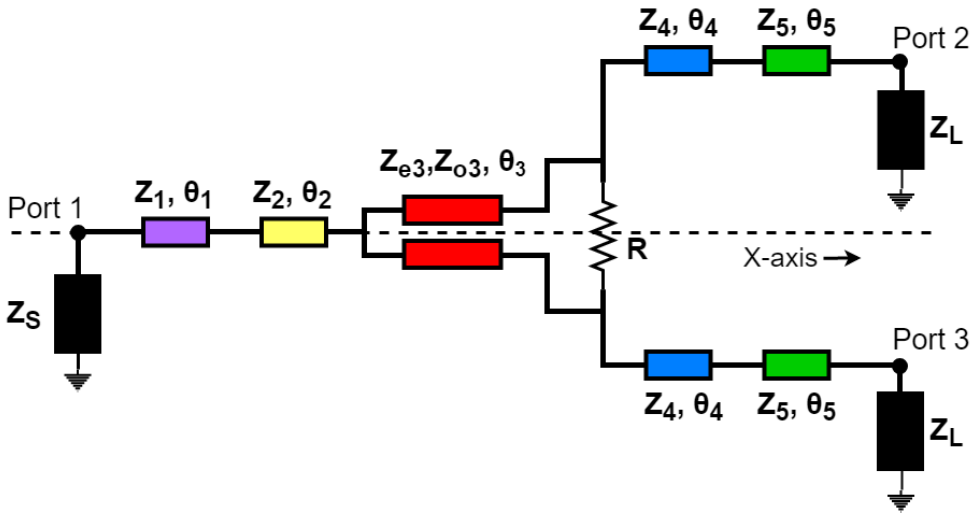


Figure 6.4: Proposed power divider with a coupled-line. input port: port 1, equal output ports: port 2 and port 3.

6.2.1 Mathematical Formulations

The even-odd mode analysis is utilized for the mathematical formulations, as follows:

6.2.1.1 Odd-mode Analysis

The odd-mode equivalent of the proposed PD, as shown in Fig. 6.5, is obtained by shorting the symmetric axis. Apparently, it is a combination of odd-mode characteristic impedance Z_{o3} and $R/2$ in parallel, and TSTL characteristic impedances Z_4 and Z_5. Now, it can be seen in Fig. 6.5 that Y_{oa}, expressed in (6.1), is the admittance generated by the parallel combination of $Y_{o3}(=1/Z_{o3})$ and $(R/2)$. The role of TSTL is to provide a match between Y_{oa} and the real or complex port admittance $Y_L(=1/Z_L = G_L + jB_L)$ for the maximum power transfer. It is imperative to note that $Y_L = G_L$ for real port termination.

$$Y_{oa} = \frac{2}{R} + \frac{-jY_{03}}{\tan\theta_3} = G_{oa} + jB_{oa} \tag{6.1}$$

The intermediate admittance, Y_{ob}, and the admittance, Y_{oc}, are expressed in (6.2) and (6.3) respectively. Subsequently, the real and imaginary parts of Y_{oc} in terms of $Y_4(=1/Z_4)$ and $Y_5(=1/Z_5)$ are given in (6.4) and (6.5). Here, $\alpha = tan\theta_4$ and $\beta = tan\theta_5$. Finally, expressions (6.6) and (6.7) need to be satisfied for the impedance matching between Y_{oc} and Y_{oa}. It will be shown in the design section that there are four independent design variables in the odd-mode

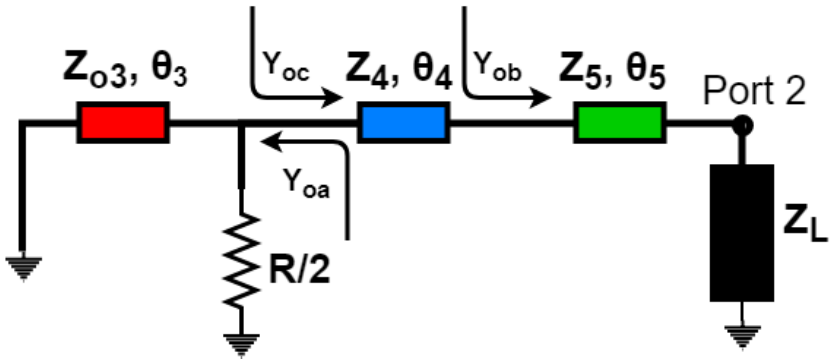


Figure 6.5: Odd-mode equivalent circuit of the proposed power divider.

analysis, including two parameters of the core, i.e, Z_{o3} and R, and θ_4 and θ_5, for realizable impedances using a micro-strip line.

$$Y_{ob} = Y_5 \left(\frac{Y_L + jY_5 tan\theta_5}{Y_5 + jY_L tan\theta_5} \right) \tag{6.2}$$

$$Y_{oc} = Y_4 \left(\frac{Y_{ob} + jY_4 tan\theta_4}{Y_4 + jY_{ob} tan\theta_4} \right) = G_{oc} + jBoc \tag{6.3}$$

$$G_{oc} = \left(\frac{{Y_4}^2 Y_5 Y_L [1 + \alpha^2 + \beta^2 + \alpha^2\beta^2]}{(Y_4 Y_5 - Y_5\alpha\beta)^2 + (Y_4 Y_L\beta + Y_L\alpha)^2} \right) \tag{6.4}$$

$$\begin{aligned} B_{oc} = Y_4 & \left(\frac{\alpha\beta({Y_4}^2{Y_L}^2\beta - {Y_5}^2\beta - Y_4{Y_5}^2\alpha + Y_4{Y_L}^2\alpha)}{(Y_4 Y_5 - Y_5\alpha\beta)^2 + (Y_4 Y_L\beta + Y_L\alpha)^2} \right) \\ & + Y_4 \left(\frac{Y_4({Y_5}^2\beta + Y_4{Y_5}^2\alpha - {Y_L}^2\beta) - {Y_L}^2\alpha}{(Y_4 Y_5 - Y_5\alpha\beta)^2 + (Y_4 Y_L\beta + Y_L\alpha)^2} \right) \end{aligned} \tag{6.5}$$

$$G_{oc} = G_{oa} \tag{6.6}$$

$$B_{oc} = -B_{oa} \tag{6.7}$$

6.2.1.2 Even-mode Analysis

Fig. 6.6 shows the even-mode equivalent of the proposed PD, and it is obtained by opening the junctions at the symmetric axis. It is a very simple series configurations of five characteristic impedances of $2Z_1$, $2Z_2$, Z_{e3}, Z_4, and Z_5 between the input and output ports. Here, the

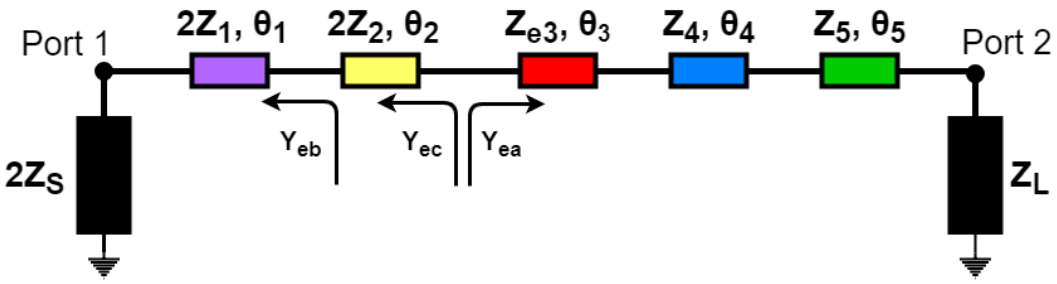


Figure 6.6: Even-mode equivalent circuit of the proposed power divider.

Table 6.1: Design Cases Of The Proposed Power Divider With Distinct Real and Complex Port Terminations

Cases	Z_S (Ω)	Z_L (Ω)	**Design Parameters**											
			Z_1 (Ω)	Z_2 (Ω)	Z_{o3} (Ω)	Z_{e3} (Ω)	Z_4 (Ω)	Z_5 (Ω)	θ_1 (°)	θ_2 (°)	θ_3 (°)	θ_4 (°)	θ_5 (°)	R (Ω)
1	50	155.9-j27	67.67	30.70	38	50	58.04	74.25	45	60	60	65	15	50
2	50	5+j10	62.15	16.81	40	65	34.10	33.85	40	65	60	30	70	400
3	40+j10	100+j200	109.8	18.44	40	55	41.19	68.71	60	25	60	55	65	10

admittance Y_{ea} is a known quantity as the design parameters Z_4 and Z_5 are already computed from the odd-mode analysis and Z_{e3} is one of the independent variables. Again, the role of TSTL, with characteristic impedances $2Z_1$ and $2Z_2$, is to create a matching environment between Y_{ea} and the equivalent even-mode input admittance, i.e. $1/2Z_S$. The unknown design parameters Z_1 (=$1/Y_1$) and Z_2 (=$1/Y_2$) although have similar forms to expressions (6.4) and (6.5) but require appropriate customization.

6.2.2 Design Procedure and Case Study

The design procedure for the proposed high frequency power divider can be summarized as:

- Choose appropriate independent design parameters Z_{e3}, Z_{o3}, θ_3, and R. Then calculate Y_{oa} using (6.1).
- Compute parameters Z_4 (=$1/Y_4$) and Z_5 (=$1/Y_5$) by solving (6.6) and (6.7) and choosing a suitable value of θ_4 and θ_5 so that these are within the realizable limits of a micro-strip transmission line, i.e. [20-140] Ω.
- Follow the above steps to compute Z_1 and Z_2.

The presence of several independent variables makes the design very flexible for a wide range of port impedances. However, in case the computed design variables are not within the realizable limits, the independent variables opted in step 1 can be altered and the process repeated. The next sub-sections provide a number of design examples to verify the design procedure and the capability of the proposed PD possessing port impedances that are distinct real and complex as well as far apart.

6.2.2.1 Real to complex Impedance Transformation

Since the peripheral devices often possess complex impedances at ports, this scenario is very pertinent. This saves the additional need for an impedance transformer at the ports. To demonstrate the flexibility of the design, the port terminations are chosen as a high complex value of $155.9 - j27.0\ \Omega$ in case 1 and as a very low complex value of $5 + j10\ \Omega$ in case 2 mentioned in Table 6.1. To reiterate, both the output ports have the same impedances, but the input port termination is kept 50 Ω for real-to-complex impedance transformation. The design parameters are then calculated for both the cases as per the design procedure.

6.2.2.2 Complex to complex Impedance Transformation

An example of widely separated complex port terminations is considered where both the input as well as output ports are complex. The output port impedance is $100 + j200\ \Omega$, and the input port impedance is $40 + j10\ \Omega$. The design case, along with the design parameters, is tabulated as case 3 in Table 6.1.

All of the above design examples from cases 1 to 3 are chosen with a variety of low and high as well as real and complex terminations to claim the high flexibility of the proposed architecture. It, therefore, validates wide ranges of the possible port terminations at different real/complex impedances.

6.3 Flexible Design Scheme of a Power Divider for Single- and Dual-Band of Operations

6.3.1 Proposed Circuit

The architecture of the proposed ITPD is shown in Fig. 6.7. The input port (port 1) of the proposed power divider is terminated with the impedance Z_S (in Ω) and the output ports (ports 2 and 3) are terminated with the impedance Z_L (in Ω) each. Both the port impedances, i.e., Z_S and Z_L, can either be a real or a complex or an uncorrelated FDCL. It should be noted here that the output ports should have equal port impedances for the equal power division. To demonstrate both the real and complex environment in the design analysis of the proposed ITPD, Z_S is considered an arbitrary real impedance while Z_L is an arbitrary complex impedance for the single-band operation and an arbitrary FDCL for the dual-band operation. The Z_L as an arbitrary FDCL is defined in (6.8) at the two arbitrary design frequencies f_1 GHz and f_2 GHz. Here, $f_2 > f_1$ ($r = f_2/f_1$). Characteristic impedance (in Ω) and electrical length (in °) of all the respective TL sections are depicted in Fig. 6.7.

$$Z_L = \begin{cases} R_{L1} + jX_{L1} \ @ f_1 \\ R_{L2} + jX_{L2} \ @ f_2 \end{cases} \tag{6.8}$$

6.3.1.1 Analytical Solution for Single-band Operation

In this section, the proposed PD is analysed for its operation at a single frequency, i.e., f_1 only. Owing to the symmetry of the architecture, the odd-even mode analysis is provided to deduce the design equations. The respective odd- and even-mode equivalent circuits are shown in Figs. 6.8 and 6.9, respectively. The load impedance Z_L is a complex entity, i.e., $Z_L = R_{L1} + jX_{L1}$ for the single-band of operation.

6.3.1.2 Odd-mode Design Analysis

The odd-mode equivalent circuit of the proposed PD is shown in Fig. 6.8. Following the TL theory, the input admittances Y_a, Y_b, and Y_c are expressed in (6.9), (6.10), and (6.11),

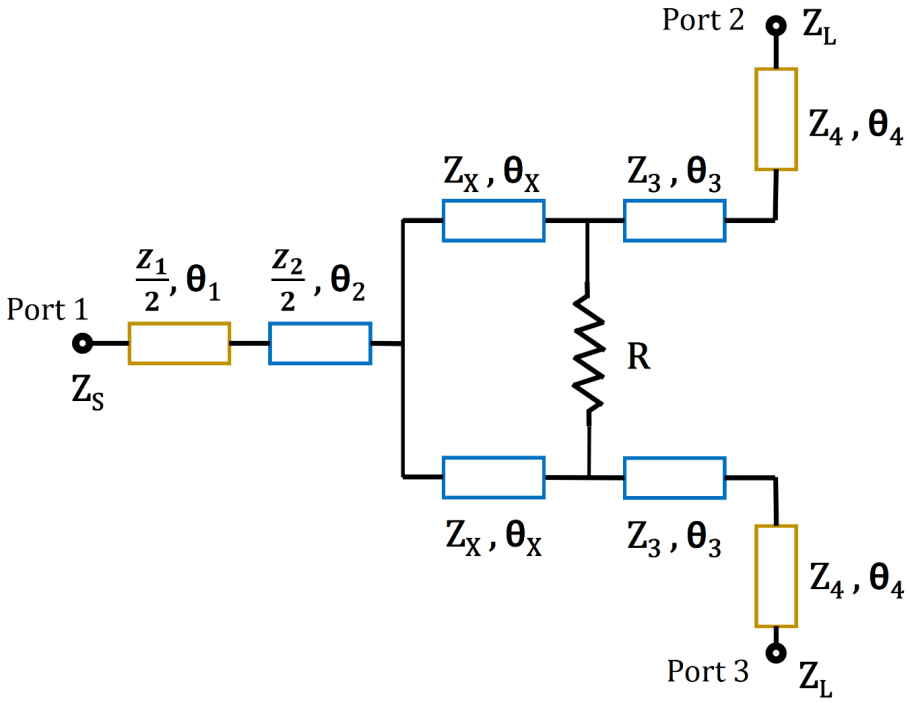


Figure 6.7: Proposed impedance transforming single and dual-band power divider circuit for real, complex, and FDCL port impedances.

respectively. For the impedance matching of the circuit, (6.12) must be followed to derive the expressions of R and Z_X. Here, the terms Z_3, Z_4, and all the electrical lengths are considered as independent design variables which makes the design scheme highly flexible for arbitrary port terminations. Subsequently, term Y_b becomes a known quantity which is expressed as $G_b + jB_b$. Following (6.12), the expressions of R and Z_X can be derived as (6.13) and (6.14), respectively.

$$Y_a = \frac{Z_4 + j\frac{1}{Y_L}tan\theta_4}{Z_4\left(\frac{1}{Y_L} + jZ_4 tan\theta_4\right)} \tag{6.9}$$

$$Y_b = \frac{Z_3 + j\frac{1}{Y_a}tan\theta_3}{Z_3\left(\frac{1}{Y_a} + jZ_3 tan\theta_3\right)} \tag{6.10}$$

$$Y_c = \frac{2}{R} + \frac{1}{jZ_X tan\theta_X} \tag{6.11}$$

$$[Y_b] = [Y_c^*] \tag{6.12}$$

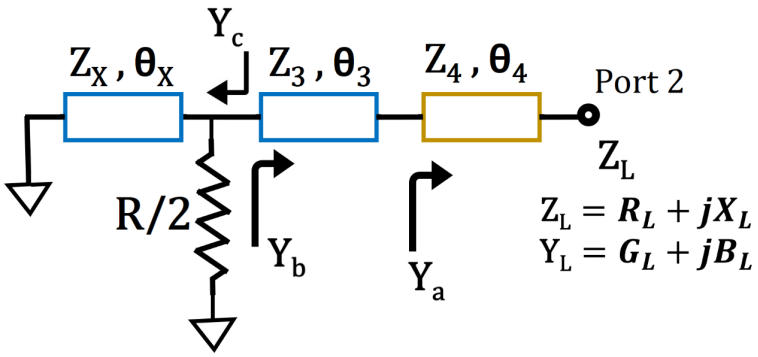


Figure 6.8: Odd-mode equivalent circuit for single-band operations.

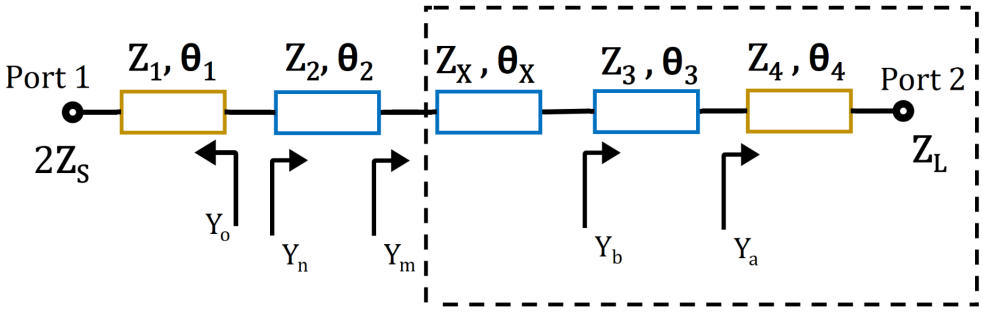


Figure 6.9: Even-mode equivalent circuit for single-band operations.

$$R = \frac{2}{G_b} \tag{6.13}$$

$$Z_X = \frac{1}{B_b \, tan\theta_X} \tag{6.14}$$

6.3.1.3 Even-mode Design Analysis

The even-mode equivalent circuit of the proposed ITPD is shown in Fig. 6.9. The design parameters Z_X, Z_3, Z_4, θ_X, θ_3, and θ_4 are known from the odd-mode analysis. The admittances Y_m, Y_n and Y_o can be expressed in (6.15), (6.16), and (6.17), respectively.

$$Y_m = \frac{Z_X + j\frac{1}{Y_b} tan\theta_X}{Z_X \left(\frac{1}{Y_b} + jZ_X \, tan\theta_X\right)} \tag{6.15}$$

$$Y_n = \frac{Z_2 + j\frac{1}{Y_m} tan\theta_2}{Z_2 \left(\frac{1}{Y_m} + jZ_2 \, tan\theta_2\right)} \tag{6.16}$$

Table 6.2: Calculated values of the design parameters of the proposed ITPD [*based on the real part of the impedances at the ports, NA: Not Applicable (single band design case)]

Case	r	k* @ f_1, f_2	Z_L, Z_S (Ω)	$Z_1(\Omega)$, $\theta_1(^\circ)$	$Z_2(\Omega)$, $\theta_2(^\circ)$	$Z_3(\Omega)$, $\theta_3(^\circ)$	$Z_4(\Omega)$, $\theta_4(^\circ)$	$Z_X(\Omega)$, $\theta_X(^\circ)$	$R(\Omega)$
1	2.6	0.55, 0.42	54.14+j8.6, 30 @f_1 70.7+j5.3, 30 @f_2	62.34, 50	33.22, 50	49.29, 50	60, 70	108.37, 50	93
2	3	20; 8	20+j8, 400 @f_1 50+j5, 400 @f_2	94.375, 45	65.175, 45	28.89, 45	30.17, 63	60.15, 45	71
3	4.5	5; 2	20+j8, 100 @f_1 50+j5, 100 @f_2	45.73, 32.73	31.93, 32.73	20.96, 32.73	30.17, 45.76	105.51, 32.73	86
4	5	2, 2	50, 100 @f_1 50, 100 @f_2	30, 30	42.34, 30	22.4, 30	77, 30	110.9, 30	120
5	2	10, 10	50, 500 @f_1 50, 500 @f_2	138.83, 60	39.5, 60	21.9, 60	41, 60	23.2, 60	32
6	NA	3.12	155.9-j27, 50 @f_1 155.9-j27, 50 @f_2	63.6, 69.5	32.6, 73.3	58.1, 65.5	68.7, 13.6	38.5, 60	50

$$Y_o = \frac{Z_1 + j\frac{1}{2Y_S} tan\theta_1}{Z_1\left(\frac{1}{2Y_S} + jZ_1\ tan\theta_1\right)} \tag{6.17}$$

Again for the impedance matching, (6.18) should be invoked to deduce the expressions of the design parameters Z_1 and Z_2. The electrical lengths θ_1 and θ_2 are independent variables here, which further enhances the design flexibility. For the simpler design analysis, θ_1 and θ_2 can also be considered equal.

$$[Y_o] = [Y_n^*] \tag{6.18}$$

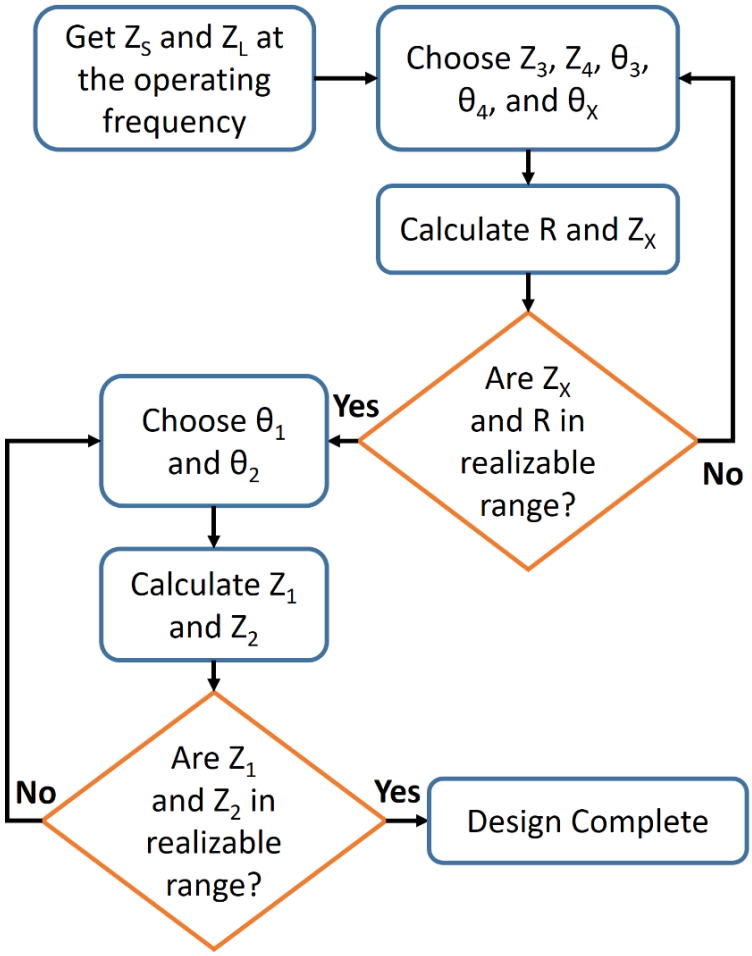


Figure 6.10: Design flowchart for the single-band ITPD.

A design flowchart of the proposed ITPD for the single-band operation is depicted in Fig. 6.10. It should be noted that the design procedure provides a number of independent variables which makes the design extremely flexible. The flexibility doesn't only make the design realizable for arbitrary port impedances but choosing smaller values of θ_1, θ_2, θ_3, θ_4, and θ_X provides a compact design of the proposed ITPD.

6.3.2 Analytical Solution for Dual-band Operation

The proposed ITPD is also analysed for its operation at two arbitrary design frequencies for the dual-band operation. Subsequently, the variation at the arbitrarily chosen design frequencies

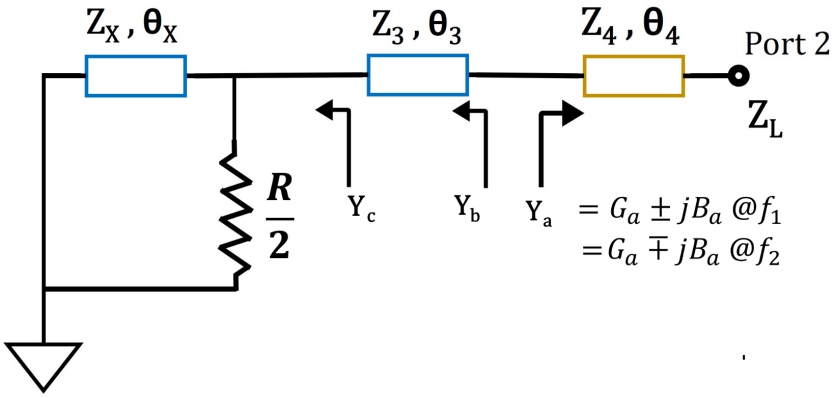


Figure 6.11: Odd-mode equivalent circuit for dual-band operations.

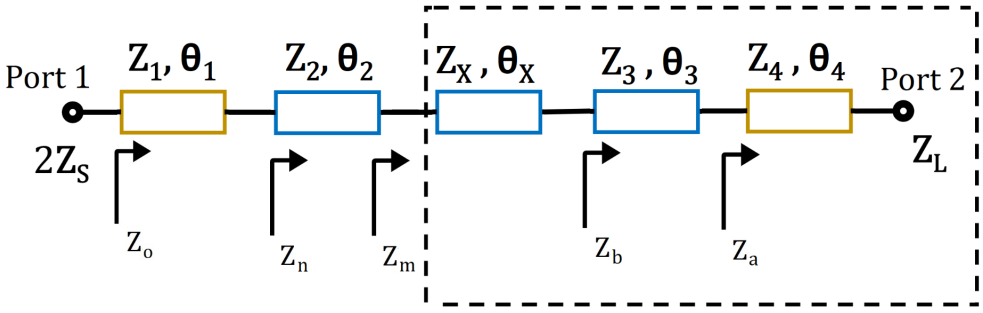


Figure 6.12: Even-mode equivalent circuit for dual-band operations.

highlights the FDCL nature of the port impedances. The impedance Z_S is an arbitrary real impedance and Z_L is an arbitrary FDCL which is already defined in (6.8).

6.3.2.1 Odd-mode Design Analysis

The odd-mode equivalent circuit of the proposed ITPD for the dual-band operation is depicted in Fig. 6.11. The arbitrary FDCL Z_L (or $1/Y_L$) is converted to a complex conjugate admittance Y_a for Z_4 and θ_4 as expressed in (6.19) and (6.20), respectively [172].

$$Z_4 = \sqrt{R_{L1}R_{L2} + X_{L1}X_{L2} + \frac{X_{L1}+X_{L2}}{R_{L2}-R_{L1}}N} \tag{6.19}$$

$$\theta_4 = \frac{\pi + \tan^{-1}\frac{Z_4(R_{L1}-R_{L2})}{R_{L1}X_{L2}-R_{L2}X_{L1}}}{1+r}, \tag{6.20}$$

Subsequently, to achieve the impedance matching for the odd-mode equivalent circuit, Y_b should follow (6.21) which results in the expressions of the design parameters Z_3 and Z_X. The electrical lengths are considered equal i.e. $\theta_3 = \theta_X = \theta$ for the simplification of the expressions. The real and imaginary parts of the admittances Y_a and Y_b are expressed in (6.22), (6.23) and (6.24), (6.25), respectively. The admittance Y_b will also be a complex conjugate entity if θ follows (6.26) [173].

$$[Y_b] = [Y_a^*] \tag{6.21}$$

$$Re[Y_a] = G_a = \frac{R_L + R_L \tan^2\theta}{R_L^2 + {Z_4}^2 \tan^2\theta} \tag{6.22}$$

$$Im[Y_a] = B_a = \frac{R_L^2 \tan\theta - {Z_4}^2 \tan\theta}{Z_4\left(R_L^2 + {Z_4}^2 \tan^2\theta\right)} \tag{6.23}$$

$$Re[Y_b] = \frac{2RZ_X^2(tan\theta^2 + 1)}{R^2Z_3^2 + R^2Z_X^2 + 4Z_3^2Z_X^2 tan\theta^2 + 2R^2Z_3Z_X} \tag{6.24}$$

$$Im[Y_b] = \frac{R^2(Z_3 + Z_X)(Z_3 - Z_X tan\theta^2) - 4Z_3^2Z_X^2 tan\theta^2}{Z_3 tan\theta((Z_3 + Z_X)^2 + 4Z_3^2Z_X^2 tan\theta^2)} \tag{6.25}$$

$$\theta = \frac{(1+n)\pi}{1+r};\ n \in (0, 1, 2, ..) \tag{6.26}$$

6.3.2.2 Even-mode Design Analysis

The even-mode equivalent circuit of the proposed power divider for the dual-band operation is shown in Fig. 6.12. It is apparent from the circuit that, except Z_1 and Z_2, all the design parameters are already calculated in the odd-mode analysis. Therefore, the input impedance Z_m is known and can be written as $R_m + jX_m$ @ f_1, and $R_m - jX_m$ @ f_2 where, R_m and X_m are the real and imaginary parts of Z_m, respectively. Again, the electrical lengths are considered equal i.e. $\theta_1 = \theta_2 = \theta$, as in (6.26), for the simplification of the expressions.

Following the TL theory and the design analysis in Chapter 4 [(4.42) - (4.54)], the two design equations to compute Z_1 and Z_2 can be expressed as:

$$2Z_S a^2 Z_2^2 + [2Z_S X_m a + Z_1(R_m - 2Z_S)]Z_2 + [Z_1 2Z_S X_m a - Z_1^2 R_m a^2] = 0 \tag{6.27}$$

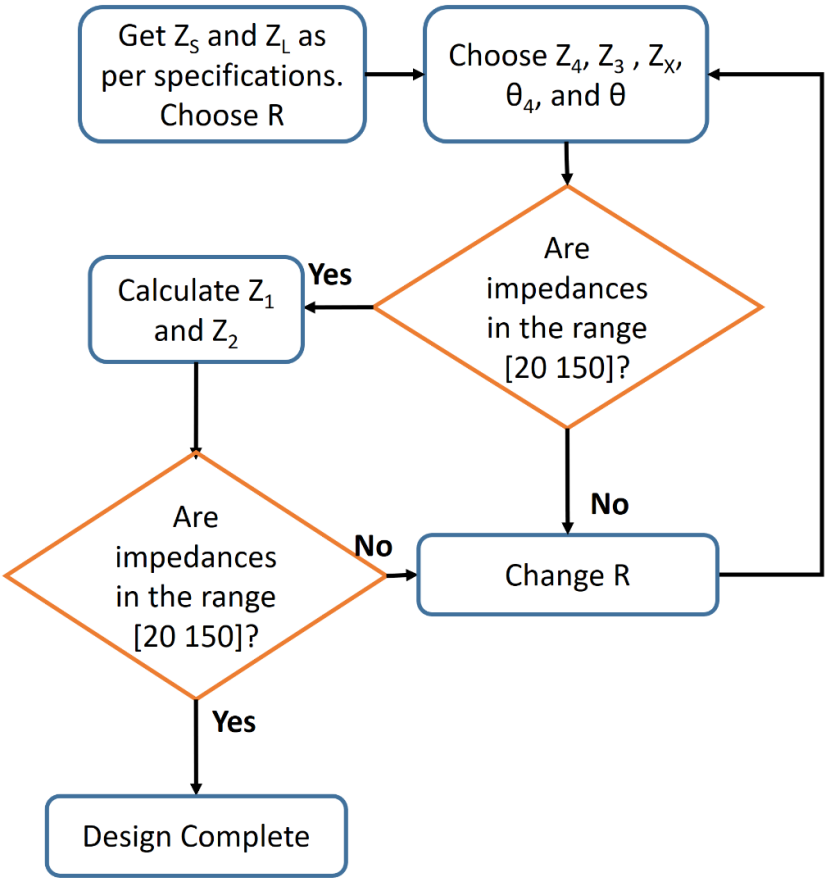


Figure 6.13: Design flowchart for the dual-band ITPD.

$$Z_1 a Z_2^2 + [Z_1 X_m - R_m 2 Z_S a + Z_1^2 a] Z_2 - [Z_1 2 Z_S R_m a + Z_1^2 X_m a^2] = 0 \tag{6.28}$$

Here, $a = tan\theta$.

A design flowchart of the dual-band PD is depicted in Fig. 6.13. It is apparent from the flowchart that the independent design parameters are reduced in comparison to single-band ITPD which is due to the additional burden of dual-band characteristics with the arbitrary frequency varying impedance transformation. The design parameter R is the only independent variable here. The electrical lengths must follow (6.26) for the dual-band operation of the ITPD except θ_4 which is provided in (6.20). However, for the design cases with real impedance terminations at the output ports θ_4 should also follow (6.26).

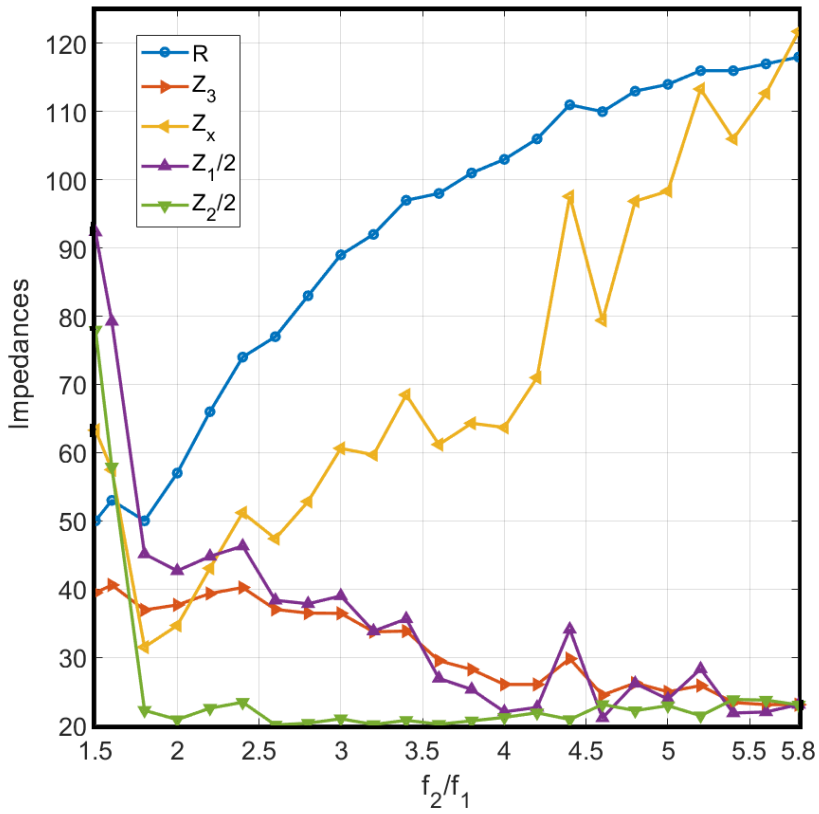


Figure 6.14: Design parameters for different frequency ratios for FDCL ($Z_S = 50$).

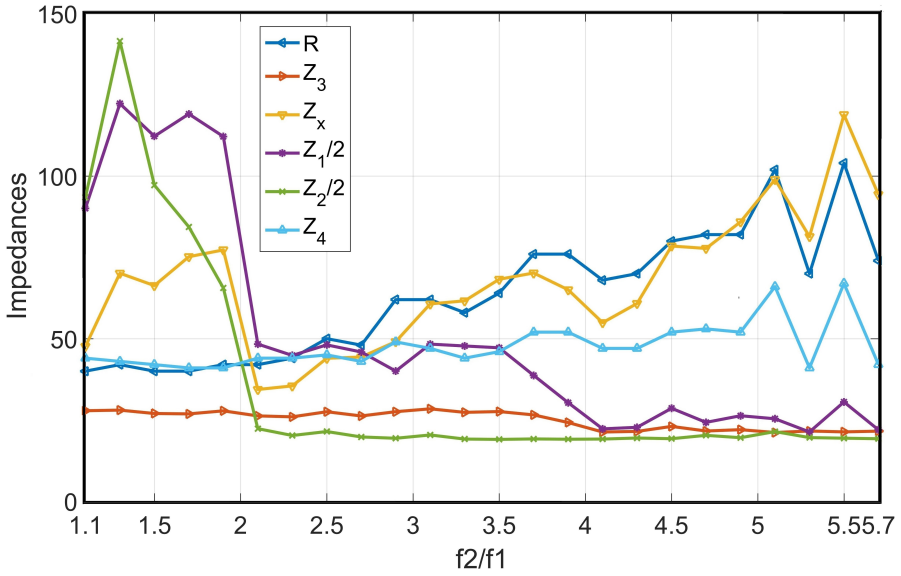


Figure 6.15: Design parameters for different frequency ratios for $Z_L = 50$ and $Z_s = 50$.

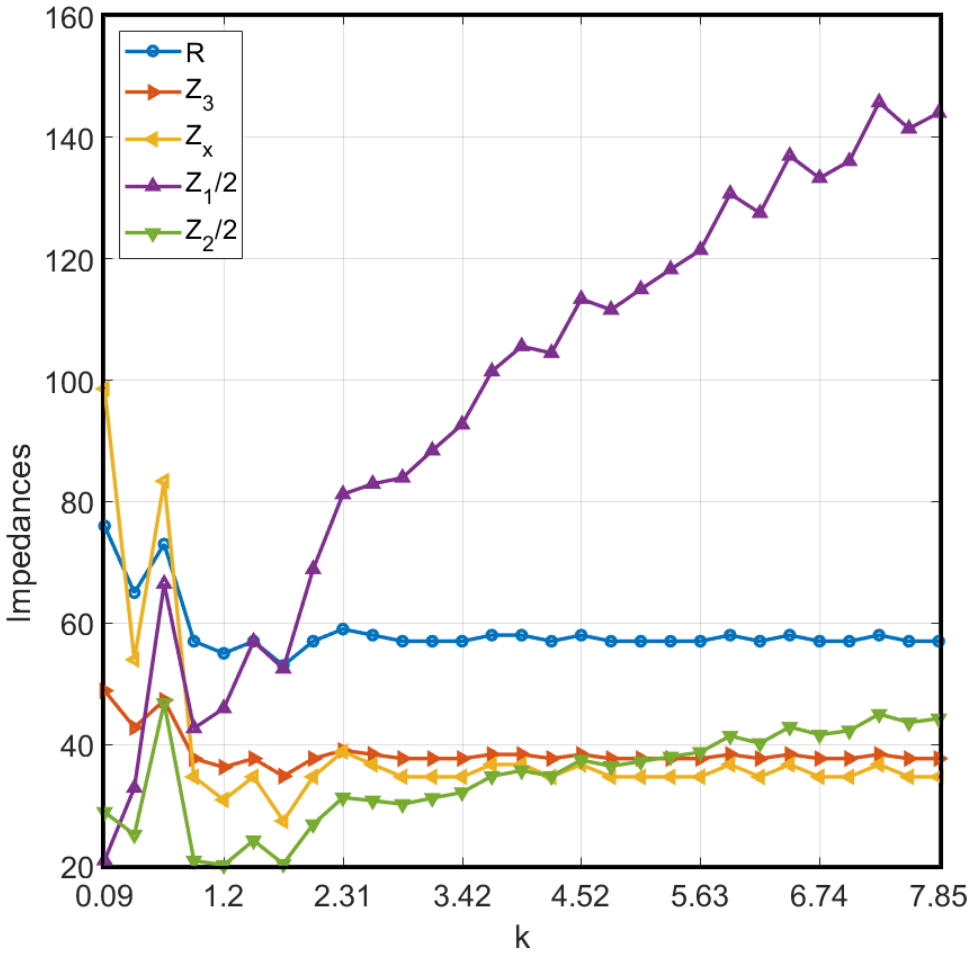


Figure 6.16: Design parameters for impedance ratios for $Z_L = 54.135 + j8.595@f_1; 70.656 + j5.269@f_2$ and $r = 2$ for smaller Zs from 5 to 425.

6.3.3 Case Studies

The reported PD is an ideal solution for varying impedance environments usually required in the front-end circuits of a wireless communication system. The effectiveness of the proposed ITPD is studied by evaluating its design parameters for varied design specifications, such as arbitrary port terminations and arbitrary design frequencies. The port terminations can independently be a real, complex, or FDCL in nature based on the design requirement.

It is apparent from the last section that the design flexibility of the proposed ITPD is limited for the dual-band operation in comparison to a single frequency of operation. It is, therefore, decided to evaluate the range of k and r for the dual-band operation of the proposed ITPD in the following case studies.

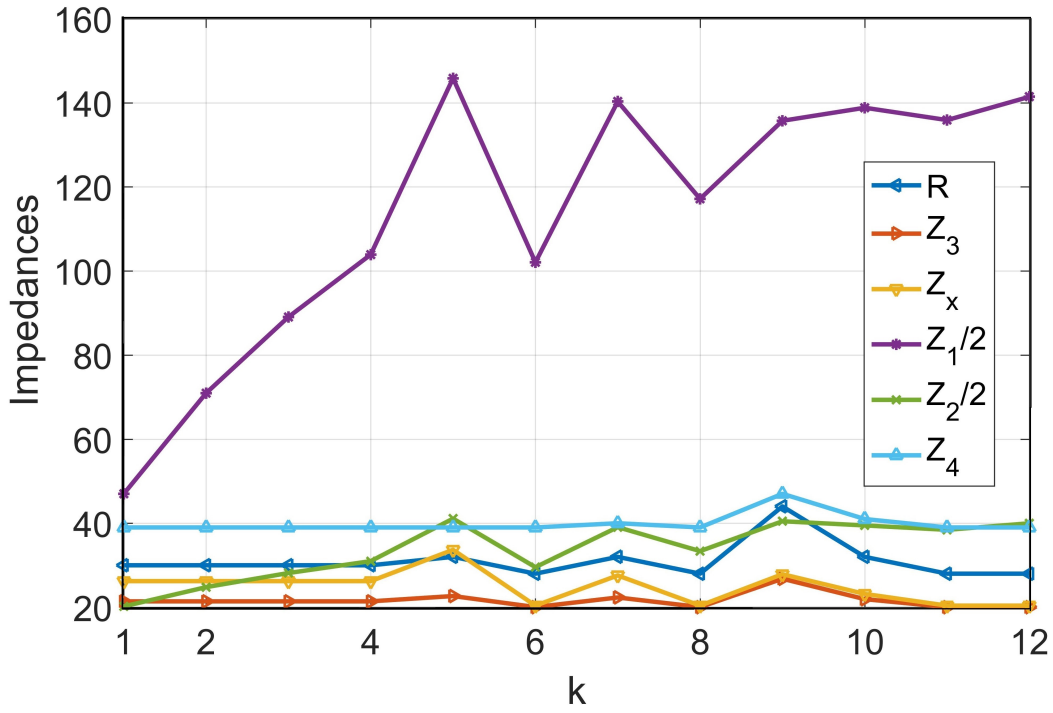


Figure 6.17: Design parameters for impedance ratios for $Z_L = 50$ and $r = 2$.

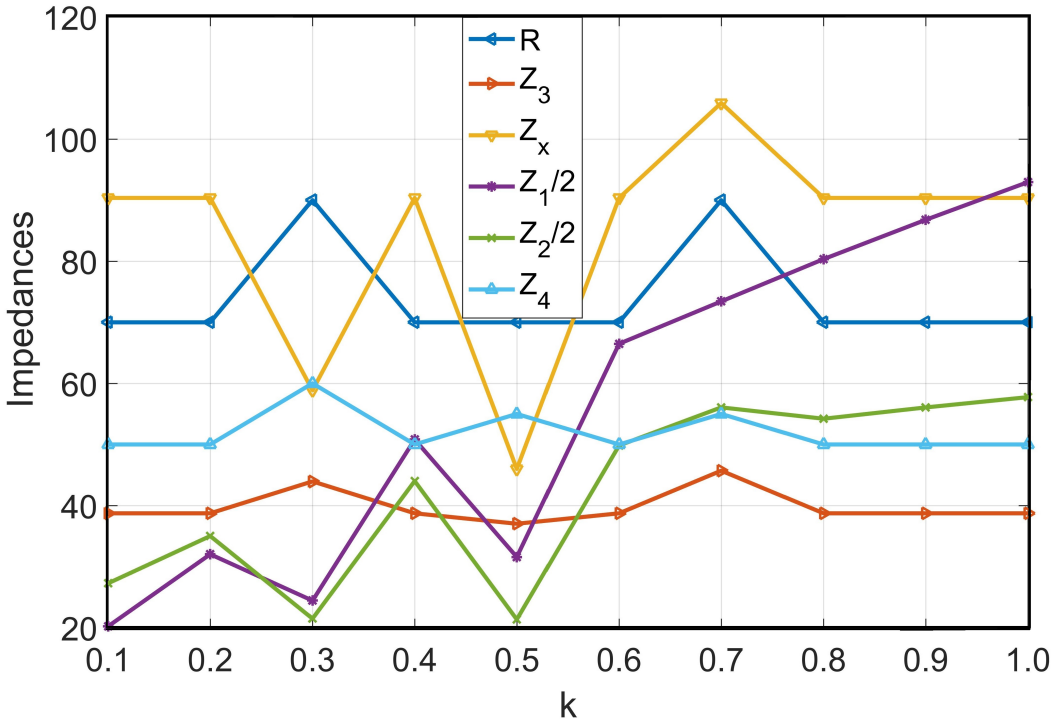


Figure 6.18: Design parameters for different impedance ratios for $Z_L = 50$ and $r = 2$ for smaller Zs.

6.3.3.1 Case Studies: Frequency ratios

The proposed ITPD is capable of providing arbitrary r for the dual-band operation. To analyse the range of r, an arbitrary design example with real input impedance i.e. $Z_S = 50$ and FDCL output impedance, i.e. $Z_L = 54.14 + j8.6$ @ f_1 GHz, and $Z_L = 70.6 + j5.3$ @ f_2 GHz is selected. The minimum and maximum range of r is evaluated for the realizable design parameters. These calculated design parameters for distinct r are plotted in Fig. 6.14 which reveals that all the design parameters are within the realizable range in the microstrip technology. A very wide range of r from 1.5 to 5.8 is achieved in this study. It should also be noted that the FDCL port terminations and its variation with frequency may influence the range of r unlike the arbitrary but real port terminations. Additionally, for the real port terminations, the analysis is repeated for the 50 Ω port impedances at all the ports and the plot is depicted in Fig. 6.15. It is safe to convey that the proposed ITPD is an ideal choice for the very wide range of arbitrary r for real, complex, and FDCL port terminations at any port.

6.3.3.2 Case Studies: Impedance transformation ratios

In this case study, the proposed ITPD is evaluated for the range of k for a fixed value of $r = 2$. Again, the design parameters are calculated for the output port impedances $Z_L = 54.14 + j8.6$ @ f_1 GHz, and $Z_L = 70.6 + j5.3$ @ f_2 GHz. The frequency ratio is fixed at $r = 2$ and the source impedance Z_S is varied from the impedance as low as 5 Ω to as high as 425 Ω. The respective design parameters are calculated and plotted in Fig. 6.16. All the design parameters are realizable in the microstrip technology. This analysis demonstrates the effectiveness of the proposed ITPD for high impedance transformations while transforming an arbitrary real impedance to an arbitrary FDCL impedance. Additionally, the PD is also evaluated and plotted for the real port terminations in Figs. 6.17 and 6.18. Here, the load impedances are fixed at 50 Ω while the source impedance is varied from as low as 5 Ω to as high as 600 Ω. For the clarity of the plots, Fig. 6.17 and Fig. 6.18 are plotted separately to demonstrate the calculated design variables when the source impedance is lower and greater than Z_L, respectively. Considering the fact of enhanced flexibility, the achievable k will improve significantly for the single-band operation of the proposed ITPD.

The design parameters for some of the design cases with arbitrary r and k are calculated and listed in Table 6.2. Cases 1 depicts the design case with dual-band operation of the ITPD for a FDCL impedance at the output ports. Cases 2 and 3 also demonstrate the design cases with FDCL impedance but with different r and k. The design cases 4 and 5 have the real port impedances at all the ports with different r and k. The case 6 of the Table 6.2 depicts the design parameters for the single-band operation of the proposed ITPD.

6.3.3.3 Discussion on Bandwidth Control

Though this thesis doesn't entail the tools and techniques on bandwidth enhancement, a brief discussion for the bandwidth control using its design parameters is provided. The proposed PD demonstrate a good improvement over the existing literature for the equal power division at arbitrary r and k. Considering the requirements from practical design environment, the proposed ITPD is tested in a simulation setup for bandwidth improvement. Owing to the independent variables, the selection of the design parameters has the ability to provide reasonable improvements on the operational bandwidth. It has been identified that the bandwidth of the proposed ITPD can be controlled using Z_X and R. It is found that keeping Z_X and R at higher value increases the overall bandwidth of the PD. Furthermore, the variation in Z_X and R controls the isolation bandwidth up to a great extent. It has been seen that the higher Z_X leads to the increased outband isolation bandwidth, whereas, higher R improves the inband bandwidth. It is worthwhile to note that in case of limited flexibility, Z_X should be prioritized over R for the higher operational bandwidth.

6.3.4 Fabrication and Experimental Evaluation

The proposed ITPD is a good solution for the frequency varying impedance environments for the single- or dual-band operations. To experimentally evaluate the performance of the proposed design, two different prototypes are fabricated on the microstrip technology. The first prototype demonstrates the single-band operation, which is designed at a high frequency of 5.8 GHz (WLAN) and the arbitrary output port impedance is $155.9 - j27\ \Omega$. The source impedance is fixed to the conventional 50 Ω. The calculated design parameters for this

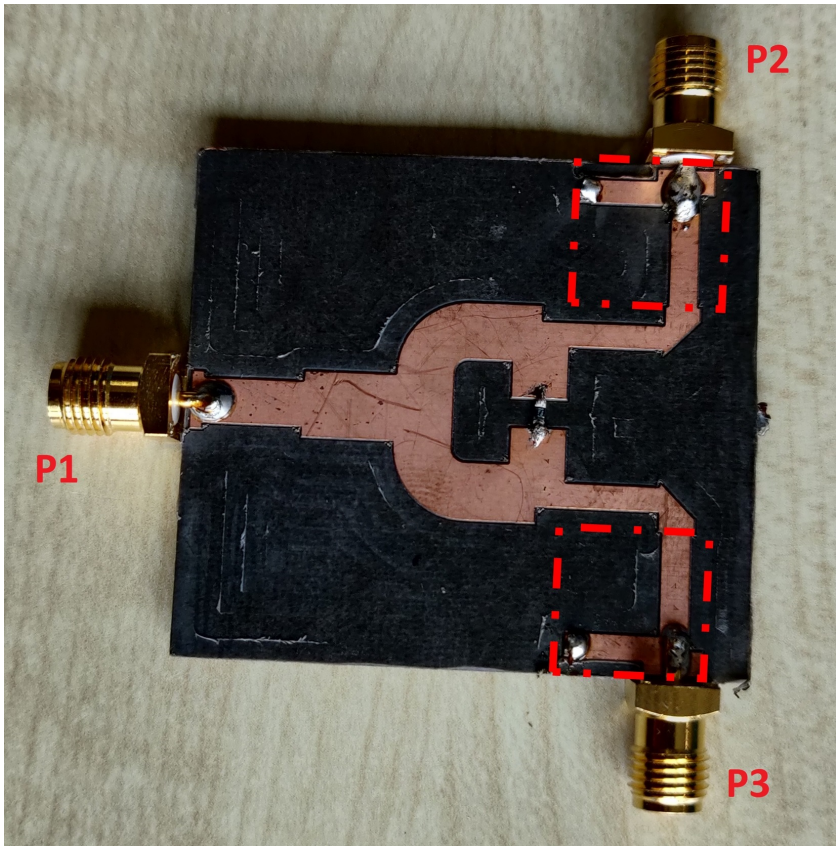


Figure 6.19: Prototype for the single-band ITPD with impedance transformers at the output ports (encircled). P1: port 1, P2: port 2, P3: port 3.

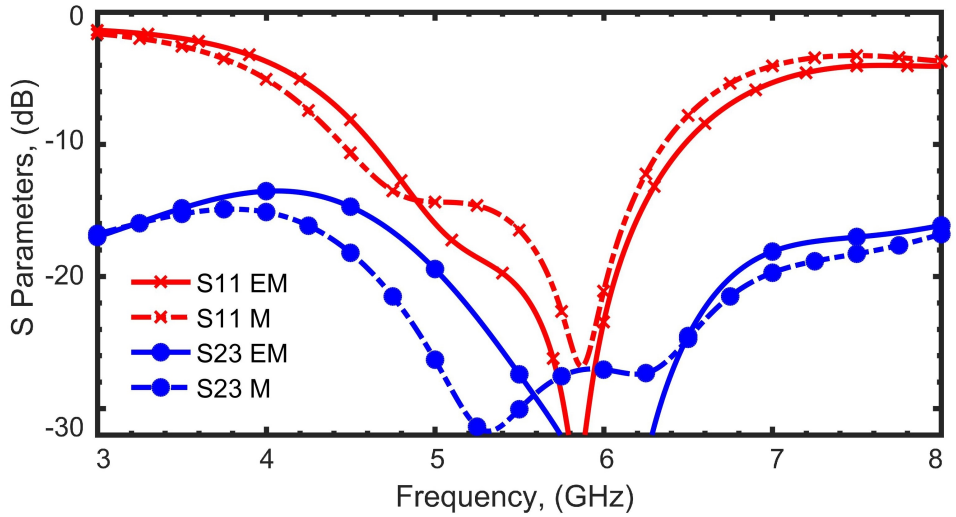


Figure 6.20: The EM simulation (EM) vs measurement results (M) for S_{11} and S_{23} of the fabricated prototype for the single-band operation.

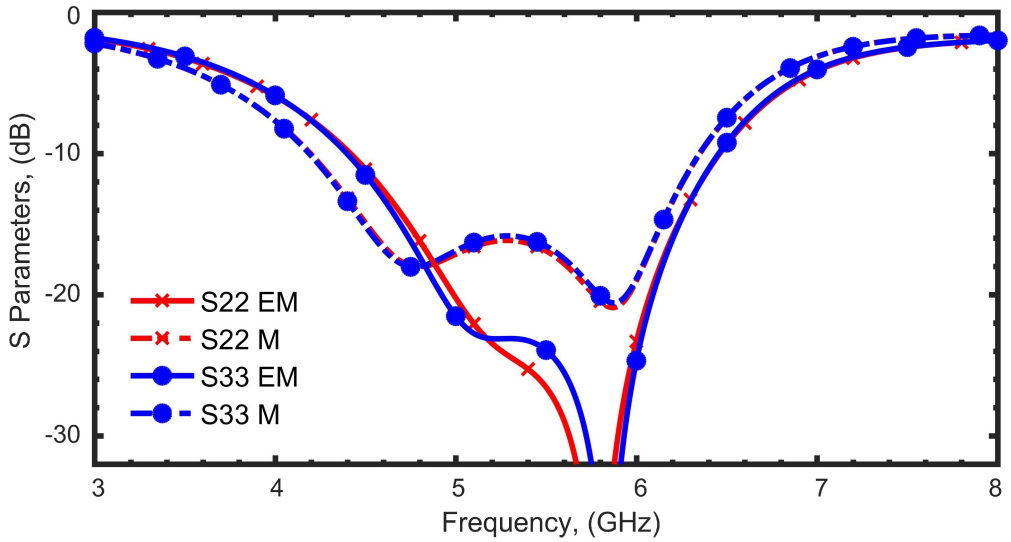


Figure 6.21: The EM simulation (EM) vs measurement results (M) for S_{22} and S_{33} of the fabricated prototype for the single-band operation.

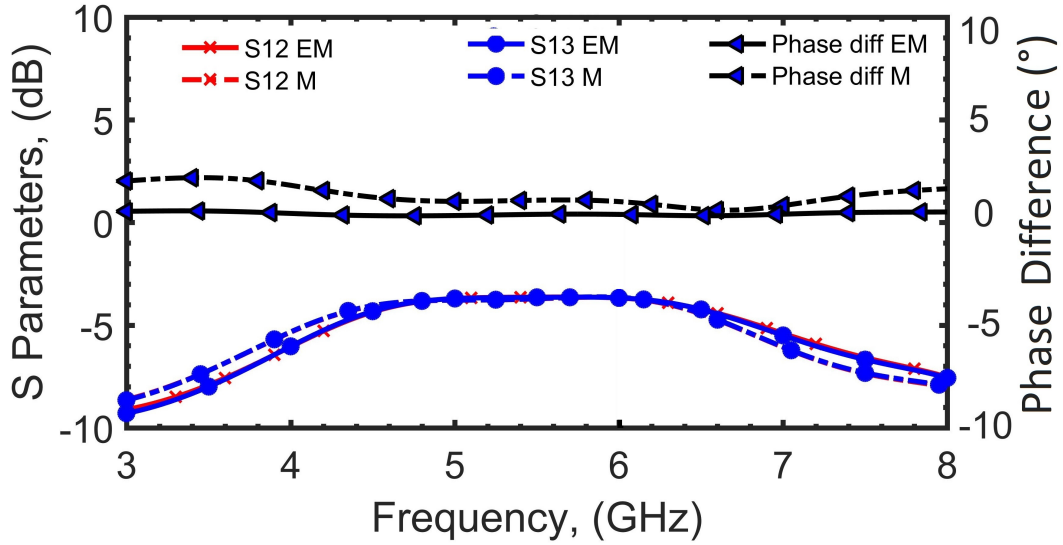


Figure 6.22: The EM simulation (EM) vs measurement results (M) for S_{12}, S_{13}, and phase difference between the output ports of the fabricated prototype for the single-band operation.

design are mentioned in case 6 of Table 6.2. The prototype is fabricated on RO5880 substrate with a substrate thickness of 1.57 mm, relative permittivity (ε_r) of 2.2 and dissipation factor ($\tan\delta$) of 0.0009. The substrate has laminates of 35 μm thick copper on both the sides. The fabricated prototype is soldered with 50 Ω isolation resistor (part no. CRCW060350R0FKEA) and is depicted in Fig. 6.19. The dimensions of the PD, without the encircled impedance

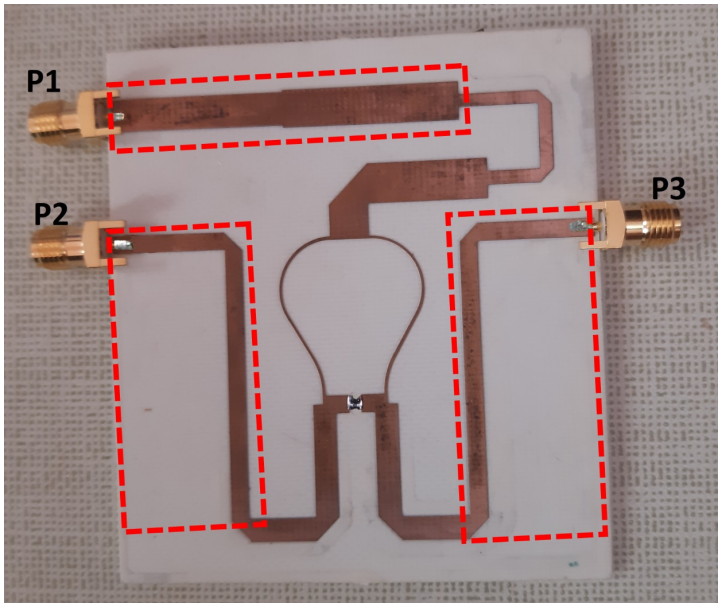


Figure 6.23: Prototype for the dual-band PD with impedance transformers at all the ports (encircled).

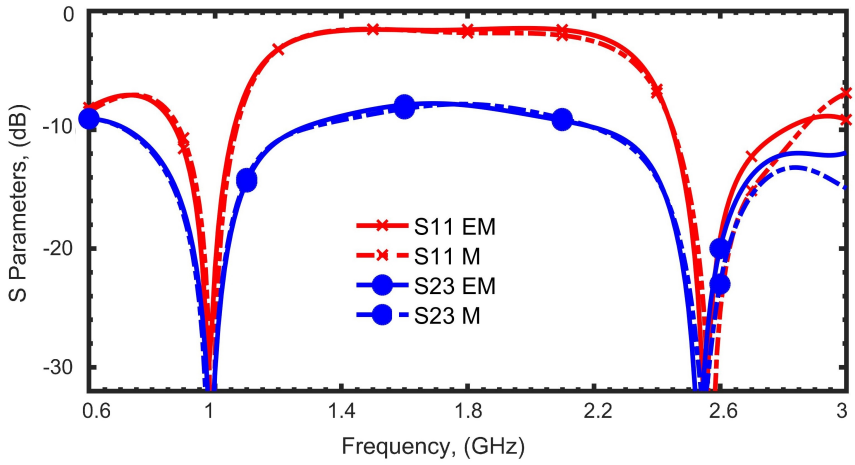


Figure 6.24: The EM simulation (EM) vs measurement results (M) for S_{11} and S_{23} of the fabricated prototype for the dual-band operation.

transformers, are 38.6 mm$\times$17.6 mm. However, an L-type impedance transformer is added at the output ports to transform the complex impedance to 50 Ω for the compatible measurement environment. Some optimizations in the design environment are done to compensate for the anomaly associated with the resistor gap, junction discontinuities, bends, etc. The measurement results of the prototype are demonstrated in Figs. 6.20, 6.21, and 6.22.

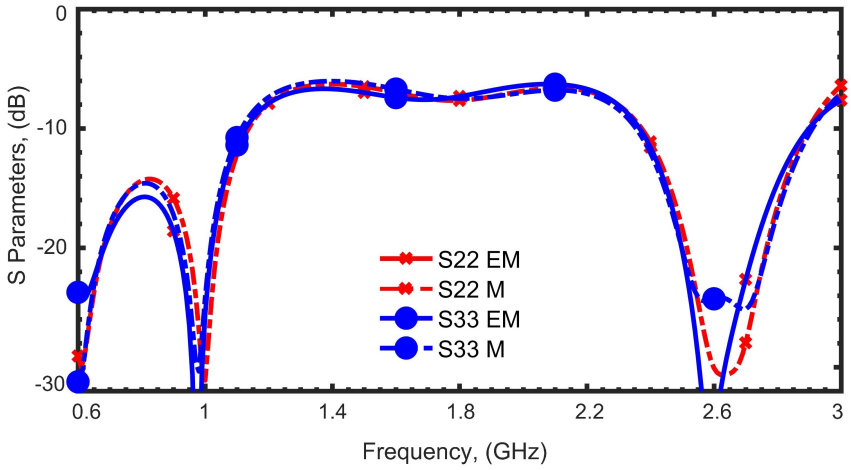


Figure 6.25: The EM simulation (EM) vs measurement results (M) for S_{22} and S_{33} of the fabricated prototype for the dual-band operation.

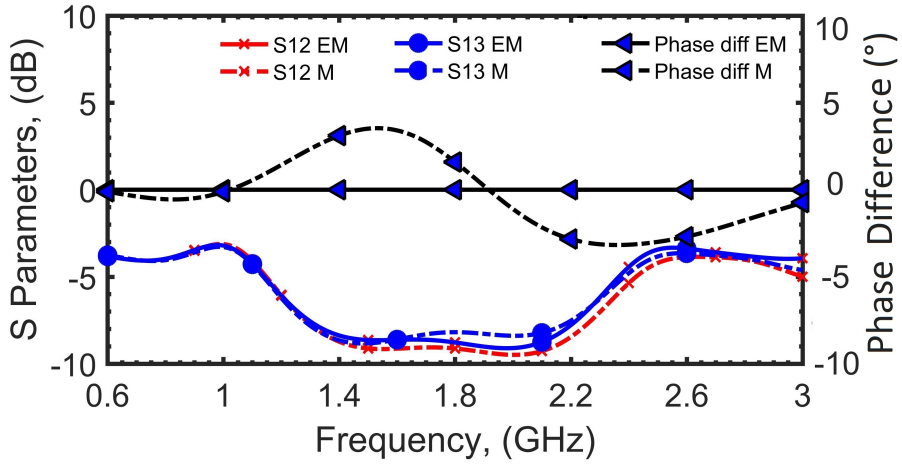


Figure 6.26: The EM simulation (EM) vs measurement results (M) for S_{12}, S_{13}, and phase difference between the output ports of the fabricated prototype for the dual-band operation.

Apparently, the measurement results (suffixed with M) and the EM simulated results (suffixed with EM) are in very good agreement. The input port matching and the isolation, as depicted in Fig. 6.20, are better than -26 dB at the design frequency. The matching at the output ports (S_{22} and S_{33}) is depicted in Fig. 6.21 and the insertion losses (S_{12} and S_{13}) and the phase difference between the two output ports are depicted in Fig. 6.22, respectively. The 3 dB fractional bandwidth (FBW) is measured to be 65.5% for the slight amplitude imbalance of 0.5 dB. For the measured bandwidth, the phase imbalance is also very good and is within the tolerance of $\pm 0.5^{\circ}$. The amplitude imbalance is the magnitude difference between the output

power at the output ports, whereas the phase imbalance is the deviation from the 0° phase difference between the output power at the output ports.

To demonstrate the effectiveness of the proposed IDPD at two arbitrary frequencies, another prototype working at 1 GHz and 2.6 GHz and, again, with FDCL port impedances of $54.14 + j8.6$@ 1 GHz and $70.7 + j5.3$@ 2.6 GHz is developed. In this case, the impedance transformation is demonstrated in the input port too, and it is fixed at 30 Ω. The calculated design parameters for this design are mentioned in case 1 of Table 6.2. The prototype is fabricated on RO4003 substrate with a substrate thickness of 1.52 mm, relative permittivity (ε_r) of 3.38 and dissipation factor ($\tan\delta$) of 0.0027. The substrate has laminates of 35 μm thick copper on both the sides. Here, the soldered resistor is a commercially available 100 Ω (part no. CRCW0603100RFKTA). Necessary optimizations are done in the design environment to compensate for the anomaly associated with the resistor, resistor gap, junction discontinuities, bends, etc. Here, the FDCL impedances at the output ports (P2 and P3) are synthesized by a combination of a micro-strip line of width 2.54 mm and length of 15.47 mm and a 50 Ω SMA connector, however, the source impedance is transformed to 50 Ω using two-section transmission lines [2]. The developed prototype is depicted in Fig. 6.23 with an overall size of 65.7 mm×61.5 mm, which includes the dimensions of the synthesized ports at the output ports and the impedance transformer at the source port. The measurement results of this dual-band prototype are depicted in Figs. 6.24, 6.25, and 6.26. The phase difference at 2.6 GHz is measured to be 2.53° which can be attributed to the soldering and fabrication losses. Ignoring this anomaly, the 3 dB fractional bandwidth (FBW) is noticeable which is measured to be greater than 60% at both the design frequencies for the slight amplitude and phase imbalance of 0.5 dB and ±0.5°, respectively.

In addition, the proposed ITPD is compared in terms of number of bands, possible impedance transformations, isolation network, the fractional bandwidth and the sizes with the recently reported PDs in Table 6.3. The proposed ITPD doesn't use any reactive element in the isolation circuit, whether for real, complex, or FDCL impedances. It can be seen that the proposed ITPD is suitable for working at both the low and high frequencies and compares favorably for both the single-band and dual-band operations. The sizes of both the fabricated prototypes, integrated with the impedance transformers at the ports, are on the lower side. It is

Table 6.3: Qualitative Comparison with State-Of-The-Art Impedance Transforming Power Dividers [R: Resistor, **15 dB bandwidth, *Not mentioned specifically, ***Calculated/estimated from provided data]

Refs	No. of bands	Impedance Transformation	Isolation Network	Operating Frequencies (GHz)	S_{11} (dB) at f_1, f_2	FBW (%) at f_1, f_2	Size (λ_g^2)
[91]	single	-	reactive	1.5	-26***	26.8**	0.023
[97]	single	real	resistor	1	-31	8	0.088
[96]	single	complex	resistive (1R only)	2.0	-29	36	0.35
[94]	single	complex	reactive	2	-17.5	16.8	0.25*
[92]	dual	-	reactive	1, 3.5	-20.0, -20.3	50**, 15**	0.023
[36]	dual	real	resistive (1R only)	1, 6.4	<-30	53, 7.3	0.087*
[173]	dual	real	resistive	1, 5	-29, -21	11, 12	0.175
[93]	dual	-	resistive	0.7, 2.6	<-15	24.3, 8.1	0.34
This Work	single	real, complex and FDCL	resistive (1R only)	5.8	-26.1	34.5	0.40
This Work	dual	real, complex and FDCL	resistive (1R only)	1, 2.6	-28.9, -27.8	18.2, 17.3	0.096

also found that the proposed ITPD has superior amplitude and phase imbalance performance over mostly published state-of-the-art designs such as [91, 93, 96, 173]. Clearly, the achievable r and k with the proposed ITPD is highest among the earlier published ITPDs, whether operating at single- or dual-band. Undoubtedly, a very high impedance transformation can be achieved for the single-band operation. In the end, the comparison of the proposed ITPD with recently published state-of-the-art PDs also reveals that there is no ITPD which can transform the FDCL loads at the two arbitrary design frequencies.

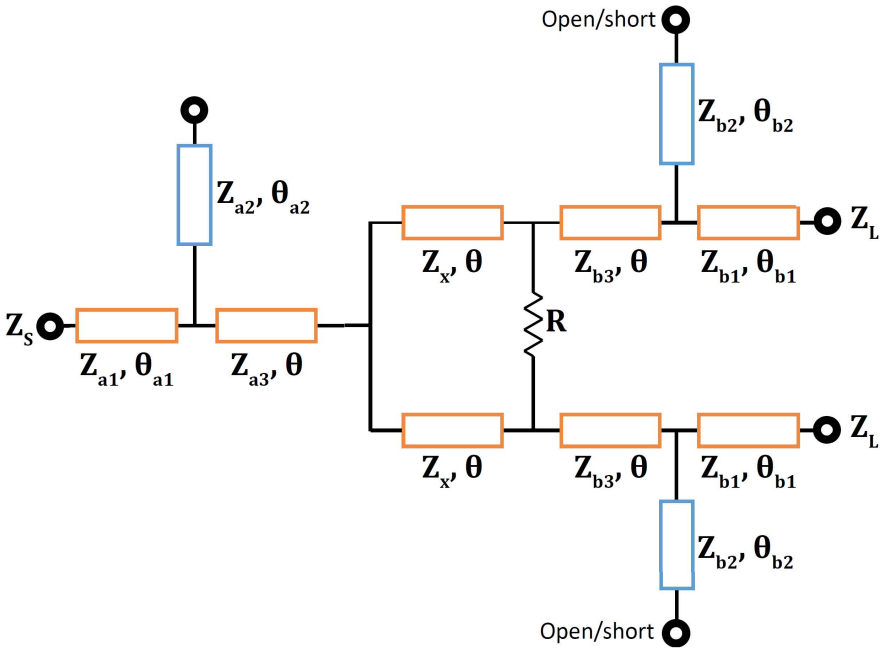


Figure 6.27: Schematics of the proposed DBITPD.

6.4 Another Configuration for Impedance Transforming Power Divider With Frequency Dependent Loads

6.4.1 Design of the Proposed Power Divider

The proposed dual-band equal PD, shown in Fig. 6.27, is a planar architecture consisting of TLs with just one lumped isolation resistor R. The characteristic impedances and electrical lengths of TLs are denoted by the corresponding Z and θ, respectively. The TLs with respective characteristic impedances Z_{a2} and Z_{b2} are either short- or open-circuited stubs. The input port (port 1) is terminated with source impedance Z_S and the output ports (ports 2 and 3) are terminated with load impedance Z_L. The impedances Z_S and Z_L are uncorrelated FDCLs at the two arbitrarily chosen design frequencies and can be defined as (6.29) and (6.30). It can now be seen that T-type structure (TTS) forms at all the three ports, and they eventually aid in creating impedance matching environment at the respective ports.

$$Z_S = \begin{cases} R_{S1} + jX_{S1} \ @f_1 \\ R_{S2} + jX_{S2} \ @f_2 \end{cases} \tag{6.29}$$

$$Z_L = \begin{cases} R_{L1} + jX_{L1} \ @f_1 \\ R_{L2} + jX_{L2} \ @f_2 \end{cases} \tag{6.30}$$

In this context, the impedance transformation capabilities of T-Type Structure are revisited for the dual-band perspective and the corresponding features to comprehend it for the DBITPD application [3]. The TTS is depicted in Fig. 6.28 for its analysis as a dual-band impedance transformer at frequencies f_1 and f_2 ($f_1 \leq f_2$). Here, port 1 has complex conjugate load (CCL) impedance, i.e., $Y_O = G_{LO} + jB_{LO}$ @f_1 and $Y_O = G_{LO} - jB_{LO}$ @f_2, and port 2 has FDCL impedance, i.e., $Y_L(Z_L) = G_{L1}(R_{L1}) + jB_{L1}(X_{L1})$ @f_1 and $Y_L = G_{L2} + jB_{L2}$ @f_2.

Here the TL, whose parameters Z_1 and θ_1 can be computed using expressions in [3], transforms the FDCL at port 2 to a CCL of Y_{X1} depicted at point X for the chosen frequencies f_1 and f_2. Subsequently, the dual-band TL segment with characteristic impedance Z_3 provides matching between the real part of the source admittance Y_O, i.e., G_{LO}, and the real part of Y_{X1} using TL theory, which translates to $G_{X1} = G_{X2}$, at the two arbitrary frequencies f_1 and f_2. The terms Y_{X2} and Y_{X1} are both CCLs with the same real parts at node X. The imaginary terms of these CCLs at node X are taken care of by the dual-band stub possessing the characteristic impedance of Z_2 and electrical length of θ_2 [3]. This stub fulfills $B_2 = -j(B_{X1} + B_{X2})$ at both design frequencies f_1 and f_2.

Furthermore, a closer look at the proposed architecture in Fig. 6.27 reveals that the proposed DBITPD is symmetric and, therefore, can be decomposed into even- and odd-mode equivalent circuits, as shown in Figs. 6.29 and 6.30, for simplifying the design analysis.

6.4.1.1 Odd-mode Design Analysis

The simplified odd-mode equivalent circuit of the proposed PD, depicted in Fig. 6.29, includes the TTS and the portion containing $R/2$ and the TL segment with parameters Z_X and θ (in red dotted box). In essence, this circuit consists of a T-network terminated with FDCL Z_L on the right side. The left side of the T-network is terminated in a CCL at node P, expressed in (6.31),

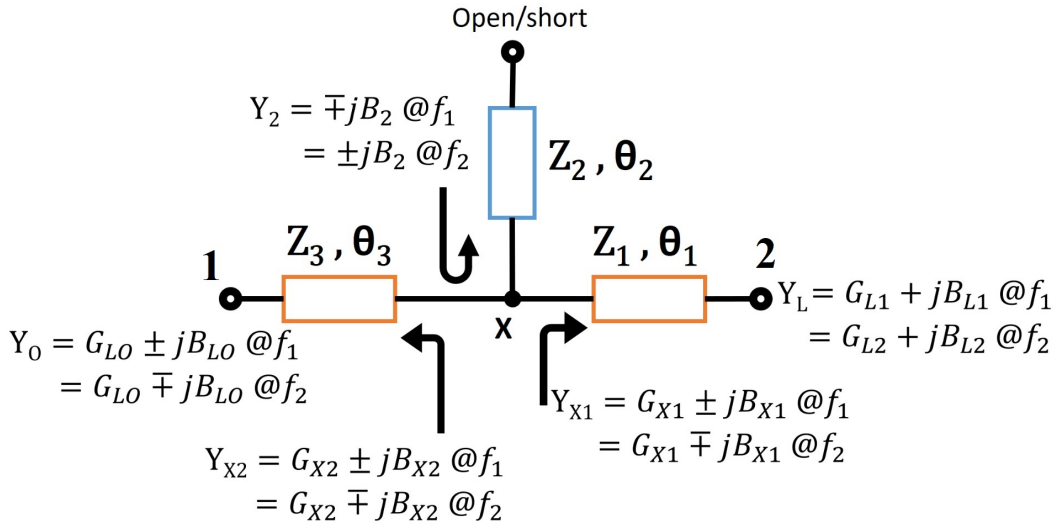


Figure 6.28: Revisited T-type structure for "FDCL to complex conjugate" impedance matching.

created by the combination of a resistor ($R/2$) and a short circuited TL (Z_X, θ). Importantly, it will be clear in the next-coming section that the term Z_X is an independent design parameter, whereas θ must follow (6.32) for dual-band operation [3]. Furthermore, the terms Z_{b1} and θ_1 in the TTS can be calculated using (6.33) and (6.34) to get a CCL, denoted as Y_m, at point Q. The TL with parameters Z_{b3} and θ transforms the real part of Y_{CCLO} in such a way that the real part of Y_n equals the real part of Y_m. Therefore, the expression of Z_{b3} can be deduced by equating the real parts of Y_m and Y_n, expressed in (6.35). Again, for dual-band functionality the electrical length θ follows (6.32), where n in an integer.

$$Y_{CCLO} = \frac{2}{R} - \frac{j}{Z_X \times tan\theta} \tag{6.31}$$

$$\theta = \frac{(1+n)\pi}{1+r} \tag{6.32}$$

$$Z_{b1} = \left[R_{L1}R_{L2} + X_{L1}X_{L2} + \frac{X_{L1}+X_{L2}}{R_{L2}-R_{L1}}(R_{L1}X_{L2} - R_{L2}X_{L1}) \right]^{\frac{1}{2}} \tag{6.33}$$

$$\theta_{b1} = \frac{n\pi + \tan^{-1}\frac{Z_1(R_{L1}-R_{L2})}{R_{L1}X_{L2}-R_{L2}X_{L1}}}{1+r}, \ n\text{: Integer} \tag{6.34}$$

$$Z_{b3} = \left[\sqrt{\frac{\mathrm{Re}\{Z_{CCLO}\}(1+\tan^2\theta)}{\mathrm{Re}\{Y_m\}} - \mathrm{Re}\{Z_{CCLO}\}^2} - \mathrm{Im}\{Z_{CCLO}\} \right] \cot\theta \tag{6.35}$$

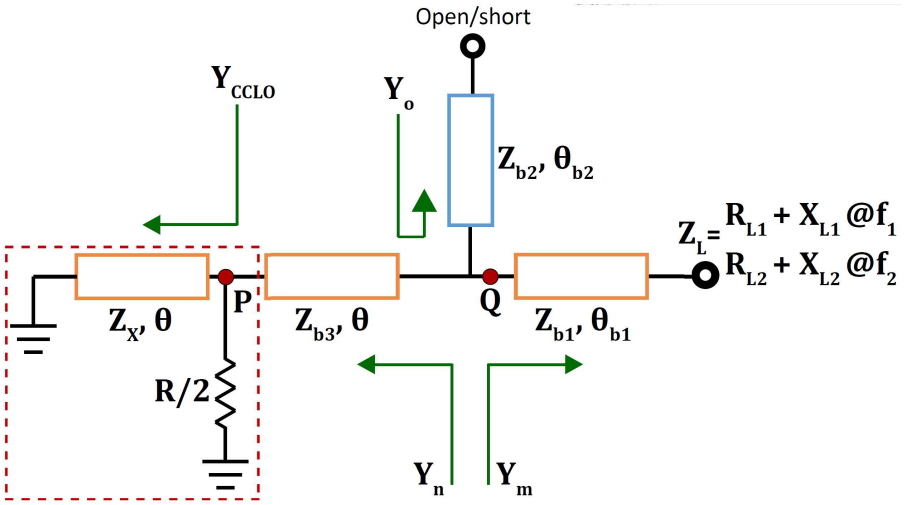


Figure 6.29: Odd-mode equivalent circuit of the DBITPD.

At this stage, the real parts are matched and the imaginary parts of Y_n and Y_m are canceled by an open-/short-circuited stub, having parameters Z_{b2} and θ_{b2}, capable of synthesizing desired susceptances at the two design frequencies. The admittance offered by the stub, Y_o, should be conjugate to the combination of imaginary parts of Y_m and Y_n. The admittance offered by the stub can be given by (6.36) and the expression of Z_{b2} is given in (6.38). Again, the electrical length θ_{b2} should follow (6.39) for its dual-band operation and cancellation of the imaginary admittance at the two different frequencies. Here, an initial value of n should be 0 for the miniaturized TL lengths and design, however, subsequent increment should be done to achieve the design parameters in the realizable range in microstrip technology [20,150] Ω.

$$\begin{aligned} Y_o &= \frac{j\tan\theta_{b2}}{Z_{b2}} \quad \text{for open condition} \\ Y_o &= -\frac{j\cot\theta_{b2}}{Z_{b2}} \quad \text{for short circuit} \end{aligned} \tag{6.36}$$

$$Y_o = -j\{\mathrm{Im}\{Y_m\} + \mathrm{Im}\{Y_n\}\} \tag{6.37}$$

$$\begin{aligned} Z_{b2} &= -\frac{\tan\theta_{b2}}{\mathrm{Im}\{Y_m\} + \mathrm{Im}\{Y_n\}} \quad \text{for open condition} \\ Z_{b2} &= \frac{\cot\theta_{b2}}{\mathrm{Im}\{Y_m\} + \mathrm{Im}\{Y_n\}} \quad \text{for short condition} \end{aligned} \tag{6.38}$$

$$\theta_{b2} = \frac{(1+n)\pi}{1+r} \tag{6.39}$$

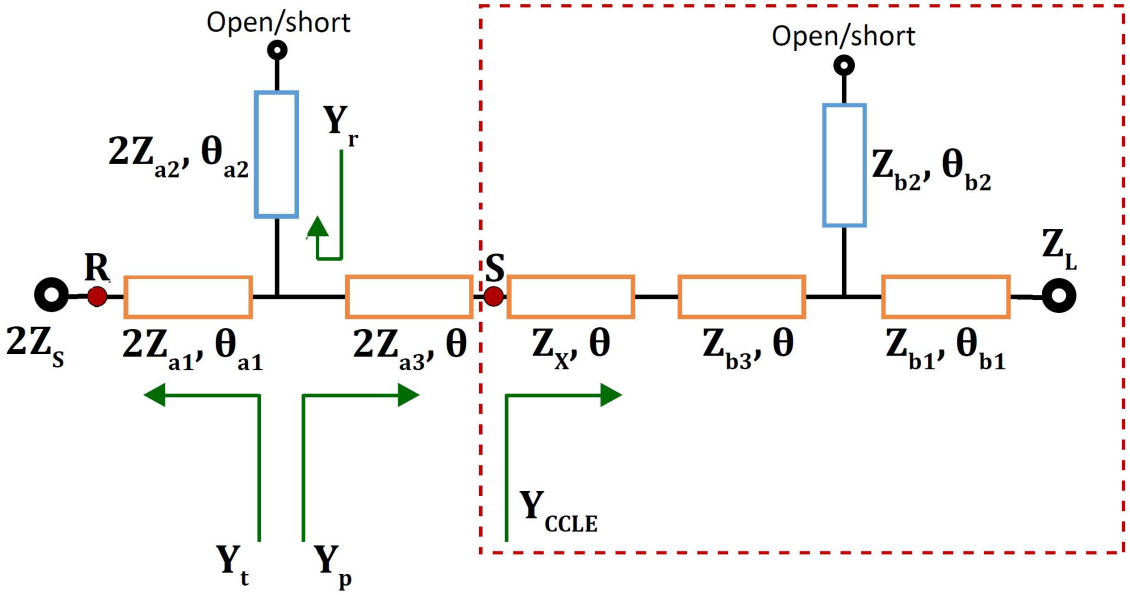


Figure 6.30: Even-mode equivalent circuit of the DBITPD.

It is interesting to note that Z_X and R are independent design parameters here. It provides the flexibility to the proposed design for the realization of design parameters Z_{b1}, Z_{b2}, and Z_{b3} as the term Y_{CCLO} can be tuned to a wide range of CCL impedances.

6.4.1.2 Even-mode Design Analysis

The even-mode equivalent circuit of the proposed PD is shown in Fig. 6.30. Again, the effective circuit includes the TTS with TL characteristic impedances $2Z_{a1}$, $2Z_{a2}$, and $2Z_{a3}$. The TTS is terminated with an FDCL of $2Z_S$ at point R, effectively. All the design parameters of the structure (inside a red dotted box) connected with the TTS at point S are known from the odd-mode analysis. It is identified from the odd-mode analysis that the term Y_{CCLE} forms a complex conjugate quantity at the two frequencies and, therefore, behaves as a CCL termination for the TTS. This effectively creates the scenario as in odd-mode analysis, and, therefore, the design parameters for the even-mode circuit given in equations (6.40)-(6.46) also have similar formulations with the appropriate changes in the design variables.

$$Z_{a1} = \left[R_{S1}R_{S2} + X_{S1}X_{S2} + \frac{X_{S1}+X_{S2}}{R_{S2}-R_{S1}}(R_{S1}X_{S2} - R_{S2}X_{S1}) \right]^{\frac{1}{2}} \tag{6.40}$$

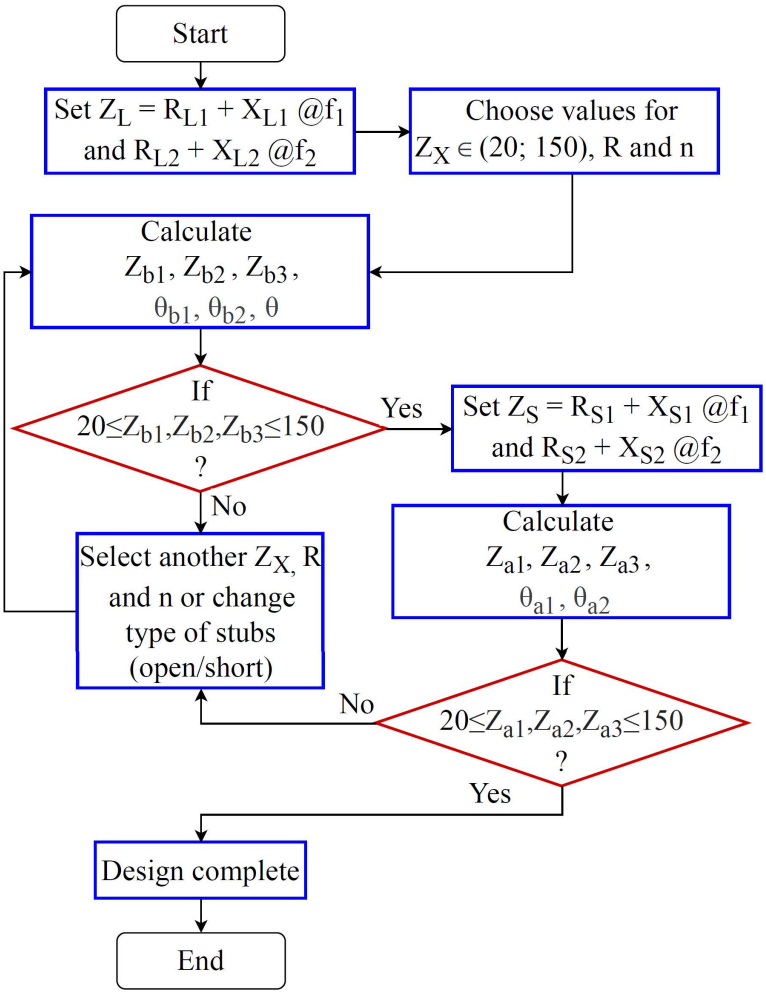


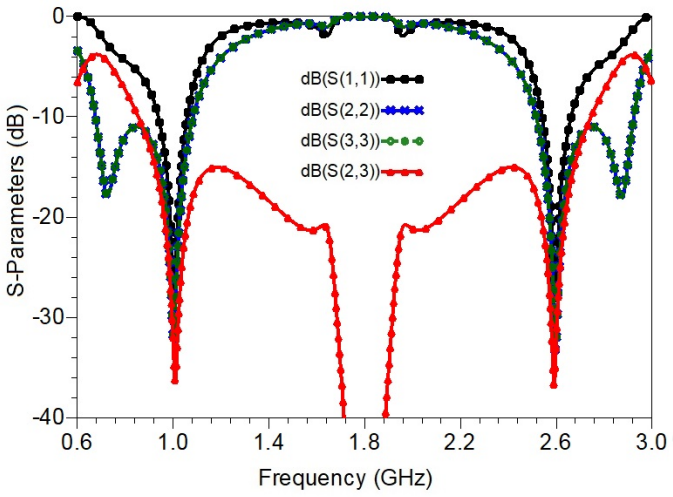
Figure 6.31: Flow chart for design of the proposed DBITPD.

$$\theta_{a1} = \frac{n\pi + \tan^{-1}\frac{Z_{a1}(R_{S1}-R_{S2})}{R_{S1}X_{S2}-R_{S2}X_{S1}}}{1+r}, n: \text{ Integer} \tag{6.41}$$

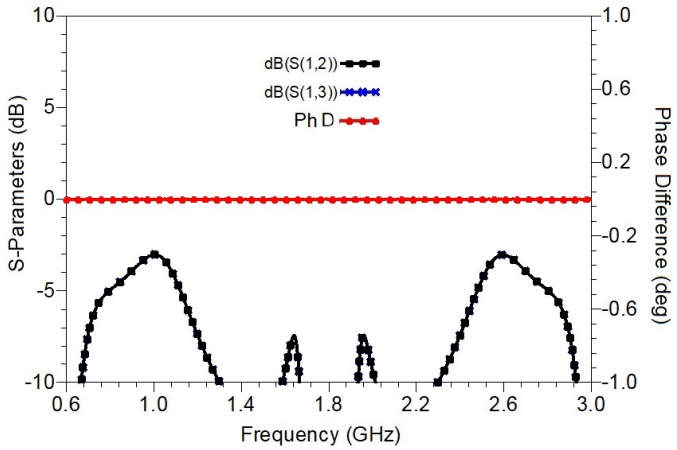
$$Z_{a3} = \left[\sqrt{\frac{\mathrm{Re}\{Z_{CCLE}\}(1+\tan^2\theta)}{\mathrm{Re}\{Y_t\}} - \mathrm{Re}\{Z_{CCLE}\}^2} - \mathrm{Im}\{Z_{CCLE}\}\right] \times \cot\theta \tag{6.42}$$

$$\begin{aligned} Y_r &= \frac{j\tan\theta_{a2}}{2Z_{a2}} \quad \text{for open condition} \\ Y_r &= -\frac{j\cot\theta_{a2}}{2Z_{a2}} \quad \text{for short circuit} \end{aligned} \tag{6.43}$$

$$Y_r = \mathrm{Im}\{Y_t\} + \mathrm{Im}\{Y_p\} \tag{6.44}$$



(a)



(b)

Figure 6.32: Calculated results for the design example (a) all port matching and isolation, and (b) insertion losses and phase difference.

$$\begin{aligned} Z_{a2} &= -\frac{\tan\theta_{a2}}{\mathrm{Im}\{Y_t\}+\mathrm{Im}\{Y_r\}} \quad \text{for open condition} \\ Z_{a2} &= +\frac{\cot\theta_{a2}}{\mathrm{Im}\{Y_t\}+\mathrm{Im}\{Y_r\}} \quad \text{for short condition} \end{aligned} \tag{6.45}$$

$$\theta_{a2} = \frac{(1+n)\pi}{1+r} \tag{6.46}$$

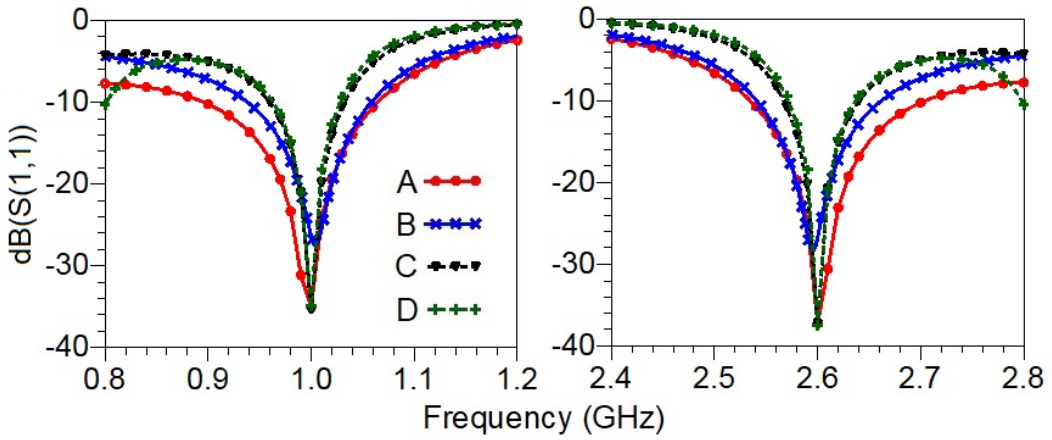
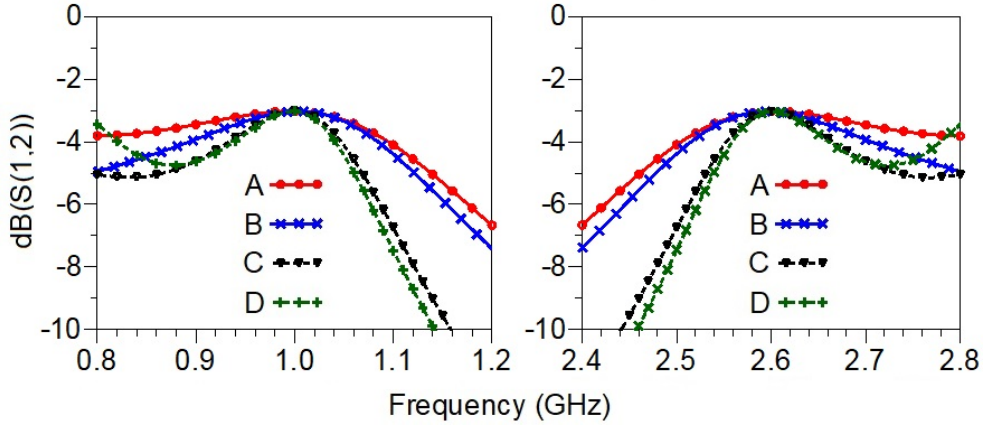


Figure 6.33: Bandwidth comparison of the proposed PD for S_{11} with different combinations of open- and short-circuited stubs. A: short-circuited stub (SCS) at source and open-circuited stub (OCS) at load, B: OCS at source and OCS at load, C: SCS at source and SCS at load, and D: OCS at source and SCS at load.

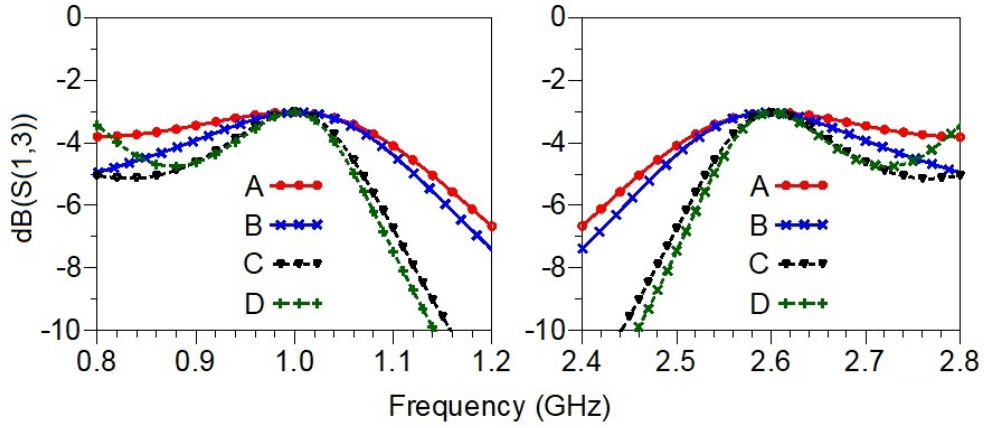
6.4.2 Design Procedure and Discussions

6.4.2.1 Design Flow Chart

The complete procedure to design the proposed DBITPD is depicted by the flow chart provided in Fig. 6.31. This design flow is explained using a design example intended for frequency of operations of 1 GHz and 2.6 GHz. The source and load impedances are assumed as $Z_S = 54.1 + j8.6$ @1 GHz / $Z_S = 70.8 + j5.2$ @2.6 GHz and $Z_L = 54.8 + j26.4$ @1 GHz / $Z_L = 93.9 + j68.3$ @2.6 GHz. Then, the parameters Z_X and R are chosen independently to be 100 Ω each to design the proposed power divider. Subsequently, the design parameters Z_{b1}, θ_{b1}, Z_{b3}, θ, Z_{b2}, and θ_{b2} are calculated as 100 Ω, 30°, 78.5 Ω, 50°, 130.5 Ω, and 50° using (6.32)-(6.35), and (6.38)-(6.39), respectively. It should be noted here that Z_{b1}, Z_{b2}, and Z_{b3} are within the realizable range. Another important point to note is that in this case an open-circuited stub with the initial value of n, i.e., n = 0 is able to provide a realizable Z_{b2}. The next step of the design according to the flow chart entails the calculation of the design parameters θ, Z_{a1}, θ_{a1}, Z_{a3}, Z_{a2}, and θ_{a2} using equations (6.32), (6.40)-(6.42), and (6.45)-(6.46), respectively. The corresponding values come out to be 60 Ω, 70°, 32.25 Ω, 50°, 65.02 Ω, and 150°, respectively. Once again, it is important to mention that an open circuited stub with $n = 3$ provides realizable Z_{a3} in this example. The other parameters Z_{a1} and Z_{a3} are within the realizable limit. This completes the design of the PD considering that all the



(a)

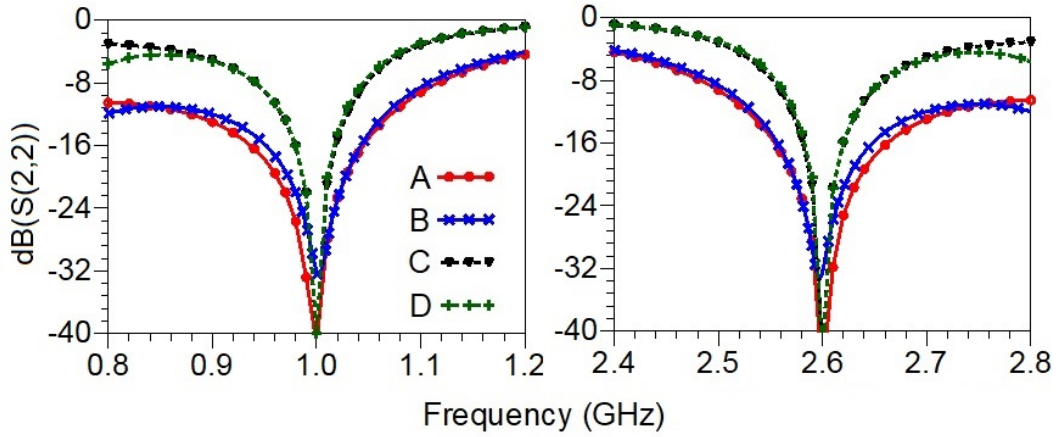


(b)

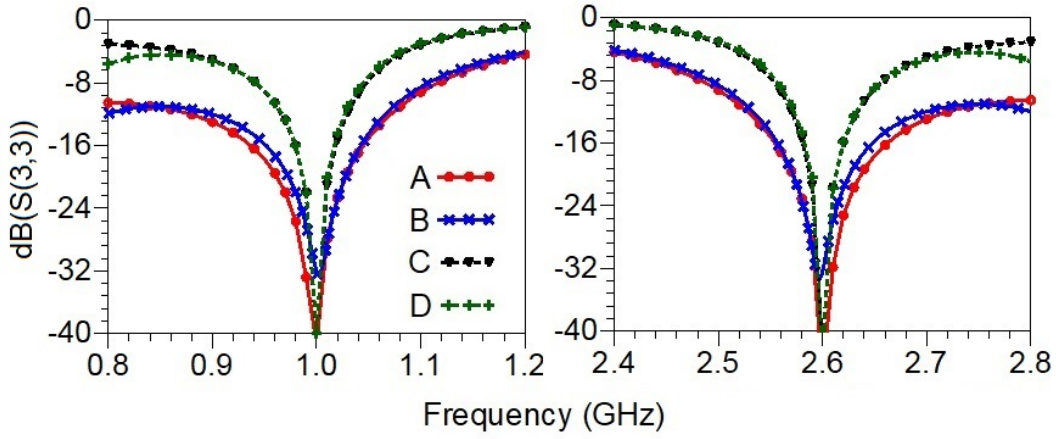
Figure 6.34: Bandwidth comparison of the proposed PD for (a) S_{12} and (b) S_{13} with different combinations of open-/short-circuited stubs. A: short-circuited stub (SCS) at source and open-circuited stub (OCS) at load, B: OCS at source and OCS at load, C: SCS at source and SCS at load, and D: OCS at source and SCS at load.

calculated design parameters are realizable and then a simulation was carried out and the achieved results are depicted in Fig. 6.32.

The plots in Fig. 6.32 provides good clarity about the performance and behavior of the dual-band PD proposed in this section. Figure 6.32(a) demonstrates that the matching at all the ports (S_{11}, S_{22}, and, S_{33}) and the isolation between the two output ports (S_{23}) of the DBITPD are achieved at the two design frequencies of 1 GHz and 2.6 GHz. In essence, the matching at the output ports is in perfect consonance, as is apparent from the fully overlapped S_{22} and S_{33}. The Fig. 6.32(b) provides the information about the output power (S_{12} and S_{13}) and the phase difference, (i.e., $\Delta\phi = \phi(S_{12}) - \phi(S_{13})$), at the two design frequencies. It can be clearly



(a)



(b)

Figure 6.35: Bandwidth comparison of the proposed PD for (a) S_{22} and (b) S_{33} with different combinations of open-/short-circuited stubs. A: short-circuited stub (SCS) at source and open-circuited stub (OCS) at load, B: OCS at source and OCS at load, C: SCS at source and SCS at load, and D: OCS at source and SCS at load.

seen that no difference exists in the magnitude of S_{21} and S_{31} and, therefore, the output power division is equal at both design frequencies. The phase difference is also maintained at 0° for a wide range of frequencies including the design frequencies. These results are a clear testament of the proposed design methodology and the design procedure for the proposed DBITPD.

6.4.2.2 Selection of Stubs for Operational Bandwidth

It is observed that the presence of the stubs can control the bandwidth performance of the PD [37], and therefore the bandwidth performance of the presented design example for all

Table 6.4: Design Examples of the Proposed DBITPD for Distinct Specifications, $f_1 = 1$ GHz, (Open): Open-circuited stub; (Short): Short-circuited stub

Design Parameters	**Case-1 (r = 2.0)**	**Case-2 (r = 2.6)**	**Case-3 (r = 3.0)**	**Case-4 (r = 3.5)**	**Case-5 (r = 6.2)**
$Z_S\Omega$ @f_1 GHz $Z_S\Omega$ @f_2 GHz	30 + j0 30 + j0	54.1 + j8.6 70.8 + j5.2	83.6 + j12.1 110 + j21.4	36.5 - j10.6 42.9 + j10.1	60.9 + j3.3 73.7 - j3.5
$Z_L\Omega$ @f_1 GHz $Z_L\Omega$ @f_2 GHz	200 + j0 200 + j0	54.8 + j26.4 93.9 + j68.3	65 + j22.3 115.9 + j53.4	153.1 + j59.5 164.7 + j50.8	141.3 + j24.8 116.6 + j26
$Z_{a1}\Omega, \theta^\circ_{a1}$	52.5, 60	60, 70	100.17, 24.97	37.3, 36.5	66.95, 33.6
$Z_{a2}\Omega, \theta^\circ_{a2}$	139.1, 60 (Short)	65, 150 (Open)	159.9, 45 (Open)	145.9, 120 (Open)	62.82, 150 (Short)
$Z_{a3}\Omega, \theta^\circ$	39.5, 60	32.25, 50	44.9, 45	20, 40	42.4, 25
$Z_x\Omega, \theta^\circ$	100, 60	100, 50	100, 45	110.8, 40	100, 25
$Z_{b1}\Omega, \theta^\circ_{b1}$	110.1, 60	100, 30	100.15, 24.97	95.5, 46.44	124.6, 35.55
$Z_{b2}\Omega, \theta^\circ_{b2}$	128.4, 60 (Short)	130.49, 50 (Open)	114.2, 45 (Open)	106.3, 160 (Open)	42.88, 25 (Open)
$Z_{b3}\Omega, \theta^\circ$	64.3, 60	78.5, 50	66.5, 45	70.4, 40	79.13, 25
$R\ \Omega$	100	100	100	185	100

the combinations of the open- or short-circuited stubs are studied. It should be noted here that the choice of open- or short-circuited stubs is limited to either the input port or the output port only and not between the two output ports (port 2 and port 3) to maintain the symmetry. Therefore, the possible configurations are short-circuited stub at the source and open-circuited stub at the load (case-A), open-circuited stub at the source and open-circuited stub at the load (case-B), short-circuited stub at the source and short-circuited stub at the load (case-C), and open-circuited stub at the source and short-circuited stub at the load (case-D). The calculated results of the presented design example with all the four cases are demonstrated in Figs. 6.33, 6.34, and 6.35, where A, B, C, and D are indicated for their respective cases. The bandwidth performance of the proposed DBITPD for case-A (Fractional bandwidth (FBW) of approx. 17%) is more than double in comparison to case-D (FBW of approx. 7%). It is important to note that the bandwidth performance of the DBITPD at these combinations of stubs may also vary depending on the type of FDCLs, CCLs, or real impedances and its variation over the frequency ranges.

6.4.2.3 Design Examples

To further assess the effectiveness of the proposed architecture, five distinct design examples, including the design example discussed in the previous section, are considered. The corresponding design parameters are given in Table 6.4. The design examples demonstrate the cases with high impedance transformation at high frequency ratios of $r = 2$, $r = 2.6$, $r = 3.0$, $r = 3.5$, and $r = 6.2$. It is apparent from Table 6.4 that all the design parameters are realizable in the microstrip technology. A very high impedance transformation of 6.6 is presented in case-1. This case also demonstrate the effectiveness of the proposed ITPD for the real impedances. The design examples of case-2 to case-5 are presented for the arbitrary FDCL port impedances at the arbitrary frequency ratios. The design flexibility of the proposed ITPD is demonstrated by designing a PD at concurrent high impedance transformation (a maximum ratio of 2.32 for the real parts and 7.43 for the imaginary parts of Z_L and Z_L) and high frequency ratio of 6.2 in case-5. The return loss performance of all the design examples is also depicted in Fig. 6.36 to validate the working of the proposed ITPD at these arbitrary port impedances and frequency ratios. These examples demonstrate the versatility of the proposed design technique and validate that the functionality is suitable for a wide range of design specifications.

6.4.3 Prototype and Experimental Results

To experimentally verify the proposed design technique, a micro-strip prototype of the design examples is fabricated on RT/Duroid 5880 substrate. The substrate has the thickness of 1.58 mm, relative permittivity (ε_r) of 2.2 and dissipation factor ($\tan\delta$) of 0.0009. The substrate is laminated with 35 μm thick copper on both the sides of the substrate. As per the specifications, the FDCL impedances at all three ports are synthesized using the combination of a TL and 50 Ω SMA connector individually. The source termination Z_S is synthesized by a combination of a micro-strip line of width 3.6 mm and length of 18.4 mm and a 50 Ω SMA connector. The load termination Z_L is synthesized by a combination of a micro-strip line of width 1.4 mm and length of 12.6 mm and a 50 Ω SMA connector. The layout, including these synthesized ports, is simulated in Keysight ADS and the optimizations are done to compensate for the anomaly associated with the resistor, resistor gap, junction discontinuities, bends, etc. The layout of the

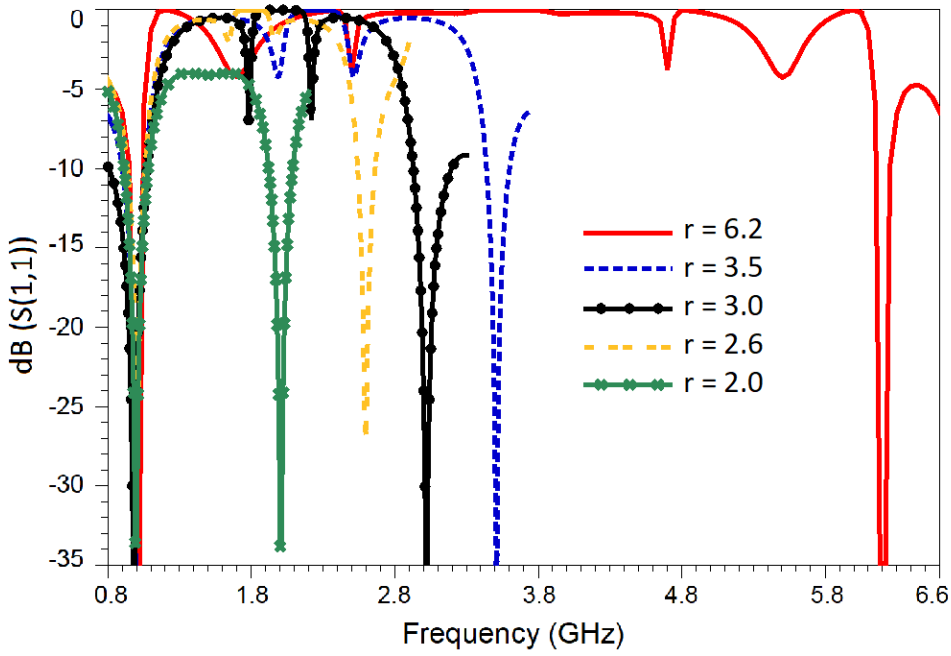


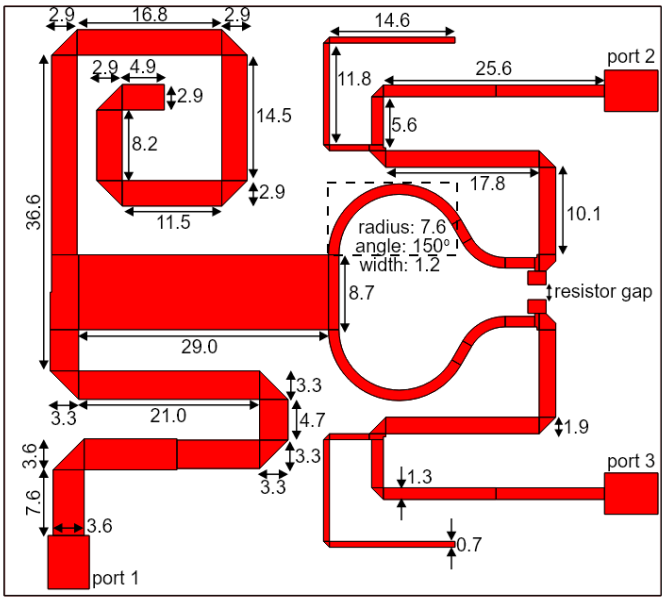
Figure 6.36: Calculated return loss of the design cases.

Table 6.5: Measurement Results of the Fabricated Prototype

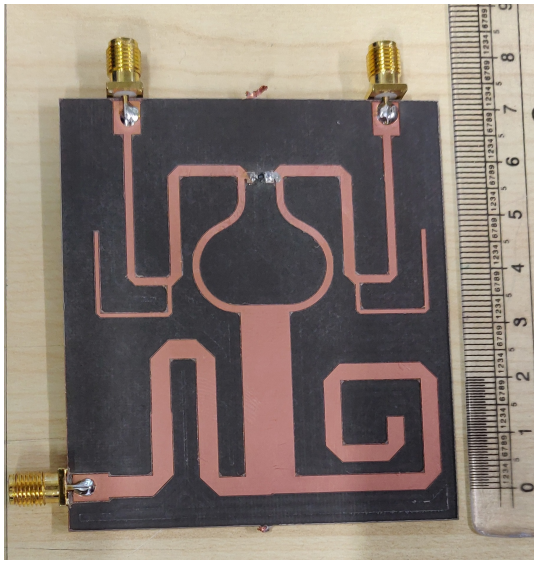
Measure	1 GHz	2.6 GHz	Measure	1 GHz	2.6 GHz
S_{11} (dB)	-46.7	-18.0	S_{23} (dB)	-25.1	-23.8
S_{22} (dB)	-27.6	-22.0	S_{33} (dB)	-27.2	-22.8
S_{21} (dB)	-3.6	-3.9	S_{31} (dB)	-3.4	-3.9
$\Delta\phi$ (°)	-0.3	0.4	FBW	16%	13.1%

fabricated PD with the details on dimensions is depicted in Fig. 6.37 with an overall size of 64.9 mm $\times$ 69.6 mm, which includes the dimensions of the synthesized ports. The fabricated prototype with the soldered 100 Ω isolation resistor (part no. CRCW0603100RFKTA) is shown in Fig. 6.37(b).

The fabricated prototype is evaluated using a Keysight vector network analyzer, and the measurement results are compared with the EM simulated result in Fig. 6.38. Apparently, the measurement results (suffixed with M) and the EM simulated results (suffixed with E) are in very good agreement. The impedance matching at all the ports and the isolation between the two output ports of the PD are depicted in Fig. 6.38(a), whereas the insertion loss at the two output ports and the phase difference between the two output ports are depicted in Fig.



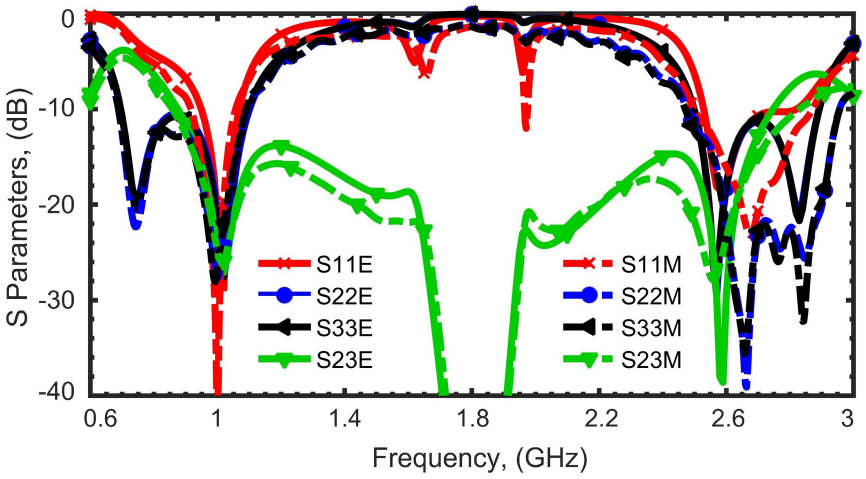
(a)



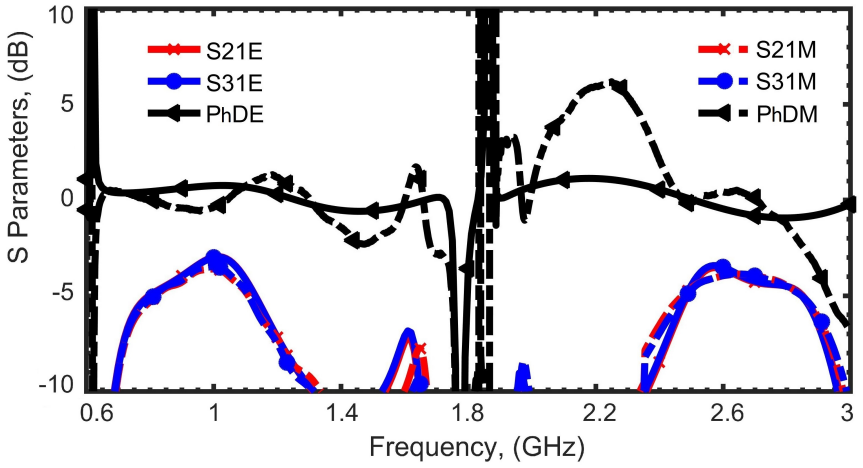
(b)

Figure 6.37: (a) Layout design (all dimensions in mm) (b) Prototype of DBITPD on RO5880 Substrate

6.38(b). The measurement results at the design frequencies are listed in Table 6.5. It can be seen that the excellent matching response at the output ports is better than -27 dB at the design frequencies. Furthermore, the matching at the input port and the isolation between the output ports are also very good and better than -25 dB at both the design frequencies with a slight frequency shift due to the soldering and fabrication losses. The phase difference



(a)



(b)

Figure 6.38: Comparison of the measured and simulated results for proposed DBITPD (a) All ports matching and isolation between output ports, (b) insertion loss and phase difference.

is also measured to be in good agreement with a tolerance of ± 0.5 dB for the operational bandwidth of the PD. It is pertinent to note that the proposed design also achieves a decent bandwidth performance for applications in antenna feeding networks, amplifiers, wireless receivers, etc [45, 125, 174–176]. The respective measured overall FBW for the proposed DBITPD are 16% at 1 GHz (0.91 GHz-1.07 GHz) and 13.1% at 2.6 GHz (2.49 GHz-2.84 GHz). These bandwidth specifications are appropriate for a wide range of applications in modern wireless/industrial electronics working at several IEEE wireless communication standards such

Table 6.6: Qualitative Comparison with State-Of-The-Art Impedance Transforming Power Dividers [R: Resistor, NP: Not Provided, *Single-band designs, **size including synthesized ports, ***Calculated/estimated from provided data.]

Refs.	**No. of bands**	**Impedance Transfor -mation**	**Isolation Network**	**Size** (λ_g^2)	**FBW** (%) @f_1,f_2
[94]	single	complex	reactive	0.25***	16.8*
[96]	single	complex	resistive (1R only)	0.35	36*
[93]	dual	No	resistive (1R only)	0.34	24.3, 8
[36]	dual	real	resistive (1R only)	0.087***	53, 7.3
[45]	dual	real	reactive	0.36***	11.9, 5.9
[173]	dual	real	resistive (1R only)	0.175**	11, 12
This Work	dual	real, complex and FDCL	resistive (1R only)	0.106**	16, 13.1

as 802.11a/b/j/p/y/g/n/ac/ax, 802.16a (Superseded), P802.16.2a, Wireless Body Area Network (WBAN), and FR-1 bands of 5G applications.

Subsequently, to highlight the uniqueness and novelty of the proposed design, a comparison with the existing state-of-the-art is made. Table III includes a number of commonly used metrics for comparative analysis within the context of DBITPDs and recently reported ITPDs. The reports with no information on an attribute are marked as "Not Provided" in the respective columns. Furthermore, the reports [39, 125] with no information about isolation between the two output ports have "Absent" marked in the respective columns.

For example, a thorough design and analysis of an ITPD are reported in [96]. It achieves a very good FBW but possesses a larger size and operates only at a single band. The DBITPDs reported in [7, 125] achieve a FBW of 10%-30%. However, the FBW of 10% is achieved for the designs exhibiting impedance transformations at two distinct bands. The design report [94] is studied a DBITPD with a complex isolation network for the FDCL terminations at the output ports. However, it uses either real loads or frequency-dependent loads at the input port. In general, there has been only one report of dual-band PD, which includes the impedance transformation for frequency-dependent loads [39]. However, this report provides a design

example without thorough analysis, case studies, isolation features, etc. On the other hand, our proposed DBITPD with FDCL terminations at the source and load ports uses just one isolation resistor and achieves superior performance over the reported impedance transforming PD techniques. The sizes of fabricated prototypes are also compared, and the proposed DBITPD is a miniaturized architecture while providing a wide range of inherent impedance transformations at two arbitrary frequencies. Although the fabricated PD demonstrates very good measurement performance, the performance comparison is not provided due to the unavailability of any other dual-band complex impedance transforming PDs in the literature. Finally, it is safe to mention that the proposed DBITPD advances the state-of-the-art significantly.

6.4.4 Further Discussions

The proposed PD is capable of providing high frequency ratios with inherent high impedance transformation for arbitrarily real, complex, and FDCL port impedances. It is well known that the designs on micro-strip technology face challenges when it comes to its realization on a printed circuited board. Still, the proposed DBITPD facilitate a wide range of port terminations except for the limitations with regards to handling Z_{b1} and/or Z_{a1} in terms of the concerned TL dimensions for realizability [3]. However, this constraint related to Z_{b1} and/or Z_{a1} can be overcome by employing the load healing technique [57]. Furthermore, it is pertinent to note that the design flexibility of the proposed PD makes it very convenient for achieving higher frequency ratios due to the independent choice of n in (6.39) and (6.46). Finally, the excellent design flexibility of the proposed DBITPD makes it a good candidate for exploring the unequal and controlled power division at the two arbitrary frequencies in future research works.

6.5 Conclusion

The arbitrary impedance environments of the RF and Microwave circuits and in between the interconnects of the WCS has been considered in this Chapter. The multi-functional components, power divider, for example, capable of handling real, complex, and frequency dependent complex impedances at all of its ports are discussed. A thorough study and investigation of the

generalized ITPD structures for single- and dual-band operations have been reported in this Chapter. The unique part of the investigation includes a detailed discussion on the versatility of impedances at the ports for a wide range of arbitrary r and k. The design procedure of the reported ITPD exhibits independent design parameters, which make the design scheme very flexible for the inherent impedance transformation while it comes to attribute the arbitrary varying impedance environments at all the ports. To demonstrate the effectiveness of the proposed architectures, several case studies have been provided with varying r and k at different design conditions. The prototypes have also been fabricated for both the single-band and dual-band operations. The agreement between the simulation and measurement results has demonstrated the effectiveness of the proposed circuits and the corresponding design procedures. In the end, the qualitative features of the power dividers are compared with some of the recently published impedance transforming PDs. The dual-band frequency-dependent complex impedance transforming PD with thorough design analysis is reported for the first time. The superior features of the prototypes demonstrate a significant contribution to the domain of advanced ITPD configurations.

Chapter 7

Conclusion and Future Prospects

7.1 Conclusion

The existing and evolving multi-faceted wireless communication system is the core of the almost all the applications in human life, such as advanced mobile communications, satellite communications, internet services, WiFi, IoT networks, digital health, wireless power transfer, etc. [5, 8–31]. It would not be exaggerating to say that ***wireless communication system is everywhere*** nowadays, and it is hard to think of life without this. However, this is also augmenting the challenging prospects on the designers' front for the development of the compatible RF/Microwave components, devices, and systems. Though the rapid developments on 5G and beyond 5G standards making it challenging to develop the wideband architecture and components for the high data rates, the confront with the alternative solutions on multi-frequency components is also significant to handle the ever-growing multi-standard communication system. Also, the size of the components and systems and the power consumption are the major issues that plays an important role in the design and development of the WCS.

To provide the solution to such issues, the contributions of this thesis provide extensive work to support the reduction of size and power consumption for the RF/Microwave circuits and systems. The proposed work not only provides the design solutions to the existing infrastructure but also to the future 5G wireless systems considering the co-existing infrastructural developments. All the contributions can be majorly classified into three categories, namely the design and development of single- and dual-band multi-functional components, strategic design

analysis for the enhanced design flexibility and re-configurability, and simplified architectures with the systematic design methodology for the design and development of the multi-functional and re-configurable single- and dual-band architectures.

The need for the impedance transformation, due to its omnipresence, is well explained in the thesis. It has been the utmost importance to have arbitrary impedance transformations for the interconnects and components integrated in an arbitrary impedance environment. Two different ultra-high impedance transformers are provided in Chapter 4. An analytical methodology for designing a dual-band high impedance transformer is provided. The enhanced design flexibility is also demonstrated through the design examples to validate the high microstrip compatibility to match the arbitrary real impedances at two uncorrelated frequencies with a high frequency ratio. The application of the impedance transformers is also demonstrated in the proposed dual-band power divider architecture and its measurement results. The role of impedance transformation is clearly highlighted in the strategic design analysis of the power divider.

This concept of impedance transformation encourages the design and development of the components which are capable of providing inherent impedance transformation. This is due to the fact that these RF/Microwave components need to be connected with each other to complete the front-end subsystem of a WCS. The interconnects (impedance transformers here) can easily be removed if the component itself exhibits the required impedance transformations. Furthermore, the same concept has been extended for the other features and subsequently, the multi-functional RF components have been proposed. The overall contributions of the multi-functional components are much higher as the proposed components are not only providing the inherent impedance transformation but also more features. It can be easily understood that more inherent features provide more advantages in terms of the reduction of the size and power consumption of the overall communication system. A simplified design scheme of a new three-section dual-band impedance transformer with DC isolation, a power divider with balanced to unbalanced signal transformation has been provided in Chapter 5. A detailed mathematical analysis along with a number of case studies demonstrate the effectiveness of the proposed techniques. The development of multi-functional features has been further improvised with the multi-functional performance at two arbitrary frequencies simultaneously. For example, a dual-band component with equal power division at the two output ports along

with inherent DC blocking and inherent impedance transformation has been proposed and explained. The Chapter has investigated the multi-functional operations from power divider and balun circuits for different attributes, which includes the high impedance transformation and high frequency ratios. The concurrent impedance transformation at high frequency ratios has also been investigated. For this, the additional degree of freedom in terms of independent design parameters have been analyzed for the flexible design characteristics. The proposed design eventually eliminates the need for an impedance transformer at both the input and output ports while possessing inherent impedance transformation and thus reducing the overall size of any communication system. Several design examples are provided to demonstrate the range of all the design parameters within the realizable limit for a wide range of r and k. Another advantage of the designs is the minimal use of lumped components to make these components capable of high frequency operations. The proposed design has also been compared with the state-of-the-art techniques and the advantages in the form of achievable r and k are apparent. The proposed design techniques have been experimentally validated with the prototypes in the microstrip technology, and a good agreement between measured and EM simulated is a testament to that. A direct application of the proposed components is in the RF energy harvesting system and on-chip antennas, where wide range of ITR could be extremely beneficial.

To the end, the thesis has also covered the aspects where the impedance at the ports of RF/Microwave components can be arbitrary in nature. The need for the real, complex, and frequency-dependent complex impedances is well investigated and correspondingly, the multi-functional dual-band components with arbitrary ports have been proposed in Chapter 6. It should be noted that the proposed architectures can handle the arbitrary impedances at both the source and load ports simultaneously. More importantly, such components with inherent FDCL impedances at the two arbitrary frequencies are provided for the first time. A thorough study and investigation of the generalized impedance transforming power dividers for single- and dual-band operations have been reported in this thesis. The design procedure of the reported ITPD exhibits independent design parameters, which make the design scheme very flexible for the inherent impedance transformation. To demonstrate the effectiveness of the proposed ITPD, several case studies have been provided with varying r and k at different design conditions.

Table 7.1: Accomplished Achievements w.r.t. Two Major Attributes r and k

Publication	Component	Maximum r	Maximum k
C[7]- APMC 2017	Impedance Transformer	7	>10
C[4]- APMC 2019	Impedance Transformer	1 <r <10	1<ZL<500, ZL>500 for lower r
J[2]- Access 2020	Impedance Transformer	20	20
C[6]- IMaRC 2018	Components (Power Divider)	4.7	NA
J[4]- MOTL 2018	Components (Balun)	NA	0.1-10.0
C[3]- APMC 2019	Components (Power Divider)	NA	10 (Also Complex Impedances)
J[3]- PIER 2019	Components (Balun)	3.5	0.4 – 4.0
C[5]- IMaRC2018	Components (Power Divider)	3	50
C[2]- EUMW 2020	Components (Balun)	<5 2 4	<7 10 9
J[1]- TCAS II 2020	Components (Balun)	>6.1 for higher θ	>20
UR[2]	Components (Power Divider)	>5.8	>10
UR[1]	Components (Power Divider)	7	10

Based on the proposed design procedures, different prototypes have also been fabricated and the design techniques have been validated. The superior features of the prototypes demonstrate a significant contribution to the domain of advanced ITPD configurations. The successful validation demonstrates the potential to fill the void in the state-of-the-art designs for arbitrary port impedance.

7.2 Summary of the Contributions

The summary of the accomplishments of the thesis are listed below in brief.

- Ultra-high frequency ratios are accomplished.
- Ultra-high impedance transformation ratios are achieved.
- Numerous multi-function architectures are proposed.
- Concurrent k and r of more than 10 is achieved for several components.
- For the first time, Dual-band impedance transforming power dividers with FDCL loads at both the source and load ports are proposed.
- Simplified architecture is a key feature for all the proposed architectures.
- Systematic analytical solutions with closed-form design equations are provided.
- To provide the systematic design flow chart to enable quick prototyping.
- High design flexibility is attained.

7.3 Future Prospects

The reported work in this thesis addresses many existing limitations and advances the state-of-the-art to mitigate the limited frequency ratios and impedance transformation ratios for the arbitrary nature of varying impedance environment. While a large number of design scenarios have been considered, the outcome of this thesis opens the doors to future research problems that are worth to be investigated and addressed. Some of the possible future research directions can be listed as follows:

7.3.1 Empowering Multi-functional Features for Heterogeneous Communication System

The thesis presents several multi-functional components however, it is always better to achieve more inherent features. For example, filtering is another very important component in a communication system that can be integrated with the performance of the multi-functional components presented in the thesis. For the ever-advancing heterogeneous communication

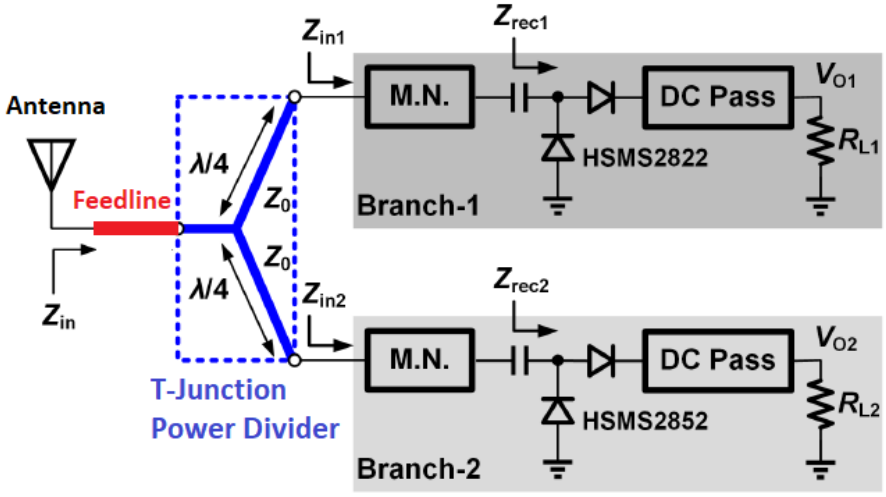


Figure 7.1: A rectenna receiver subsystem [5]

system, the concurrent operation at multiple frequencies is a necessity therefore, the work of the thesis can also be extended for multi-band components where the number of operating frequencies are more than two. Moreover, group delay considerations can also be evaluated for the efficient performance of a co-designed communication system.

For the example purpose, an illustration is provided in Fig. 7.1, where the complete circuit along with the receiver antenna can be fabricated on a single PCB. With single PCB fabrication and utilization of an impedance transforming power divider (one of the contributions of this thesis), the feedline and M.N. (matching networks) can be eliminated from the subsystem.

7.3.2 Suppression of Spurious Stop-Band Signals

The thesis has highlighted the frequency separation for the dual-band circuits and provides the architecture with high frequency ratios. However, it must be noted that the high frequency separation can have significant spurious transmission bands due to the resonance created by the segments of the design architecture. Some of these spikes may be comparable to the return loss performance at the operational bands. Therefore, the suppression of these spurious bands could be a significant improvement [177–179].

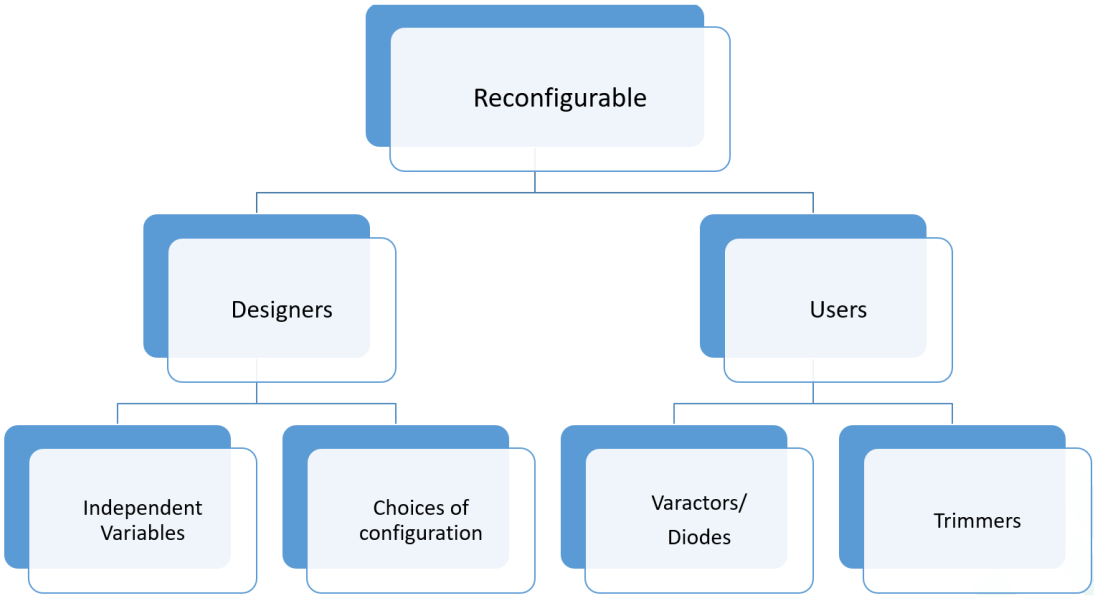


Figure 7.2: View on reconfigurability

7.3.3 Single PCB Solutions

Considering the progress in WCS and integration of its circuits and subsystems, the improvement on conventional approach of developing independent components is much highlighted in the thesis. Most of the contributions are specifically providing the solutions to the size reduction of the WCS with design and development on multi-functional components, i.e., by inheriting the multiple features and removal of redundant components. The same approach has gained much significance and the immediate and tremendous need in search for disruptive solutions are widely discussed in recent times. The future prospects can, therefore, be the development of co-design schemes for the unified PCB solutions cohabitating the active and passive components including the antennas.

7.3.4 Cost-Effective Solutions: A Reconfigurability Prospect

With the reported work on the development of single- and dual-band multi-functional components, this thesis contributes to the reduction of size and power consumption, which in-turn is a cost-effective solution. The additional figure of merit is reconfigurability and tunability of the components for cost-effectiveness. The reconfigurability of the RF/Microwave components, as

depicted in Fig. 7.2, can be classified in two ways, i.e., from either *designers* or *users* point of view. The work reported in this thesis majorly discusses the reconfigurability from the designers' point of view. For example, based on the design specifications, a designer can use the available independent design parameters and choice of the open- or short-circuited stubs to obtain the realizable design parameters. However, as a future prospect, the solutions can be developed to provide the re-configurability from the users' point of view. For example, the usage of trimmers and varactors enables the circuits where a user can tune the circuit performance for the desired frequency, bandwidth, performance, etc.

7.3.5 Millimeter-wave Circuits and Systems

With all of these possible future directions, the requirement of wideband circuits and components catering to 5G and beyond 5G standards can not be ignored. It should also be noted that the PCB based solutions may not be able to provide the solutions at the higher frequency bands of 5G standards due to high substrate losses at high frequencies. It is therefore important to develop these multi-functional unified solutions on the high -frequency high-bandwidth compatible technologies. The Substrate Integrated Waveguides (SIW) and mm-wave Monolithic microwave integrated circuit (mm-MMIC) are the examples of those technologies, though the fabrication challenges may increase. Moreover, the development backed by the analytical solutions would prove to be of paramount importance.

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