Nanoscale Tunnel Field-Effect Transistors for Digital Circuit Applications: Design and Analysis

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By

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Certificate

This is to certify that the thesis titled "***Nanoscale Tunnel Field-Effect Transistors for Digital Circuit Applications: Design and Analysis***" being submitted by ***Shelly Garg*** to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of Doctor of Philosophy, is an original research work carried out by her under my supervision. In my opinion, the thesis has reached the standard fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree or diploma.

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Abstract

Metal–oxide–semiconductor field-effect transistor (MOSFET) has been used for decades in the semiconductor industry. However, with the continuous downscaling of the device dimensions to the nanometer regime, conventional MOSFETs have reached a fundamental physical limit that restricts the subthreshold swing of the device to $\geq 60\ \mathrm{mV/dec}$, at room temperature. It prohibits scaling threshold voltage below a specific limit; otherwise, the OFF-state current in the device becomes too high. Therefore, at nanoscale dimensions, conventional MOSFET suffers from high leakage current, non-scalability of the supply voltage, and high power consumption.

In recent times, tunnel field-effect transistors (TFETs) have attracted a great deal of attention as an alternative to MOSFETs at nanoscale device dimensions. A TFET is structurally similar to a MOSFET except that in a TFET, the drain and source are oppositely doped in contrast to a MOSFET where the drain and the source are doped similarly. Moreover, the switching mechanism of a TFET is based on band-to-band tunneling, which allows TFET to exhibit subthreshold swing below $60\ \mathrm{mV/dec}$, at room temperature. It makes TFET suitable for low-voltage and energy-efficient digital circuit applications. However, there are some challenges in the application of a TFET in digital circuits. These challenges arise primarily due to the low ON-state current and high ambipolar current.

Further, scalability is another challenge for tunneling devices at nanoscale dimensions. TFETs are known to exhibit degraded electrical characteristics at small gate lengths, primarily due to direct source–to–drain band-to-band tunneling. Moreover, various studies have shown that TFETs are highly susceptible to process-induced variations such as random dopant fluctuations, non-abrupt source–channel junction, the shift in gate-edge with respect to source, and variation in work-function. These variations can lead to degraded electrical characteristics of the device at the nanoscale. This work aims to tackle the above-mentioned problems in a TFET.

In this work, a technique of suppressing ambipolar current has been proposed by inserting a drain-pocket (DP) at the drain–channel interface in a double-gate TFET (DGTFET). The DP reduces BTBT on the drain-side by increasing the tunneling barrier width and decreasing the band overlap. It results in a reduction of ambipolar current from $5 \times 10^{-6}\mathrm{A}/\mu\mathrm{m}$ in the DGTFET to $1 \times 10^{-14}\mathrm{A}/\mu\mathrm{m}$ in the DP-DGTFET for complete range of negative gate voltage ($-\mathrm{V_{DD}} \leq \mathrm{V_{GS}} \leq \mathrm{Gnd}$) and high drain doping, such as 1×10^{20} $\mathrm{atoms/cm^3}$.

To tackle the problem of scalability of TFETs, a silicon–on–insulator TFET (SOI-TFET) has been proposed. A ground plane (GP) is incorporated inside the buried-oxide (BOX) in the SOI-TFET. It is demonstrated that the addition of GP leads to increased effective drain–to–source distance, which suppresses the direct source–to–drain tunneling. Therefore, the OFF-state current ($\mathrm{I_{OFF}}$) is suppressed even at short gate lengths, and the device becomes more scalable. Further, the ambipolar current ($\mathrm{I_{AMB}}$) is suppressed even at short gate lengths.

A novel TFET demonstrating within-channel tunneling has been proposed using a dual-material gate (DMG) architecture. The gate material work-functions are chosen such that a sharp transition in the energy bands is obtained at the junction of high–low work-function materials. Therefore, tunneling occurs at the DMG interface (referred to as within-channel tunneling) rather than at the source–channel junction. The sharp transition at the DMG interface leads to an inherent lateral electric field and a strong gate control over the BTBT region. Therefore, several electrical parameters such as subthreshold swing, ON-state current, etc., improve in the proposed TFET. It becomes immune to variations in source doping concentration and gate-edge shift at the source–channel interface. However, the impact of work-function variations and interface trap charges in the proposed device is important and needs to be tackled.

Additionally, this work explores implementations that can exploit the unique characteristics of TFETs to realize logic functions. Separate single tunneling devices realizing logic functions such as OR, NAND, NOR, AND, XNOR and XOR have been proposed. Further, these devices can be combined in a complementary manner to obtain different logic gates. These gates are compact since fewer transistors are required compared to conventional complementary–metal–oxide–semiconductor (CMOS) logic gates. For instance, realizing AND gate using CMOS requires six transistors, whereas using the proposed devices, the AND gate can be realized using only two transistors.

In summary, this work contributes towards making TFETs more suitable for digital circuit applications. This has been achieved by proposing different TFET structures that ameliorate one or more problems in the conventional TFET. Moreover, the unique properties of TFETs, such as ambipolar conduction, the impact of the gate–source overlap, symmetric operation, and modulation of current within the channel, are utilized to realize all two-input logic functions using a single tunneling device.

This thesis is dedicated to my husband, and my family.

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List of Abbreviations

BTBT Band-to-band tunneling

CMOS Complementary metal oxide semiconductor

DGFET Double gate field-effect transistor

DGTFET Double gate tunnel field-effect transistor

DIBL Drain induced barrier lowering

DMG Dual material gate

DP Drain pocket

DP-SDGTFET Strained silicon based DGTFET with DP

DOS Density of states

EOT Effective oxide thickness

GP Ground plane

Ge Germanium

Gnd Ground potential or $0\ V$

HJ-TFET Si TFET with Ge source forming Si-Ge heterojunction TFET

IC Integrated circuits

ITRS International technology roadmap for semiconductors

ITC Interface trap charges

LDD Lightly doped Drain

MOSFET Metal oxide semiconductor field-effect transistor

QC Quantum confinement

QFL Quasi fermi level

RDF Random dopant fluctuations

SDGTFET Strained double gate tunnel field-effect transistor

SOIAS Silicon-on-insulator-with-active-substrate

SP Source pocket

SOI Silicon-on-insulator

TFET Tunnel field-effect transistor

T(E) Electron/hole transmission probability

WKB Wentzel–Kramers–Brillouin

List of Symbols

C_{GG}	Total gate capacitance
C_{GD}	Miller capacitance (Capacitance between gate and drain)
C_{GS}	Capacitance between gate and source
d_{gp}	Depth of the ground plane
E_g	Energy bandgap of the material
E_{ov}	Energy band overlap
E_{Field}	Electric Field
e	Electronic charge
HfO_2	Hafnium dioxide
I_{AMB}	Ambipolar current
I_{OFF}	OFF-state current
I_{ON}	ON-state current
I_{ON}/I_{OFF} ratio	ON-state to OFF-state current ratio
I_{OFF}	Drain current at $V_{GS} = V_{OFF,1}$
L_G	Channel length
L_D	Drain length
L_S	Source length
L_P	Pocket length
m^*	Effective mass of the electron
$m^*_{h,Si}$	Density of state effective mass of hole in normal silicon
$m^*_{h,s-Si}$	Density of state effective mass of hole in strained silicon
N_P	Pocket doping concentration
N_{gp}	Ground plane doping concentration
N_S	Source doping concentration
N_D	Drain doping concentration
N_C	Channel doping concentration
$N_{V,Si}$	Density of states in the valence band in normal silicon
$N_{V,s-Si}$	Density of states in the valence band in strained-silicon
SiO_2	Silicon dioxide
SS	Subthreshold swing

SS_{avg}	Average subthreshold swing
t_{gp}	Ground plane thickness
t_{box}	BOX thickness
t_{ox}	Gate Oxide thickness
t_{Si}	Silicon Body thickness
V_{DD}	Supply voltage
V_T	Thermal voltage (kT/q)
V_{FB}	Flat band voltage
V_D	Drain voltage
V_S	Source voltage
V_G	Gate voltage
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
V_{th}	Threshold voltage
$V_{th,d}$	Drain threshold voltage
$V_{D,SAT}$	Drain voltage at which saturation is observed in the output characteristics
$V_{OFF,1}$	The gate voltage from which the drain current starts to take off in the transfer characteristics for $V_{GS} \geq 0$
$V_{OFF,2}$	The gate voltage from which the drain current starts to take off in the transfer characteristics for $V_{GS} < 0$
x	Germanium mole fraction
$\Delta(E_c)_{s-Si}$	Increase in electron affinity of silicon due to the strain
$\Delta(E_g)_{s-Si}$	Decrease in the band gap of silicon due to the strain
ϵ_{ox}	Dielectric constant of the oxide
ϵ_{Si}	Dielectric constant of the silicon
$\Delta\Phi$	Energy range over which tunneling can take place
$\hbar$	Reduced Planck's constant
Λ	The tunneling barrier width created between the valence band of the source and the conduction band of the channel
ψ_d	Potential in the drain
Φ_m	Work-function of the gate material of the transistor

Chapter 1

Introduction

1.1 Motivation for the research work

The scaling of the metal–oxide–semiconductor field-effect transistor (MOSFET) has been driving the semiconductor industry since the 1960s. Scaling of the device dimension of a MOSFET by a scaling factor $\alpha\ (> 1)$ facilitates the packing of more transistors in the same area in an integrated circuit (IC). It results in decreased cost, improved performance, and lower power consumption in an IC [1–4]. Further, scaling the supply voltage helps maintain the electric fields in the device and reduce the total power consumption (which is the sum of dynamic and static power consumption). However, with continued down-scaling in the device dimensions, further scaling of the MOSFET, either in terms of device dimensions or supply voltage, has become challenging. As the device dimensions are scaled to a few nanometers or the power supply is scaled to < 0.8 V, the OFF-state leakage current I_{OFF} in the device increases significantly, leading to increased power consumption [2–6].

Further, the supply voltage (V_{DD}) can no longer be scaled significantly. The non-scalability in the supply voltage can be attributed to the subthreshold swing (SS) remaining above $60\ \mathrm{mV/dec}$ at room temperature [3, 4]. The SS of the MOSFET is defined as the change in gate voltage (V_G) required to increase the drain current (I_D) by a factor of 10. Therefore, to achieve an ON-state current to OFF-state current (I_{ON}/I_{OFF}) ratio of $\sim 10^6$, a gate–source voltage (V_{GS}) of $6 \times 60\ \mathrm{mV} = 0.36\ \mathrm{V}$ is required. Therefore, it is difficult to scale down the threshold voltage (V_{th}) below a certain limit. Additionally, to maintain the performance of a digital circuit, the overdrive voltage ($V_{DD} - V_{th}$) should be sufficiently high. Therefore, the non-scalability of threshold voltage translates to the non-scalability of the supply voltage. When the supply voltage cannot be scaled, the power consumption of an IC remains high. Therefore, there is a need for the devices which can work at lower V_{DD}, exhibit SS $< 60\ \mathrm{mV/dec}$ at the room temperature and draws low leakage current at nanoscale dimensions [1, 2, 4, 6].

In recent times, tunnel field-effect transistor (TFET) has attracted a great deal of attention as an alternative to MOSFETs at nanoscale device dimensions (channel length less than 100 nm) [4, 7–9]. TFET is structurally similar to MOSFET except that in a TFET, the drain and source are oppositely doped in contrast to a MOSFET where the drain and the source are doped similarly. Therefore, the TFET is similar to a MOSFET in terms of fabrication, except that in TFET, due to oppositely doped drain and source, when the source doping is done, the drain needs to be masked and vice-versa. This leads to an additional

step while fabricating a TFET compared to a MOSFET [10–13]. However, if same source/drain doping concentration is used for p-type and n-type TFETs in a CMOS-type TFET-based circuit, we can avoid this additional step. The most distinguishing feature of a TFET, when compared to a MOSFET, is its switching mechanism. A TFET operates on the principle of band-to-band tunneling (BTBT) rather than thermionic emission of carriers over a potential barrier. Due to the difference in the mechanism of current flow, a TFET can exhibit SS smaller than $60\ \mathrm{mV/dec}$ at room temperature [9, 14–16]. Therefore, a TFET can potentially be employed in energy-efficient digital circuits operating at lower supply voltages ($\mathrm{V_{DD}} < 0.5\ \mathrm{V}$) [8, 17–22]. Additionally, the current flowing through a TFET in the OFF-state is due to the reverse leakage current of a p-i-n diode, which is extremely low [3, 4, 8, 23].

Due to excellent subthreshold swing and low leakage current, TFETs are worth exploring in digital circuit applications. It is worth mentioning that TFET is currently not commercially used. However, various researchers have demonstrated the potential of TFETs using simulation and fabrication-driven experiments, even at small gate lengths of sub-9 nm [13, 24–32]. There are some challenges due to the low ON-state current $(\mathrm{I_{ON}})$ and high ambipolar current $(\mathrm{I_{AMB}})$. The scalability of the TFETs is another concern. TFETs are known to exhibit degraded electrical characteristics at smaller channel lengths, primarily due to direct source–to–drain band-to-band tunneling [33, 34]. Moreover, various studies have shown that TFETs are highly susceptible to process-induced variations. These variations can lead to degraded electrical characteristics [35–37].

Before employing TFETs in digital circuits, these limitations need to be tackled. This work aims to propose TFETs that can tackle the above-mentioned problems.

Further, it is important to note that some of the characteristics of the TFETs, such as ambipolar conduction, are undesirable when TFETs are considered as a direct replacement of MOSFETs in digital circuits [24, 38, 39]. However, the unique properties of the TFETs, such as ambipolar conduction, the effect of the gate–source and gate–drain overlap, symmetric operation, and modulation of current within the channel, can also be exploited to design the digital circuits differently. Therefore, in this work, novel compact TFET implementation of logic gates are explored.

1.2 Scope of the work

In this work, novel architectures and configurations of TFETs are proposed. A detailed investigation of the proposed devices is done using device simulations. The electrical parameters primarily analyzed in this work include average sub-threshold swing ($\mathrm{SS_{avg}}$), $\mathrm{I_{ON}}$, $\mathrm{I_{AMB}}$, and $\mathrm{I_{ON}/I_{OFF}}$ ratio. Further, the impact of process-induced variations and short-channel effects such as drain-induced barrier lowering (DIBL) and threshold voltage ($\mathrm{V_{th}}$) roll-off have been analyzed in this work. The conventional and proposed structures are compared based on the above parameters to highlight the improvement.

Though researchers are examining many structures for realizing TFETs, double-gate TFET (DGTFET) has been used primarily in this work. A double

gate architecture with a thin channel has electrostatics similar to the contemporary FinFETs and fully-depleted silicon–on–insulator (FD-SOI) FETs [7]. Additionally, the focus is on silicon-based TFETs in this work. It is worth pointing out that the tunneling probability is lower in Si-based TFETs due to the large bandgap. Therefore, researchers are exploring other material systems also [40–45]. Nevertheless, this work focuses on silicon since the material parameters, and tunneling model for silicon are widely experimented with, and well-established [7, 46–48].

This research has been carried out in the following major stages:

1. A technique of suppressing $\mathrm{I_{AMB}}$ has been proposed in which a drain-pocket (DP) is inserted at the drain–channel interface in a double-gate TFET (DGTFET). Using this technique, $\mathrm{I_{AMB}}$ can be fully suppressed for complete range of negative gate voltage ($-\mathrm{V_{DD}} \leq \mathrm{V_{GS}} \leq \mathrm{Gnd}$) and even for high drain doping such as $1 \times 10^{20}\ \mathrm{atoms/cm^3}$. Further, the technique of addition of DP is combined with current enhancement techniques such as strained silicon TFET and source pocket technique to illustrate the overall improvement in the electrical characteristics of the device.

2. A technique of improving the scalability of silicon–on–insulator TFET (SOI-TFET) has been proposed. A ground plane (GP) is inserted inside the buried-oxide (BOX) in an SOI-TFET. Besides improving the scalability of the device, insertion of GP results in the reduction of the $\mathrm{I_{OFF}}$ as well as the $\mathrm{I_{AMB}}$ at smaller gate lengths, such as $20\ \mathrm{nm}$.

3. A novel TFET structure has been designed using the dual-material gate (DMG) architecture. With the choice of appropriate gate material work-function, a sharp transition in the energy bands is obtained at the DMG interface. Therefore, tunneling is enabled in the middle of the channel (at the DMG interface) rather than at the source–channel junction. The proposed device results in an improvement in the overall characteristics in a conventional DGTFET.

4. An implementation of logic functions such as OR, NAND, AND, NOR, XNOR, and XOR has been explored using a single tunneling device. Further, these devices are used in a complementary manner to realize logic gates. These gates employ fewer transistors compared to conventional complementary–metal–oxide–semiconductor (CMOS) logic gates.

1.3 Thesis Organization

The rest of the thesis is organized as follows:

- **Chapter 2 Introduction to Tunnel Field-Effect Transistors:** The basic structure and operating principle of a TFET are discussed.

- **Chapter 3 Suppression of Ambipolar Current using Drain-Pocket:** This chapter investigates DGTFET with drain-pocket (DP-DGTFET). It is shown that the addition of a drain-pocket is useful in fully suppressing the I_{AMB} in a TFET.

- **Chapter 4 Improving the scalability of SOI-based TFETs:** This chapter investigates silicon–on–insulator (SOI) TFET with the ground plane (GP-TFET). It is shown that the addition of a ground plane in a TFET results in overall scalability improvement.

- **Chapter 5 Exploiting within-channel tunneling in a TFET:** This chapter investigates a novel TFET in which within-channel tunneling is employed. The proposed device results in an overall improvement in the electrical performance of a TFET.

- **Chapter 6 Implementation of Logic Functions:** This chapter shows the realization of various logic functions using tunneling devices and how they can be used to implement various logic gates.

- **Chapter 7 Conclusion:** This chapter concludes this dissertation and suggests future research directions.

Chapter 2

Introduction to Tunnel Field-Effect Transistors

In this chapter, the TFET structure, operating principle, and basic terminologies are described. Additionally, the promises and challenges in using TFETs in digital circuits are discussed. The focus of the chapter is to present relevant prior works.

2.1 Device Structure of a TFET

TFET is a p-i-n gated structure, where the intrinsic or lightly doped channel lies underneath the gate similar to that of a MOSFET. The major structural difference between a TFET and a MOSFET is that in a MOSFET, both the drain and the source are doped with a similar doping type (n^+ or p^+), while in a TFET, the doping type in the drain and the source is opposite. For example, if the drain is doped n^+, then the source would be doped p^+ and vice-versa. Thus, MOSFET

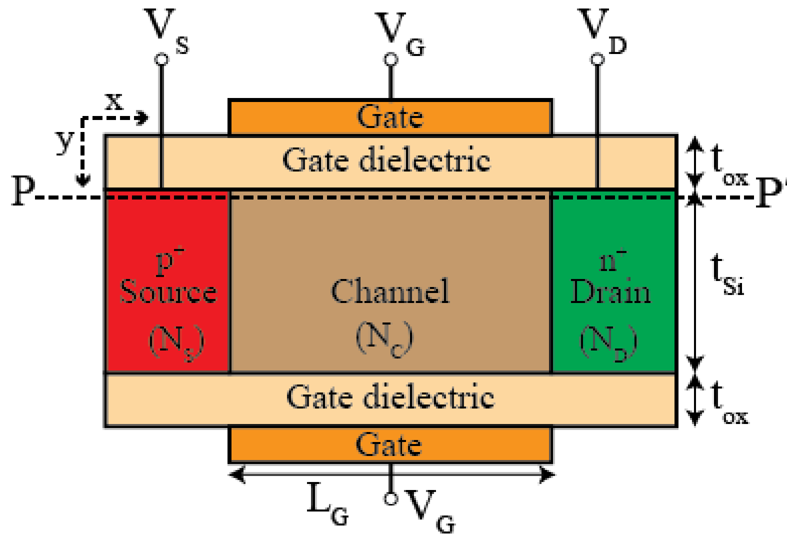


Figure 2.1: Cross-sectional view of an n-DGTFET.

is a symmetric device structurally, while TFET is an asymmetric device. Fig. 2.1 shows the cross-sectional view of a double-gate n-TFET. In an n-TFET, the drain is doped with n-type dopants, while the source is highly doped with the p-type dopants. In contrast, the drain of p-TFET is doped with p-type dopants, whereas the source is highly doped with n-type dopants. The channel region of a TFET is usually intrinsic or low-doped. It is separated from the gate electrode by a dielectric material, usually silicon dioxide (SiO_2) or hafnium dioxide (HfO_2), as in a conventional MOSFET [4].

Fig. 2.1 shows the cross-sectional view of an n-type DGTFET. It has been widely used in literature since it results in better control of the gate over the channel region compared to a single gate TFET and delivers a higher I_{ON} [7, 46]. Another advantage of using a double-gate device is that it improves the convergence behavior of the simulation [4, 49]. A DGTFET has two gates, one being the top gate and another the bottom gate. Generally, both gates are biased

at a common gate voltage referred to as $\mathrm{V_G}$. The drain and the source region are biased at voltages $\mathrm{V_D}$ and $\mathrm{V_S}$, respectively. The doping concentration of the drain, source, and channel regions is denoted as $\mathrm{N_D}$, $\mathrm{N_S}$, and $\mathrm{N_C}$, respectively. The thickness of gate oxide and thickness of the silicon body is referred to as $\mathrm{t_{ox}}$ and $\mathrm{t_{si}}$, respectively. The length of the drain, source, and channel regions is referred to as $\mathrm{L_D}$, $\mathrm{L_S}$, and $\mathrm{L_G}$, respectively. The basic device parameters used for simulating the DGTFET in this chapter are shown in Table 2.1. The same parameters have been used throughout the thesis unless mentioned differently. Additionally, it is worthy to point out that the basic simulations have been performed at 100 nm gate length. This has been done for the sake of a better understanding of the device operation. However, the scalability has been examined and reported for the devices proposed in the thesis.

Table 2.1: Device Parameters used in the simulation of an n-DGTFET

Parameter	**Value**
Supply voltage ($\mathrm{V_{DD}}$)	1.0 V
Silicon film thickness ($\mathrm{t_{si}}$)	10 nm
Gate dielectric constant (ϵ_r)	3.9
Gate oxide thickness ($\mathrm{t_{ox}}$)	3 nm
Gate work-function (ϕ_m)	4.20 eV
Source doping ($\mathrm{N_S}$) (p-type)	1×10^{20} atoms/cm^3
Drain doping ($\mathrm{N_D}$) (n-type)	1×10^{20} atoms/cm^3
Channel doping ($\mathrm{N_C}$) (p-type)	1×10^{17} atoms/cm^3
Gate length ($\mathrm{L_G}$)	$20 - 100$ nm

2.2 Simulation model used in the simulations

In this work, ATLAS (version 5.12.1.R) has been used for the device simulations [50]. The tunneling model plays a vital role in the simulation of TFETs. There

are two types of band-to-band tunneling (BTBT) models supported by ATLAS: the local BTBT model and the non-local BTBT model. The local tunneling models, such as Schenk's model and Kane's model, calculate the recombination-generation rate at each point based on the local electric field only. However, in a non-local tunneling model, the spatial energy band profile is taken into account for the computation of the tunneling current. Additionally, the spatial separation of the electrons generated in the conduction band from the holes generated in the valence band is also considered. Therefore, their accuracy is high in modeling the tunneling phenomenon. In this research, the non-local band-to-band tunneling model has been used. To activate this model, the keyword BBT.NONLOCAL is used in the simulations. The simulator uses the WKB approximation to calculate the tunneling probability [50]. For achieving this, a fine mesh is defined around the tunneling junction in the device by using the QTX.MESH and QTY.MESH statements. For investigating TFETs, the non-local BTBT model of ATLAS is widely used and has exhibited a good match with experimental and theoretical results [11,51–55].

In this work, the source and drain doping profiles are taken as abrupt [7,49,56]. A thin-film silicon body has been used in a DGTFET since it is observed that thin-film silicon improves the $\mathrm{I_{ON}}$ in a DGTFET. The thickness of the silicon body is taken to be $10\ \mathrm{nm}$ since below $10\ \mathrm{nm}$ considering quantum confinement effects in the simulator becomes important, which have not been considered in this work [57]. Furthermore, it is important to mention that this work aims to demonstrate how the shortcomings of the TFETs can be ameliorated using the

proposed techniques and not to report the absolute value of currents and voltages, which could strongly depend on the simulation model.

Fermi–Dirac statistics and the bandgap narrowing effects have been considered in the simulations to account for highly doped regions in the device. These models can be activated by using the keyword FERMI and BGN, respectively. Shockley–Read–Hall recombination model has been included in the simulations to account for the recombination effects. The model considers the leakage currents that exist due to thermal generation. The keyword for this model is SRH. The Lombardi mobility model has been used in the simulations. This model accounts for the dependence of mobility on the doping, temperature, and electric field [50].

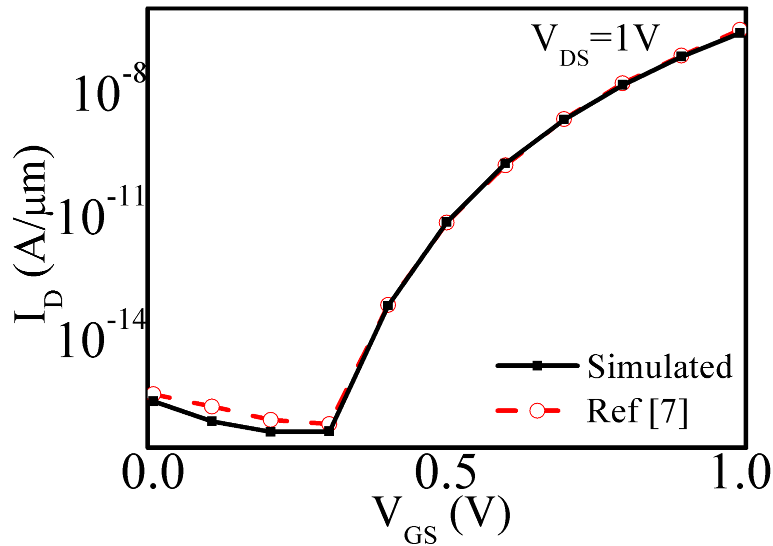


Figure 2.2: Simulation model calibrated by reproducing the results of [7].

The device simulation model used throughout the thesis has been calibrated and validated using the results presented in [7]. Several papers have corroborated the results of [7] using experiments or theoretical models [11, 48, 58–61]. In Fig.

2.2, the simulation model is calibrated by reproducing the results presented in Fig. 4(a) in ref [7].

2.3 Operating Principle of a TFET

The carrier injection in a TFET is based on the band-to-band tunneling (BTBT) mechanism rather than the thermionic emission [4, 8, 9, 19, 20]. Therefore, in a TFET, the current flowing through the device depends on the tunneling of the carriers through the potential barrier created at the tunneling junction. This potential barrier is controlled by the gate electrode lying over the channel region [8, 19, 62]. In an n-TFET, when the drain is biased at $\mathrm{V_{DD}}$, the source is biased at Gnd, and the gate voltage is varied from $-\mathrm{V_{DD}}$ to $\mathrm{V_{DD}}$. When drain–source voltage $(\mathrm{V_{DS}})$ is equal to $\mathrm{V_{DD}}$ and the gate–source voltage $(\mathrm{V_{GS}})$ is varied, the electrostatic potential and band bending get modulated at the source–channel junction and the drain–channel junction in the device. Therefore, depending on the band alignment, the BTBT is enabled or disabled at these junctions, thus controlling the tunneling current flowing through the device. The gate work-function is generally chosen such that the current starts to increase when the $\mathrm{V_{GS}} = 0$ V and $\mathrm{V_{DS}} = \mathrm{V_{DD}}$.

2.3.1 Regions of operation in a TFET

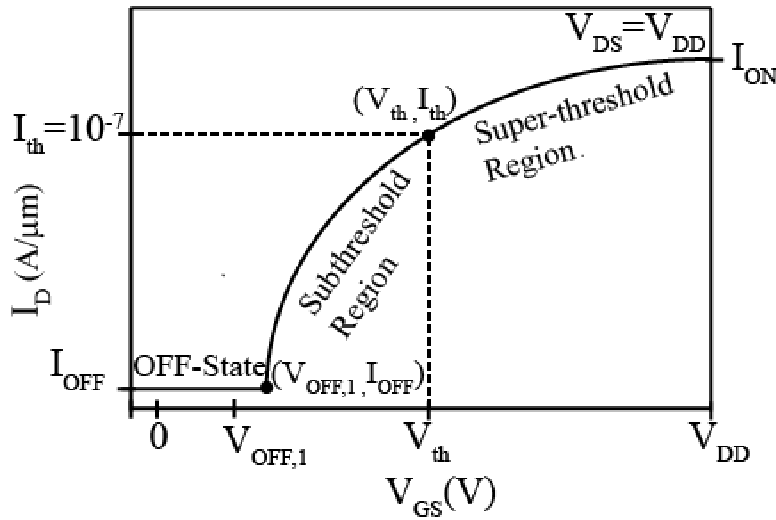


Figure 2.3: Expected transfer characteristics of an n-DGTFET showing different regions of operation at $V_{DS} = V_{DD}$.

Fig. 2.3 shows the expected transfer characteristics of an n-DGTFET illustrating different regions of operation. The different regions of operation are as follows [4]:

1. **OFF-state**: When $V_{GS} < 0$, the BTBT is inhibited and the TFET has an extremely low current. This is termed as the OFF-state in a TFET.

2. **Subthreshold region**: When $0 < V_{GS} < V_{th}$ (where V_{th} is the threshold voltage of the device, defined later in this chapter), the BTBT gets initiated and the drain current rises rapidly with the applied V_{GS}. This is termed as the subthreshold region of operation in a TFET.

3. **Super-threshold region**: When $V_{GS} > V_{th}$, the drain current rises at a reduced rate with the applied V_{GS}. This is termed as the super-threshold region of operation in a TFET.

2.3.1.1 OFF-state and ON-state in a TFET

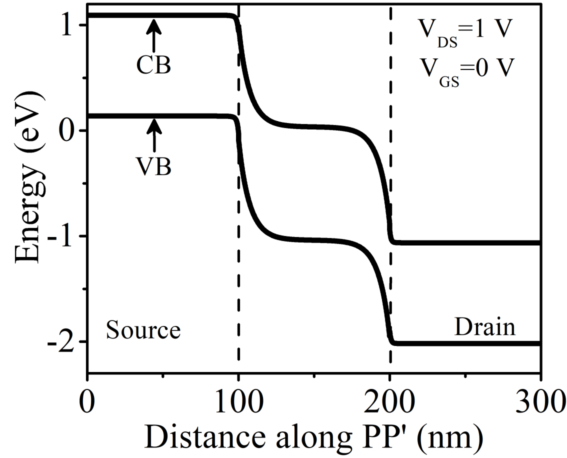


Figure 2.4: Energy band diagram of an n-DGTFET at $V_{GS} = 0$ V and $V_{DS} = V_{DD}$ along the cutline PP′.

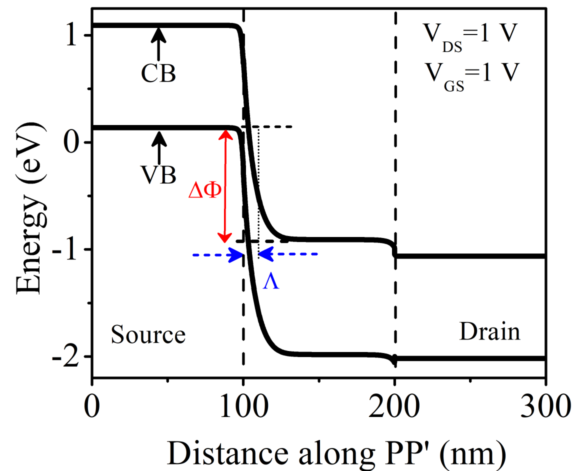


Figure 2.5: Energy band diagram of an n-DGTFET at $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}$ along the cutline PP′.

Fig. 2.4 and 2.5 show the band diagrams of an n-type DGTFET along the cutline PP′ in the OFF-state and the ON-state, respectively. It can be seen that when $V_{GS} = 0$ V, the conduction band of the channel is not aligned to the valence band of the source, and hence no band-to-band tunneling is possible. The DGTFET behaves like a reverse-biased p-i-n diode. The current flowing

through the device is the reverse leakage current of the p-i-n diode, which is very low. Hence the OFF-state current in a TFET is extremely low.

When $\mathrm{V_{GS}} > 0$, the conduction band of the channel is pushed down. This results in an alignment of the conduction band of the channel with the valence band of the source. Therefore, an overlap window gets created between the conduction band of the channel and the valence band of the source, shown as $\Delta\Phi$ in Fig. 2.5. Further, there is a decrease in the tunneling barrier width Λ at the source–channel junction, as shown in Fig. 2.5. They lead to significant tunneling of electrons from the valence band of the source to the conduction band of the channel, and current flows through the TFET.

The drain current in a TFET depends on the tunneling transmission probability $(\mathrm{T(E)})$ of the carriers through the tunneling barrier. The $\mathrm{T(E)}$ can be calculated by using the Wentzel–Kramers–Brillouin (WKB) approximation. In this approximation, the tunneling barrier is approximated as a triangular barrier. $\mathrm{T(E)}$ is analytically given as follows:

$$T(E) \approx exp\left[-\frac{4\,\sqrt{2m^*}\;E_g^{3/2}}{3\;|e|\;\hbar\;E_{Field,\Lambda}}\right] \tag{2.1}$$

where $\mathrm{E_{Field,\Lambda}}$ is the electric field across Λ and is given as follows:

$$E_{Field,\Lambda} = \frac{E_g\;+\;\Delta\Phi}{\Lambda} \tag{2.2}$$

where $\mathrm{m^*}$ is the effective mass of the electron, $\mathrm{E_g}$ is the effective bandgap of the

material, $\Delta\Phi$ is energy band overlap, $\hbar$ is the reduced Planck's constant, $|e|$ is the charge of an electron.

The drain current in the TFET, which is proportional to $T(E)$ is given as follows:

$$I_D \propto exp\left[-\frac{4\sqrt{2m^*}\, E_g^{*3/2}\ \Lambda}{3\,|e|\,\hbar\,(E_g\ +\ \Delta\Phi)}\right]\ \Delta\Phi \tag{2.3}$$

According to Eq. 2.3, the I_{ON} in a TFET depends on m^*, E_g, $\Delta\Phi$ and Λ. Therefore, one or more of these parameters can be adjusted, to increase the I_{ON}. There are various methods proposed in the literature to boost the I_{ON} in a TFET based on these parameters and are discussed in the next section [7,46,58,63].

2.3.1.2 Achieving subthreshold Swing less than 60 mV/dec in a TFET

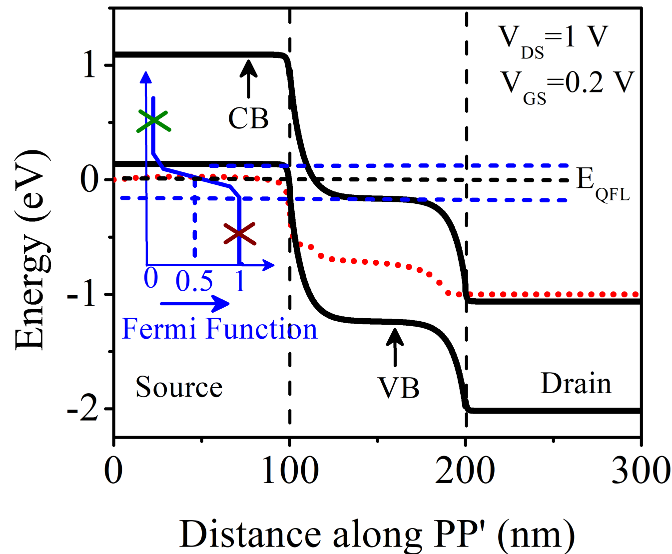


Figure 2.6: Energy band diagram of an n-DGTFET at $V_{GS} = 0.2$ V and $V_{DS} = V_{DD}$ along the cutline PP′.

TFETs are capable of achieving a SS lower than 60 mV/dec. This is because, during the tunneling process, the electrons only in the overlapped energy window can tunnel from the source into the channel, as shown in Fig. 2.6. The channel bandgap inhibits the tunneling of the low-energy electrons (as shown by the red cross) of the source Fermi–Dirac distribution. Further, the source bandgap inhibits the tunneling of the high-energy electrons (as shown by green cross) of the source Fermi–Dirac distribution. This allows only the electrons near the Fermi level to tunnel from the source to the channel. Therefore, the exponential tail of the Fermi-Dirac distribution is effectively cut-off, and a band-pass filter action is achieved. This leads to effective cooling of the carrier distribution, resulting in a lower SS in the TFETs [4, 8, 19, 64].

2.3.2 Ambipolar conduction in TFET

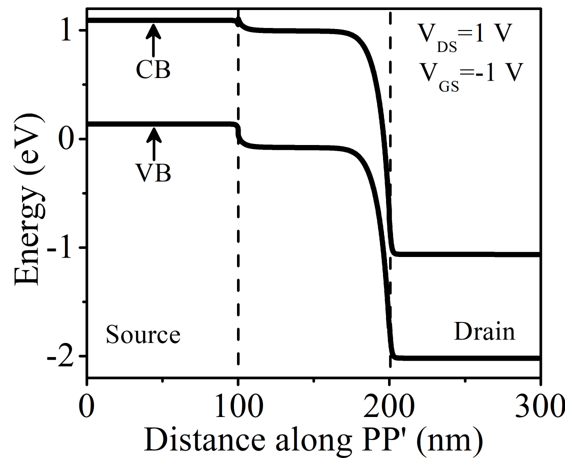


Figure 2.7: Energy band diagram of an n-DGTFET at $V_{GS} = -V_{DD}$ and $V_{DS} = V_{DD}$ along the cutline PP′.

TFETs show ambipolar conduction. The ambipolar conduction in TFETs originates due to large BTBT occurring at the source–channel junction as well

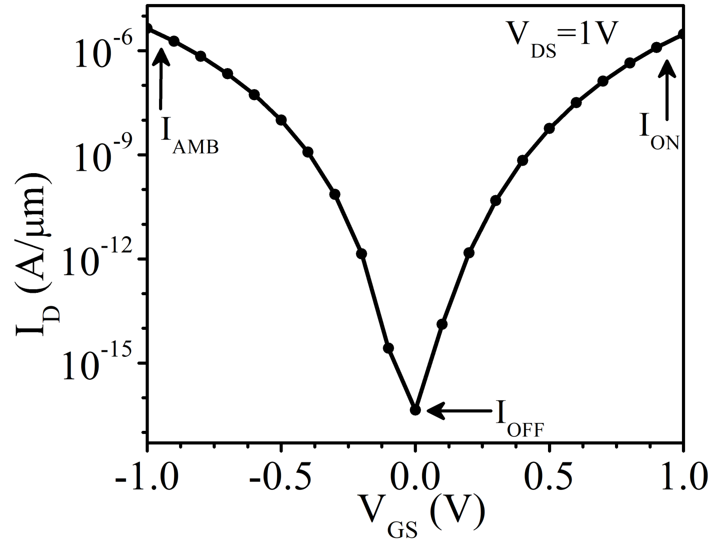


Figure 2.8: Transfer Characteristics of an n-DGTFET at $\mathrm{V_{DD}} = 1$ V.

as the drain–channel junction at different polarities of gate voltages. When $\mathrm{V_{GS}} = -\mathrm{V_{DD}}$, the valence band of the channel and the conduction band of the drain get aligned. Therefore, tunneling starts at the drain–channel interface rather than the source–channel interface. Fig. 2.7 shows the band diagrams of a DGTFET along cutline PP′ in the ambipolar state. Therefore, a TFET can show n-type behaviour with the electrons contributing as majority carriers and p-type behaviour with the holes contributing as majority carriers for the same drain voltage [4]. Fig. 2.8 shows the transfer characteristics of an n-DGTFET at $\mathrm{V_{DS}} = 1$ V and -1 V $< \mathrm{V_{GS}} < 1$ V.

2.4 Terminologies

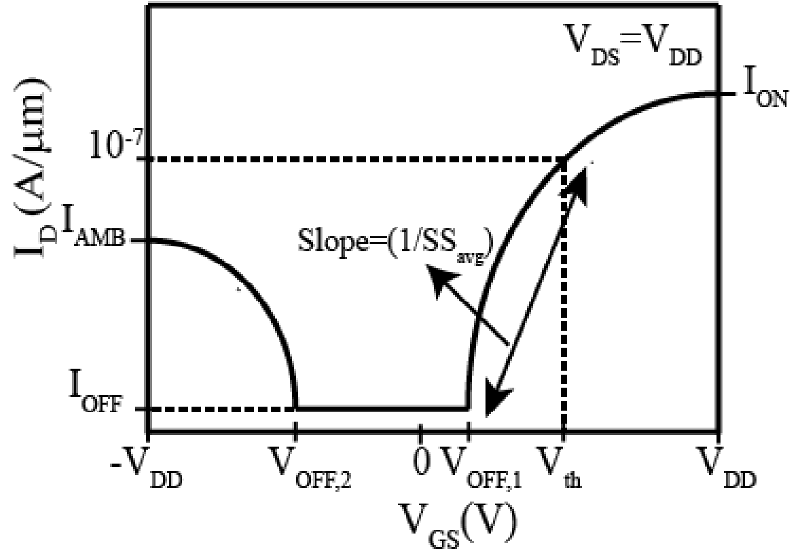


Figure 2.9: Definition of Electrical Parameters.

Fig. 2.9 illustrates some definitions of electrical parameters relevant to TFETs. These definitions are used throughout the thesis.

1. **ON-state current** (I_{ON}): It is defined as the drain current at $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}$.

2. **Ambipolar current** (I_{AMB}): It is defined as the drain current at $V_{GS} = -V_{DD}$ and $V_{DS} = V_{DD}$.

3. **OFF-state current** (I_{OFF}): It is defined as the drain current at $V_{GS} = 0$ and $V_{DS} = V_{DD}$.

4. **Threshold voltage** (V_{th}): It is defined as the positive V_{GS} at which the drain current $I_D = 10^{-7}$ A/μm at $V_{DS} = V_{DD}$.

5. **OFF-voltage 1** ($V_{OFF,1}$)**:** It is defined as the V_{GS} at which the drain current

starts rising from $\mathrm{I_{OFF}}$ to $\mathrm{I_{ON}}$ at $\mathrm{V_{DS}} = \mathrm{V_{DD}}$. In this work, $\mathrm{V_{OFF,1}} = 0$ V. The $\mathrm{I_{OFF}}$ is defined as drain current at $\mathrm{V_{OFF,1}}$.

6. **OFF-voltage 2** ($\mathrm{V_{OFF,2}}$)**:** It is defined as the $\mathrm{V_{GS}}$ at which the drain current starts rising from $\mathrm{I_{OFF}}$ to $\mathrm{I_{AMB}}$ at $\mathrm{V_{DS}} = \mathrm{V_{DD}}$. $\mathrm{V_{OFF,1}} - \mathrm{V_{OFF,2}}$ gives the range for which the $\mathrm{I_{AMB}}$ is suppressed in the device. If $\mathrm{V_{OFF,1}} - \mathrm{V_{OFF,2}} = \mathrm{V_{DD}}$, the $\mathrm{I_{AMB}}$ is said to be fully suppressed.

7. **Average subthreshold swing** ($\mathrm{SS_{avg}}$)**:** It is defined as the inverse slope obtained from the transfer characteristics from the point at which $\mathrm{I_{OFF}}$ is extracted to the point at which $\mathrm{V_{th}}$ is extracted at $\mathrm{V_{DS}} = \mathrm{V_{DD}}$. Analytically, it can be calculated as given below [4, 7]:

$$SS_{avg} = \frac{V_{th} - V_{OFF,1}}{log(10^{-7}) - log(I_{OFF})} \tag{2.4}$$

2.5 Literature Survey relevant to this work

Due to its low $\mathrm{I_{OFF}}$ and ability to achieve an SS less than $60\ \mathrm{mV/dec}$ at room temperature, TFET is considered a suitable candidate to be used in energy-efficient digital circuits operating at lower $\mathrm{V_{DD}}(\leq 0.5\ \mathrm{V})$ [3, 4, 8, 18]. However, there are several challenges in a TFET, which prohibit the usage of TFETs in digital circuit applications. In the past decade, research has been focused on tackling these challenges. Some of the notable techniques in the literature are described in the following paragraphs.

2.5.1 I_{ON} improvement in a TFET

The I_{ON} is low in the TFETs since the carrier transport is based on the BTBT mechanism. The I_{ON} determines the performance of the digital circuit. A low I_{ON} leads to degraded speed of the digital circuit [4, 8]. Therefore, techniques to boost the I_{ON} in a TFET are crucial to make it suitable for digital circuit applications.

According to Eq. 2.3, the I_{ON} can be enhanced by a) employing a material with lower effective carrier mass (m^*) or lower bandgap (E_g) b) enhancing the electric field ($E_{Field,\Lambda}$) at the tunnel junction by reducing the tunneling barrier width (Λ (refer Eq. 2.2). To achieve increased I_{ON}, various TFETs have been demonstrated employing lower bandgap materials such as germanium, III–V materials, strained materials, etc. [40–43, 61, 65]. However, employing a low-E_g material throughout the device leads to increased I_{OFF} and I_{AMB} along with increased I_{ON}. In a TFET, the I_{ON} depends on the material properties at the source–channel junction. Therefore, TFETs employing low-E_g material in the source region and high-E_g material in the channel and drain regions were proposed. These TFETs are known as heterojunction TFETs and leads to increased I_{ON} without an increase in the I_{AMB} or I_{OFF} [4, 42, 63, 66].

Further, I_{ON} can be boosted by enhancing the electric field $E_{Field,\Lambda}$ at the tunnel junction. Better control of the gate over the tunnel region results in an increased $E_{Field,\Lambda}$. Some methods proposed in the literature to increase the electric field at the tunnel junction include insertion of a source-pocket (SP)

at the source–channel junction, inserting a SiGe δ-doped layer in a TFET, by using a thin device body, using high-k gate-dielectric, fringing-field engineering, electron-hole bilayer concept, stacked source configuration, and gate work-function engineering [7, 56, 67–73]. Furthermore, structures based on double-gate, multiple-gates, gate-all-around architecture have been proposed. These structures provide better gate control in the device, resulting in decreased tunnel barrier width (Λ) and increased $E_{Field,\Lambda}$. Thus, they boost the I_{ON} in the device [7, 52, 74, 75].

In a conventional p-i-n TFET, the gate overlaps the channel region, and the tunneling occurs at the source–channel interface. Such a TFET is described as point-tunneling TFET. In point-tunneling TFETs, the tunneling area is limited, resulting in a low I_{ON}. To overcome this limitation, line-tunneling, also known as vertical tunneling, has been explored by the researchers [11, 17, 72, 76–81]. In a line-tunneling TFET, the gate is overlapped with the source such that a strong band-bending occurs. This leads to tunneling within the source towards the source–gate-oxide interface [82]. In such TFETs, the I_{ON} can be boosted by increasing the gate–source overlap area. Further, various devices exhibiting line-tunneling, such as L-TFETs, U-TFETs, T-TFETs, etc., have been proposed [83–85]. Furthermore, TFET based on graphene-nanoribbon, carbon nanotubes, nanowires, 2-D transition–metal–dichalcogenides (TMDs), black phosphorus and 1-D broken-gap material have been proposed in the literature to improve the I_{ON} [14, 44, 45, 86–91].

2.5.2 Mitigation of $\mathrm{I_{AMB}}$ in a TFET

In a TFET, the current flow for both positive and negative $\mathrm{V_{GS}}$ (at same $\mathrm{V_{DS}}$) due to a large BTBT occurring at the source–channel junction and the drain–channel junction, respectively. This gives rise to the ambipolar behaviour in a TFET. Ambipolar conduction is one of the primary concerns in employing the TFETs in CMOS-based digital circuits [4, 8]

Ambipolar current can be decreased as follows [58]:

1. By increasing the depletion region width on the drain side,
2. By reducing the electric field on the drain side,
3. By using wide-bandgap materials on the drain side.

There are various techniques proposed in the literature based on the above approaches to suppress the $\mathrm{I_{AMB}}$. Some of the notable techniques include asymmetric source/drain doping, gate–drain overlap/underlap, work-function engineering of gate electrodes, spacer engineering, gate material engineering, and insertion of hetero-BOX [7, 33, 47, 49, 92–95]. Although the techniques mentioned above help decrease the $\mathrm{I_{AMB}}$, most of these techniques are not able to completely suppress the $\mathrm{I_{AMB}}$. Additionally, these techniques have some drawbacks associated with them. For instance, the asymmetric source/drain doping technique frequently employed to suppress $\mathrm{I_{AMB}}$ in TFETs requires a drain doping of 1×10^{17} atoms/cm^3 to completely suppress the $\mathrm{I_{AMB}}$ and has the side-effect of increasing the access resistance of the device [49]. As reported in [47], hetero-

dielectric BOX is another technique to suppress the I_{AMB}. However, it results in a decrease in the I_{ON} by a factor of 1.8. Further, gate-underlap is one of the techniques used to suppress the I_{AMB}. However, it reduces the current driving capability of the device when the tunnel resistance is low [49, 94].

Furthermore, gate–on–drain overlap TFET is proposed to suppress the I_{AMB} [58]. However, for an overlap of 30 nm, the I_{AMB} is not fully suppressed when the V_{GS} is less than -0.5 V. Additionally, this technique reduces the I_{AMB} in TFET only when the drain doping is kept appreciably lower than the source doping. For instance, in a silicon-DGTFET, considering the source doping of 1×10^{20} atoms/cm^3, the I_{AMB} can be effectively suppressed for the drain dopings not more than 1×10^{19} atoms/cm^3. Moreover, it results in an increase in the capacitance between gate and drain (C_{GD}) of the device [47, 58]. Additionally, a tunnel dielectric-based TFET was proposed to boost the I_{ON} and eliminate the I_{AMB} by providing an additional barrier in the channel between the source and the drain [96]. In [97], a TFET is proposed by replacing the conventional drain semiconductor by metal-silicide with work-function of 4.25 eV, such as $TaSi_x$ and $TiSi_x$, to reduce the I_{AMB}.

In summary, many techniques to reduce the I_{AMB} have been proposed in the literature. Each technique has its advantages and shortcomings. In the subsequent chapters, techniques to reduce ambipolar current and remove some of the demerits of the above techniques have been proposed.

2.5.3 Scalability of TFETs

Scalability of devices is essential for meeting the requirement of increased functionality in a given area, and reduced power consumption [1–5]. The problems in MOSFET scaling have motivated the search for alternative devices [2, 4–6]. TFETs are scalable in terms of supply voltage due to their lower SS [4, 8, 20]. However, the scalability of TFET in terms of device dimensions needs more investigation. It is demonstrated using analytical models that TFETs are typically more immune to short-channel effects than the MOSFETs. However, when the gate length is scaled below some limit, the scalability of TFETs degrades at a higher rate compared to the MOSFETs [98]. Further, at smaller channel lengths, primarily due to direct source–to–drain BTBT, the $\mathrm{I_{OFF}}$ in TFET increases. As a result, the $\mathrm{I_{ON}/I_{OFF}}$ ratio of the device decreases, and the $\mathrm{SS_{avg}}$ increases. Thus, it deteriorates the energy-efficiency of the TFETs [4, 33, 34, 34, 59, 99]. Therefore, techniques for improving the scalability of TFETs play an important role for future applications. Some of the notable works related to the TFET scalability are [26, 100–104]. It is shown that a device with a thin channel is scalable to sub-10 nm channel lengths. However, it has problems related to the yield and device variability [100, 101]. In [102], it is shown that if the channel material has high-$\mathrm{E_g}$, low $\mathrm{m^*}$ and high dielectric constant along with a highly doped source region, the device can be scaled below 10 nm. Further, highly scalable vertical nanowire TFET, resonant TFET, Ge-pocket TFET with superior SS and and $\mathrm{I_{ON}}$ are proposed in [26, 103, 104]. Additionally, an optimized

p-type $Si_{0.5}Ge_{0.5}$-pocket TFET with a gate length of 150 nm has been shown to outperform 14 nm FinFET for $V_{DD} \leq 0.4$ V [28]. Further, as per ref. [32], the TFET simulated using 28 nm technology and the one fabricated at 100 nm gate length show almost similar ON-state current. This is because the ON-state current in a TFET is weakly dependent on the gate length [105]. These results again highlight the potential of TFETs for low-voltage futuristic applications.

2.5.4 Tackling process-induced variations

In TFETs, the properties of source–channel interface determines the I_{ON}. A high source doping is required to obtain a high I_{ON} [4, 19, 106]. However, the formation of a highly doped source results in increased fabrication complexity and high thermal budgets [57]. Further, an abrupt source doping profile is required to boost the I_{ON} and obtain a low subthreshold swing [8, 9, 19, 107]. The source doping is typically obtained using ion-implantation. During ion-implantation, there is a random and discrete positioning of the dopant atoms in the substrate leading to random dopant fluctuations (RDF) [108, 109]. Additionally, some dopants extend laterally from the source towards the channel [36, 37]. As a result, obtaining sharp doping profiles becomes difficult [57, 108, 110]. Moreover, during the fabrication process, in the patterning steps such as lithography, etching, deposition, etc., the edges can deviate from the reference straight line, thus resulting in a misalignment of gate-edge to the source–channel junction resulting in an imperfect source–channel interface [35, 111]. Furthermore, TFETs are susceptible to work-function variations (WFV) [35, 112]. A metal gate electrode

consists of multiple crystalline grains of different orientations. These grain orientations can lead to different effective work-function of a gate metal [112, 113]. The above process-induced variations leads to degraded electrical parameters such as I_{ON} and SS_{avg} in the device [57, 108, 114]. These variations become more detrimental at the nanoscale dimensions [53, 109, 115]. Researchers have proposed architectures such as dopingless TFETs and junctionless TFETs to tackle these variations in the device [53, 57, 109, 110, 115–117]. In a dopingless TFET, an intrinsic semiconductor is taken throughout the TFET body. The source and drain regions are formed using appropriate work functions for the corresponding metal electrodes. Further, in a junctionless TFET, a highly doped n-type (or p-type) semiconductor is taken throughout the TFET body. The channel and source (or drain) regions are formed using appropriate work functions for the channel and source (or drain) metal electrodes, respectively. Therefore, no metallurgical junctions are required in these devices, minimizing the variations due to non-abrupt doping and gate-edge misalignment at the source–channel junction.

2.5.5 TFETs in digital circuits

Due to their energy-efficiency and low leakage current, TFETs are promising for future digital circuit applications. Additionally, there are some unique characteristics of TFETs that can be employed in digital circuits. TFETs have been used to realize different digital circuits such as logic gates, memories, D/A converter, arithmetic circuits such as adders etc., demonstrating interest-

ing characteristics [24, 38, 39, 54, 55, 118–120]. It is shown that low-voltage, energy-efficient circuits can be realized using TFETs. Further, TFET based circuit has been shown to perform $2\times$ better than its MOSFET counterpart at low voltages$\mathrm{V_{DD}} \leq 0.25$ V [119, 121]. However, TFET-based circuits suffer from degradation in the output levels due to ambipolar conduction. Additionally, there are overshoots and undershoots in the transient response due to the high Miller capacitance [24, 90, 122]. Further, it is important to note that some of the characteristics of the TFETs, such as ambipolar conduction, are undesirable when TFETs are considered as a direct replacement of MOSFETs in digital circuits [24, 38, 39]. Nevertheless, these unique properties of the TFETs, such as ambipolar conduction, the effect of the gate–source and gate–drain overlap, symmetric operation, and modulation of current within the channel, can be used to implement efficient digital circuits, as demonstrated in this work.

Chapter 3

Suppression of Ambipolar Current using Drain-Pocket

3.1 Introduction

One of the serious concerns in using TFETs for CMOS circuit applications is ambipolar conduction. The ambipolar conduction can be suppressed by minimizing band-to-band tunneling probability at the drain–channel junction. Various techniques proposed to reduce ambipolar conduction in TFETs have been discussed in Chapter-2. In this chapter, a DGTFET with drain-pocket (DP) is proposed to suppress the ambipolar current. It is demonstrated that the inclusion of DP in a DGTFET suppresses the $\mathrm{I_{AMB}}$ in the device, even when TFET is biased at high negative gate voltages and drain doping is kept as high as source doping. Additionally, to illustrate that the proposed technique can be employed in future TFETs, the application of DP in strained-silicon-based DGTFET (SDGTFET) with high-k gate dielectric operating at $\mathrm{V_{DD}} = 0.5$ V is

also demonstrated. The limitations of the proposed technique are also discussed.

3.2 Device structure

Table 3.1: Device Parameters used in the simulation of DGTFET and DP-DGTFET

Parameter	**Value**
Supply voltage (V_{DD})	$0.5 - 1.0$ V
Silicon film thickness (t_{si})	10 nm
Gate dielectric constant (ϵ_{ox})	3.9
Gate oxide thickness (t_{ox})	3 nm
Gate work-function (ϕ_m)	4.20 eV
Source doping (N_S) (p-type)	1×10^{20} atoms/cm^3
Drain doping (N_D) (n-type)	1×10^{20} atoms/cm^3
Channel doping (N_C) (p-type)	1×10^{17} atoms/cm^3
Gate length (L_G)	100 nm
Pocket doping (N_P) (n-type)	$5 \times 10^{18} - 1 \times 10^{20}$ atoms/cm^3
Pocket length (L_P)	$0 - 60$ nm

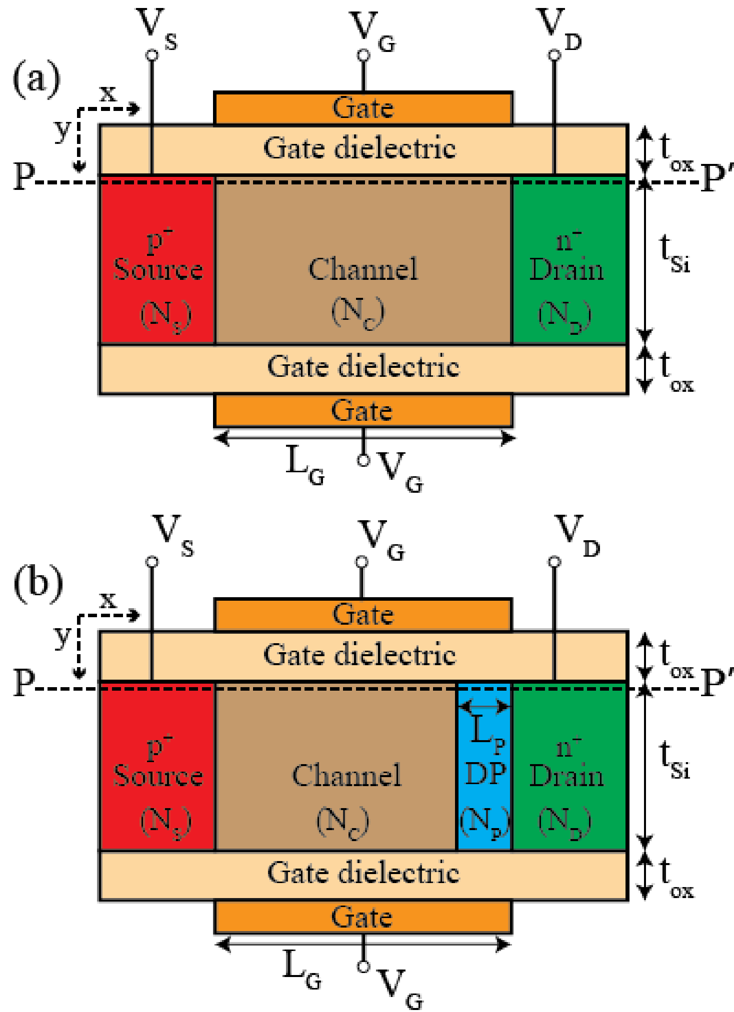


Figure 3.1: Cross-sectional view of (a) DGTFET (b) DP-DGTFET.

The cross-sectional view of the DGTFET with and without DP are shown in Fig. 3.1(a) and 3.1(b), respectively. The DGTFET without DP is referred to as DGTFET, and with DP is referred to as DP-DGTFET. The device parameters of the DGTFET and DP-DGTFET used in the simulations are shown in Table 3.1. The only differentiating feature between a conventional DGTFET and a DP-DGTFET is the DP. The type of dopant in the DP and the drain is the same. However, the doping concentration in the DP (N_P) is kept lower than the doping concentration in the drain (N_D).

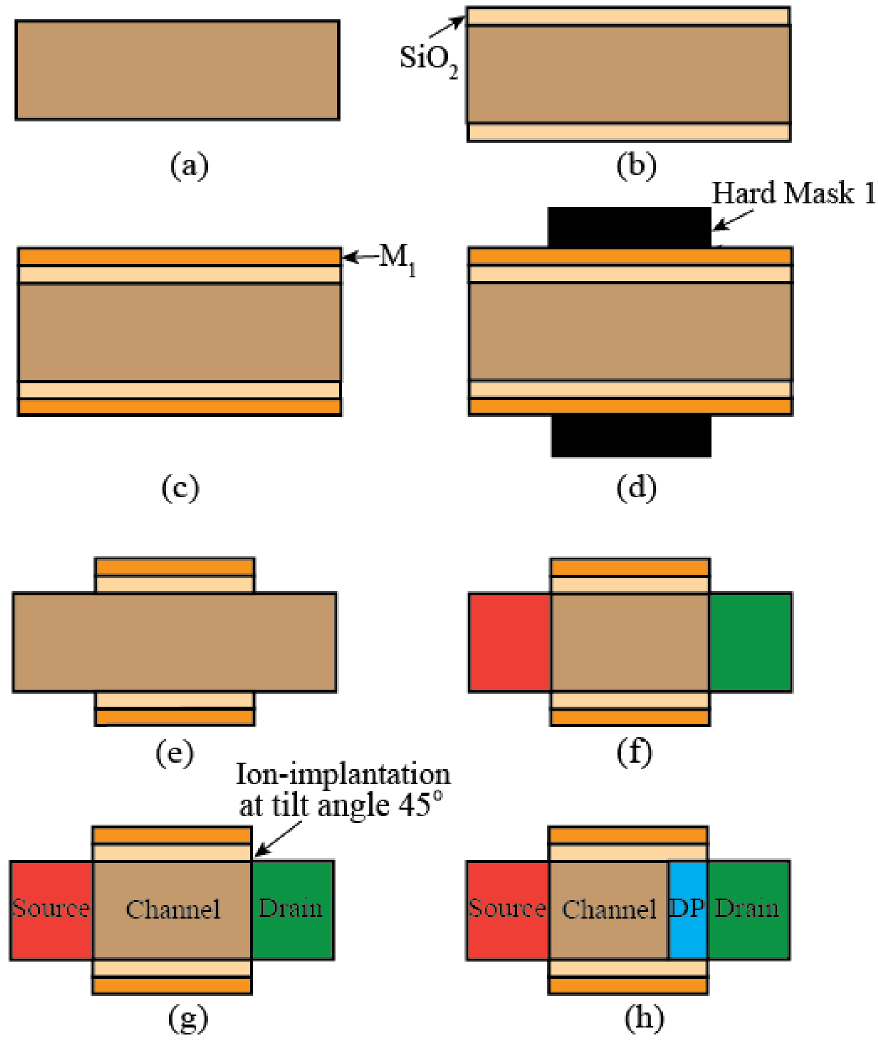


Figure 3.2: Proposed fabrication steps for the DP-DGTFET structure.

Fig. 3.2 illustrates one of the possible ways of fabricating the proposed DP-DGTFET. The process starts with a $10\ \mathrm{nm}$ thick, lightly doped silicon wafer with doping $\mathrm{N_C} \approx 1 \times 10^{17}\ \mathrm{atoms/cm^3}$, as shown in Fig. 3.2(a). Afterward, the wafer undergoes an RCA-cleaning process [123], making it suitable for the gate-oxidation process. Then the wafer is oxidized for about 25 minutes in a rapid thermal oxidation processor at $800 - 1000°\mathrm{C}$. This results in a $3\ \mathrm{nm}$ thick $\mathrm{SiO_2}$ gate dielectric layer as shown in Fig. 3.2(b) [123, 124]. This is followed by the deposition of a metal layer $\mathrm{M_1}$ with a work-function ϕ_m, using the e-

beam deposition technique, as shown in Fig. 3.2(c) [125]. This is followed by the gate patterning in which a hard mask is deposited over the area where the M_1/SiO_2 stack is to be retained, as shown in Fig. 3.2(d) [126]. The M_1/SiO_2 stack is selectively etched from the remaining area, as shown in Fig. 3.2(e). The source and the drain regions are formed using ion-implantation techniques, as shown in Fig. 3.2(f) [124]. The drain and source needs to be doped oppositely, therefore, when source doping is done, the drain needs to be masked and vice-versa. Finally, the drain pocket is formed by using the ion-implantation technique at a tilt angle of $45°$ at $3\ \mathrm{KeV}$, as shown in Fig. 3.2(g) [67,68,127]. The proposed DP-DGTFET structure obtained is shown in Fig. 3.2 (h).

It is worthy to note that the addition of DP to the TFET is similar to using the lightly-doped-drain (LDD) extension, which has been devised for MOSFETs [128, 129]. However, the purpose of LDD in a MOSFET is different from adding DP in a TFET. In a TFET, the introduction of DP is motivated by the observation that BTBT on the drain-side is undesirable in a TFET since it results in a higher I_{AMB}. The BTBT at the drain–channel junction depends on the tunneling barrier width at the drain-side and the overlap between the conduction band of the drain and the valence band of the channel. An appropriately designed DP adjacent to the drain is expected to reduce BTBT on the drain-side by increasing the tunneling barrier width and decreasing the energy band overlap on the drain-side.

3.3 Design and Optimization of Drain-Pocket

In a DP-DGTFET, the BTBT can occur at the drain–DP junction, as well as DP-intrinsic-channel junction. Therefore, a DP must be designed such that BTBT is inhibited at both these junctions under all bias conditions by finding appropriate doping concentration (N_P) and the DP length (L_P). This is explained using the DP-DGTFET shown in Fig. 3.1(b), in the following paragraphs.

3.3.1 Effect of N_P

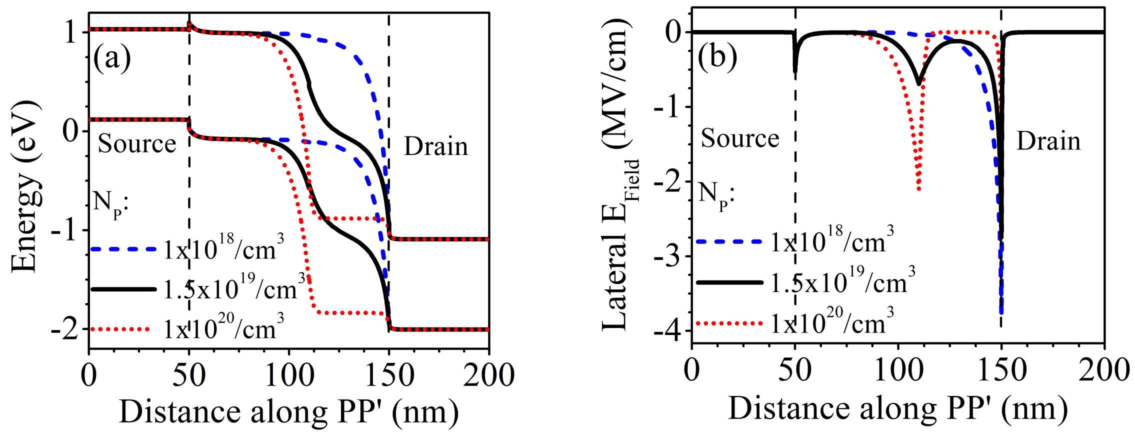


Figure 3.3: (a) Energy band diagram, and (b) Lateral E_{Field} profile in DP-DGTFET at $V_{DS} = 1$ V and $V_{GS} = -1$ V along the cutline PP′ in Fig. 3.1(a) for different values of N_P and $L_p = 40$ nm.

The effect of N_P on the band diagram and the lateral electric field profile in the DP-DGTFET are shown in Fig. 3.3, for $V_{DS} = 1$ V and $V_{GS} = -1$ V (the ambipolar conduction state). When N_P is low (1×10^{18} atoms/cm^3), there is a large overlap between the conduction band and the valence band, and a small tunneling barrier exists at the drain–DP junction which allows large BTBT to occur, as shown in Fig. 3.3(a). The lateral electric field profile also exhibits

a peak at the drain–DP junction at low N_P, as shown in Fig. 3.3(b). As N_P is increased, the tunneling barrier width at the drain–DP junction increases, and a reduction in the peak electric field at the drain–DP junction is noticed. As a result, the BTBT at the drain–DP junction reduces. However, as N_P is increased, the electric field at the DP-intrinsic-channel junction starts increasing, and when the tunneling barrier width at the DP-intrinsic-channel junction becomes sufficiently small, an undesirable BTBT at the DP-intrinsic-channel junction occurs (when $N_P = 1 \times 10^{20}$ atoms/cm^3). Therefore, an optimum DP doping $N_{P,opt} = 1.5 \times 10^{19}$ atoms/cm^3 is found to result in the minimum overall BTBT on the drain-side.

3.3.2 Effect of L_P and L_G

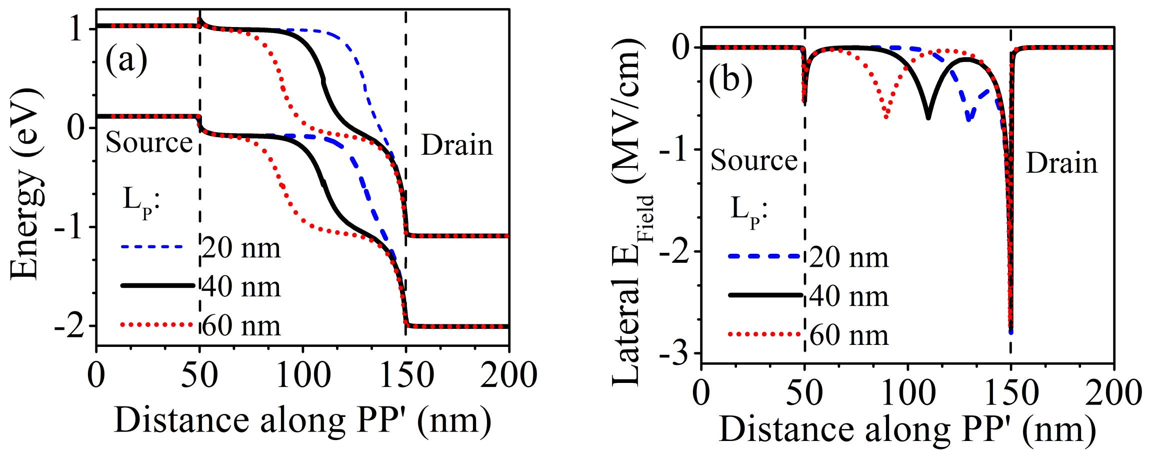


Figure 3.4: (a) Energy band diagram, and (b) Lateral E_{Field} profile in DP-DGTFET at $V_{DS} = 1$ V and $V_{GS} = -1$ V along the cutline PP′ in Fig. 3.1(a) for different values of L_P and $N_P = 1.5 \times 10^{19}$ atoms/cm^3.

Next, keeping the DP doping at $N_{P,opt}$, L_P is varied to minimize BTBT at the drain side. Fig. 3.4(a) and 3.4(b), respectively, show the change in the band diagram and electric field profile of the device at $V_{DS} = 1$ V and $V_{GS} = -1$ V.

It is observed that as $\mathrm{L_P}$ increases the tunneling barrier width at the drain–DP junction increases. However, increasing $\mathrm{L_P} > 40\ \mathrm{nm}$ does not further reduce BTBT on the drain-side. Therefore, optimum DP length, $\mathrm{L_{P,opt}} = 40\ \mathrm{nm}$ is chosen. In this work, therefore, $\mathrm{L_P} = 40\ \mathrm{nm}$ and $\mathrm{N_P} = 1.5 \times 10^{19}\ \mathrm{atoms/cm^3}$ have been considered as optimized pocket parameters for all the simulations.

It is worthy to point out that the optimum values of $\mathrm{N_P}$ and $\mathrm{L_P}$ are found to be independent of the drain doping ($\mathrm{N_D}$) for realistic doping levels $5 \times 10^{19}\ \mathrm{atoms/cm^3} \leq \mathrm{N_D} \leq 1 \times 10^{21}\ \mathrm{atoms/cm^3}$. However, the optimum values of $\mathrm{N_P}$ and $\mathrm{L_P}$ are found to be dependent on the gate length ($\mathrm{L_G}$). For example, for $\mathrm{L_G} = 50\ \mathrm{nm}$, $\mathrm{N_{P,opt}}$ and $\mathrm{L_{P,opt}}$ are found to be $1 \times 10^{19}\ \mathrm{atoms/cm^3}$ and 20 nm, respectively.

In this work, the gate length is taken as $100\ \mathrm{nm}$ since the effects of DP are easy to demonstrate and comprehend at longer device lengths. Nevertheless, the technique of using DP is found to be effective at lower gate lengths also, such as $50\ \mathrm{nm}$. However, when direct drain–to–source tunneling becomes a dominant mechanism of ambipolar conduction, as in silicon-based TFETs at $20\ \mathrm{nm}$ and below, DP is not able to modulate the electric field sufficiently to fully suppress the ambipolar conduction in the device. Therefore, in such cases, to suppress the ambipolar conduction, the technique of adding DP needs to be combined with other techniques that can reduce direct source–to–drain tunneling. However, the proposed technique can easily be applied on TFETs based on the nanowires proposed in [86, 87, 89] where the dimension in the axial direction is not constrained.

3.4 Device Characteristics of DP-DGTFET

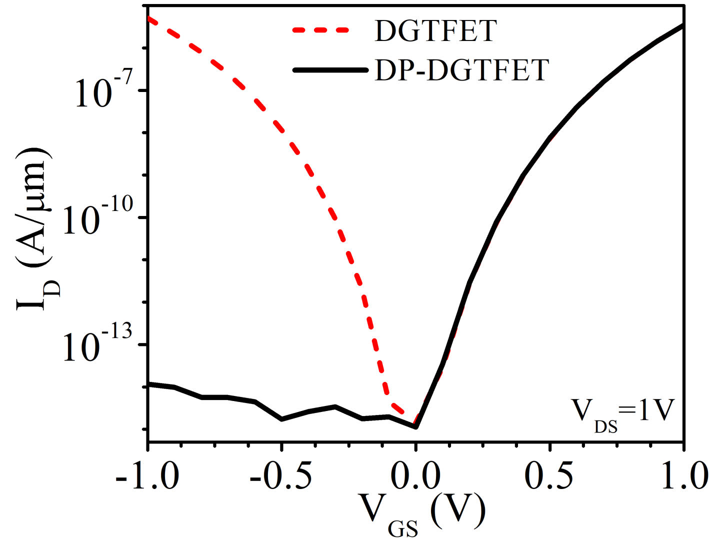


Figure 3.5: Transfer characteristics of DGTFET and DP-DGTFET.

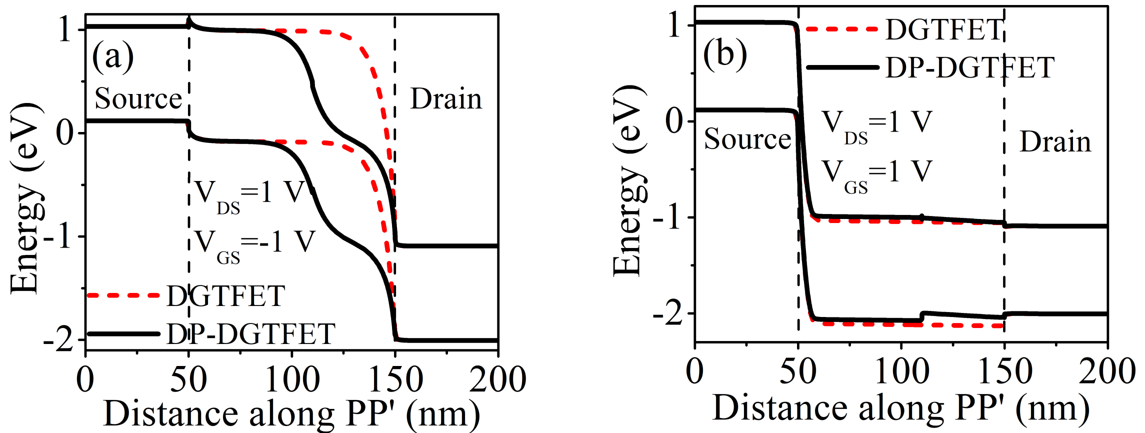


Figure 3.6: Energy band diagram of DGTFET and DP-DGTFET along the cutline PP′ in (a) Ambipolar state ($V_{DS} = 1$ V and $V_{GS} = -1$ V) (b) ON-state ($V_{DS} = 1$ V and $V_{GS} = 1$ V).

Fig. 3.5 compares the transfer characteristics of the DGTFET and DP-DGTFET. Firstly, it is noticed that the transfer characteristics of DGTFET and DP-DGTFET are similar for positive gate voltages. The addition of DP does not affect the I_{ON} and SS_{avg}. However, for the negative gate voltages, it is noticed

that $\mathrm{I_{AMB}}$ reduces from 5×10^{-6} A/μm in the DGTFET to 1×10^{-14} A/μm in the DP-DGTFET. The reason for the observed transfer characteristics can be understood from the band diagrams shown in Fig. 3.6(a) and Fig. 3.6(b). The band diagram of the devices in the ambipolar-state shown in Fig. 3.6(a) exhibits that the introduction of DP results in a considerable increase in the tunnel width and a large reduction in the overlap between the conduction band and the valence band. Consequently, a dramatic decrease in the $\mathrm{I_{AMB}}$ is obtained. The band diagrams in the ON-state shown in Fig. 3.6(b) demonstrate that the introduction of DP does not lead to any appreciable change in the ON-state, and the same $\mathrm{I_{ON}}$ is observed in the DGTFET and DP-DGTFET.

Further, the drain-induced barrier lowering (DIBL) has been analyzed for DGTFET and DP-DGTFET. DIBL is computed as the difference in the $\mathrm{V_{GS}}$ required to attain the drain current $\mathrm{I_{DIBL}} = 10^{-9}$ A/μm, at $\mathrm{V_{DS}} = 0.1$ V and at $\mathrm{V_{DS}} = \mathrm{V_{DD}} = 1$ V. Using simulations, the DIBL is found to be 22% for DGTFET as well as DP-DGTFET. Next, the $\mathrm{V_{th}}$ roll-off for the TFET is analyzed. It is calculated as the difference in the $\mathrm{V_{th}}$ at $\mathrm{L_{G,1}} = 100$ nm, and $\mathrm{L_{G,2}} = 50$ nm. Using simulations, the $\mathrm{V_{th}}$ is 656 mV for both the devices at $\mathrm{L_{G,1}} = 100$ nm and 640 mV at $\mathrm{L_{G,2}} = 50$ nm (we have taken $\mathrm{L_{G,2}} = 50$ nm since DP-DGTFET is scalable up to 50 nm gate length). Therefore, the $\mathrm{V_{th}}$ roll-off is 16 mV for both devices.

3.5 Impact of Process-Induced Variations

In realistic devices, it is difficult to obtain an exact doping concentration and maintain the alignment of the DP with respect to the gate electrodes, the intrinsic channel, and the drain regions [35, 130, 131]. Therefore, an important consideration for DP-DGTFET is to assess the impact of process-induced variations on the electrical parameters such as I_{AMB}.

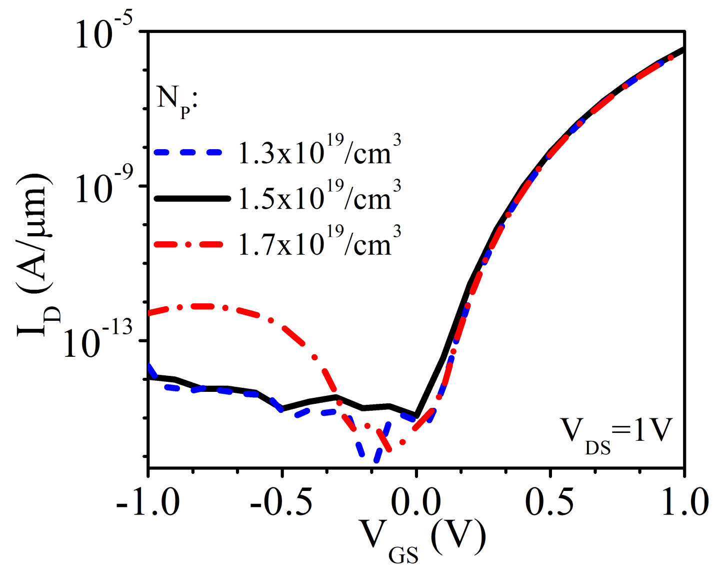


Figure 3.7: Transfer Characteristics of DP-DGTFET for small variations in N_P.

An initial estimate accounting for $\pm 10\%$ variations in N_P shows that I_{AMB} will increase to not more than $1\ \mathrm{pA}/\mu\mathrm{m}$ in the worst case, as shown in Fig. 3.7. The change in L_P and misalignment of $\pm 5\ \mathrm{nm}$ in the pocket with respect to the drain/gate edges are found to have no significant impact on the I_{AMB}.

3.6 DP combined with current enhancement techniques

With intensive research on TFETs carried out during the last decade, it is becoming apparent that various architectural modifications and material engineering in TFETs need to be appropriately combined to establish TFETs superiority over advanced CMOS technology [4]. Therefore, DGTFET employing drain pocket can be combined with techniques used to tackle other problems, such as, low I_{ON}, to improve the overall electrical characteristics of the device. From this perspective, the performance of DP-DGTFET combined with (a) strained-silicon body and (b) addition of the source-pocket is evaluated.

3.6.1 Effect of addition of Drain-Pocket on Strained-DGTFET

Considering future CMOS applications, the effectiveness of the proposed technique is demonstrated on device with the following modifications to the DGTFET:

1. lower bandgap (by using strained-silicon)
2. higher gate-dielectric ($\epsilon_r = 21$)
3. lower supply voltage ($V_{DD} = 0.5$ V)
4. lower gate length ($L_G = 50$ nm)

In this section, the technique of employing DP is demonstrated on Strained-DGTFET (SDGTFET). An SDGTFET is composed of a strained silicon body

rather than normal silicon. It can be fabricated using the strained–silicon–on–insulator (s-SOI) technology. The amount of strain is controlled by varying the Ge mole fraction (x) in the SiGe buffer layer used during its fabrication. Due to the introduction of strain in silicon, the bandgap and the effective mass of carriers decreases, and the electron affinity increases [41, 46, 132]. These effects can be modelled as in Eq. 3.1 [46, 132].

$$\Delta(E_g)_{s-Si} = 0.4x \tag{3.1}$$

$$\Delta(E_c)_{s-Si} = 0.57x \tag{3.2}$$

$$V_T \; ln \left(\frac{N_{V,Si}}{N_{V,s-Si}} \right) = V_T \; ln \left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}} \right)^{3/2} \approx 0.075 \; x \tag{3.3}$$

where $\mathrm{(E_g)_{s-Si}}$ is the decrease in the bandgap of silicon due to strain, $\mathrm{(E_c)_{s-Si}}$ is the increase in electron affinity of silicon due to strain, $\mathrm{V_T}$ is the thermal voltage, $\mathrm{N_{V,Si}}$ and $\mathrm{N_{V,s-Si}}$ are the density of states (DOS) in the valence band in the normal and strained silicon, respectively, $\mathrm{m^*_{h,Si}}$ and $\mathrm{m^*_{h,s-Si}}$ are the hole DOS effective masses in normal and strained-silicon, respectively.

The simulator calculates the change in bandgap and the electron affinity for the strained silicon, using the Eq. 3.1 and 3.2 for a given x. To calculate the change in the effective density of states and the hole DOS effective mass in the strained silicon for a given x, the simulator uses Eq. 3.3 and the standard values

of $\mathrm{N_{V,Si}}$ and $\mathrm{m^*_{h,Si}}$ given in [50]. The effects of warping and non-parabolicity are not considered in this study. The mobility of the carriers is also affected due to the presence of strain; however, the effect of mobility on the characteristics of a TFET is somewhat limited [132]. A concentration and strain-dependent mobility model as reported in [133] is used in this study.

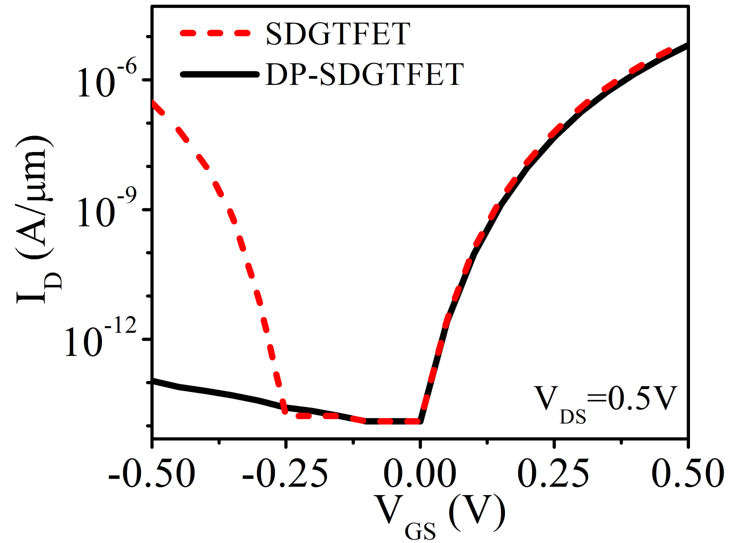


Figure 3.8: Transfer Characteristics of SDGTFET and DP-SDGTFET.

The x is taken as 0.5 in this work. The optimum parameter value for the DP that suppresses the $\mathrm{I_{AMB}}$ is found to be: $\mathrm{L_P} = 20\ \mathrm{nm}$ and $\mathrm{N_P} = 2.5 \times 10^{19}$ $\mathrm{atoms/cm^3}$ respectively. The transfer characteristics of the SDGTFET and DP-SDGTFET are compared in Fig. 3.8 showing that $\mathrm{I_{AMB}}$ reduces from 4×10^{-7} $\mathrm{A}/\mu\mathrm{m}$ in SDGTFET to 10^{-13} $\mathrm{A}/\mu\mathrm{m}$ in DP-SDGTFET, thus, illustrating the effectiveness of DP in suppressing the $\mathrm{I_{AMB}}$.

3.6.2 Effect of addition of Drain-Pocket on DGTFET with Source Pocket

Several researchers have demonstrated that the introduction of a highly doped pocket adjacent to the source and having an appropriate thickness results in an improvement in the I_{ON} and the SS_{avg} [67, 68, 131, 134, 135]. Since the type of doping of a source-pocket (SP) and a DP is the same, the two pockets can potentially be fabricated with the same doping concentration to reduce additional fabrication cost and achieving an improved I_{ON}/I_{OFF} ratio.

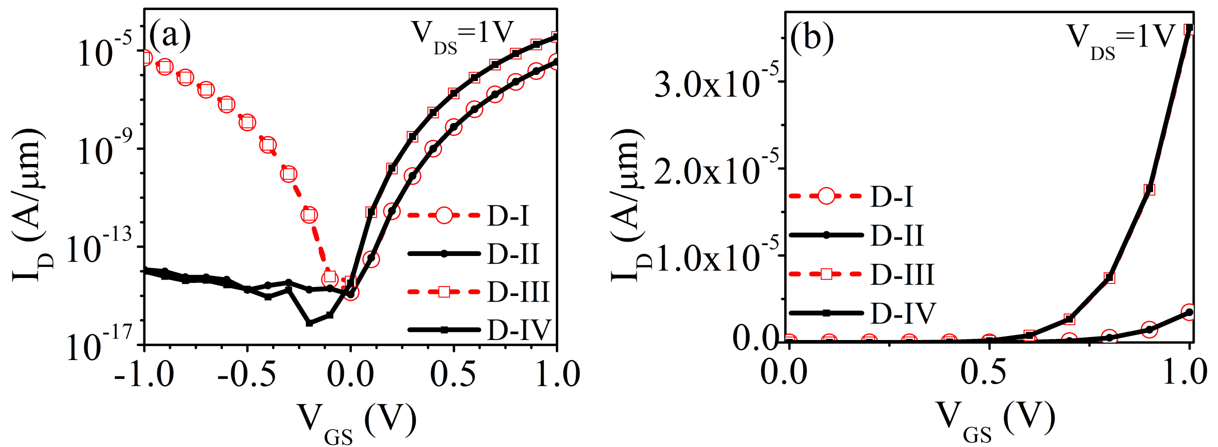


Figure 3.9: Transfer characteristics of Device I (D-I): DGTFET, Device II (D-II): DP-DGTFET, Device III (D-III): DGTFET with SP, Device IV (D-IV): DP-DGTFET with SP (a) in log scale (b) in linear scale.

Table 3.2: Performance comparison of Device I: DGTFET, Device II: DP-DGTFET, Device III: DGTFET with SP, Device IV: DP-DGTFET with SP at $V_{DD} = 1$ V

Device	I_{ON} (μA/μm)	I_{AMB} (μA/μm)	SS_{avg} (mV/dec)
Device I	3	6	83
Device II	3	10^{-8}	83
Device III	36	6	62
Device IV	36	10^{-8}	62

Fig. 3.9(a) and 3.9(b) compares the transfer characteristics and Table 3.2 summarizes the important electrical parameters of DGTFETs with/without DP

and with/without SP. The same doping concentration has been used for the SP and the DP. The addition of DP increases the tunneling barrier width inhibiting the BTBT on the drain-side and decreases the I_{AMB}. The addition of SP decreases the tunneling barrier width on the source side and boosts the I_{ON}. From Fig. 3.9, it can be noticed that in devices II and IV, the I_{AMB} is suppressed due to the addition of DP, compared to the device I and III which do not contain DP. It is worthy to point out that the addition of DP does not affect the I_{ON} of the devices. Therefore, the I_{ON} of devices I and II are the same. Similarly, the I_{ON} for devices III and IV are the same. Additionally, devices III and IV have higher I_{ON} compared to devices I and II due to the inclusion of SP. Therefore, DP-DGTFET with an SP (device IV) shows superior characteristics.

3.7 Comparison with some other ambipolar suppression techniques

It is worthy to point out that the most common technique to reduce I_{AMB} in a TFET is to use a lower drain doping than the source doping. It is commonly referred to as the asymmetric-doped drain technique. Therefore, a detailed comparison of the proposed device with the asymmetric-doped drain technique is done.

For DGTFETs, several researchers have used a lower drain doping ($N_D = 5 \times 10^{18}\ \mathrm{atoms/cm^3}$) for suppressing I_{AMB} [7,46,99,131,134]. However, it has been found that using lower drain doping is not as effective as the introduction of DP in suppressing I_{AMB}. To illustrate this, transfer characteristics of the

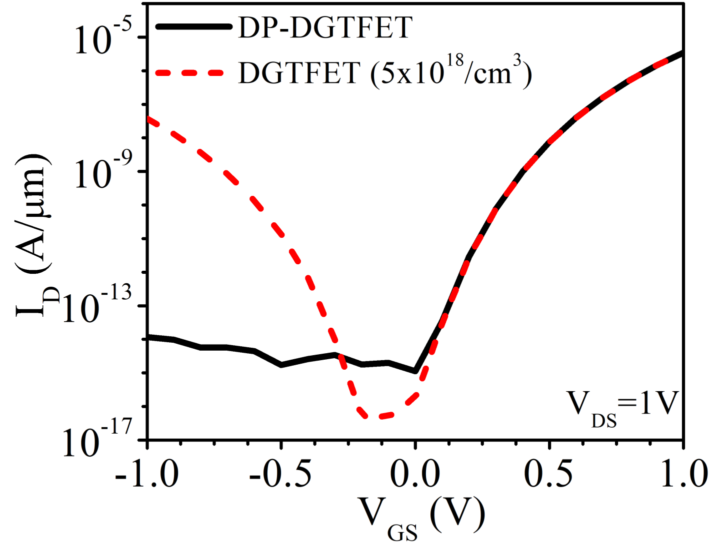


Figure 3.10: Comparison of transfer characteristics of a DP-DGTFET and an asymmetric-doped DGTFET ($N_D = 5 \times 10^{18}$ atoms/cm^3).

DP-DGTFET and the DGTFET with the asymmetric-doped drain technique with $N_D = 5 \times 10^{18}$ atoms/cm^3 have been compared in Fig. 3.10. It can be seen that in a DGTFET with the asymmetric-doped drain, $I_{AMB} = 5 \times 10^{-8}$ A/μm and is still high even with a low drain doping of $N_D = 5 \times 10^{18}$ atoms/cm^3. However, with DP-DGTFET, the ambipolar conduction is fully suppressed, and $I_{AMB} = 1 \times 10^{-14}$ A/μm is achieved. Additionally, asymmetric-doped DGTFET results in undesirable high drain access resistance due to lower drain doping. However, employing DP in a TFET allows us to keep drain doping as high as 1×10^{20} atoms/cm^3 (similar to the source doping), resulting in lower access resistance and possibly, less number of ion implantation steps required in fabricating CMOS-type circuits.

It is also important to note that the high tunnel resistance in series with the drain access resistance can mask the utility of low drain access resistance for

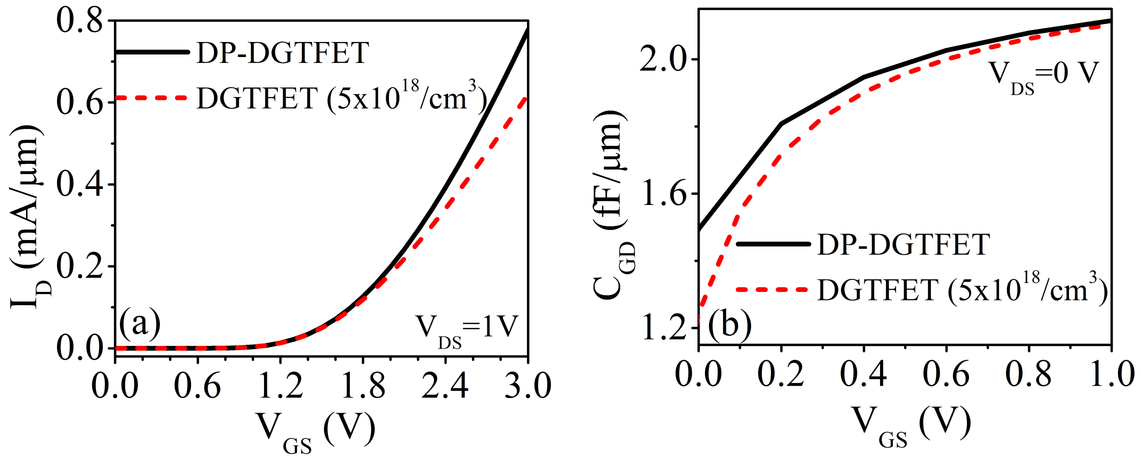


Figure 3.11: Comparison of DP-DGTFET and asymmetric-doped DGTFET ($N_D = 5 \times 10^{18}$ atoms/cm^3) (a) Transfer characteristics up to $V_{GS} = 3$ V illustrating higher current in DP-DGTFET (b) C_{GD}.

TFETs [49]. In future TFETs, with the advancement in materials used for making TFETs, the tunnel resistance is expected to decrease, and the importance of the proposed technique may become more evident. The impact of lower access resistance in DP-DGTFET compared to asymmetric-doped DGTFET can be observed at higher gate voltages such that the tunnel resistance decreases and becomes comparable to the drain access resistance. Fig. 3.11(a) illustrates that the lower drain access resistance in a DP-DGTFET result in a 30% increase in the drain current at $V_{GS} = 3$ V.

An important consideration in designing a DP-DGTFET is the expected increase in the gate capacitance due to increased doping near the drain compared to low-doped DGTFET. The capacitance between the gate and drain (C_{GD}) of the proposed structure is examined. In a TFET, C_{GD} has a dominant role compared to the capacitance between gate and source (C_{GS}). The C_{GD} determines the overall gate capacitance [58, 122, 136, 137]. Fig. 3.11(b) compares the C_{GD} of

the DP-DGTFET and asymmetric-doped DGTFET. The value of ON-state $\mathrm{C_{GD}}$ is around 2 $\mathrm{fF}/\mu\mathrm{m}$ for both devices. Under other bias conditions ($\mathrm{V_{GS}} < 1$ V), there is only a marginal increase in $\mathrm{C_{GD}}$ due to DP, indicating that the DP is not expected to degrade the performance of the devices significantly.

Table 3.3: Comparison of ambipolar behaviour of DP-DGTFET with TFETs employing other techniques to control ambipolar conduction

Device Structure	$\mathrm{L_G}$ (nm)	$\mathrm{N_D}$ ($\mathrm{atoms/cm^3}$)	$\mathrm{V_{DD}}$ (V)	EOT	$\mathrm{I_{AMB}}$ ($\mathrm{A}/\mu\mathrm{m}$)	$\mathrm{V_{OFF,2}}$ (V)
[1] Asymmetric TFET [7,46]	100	5×10^{18}	1	3	5×10^{-8}	-0.2
Gate–Drain Overlap [58]	100	1×10^{19}	1	3	10^{-9}	-0.5
HDB TFET [47]	100	5×10^{18}	1	3	10^{-13}	-0.8
[1] Non-uniform drain-doped TFET [118, 121]	100	1.5×10^{19} and 1×10^{20}	1	3	6×10^{-7}	-0.1
This Work	100	1×10^{20}	1	3	10^{-14}	-1

[1] For these techniques, the exact values of $\mathrm{I_{AMB}}$ and $\mathrm{V_{OFF,2}}$ are not available in literature. For a fair comparison, we have incorporated the techniques in the device with parameters listed in Table 3.1 and extracted the values of $\mathrm{I_{AMB}}$ and $\mathrm{V_{OFF,2}}$.

Additionally, the effectiveness of the proposed technique in suppressing the $\mathrm{I_{AMB}}$ is compared with some of the techniques already proposed in the literature. The comparison is summarized in Table 3.3. It is evident that the proposed technique shows lower $\mathrm{I_{AMB}}$ compared to other techniques. Additionally, the $\mathrm{V_{OFF}}$ of the proposed technique is $-\mathrm{V_{DD}}$, implying that the $\mathrm{I_{AMB}}$ is fully suppressed in negative gate bias condition, which is not attainable by any other technique listed in Table 3.3. It is also worthy to note that all other techniques listed in Table 3.3, use a lower drain doping compared to source doping ($\mathrm{N_S} = 1\times10^{20}$ $\mathrm{atoms/cm^3}$). It results in an increased access resistance. However, the proposed technique removes this drawback.

3.8 Summary

The technique of the addition of drain-pocket in DGTFETs is explored as an effective means to suppress the ambipolar conduction in a TFET. It works even at high negative gate voltages and drain doping as high as source doping. It is demonstrated that including DP in a DGTFET minimizes the energy band overlap and increases the tunneling barrier width at the drain-side, and effectively suppresses the I_{AMB}. However, a marginal increase in C_{GD} is observed under certain conditions. Additionally, the issues arising out of the fabrication of pockets and process-induced variations need careful evaluation. Nevertheless, interesting attributes of DP are worth experimenting with for futuristic TFETs that are based on nanowires, III–V semiconductors, and other small bandgap materials.

Chapter 4

Improving the scalability of SOI-based TFETs

TFETs are known to exhibit higher OFF-state leakage current at smaller channel lengths, primarily due to direct source–to–drain BTBT [33, 34]. As a result, the biggest advantage of TFET to achieve steeper $\mathrm{SS_{avg}}$ is lost at smaller gate lengths [33, 34, 59, 98, 99]. Additionally, TFETs are prone to short-channel effects (SCE) such as drain-induced barrier lowering (DIBL) and threshold voltage ($\mathrm{V_{th}}$) roll-off [4, 34, 98]. Therefore, the scalability of TFETs, which is critical for employing them in futuristic circuits, needs to be examined carefully.

In this chapter, it is proposed to add a ground plane (GP) in silicon–on–insulator (SOI) TFET and analyze its efficacy in extending the scalability of the device. The addition of ground plane in buried-oxide (GPB structure) has been demonstrated earlier to improve the performance of the MOSFET in [138]. It has been demonstrated that GBP suppresses DIBL in SOI-MOSFET by acting as a sink to the drain electric field. However, since the operating principles

of MOSFETs and TFETs are different, the application of GP in TFETs is not straightforward. Hence, in this chapter, the addition of GP in the buried-oxide of an SOI-TFET has been explored. It is shown that the introduction of the GP helps in depleting the drain and increases the effective drain–to–source distance. It inhibits the direct source–to–drain tunneling even at lower gate lengths such as $10\,\mathrm{nm}$. Thus, it improves the scalability of the device. Additionally, this technique reduces $\mathrm{I_{OFF}}$ and improves the $\mathrm{SS_{avg}}$ for small channel lengths.

4.1 Device Structure and Simulation Model

Table 4.1: Device Parameters used in the simulation of conventional TFET and GP-TFET

Parameter	**Value**
Supply voltage $(\mathrm{V_{DD}})$	1.0 V
Silicon film thickness $(\mathrm{t_{si}})$	$10\ \mathrm{nm}$
Gate oxide thickness $(\mathrm{t_{ox}})$	3 nm (EOT$\approx$ 0.5)
Gate work-function (ϕ_{m})	$4.17\ \mathrm{eV}$
Source doping $(\mathrm{N_S})$ (p-type)	$1\times10^{20}\ \mathrm{atoms/cm^3}$
Drain doping $(\mathrm{N_D})$ (n-type)	$5\times10^{18}\ \mathrm{atoms/cm^3}$
Channel doping $(\mathrm{N_C})$ (p-type)	$1\times10^{17}\ \mathrm{atoms/cm^3}$
Gate length $(\mathrm{L_G})$	$10-50\ \mathrm{nm}$
BOX thickness $(\mathrm{t_{box}})$	$60\ \mathrm{nm}$
GP doping $(\mathrm{N_{gp}})$ (p-type)	$1\times10^{20}\ \mathrm{atoms/cm^3}$
GP Depth $(\mathrm{d_{gp}})$	$2-10\ \mathrm{nm}$
GP Thickness $(\mathrm{t_{gp}})$	$10\ \mathrm{nm}$

SOI-based n-TFET consists of a thin silicon film over buried-oxide (BOX) made up of $(\mathrm{SiO_2})$ with $\mathrm{p^+}$ doped source and $\mathrm{n^+}$ doped drain. The gate dielectric material is assumed to be $\mathrm{HfO_2}$ ($\epsilon_{\mathrm{r}}\approx 21$). This conventional SOI-based n-TFET is referred to as C-TFET in this chapter. The proposed TFET consists of a heavily doped $\mathrm{p^+}$ layer, known as a ground plane (GP), inside BOX at depth $\mathrm{d_{gp}}$. This device is referred to as GP-TFET in this chapter. The GP-TFET

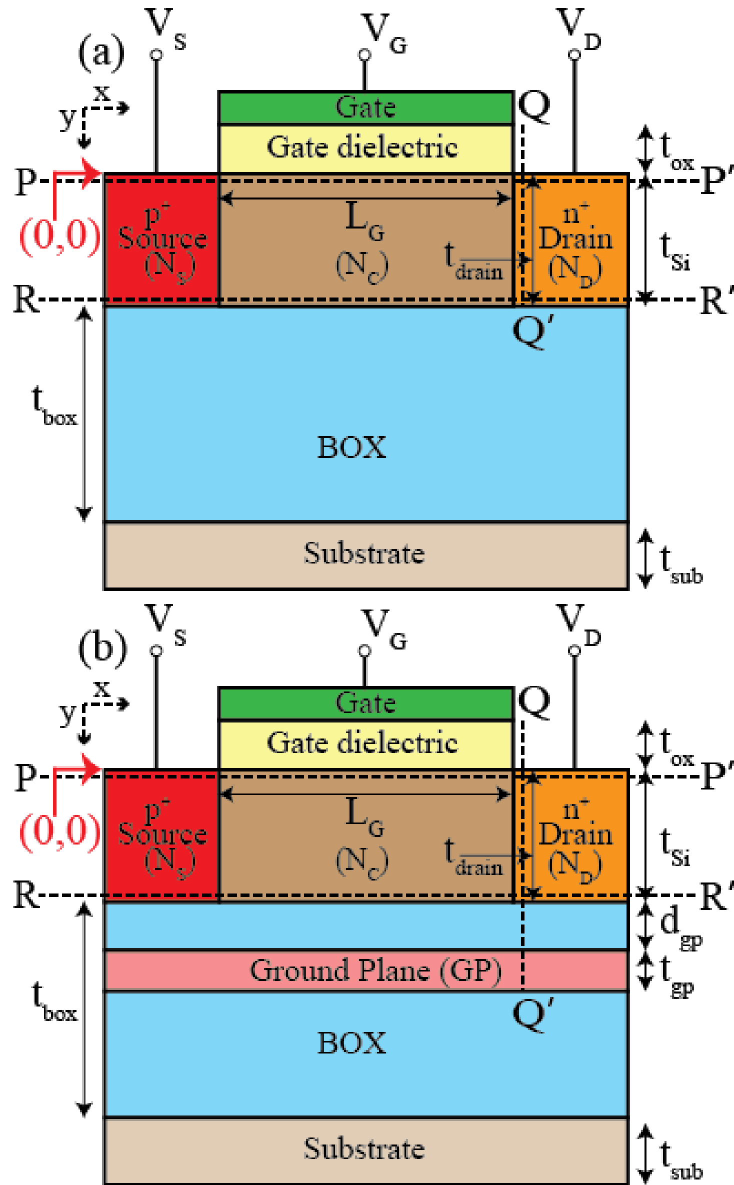


Figure 4.1: Schematic cross-sectional view of (a) C-TFET (b) GP-TFET.

structure can be created using the Silicon–on–insulator–with–active–substrate (SOIAS) technology [139, 140]. The structure can be implemented easily using the FDSOI CMOS process since the TFETs are compatible with CMOS in terms of fabrication [32, 141–143]. The GP is created by ion-implantation of boron through the silicon film [138]. Since the GP is throughout the length of the device, GP can be formed before the formation of the gate, drain, and source

areas in the device fabrication flow. Fig. 4.1(a) and 4.1(b) shows the schematic cross-sectional view of a C-TFET and a GP-TFET. The device parameters used in the simulations are listed in Table 4.1.

4.2 Analysis of a GP-TFET

4.2.1 Transfer Characteristics of GP-TFET

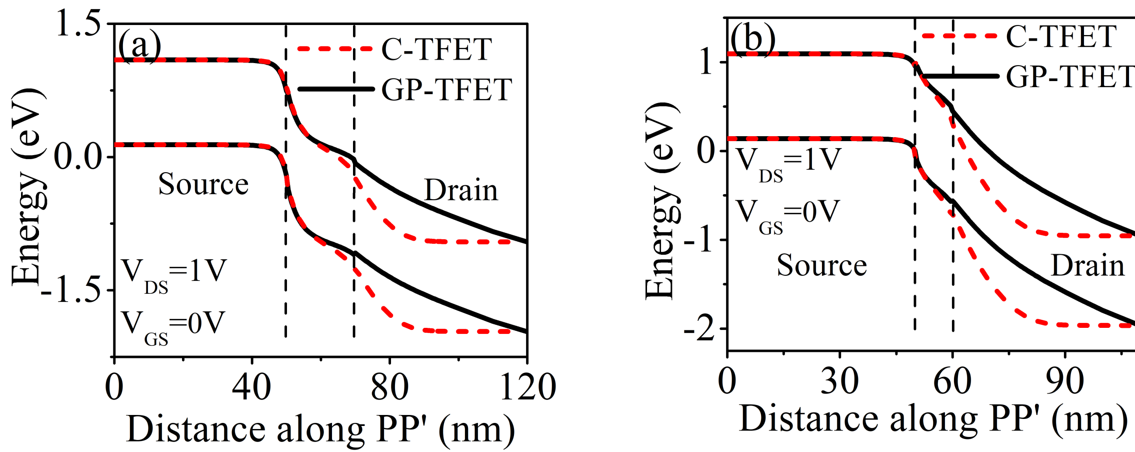


Figure 4.2: Energy band diagrams of C-TFET and GP-TFET along the cutline PP′ in the OFF-state (a) $L_G = 20$ nm (b) $L_G = 10$ nm.

The motivation behind the introduction of the ground plane is to deplete the drain and increase the effective drain–to–source distance. Fig. 4.2(a) shows the band diagrams of C-TFET and GP-TFET for $L_G = 20$ nm in the OFF-state. It can be seen that for the GP-TFET, the bending of the energy bands extends more into the drain region compared to the C-TFET, indicating the extension of the depletion region inside the drain. This results in an increased effective drain–to–source distance in GP-TFET compared to C-TFET. As a result, the direct source–to–drain tunneling is inhibited in GP-TFET. Moreover, the band diagrams for C-TFET and GP-TFET for $L_G = 10$ nm are shown in the Fig. 4.2(b). It

can be observed that at $L_G = 10$ nm, the problem is aggravated by an increased direct source–to–drain tunneling in C-TFET. However, direct source–to–drain tunneling is suppressed in GP-TFET even at $L_G = 10$ nm.

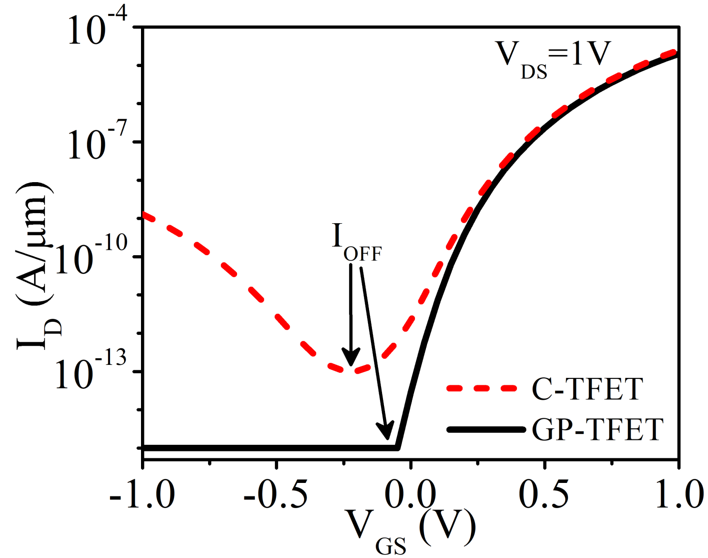


Figure 4.3: Transfer characteristics for $L_G = 20$ nm.

The transfer characteristics of C-TFET and GP-TFET at $L_G = 20$ nm are compared in Fig. 4.3. From Fig. 4.3, it can be inferred that the I_{OFF} decreases from 5×10^{-10} A/μm in C-TFET to 1×10^{-15} A/μm in the GP-TFET. The reduction in I_{OFF} can be attributed to the increased effective drain–to–source distance which suppresses the direct source–to–drain tunneling in GP-TFET. Additionally, SS_{avg} (averaged over 8 decades of current) improves from 104 mV/dec in C-TFET to 62 mV/dec in GP-TFET.

4.2.2 Scaling trend of GP-TFET

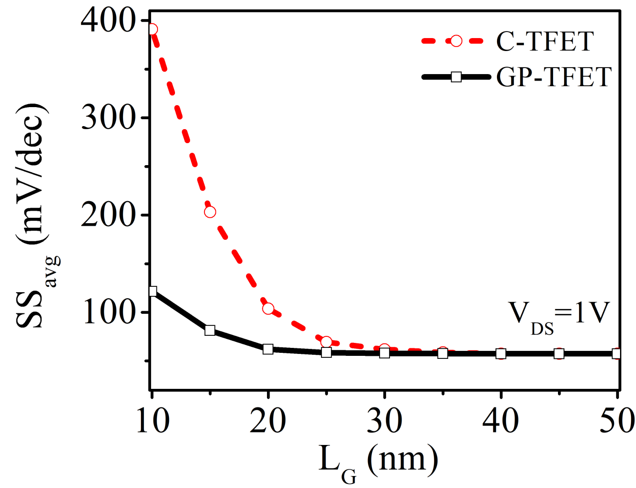


Figure 4.4: Scaling trend of $\mathrm{SS_{avg}}$ for C-TFET and GP-TFET.

Fig. 4.4 shows the device scaling trend for $\mathrm{SS_{avg}}$ exhibiting the superior scalability of GP-TFET compared to C-TFET, especially for $\mathrm{L_G} \leq 20$ nm. The improvement in the scalability of GP-TFET can be attributed to the depletion of majority carriers in the drain, as explained below.

4.2.2.1 Impact of $\mathrm{d_{gp}}$ in a GP-TFET

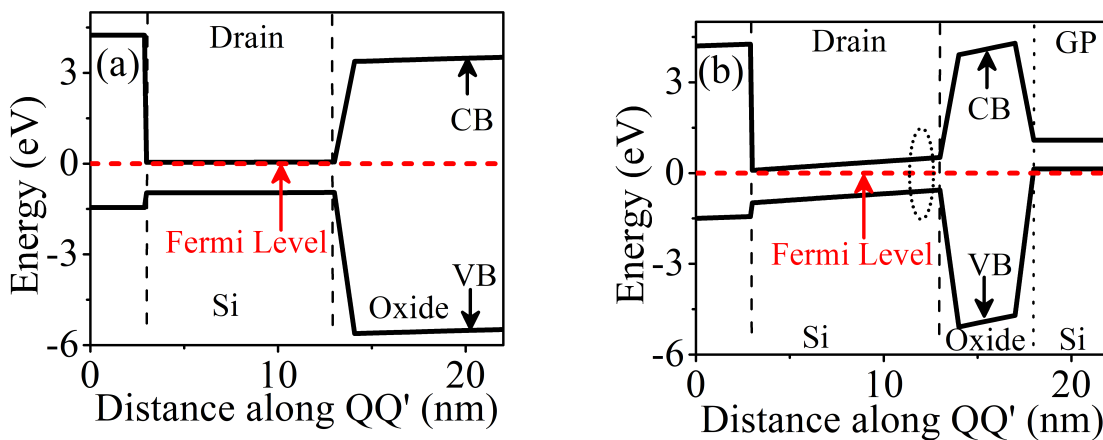


Figure 4.5: Energy band diagrams in (a) C-TFET (b) GP-TFET at $\mathrm{V_{DS}} = \mathrm{V_{GS}} = 0$ V for $\mathrm{L_G} = 20$ nm along the cutline QQ$'$.

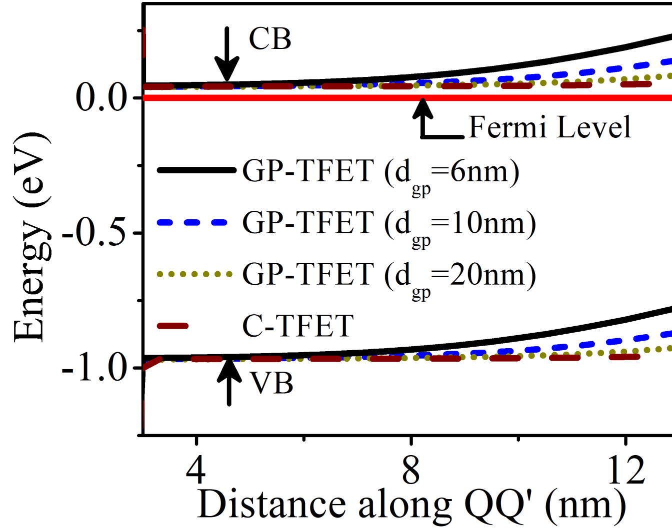


Figure 4.6: Impact of increase in $\mathrm{d_{gp}}$ on the energy band diagram in the drain region along the cutline QQ′ (as shown in Fig. 4.1) at $\mathrm{V_{DS}} = \mathrm{V_{GS}} = 0$ V for $\mathrm{L_G} = 20$ nm.

Fig. 4.5(a) and 4.5(b), respectively, show the band diagrams along Y-axis in drain for the C-TFET and GP-TFET at equilibrium. It is evident that in GP-TFET, due to the insertion of GP, the drain gets depleted, especially close to the BOX, as shown in the encircled region. However, it should be noted that the depth of GP ($\mathrm{d_{gp}}$) plays an important role in the depletion of the drain region. Fig. 4.6 shows the impact of the increase in $\mathrm{d_{gp}}$ on the band diagrams along the Y-axis in the drain for C-TFET and GP-TFET. It can be seen that as $\mathrm{d_{gp}}$ increases, the conduction band comes closer to the Fermi level, and the drain is less depleted. For a very high value of $\mathrm{d_{gp}}$, the drain depletion ceases, and the band profile becomes almost similar to the C-TFET. The improvement in scalability is found to disappear when $\mathrm{d_{gp}} > 10$ nm.

4.2.2.2 Impact of N_{gp} and t_{gp} in a GP-TFET

It is important to analyze the impact of doping of GP (N_{gp}) on the electrical characteristics of GP-TFET. Using simulations, it is found that varying the N_{gp} by $\pm 50\%$ around $N_{gp} = 1 \times 10^{20}$ atoms/cm^3 does not degrade the ambipolar performance. Moreover, the maximum change in the I_{ON} by the variation of N_{gp} in the above-mentioned range is 6.2%. Similarly, it is important to analyze the impact of t_{gp} on the performance of GP-TFET. Using simulations, it is observed that even $\pm 50\%$ variation in t_{gp} around $t_{gp} = 10$ nm does not impact the characteristics of the GP-TFET. The maximum change in the I_{ON} by the variation of t_{gp} in the above-mentioned range is 2.8%.

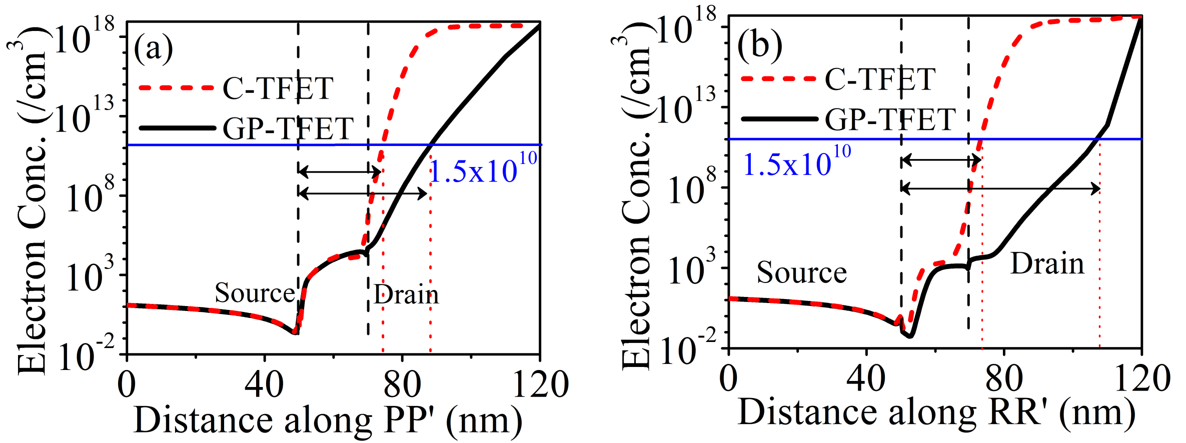


Figure 4.7: Electron concentration for C-TFET and GP-TFET at $V_{DS} = 1$ V and $V_{GS} = 0$ V for $L_G = 20$ nm (a) along the cutline PP′ (b) along the cutline RR′.

Next, Fig. 4.7(a) and 4.7(b), respectively, compares the electron concentration across the cutline PP′ and RR′ for $L_G = 20$ nm. It is evident that the electron concentration in the drain region is much lower in GP-TFET than C-TFET, indicating the extension of the depletion region into the drain in GP-TFET. The effective drain–to–source distance can be defined as the distance between

the metallurgical source–channel junction and the point in the drain where the electron concentration becomes equal to the intrinsic carrier concentration ($\mathrm{n_i} = 1.5 \times 10^{10}\ \mathrm{atoms/cm^3}$). It is observed that the effective drain–to–source distance increases from $22\ \mathrm{nm}$ in C-TFET to $34\ \mathrm{nm}$ for GP-TFET for cutline PP$'$ and from $22\ \mathrm{nm}$ in C-TFET to $54\ \mathrm{nm}$ for GP-TFET for cutline RR$'$. This results in improving the scalability using the ground plane. Another important point to note is that the effective drain–to–source distance increases throughout the thickness of the silicon body (both along the cutline PP$'$ and RR$'$) in GP-TFET. This can be attributed to the thin silicon body ($\mathrm{t_{si}} = 10\ \mathrm{nm}$) and is important for improving the scalability of the device.

The addition of GP is known to improve the scalability of a MOSFET by improving the electrostatics of the device [138]. Therefore, it is important to assess if the improvement in the scalability in TFET can be attributed to improved electrostatics. This work shows that the mechanism of improvement in scalability due to GP is quite different in a TFET compared to a MOSFET. In a MOSFET, the scalability improvement is due to the GP providing a sink to the electric field such that the electric field lines from the drain cannot reach the source directly. However, in a TFET, the introduction of GP results in the depletion of the drain region resulting in increased effective drain–to–source distance and suppression of direct source–to–drain tunneling that becomes dominant at smaller gate lengths. Therefore, in a TFET, the improvement in scalability cannot solely be attributed to improved electrostatics but also to the increased effective drain–to–source distance that suppresses direct source–to–drain tunneling.

4.2.3 Short-Channel performance of GP-TFET

In this section, the short-channel effects such as DIBL and V_{th} roll-off are analyzed for C-TFET and GP-TFET.

4.2.3.1 DIBL

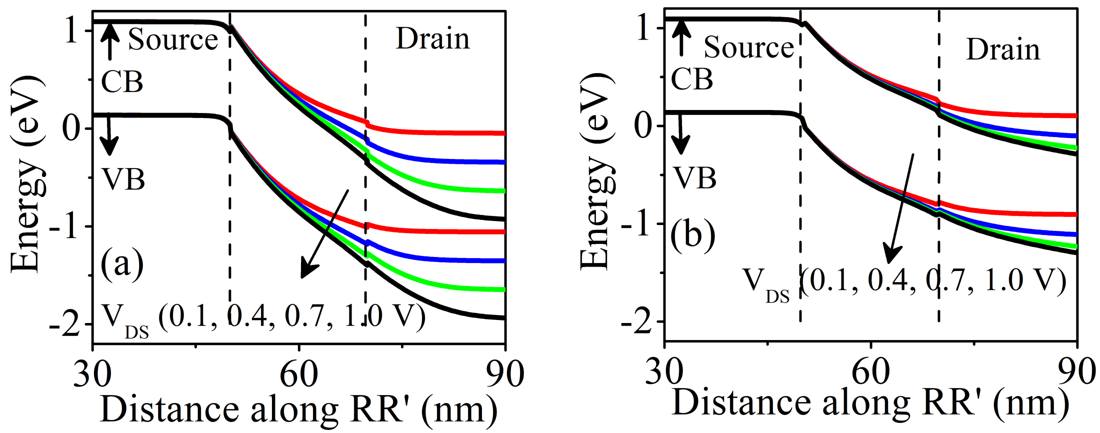


Figure 4.8: Energy band Diagram of (a) C-TFET and (b) GP-TFET along the cutline RR′ at $L_G = 20$ nm and $V_{GS} = 0.1$ V.

Fig. 4.8(a) and 4.8(b) compare the effect of drain–source voltage on the band diagrams of C-TFET and GP-TFET, respectively. It is evident that the drain voltage has a more pronounced effect on the tunneling barrier in the C-TFET compared to the GP-TFET. This implies that the GP-TFET is expected to exhibit a lower DIBL compared to C-TFET.

To quantify the DIBL effect, the difference in the V_{GS} required to attain the same drain current, at low V_{DS} and at $V_{DS} = V_{DD}$ is measured. The DIBL can be computed at drain current $I_{DIBL} = 10^{-9}$ A/μm as follows [46]:

$$DIBL = \frac{V_{GS,2} - V_{GS,1}}{V_{DS,2} - V_{DS,1}} \tag{4.1}$$

where, $V_{GS,2}$ is the gate–source voltage at which $I_D = I_{DIBL}$ and $V_{DS} = V_{DS,2} = V_{DD}$. Similarly, $V_{GS,1}$ is the gate–source voltage at which $I_D = I_{DIBL}$ and $V_{DS} = V_{DS,1} = 0.1$ V.

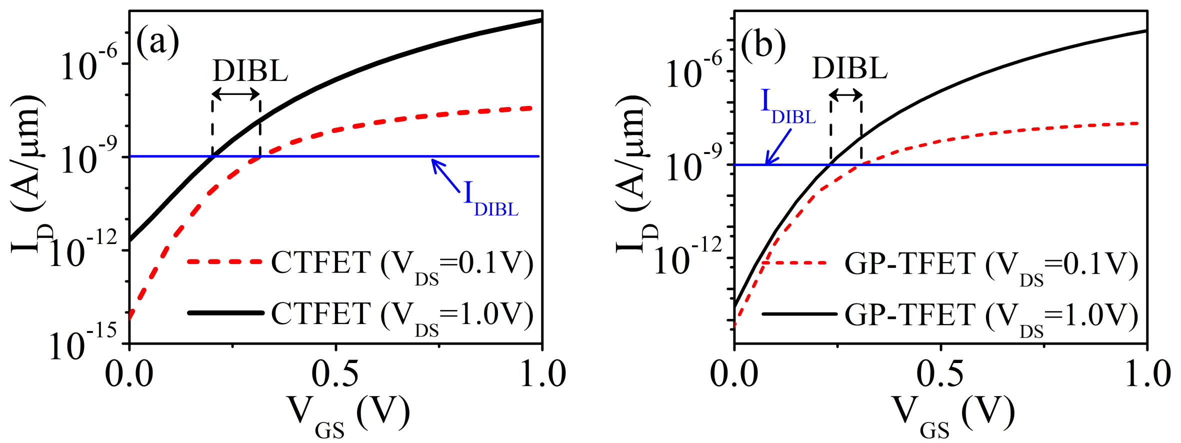


Figure 4.9: Transfer characteristics of (a) C-TFET (b) GP-TFET at $L_G = 20$ nm highlighting DIBL.

Fig. 4.9(a) shows the transfer characteristics of C-TFET at $V_{DS} = 0.1$ V and $V_{DS} = 1.0$ V for $L_G = 20$ nm. For the C-TFET, the transfer characteristics are highly dependent on the V_{DS} and the extracted value of DIBL is 121 mV/V. Fig. 4.9(b) shows the transfer characteristics of GP-TFET at $V_{DS} = 0.1$ V and $V_{DS} = 1.0$ V. The extracted value of DIBL is 81 mV/V for GP-TFET. Therefore, the DIBL is suppressed by 33%.

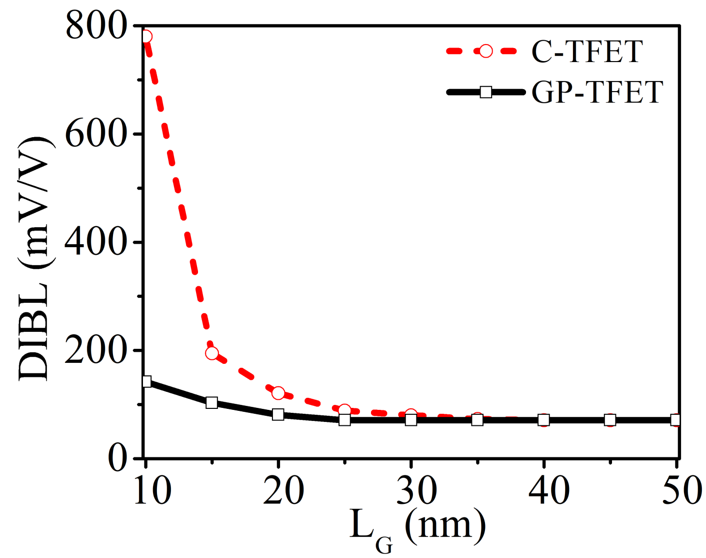


Figure 4.10: Scaling trend of DIBL characteristics for C-TFET and GP-TFET.

Fig. 4.10 shows the DIBL at different gate lengths, both for C-TFET and GP-TFET. For $\mathrm{L_G} < 20\ \mathrm{nm}$, the GP-TFET exhibits significantly lower DIBL compared to C-TFET.

4.2.3.2 $\mathrm{V_{th}}$ roll-off

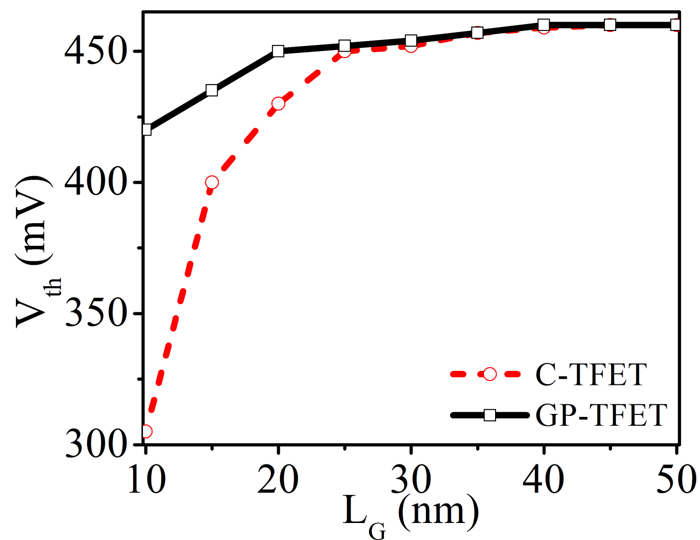


Figure 4.11: Comparison of $\mathrm{V_{th}}$ roll-off for C-TFET and GP-TFET.

Next, the V_{th} roll-off for the TFET is analyzed. Fig. 4.11 shows the V_{th} of C-TFET and GP-TFET at different gate lengths. It is evident that there is an appreciable V_{th} roll-off in C-TFET compared to GP-TFET. To quantify V_{th} roll-off, the change in V_{th} can be computed as follows:

$$\Delta V_{th} = V_{th,L_G=L1} - V_{th,L_G=L2} \tag{4.2}$$

where, $V_{th,L_G=L1}$ is the threshold voltage at $L_G = L1$ and $V_{th,L_G=L2}$ is the threshold voltage at $L_G = L2$. Here, $L1 = 50$ nm and $L2 = 10$ nm. ΔV_{th} is found to be 155 mV for C-TFET. However, for GP-TFET, ΔV_{th} is 40 mV. Therefore, the V_{th} roll-off is suppressed by 74% in GP-TFET.

4.3 Ambipolar Behaviour of GP-TFET

In this section, the ambipolar behaviour of GP-TFET is analyzed.

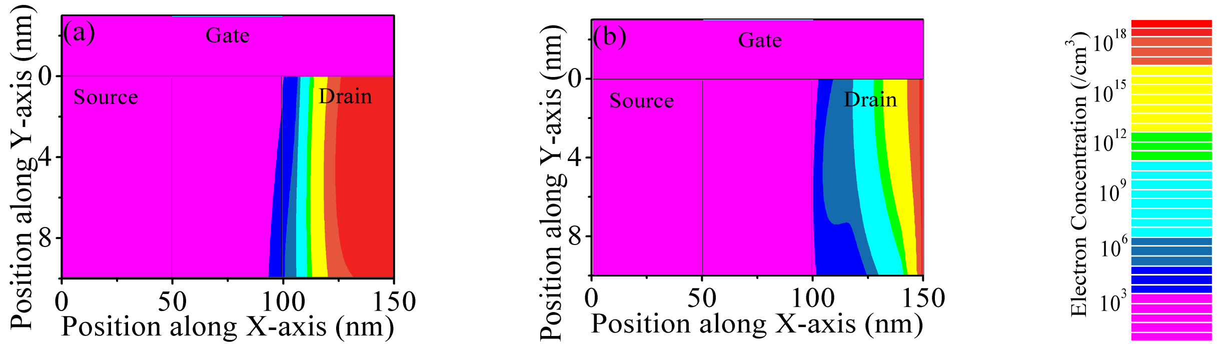


Figure 4.12: Electron concentration for (a) C-TFET and (b) GP-TFET at $V_{DS} = 1$ V and $V_{GS} = -1$ V for $L_G = 50$ nm.

Since, addition of the GP results in the drain depletion at the drain–channel interface, BTBT is expected to be suppressed in GP-TFET. Fig. 4.12 shows the electron concentration for GP-TFET and C-TFET in the ambipolar state. Using

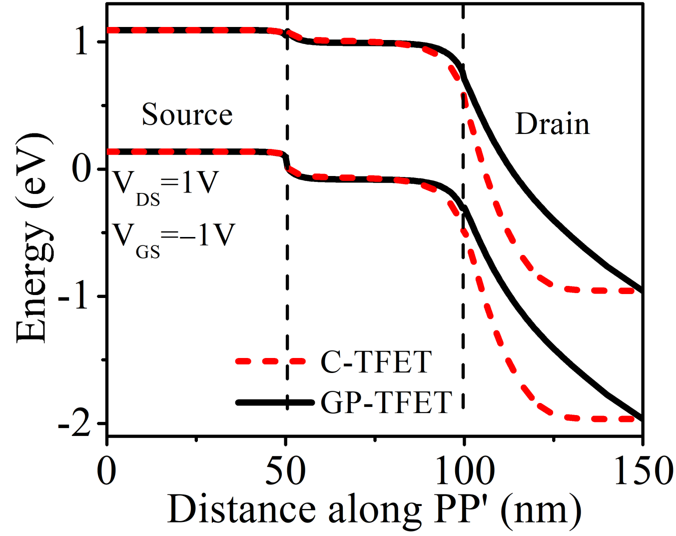


Figure 4.13: Energy band diagram along the cutline PP′ (as shown in Fig. 4.1) for p-type C-TFET and GP-TFET for $\mathrm{L_G} = 50$ nm.

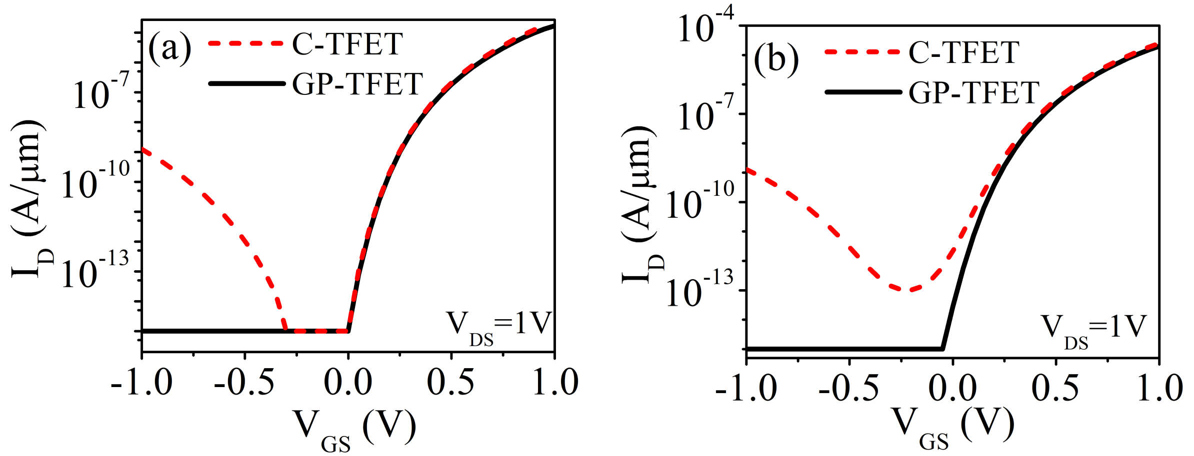


Figure 4.14: Transfer characteristics for n-type C-TFET and GP-TFET at (a) $\mathrm{L_G} = 50$ nm (b) $\mathrm{L_G} = 20$ nm.

simulations, it is found that in the ambipolar state, the electron concentration in the drain region for GP-TFET is much lower compared to C-TFET, as depicted in Fig. 4.12. The corresponding band diagrams in the ambipolar state are compared in Fig. 4.13 illustrating the increased tunneling barrier width in the GP-TFET. Consequently, there is a dramatic decrease in the $\mathrm{I_{AMB}} = 1.3 \times 10^{-9}$ A/μm in C-TFET to $\mathrm{I_{AMB}} = 1 \times 10^{-15}$ A/μm in the GP-TFET for $\mathrm{L_G} = 50$ nm, as

shown in Fig. 4.14(a). The I_{AMB} decreases from 1.8×10^{-9} A/μm in C-TFET to 1×10^{-15} A/μm in GP-TFET for $L_G = 20$ nm, as shown in Fig. 4.14(b). This illustrates that the GP-TFET is able to suppress the I_{AMB} even for small channel length devices.

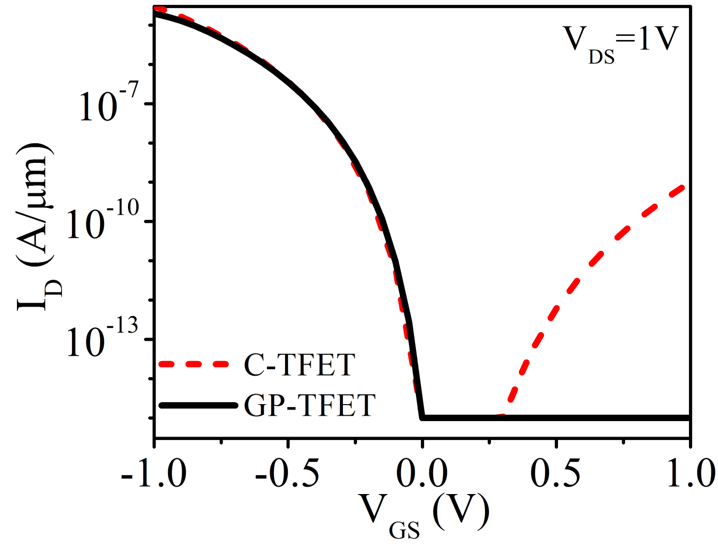


Figure 4.15: Transfer characteristics for p-type C-TFET and GP-TFET for $L_G = 50$ nm.

In previous sections, n-TFETs are analyzed primarily. However, considering CMOS applications, it is important to examine the impact of addition of GP in mitigating the I_{AMB} in p-type TFETs. The simulations show that addition of GP can suppress I_{AMB} in p-type TFET also. Fig. 4.15 compares the transfer characteristics of the p-type C-TFET with p-type GP-TFET for $L_G = 50$ nm. It shows that addition of GP results in a decrease in I_{AMB} from 1×10^{-9} A/μm to 1×10^{-15} A/μm. For a p-type TFET, the following parameters are used: N_S (n-type) $= 1 \times 10^{20}$ atoms/cm^3, N_D (p-type) $= 5 \times 10^{18}$ atoms/cm^3 and $\phi_m = 5.3$ eV. The other device parameters of p-type TFET are same as in Table 4.1. The optimum parameter values for GP in p-type TFET are found to be:

$d_{gp} = 6$ nm and N_{gp} (n-type) $= 1 \times 10^{20}$ atoms/cm^3.

4.3.1 Optimizing d_{gp} in a GP-TFET to fully suppress I_{AMB} without degrading the I_{ON} and SS_{avg}

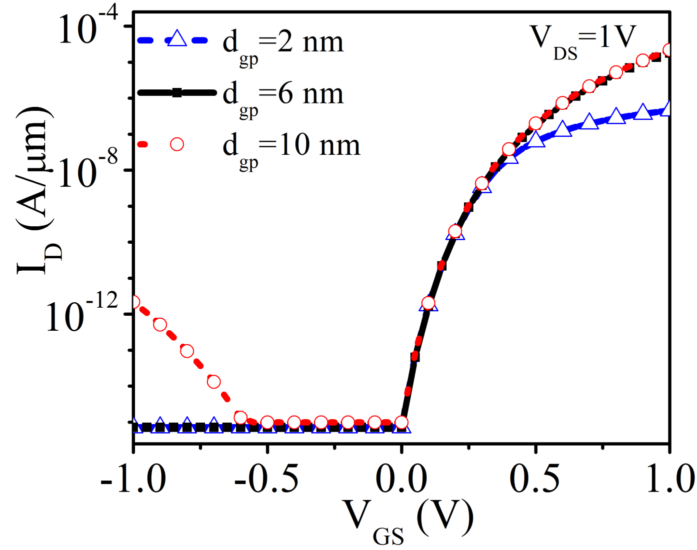


Figure 4.16: Transfer characteristics of GP-TFET at different d_{gp}.

The depth of the GP (d_{gp}) is the important parameter in the GP-TFET structure. Using simulations, it is found that $d_{gp} > 6$ nm is not able to fully suppress the I_{AMB}, as shown in Fig. 4.16. As d_{gp} increases beyond 6 nm, the ground plane becomes less effective in depleting the drain in the ambipolar state. Therefore, a $d_{gp} \leq 6$ nm is desirable for fully suppressing the I_{AMB} till $V_{OFF,2} = -V_{DD}$. However, d_{gp} cannot be decreased arbitrarily to very small values, since for extremely small d_{gp} (for instance, 2 nm), the I_{ON} decreases as shown in Fig. 4.16. The reduction in I_{ON} can be attributed to the reduced energy window available for BTBT at the source–channel interface. Hence, the optimum $d_{gp} \approx 6$ nm results in fully suppressed I_{AMB} and reduced I_{OFF}. However, the addition of

GP does not impact the I_{ON} for optimum d_{gp} (i.e., $d_{gp} = 6$ nm). Moreover, the addition of GP does not impact the subthreshold characteristics as evident from Fig. 4.16.

4.3.2 Mechanism of suppression of I_{AMB} in GP-TFET

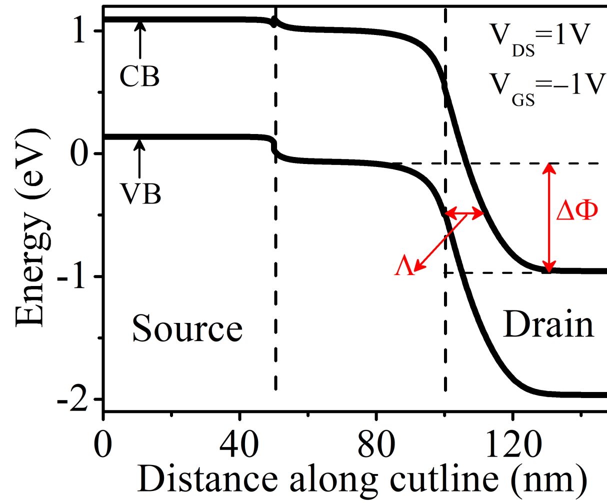


Figure 4.17: Illustration of Λ and $\Delta\Phi$ in a GP-TFET (energy band diagram along the cutline RR′).

In a GP-TFET, as mentioned above, when the d_{gp} is decreased, the drain becomes more depleted of the carriers, and the I_{AMB} is suppressed. In this section, the mechanism of suppression of the I_{AMB} is examined in more detail. The tunneling current in a TFET primarily depends on two parameters: [4]

1. Tunneling barrier width (Λ)

2. Energy band overlap ($\Delta\Phi$)

These parameters are illustrated in Fig. 4.17. When Λ is small or $\Delta\Phi$ is large, then more tunneling current flows in a TFET. The existence of the GP modulates

these parameters, and the combined effect of these modulations suppresses the I_{AMB}, as described in the following paragraphs [4, 144].

4.3.2.1 Impact of GP on Λ

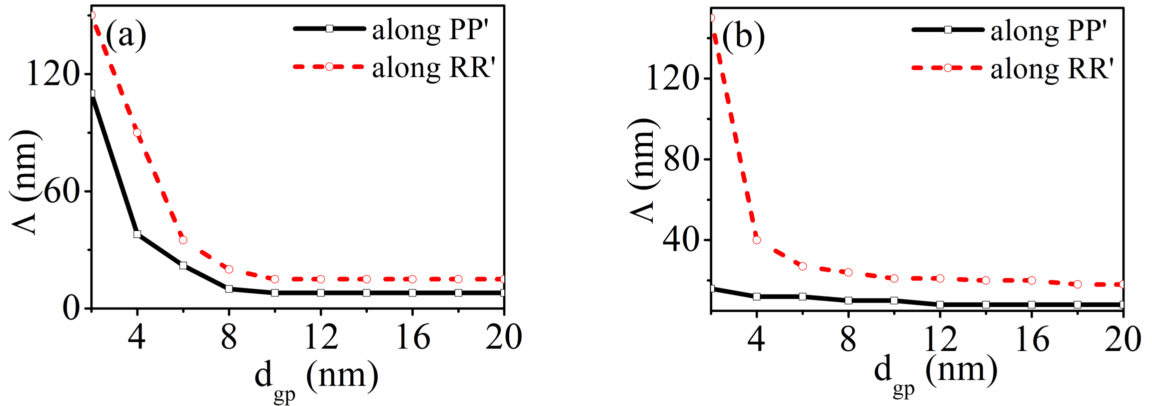


Figure 4.18: Λ vs d_{gp} at $V_{GS} = -V_{DD}$ and $V_{DS} = V_{DD}$ for (a) $t_{si} = 10$ nm (b) $t_{si} = 20$ nm.

In a TFET, unwanted tunneling occurs at the drain–channel interface in the ambipolar mode ($V_{GS} = -V_{DD}$ and $V_{DS} = V_{DD}$). For the full suppression of the I_{AMB}, the drain throughout its thickness (represented by t_{drain} in Fig. 4.1), should be depleted. In GP-TFETs with small silicon body thickness, such as $t_{si} = 10$ nm, the addition of the GP results in depletion of the drain throughout its thickness. Thus, an increase in the Λ at the top (along the cutline PP$'$), as well as at the bottom (along the cutline RR$'$) is observed, as shown in Fig. 4.18(a). This results in full suppression of I_{AMB} for $d_{gp} \leq 6$ nm (as shown in Fig. 4.16).

Further, it should be noted that the thickness of the silicon body also plays an important role in deciding whether the complete drain along its thickness is depleted. For instance, if the thickness of the silicon body (t_{si}) is 20 nm, then though Λ is increased at the bottom of the drain (along the cutline RR$'$), it is not

increased at the top of the drain (along the cutline PP′) even for $d_{gp} < 6$ nm, as illustrated in Fig. 4.18(b). As a result, the I_{AMB} in a GP-TFET with $t_{si} = 20$ nm is 8×10^{-10} A/μm even at $d_{gp} = 6$ nm, in contrast to 1×10^{-15} A/μm for $t_{si} = 10$ nm at $d_{gp} = 6$ nm.

4.3.2.2 Impact of GP on $\Delta\Phi$

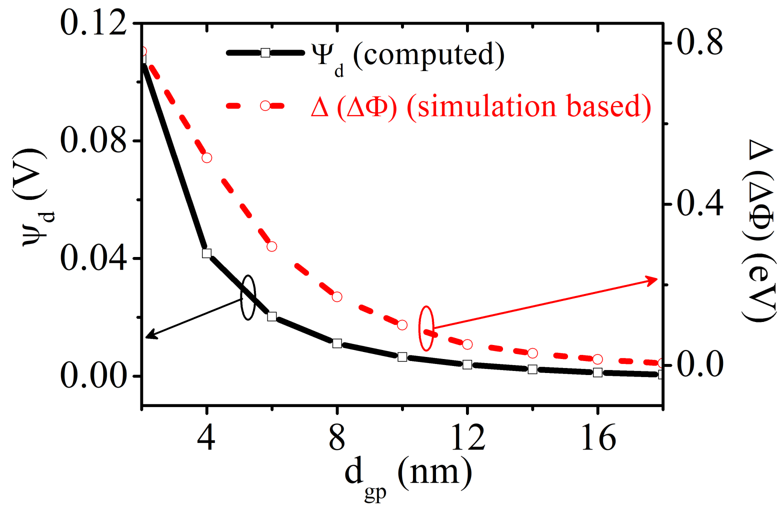


Figure 4.19: Trend of variation of ψ_d and $\Delta(\Delta\Phi)$ w.r.t d_{gp} at $V_{GS} = -V_{DD}$ and $V_{DS} = V_{DD}$.

The addition of GP decreases the energy band overlap ($\Delta\Phi$) at the drain–channel interface. As the GP is brought closer to the drain, the energy band overlap decreases further. In Fig. 4.19, the decrease in the energy band overlap ($\Delta(\Delta\Phi)$) extracted using device simulations is shown. The $\Delta(\Delta\Phi)$ is defined as Eq. 4.3:

$$\Delta(\Delta\Phi) = \Delta\Phi_{20} - \Delta\Phi \tag{4.3}$$

where, $\Delta\Phi_{20}$ is the energy band overlap at $d_{gp} = 20$ nm and $\Delta\Phi$ is the energy band overlap at a given d_{gp}. It can be noticed that with the decrease in the d_{gp}, the impact of the GP becomes prominent and $\Delta(\Delta\Phi)$ increases. The increase in

$\Delta(\Delta\Phi)$ can be attributed to the modulation in the potential in the drain due to the application of the GP. As the $\mathrm{d_{gp}}$ is decreased, the potential in the drain (ψ_d) is modulated and the bands in the drain move upwards, resulting in an increase in $\Delta(\Delta\Phi)$. The ψ_d in the drain, which is depleted of the carriers, can be computed as follows [145]:

$$\psi_d = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{DD} - V_{FB})}\right)^2 \tag{4.4}$$

where, $\gamma = \sqrt{2\mathrm{q}\epsilon_\mathrm{Si}\mathrm{N_D}}\,\frac{\mathrm{d_{gp}}}{\epsilon_\mathrm{ox}}$, ϵ_ox= permittivity of silicon dioxide, ϵ_Si= permittivity of silicon and $\mathrm{V_{FB}}$=flat band voltage.

In Fig. 4.19, the ψ_d (with respect to ψ_d at $\mathrm{d_{gp}} = 20$ nm) computed using Eq. 4.4, is also shown. The trend of ψ_d and $\Delta(\Delta\Phi)$ with respect to $\mathrm{d_{gp}}$ is showing a good match. Since Eq. 4.4 is a very simplistic model, the mismatch in ψ_d and $\Delta(\Delta\Phi)$ are expected. However, Fig. 4.19 illustrates that a decrease in the energy band overlap in GP-TFET can be attributed to the modulation of the potential in the drain ψ_d. Since the decrease in the energy band overlap suppresses tunneling, this analysis shows that the decrease in $\Delta(\Delta\Phi)$ due to the existence of the GP contributes to the suppression in the $\mathrm{I_{AMB}}$ in a GP-TFET.

4.4 Comparison with other ambipolar suppression techniques

The ambipolar performance of the GP-TFET is compared with respect to the other reported techniques in Table 4.2 [146]. The distinct advantage of the

Table 4.2: Comparison of ambipolar behaviour of GP-TFET with techniques existing in literature

Device Structure	L_G (nm)	N_D (atoms/cm^3)	V_{DD} (V)	I_{AMB} (A/μm)	$V_{OFF,2}$ (V)
Asymmetric TFET [7,46]	100	5×10^{18}	1	5×10^{-8}	-0.2
Gate–Drain Overlap [58]	100	1×10^{19}	1	10^{-9}	-0.5
HDB TFET [47]	100	5×10^{18}	1	10^{-13}	-0.8
Non-uniform drain-doped TFET [118]	100	1.5×10^{19} and 1×10^{20}	1	6×10^{-7}	-0.1
DP-DGTFET (Chapter-3)	100	1×10^{20}	1	10^{-14}	-1
This work	100	5×10^{18}	1	10^{-15}	-1

GP-TFET is that it can fully suppress the I_{AMB} at maximum negative gate bias, i.e., $V_{OFF,2} = -V_{DD}$. Moreover, the suppression of I_{AMB} can be achieved at smaller gate lengths, which can be attributed to the scalability of the GP-TFET, as demonstrated in the previous section.

4.5 Summary

The technique of the addition of ground plane in silicon–on–insulator TFETs is demonstrated as an effective means to extend the scalability of TFETs. Besides improving the scalability, the addition of the ground plane in the buried-oxide at an appropriate depth ameliorates the short-channel effects and mitigates the ambipolar conduction in the device. The proposed technique highlights the importance of depleting the drain of the majority carriers in suppressing the direct source–to–drain tunneling in short-channel TFETs.

Chapter 5

Exploiting within-channel tunneling in a TFET

In TFETs, the current is controlled by the band-to-band tunneling mechanism. Traditionally, the TFETs are designed such that the BTBT at the source–channel junction is enabled by the application of the positive V_{GS} [4,19,22]. To maximize the BTBT at the source–channel junction and boost the I_{ON}, in general, a high source doping concentration is used [4, 19, 106]. Furthermore, an abrupt source doping profile aids in boosting the BTBT at the source–channel junction [8, 9, 19, 107]. However, obtaining an abrupt doping profile is challenging in fabrication [57, 110].

In this chapter, a dual-material DGTFET with dominant within-channel BTBT is proposed. The gate material work-function is chosen such that the tunneling occurs within the channel at the dual-material gate (DMG) interface, rather than at the source–channel junction. In literature, DMGs are shown to improve the electrical characteristics in a TFET by enhancing BTBT on the source side and

suppressing BTBT on the drain side [4, 46, 48, 115]. In this work, DMG is used to obtain a sharp transition in the energy bands at the junction of high–low work-function materials and enable within-channel BTBT. Due to an inherent lateral electric field, a strong gate control over the BTBT region, several electrical parameters improve in the proposed TFET.

Further, TFETs exhibit exponential onset in the output characteristics because of the dependence of the BTBT on the V_{GS} and the V_{DS}, in contrast to the conventional MOSFET [147, 148]. There exists two types of threshold voltages: gate threshold voltage (V_{th}) and drain threshold voltage ($V_{th,d}$). For digital circuit applications, for achieving improved performance, a TFET should have a low $V_{th,d}$ [147–149]. The proposed structure exhibits a lower $V_{th,d}$ compared to the conventional DGTFET. Furthermore, it is demonstrated that in contrast to the conventional TFETs, the proposed device is less susceptible to variations in source doping and shift in the gate-edge with respect to the source–channel junction.

5.1 Device Structure and Simulation Setup

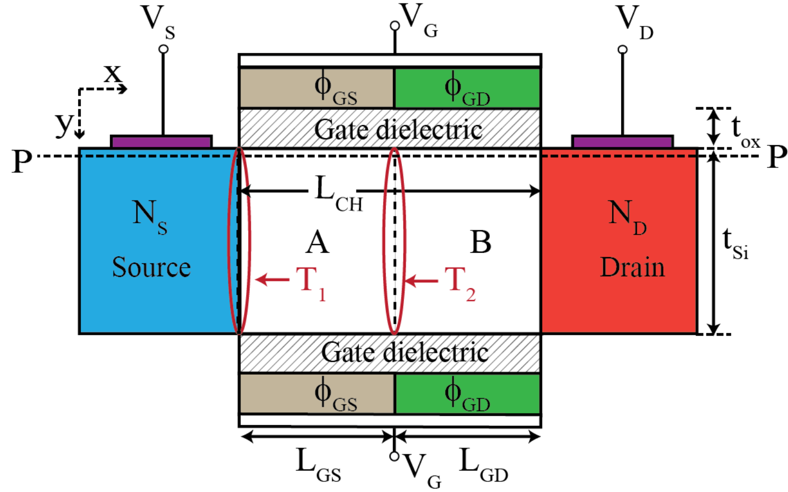


Figure 5.1: Schematic cross-section of the proposed TFET.

Table 5.1: Parameters of the proposed TFET

Parameter	**Value**
Supply voltage (V_{DD})	0.5 V
Silicon film thickness (t_{si})	10 nm
Effective oxide thickness (EOT)	0.5 nm (HfO_2)
s-gate work-function (ϕ_{GS})	5.93 eV
d-gate work-function (ϕ_{GD})	4.2 eV
Source doping (N_S) (p-type)	1×10^{19} atoms/cm^3
Drain doping (N_D) (n-type)	1×10^{19} atoms/cm^3
Channel doping (N_C) (p-type)	1×10^{17} atoms/cm^3
Channel length (L_{CH})	20 – 100 nm
s-gate length (L_{GS})	10 – 50 nm
d-gate length (L_{GD})	10 – 50 nm

Fig. 5.1 shows the schematic cross-sectional view of the proposed device. The top and the bottom gates are composed of materials with different work-functions, similar to DMG-DGTFET in [46]. The gate closer to the source is having a work-function ϕ_{GS} and is termed as s–gate, and the gate closer to the drain is having a work-function ϕ_{GD} and is termed as d–gate. The channel region under the s–gate is denoted as “A” and under the d–gate as “B”. In this work, the

device parameters are chosen such that a sharp transition in the energy bands is obtained at the junction of high–low work-function materials $\mathrm{T_2}$ rather than at the source–channel junction $\mathrm{T_1}$. Consequently, within-channel BTBT at the junction $\mathrm{T_2}$ constitutes the dominant component of the $\mathrm{I_{ON}}$. Furthermore, suppression of source–channel junction BTBT exhibits certain interesting characteristics which are investigated in detail. The simulation parameters used in this work are shown in Table. 5.1. The device in this work is different from the DMG-TFET proposed in [46] in the operation mechanism as follows:

1. The tunneling occurs at the source-channel interface in the DMG-DGTFET proposed in [46]. However, tunneling occurs within the channel at the $\phi_{\mathrm{GS}} - \phi_{\mathrm{GD}}$ interface in the device proposed in this work.

2. A high lateral electric field and an abrupt tunneling junction exist at the DMG interface in the device proposed in this work compared to the DMG-DGTFET proposed in [46].

3. Since tunneling occurs at the interface of the two work functions in the proposed device, the interface needs to be sharp in the proposed device. If the DMG interface is not sharp, then the abruptness of switching reduces to some extent, as explained later in the chapter. This requirement is not so stringent in the DMG-DGTFET proposed in [46].

In literature, DMG devices have been widely studied and fabricated [4, 46, 115, 150, 151]. To realize a DMG architecture, techniques such as tilt angle evaporation and lithography, metal inter-diffusion technique, and metal wet

etching techniques can be used [115, 152, 153]. In the tilt angle evaporation method, one of the gate materials is evaporated with a carefully controlled tilt angle, and then the other material is deposited using conventional evaporation [150]. In the metal inter-diffusion technique to fabricate the DMG architecture, the two materials with different work-functions are deposited one after the other. Subsequently, one of the metals is selectively removed from unwanted regions [154]. Additionally, metal wet etching and other advanced fabrication processes can be used for fabricating DMG, as demonstrated in [126, 155, 156].

5.2 Device Operation and Characteristics

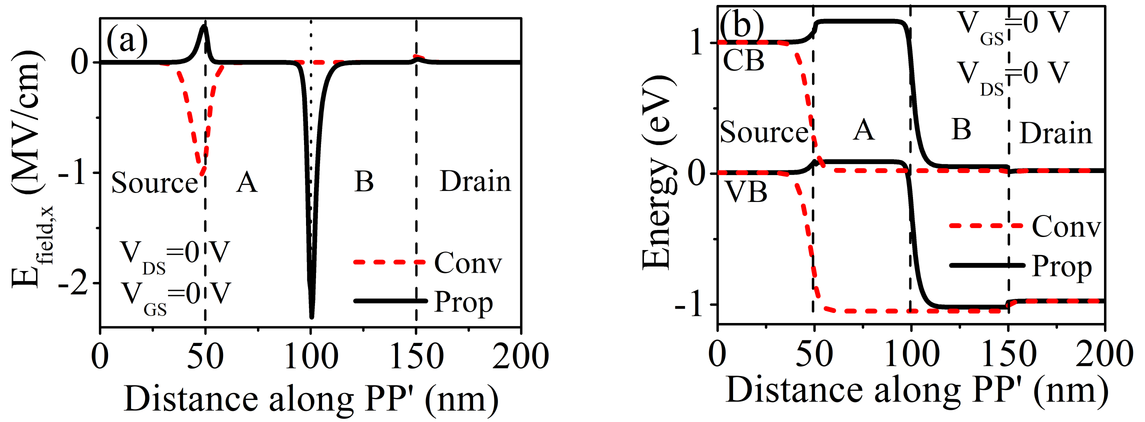


Figure 5.2: Devices under equilibrium (a) Lateral electric field (b) Energy band diagram along the cutline PP′.

In the proposed device, within-channel tunneling (at the junction T_2) is enabled by DMG. Fig. 5.2(a) shows the magnitude of the lateral electric field ($E_{field,x}$) at equilibrium ($V_{GS} = 0$, $V_{DS} = 0$). In the proposed device ($\phi_{GS} = 5.93$ eV, $\phi_{GD} = 4.2$ eV), there is a high electric field at the junction T_2. A high inherent $E_{field,x}$ leads to improved electrical characteristics, as explained in the

following paragraphs [4, 67, 157]. In contrast, in the conventional device ($\phi_{\rm GS} = \phi_{\rm GD} = 4.2$ eV), the peak $\rm E_{field,x}$ occurs at the junction $\rm T_1$. Moreover, the step in the potential profile in the proposed device is manifested in the energy band diagram, as shown in Fig. 5.2(b). It leads to a small tunneling barrier width and appropriate energy band alignment at the junction $\rm T_2$. In the equilibrium, despite small tunneling barrier width, negligible energy band overlap exists, which inhibits BTBT and the device remains in the OFF-state. However, when a small $\rm V_{GS}$ is applied, energy band overlap occurs and due to a small tunneling barrier width, the proposed device switches ON abruptly. Therefore, an excellent $\rm SS_{avg}$ is expected in a TFET that exploits within-channel tunneling.

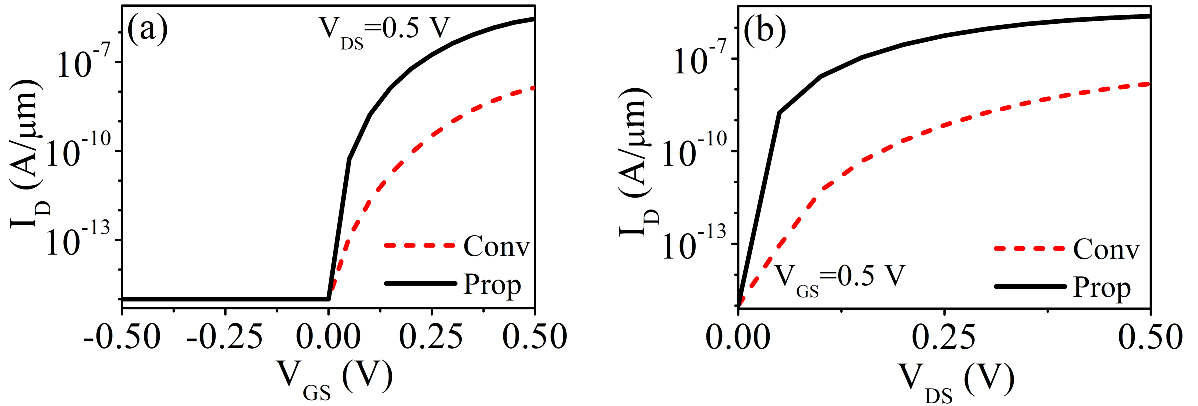


Figure 5.3: Comparison of the conventional and proposed devices (a) Transfer characteristics (b) Output characteristics.

Fig. 5.3(a) compares the transfer characteristics of the conventional and the proposed device. In this chapter, $\rm V_{th}$ is taken as the $\rm V_{GS}$ when the drain current ($\rm I_D$) reaches 1×10^{-8} A/μm. It can be seen from Fig. 5.3(a), that in the conventional device, $\rm I_{ON} = 1.4 \times 10^{-8}$ A/μm. Therefore, in this chapter, $\rm V_{th}$ is evaluated at $\rm I_D = 1 \times 10^{-8}$ A/μm instead of $\rm I_D = 1 \times 10^{-7}$ A/μm used in previous chapters. The $\rm V_{th}$ is found to be 145 mV and 457 mV for the proposed

device and the conventional device, respectively. Furthermore, the $\mathrm{SS_{avg}}$ in the proposed device is $21\ \mathrm{mV/dec}$, in contrast to $65\ \mathrm{mV/dec}$ in the conventional device. A low $\mathrm{V_{th}}$ and an excellent $\mathrm{SS_{avg}}$ in the proposed device is due to the inherent lateral electric field supporting BTBT. The $\mathrm{I_{ON}}$ in the proposed device is $2.6 \times 10^{-6}\ \mathrm{A}/\mu\mathrm{m}$. The work function of the gates in both the devices has been adjusted such that the $\mathrm{I_D}$ starts to take-off at $\mathrm{V_{GS}} = 0\ \mathrm{V}$. When $\mathrm{V_{GS}} < 0\ \mathrm{V}$, there is no conduction–valence band overlap, and the band-to-band tunneling is inhibited to a large extent in the device. However, a small current exists due to direct source–to–drain BTBT and thermal effects [4, 158, 159].

Next, the output characteristics of the conventional and the proposed devices are compared in Fig. 5.3(b). The distinct features of the output characteristics in a TFET, such as exponential onset and existence of drain threshold voltage ($\mathrm{V_{th,d}}$), are evident [4, 148]. In general, a low $\mathrm{V_{th,d}}$ is desirable in a TFET to reduce the transition time in CMOS-type TFET-based digital circuits [149,160]. $\mathrm{V_{th,d}}$ can be defined as the $\mathrm{V_{DS}}$ required to make $\mathrm{I_D}$ reach 10% of the saturation current level. The extracted $\mathrm{V_{th,d}}$ is found to be $0.16\ \mathrm{V}$ for the proposed device and $0.24\ \mathrm{V}$ for the conventional device. The presence of an inherent lateral electric field in the proposed device enables it to be turned-ON at lower $\mathrm{V_{DS}}$, achieving low $\mathrm{V_{th,d}}$ and suppressing super-linear onset [4, 157, 160]. It is worth mentioning that the characteristics of both the conventional device and the proposed device depend on the source doping concentration. In Fig. 5.3(a), the device characteristics for $\mathrm{N_S} = 1 \times 10^{19}\ \mathrm{atoms/cm^3}$ are shown. The characteristics of these devices at other source doping concentrations and profiles are shown in the subsequent

sections.

5.3 DIBL performance of the device

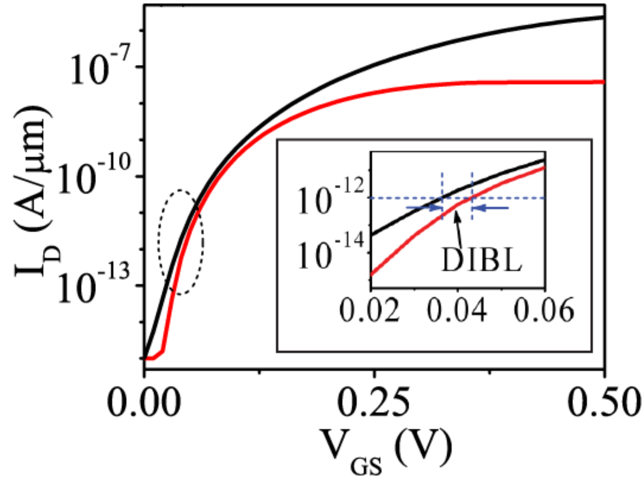


Figure 5.4: Illustration of DIBL in the proposed device (red line denotes $\mathrm{V_{DS}} = 0.1$ V and black line denotes $\mathrm{V_{DS}} = 0.5$ V).

In general, TFETs suffer from DIBL due to a stronger impact of the $\mathrm{V_{DS}}$ on BTBT [4]. To quantify the DIBL effect (Eq. 5.1), the shift in the transfer characteristics due to drain–source voltage at a fixed drain current $\mathrm{I_{DIBL}} = 10^{-12}\ \mathrm{A}/\mu\mathrm{m}$ is measured, as shown in Fig. 5.4 [46]:

$$DIBL = \frac{V_{GS,2} - V_{GS,1}}{V_{DS,2} - V_{DS,1}} \tag{5.1}$$

where, $\mathrm{V_{GS,2}}$ is the gate–source voltage at which $\mathrm{I_D} = \mathrm{I_{DIBL}}$ and $\mathrm{V_{DS}} = \mathrm{V_{DS,2}} = \mathrm{V_{DD}}$. Similarly, $\mathrm{V_{GS,1}}$ is the gate–source voltage at which $\mathrm{I_D} = \mathrm{I_{DIBL}}$ and $\mathrm{V_{DS}} = \mathrm{V_{DS,1}} = 0.1$ V. The extracted value of DIBL is $20\ \mathrm{mV/V}$ for the proposed TFET and $280\ \mathrm{mV/V}$ for the conventional TFET. A high inherent lateral electric field at the BTBT junction in the proposed device suppresses the further impact of

drain-induced electric field leading to a smaller DIBL effect.

5.4 Scaling gate length

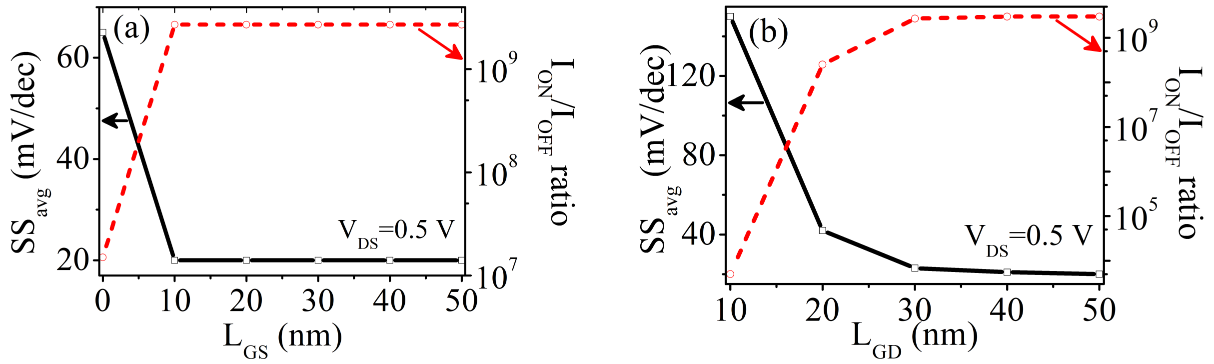


Figure 5.5: SS_{avg} and I_{ON}/I_{OFF} ratio for the proposed TFET with (a) with varying L_{GS} ($L_{GD} = 50$ nm) (b) varying L_{GD} ($L_{GS} = 50$ nm).

Considering the futuristic applications, it is important to analyze the scaling trend of the proposed device. In this section, the minimum values of L_{GS} and L_{GD} are found such that the device characteristics are not affected significantly. Fig. 5.5(a) and 5.5(b) show the trend of I_{ON}/I_{OFF} ratio and SS_{avg} of the proposed device with respect to changes in the L_{GS} and L_{GD}, respectively. Fig. 5.5(a) shows that as the L_{GS} is decreased up to 10 nm, there is no effect on the I_{ON}/I_{OFF} ratio and SS_{avg}. However, as L_{GS} is decreased below 10 nm, the I_{ON}/I_{OFF} ratio decreases by 2 orders and SS_{avg} increases by around 200%. At $L_{GS} = 10$ nm the characteristics of the proposed device is similar to the conventional device. This is expected, since with a large reduction in L_{GS}, the distinction between within-channel tunneling and source–channel junction tunneling disappears. Therefore, the $L_{GS,min} = 10$ nm is chosen. Similarly, when L_{GD} decreases from 30 nm to 10 nm (keeping $L_{GS} = 10$ nm), the I_{ON}/I_{OFF} ratio decreases by 6 orders of

magnitude and the SS_{avg} increases by $5\times$, as shown in Fig. 5.5(b). However, above $L_{GD} = 30$ nm, there is no significant change in the I_{ON}/I_{OFF} ratio and SS_{avg} of the device. Therefore, $L_{GD,min}$ is chosen to be 30 nm. Therefore, $L_{G,min} = L_{GS,min} + L_{GD,minopt} = 40$ nm is needed for obtaining within-channel tunneling in the proposed device.

5.5 C_{GD} and C_{GS} in the proposed structure

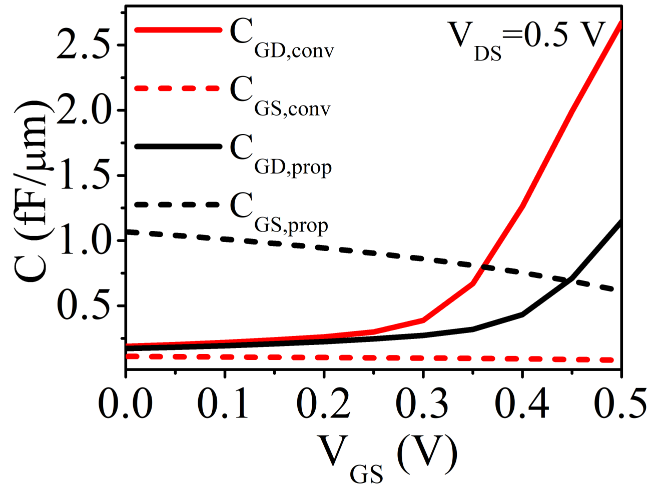


Figure 5.6: Capacitance of the conventional and the proposed TFET.

It is important to analyze the capacitance between the gate and drain (C_{GD}) and capacitance between gate and source (C_{GS}) of the proposed device. It is worth noting that in a conventional TFET, C_{GS} is much lower and C_{GD} dominates for all V_{GS} [4, 58, 122, 136]. However, in the proposed TFET, it is observed that as L_{GS} increases, C_{GS} increases, while the C_{GD} remains almost constant. Similarly, as the L_{GD} increases, C_{GD} increases, while the C_{GS} remains almost constant. The absence of reverse-biased junction at the source–channel interface and the decrease of effective distance between the drain and the BTBT region

can explain the observed behavior. Fig. 5.6 compares the capacitance of the conventional and proposed device with $L_{G,min} = 40$ nm (where $L_{GD,min} = 30$ nm and $L_{GS,min} = 10$ nm). It indicates that the C_{GD} decreases from 2.7 fF/μm in the conventional device to 1.2 fF/μm in the proposed device. This is good for CMOS-type digital applications because due to the Miller effect, the contribution of C_{GD} in determining the delay of the circuit is much higher [58, 122]. Therefore, a lower C_{GD} in the proposed device is expected to be beneficial for future CMOS-based applications. However, it is worthy to note that in the proposed device, the C_{GS} increases from 0.1 fF/μm (in the conventional device) to 0.6 fF/μm. Therefore, in contrast to conventional TFET where C_{GD} dominates over C_{GS} for all values of V_{GS}, in the proposed device, C_{GS} dominates for lower V_{GS} values. Further, for higher V_{GS}, C_{GD} as well as C_{GS} need to be considered.

5.6 Finding optimum values of ϕ_{GS} and ϕ_{GD}

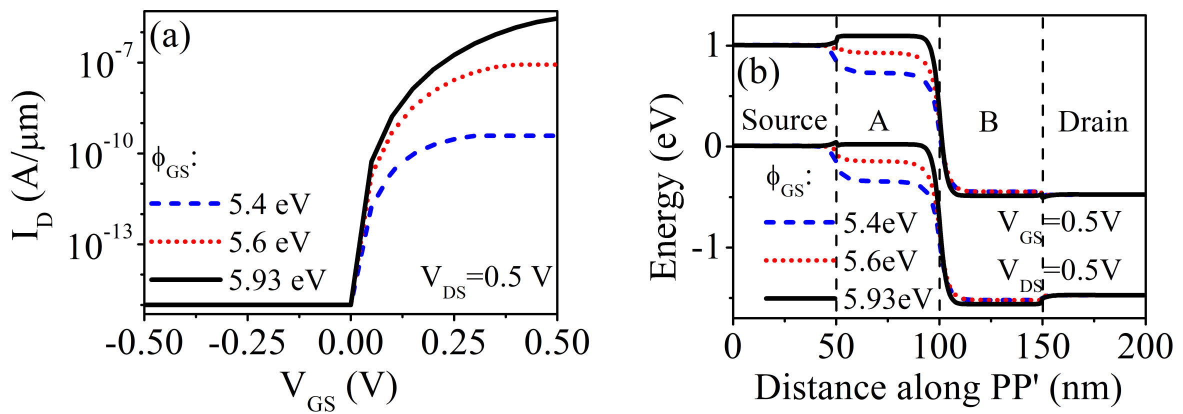


Figure 5.7: (a) Transfer characteristics (b) Energy band diagram of the proposed device keeping $\phi_{GD} = 4.2$ eV and varying the ϕ_{GS}.

A DMG structure with the work-functions ϕ_{GS} and ϕ_{GD} is used in the proposed device. In this section, the optimization of the work-function for the

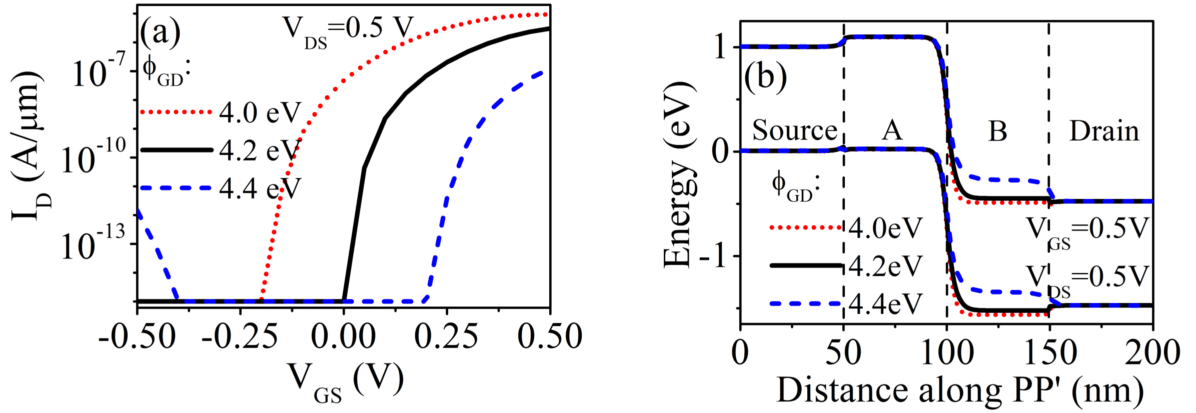


Figure 5.8: (a) Transfer characteristics (b) Energy band diagram of the proposed device keeping $\phi_{\mathrm{GS}} = 5.93$ eV and varying the ϕ_{GD}.

proposed device is explained. Fig. 5.7(a) shows that as ϕ_{GS} increases, the $\mathrm{I_{ON}}$ increases. Therefore, a high ϕ_{GS} is desirable. However, the increase in ϕ_{GS} above 5.93 eV does not lead to any appreciable improvement in the $\mathrm{I_{ON}}$. Therefore, an optimum ϕ_{GS} is chosen to be 5.93 eV. The corresponding energy band diagram of the device along cutline PP′ is shown in Fig. 5.7(b). It shows that as the ϕ_{GS} increases, the tunneling barrier width decreases, and the energy band overlap increases, resulting in an increase in the BTBT. The gate with $\phi_{\mathrm{GS}} = 5.93$ eV can be realized using platinum [115]. Furthermore, when ϕ_{GD} is increased, the transfer characteristics shift towards the right, as shown in Fig. 5.8(a). Therefore, $\phi_{\mathrm{GD}} = 4.2$ eV is chosen such that the take-off point of the transfer characteristics remains at $\mathrm{V_{GS}} = 0$ V and a minimum $\mathrm{I_{OFF}}$ is obtained. The gate with $\phi_{\mathrm{GD}} = 4.2$ eV can be realized using tantalum [161, 162]. The corresponding band diagram is shown in Fig. 5.8(b).

5.7 Effect of source doping concentration

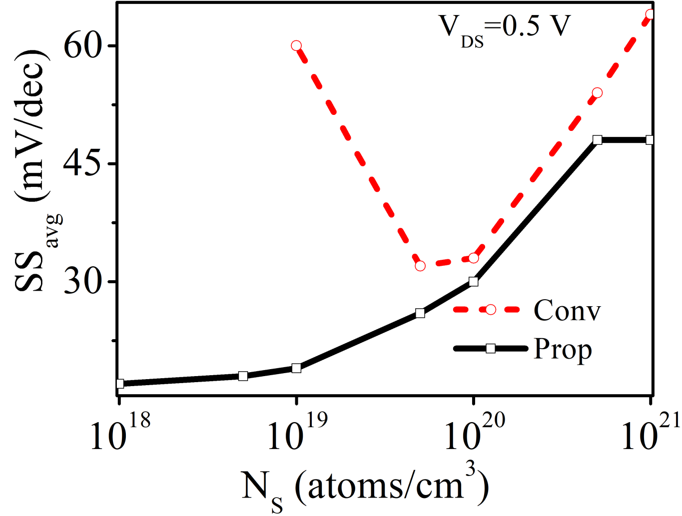
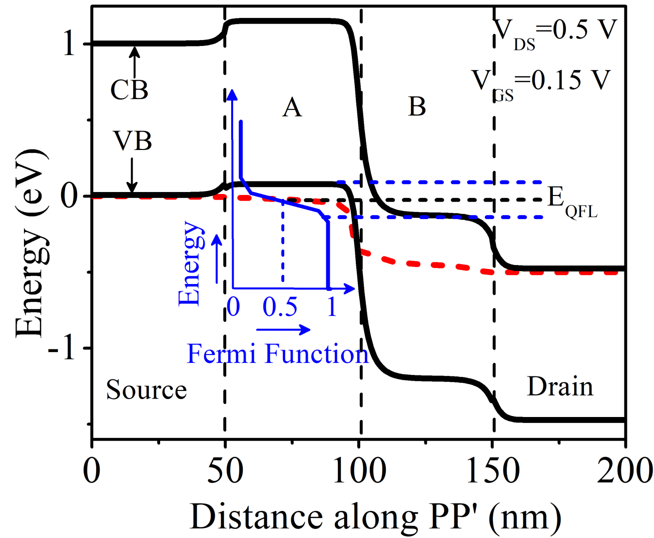


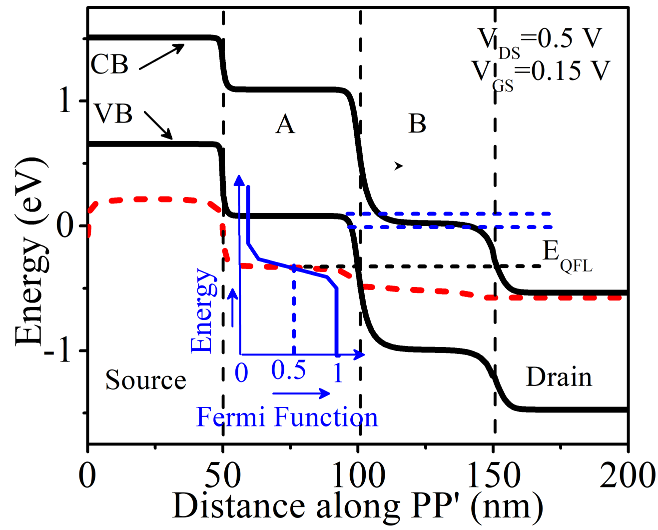
Figure 5.9: SS_{avg} for the conventional and proposed TFET with varying N_S at $V_{DS} = 0.5$ V.

Next, the performance of the proposed device as a function of the source doping concentration is analyzed. In a conventional TFET, an optimum source doping is shown to achieve a minimum SS_{avg} [19, 106, 163]. Fig. 5.9 compares the change in the SS_{avg} with the source doping (N_S) for a conventional and the proposed device. It is found that in the conventional device, the lowest SS_{avg} can be obtained in the range $N_S = 5 \times 10^{19} - 1 \times 10^{20}$ atoms/cm^3. However, in the proposed device, a much lower SS_{avg} can be achieved for a lower range $N_s = 1 \times 10^{18} - 1 \times 10^{19}$ atoms/cm^3. Above this range, the SS_{avg} increases and becomes similar to the SS_{avg} exhibited by the conventional TFET at $N_S = 1 \times 10^{20}$ atoms/cm^3.

The above trend for the SS_{avg} can be explained based on the band diagrams when the I_D starts to take-off and the position of quasi-Fermi level (QFL). To obtain a sharp OFF–ON transition or lower SS_{avg}, it is required that the



(a)



(b)

Figure 5.10: Energy band diagram along the cutline PP′ at $V_{GS} = 0.15$ V and $V_{DS} = V_{DD}$ (a) For proposed TFET when $N_S = 1 \times 10^{19}$ atoms/cm^3 (b) For proposed TFET when $N_S = 1 \times 10^{21}$ atoms/cm^3.

electrons occupying energy levels close to the Fermi level contribute to the BTBT in a TFET [4, 8, 19]. If electrons occupying the tails of the Fermi distribution function contribute to a large extent in BTBT, then an abrupt OFF–ON transition cannot be obtained in a TFET. Fig. 5.10(a) shows the alignment of the conduction band (CB), valence band (VB) and the electron QFL

for $N_S = 1 \times 10^{19}$ atoms/cm^3 for the proposed device at $V_{GS} = 0.15$ V and $V_{DS} = 0.5$ V. It can be noted that the electrons with energy close to the QFL in region A contribute to the tunneling current. Therefore, a sharp transition or lower SS_{avg} is obtained in the proposed device for $N_S = 1 \times 10^{19}$ atoms/cm^3. In contrast, when $N_S = 1 \times 10^{21}$ atoms/cm^3 in the proposed device, it can be noted from Fig. 5.10(b) that the electrons having energy much greater than the QFL in region A contribute to the BTBT. Therefore, a gentler transition or higher SS_{avg} is observed in this case.

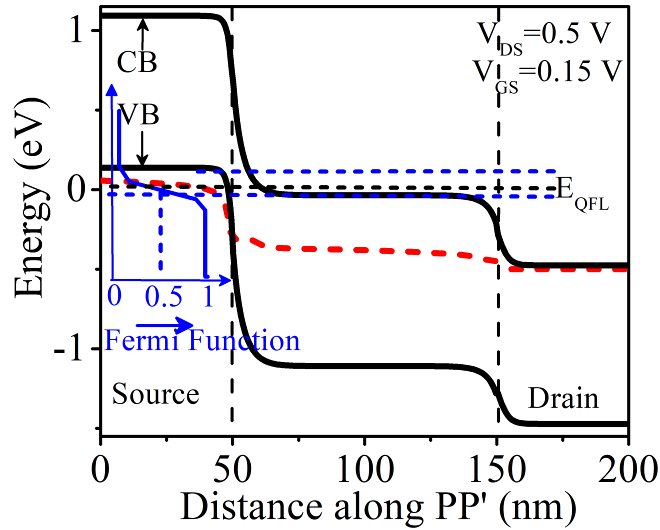


Figure 5.11: Energy band diagram along the cutline PP′ at $V_{GS} = 0.15$ V and $V_{DS} = V_{DD}$ for conventional TFET when $N_S = 1 \times 10^{20}$ atoms/cm^3.

Next, the band alignment for the conventional TFET and the position of the QFL at $N_S = 1 \times 10^{20}$ atoms/cm^3 are shown, in Fig. 5.11. It can be noted that the electrons with energy close to the QFL in the source contribute to the BTBT. Therefore, a low SS_{avg} is obtained at $N_S = 1 \times 10^{20}$ atoms/cm^3 in a conventional TFET. However, it is observed that when $N_S = 1 \times 10^{19}$ atoms/cm^3 or

$N_S = 1 \times 10^{21}$ atoms/cm^3, the electrons with energy away from the QFL contribute to the BTBT. Therefore, in both these cases, a higher SS_{avg} is obtained, in the conventional device (refer Fig 5.9).

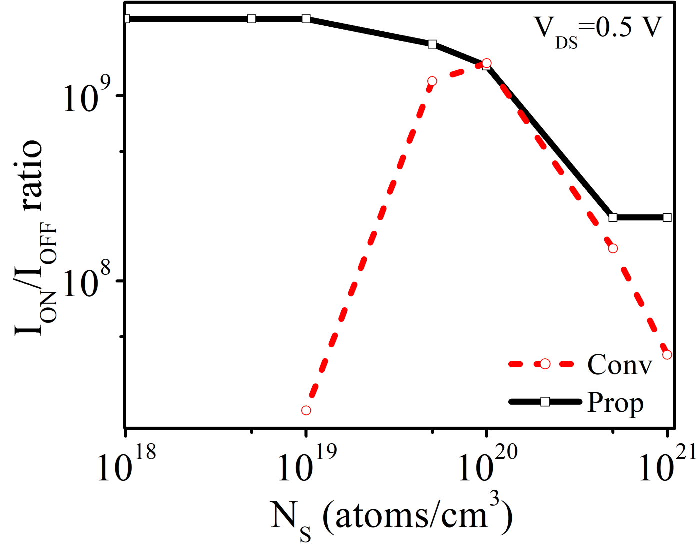


Figure 5.12: I_{ON}/I_{OFF} ratio for the conventional and proposed TFET with varying N_S at $V_{DS} = 0.5$ V.

Further, Fig. 5.12, compares the variation in the I_{ON}/I_{OFF} ratio with the source doping (N_S) for a conventional and the proposed device. It is found that in the proposed device, the highest I_{ON}/I_{OFF} ratio can be obtained in the range of $N_S = 1 \times 10^{18} - 1 \times 10^{19}$ atoms/cm^3. This is in contrast to the conventional device, where the highest I_{ON}/I_{OFF} ratio is obtained in the range $N_S = 5 \times 10^{19}$ -1×10^{20} atoms/cm^3. Furthermore, at $N_S = 1 \times 10^{20}$ atoms/cm^3, the I_{ON}/I_{OFF} ratios of both the devices are similar.

5.8 Effect of source doping profile

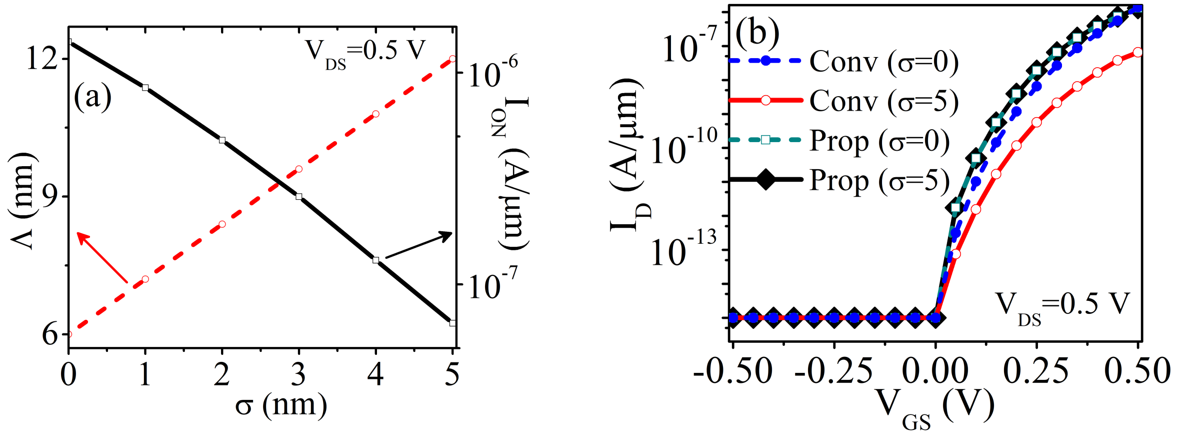


Figure 5.13: (a) Λ and I_{ON} for the conventional TFET with varying lateral straggle parameter, σ at $V_{DS} = 0.5$ V (b) Transfer characteristics of the conventional and the proposed TFET at $N_S = 1 \times 10^{20}$ atoms/cm^3 with $\sigma = 0$ nm (abrupt) and $\sigma = 5$ nm (non-abrupt) source doping profile.

The source doping profile is assumed to be abrupt in this work. However, obtaining an abrupt doping profile is challenging. Practically, during the ion-implantation process, some dopants extend laterally from the source towards the channel [36, 37]. Therefore, the electrical characteristics of the devices with the Gaussian source doping profile with lateral straggle (σ) varying between 0 nm (abrupt doping) to 5 nm keeping the peak doping concentration, $N_S = 1 \times 10^{20}$ atoms/cm^3 are examined. It is found that when the source doping profile becomes non-abrupt (σ increases), the tunneling barrier width (Λ) increases in the conventional device, as shown in Fig. 5.13(a). Consequently, the I_{ON} decreases in a conventional device as the doping profile becomes non-abrupt. In contrast, there is an insignificant effect of the abruptness of the source doping profile on the I_{ON} in the proposed device. This is intuitive since, in the proposed device, the tunneling occurs within the channel rather than the source-channel

interface. Fig. 5.13(b) shows the transfer characteristics of the conventional and the proposed device with lateral straggle parameter $\sigma = 0$ nm and $\sigma = 5$ nm. Thus, the proposed device can tolerate the variations in the source doping profile to a greater extent.

5.9 Effect of the shift in gate-edge with respect to the source–channel junction

Figure 5.14: Schematic cross-section of the proposed TFET demonstrating gate–underlap or gate–overlap, at the source–channel junction.

Figure 5.15: (a) I_{ON} (b) SS_{avg} for the conventional and proposed TFET with varying L_{ov} ($L_{un} = 0$) at $V_{DS} = 0.5$ V.

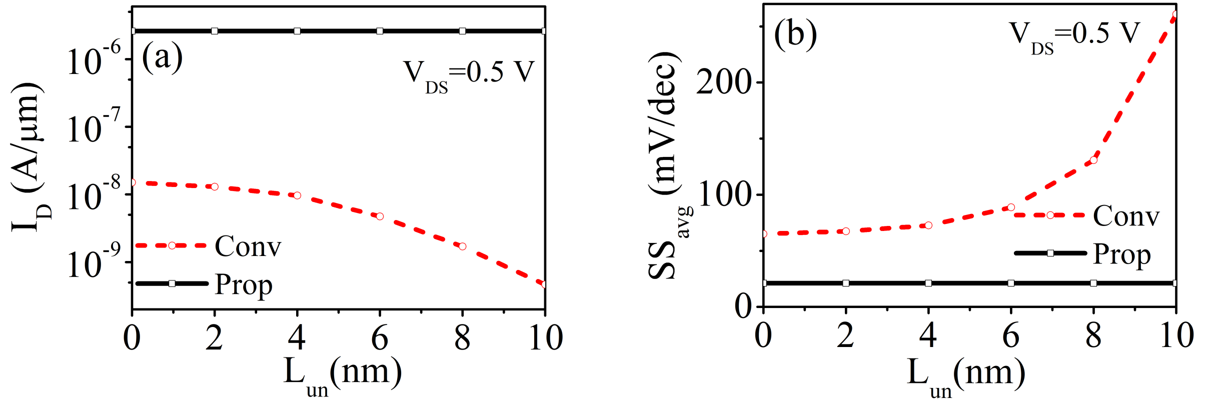


Figure 5.16: (a) I_{ON} (b) SS_{avg} for the conventional and proposed TFET with varying L_{un} ($L_{ov} = 0$) at $V_{DS} = 0.5$ V.

While fabricating a device, specifically during patterning steps, such as lithography, etching, deposition, etc., the edges can deviate from the reference straight line, thus resulting in a misalignment of gate-edge to the source–channel junction [111]. This creates an underlap or overlap in the device as shown in Fig. 5.14 [35]. In this work, the sensitivity of I_{ON} and SS_{avg} due to the gate–overlap or gate–underlap, at the source–channel junction is evaluated. It is found that, in the conventional TFET, for a 10 nm overlap ($L_{ov} = 10$ nm), the I_{ON} can decrease by 65.8% and the SS_{avg} can increase by $1.14\times$ with respect to the nominal value ($L_{ov} = 0$), as shown in Fig. 5.15(a) and 5.15(b), respectively. Similarly, for a 10 nm underlap ($L_{un} = 10$ nm), the I_{ON} can decrease by 97% and the SS_{avg} can increase by $4\times$ with respect to the nominal value ($L_{un} = 0$), as shown in Fig. 5.16(a) and 5.16(b), respectively. This degradation is expected since, in the conventional TFET, BTBT occurs at the source–channel edge and a shift of the gate-edge leads to a change in the tunneling barrier width and the resultant BTBT current. On the other hand, when a TFET utilizes within-channel tunneling, the underlap and overlap of gates do not impact the electrical characteristics of the

device, as shown in Fig. 5.15 and 5.16. This is expected because, in the proposed device, tunneling does not occur at the source–channel junction.

5.10 Effect of work-function variations

TFETs are shown to be susceptible to work-function variations (WFV) [35, 112]. In general, a gate electrode consists of multiple crystalline grains, each having a different orientation. These grain orientations can lead to different effective work-function of a gate metal [112, 113]. For instance, the work-function for Tantalum nitride can vary from 4.0 eV to 4.8 eV depending on the grain orientation [35]. In general, to assess the impact of WFV, random grain orientation and statistical analysis are required [35]. In this work, to assess the impact of the WFV on the electrical characteristics of a TFET in a simplistic manner, a work-function variation of $\pm 0.1\mathrm{eV}$ around the nominal value is taken [54]. In the conventional TFET, a change in gate work-function leads to a lateral shift in the transfer characteristics. As a result, with a uniform $\pm 0.1\mathrm{eV}$ change in the gate work-function, the $\mathrm{I_{ON}}$ changes by $3\times$ and the $\mathrm{SS_{avg}}$ is not affected. It is worthy to point out that, if high work-function grains are concentrated near the source, and the low work-function grains are concentrated next to them, the $\mathrm{SS_{avg}}$ can also exhibit degradation in a conventional TFET [112].

In the proposed device, since the BTBT occurs at the abrupt tunnel junction created at the interface of the work-function ϕ_{GS} and ϕ_{GD}, it is expected that the proposed device will be susceptible to the WFV. To quantify the variations,

both the work-functions ϕ_{GS} and ϕ_{GD} are varied by ± 0.1 eV. The worst-case degradation in the I_{ON} and the SS_{avg} is noticed when the ϕ_{GS} is decreased by 0.1 eV and the ϕ_{GD} is increased by 0.1 eV, simultaneously. In this case, the I_{ON} decreases by $6\times$ and the SS_{avg} degrades by 17 %. Therefore, in the proposed device, techniques such as amorphization should be employed to reduce the impact of WFV [112].

Figure 5.17: Schematic cross-section of the proposed TFET with averaged work-function ϕ_A at the DMG interface.

Figure 5.18: SS_{avg} for the proposed TFET with varying L_{INT} at $V_{DS} = 0.5$ V.

Furthermore, since tunneling occurs at the interface of the two work-functions, the interface needs to be sharp in the proposed device. Due to process-induced variations, it can be difficult to obtain a sharp 5.93–4.2 eV interface for DMG [46, 153]. Therefore, the proposed device is examined by keeping the work-function $\phi_{\mathrm{A}} = 5.0\ \mathrm{eV}$ (average of $5.93\ \mathrm{eV}$ and $4.2\ \mathrm{eV}$) at the A-B interface for a length ($\mathrm{L_{INT}}$) of 2 nm, 3 nm, 4 nm and 5 nm (beyond this length the work-function is taken as $5.93\ \mathrm{eV}$ and $4.2\ \mathrm{eV}$), as shown in Fig. 5.17. The simulations reveal that in the proposed device, the $\mathrm{SS_{avg}}$ degrades from $21\ \mathrm{mV/dec}$ to $40\ \mathrm{mV/dec}$, as $\mathrm{L_{INT}}$ varies from $0\ \mathrm{nm}$ to $5\ \mathrm{nm}$, as shown in Fig. 5.18. Thus, if the DMG interface is not sharp, then the abruptness of switching reduces to some extent. Therefore, the techniques for fabricating a good DMG interface are important.

5.11 Effect of Interface Trap Charges

This section analyzes the impact of the interface trap charges (ITCs) on the device performance. The ITCs can be process-induced, radiation-induced, or stress-induced. The ITCs can decrease device reliability and lifetime [74, 164]. Therefore, it is important to assess the impact of ITCs on device performance. The interface charges can be positive (donor) ITCs or negative (acceptor) ITCs. In this work, the density of these charges is considered as $\mathrm{N_f} = \pm 10^{12}\ \mathrm{cm^{-2}eV^{-1}}$. This value is chosen based on various experimental observations and simulation studies that have considered the trap density of $\pm 10^{11} - \pm 10^{13}\ \mathrm{cm^{-2}eV^{-1}}$ [165–167]. To include the ITCs in simulations, the INTERFACE statement in ATLAS is used, which considers the density of interface fixed charges at the silicon–oxide

interface [50].

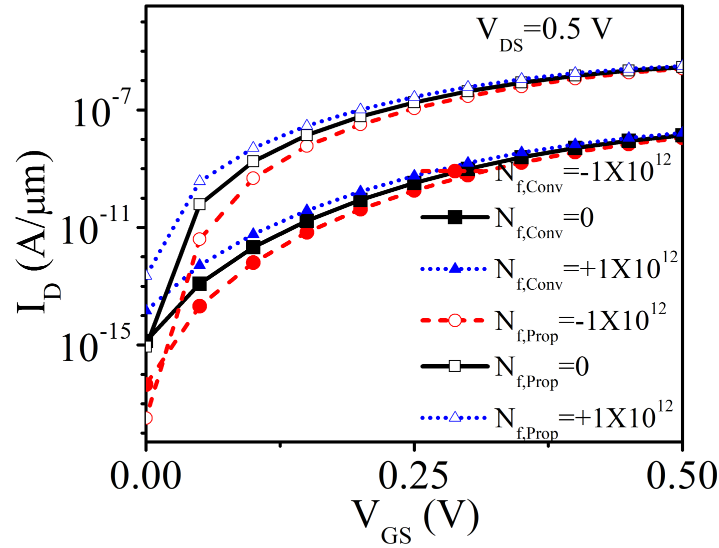


Figure 5.19: Transfer characteristics of the conventional and proposed TFET for acceptor, donor, and no ITCs.

Fig. 5.19 compares the transfer characteristics of the conventional and the proposed devices in the presence of the ITCs. It can be seen that presence of negative (acceptor) ITCs do not result in degradation in the device performance as far as electrostatic performance is concerned. However, the positive (donor) ITCs result in a higher I_{OFF} in both the devices, resulting in a lower I_{ON}/I_{OFF} ratio. The I_{ON}/I_{OFF} ratio degrades from 2×10^7 to 1×10^6 in the conventional device and from 2.6×10^9 to 1.4×10^7 in the proposed device. Further, the location of the traps is also critical in the device. The presence of the interface traps around the source is more harmful to the device performance in the conventional device. However, the presence of the traps around the DMG interface is more harmful to the proposed device. This is expected since the electric field and BTBT is maximum at the source–channel interface in the conventional device and at the

DMG interface in the proposed device.

Furthermore, it is important to mention that only electrostatic degradation due to ITCs is considered. The bulk trap states and trap-assisted tunneling (TAT) can also degrade device performance. Therefore, a more in-depth analysis involving bulk traps and TAT is required to assess the impact of traps on DMG-TFETs.

5.12 Summary

In this chapter, within-channel tunneling using DMG is exploited, and novel attributes of the proposed device have been reported. Though the technique of exploiting within-channel tunneling is demonstrated in a silicon-based TFET, in this work, with proper device optimization, the concept can be extended to TFETs based on other materials as well. Due to the inherent lateral electric field, a strong gate control over the BTBT region, and the shift of the BTBT region towards the drain, some of the electrical characteristics improve compared to a conventional TFET. It is demonstrated that within-channel tunneling can be exploited for channel lengths of $40\ \mathrm{nm}$ and above. Additionally, it is demonstrated that the proposed TFET is immune to variations in source doping concentration and gate-edge shift at the source–channel interface. However, the impact of work-function variations and interface trap charges in the proposed device is important and needs to be tackled. Further, within-channel tunneling device exhibits reasonably good $\mathrm{I_{ON}}$ and $\mathrm{SS_{avg}}$. Therefore, it can be exploited in energy-efficient digital circuits, as demonstrated in the next chapter.

Chapter 6

Implementation of Logic Functions

In the previous chapters, various novel TFET structures have been proposed and analyzed. These devices are shown to ameliorate several known problems of a conventional TFET. The aim of device modifications has been to make TFETs suitable for digital circuit applications by making them behave similar to or better than the conventional MOSFETs. This chapter investigates whether distinct characteristics of TFETs can be utilized in CMOS-type digital circuits.

In this chapter, a single tunneling device has been shown to realize two-input logic functions such as AND, OR, NAND, NOR, XNOR, and XOR. It is shown that when the architecture of a DGTFET is modified, it can implement the two-input logic function. The input to the logic function is provided by the top and the bottom gates of the DGTFET. Thus, the two gates of DGTFETs are biased independently in the rest of this chapter.

Table 6.1: Expected Output corresponding to the logic inputs A and B for the functions

Function (→) Input (↓)	**OR**	**NAND**	**AND**	**NOR**	**XNOR**	**XOR**
00	I_{OFF}	I_{ON}	I_{OFF}	I_{ON}	I_{ON}	I_{OFF}
01	I_{ON}	I_{ON}	I_{OFF}	I_{OFF}	I_{OFF}	I_{ON}
10	I_{ON}	I_{ON}	I_{OFF}	I_{OFF}	I_{OFF}	I_{ON}
11	I_{ON}	I_{OFF}	I_{ON}	I_{OFF}	I_{ON}	I_{OFF}

6.1 Terminologies

In this work, the voltages V_{DD} (= 1 V) and ground (= 0 V) are treated as logic '1' and logic '0', respectively. When the gates of the DGTFET are biased at logic A and B, respectively, the input to the function can be represented as "AB". Therefore, four possible input combinations are "00", "01", "10", and "11". The drain current flowing through the device corresponding to the input "AB" is denoted as I_{AB}. In these logic function realizations, the magnitude of drain current I_{AB} flowing through the device depends on the input to the function ("AB") and is modulated in accordance with the intended functionality. Table. 6.1 shows the input to the functions and the corresponding current flowing through the device, I_{AB}. When the expected output is logic '0' for the function, a low current flows through the DGTFET and is termed as I_{OFF}, and when the expected output is logic '1' for the function, a high current flows through the DGTFET and is termed as I_{ON}. For DGTFET-based logic function realizations, it is desirable to achieve a sufficient I_{ON}/I_{OFF} ratio to differentiate between the logic '0' and logic '1'.

6.2 Realizing OR functions using DGTFET

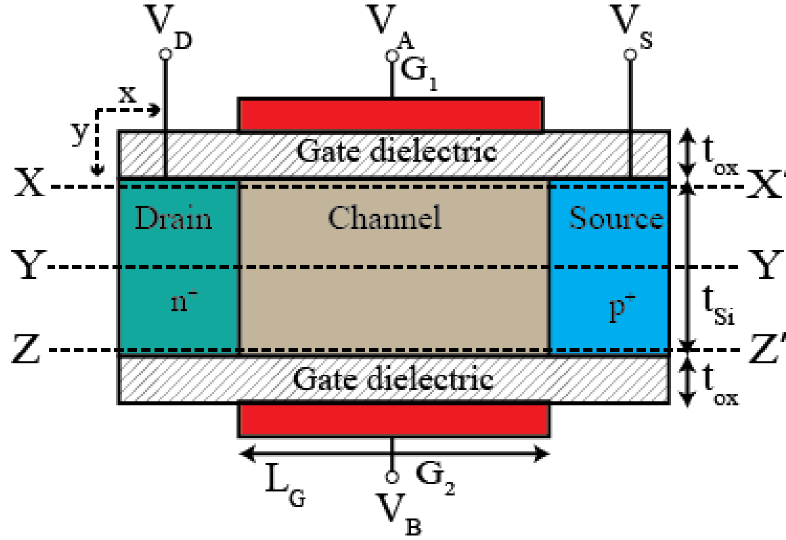


Figure 6.1: Cross-sectional view of an n-DGTFET realizing OR logic function.

Table 6.2: Device Parameters used in the simulation of DGTFET-based logic functions

Parameter	OR	NAND	AND	NOR	XNOR	XOR
Supply voltage (V_{DD}) (V)	1	1	1	1	1	1
Silicon film thickness (t_{si}) (nm)	10	10	10	10	10	10
Gate oxide thickness (t_{ox}) (nm)	2 (EOT≈ 0.5)	2	2	2	2	2
Channel doping (N_C) ($atoms/cm^3$)	1×10^{17}	1×10^{17}	1×10^{17}	1×10^{17}	1×10^{17}	1×10^{17}
Drain doping (N_D) ($atoms/cm^3$)	1×10^{18} (n-type)	1×10^{18} (p-type)	1×10^{18} (n-type)	1×10^{18} (p-type)	1×10^{20} (n-type)	1×10^{18} (n-type)
Source doping (N_S) ($atoms/cm^3$)	1×10^{20} (p-type)	1×10^{20} (n-type)	1×10^{20} (p-type)	1×10^{20} (n-type)	1×10^{20} (p-type)	1×10^{18} (p-type)
Channel length (L_G)(nm)	100	100	100	100	100	105
L_1(nm)	–	–	–	–	50	50
L_2(nm)	–	–	–	–	50	50
L_{gap}(nm)	–	–	–	–	–	5 [57,110]
L_{ov}(nm)	–	–	20	20	20	–
ϕ_1(eV)	4.3	5.2	4.9	4.5	4.5	5.4
ϕ_2(eV)	–	–	–	–	4.9	4.3

Fig. 6.1 shows the cross-sectional view of an n-DGTFET. The top gate is called G_1, and the bottom gate is called G_2. Conventionally, the two gates are tied together to boost the I_{ON} [4, 46]. However, in the DGTFET-based logic function implementation, the two gates are biased independently at the voltages, V_A and V_B. In an OR function implementation, the band-to-band tunneling (BTBT) should occur when one or both the inputs are at logic ‘1’ (refer to Table. 6.1). Therefore, a conventional n-DGTFET with independent gate-control performs the OR logic function. The device parameters used in the simulations for the DGTFET-based OR function are listed in Table. 6.2.

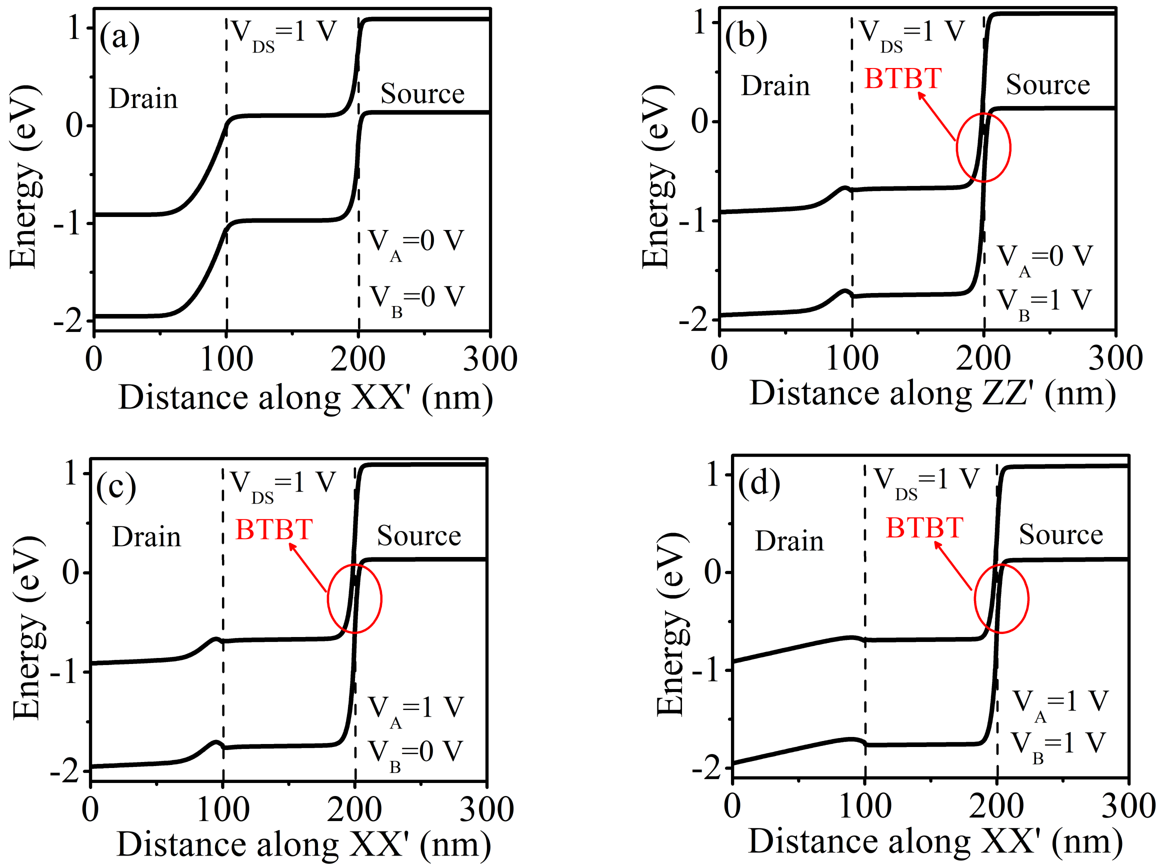


Figure 6.2: Energy band diagram of a DGTFET realizing OR logic function, along X-axis V_{DS} = 1 V, for input combinations (a) “00”, (b) “01”, (c) “10” and (d) “11”. Note that the band diagram is shown along the cutline ZZ′ for the “01” case and along the cutline XX′ for ”10” case because the surface-tunneling is maximum near the gate where the input is logic ‘1’ in n-TFET.

Fig. 6.2 illustrates the band diagrams along the length of the device for DGTFET realizing OR logic function for different input combinations, showing that the BTBT is enabled in "01", "10" and "11" cases.

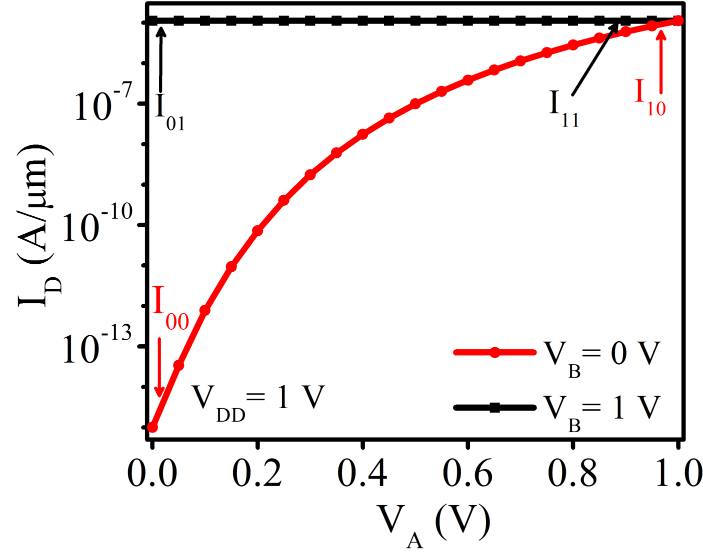


Figure 6.3: Transfer characteristics of DGTFET realizing OR logic function.

The transfer characteristics of the DGTFET realizing OR function are shown in Fig. 6.3. It provides an $\mathrm{I_{ON}/I_{OFF}}$ ratio of $\sim 10^{10}$ at $\mathrm{V_{DD}} = 1$ V.

6.2.1 Impact of Process-Induced Variations

It is worth pointing out that the $\mathrm{I_{ON}/I_{OFF}}$ ratio is sensitive to process-induced variations. For example, due to process-induced variations, the gates can shift, creating underlap or overlap with the source. Using simulations, it is found that when both the gates shift by $5\ \mathrm{nm}$ creating underlap with the source, the $\mathrm{I_{ON}/I_{OFF}}$ ratio reduces from 1×10^{10} to 2.7×10^{9}. Similarly, when both the gates shift by $5\ \mathrm{nm}$ creating an overlap with the source, the $\mathrm{I_{ON}/I_{OFF}}$ ratio reduces from 1×10^{10} to 1×10^{9}. Further, the impact of variation in silicon

body thickness (t_{si}) on the I_{ON}/I_{OFF} ratio of the logic function is examined. Using simulations, it is found that a small variation in t_{si} of ± 2 nm does not impact the I_{ON}/I_{OFF} ratio of the OR logic function.

6.2.2 Scaling Trend

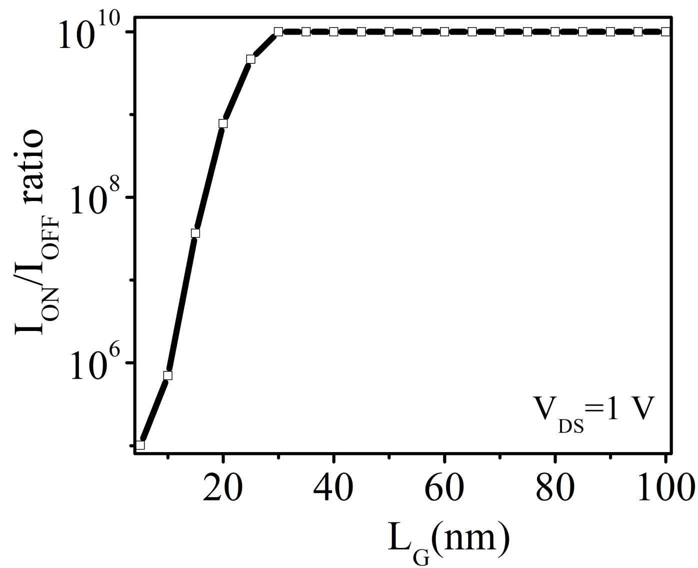


Figure 6.4: Scaling Trend for DGTFET realizing OR logic function.

Moreover, it is important to examine the effect of change in gate length on the I_{ON}/I_{OFF} ratio for the OR gate. It is noticed that the I_{ON}/I_{OFF} ratio remains unaffected for $L_G \geq 30$ nm, and then decreases. However, the functionality remains intact for $L_G \geq 15$ nm, though the I_{ON}/I_{OFF} ratio decreases to 3.7×10^7 as shown in Fig. 6.4.

6.3 Realizing NAND Logic Functions using DGTFET

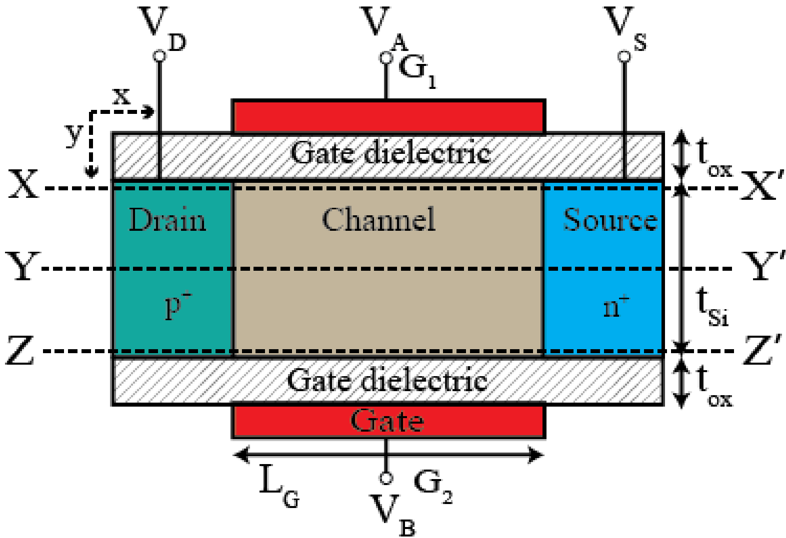


Figure 6.5: Cross-sectional view of a p-DGTFET realizing NAND logic function.

Fig. 6.5 shows the cross-sectional view of a p-DGTFET. In a NAND function implementation, the BTBT should occur when one or both the inputs are at logic '0'. Therefore, it can be realized using p-DGTFET with independent gate control, as shown in Fig. 6.5. The device parameters used in the simulations for the DGTFET-based NAND function are listed in Table. 6.2.

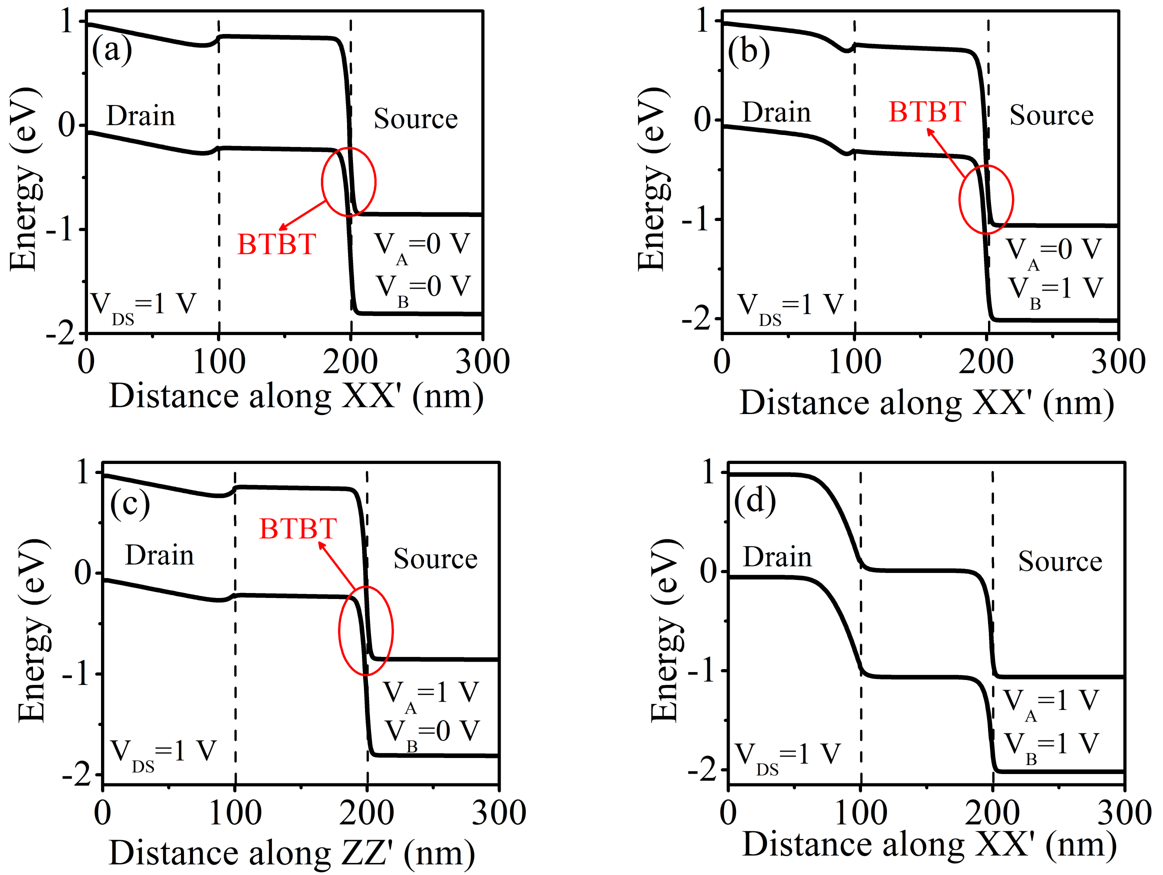


Figure 6.6: Energy band diagram of a DGTFET realizing NAND logic function, along X-axis $V_{DS} = 1$ V, for input combinations (a) “00”, (b) “01”, (c) “10” and (d) “11”. Note that the band diagram is shown along the cutline XX′ for the “01” case and along the cutline ZZ′ for ”10” case because the surface-tunneling is maximum near the gate where the input is logic ‘0’ in p-TFET.

Fig. 6.6 illustrates the band diagrams along the length of the device for DGTFET realizing NAND logic function for different input combinations, showing that the BTBT is enabled in “00”, “01” and “10” cases.

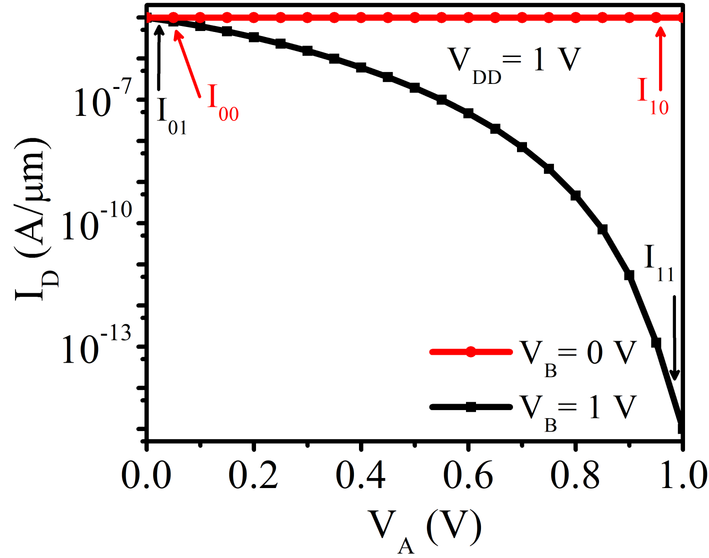


Figure 6.7: Transfer characteristics of DGTFET realizing NAND logic function.

The transfer characteristics of the DGTFET realizing NAND function are shown in Fig. 6.7. It provides an I_{ON}/I_{OFF} ratio of $\sim 10^{10}$ at $V_{DD} = 1$ V.

6.3.1 Impact of Process-Induced Variations

It is worth pointing out that the I_{ON}/I_{OFF} ratio is sensitive to process-induced variations. For example, due to process-induced variations, the gates can shift, creating, underlap or overlap with the source. Using simulations, it is found that when both the gates shift by 5 nm creating underlap with the source, the I_{ON}/I_{OFF} ratio reduces from 1×10^{10} to 2.6×10^{9}. Similarly, when both the gates shift by 5 nm creating an overlap with the source, the I_{ON}/I_{OFF} ratio reduces from 1×10^{10} to 1×10^{9}. Further, the impact of variation in silicon body thickness (t_{si}) on the I_{ON}/I_{OFF} ratio of the logic function is examined. Using simulations, it is found that a small variation in t_{si} of ± 2 nm does not impact the I_{ON}/I_{OFF} ratio of the NAND logic function.

6.3.2 Scaling Trend

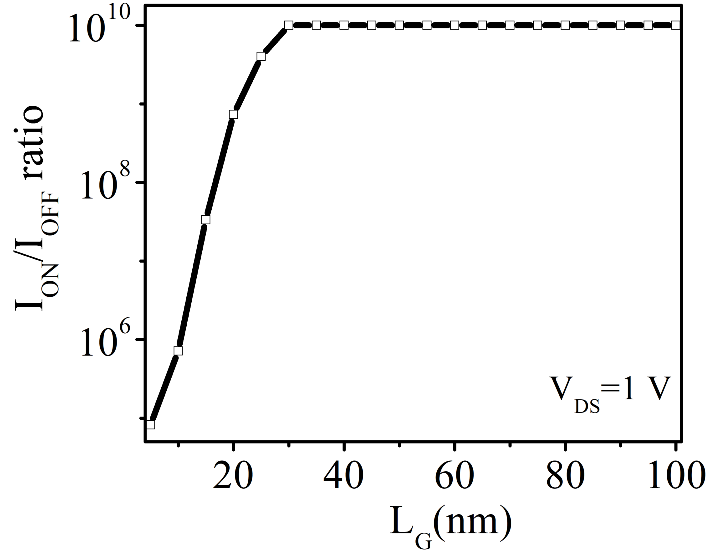


Figure 6.8: Scaling Trend for DGTFET realizing NAND logic function.

It is noticed that the $\mathrm{I_{ON}/I_{OFF}}$ ratio remains unaffected for $\mathrm{L_G} \geq 30$ nm, and then decreases. However, the functionality remains intact for $\mathrm{L_G} \geq 15$ nm, though the $\mathrm{I_{ON}/I_{OFF}}$ ratio decreases to 3.3×10^7, as shown in Fig. 6.8.

6.4 Realizing AND function using DGTFET

The AND function requires the BTBT to occur only when the input combination is “11”. A n-DGTFET conducts in “01”, “10”, and “11” cases (as shown in OR function realization). Therefore, to obtain a DGTFET realizing AND function, there is a need to stop the conduction in “01” and “10” cases. The key elements in the proposed implementation of the AND logic are as follows [168]:

1. Employing a gate–source overlap in the device to suppress the surface-

tunneling (explained later in the chapter). This results in a low I_{OFF} when the gate terminals are at logic "00","01" and "10".

2. The body-tunneling (explained later in the chapter) is maximized by choosing an appropriate silicon body thickness (t_{si}). This results in a high I_{ON} when the gate terminals are at logic "11". Therefore, a high I_{ON}/I_{OFF} ratio is achievable in the proposed logic realization.

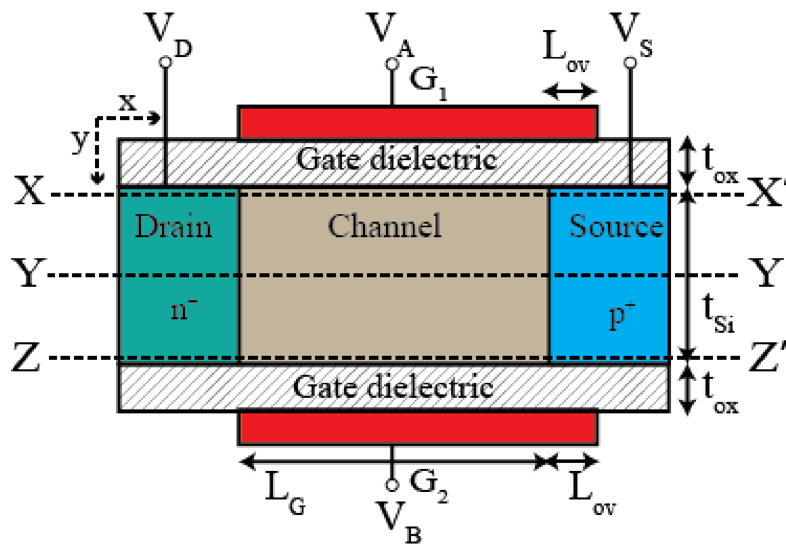


Figure 6.9: Cross-sectional view of DGTFET realizing AND logic function.

The cross-sectional view of the DGTFET performing the AND function is shown in Fig. 6.9.

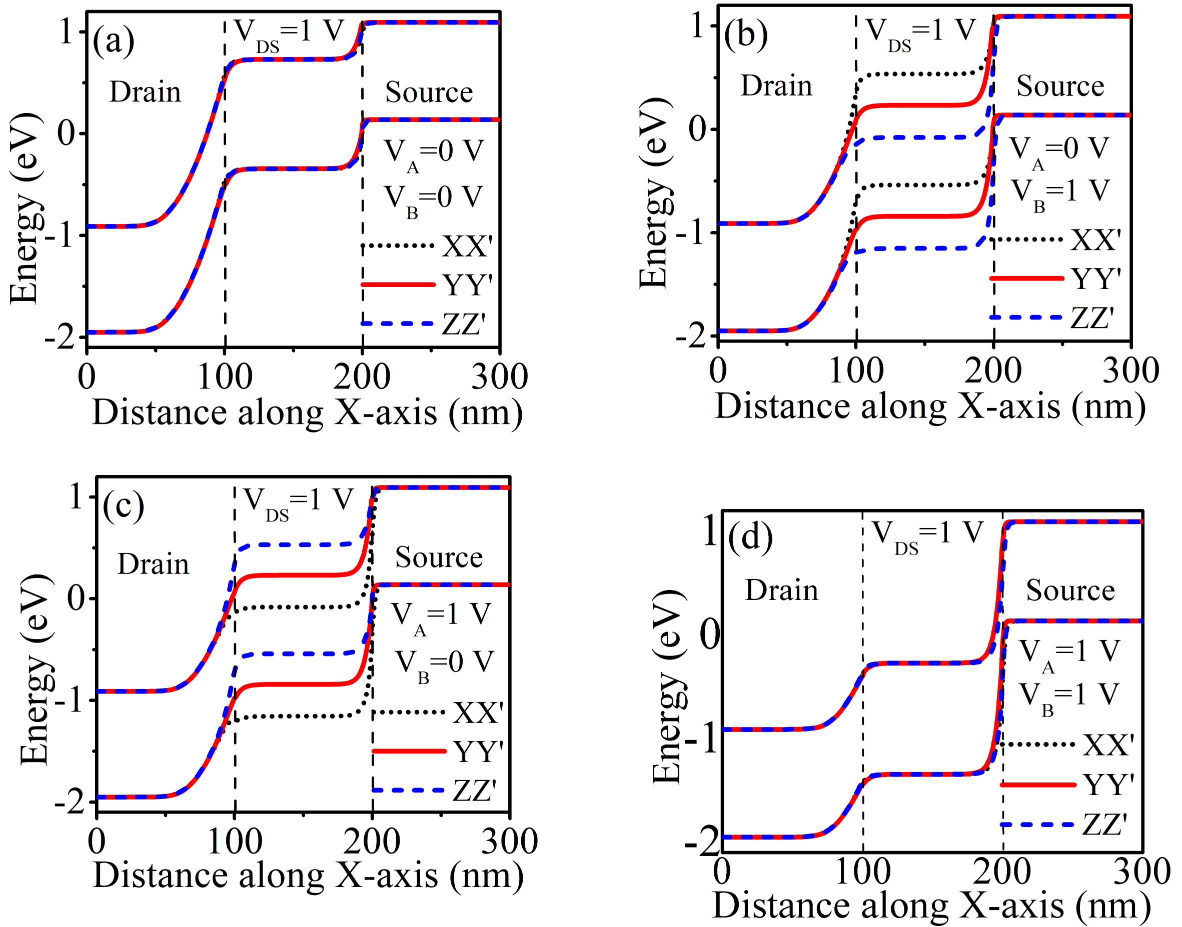


Figure 6.10: Energy band diagram along X-axis for different cutlines XX′, YY′ and ZZ′ at $V_{DS} = 1$ V without gate–source overlap, for input combinations (a) "00", (b) "01", (c) "10" and (d) "11".

Fig. 6.10 shows the band diagram of the DGTFET without gate–source overlap. It can be observed that tunneling is enabled near the gates (along the cutlines XX′, ZZ′, or both) at all bias conditions. The tunneling near the silicon–dielectric interface is referred to as the surface-tunneling. However, tunneling gets enabled in the middle of the silicon body (along the cutline YY′), only when input at both the gates (top gate and the bottom gate) is high (Fig. 6.10(d)). The tunneling deep inside the silicon body is referred to as body-tunneling.

The band diagrams in Fig. 6.10 suggest that if the surface-tunneling can be

inhibited in the device, then the tunneling current in the "01" and "10" cases will be negligible since the body-tunneling is not occurring at these bias conditions. In this work, the inhibition of surface-tunneling is achieved using the gate–source overlap.

6.4.1 Addition and optimization of Gate–source Overlap

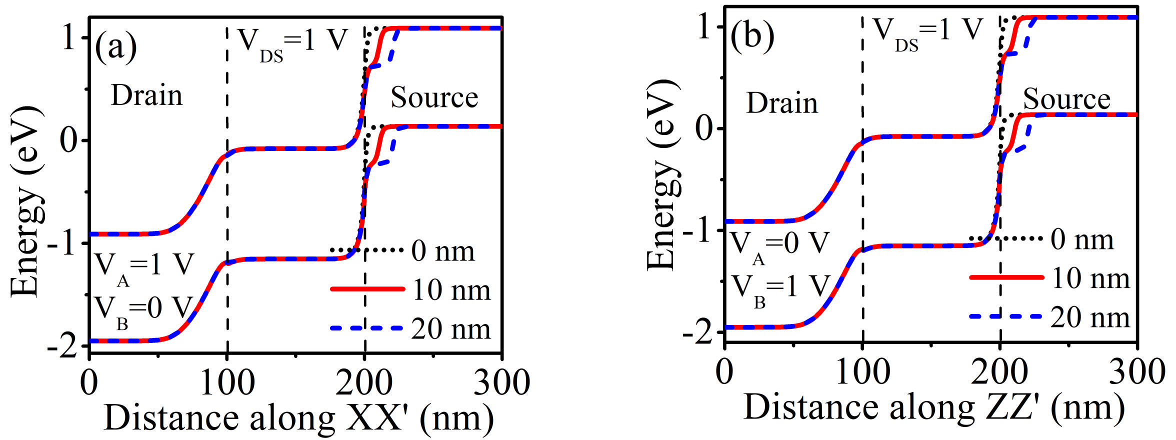


Figure 6.11: Energy band diagram of a DGTFET realizing AND logic function, along X-axis at $V_{DS} = 1$ V with varying gate–source overlap from 0 to 20 nm, for input combinations (a) "10", and (b) "01".

Fig. 6.11 shows that the addition of the gate–source overlap affects the band alignment of the device such that the surface tunneling (along the cutline XX′ and ZZ′) is inhibited. When $L_{ov} = 0$, the tunneling barrier width is low at the tunneling junction, as shown in Fig. 6.11. Therefore, a high I_{OFF} ($\sim 10^{-9}$ A/μm) flows through the device. As L_{ov} increases, the tunneling barrier width increases, and BTBT decreases as shown in Fig. 6.11. However, when L_{ov} is increased beyond 20 nm, no further decrease in the drain current is observed. Therefore, $L_{ov} = 20$ nm is chosen to minimize the I_{OFF} for the input combinations "01" or "10". However, the functionality remains intact till $L_{ov} = 10$ nm

with an I_{ON}/I_{OFF} ratio of 9×10^6. When $L_{ov} < 10$ nm, the I_{ON}/I_{OFF} ratio starts decreasing sharply and the functionality is lost.

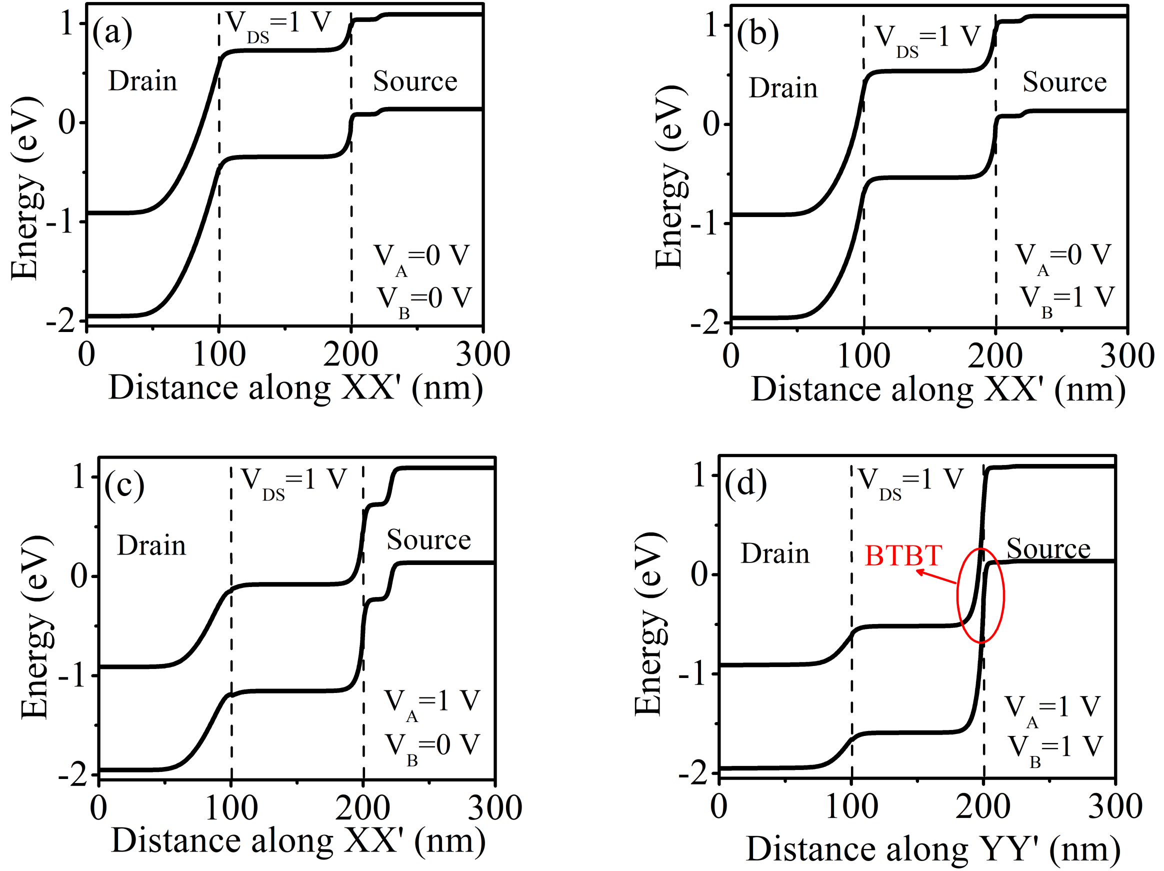


Figure 6.12: Energy band diagram of a DGTFET realizing AND logic function, along X-axis at $V_{DS} = 1$ V, for input combinations (a) "00", (b) "01", (c) "10" and (d) "11". Note that the band diagram is shown along the cutline YY' for the "11" case because the body-tunneling occurs in the middle of the body, as explained above.

The device parameters used in the simulations for the DGTFET-based AND function are listed in Table. 6.2. The band diagrams for DGTFET realizing AND logic function along the length of the device for different input combinations are shown in Fig. 6.12, illustrating that the BTBT is enabled for the "11" case.

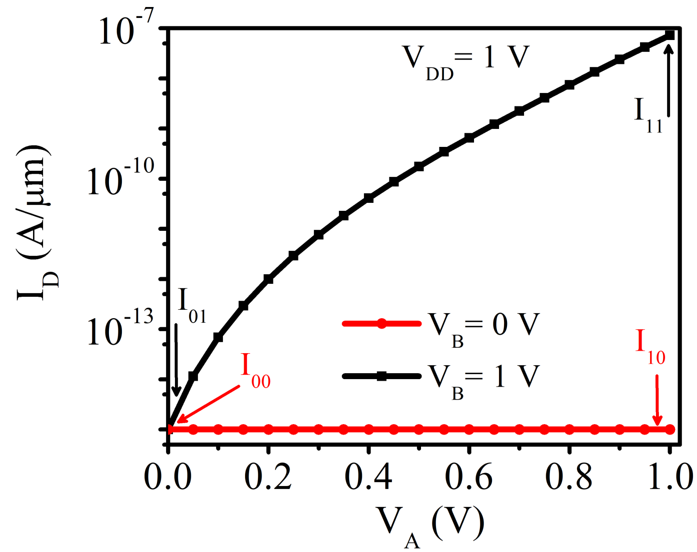


Figure 6.13: Transfer characteristics of DGTFET realizing AND logic function.

The transfer characteristics of the DGTFET performing AND function are shown in Fig. 6.13. The I_{ON}/I_{OFF} ratio of orders $\sim 10^8$ at $V_{DD} = 1$ V is observed.

6.4.2 Optimization of Silicon body thickness

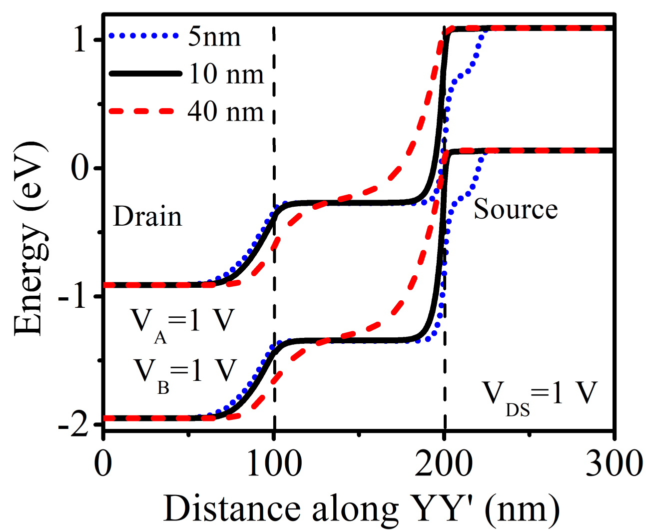


Figure 6.14: Energy band diagram of a DGTFET realizing AND logic function, along X-axis at $V_{DS} = 1$ V, for the input combinations "11" with varying t_{si}.

It is important to analyze the impact of silicon body thickness (t_{si}) on the electrical characteristics of the DGTFET that realizes the AND logic function. It is found that as t_{si} increases, the body-tunneling decreases since the impact of the gate bias inside the silicon body becomes weak. This leads to an increase in the tunneling barrier width, as shown in Fig. 6.14. Since the tunneling barrier width increases, the BTBT and the I_{ON} decreases. This leads to undesirable degradation in the I_{ON}/I_{OFF} ratio. Therefore, a large t_{si} is not preferred for a DGTFET that realizes the AND function. Nevertheless, t_{si} cannot be too small since the gate–source overlap inhibits BTBT throughout the silicon body. Therefore, for a reasonable I_{ON}/I_{OFF} ratio, a $t_{si} \sim 10$ nm is chosen.

6.4.3 Scaling Trend

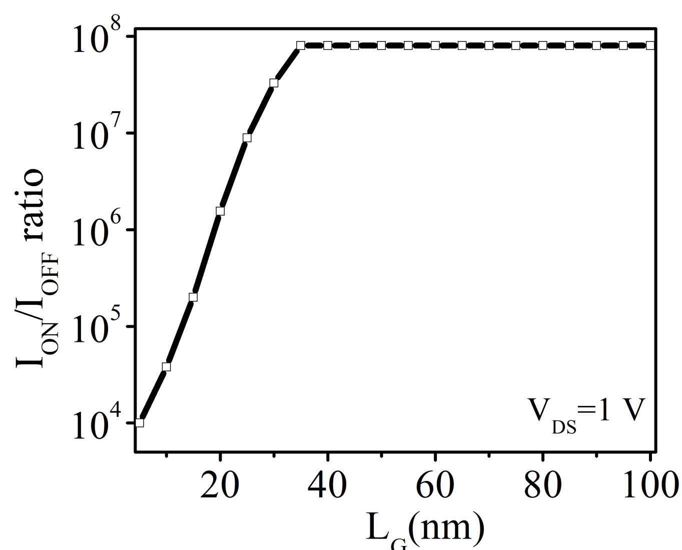


Figure 6.15: Scaling Trend for DGTFET realizing AND logic function.

The effect of the change in the gate length on the I_{ON}/I_{OFF} ratio is evaluated. It is noticed that the I_{ON}/I_{OFF} ratio remains unaffected for $L_G \geq 35$ nm, and then

decreases. However, the functionality remains intact for $\mathrm{L_G} \geq 20\ \mathrm{nm}$, though the $\mathrm{I_{ON}/I_{OFF}}$ ratio decreases to 1.5×10^6, as shown in Fig. 6.15.

6.4.4 Impact of Independent Gate Control and Gate–source Overlap on Electrical Characteristics

6.4.4.1 $\mathrm{SS_{avg}}$

$\mathrm{SS_{avg}}$ is an important parameter for digital applications since lower $\mathrm{SS_{avg}}$ allows low voltage and energy-efficient operations [4, 19]. The $\mathrm{SS_{avg}}$ is calculated as the inverse slope extracted from the transfer characteristics from $\mathrm{V_A} = 0$ to the point at which $\mathrm{I_D} = 10^{-9}\ \mathrm{A}/\mu\mathrm{m}$.

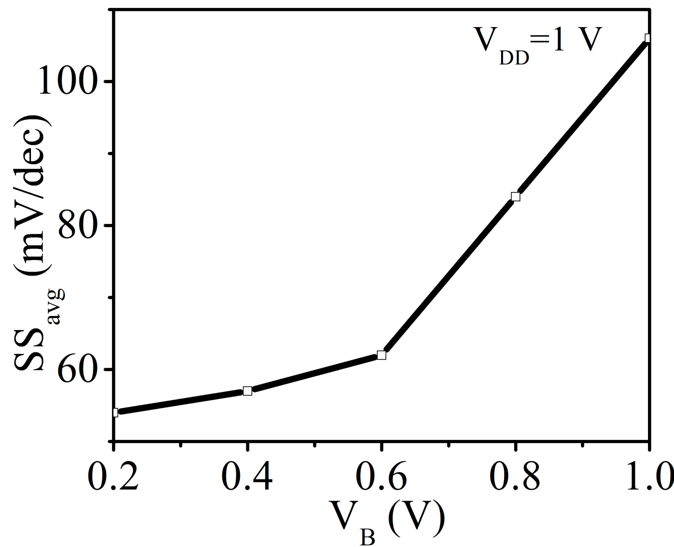


Figure 6.16: Variation of $\mathrm{SS_{avg}}$ with respect to $\mathrm{V_B}$. The $\mathrm{SS_{avg}}$ is extracted from the transfer characteristics of $\mathrm{I_D}$ vs. $\mathrm{V_A}$.

To study the effect of independently-controlled gate, $\mathrm{SS_{avg}}$ is extracted from the transfer characteristics ($\mathrm{I_D}$ vs. $\mathrm{V_A}$) at different $\mathrm{V_B}$, as shown in Fig. 6.16. It can be inferred from Fig. 6.16 that as $\mathrm{V_B}$ increases, the $\mathrm{SS_{avg}}$ increases. The

$\mathrm{SS_{avg}}$ is extracted to be $105\ \mathrm{mV/dec}$ for the DGTFET-based AND logic. On the other hand, when both the gate terminals are tied together such that $\mathrm{V_A} = \mathrm{V_B}$, the $\mathrm{SS_{avg}}$ is found to be $50\ \mathrm{mV/dec}$. Therefore, the degraded $\mathrm{SS_{avg}}$ in the AND logic realization can be attributed to the independently-controlled gate. The degradation of $\mathrm{SS_{avg}}$ with increase in $\mathrm{V_B}$ can be explained by examining the device under different bias-conditions, as explained below.

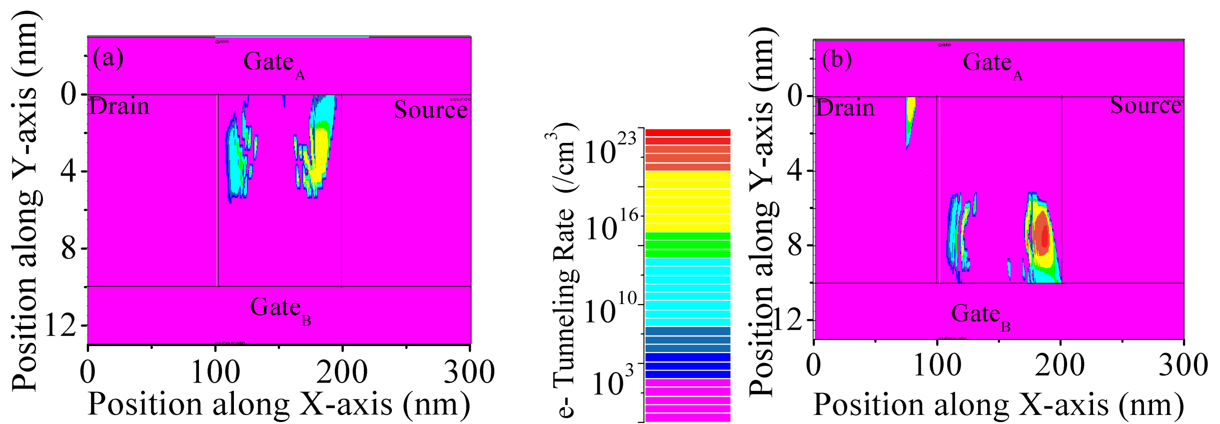


Figure 6.17: Tunneling rate in the TFET at $\mathrm{V_{DS}} = \mathrm{V_{DD}}$ (a) For $\mathrm{V_A} = 0.7$ V and $\mathrm{V_B} = 0.5$ V (b) For $\mathrm{V_A} = 0$ V and $\mathrm{V_B} = 1$ V.

Fig. 6.17(a) and 6.17(b) show the tunneling rate in the body of DGTFET at two different $\mathrm{V_B}$ (0.5 V and 1 V). In these figures, appropriate $\mathrm{V_A}$ is chosen such that the drain current just starts to take-off in the transfer characteristics. The drain current starts to take-off in the transfer characteristics when the BTBT gets initiated due to the alignment of the valence band and the conduction band. It is worth pointing out that at different $\mathrm{V_B}$, BTBT gets initiated at different $\mathrm{V_A}$. For instance, when $\mathrm{V_B} = 0.5$ V, BTBT gets initiated at $\mathrm{V_A} = 0.7$ V and when $\mathrm{V_B} = 1$ V, BTBT gets initiated at $\mathrm{V_A} = 0$ V. Therefore, in the Fig. 6.17(a) and 6.17(b) different $\mathrm{V_A}$ are chosen to determine the regions where BTBT initiates. From Fig. 6.17(a) it is evident that BTBT is initiated in the upper half of the

device when $V_B = 0.5$ V. It illustrates that when $V_B << V_{DD}$, the control of the top gate is dominant. However, when $V_B \approx 1$ V, BTBT initiates in the lower half of the device, as shown in Fig. 6.17(b), illustrating the dominant control of the bottom gate at higher V_B. In Fig. 6.17(b), it can be observed that there is a small BTBT occurring in the drain side closer to the top-gate. However, the contribution of this component of BTBT on the drain current is negligible.

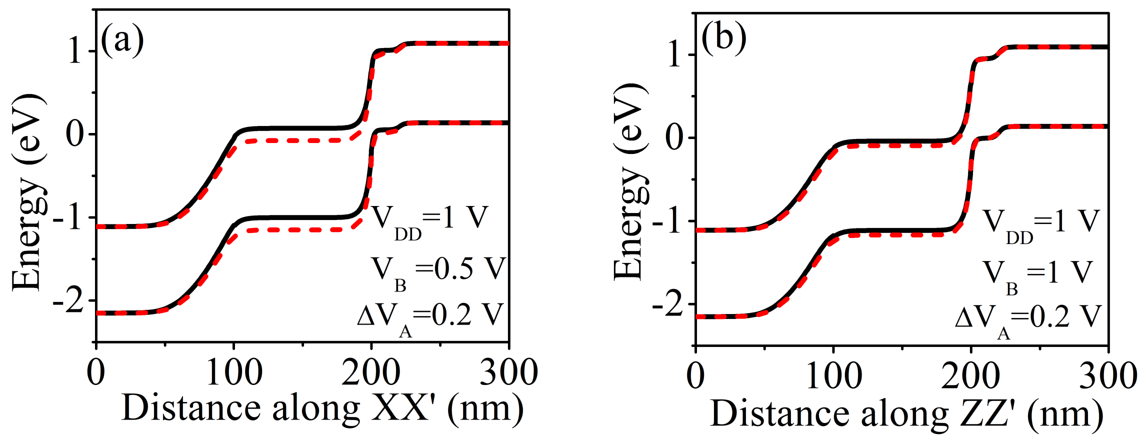


Figure 6.18: Energy band diagram at $V_{DS} = V_{DD}$ (a) For $\Delta V_A = 0.2$ V and $V_B = 0.5$ V, the extracted energy band overlap $\Delta\Phi = 0.14$ eV (b) For $\Delta V_A = 0.2$ V and $V_B = 1$ V, the extracted energy band overlap is $\Delta\Phi = 0.045$ eV.

Fig. 6.18(a) and 6.18(b) compare the band diagrams of the device for $V_B = 0.5$ V (along the cutline XX′) and $V_B = 1$ V (along the cutline YY′), keeping the same $\Delta V_A = 0.2$ V. ΔV_A is taken as the increase in the voltage V_A above the bias point at which the BTBT initiates. Different cutlines are chosen since BTBT initiates in different regions at different bias conditions, as explained above. The band diagrams show that for the same ΔV_A, the increase in the band alignment is more when $V_B = 0.5$ V compared to when $V_B = 1$ V. This results in a change in the drain current ($\Delta(\log I_D)$) by two decades and four decades, respectively, for $V_B = 1$ V and $V_B = 0.5$ V (for the same $\Delta V_A = 0.2$ V). Since

$SS_{avg} = \Delta V_A/\Delta(\log I_D)$, and $\Delta(\log I_D)$ is higher for $V_B = 0.5$ V, a smaller SS_{avg} is exhibited at $V_B = 0.5$ V compared to $V_B = 1$ V. Further, the simulations show that the architectural modifications such as gate–source overlap do not contribute to the degradation in the SS_{avg} of the DGTFET. The SS_{avg} for the conventional TFET with and without gate–source overlap was extracted and found to be the same. Therefore, the degradation in the SS_{avg} can solely be attributed to the independently-controlled gate and is prominent when the voltage at one of the terminals is fixed at a value close to V_{DD}.

6.4.4.2 I_{ON}/I_{OFF} ratio:

It is desirable to have a higher I_{ON}, lower I_{OFF}, and higher I_{ON}/I_{OFF} ratio for digital circuits. A higher I_{ON} leads to lower delays, and a lower I_{OFF} reduces the static power consumption. The AND function implementation proposed above is compact. However, it can be seen that the I_{ON} obtained for the DGTFET realizing AND functions is almost two order lower than the I_{ON} obtained for DGTFET realizing the OR/NAND function. This reduction in the I_{ON} can be attributed to the addition of gate–source overlap. In other words, the gate–source overlap employed to suppress the I_{OFF} adversely affects the I_{ON} too. Using simulations, it is found that the I_{ON} obtained with gate–source overlap is 40% lower as compared to the I_{ON} obtained without gate–source overlap in a DGTFET. This is because the surface-tunneling component gets suppressed even in the "11" case, as explained above, due to the gate–source overlap. Therefore, the techniques that can boost the I_{ON} are critical in the proposed logic realizations.

Various techniques have been proposed to boost the I_{ON} in a TFET [42, 67]. However, the proposed DGTFET-based logic implementations logic works well only when the gate–source overlap is able to turn-OFF the device when the input combinations are "10" and "01". The current boosting techniques which fail to do so cannot be used in these implementations (to increase the I_{ON}) since those techniques can adversely impact the functionality itself (by drawing a higher I_{OFF} and thus delivering a lower I_{ON}/I_{OFF} ratio). Hence, it is important to analyze whether techniques used for increasing I_{ON} in a conventional DGTFET can be adopted in logic implementations.

a. Employing high-k dielectric:

When the dielectric constant (ϵ_{ox}) of the gate insulator in a TFET is increased, the tunneling current increases [4, 7]. However, the application of high-k dielectric in a TFET that realizes AND logic function is complicated.

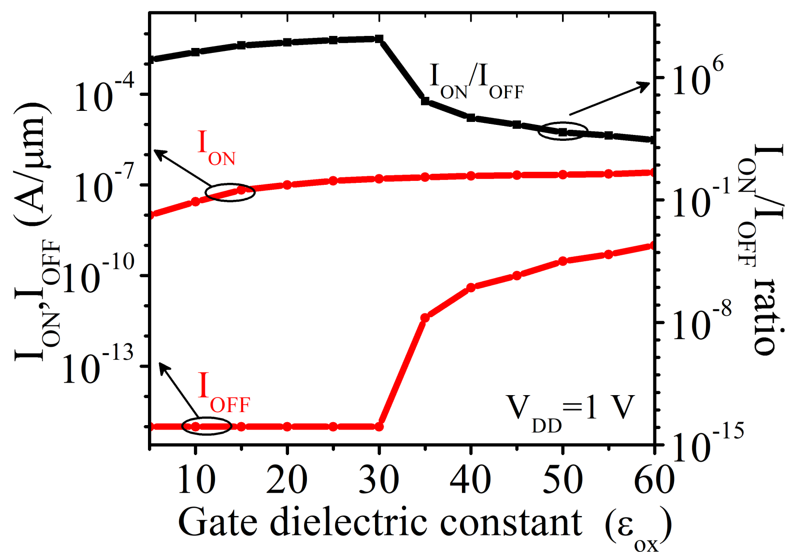


Figure 6.19: Variation of I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} with respect to ϵ_{ox}.

Fig. 6.19 shows the I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio at different ϵ_{ox}. As ϵ_{ox} increases, for a fixed oxide thickness (t_{ox}), the control of the gate becomes more prominent, resulting in a sharper band-bending and increased I_{ON}. However, as the dielectric constant increases beyond a certain limit ($\epsilon_{ox} > 30$), it becomes difficult to suppress the BTBT at the surface of the device using gate–source overlap. As a result, with the increase in ϵ_{ox}, the I_{OFF} starts increasing rapidly when $\epsilon_{ox} > 30$. Therefore, a lower I_{ON}/I_{OFF} ratio is obtained for a high value of ϵ_{ox}.

b. Employing strain:

The strain has been exploited in TFETs to achieve a higher I_{ON} [24, 61, 90, 132, 169]. A strained-silicon-based DGTFET (SDGTFET) has been described in Section: 3.6.1. In this section, the suitability of the proposed technique of realizing AND function in an SDGTFET is examined.

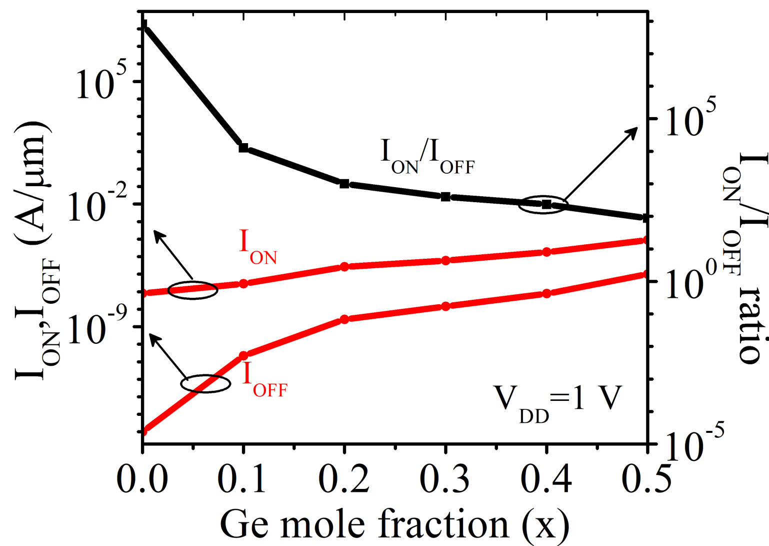


Figure 6.20: Variation of I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} ratio at different germanium mole fractions (x) in SDGTFET.

Fig. 6.20 shows the I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio at different Ge mole fraction (x) in SDGTFET. It can be seen that although I_{ON} increases with increasing x, I_{OFF} also increases leading to a degraded I_{ON}/I_{OFF} ratio at higher Ge mole fractions. The I_{OFF} increases at a higher Ge mole fraction because the device cannot be effectively turned-OFF as explained in the following paragraphs.

c. Employing heterojunctions:

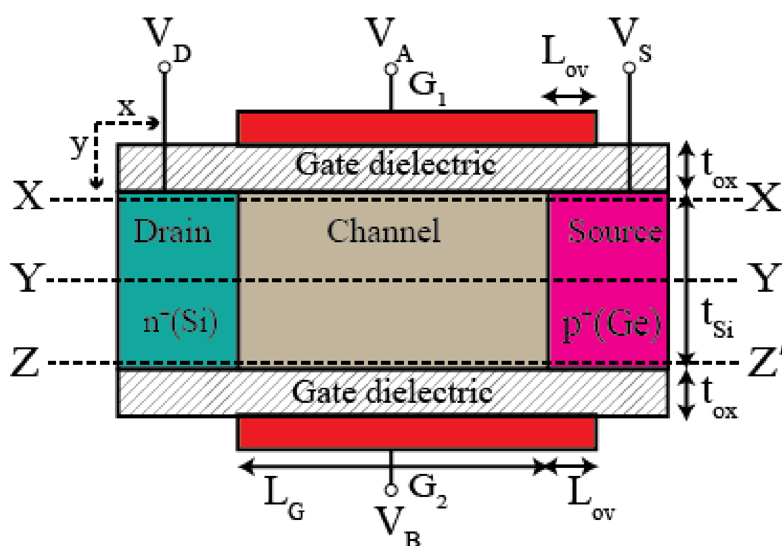


Figure 6.21: Cross-sectional view of an HJ-TFET that realizing AND logic function.

Table 6.3: Device parameters used in the simulation

Parameter	Value
Supply voltage (V_{DD})	1 V
Gate work-function (ϕ_m)	4.9 eV
Silicon film thickness (t_{si})	10 nm
Gate dielectric constant (ϵ_r)	15.6
Gate oxide thickness (t_{ox})	2 nm (Effective Oxide Thickness; EOT= 0.5 nm)
Channel length (L_C)	100 nm
Gate–Source Overlap (L_{ov})	20 nm
Drain doping (N_D) (n-type)	1×10^{18} atoms/cm^3
Channel doping (N_C)	1×10^{17} atoms/cm^3
Source doping (N_S) (p-type)	1×10^{20} atoms/cm^3 (Si-TFET) 4×10^{19} atoms/cm^3 (HJ-TFET)

Silicon–Germanium heterojunction TFET with germanium as the source material has been proposed and widely studied in literature [40, 65, 71, 170]. Using a Si-Ge heterojunction helps in obtaining a higher I_{ON}/I_{OFF} ratio due to smaller effective bandgap [40]. Therefore, in this section, the application of silicon–germanium heterojunction TFET (HJ-TFET) for realizing AND logic functions is investigated. The HJ-TFET realizing AND logic function is shown in Fig. 6.21. The tunneling parameters of germanium used in this work are calibrated using Fig. 4 of ref. [171]. The relevant device parameters used for Si-TFET and HJ-TFET are listed in Table. 6.3.

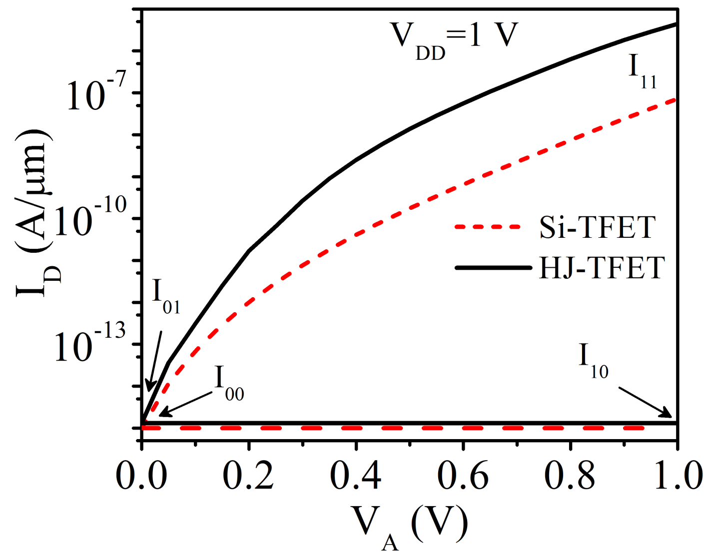


Figure 6.22: Comparison of transfer characteristics of Si-TFET and HJ-TFET-based AND at $V_{DD} = 1$ V and $L_G = 100$ nm.

Fig. 6.22 compares the transfer characteristics of AND logic function realized using Si-TFET and HJ-TFET at $V_{DD} = 1$ V. It can be inferred from Fig. 6.22 that the I_{ON} improves from 8.4×10^{-10} A/μm in Si-TFET to 1.2×10^{-7} A/μm in HJ-TFET. The I_{ON}/I_{OFF} improves from 1×10^{7} in Si-TFET to 5×10^{9} in

HJ-TFET. The $\mathrm{SS_{avg}}$ improves from $105\ \mathrm{mV/dec}$ in Si-TFET to $58\ \mathrm{mV/dec}$ in HJ-TFET, at $\mathrm{V_{DD}} = 1\ \mathrm{V}$.

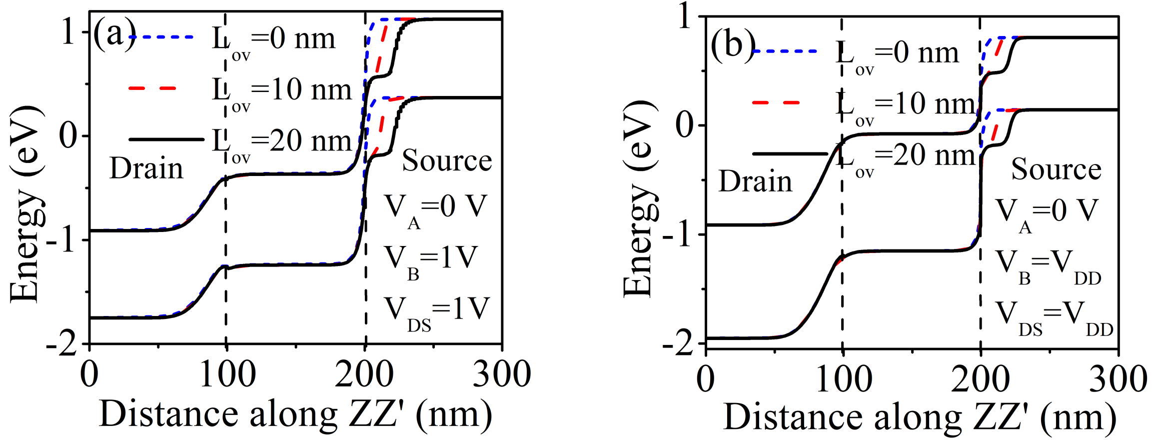


Figure 6.23: Energy band diagram at $\mathrm{V_A} = 0\ \mathrm{V}$ and $\mathrm{V_{DS}} = \mathrm{V_B} = \mathrm{V_{DD}}$ for different $\mathrm{L_{ov}}$ (a) SDGTFET (b) HJ-TFET.

Next, it is investigated why an SDGTFET-based AND logic implementation is unable to deliver a high $\mathrm{I_{ON}/I_{OFF}}$ ratio in contrast to the HJ-TFET-based AND logic implementation. The band diagrams for the SDGTFET and the HJ-TFET for different values of gate–source overlap ($\mathrm{L_{ov}}$) in the OFF-state ($\mathrm{V_{DS}} = \mathrm{V_B} = \mathrm{V_{DD}}$ and $\mathrm{V_A} = 0\ \mathrm{V}$) are shown in Fig. 6.23(a) and Fig. 6.23(b), respectively. It can be seen that in both cases, the tunneling barrier width (Λ) increases as the $\mathrm{L_{ov}}$ increases. However, the initial energy band overlap ($\Delta\Phi$) is comparatively high in SDGTFET compared to HJ-TFET. In a TFET, Λ and $\Delta\Phi$ are important factors in deciding the tunneling current (refer 2.3) [4]. Since the gate–source overlap is unable to decrease the $\Delta\Phi$ sufficiently in an SDGTFET, the $\mathrm{I_{OFF}}$ cannot be suppressed. It demonstrates that the proposed technique of realizing AND logic requires greater attention in TFETs with high $\Delta\Phi$.

6.5 Realizing NOR Logic Functions using DGTFET

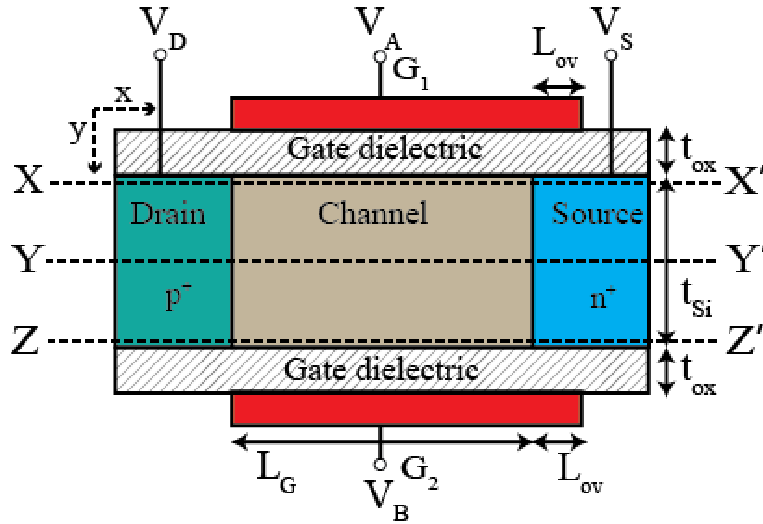


Figure 6.24: Cross-sectional view of DGTFET realizing NOR logic function.

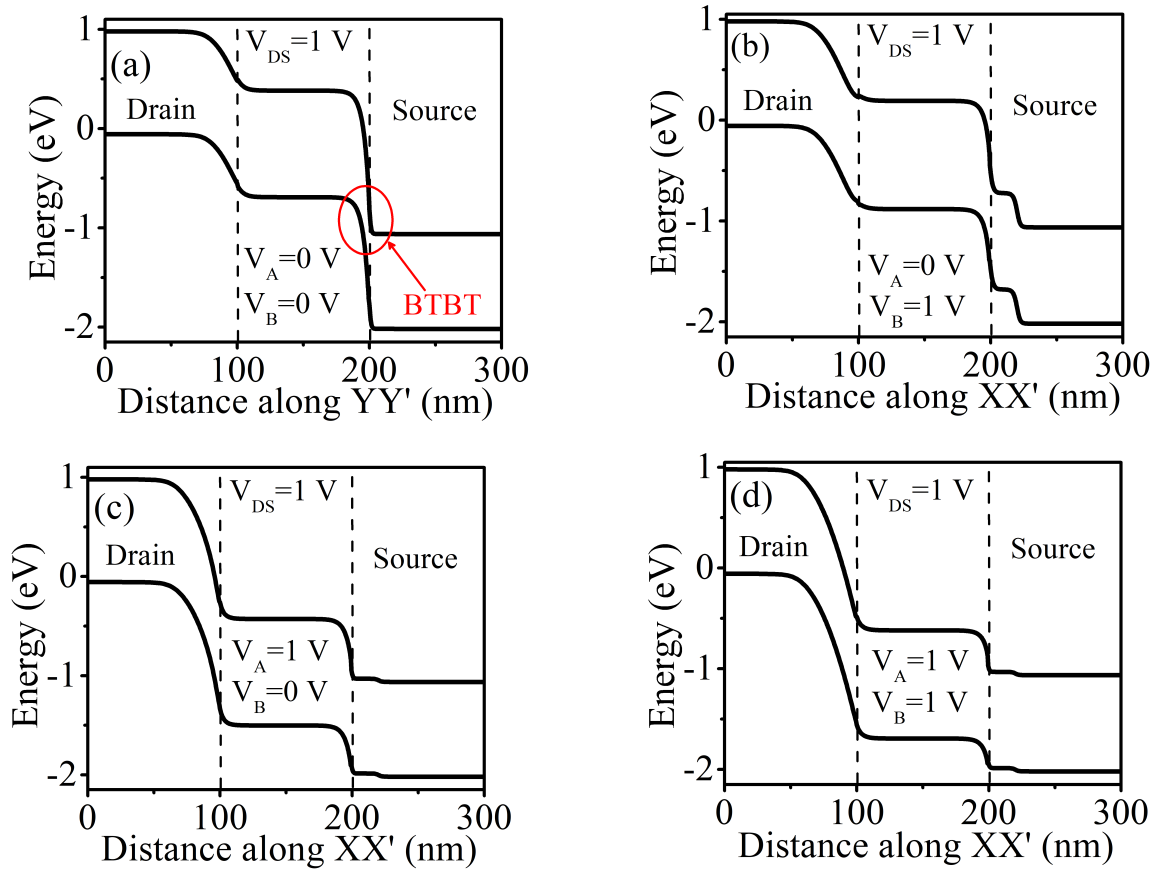


Figure 6.25: Energy band diagram of a DGTFET realizing NOR logic function, along X-axis V_{DS} = 1 V, for input combinations (a) “00”, (b) “01”, (c) “10” and (d) “11”

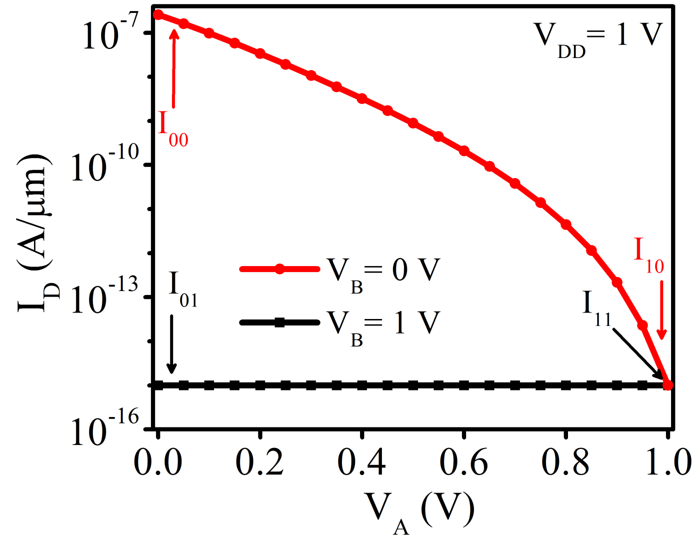


Figure 6.26: Transfer characteristics of DGTFET realizing NOR logic function.

In the NOR logic function, BTBT should occur only when the input combination is "00". This contrasts with the AND function where the BTBT should occur only when the input combination is "11". Therefore, to obtain a DGTFET realizing NOR function, a p-DGTFET is used instead of an n-DGTFET. Next, the BTBT needs to be suppressed in "01" and "10" cases, similar to AND function realization. Therefore, a gate–source overlap is added to the p-DGTFET to obtain NOR function, as shown in Fig. 6.24. The device parameters used in the simulations for the DGTFET-based NOR function are listed in Table. 6.2. The analysis of the DGTFET realizing NOR function is the same as that of the DGTFET realizing AND function. The band diagrams of the DGTFET realizing NOR logic function is shown in Fig. 6.25, showing that the BTBT is enabled only in the "00" case. The transfer characteristics of the DGTFET performing NOR function are shown in Fig. 6.26. The I_{ON}/I_{OFF} ratio of $\sim 10^8$ at $V_{DD} = 1$ V is observed.

6.5.1 Impact of Process-Induced Variations

The effect of change in the gate–source overlap due to process-induced variations is studied. It is found that when the gate–source overlap changes by ± 5 nm, the I_{ON}/I_{OFF} ratio is not significantly impacted. Furthermore, the functionality remains intact till $L_{ov} = 10$ nm with an I_{ON}/I_{OFF} ratio of 1×10^7. When $L_{ov} < 10$ nm, the I_{ON}/I_{OFF} ratio starts decreasing sharply and the functionality is lost. Further, the impact of variation in silicon body thickness (t_{si}) on the I_{ON}/I_{OFF} ratio of the logic function is examined. Using simulations, it is found that when t_{si} increases by 2 nm, the I_{ON}/I_{OFF} ratio degrades from 1×10^8 to 4×10^7. Similarly, when t_{si} decreases by 2 nm, the I_{ON}/I_{OFF} ratio improves from 1×10^8 to 1×10^9.

6.5.2 Scaling Trend

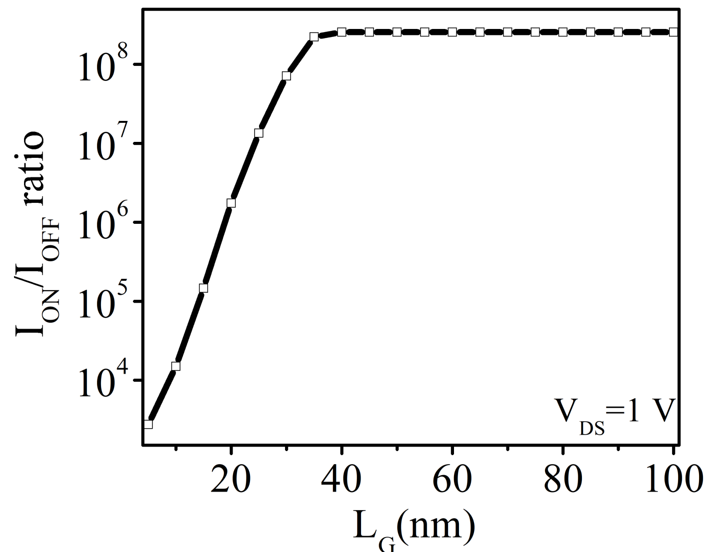


Figure 6.27: Scaling Trend for DGTFET realizing NOR logic function.

The effect of the change in the gate length on the I_{ON}/I_{OFF} ratio is examined. It is noticed that the I_{ON}/I_{OFF} ratio remains unaffected for $L_G \geq 35$ nm, and then decreases. However, the functionality remains intact for $L_G \geq 20$ nm, though the I_{ON}/I_{OFF} ratio decreases to 1.7×10^6, as shown in Fig. 6.27.

6.6 Realizing XNOR Logic Function using DGTFET

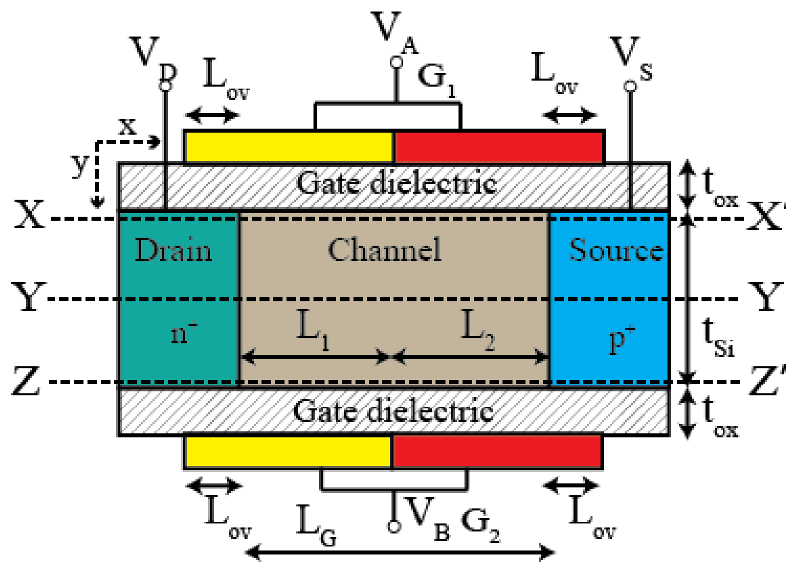


Figure 6.28: Cross-sectional view of DGTFET realizing XNOR logic function.

The XNOR logic function requires the BTBT to occur when the input combination is either "00" or "11" and inhibited when the input combination is either "01" or "10". The cross-sectional view of the DGTFET performing the XNOR function is shown in Fig. 6.28. The key elements in the proposed implementation of the XNOR logic are as follows:

1. The inhibition of the BTBT in the device in "01" and "10" cases can be achieved using the gate–overlap technique, as already explained in the AND function realization.

2. When the input combination is “00”, BTBT can be enabled using p-DGTFET. Similarly, when the input combination is “11”, BTBT can be enabled using n-DGTFET. Therefore, to obtain an XNOR function, a combination of functionalities of a p-DGTFET and an n-DGTFET is required. However, to avoid using two devices, the ambipolar conduction in the TFET has been exploited in the XNOR function realization.

3. Further, the DMG architecture is employed along with suitable work-functions ϕ_1 and ϕ_2 to create the current modulation required for the DGTFET-based XNOR function implementation. This enables the tunneling at the source–channel junction when the input combination is “11” and at the drain–channel junction (due to ambipolar conduction) when the input combination is “00”.

4. Furthermore, the gate–drain overlap is employed to inhibit the surface-tunneling completely. In AND function realization, the tunneling was occurring only at the source–channel junction. However, in XNOR function realization, the tunneling occurs at the source–channel junction as well as the drain–channel junction. Therefore, in addition to the gate–source overlap, gate–drain overlap is required to completely suppress the surface-tunneling in the device.

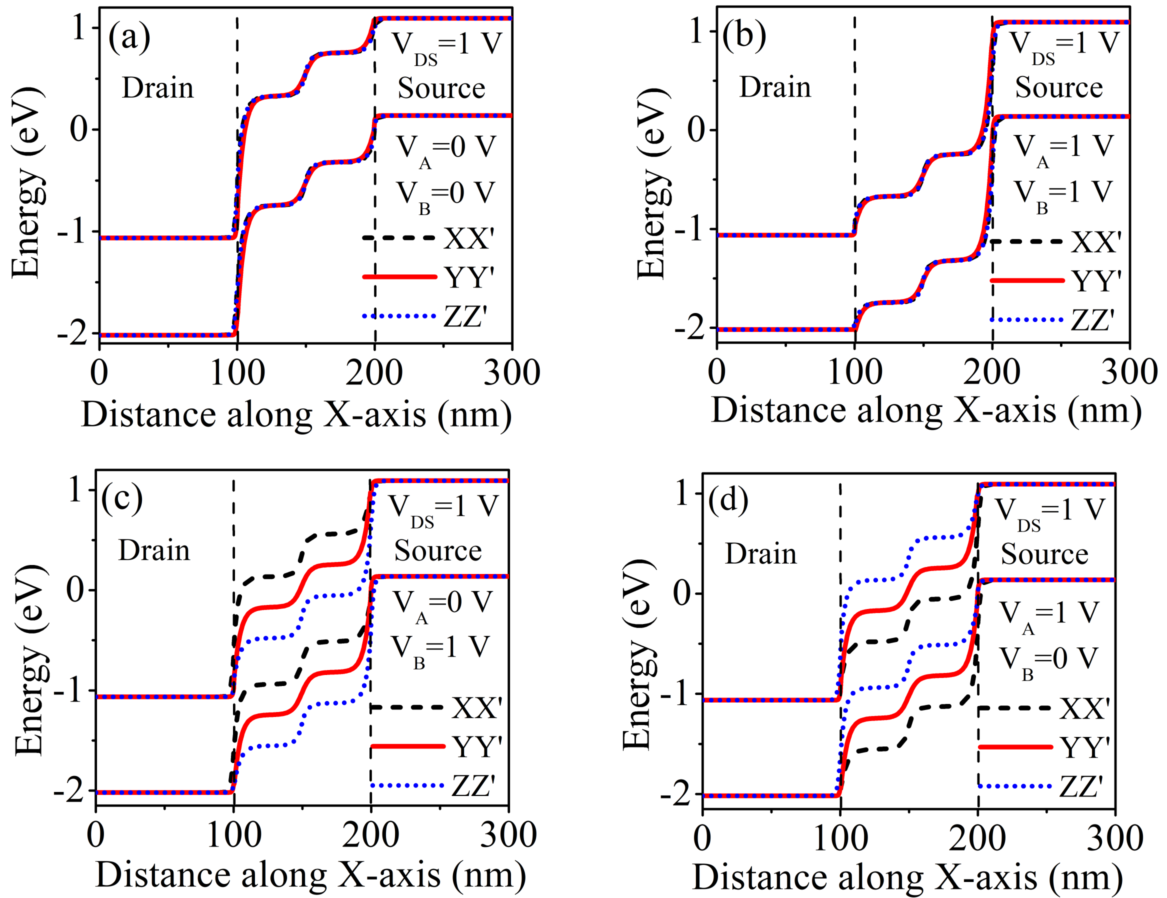


Figure 6.29: Energy band diagram along X-axis for different cutlines XX′, YY′ and ZZ′ at $V_{DS} = 1$ V without gate–source overlap and gate–drain overlap, when (a) Input combination is “00”, (b) Input combination is “11”, (c) Input combination is “01” and (d) Input combination is “10”.

First, the trend of BTBT in a DM-DGTFET without overlap is examined. Using simulations, it is found that in a DM-DGTFET without overlap, the BTBT occurs at the drain–channel junction along the whole silicon body in “00” case 6.29(a). However, the BTBT occurs at the source–channel junction along the whole silicon body in “11” case 6.29(b). In the “01” case, the band alignment is such that the tunneling occurs at the drain–channel junction along the cutline XX′ (near the top gate) and at the source–channel junction along the cutline ZZ′ (near the bottom gate) 6.29(c). In the “10” case, the band alignment is

such that the tunneling occurs at the source–channel junction along the cutline XX′ and at the drain–channel junction along the cutline ZZ′ 6.29(d). To obtain the XNOR functionality, the surface tunneling component, i.e., tunneling along the cutline XX′ and ZZ′, both need to be inhibited using the overlap technique. Since the BTBT at the drain–channel and the source–channel junction both need to be inhibited, the gate–source overlap and gate–drain overlap are used in DM-DGTFET-based XNOR implementation, as shown in Fig. 6.28. This is in contrast to the AND function realization, where only gate–source overlap is used. This is because, in the AND realization, the BTBT occurs only at the source–channel junction and was inhibited at the drain–channel junction due to the low drain doping ($\mathrm{N_D} = 1 \times 10^{18}\ \mathrm{atoms/cm^3}$). Additionally, it is important to note that due to the gate–source overlap, there is a possibility of vertical line tunneling [82, 172]. However, in this work, the work-functions ϕ_1 and ϕ_2 are selected, such that no vertical line tunneling occurs in the overlapped source region.

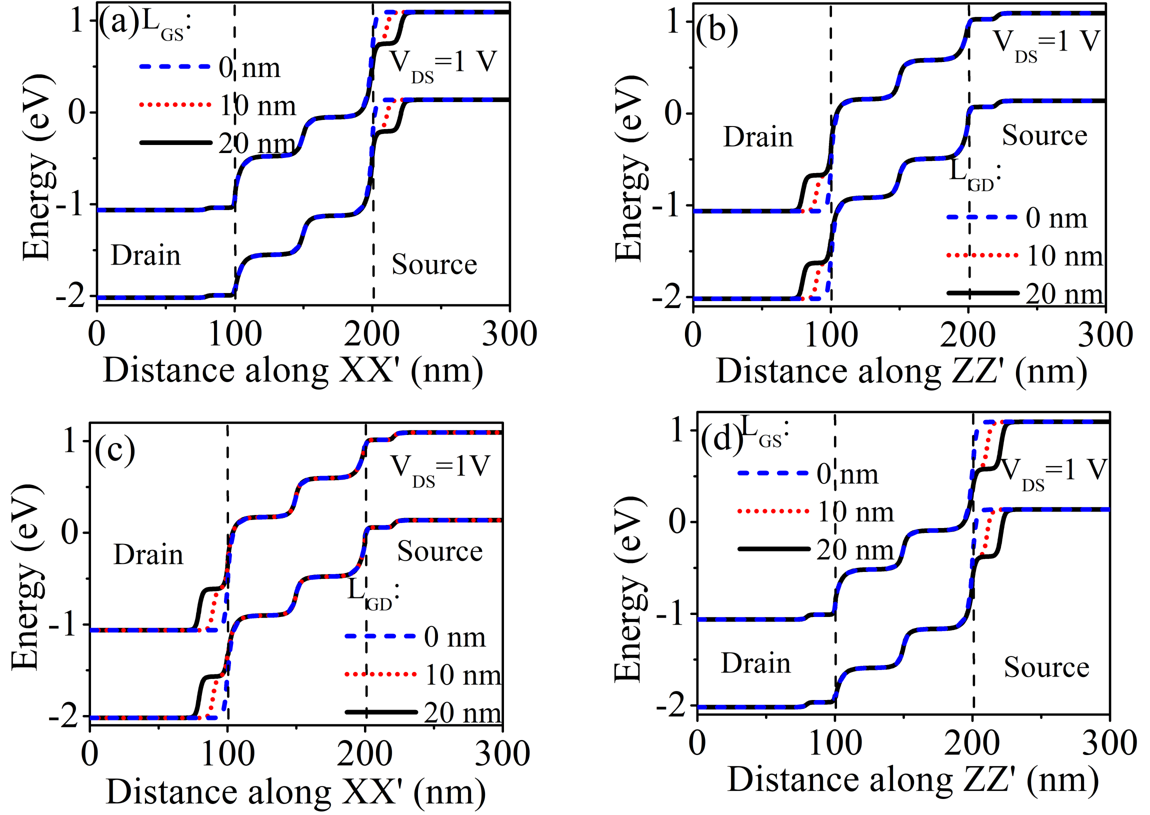


Figure 6.30: Band-diagram along X-axis for cutlines XX′ and ZZ′ at $V_{DS} = 1$ V when (a) Input combination is "10", gate–drain overlap $L_{GD} = L_{ov} = 20$ nm, and gate–source overlap ($L_{GS} = L_{ov}$) is varied from 0 to 20 nm, (b) Input combination is "10", gate–source overlap $L_{GS} = L_{ov} = 20$ nm, and gate–drain overlap ($L_{GD} = L_{ov}$) is varied from 0 to 20 nm, (c) Input combination is "01", gate–source overlap $L_{GS} = L_{ov} = 20$ nm, and gate–drain overlap ($L_{GD} = L_{ov}$) is varied from 0 to 20 nm, and (d) Input combination is "01", gate–drain overlap $L_{GD} = L_{ov} = 20$ nm, and gate–source overlap ($L_{GS} = L_{ov}$) is varied from 0 to 20 nm.

Fig. 6.30 illustrates how the addition of the overlap affects the band alignment of the device and inhibits the surface tunneling (along the cutline XX′ and ZZ′). When $L_{ov} = 0$, the tunneling barrier width is low at the drain–channel and the source–channel junctions, as shown in Fig. 6.30. Therefore, a high $I_{OFF} \approx 2 \times 10^{-7}$ A/μm flows through the device when $L_{ov} = 0$. As L_{ov} increases, the tunneling barrier width increases, and the I_{OFF} decreases, as shown in Fig. 6.30. Moreover, when L_{ov} is increased beyond 20 nm, there is no further increase in the tunneling barrier width, and thus, the drain current cannot be

decreased further. Therefore, $L_{ov} = 20$ nm is sufficient to minimize the current to $\approx 10^{-15}$ A/μm, when the input combination is either “01” or “10”.

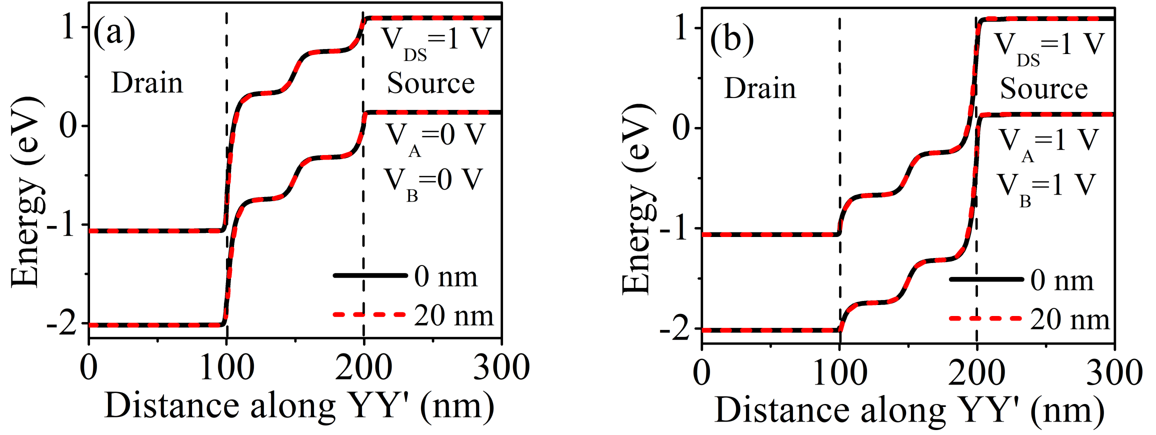


Figure 6.31: Energy band diagram along cutlines YY′ at $V_{DS} = 1$ V with and without gate–source overlap and gate–drain overlap, when (a) Input combination is “00”, (b) Input combination is “11”.

In a DM-DGTFET without overlap, for the input combinations “00” and “11”, in addition to the tunneling near the surface, the tunneling occurs in the middle of the device, i.e., along the cutline YY′ (as shown in Fig. 6.29(a) and 6.29(b)). Though gate overlap suppresses surface tunneling under all bias conditions, it does not switch-off tunneling in the middle of the silicon body (along cutline YY′), as shown in Fig. 6.31(a) and 6.31(b). Since appreciable tunneling occurs in “00” and “11” cases in the middle of the silicon body, a sufficient I_{ON} (current in “00” and “11” cases) is obtained in the device. However, in “00” and “11” cases, the current decreases by $0.6\times$ when the overlap is used compared to the no-overlap case. This decrease in current can be attributed to the inhibition of the surface tunneling component, as already explained.

The transfer characteristics of the DGTFET realizing the XNOR function

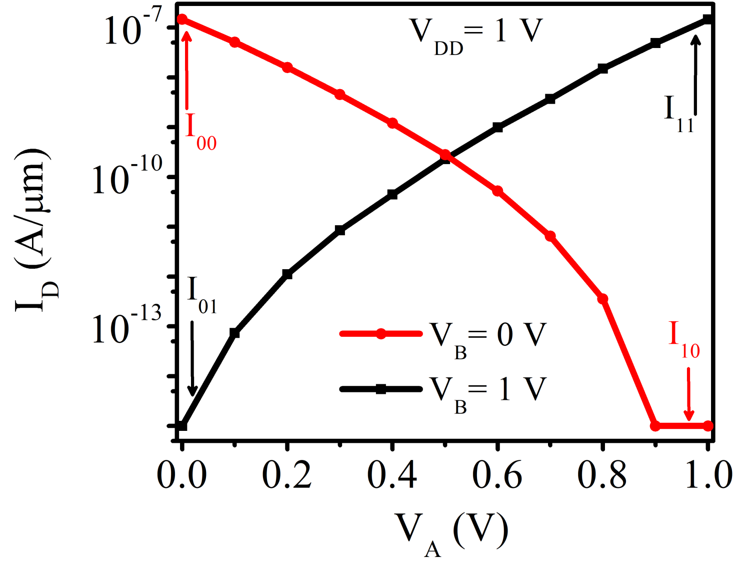


Figure 6.32: Transfer characteristics of DGTFET realizing XNOR logic function.

are shown in Fig. 6.32. The I_{ON}/I_{OFF} ratio for this implementation is $\sim 10^8$ at $V_{DD} = 1$ V.

6.6.1 Impact of Process-Induced Variations

For the proposed XNOR function, the gate–source and gate–drain overlaps can change due to process-induced variations. It is found that when the gate–source and gate–drain overlaps are changed by ± 5 nm, the I_{ON}/I_{OFF} ratio is not significantly impacted. Moreover, the functionality remains intact till $L_{ov} = 10$ nm with an I_{ON}/I_{OFF} ratio of 5×10^6. For $L_{ov} < 10$ nm, the I_{ON}/I_{OFF} ratio decreases sharply and the functionality is lost. Further, the impact of variation in silicon body thickness (t_{si}) on the I_{ON}/I_{OFF} ratio of the logic function is examined. Using simulations, it is found that when t_{si} increases by 2 nm, the I_{ON}/I_{OFF} ratio degrades from 1×10^8 to 1×10^7. Similarly, when t_{si} decreases by 2 nm, the I_{ON}/I_{OFF} ratio improves from 1×10^8 to 5×10^8.

6.6.2 Scaling Trend

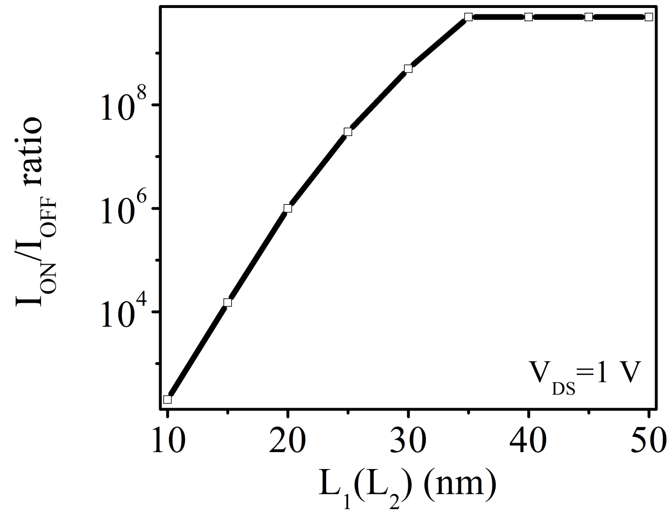


Figure 6.33: Effect of $L_1(L_2)$ on the I_{ON}/I_{OFF} ratio of the proposed DGTFET realizing XNOR function.

The trend of the I_{ON}/I_{OFF} ratio with respect to the change in the gate lengths L_1 and L_2 is examined, as shown in Fig. 6.33. It is noticed that the I_{ON}/I_{OFF} ratio remains unaffected for $L_1 = L_2 \geq 35$ nm, and then decreases. However, the functionality remains intact for $L_1 = L_2 = 20$ nm and the I_{ON}/I_{OFF} ratio decreases to $\sim 10^6$.

6.7 Realizing XOR Logic Function using DGTFET

The XOR logic function requires that BTBT occurs when the input combination is “01” or “10” and should be inhibited when the input combination is “00” or “11”. In all the above implementations, the tunneling in the “01” and “10” cases is inhibited using the gate–source or gate–drain overlaps. However, for the XOR function, the tunneling needs to be enhanced in the “01” and “10” cases.

This requirement is contradictory to the functions realized above. Therefore, the XOR function cannot be realized using earlier described techniques. It is proposed to realize the XOR function ($A \oplus B = A'B + AB'$) as the combination of inhibition functions $A'B$ and AB' [173, 174]. Therefore, XOR logic function realization requires two DGTFETs, where one DGTFET realize $A'B$ and the other DGTFET will realize AB'. Furthermore, these two DGTFETs can be combined into a single device, as illustrated in the following paragraphs.

6.7.1 Realizing inhibition functions using DGTFET

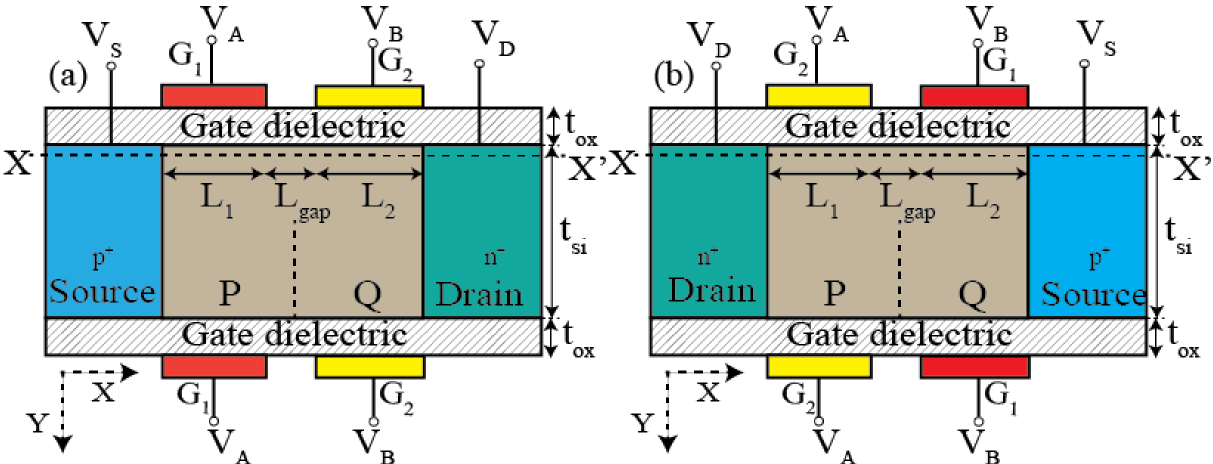


Figure 6.34: Cross-sectional view of a TDG-TFET that realizes inhibition function (a) $A'B$ (b) AB'.

Fig. 6.34(a) shows the cross-sectional view of the proposed device, realizing AB', in which there are two gates at the top called G_1 and G_2, separated by a gap L_{gap}. Similarly, two gates at the bottom correspond to the top gates G_1 and G_2. Thus, a twin double-gate (TDG) structure is formed. The proposed device is referred to as TDG-TFET in this work. The gates G_1 and G_2 are made up of different materials, with work-functions ϕ_1 and ϕ_2, respectively. The key

aspect of a TDG-TFET is that the twin gates are able to modulate the BTBT at their interfaces as per the required functionality. Thus, TDG-TFET exploits within-channel tunneling described in the previous chapter.

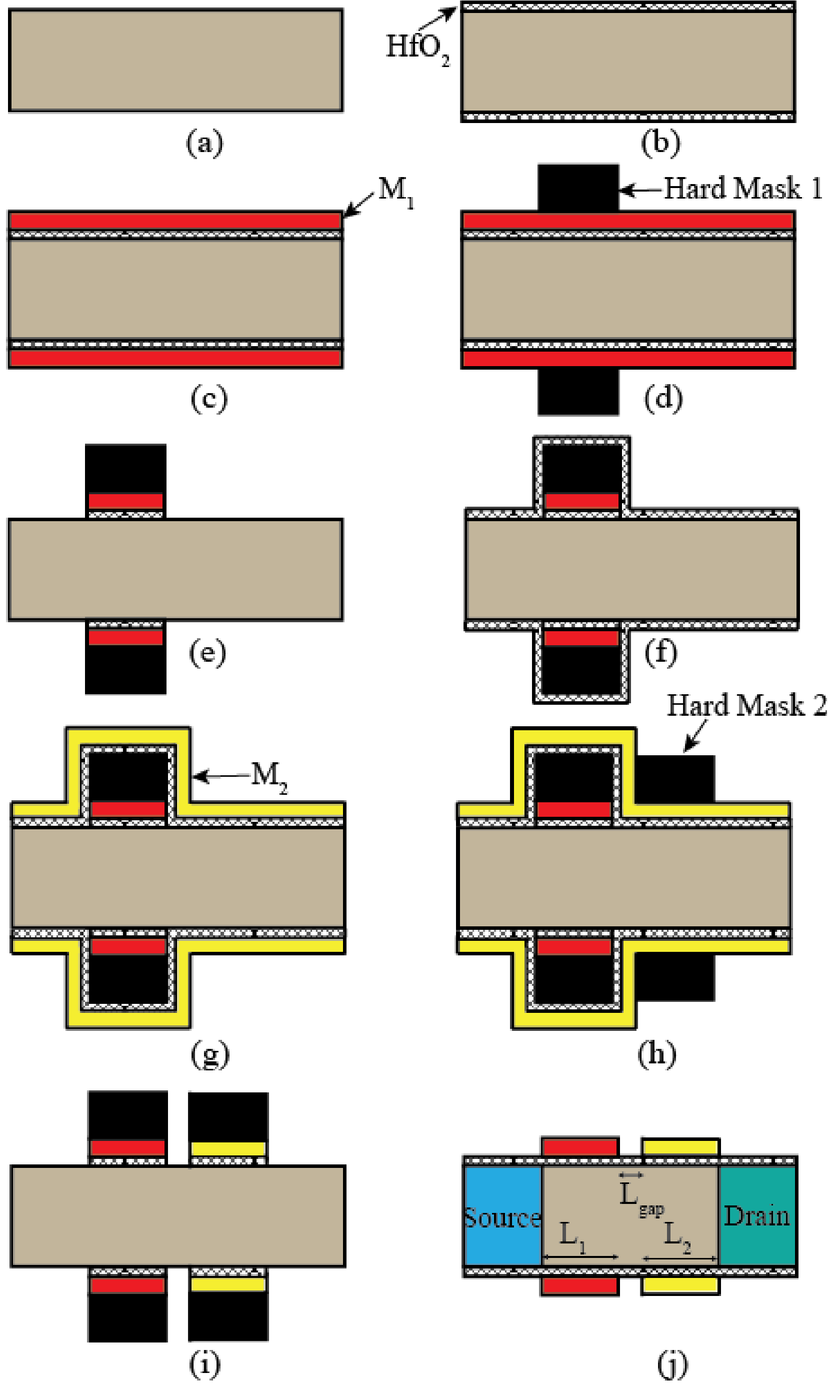


Figure 6.35: Proposed fabrication steps for the TDG-TFET structure.

The proposed device can be fabricated using various techniques. In literature,

some techniques have been suggested to fabricate DGTFETs and DMG structures [4, 46, 115, 126, 150–152, 154–156, 175]. Due to the structural similarity, the proposed devices can also be fabricated by adopting these techniques. A possible technique to fabricate the DMG structure is described in the proposed device in the following paragraph.

Fig. 6.35 illustrates the fabrication steps of the proposed device. The process starts with a $10\ \mathrm{nm}$ thick, lightly doped silicon wafer with doping $\mathrm{N_C} \approx 1 \times 10^{17}$ $\mathrm{atoms/cm^3}$, as shown in Fig. 6.35(a). Then, using atomic layer deposition (ALD) technique, a $2\ \mathrm{nm}$ thick HfO_2 layer is deposited on the silicon surface, as shown in Fig 6.35(b) [116,176,177]. This is followed by the deposition of a $3\ \mathrm{nm}$ thick metal layer $(\mathrm{M_1})$ with a work-function ϕ_1, using the e-beam deposition technique, as shown in Fig. 6.35(c) [125]. Then, a hard mask (a $4\ \mathrm{nm}$ thick Si layer) is deposited over the area where the $\mathrm{M_1/HfO_2}$ stack is to be retained, as shown in Fig. 6.35(d) [126]. The $\mathrm{M_1/HfO_2}$ stack is selectively etched from the remaining area, as shown in Fig. 6.35(e). Next, a $2\ \mathrm{nm}$ thick HfO_2 layer is deposited again followed by the deposition of $3\ \mathrm{nm}$ thick metal layer $(\mathrm{M_2})$ with work-function ϕ_2, as shown in Fig. 6.35(f) and 6.35(g), respectively. The deposition of a hard mask is done, as shown in Fig 6.35(h). The $\mathrm{M_2/HfO_2}$ stack is selectively etched from the unwanted areas resulting in a structure, as shown in Fig. 6.35(i). Finally, the hard masks are removed using warm acetone, and the source and the drain regions are formed using ion-implantation techniques [124]. The proposed DMG structure obtained is shown in Fig. 6.35(j). The additional gate–source and gate–drain overlap can be created using the tilt/oblique angle

technique for doping the overlapped regions [127, 146]. It is worth pointing out that the above fabrication steps are described to illustrate the feasibility of the proposed device. However, the challenges of fabricating the proposed device can be fully appreciated only when experiments on fabrication are done.

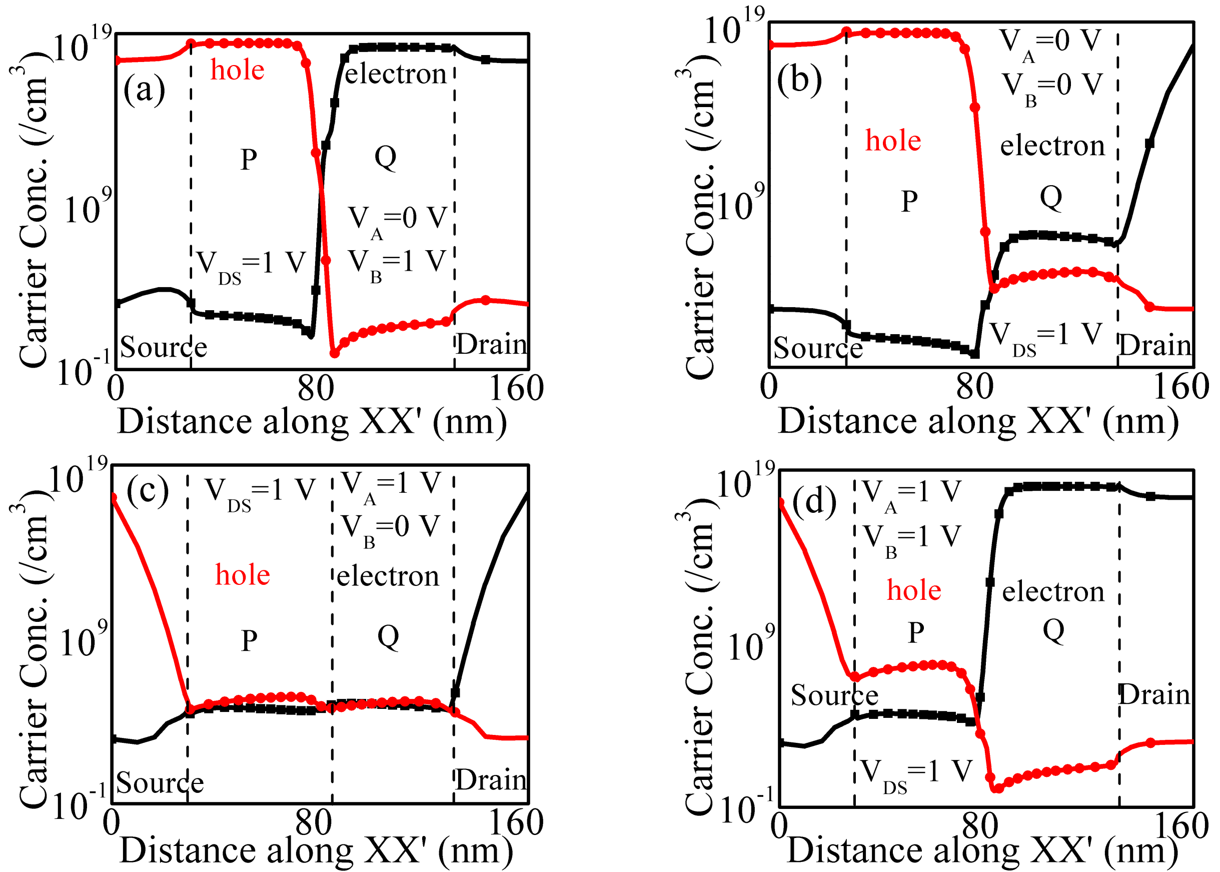


Figure 6.36: Carrier Concentrations of a DGTFET realizing “A′B” function, along X-axis at $V_{DS} = 1$ V for input combinations (a) “01”, (b) “00”, (c) “10” and (d) “11”.

Next, how A′B is realized by the TDG-TFET shown in Fig. 6.34(a) is described. For easier explanation, the channel is divided into two regions: P and Q. The work-function ϕ_1 is chosen, such that the region P becomes p-type (rich in holes) when $V_A = 0$ and is depleted when $V_A = V_{DD}$. Similarly, the work-function ϕ_2 is chosen, such that the region Q becomes n-type (rich in electrons) when $V_B = V_{DD}$ and is depleted when $V_B = 0$. The electron and the

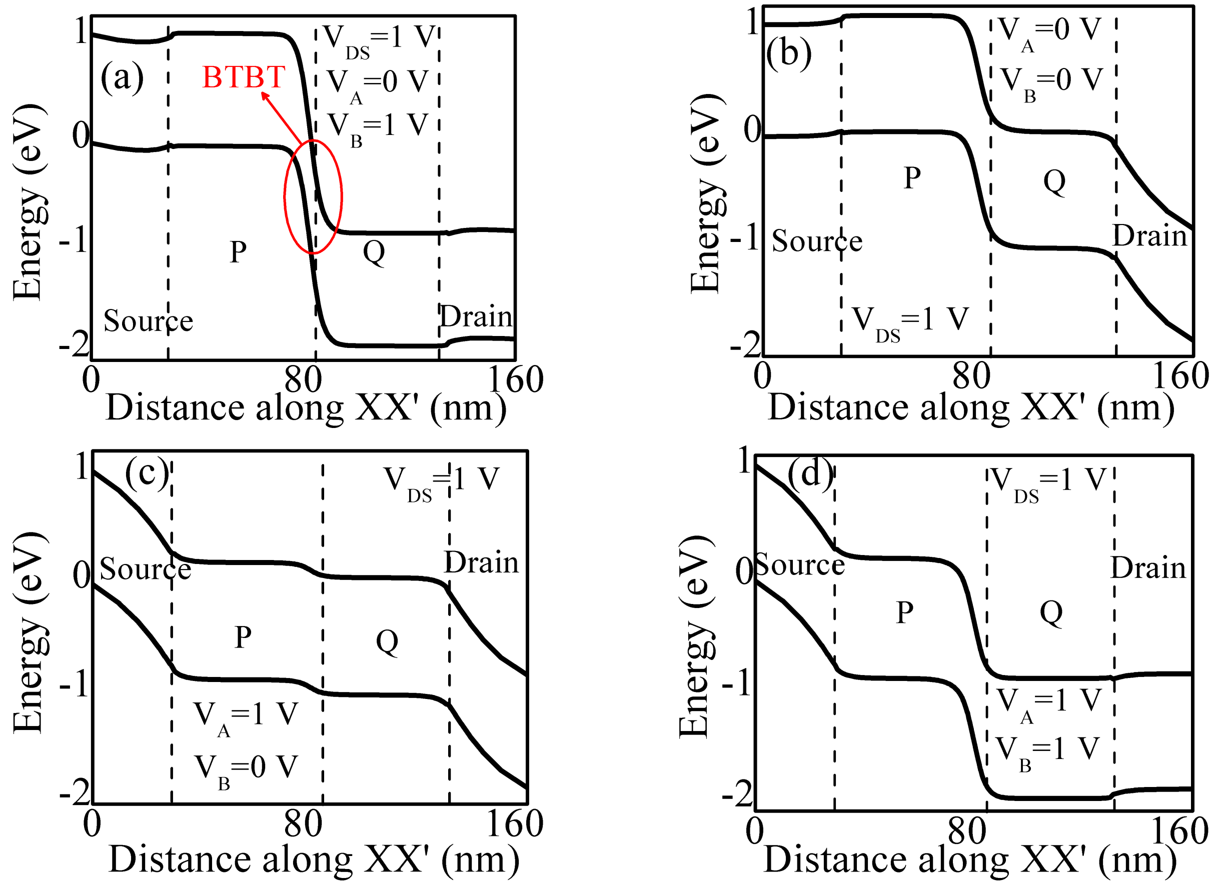


Figure 6.37: Energy band diagram of a DGTFET realizing "A′B" function, along X-axis at V_{DS} = 1 V for input combinations (a) "01", (b) "00", (c) "10" and (d) "11".

hole concentrations for different input combinations are shown in Fig. 6.36. For the input combination "01", the region P is rich in holes, and the region Q is rich in electrons, as shown in Fig. 6.36 (a). Therefore, the conduction and the valence bands get aligned, and the BTBT is enabled at the boundary of regions P and Q, as shown in Fig. 6.37 (a). For the other three input conditions, either region P or Q or both remain depleted, as shown in Fig. 6.36(b), 6.36(c), 6.36(d). Thus, BTBT is inhibited under the other three input conditions, as illustrated in Fig. 6.37(b)-(d).

The transfer characteristics of a TDG-TFET realizing A′B are shown in

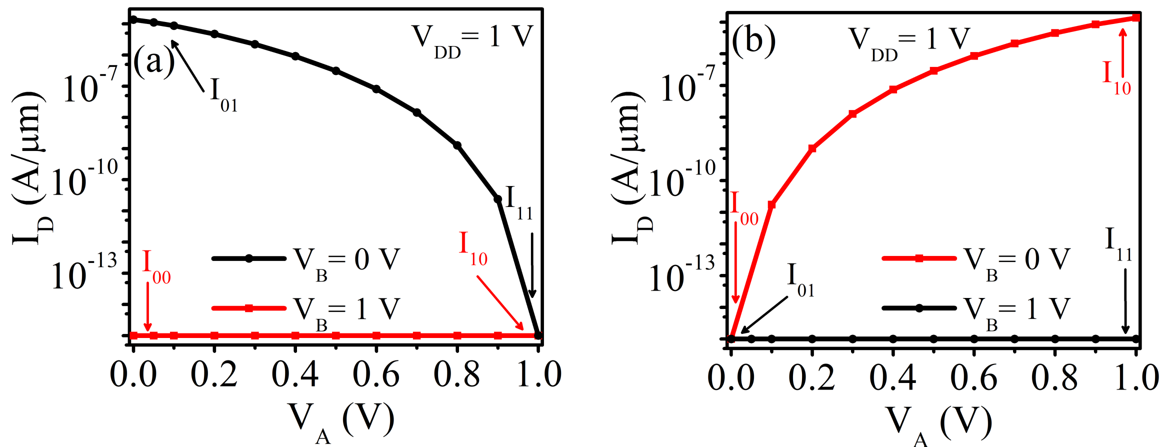


Figure 6.38: Transfer characteristics of a TDG-TFET realizing (a) $A'B$ (b) AB'.

Fig. 6.38(a). Further, the other inhibition function AB' can be realized just by interchanging the inputs at the gates G_1 and G_2, as shown in Fig. 6.34(b). The transfer characteristics of a TDG-TFET realizing AB' are shown in Fig. 6.38(b).

6.7.2 Realizing DGTFET-based XOR function using the inhibition functions

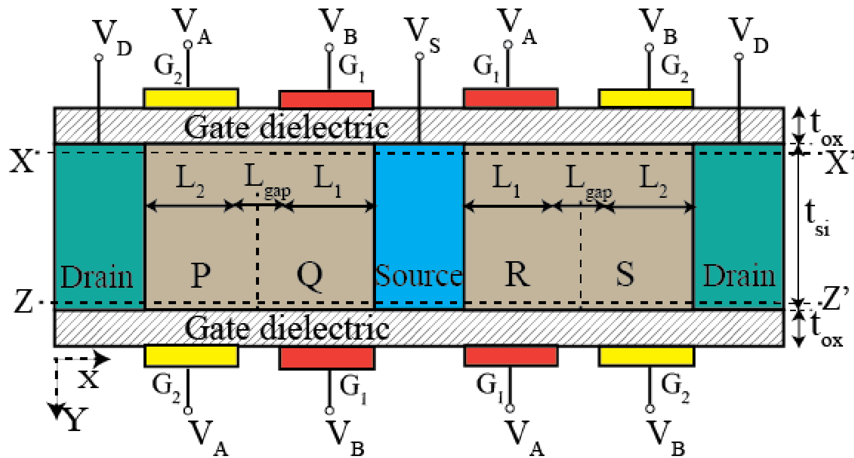


Figure 6.39: Cross-sectional view of TDG-TFET realizing XOR logic function.

Fig. 6.39 shows the implementation of an XOR function by combining TDG-TFETs that realize $A'B$ and AB'. In this implementation, two TDG-TFETs transistors are abutted such that the source can be shared. The source sharing is

possible in this case due to the symmetric TFET-XOR structure. This contrasts with the conventional implementation of TFET-based circuits in which electrode sharing is not feasible due to the asymmetric device structure. Thus, the proposed implementation of the XOR function is compact. The device parameters used in the simulations for the DGTFET-based XOR function are listed in Table. 6.2. It is important to note that the proposed XOR function implementation uses doping of $1 \times 10^{18}\ \mathrm{atoms/cm^3}$ for both the source and the drain. Therefore, the contact resistance can be high. However, low doping for the source and the drain is required to suppress BTBT at the source–channel and drain–channel junctions. This can be accomplished by keeping smaller doping only near the junctions as in lightly-doped drain, or pocket-based methods, described in Chapter-3 [33, 146]. The regions 'P', 'Q', 'R', and 'S' are defined in Fig. 6.39 for easy explanation. In this device, the tunneling occurs at the DMG interface rather than at the source–channel or drain–channel junctions. There are two tunneling interfaces in this device: the P–Q interface and the R–S interface. It is worth mentioning that regions rich in electrons and holes are created by electrostatics rather than chemical doping. The work-function ϕ_1 is chosen such that the region under the gate $\mathrm{G_1}$, i.e., 'Q' and 'R' becomes rich in holes, when $\mathrm{V_A} = 0$ and depleted when $\mathrm{V_A} = \mathrm{V_{DD}}$. Similarly, the work-function ϕ_2 is chosen such that the region under the gate $\mathrm{G_2}$, i.e., 'P' and 'S' becomes rich in electrons when $\mathrm{V_B} = \mathrm{V_{DD}}$ and depleted when $\mathrm{V_B} = 0$.

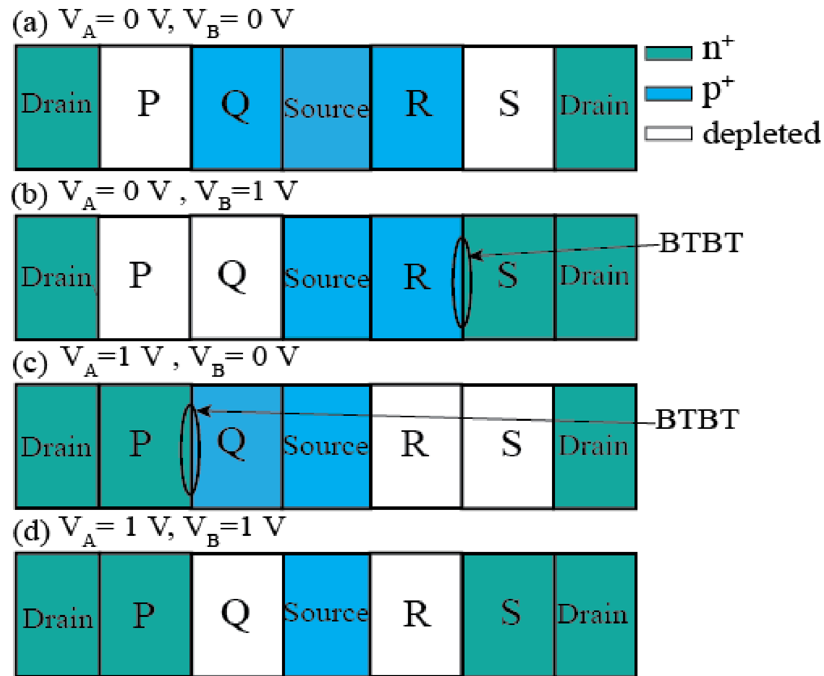


Figure 6.40: Illustration of the operating mechanism of a DGTFET-based XOR function.

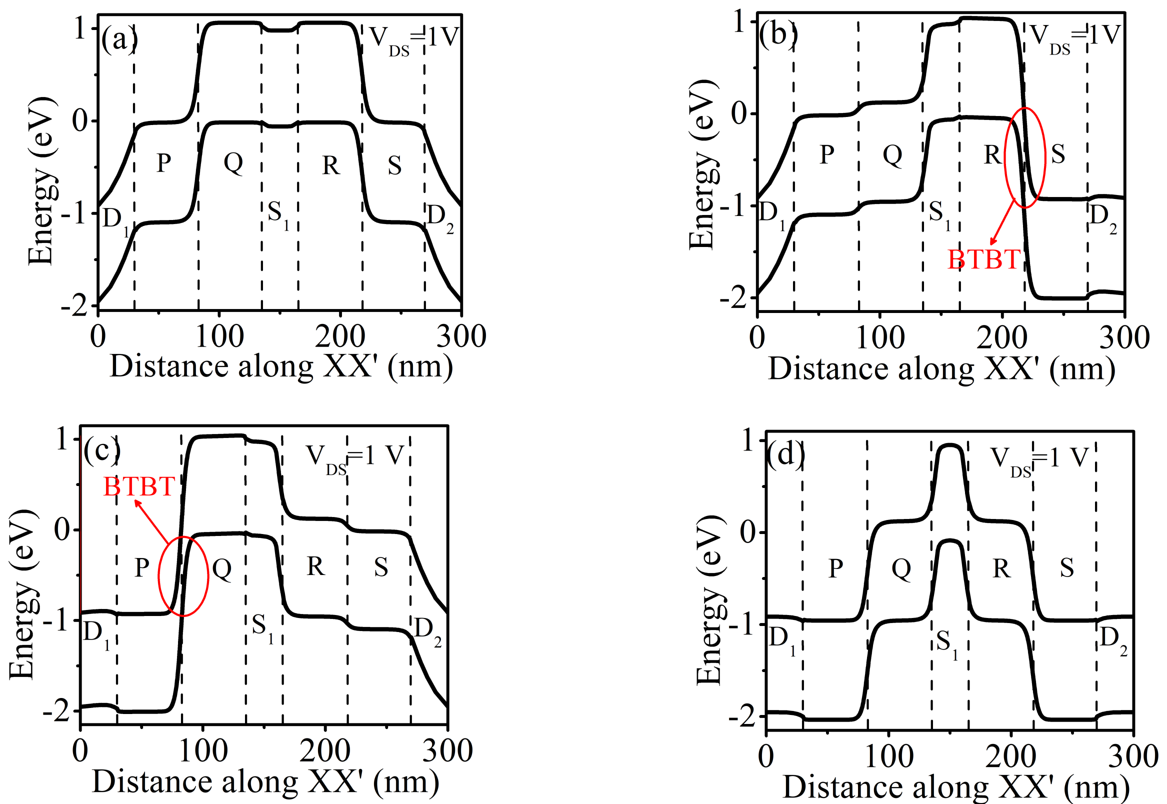


Figure 6.41: Energy band diagram of a DGTFET realizing XOR logic function, along X-axis at $V_{DS} = 1$ V, for input combinations (a) “00”, (b) “01”, (c) “10” and (d) “11”.

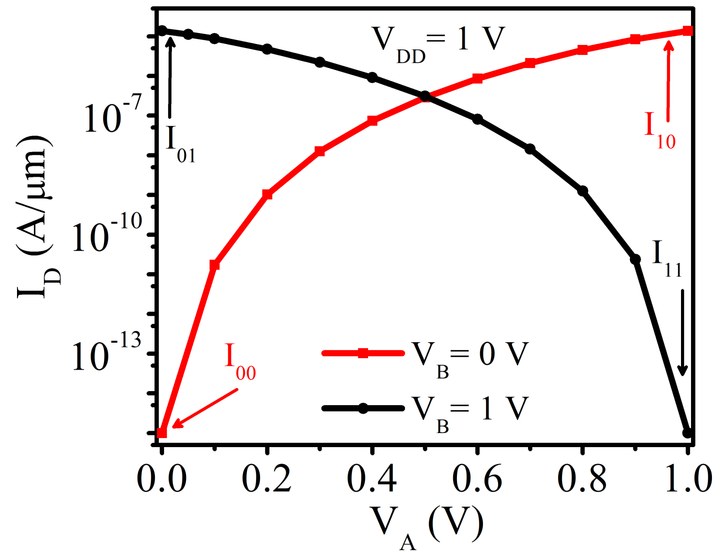


Figure 6.42: Transfer characteristics of DGTFET realizing XOR function.

Fig. 6.40 and Fig. 6.41, respectively, illustrate the electrostatic conditions of the various regions and the band diagrams along the length of the device for different input combinations. The drain1, source, and drain2 regions in Fig. 6.39 have been indicated as D_1, S_1, and D_2, respectively, in Fig. 6.41. For the input combination of "00", though the regions 'Q' and 'R' are rich in holes, the regions 'P' and 'S' are depleted, as shown in Fig. 6.40(a). Thus, the tunneling barrier width is high, and no current can flow through the device in this case, as illustrated in Fig. 6.41(a). For the input combination of "01", the regions 'P' and 'Q' are depleted, as shown in Fig. 6.40(b). Thus, the tunneling barrier width is high, and no tunneling occurs at the P–Q interface, as illustrated in Fig. 6.41(b). However, in this case, the region 'R' is rich in holes, and the region 'S' is rich in electrons, as shown in Fig. 6.40(b). Thus, a low tunneling barrier width exists at the R–S interface, as shown in Fig. 6.41(b), and a high tunneling current flows through the device. Similarly, for the input combination "10", the region 'P' is

rich in electrons, and the region ‘Q’ is rich in holes, as shown in Fig. 6.40(c). Thus, a low tunneling barrier width exists at the P–Q interface, as shown in Fig. 6.41(c), and a high tunneling current flows through the device. However, in this case, tunneling does not occur at the R–S interface due to higher tunneling barrier width, as shown in Fig. 6.41(c). This is due to the depleted ‘R’ and ‘S’ regions in the device, as shown in Fig. 6.40(c). Lastly, for the input combination of “11”, though the regions ‘P’ and ‘S’ are rich in electrons, the regions ‘R’ and ‘Q’ are depleted of carriers, as shown in Fig. 6.40(d). Consequently, a high tunneling barrier width exists at both the interfaces, as shown in Fig. 6.41(d). Therefore, no current flows through the device for this input combination. The transfer characteristics of the proposed XOR function are shown in Fig. 6.42. The $\mathrm{I_{ON}/I_{OFF}}$ ratio is observed to be $\sim 10^{10}$ at $\mathrm{V_{DD}} = 1$ V.

6.7.2.1 Impact of $\mathrm{L_{gap}}$

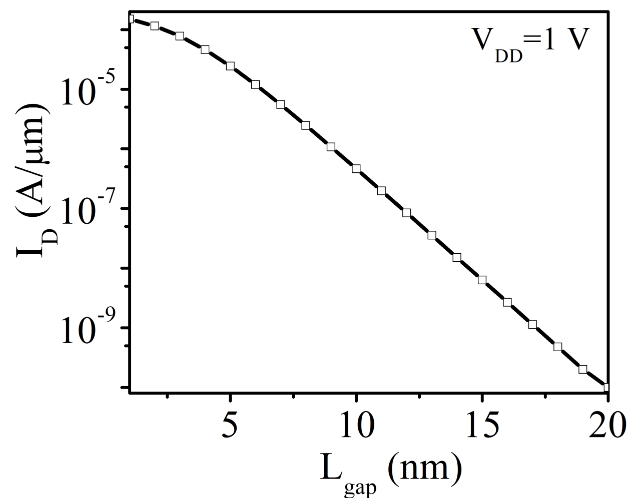


Figure 6.43: $\mathrm{I_{ON}}$ corresponding to different $\mathrm{L_{gap}}$ values obtained in DGTFET realizing XOR function.

In the proposed device, the tunneling current is dependent on the $\mathrm{L_{gap}}$, which

is defined as the gap between the gates electrodes G_1 and G_2. As the L_{gap} increases, the channel region within the gap remains close to intrinsic, and the sharpness of the band profiles at the tunneling junctions P–Q and R–S decreases. Therefore, the tunneling barrier width at the tunneling interfaces P–Q and R–S increases, resulting in a decrease in the I_{ON}, as illustrated in Fig 6.43. Therefore, a lower L_{gap} is preferable in the proposed device. The $L_{gap} = 5\ \mathrm{nm}$ is chosen in this work, similar to other published works [57, 110]. Further, it is important to note that the process-induced variations can change the gap L_{gap} between the gate electrodes G_1 and G_2 in the device. When the L_{gap} increases to 10 nm, the I_{ON} reduces from 1.2×10^{-5} to 5×10^{-7}.

6.7.2.2 Scalability trend

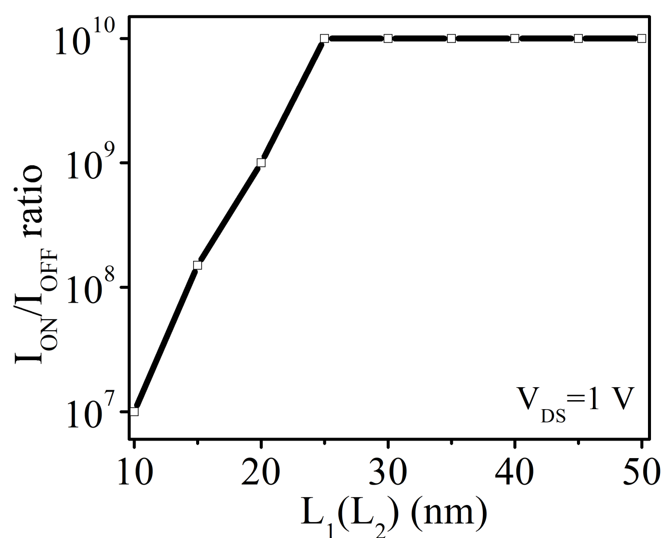


Figure 6.44: Trend of I_{ON}/I_{OFF} ratio for different L_1 (L_2) values obtained in DGTFET realizing XOR function.

The trend of the I_{ON}/I_{OFF} ratio with respect to the change in the gate lengths L_1 and L_2 is examined, as shown in Fig. 6.44. It is noticed that the I_{ON}/I_{OFF}

ratio remains unaffected for $\mathrm{L_1 = L_2 \geq 25\ nm}$, and then decreases. However, the functionality remains intact for $\mathrm{L_G \geq 20\ nm}$ i.e., $\mathrm{L_1 = L_2 = 10\ nm}$ (where $\mathrm{L_G = L_1 + L_2}$) and the $\mathrm{I_{ON}/I_{OFF}}$ ratio decreases to 10^7.

6.8 Implementing Logic Gates

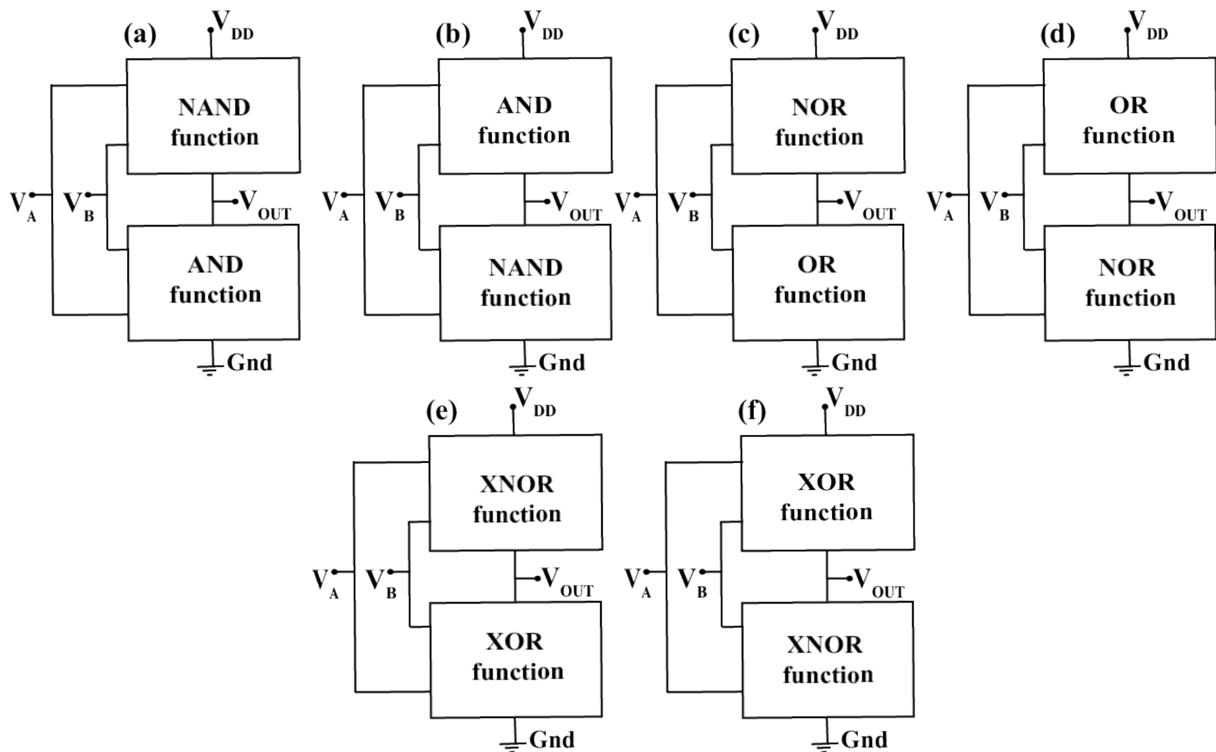


Figure 6.45: Schematic of DGTFET-based (a) NAND gate (b) AND gate (c) NOR gate (d) OR gate (e) XNOR gate (f) XOR gate.

Using the logic function implementations proposed in the previous sections, CMOS-type two-input logic gates can be implemented compactly. It can be noted that the six logic functions proposed in the previous sections form three complementary pairs: AND-NAND, OR-NOR, and XOR-XNOR. These complementary logic functions can be used in the pull-up and pull-down configuration to realize CMOS-type two-input logic gates, as shown in Fig. 6.45. For instance,

when the pull-up configuration is the NAND function, and the pull-down configuration is the AND function, the circuit works as a CMOS-type NAND gate, as shown in Fig. 6.45(a).

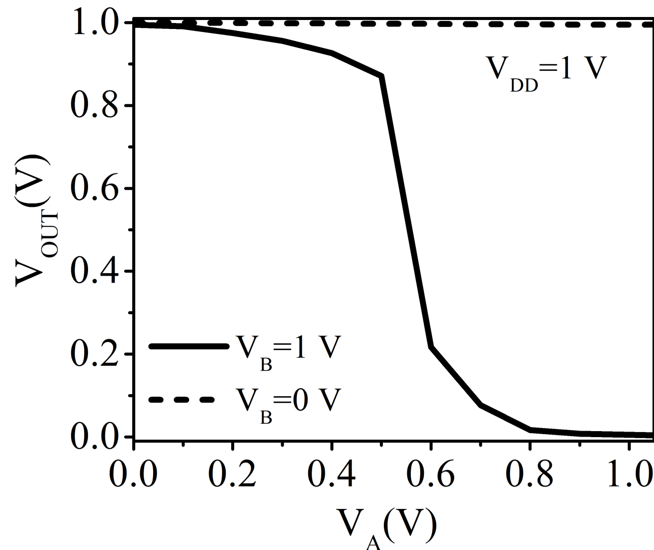


Figure 6.46: Static characteristics of DGTFET realizing NAND gate.

When either of the two inputs is at logic '0', then current flows through the NAND device (a low resistance path exists between $\mathrm{V_{DD}}$ and the output node), and the output is pulled up to logic '1'. However, when both the inputs are at logic '1', the current flows through the AND device (a low resistance path exists between Gnd and the output node), and the output is pulled down to logic '0'. Note that due to the complementary functionality, when the pull-up transistor is switched-on, then the pull-down transistor is switched-off, and vice-versa. Thus, the outputs of the proposed two-input gates are always connected to $\mathrm{V_{DD}}$ or Gnd through a low resistance path, similar to CMOS logic gates. It is worth mentioning that a conventional CMOS realization of a NAND gate requires four transistors, while the proposed gate requires two transistors. The static

characteristics of the NAND gate are shown in Fig. 6.46.

Similarly, AND gate can be realized just by swapping the pull-up and pull-down transistors of the NAND gate, as shown in Fig. 6.45(b). Similarly, other two-input logic gates can be obtained using these logic function implementations. These implementations employ fewer transistors than the conventional CMOS implementation of logic gates. Therefore, the proposed implementations are more compact and are expected to result in area/capacitance savings of around 2$\times$ due to halved transistor count compared to conventional CMOS implementations [178].

Table 6.4: Performance metrics of the DGTFET-based logic functions

Function	$\mathbf{V_{DD}}$ **(V)**	$\mathbf{I_{ON}}$ $\mathbf{(A/\mu m)}$	$\mathbf{I_{ON}/I_{OFF}}$	$\mathbf{C_{GG}}$ $\mathbf{(fF/\mu m^2)}$	**Delay (ns)**
OR	1	1.1×10^{-5}	10^{10}	1.65	0.2
NAND	1	9.8×10^{-6}	10^{10}	0.7	0.33
AND	1	8.2×10^{-8}	10^{8}	1.7	47
NOR	1	2.6×10^{-7}	10^{8}	1.76	14
XNOR	1	1.1×10^{-7}	10^{8}	2.3	60
XOR	1	1.35×10^{-5}	10^{10}	0.35	0.18

The performance metrics of the proposed implementations are listed in Table. 6.4. The effective drive current method proposed in [179] has been used to estimate the delay of these implementations. According to this method, the delay (τ_D) can be defined as follows:

$$\tau_D = \frac{C_{GG} \times V_{DD}}{I_{eff}} \tag{6.1}$$

where C_{GG} is the total gate capacitance of the device and I_{eff} is the effective

drive current. The effective drive current can be computed as follows [179]:

$$I_{eff} = \frac{(I_H + I_L)}{2} \tag{6.2}$$

where $\mathrm{I_H}$ is the drain current when $\mathrm{V_{DS}} = \mathrm{V_{DD}}/2$ and $\mathrm{V_{GS}} = \mathrm{V_{DD}}$, and $\mathrm{I_L}$ is the drain current when $\mathrm{V_{DS}} = \mathrm{V_{DD}}$ and $\mathrm{V_{GS}} = \mathrm{V_{DD}}/2$.

However, to accurately compute and compare the performance of the proposed implementation with the CMOS-based implementations, more rigorous analysis based on transient simulations is required. It should be noted that due to the limitations of the tool, the transient analysis using device-circuit co-simulations is not performed. The delays of the proposed implementations are presented in Table. 6.4 are very high compared to the state-of-the-art CMOS logic gates. This is expected since the above implementations are obtained using Si-based TFETs and it is well known that Si-based TFET circuits exhibit higher delay due to low $\mathrm{I_{ON}}$ and high $\mathrm{C_{GD}}$ [19, 58, 122]. Further, it is worth mentioning that due to large Miller capacitance ($\mathrm{C_{GD}}$), TFETs tend to have reduced bandwidth in comparison to MOSFET [24]. Thus, TFETs can be best employed in low power applications in a moderate frequency range [24, 180]. Nevertheless, it is important to mention that it is not claimed that the proposed realizations can outperform the state-of-the-art CMOS logic gates in terms of performance. However, in the future, the techniques demonstrated in this work can be adapted to TFETs that exhibit higher $\mathrm{I_{ON}}$ and compete with CMOS.

It is worth pointing out that in this work, only two-input logic gates are

considered. However, for practical applications implementing logic functions of more input variables are necessary. Using the devices proposed in this work, stacked and cascaded implementations of logic functions are possible.

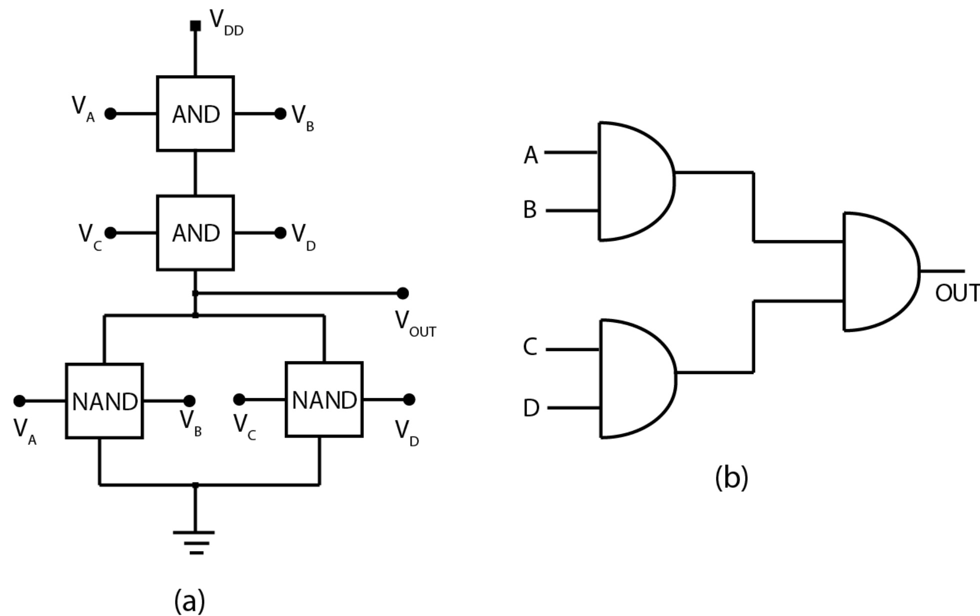


Figure 6.47: Four-input AND gate (a) stacked implementation (b) cascaded implementation.

Fig. 6.47(a) illustrates how a four-input AND gate can be implemented by stacking four transistors. Though the above implementation is functionally correct, there are several challenges in the stacked implementation. For a large number of inputs, the delay will significantly increase due to the resistances of the series transistors, the capacitance of the internal nodes, increased input capacitance, and self-loading effects. In TFET implementations, the impact of increased C_{GD} including Miller effects and low I_{ON} needs to be considered [122, 181]. Fig. 6.47(b) illustrates how a four-input AND gate can be implemented by cascading two-input AND gates. This implementation will require six transistors (two transistors for each AND gate), which is still less than the traditional CMOS implementation that requires ten transistors. Though

the proposed implementations consume fewer transistors, there are several non-trivial challenges in these implementations. It can be observed from Tab. III that the transistors providing complementary functions are not fully balanced. This can result in noise margin reduction, asymmetric rise/fall delays, output logic levels degradation, and increased power consumption in the subsequent logic gates [182]. Balancing the complementary devices is challenging due to the dependence of SS on the V_{GS} [181]. It can incur additional area, increase input capacitance and impact the delay of the preceding gate. Additionally, when TFETs are cascaded, high settling time, output voltage degradation, and susceptibility to cross-talk become important due to super-linear onset of saturation in the output characteristics, ambipolar conduction, dominant C_{GD} and high ON-state resistance [24, 122, 136]. These problems need to be addressed in the proposed implementations also.

6.9 Summary

In this chapter, the unique characteristics of TFET, such as ambipolar conduction and dependency of BTBT on the gate–source/drain overlaps, are exploited to realize logic functions compactly. It is worth pointing out that typically TFETs are made similar to MOSFETs by suppressing the I_{AMB} for digital applications. However, in this work, it is shown that distinct electrical characteristics of TFETs can be exploited, and certain differences with MOSFETs can be tolerated for useful applications. Though the low I_{ON} of TFETs remains a primary concern for researchers, novel circuit applications are possible using TFETs.

Chapter 7

Conclusion

7.1 Summary

In this work, different TFET structures have been proposed and analyzed. It is shown that the proposed structures can ameliorate some of the problems that are present in a TFET. Significant results include: (i) suppression of the ambipolar conduction using drain-pocket and other techniques in TFETs, (ii) extending the scalability of TFETs to $10\ \mathrm{nm}$ using the ground plane, (iii) improvement in short-channel performance such as drain-induced barrier lowering and threshold voltage roll-off using the ground plane and within-channel tunneling, (iv) reduced impact of source doping variations and reduced drain threshold voltage in DMG-DGTFET.

Additionally, an alternative approach of utilizing TFETs in digital circuits is explored. The unique properties of TFETs such as ambipolar conduction, the impact of the gate–source overlap, symmetric operation, and modulation of current within the channel are utilized to realize all two-input logic functions

using a single device. Larger logic functions and logic gates are implemented using TFETs more compactly compared to conventional CMOS. For example, a four-input AND gate is shown to be implemented using just four TFETs, while traditional CMOS implementation requires ten transistors. The results present in this work provide an incentive to further explore TFETs and their applications in digital circuits.

7.2 Future work

In this work, experiments have been carried out using a two-dimensional device simulator, and reasonable device parameters have been chosen for all the devices. Nevertheless, more accurate simulations considering the impact of quantum confinement effects, trap-assisted tunneling, non-abrupt source doping profiles, and effects such as leakage through gate oxide can be undertaken in the future work. These simulations can provide further insights into the devices. Further, the compact modeling of the proposed devices for DC and AC simulations for a TFET will be an important area to work on in the future. These models are important for efficient circuit simulations. Moreover, studying and modeling different noise sources present in the proposed TFETs can be an important area of research.

Fabrication-driven experiments on the proposed devices would be the next natural step. In this work, the focus is on the silicon-based material system. Silicon has been considered in this work since it is easier to fabricate silicon-based

devices due to already available matured Si-based IC fabrication technology. Though exploring the proposed techniques on other material systems such as germanium, III-V materials, 2-D materials, etc., can show more interesting improvements. Further, the combination of MOSFET and TFET can be exploited in obtaining better-performing circuits [13]. This is possible due to the compatibility of TFET with MOSFET in terms of fabrication, making it easier to deploy the TFET in the existing MOSFET-based fabrication flow. In this work, DGTFET has been primarily used. The proposed techniques can also be studied on advanced architectures such as gate-all-around structures, nanowires, and nanotubes.

The logic functions realized in this work are compact in terms of the number of transistors. They are combined in a complementary manner to realize logic gates that exhibit good static characteristics. However, an in-depth transient analysis of these logic gates needs to be done. Further, the application of these logic gates in some complex digital circuits such as adder, subtractor, flip-flops, etc., can be explored [183]. This can be helpful in examining the impact of this work in designing a bigger system.

Besides digital circuit applications, the utility of TFETs in analog and RF circuits can be explored. TFET can outperform MOSFET in terms of transconductance and intrinsic voltage gain due to their excellent output saturation [183]. Further, their large Miller capacitance (C_{GD}) makes them suitable for low power applications in a moderate frequency range [24, 180]. The larger I_{ON} to I_{OFF} ratio in TFETs can be useful in designing analog memories such as DRAM [143].

Due to their unique characteristics, TFETs can be employed in biasing circuits, digital to analog and analog to digital converters, sensors, etc. [4, 120, 184–186]. Moreover, some properties of TFET, which are different from MOSFETs, such as negative differential resistance (NDR) and unidirectional current conduction, can be explored in designing novel circuit architectures [19, 92, 143, 184, 187].

Since the behaviour of TFET is quite different from the conventional MOSFET, the application of TFET-based logic gates in complex circuits can pose newer challenges for circuit designers. Therefore, more experiments, including fabrication-driven, need to be carried out on complex digital circuits and systems.

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APPENDIX-A: SAMPLE ATLAS INPUT FILE USED IN THE SIMULATION OF DGTFET

```
# Input file for device simulation tool ATLAS
go atlas


# Defining meshes for the device.
mesh space.mult=1.0 width=1
x.mesh loc=0.000 spac=0.01
x.mesh loc=0.050 spac=0.005
x.mesh loc=0.075 spac=0.001
x.mesh loc=0.095 spac=0.0005
x.mesh loc=0.105 spac=0.0005
x.mesh loc=0.125 spac=0.0005
x.mesh loc=0.150 spac=0.001
x.mesh loc=0.175 spac=0.0005
```

x.mesh loc=0.195 spac=0.0005

x.mesh loc=0.205 spac=0.0005

x.mesh loc=0.225 spac=0.001

x.mesh loc=0.250 spac=0.005

x.mesh loc=0.300 spac=0.01

y.mesh loc=-0.002 spac=0.001

y.mesh loc=0.000 spac=0.0005

y.mesh loc=0.010 spac=0.0005

y.mesh loc=0.012 spac=0.001

Defining another mesh for non-local BTBT modelling in ATLAS

qtx.mesh loc=0.075 spac=0.0005

qtx.mesh loc=0.225 spac=0.0005

qty.mesh loc=0.000 spac=0.0005

qty.mesh loc=0.010 spac=0.0005

Defining regions in the device

region num=1 y.max=0.000 material=Oxide

region num=2 y.min=0.000 y.max=0.010 material=Silicon

region num=3 y.min=0.010 material=Oxide

Defining electrodes

```
electrode name=gate x.min=0.100 x.max=0.200 top
electrode name=drain x.min=0.000 x.max=0.000 y.min=0.000 y.max=0.010
electrode name=source x.min=0.300 x.max=0.300 y.min=0.000 y.max=0.010
electrode name=gate2 x.min=0.100 x.max=0.200 bottom

# Defining the tunneling parameter for silicon:
material material=Silicon me.tunnel=0.14 mh.tunnel=0.14 region=2

# Defining doping
doping uniform p.type conc=1e17 reg=2
doping uniform n.type conc=1e20 x.max=0.100 reg=2
doping uniform p.type conc=1e20 x.min=0.200 reg=2

# Defining contacts
contact name=gate workfunction=4.5
contact name=gate2 workfunction=4.5 common=gate
save outf=init_ndgtfet.str

# Defining physical models
models bbt.nonlocal qtunn.dir=1 bgn fermi consrh conmob print

# Applying bias for simulation
```

```
method newton
solve init
solve vsource=0.0
solve vgate=0.0
solve vdrain=0.0 vstep=0.05 name=drain vfinal=1.0

# Simulating the transfer characteristics
save outf=off_ndgtfet.str
log outf=xfer_ndgtfet.log master
solve vgate=0.0 vstep=0.1 name=gate vfinal=1.0
save outf=on_ndgtfet.str
tonyplot xfer_ndgtfet.log
quit
```

Publications

Related to this Work:

1. **S. Garg** and S. Saurabh, "Suppression of ambipolar current in tunnel FETs using drain-pocket: Proposal and analysis," *Superlattices and Microstructures*, vol. 113, pp. 261-270, Jan 2018.

2. S. Banerjee, **S. Garg** and S. Saurabh, "Realizing Logic Functions Using Single Double-Gate Tunnel FETs: A Simulation Study," *IEEE Electron Device Letters*, vol. 39, no. 5, pp. 773-776, May 2018.

3. **S. Garg** and S. Saurabh, "Improving Scalability of SOI-based Tunnel FETs using Ground Plane in Buried Oxide," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 435-443, April 2019.

4. **S. Garg** and S. Saurabh, "Implementing Logic Functions using Independent Gate Control in Double Gate Tunnel FETs: Investigation and Analysis," *IEEE Access*, vol. 7, pp. 117591-117599, Aug 2019.

5. **S. Garg** and S. Saurabh,"Realizing XOR and XNOR Functions Using Tunnel Field-Effect Transistors," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 1001-1009, Sep 2020.

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7. **S. Garg** and S. Saurabh, "Implementation of Boolean Functions Using Tunnel Field-Effect Transistors," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 6, no. 2, pp. 146-154, Nov 2020.

Other Related Works:

1. S. Saurabh, S. K. Semwal, **S. Garg** and A. Gupta, "Emerging devices beyond CMOS: fundamentals, promises and challenges" in *VLSI and Post-CMOS Electronics, Volume 1: Design, modelling and simulation*, IET Digital Library, 2019, pp. 161-186.
2. S. Poria, **S. Garg** and S. Saurabh, "Suppression of Ambipolar current in Tunnel Field-Effect Transistor using Field-Plate," in *2020 24th International Symposium on VLSI Design and Test (VDAT)*, 2020, pp. 1-6.

Brief Bio data of the Author

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