An Energy-Efficient Hybrid DAC based SAR ADC using Deep-submicron CMOS and Large-Area Oxide TFT Technologies

A Thesis

submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

By

Bhawna Tiwari

Under the supervision of

Dr. Pydi Ganga Mamba Bahubalindruni (Advisor),

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New Delhi– 110020

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Dedicated to my beloved parents and sister...

Certificate

This is to certify that the thesis titled "***An Energy-Efficient Hybrid DAC based SAR ADC using Deep-submicron CMOS and Large-Area Oxide TFT Technologies***" being submitted by Bhawna Tiwari to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of Doctor of Philosophy, is an original research work carried out by her under our supervision. In our opinion, the thesis has reached the standard fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree or diploma.

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Declaration

This is certified that the thesis entitled "***An Energy-Efficient Hybrid DAC based SAR ADC using Deep-submicron CMOS and Large-Area Oxide TFT Technologies***" being submitted by me to the Indraprastha Institute of Information Technology Delhi, for the award of degree of **Doctor of Philosophy**, is a bonafide work carried out by me. This research work has been carried out under the supervision of **Dr. Pydi Ganga Mamba Bahubalindruni (Advisor), Prof. João Goes (Co-Advisor), Prof. Pedro Barquinha (Co-Advisor) and Dr. Sujay Deb (Co-Advisor)**.

The study pertaining to this thesis has not been submitted in part or in full, to any other University or Institution for the award of any other degree.

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Bhawna Tiwari

Abstract

The successive approximation-register (SAR) analog-to-digital converters (ADCs) have excellent energy efficiency compared to other Nyquist-rate ADCs like Flash, Pipeline, etc. The simplest form of a SAR ADC employs track-and-hold (T/H) switches, a voltage comparator, a digital controller, and a capacitive digital-to-analog converter (DAC). Due to its simple architecture and highly digital and switching intensive behavior, its popularity has been boosted with technology down scaling. However, most of the designs reported in the literature employ binary-weighted capacitive DAC array, whose size increases exponentially with an increase in resolution of the ADC. This exponential increase degrades the conversion speed and energy efficiency of the SAR ADC.

One of the best methods to reduce the size of the binary-weighted capacitive DAC array with the increasing resolution is to use two (or more) small-sized sub-DACs to form the complete DAC of the ADC. Though capacitive-resistive hybrid DAC-based SAR ADCs have been reported in the literature, resistive DAC tradeoff between power consumption, active area, and operating speed, which compromise the performance and energy efficiency. On the other hand, limited number of SAR ADCs with capacitive sub-DACs have been reported, which demand calibration logic and additional digital controller circuitry. Charge-Sharing (CS) and Merged-Capacitor Switching (MCS) are the two extensively employed switching schemes in the SAR ADCs. While the CS switching principle works on a single array of binary-weighted capacitive DAC, MCS works on two arrays of binary-weighted capacitive DAC for the differential implementation SAR ADC. It should be noted that though CS DAC employs a single array of capacitive DAC, it requires explicit T/H capacitors to perform the conversion algorithm. In addition, this scheme requires a pre-charging phase, in which the capacitors of the DAC array are charged to the reference voltage. As a result, for moderate to high resolution ADCs, the DAC size will be significant, and it will require a large current from the reference buffer to charge the DAC capacitors in a short

duration of time.

This research work presents a new hybrid capacitive DAC design for SAR ADC, which employs two switching principles, namely CS and MCS, to improve the performance metrics of the SAR ADC. The proposed hybrid DAC is purely based on capacitors, and it is designed to work without any calibration logic and additional digital controllers. Moreover, the proposed hybrid DAC architecture presents a solution where the capacitors of the MCS DAC act as T/H capacitors for the CS scheme when the conversion is done using this scheme, thus, eliminating the explicit T/H capacitors. On the other hand, due to the deployment of two sub-DACs in the proposed hybrid DAC design, the size of the CS sub-DAC can be reduced significantly, which helps in pre-charging the DAC capacitors in a small duration of time without drawing large current from the reference buffers. As a result, the hybrid DAC design can significantly improve the operating speed and energy efficiency of the complete ADC architecture.

The proposed hybrid DAC based SAR ADC has been implemented in both deep-submicron CMOS and large-area oxide Thin-film transistor (TFT) technologies to show the design suitability for deep sub-micron and large-area semiconductor technologies. Since oxide TFT technology lacks stable and reproducible amorphous p-type transistors with reasonable performance, the complete ADC in this technology is designed using all enhancement n-type transistors with novel switches, comparator and shift register. The obtained results show FoM of the proposed SAR ADC to be 5fJ/c.s and 56nJ/c.s. in CMOS and oxide TFT technologies respectively, which are the best compared to the similar state of the art work reported in a particular technology to the best of authors knowledge. Since, the proposed CS-MCS hybrid DAC based SAR ADC design offers high energy efficiency, it finds wide applications in the field of wireless communication, biomedical, smart packaging and sensing systems.

Keywords-**Hybrid DAC based SAR ADC, Energy efficiency, Oxide TFTs, Charge-sharing, Merged-capacitor switching, Biomedical, wireless communication**

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List of Acronyms

ADC Analog-to-Digital Converter

CMOS Complementary Metal-Oxide Semiconductor

CB Clock Booster

CR Charge-Redistribution

CS Charge-Sharing

DAC Digital-to-Analog Converter

DNL Differential Non-Linearity

ENOB Effective number of bits

FOM Figure-of-Merit

FFT Fast Fourier transform

IC Integrated circuit

INL Integral Non-Linearity

LSB Least-significant-bit

MCS Merged-Capacitor Switching

MOS Metal-Oxide Semiconductor

MSB Most-significant-bit

NS Noise-shaping

PCM Pulse code modulation

RO Ring Oscillator

SAR Successive approximation-register

SFDR Spurious-free dynamic range

SNDR Signal to Noise and Distortion Ratio

TFT Thin-film transistor

VLSI Very Large Scale Integration

Chapter 1

Introduction

The single largest driving force behind the development of electronic data converters has been the field of wireless and wire-line communications [20]. Back in ancient times, the communication between remotely located individuals was a difficult task. The messages were taken from the sender's place to the recipient's location by a horse rider or pigeons. These old schemes took months in distributing essential letters to the destination, thus, jeopardizing their secure delivery. With the inventions of the telegraph (the 1840s) and pulse code modulation (PCM), long-distance communication was revolutionized. The messages were able to reach the destination with a delay of one day. Later, the inventions of the vacuum tube (1907), transistors (1947), and the integrated circuits (ICs) (1959) had contributed significantly to the advancement of the telecommunication systems, which assisted in the up-gradation of the long-distance communications. In the present era, the escalation of digital computing and signal processing in electronic systems permits messages to travel across the world in a fraction of a second. Thanks to the scaling properties of the Very Large Scale Integration (VLSI) process, billions of transistors can be laid out in a single IC, making the present digital circuits and processors compact, faster, and much more potent than those of their older generations.

The performance of the digital circuits is augmented with the advancement in IC technologies. Unlike analog circuits, digital circuits allow more accessible design and automation, and offer more extensive programmability. Moreover, they are less sensitive to the noise, robust against supply, and process variations than analog counterparts [21]. As a result, the world is becoming more digital every day [21]. However, our physical environment can obstruct the digital world's proliferation because the signals are naturally in analog form (continuous-

amplitude with continuous-time). Besides, humans can apprehend and perpetuate only analog information. Therefore, proper interfacing between the analog and digital domains is essential. Data converters (analog-to-digital converters (ADCs) and digital-to-analog converters (DACs)) are used to interface digital processors with the analog world. ADCs convert analog signals into digital language, which is used in computing, data transmission, etc. On the other hand, DACs are used in translating the data from digital processing back in the analog form. The three triads: power, speed, and resolution, dictate the performance of data converters. The specification of the system and the signal characteristic decide the resolution and speed ($i.e.$ conversion-rate) of the ADCs and DACs. The power dissipation of these converters should be minimized to save energy, particularly in battery-operated applications.

1.1 Energy-Efficient ADC

Almost all wireless and/ or portable devices and systems consume energy that is collected either from energy harvesters or batteries. Energy harvesters use energy from the environment like solar, vibrations, RF, etc. to provide optimal conditions for operation [22, 23] and, therefore, act as a viable solution for self-sustainable wireless system [24, 25]. However, these harvesters provide a limited amount of power to the circuits [26–28]. On the other hand, batteries have a finite capacity and lifetime, and therefore, require either frequent charging or replacement. Since ADC is an integral part of wireless systems, boosting its energy efficiency without affecting the other metrics is an active research problem. The energy efficiency of an ADC is quantified by figure-of-merit (FOM) given by Walden in 1999 [29], and it is defined in (1.1).

$$FOM_W = \frac{P}{2^{ENOB} f_s} \tag{1.1}$$

Here, P is the total power dissipated by the ADC, ENOB (effective number of bits) is the effective resolution of the ADC and f_s is the sampling frequency. In the past years, several architectures of the ADCs have been established based on the applications and requirements [1] as shown in Figure 1.1. It is observed from the previously published works [17] in CMOS technology that a trade-off exists between the triads: speed, power, and resolution of the ADC. This trade-off impacts the energy efficiency of the ADC (1.1). If the ADCs have a

high conversion speed, the architecture should have a high level of parallelism. The resolutions of such ADCs are limited by the complexity of the circuits, which increases exponentially with the resolution. These ADCs have low energy efficiency because many modules are operated simultaneously and drain more power for the same resolution. On the other hand, ADCs with high-resolution have low conversion speed and require large internal capacitance to assist in noise filtering, increasing the power dissipation [30]. It should be noted that power dissipation is a critical factor for wireless and wearable systems as only a limited amount of energy is available for driving the on-chip components.

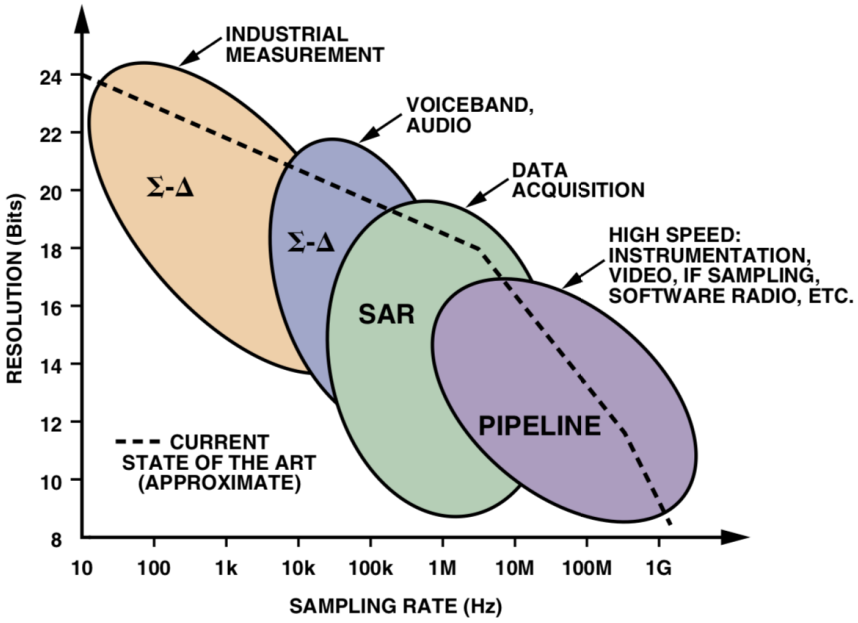

Figure 1.1: ADC architectures, applications, resolution, and sampling rates. [1].

Among other Nyquist rate ADCs, successive-approximation-register (SAR) ADCs present an outstanding energy efficiency when designed using modern technologies due to its scaling-friendly nature. Moreover, the lack of precision amplifiers and highly digital behavior of the ADC benefit directly from faster transistors, leading to a high switching speed at low technology nodes. The graphs in Figure 1.2 summarizes the SAR and other ADCs (flash, pipeline, delta-sigma, etc.) in terms of conversion efficiency, speed, and signal-to-noise-and-distortion ratio (SNDR). The conversion energy is defined as the ratio of P to f_s. The term SNDR, on the other hand, is used to quantify the output signal fidelity of the ADC [31]. The data presented in the figure is taken from the work that was published from 2015-2020 in the IEEE International Solid-State Circuits Conference (ISSCC) and IEEE Symposium on VLSI Circuits

(VLSIC) [17] in CMOS technology. In these graphs, the ADC architectures (like flash, pipeline, two-step flash etc.), which employ SAR ADC as the local quantizers, are presented using legend *SAR-assisted*. It is observed from the figure that the SAR and SAR-assisted ADCs provide the best energy efficiency compared to other ADCs for moderate resolution (8 to 10 bits) and moderate speed (tens of kilo-Samples/s to tens of Mega-Samples/s). As a result, these ADCs are the dominant and popular ADCs for the applications that demand moderate resolution and speed, which leads to the increasing interest of the scientific community in the design of these ADCs.

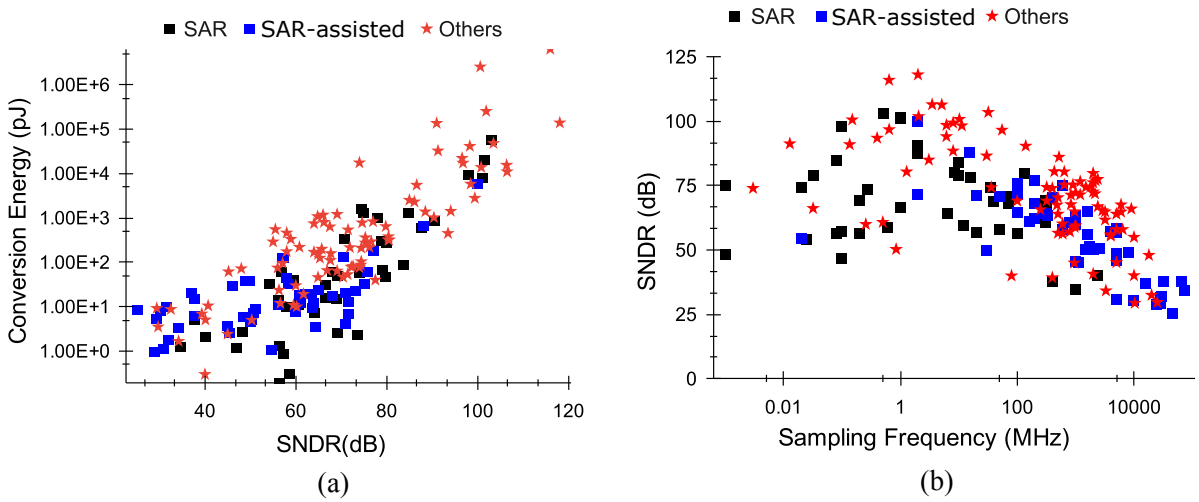

Figure 1.2: ADC performance data published in CICC [2–7], ISCAS [8–12], ESSCIRC [13–16], VLSIC and ISSCC from 2015 to 2020 [17] (a) Conversion Energy and (b) SNDR.

The graph presented in Figure 1.3 shows the number of published papers on ADCs since 1997 in ISSCC and VLSIC [17]. The figure shows that the number of SAR ADC publications has increased significantly after 2006. Before 2006, this number was negligible. The simple architecture of the SAR ADC and the advantage it delivers compared to the other ADCs, which is discussed above, are making SAR ADCs popular among the researchers and the best fit for the systems that demand moderate resolution at moderate conversion speed with high energy efficiency.

On the other hand, amorphous oxide thin-film transistor (TFT) technology has gained popularity since last ten years in the field of circuit design as this technology empowers low-cost flexible and transparent electronics due to its compatibility with low-temperature fabrication techniques [32–35]. As a result, this technology helps to implement intelligent flexible wearable electronic systems, which promotes conformability to the human body at low cost. The ma-

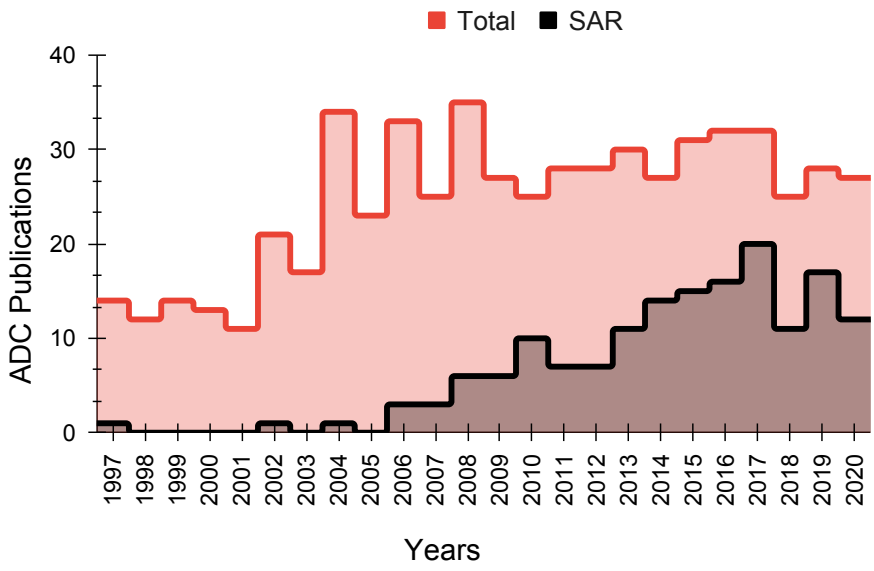

Figure 1.3: The ADCs published in CICC, ISCAS, ESSCIRC, VLSIC and ISSCC since 1997 [17].

terials exploited in these flexible devices are lightweight and fully conformable to human body, ensuring maximum user comfort. However, due to the large device parasitics and amorphous nature of the semiconductor, the technology is more suitable for low frequency application like temperature sensing systems [36], biomedical [37] etc. ADCs are an important functional block in such systems. Recently, with the advancement in the area of printed batteries [38], researchers have gained interest in the development of self-sustainable flexible and transparent systems with oxide TFT technology. However, due to the finite life-time of the batteries, energy-efficient on-chip blocks are required to increase the life time of the system. It should be noted that with oxide TFT technology, the state of the art work with Nyquist-rate ADCs are very few [36], which are designed to operate at a voltage not less than 8V and with a very high FOM of nearly 580μJ/c.s. As discussed previously, due to the switching intensive behavior of the SAR ADC, the architecture is suitable for different technology nodes. Moreover, SAR ADCs have higher energy efficiency compared to other Nyquist-rate ADCs. As a result, these ADCs can be the best choice for the battery operated self-sustainable systems with oxide TFT technology.

1.2 Motivation for Hybrid DAC based SAR ADCs

In all the low-power SAR ADCs, one of the critical blocks is the capacitive DAC. The capacitors of the DAC along-with the DAC switches form a switched-capacitor (SC) circuit. This switching intensive block employs different switching schemes to perform the digital-to-analog (D/A) conversion. One of the most popular and extensively used schemes is the charge-redistribution (CR), which was introduced in 1975 [39]. This scheme utilizes binary-weighted capacitors to perform the required conversion. As a result, the size of the DAC increases exponentially with the resolution of the SAR ADC, which consumes a significant chip area compared to the other blocks of the ADC. The DAC's switching energy (E_{DAC}), for a fixed reference voltage (V_{REF}), depends directly on the total DAC capacitance (C_{DAC}) as shown in (1.2).

$$E_{DAC} \propto C_{DAC} V_{REF}^2 \tag{1.2}$$

Moreover, the size of the DAC capacitors along with the on-resistance of the DAC switches decide the time required to charge the capacitors to the reference voltage. Therefore, an exponential increase in DAC size will increase the active area, degrade the conversion speed, input signal bandwidth and energy efficiency of the SAR ADC. Several switching schemes [40–44] were introduced at the later stages to improve the performance of the CR schemes and are extensively employed in the SAR ADCs. Most of these schemes were able to achieve a modest improvement in the energy efficiency of the ADC. One of the contributing factors for this improvement is the decrease in the total DAC capacitance (factor of two or four) by eliminating the MSB and equivalent capacitors to reduce the total switching energy of the DAC. Another scheme that has been recently employed in the SAR ADC is the charge-sharing (CS) scheme [45]. In this scheme, unlike CR, the energy is independent of the output code. It employs an explicit track-and-hold (T/H) capacitor, on which the charges are added and subtracted during the conversion phase. One of the critical features of this scheme is that it performs the conversion process passively, *i.e.*, the DAC capacitors are connected to the reference voltage during the tracking/sampling phase, which is not the case in CR and equivalent schemes. Therefore, the energy is spent on charging the DAC capacitors only during the ADC tracking phase. However, similar to the CR scheme, the DAC size in this scheme increases exponentially with increase in ADC resolution. Major limitation of the CS scheme is its sensitivity to the comparator offset and its input-referred noise. This limitation

has reduced the popularity of the CS scheme among the scientific community. The works reported with CS scheme mainly overcome the sensitivity of the ADC to the comparator offset and noise, power optimization etc. The CS ADC in [45] mitigates the effect of the comparator offset by using the calibration technique. Moreover, the design presented in [46] employs two different comparators (low-power/high-noise and high-power/low-noise) to restore the error caused by noise. On the other hand, the ADC reported in [47] uses a full-custom digital controller to optimize the power dissipation of the ADC. The work in [48] reports an ADC that employ current integration in the sampling front-end. In this work, instead of feeding the T/H capacitors directly from the input signal, a voltage-gain transconductor is used to convert the input voltage into a current. This current is integrated as a charge in the sampling capacitors. The authors also used non-linear T/H metal-oxide-semiconductor (MOS) capacitances for passive amplification, which relaxes the comparator's noise requirements. The CS ADC reported in [30] employs non-linear MOSCAPS as the DAC capacitances, to decrease its sensitivity towards comparators offset and noise. The works reported with the CS scheme do not significantly reduce the DAC size and its switching energy (1.2). On the other hand, most of the CR schemes scale down the length of DAC by a small number. One of the best methods to reduce the size of the DAC, and improve the energy efficiency, input signal bandwidth and conversion speed, with increasing resolution of the SAR ADC, is to use two (or more) small-sized sub-DACs to form the complete DAC of the **ADC [49–51]**. These sub-DACs can work on the same or different switching principles, depending upon the requirement. The works reported in the literature on the hybrid DACs are discussed next.

1.2.1 Previous Works on Hybrid DAC

- **Hybrid DACs with CMOS technology**

  Capacitive-Resistive Hybrid DAC:
  The combination of capacitors and resistors in the DAC of the SAR ADCs are widely used. Several SAR ADCs have been reported in the literature with this type of hybrid DAC. The work reported by **Tong *et al.***, in the year 2011 [52], proposes two-hybrid network for the DAC: resistor-reusing *R-C* and intermittent-sleeping *C-R* networks. Both the networks employ a resistive ladder along with a DAC, which uses CR switching scheme. In

resistor-reusing, a resistive ladder is used for MSBs. This network reduces the capacitor switching energy by reducing the number of capacitors in the least-significant-bits (LSBs) DAC. However, it contributes to the static power from the resistor ladder. Therefore, intermittent-sleeping has been proposed in the same work, where the resistive ladder is used for the LSBs. To avoid the static power dissipation by the resistive ladder, a switch is employed. This switch connects the ladder to the reference voltage during the LSB conversions, and it disconnects it from the voltage when MSB conversion is in progress. The switch that is employed to connect and disconnect the resistive ladder from the reference voltage limits the ADC's operating speed. Moreover, using R-string sub-DAC mandates having a complicated switching network or a digital decoder [21, 53]. **Sedighi *et al***. in the year 2012 [53], reported a hybrid DAC, which employed a binary-weighted resistive ladder with CR scheme to overcome the shortcomings faced by the previous DAC structure, and later it had been adopted by **Wen *et al***. in his ADC design [54]. It should be noted that with binary-weighted resistive DAC, the requirement of high-precision resistors are very stringent as it involves a wide range of the resistor values. Moreover, it demands the DAC switches to have a low impedance. The ADC reported by **Jin *et al.*** [49] and **Li *et al.*** [55] employed R-2R rather than binary-weighted resistive ladder along with capacitive DAC to rectify the problems faced by the previous DAC structures. The R-2R ladder uses only two values of resistors and relaxes the requirement for high-precision resistors and the on-resistance value of DAC switches. Another work reported by **Park *et al.*** [56] uses two capacitive DACs along with the resistive ladder that is used to generate a set of binary-weighted scaled reference voltages for LSB DAC. In this work, the MSB DAC uses binary-weighted capacitors and the LSB DAC employs only a set of unit capacitors. Each unit capacitor in the LSB DAC is connected to the respective scaled reference voltages, generated by the resistive ladder, depending upon the output binary codes of the ADC. Though, this work reduces the overall size of the DAC but, the static power dissipation due to the resistive ladder cannot be avoided. It should be noted that capacitive-resistive hybrid DAC is a good choice to reduce the total capacitance and switching energy of SAR ADCs, but, the design of the resistive DAC faces tradeoffs between power dissipation, operation speed and chip area [57]. Moreover, the matching accuracy of the resistors are poor than the matched capacitors [58], which is a critical factor

in deciding the DAC performance.

Capacitive-Transistor/Capacitive Hybrid DAC:
This is the another way to reduce the total size of the DAC. Here, all the sub DACs are capacitive and thus, eliminates the limitations faced by the resistive DAC. The ADC reported by **Sani *et al.*** [59] employs a spilt-capacitor DAC, where the two binary-weighted capacitive sub-DACs are connected together by a means of a bridge capacitor. They have presented a differential implementation of the DAC in the ADC. It should be noted that the parasitics contributed by the bridge capacitor can degrade the performance of the DAC. Therefore, a calibration logic had been used in the reported work. The calibration is achieved by using the sub-DAC of any one side of the DAC in the differential implementation. **H. Zhang *et al.*** in the year 2019 [60], have used the concept of intermittent-sleeping *C-R* from [52] to design the ADC. In this work, they have replaced the resistive ladder with diode-connected transistors to minimize the power dissipation and save the chip area. In addition, the capacitive DAC is a binary-weighted DAC, which works on the switching principle described in [41]. A combination of serial and split-capacitor DAC has been used by **Q. Zhang *et al.*** in their work [50]. The concept of serial DAC can be studied in [39]. Though, this work was able to deliver a good performance but, it requires a separate SAR logic design for the two sub-DACs. Therefore, it can make the design of SAR controller much more complicated compared to the other works.

- **Hybrid DACs with Oxide TFT technology**
  The work reported on ADC with oxide TFT technology is very scarce. While the SAR ADC reported in [36] employs the conventional C-2C architecture, which adds to the parasitics in the signal path and degrades the operating speed of the ADC, no attempts have been reported on the hybrid DAC based SAR ADCs with this technology to the best of author's knowledge.

1.2.2 Research Goal

Due to the highly digital behavior of the SAR ADCs, the architecture is suitable for different technology nodes. As a result, this work considers implementation of the hybrid DAC based SAR ADC in both sub-micron CMOS technology (STM 65nm) and large-area oxide TFT technology (with 5μm feature size). Looking at the limitations of the resistive sub-DAC, employing only the capacitive sub-

DACs to construct the complete hybrid DAC of the ADC, can be a good choice especially, for the deep-submicron designs and moderate to high frequency applications. As can be seen from the literature, the SAR ADCs with capacitive sub-DACs are very small in numbers. Therefore, we could say, there is a need to investigate more designs under this category to improve the performance of the SAR ADCs. As a result, this research work investigates a hybrid DAC, which employs two capacitive switching principles namely, merged-capacitor switching (MCS) and CS, for the implementation of the SAR ADC in deep-submicron CMOS and large-area oxide TFT technology.

1.3 Research Contributions

The original research contributions of this dissertation are as follows:

- A hybrid capacitive DAC SAR ADC with merged-capacitor switching (MCS) and charge sharing (CS) has been investigated to improve the active-area and energy efficiency of the SAR ADC (Chapter-3). Using the proposed hybrid DAC design, a 10-bit SAR ADC with CMOS technology (Chapter-4) and 7-bit SAR ADC with oxide TFT Technology (Chapter-5) are designed. The two ADCs have shown FoM of 5fJ/c.s. and 56nJ/c.s. in CMOS and oxide TFT technology respectively.

- As a part of this research work, a robust linear sampling switch [61] has been proposed in standard CMOS technology (Chapter-4), which completely eliminates the effect of the transistor's threshold voltage on the on-resistance of the switch. In addition, a linear sampling switch has also been proposed in oxide TFT technology [62] (Chapter-5) using all enhancement n-type transistors due to the lack of stable p-type transistors in oxide TFT technology.

- To eliminate the threshold voltage drop of the n-type switches employed in the DAC, a clock booster has been proposed [63] (Chapter-5) with only n-type transistors in oxide TFT technology.

- Due to the low-intrinsic mobility and lack of stable p-type transistors in oxide TFT technology, various high-speed and low-power ring oscillators

[64–66] (Appendix A) have been proposed, which can be used to produce the oversampling clock signals for operation of SAR ADC in the oxide TFT technology.

- A compact D-type flip-flop [67] and a latch-type comparator [68] have been proposed with Oxide TFT technology to implement SAR ADC in this technology.

1.4 Publications

1.4.1 Journals

1. **B. Tiwari** and P. G. Bahubalindruni, "A Compact Low-Voltage D-type Flip Flop Using Oxide TFTs and its Application in Sequential Circuit." *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2022, doi: 10.1109/TCSII.2022.3220518.
2. **B. Tiwari**, P. G. Bahubalindruni, S. Shrivastava and J. Goes, "Mixed-Signal Building Blocks for Communication Systems Using Flexible Oxide TFT Technology." *IEEE Journal on Flexible Electronics*, 2022, doi: 10.1109/JFLEX.2022.3220719.
3. **Bhawna Tiwari**, Pydi Ganga Bahubalindruni, and Sujit Pedda. "Low-voltage linear bootstrapped sampling switch with a-InGaZnO TFTs." *Electronics Letters* 57.15 (2021): 584-586.
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1.4.2 Conferences

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1.5 Document Outline

- Chapter-2 presents the working principles of CS and MCS SAR ADCs. The two switching principles of the capacitive DAC have been explained using mathematical models, which are used in derivation and explaining the working principle of the proposed hybrid DAC SAR ADC.

- Chapter-3 describes in details the working principle of the proposed CS-MCS hybrid DAC to be employed in the SAR ADC. The mathematical models explained in chapter-2 are used to derive an equivalent model for the hybrid DAC. Moreover, segmentation strategy of the DAC has been discussed, which is followed by the comparison with state of the art capacitive DAC switching schemes.

- Chapter-4 presents the implementation of the hybrid DAC SAR ADC with CMOS technology. The design of the proposed robust linear sampling switch has been presented along with the complete design description of the 10-bit hybrid DAC SAR ADC.

- Chapter-5 presents the implementation of the hybrid DAC SAR ADC with oxide TFT technology. Since this technology lacks stable amorphous p-type transistors, the blocks of the ADC have been designed using all enhancement n-type transistors. As a result, the design of sampling switches, comparator, shift register and clock booster are proposed, which show superior performance compared to state of the art work at a low supply voltage of

2V. In addition, the proposed SAR ADC also shows superior performnace compared to state of the art work with post-layout simulations.

- Finally, this research work is concluded by presenting the possible future scope of the proposed CS-MCS hybrid DAC SAR ADC.

Chapter 2

Working Principles of MCS and CS SAR ADCs

The block diagram of a differential SAR ADC is shown in Figure 2.1. It comprises a voltage comparator, a capacitive DAC and a SAR controller. In addition to all the previous blocks, it requires track-&-hold (T/H) switches for sampling the input analog signal (V_{in}) on the DAC capacitors. The analog-to-digital conversion is performed using two phases of the sampling clock (clk_{samp}). The first phase begins when clk_{samp} makes a transition from logic '0' to logic '1'. In this

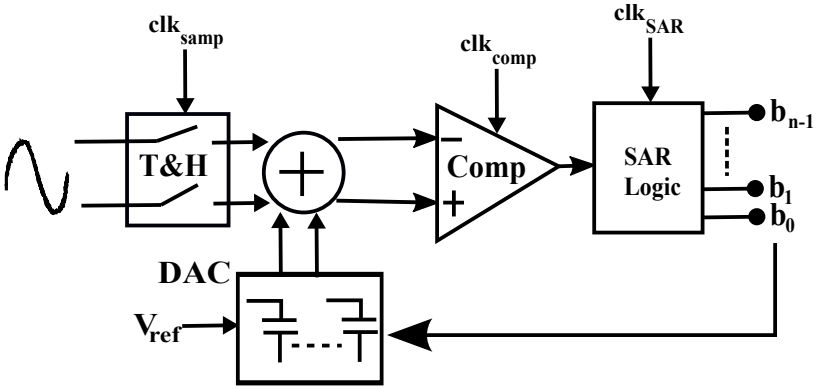


Figure 2.1: **Block Diagram of differential SAR ADC.** [18]

phase, T/H switches provides a resistive path between V_{in} and DAC capacitors. As a result, these capacitors track V_{in} and this phase is known as the tracking phase. Moreover, during this phase, comparator and SAR controller can be turned off to save the power. Next, when the clk_{samp} makes a transition from logic '1' to logic '0', V_{in} is isolated from DAC capacitors. As a result, these capacitors hold the value of V_{in}, which is sampled on it before the end of tracking phase. The comparator and SAR controller are in active state, and the conversion

process is performed in a serial fashion. At the end of this phase, the sampled value of V_{in} is converted to its corresponding digital bits using the binary search algorithm and the process is repeated for the next cycle of clk_{samp}.

The capacitive DAC of the SAR ADC employs one or more array of binary-weighted capacitors. In order to examine the dependency of the active-area and DAC switchinig energy on ADC resolution (n), a conventional charge re-distribution (CR) switching scheme in capacitive DAC is taken under consideration, which employs binary-weighted capacitors. Considering C_{min} is the minimum capacitance realised in a given technology node and V_{REF} is the reference voltage used by the DAC for conversion, the size of the DAC is defined as 2^nC_{min}. Moreover, to have a uniform charging and discharging time constant of every C_{min} irrespective of n, each C_{min} is associated with one switch to form an instance, which is repeated 2^n times to form a DAC. If the active-area occupied by C_{min} and the associated switch is A sq. units, then the minimum total active-area of the DAC will be 2^nA, which increases exponentially with n as shown in Figure 2.2. It should be noted that for minimizing the errors due to mismatches, common-centroid technique is widely used in the layout of the DAC, which may involve addition of dummy capacitors, thus further increasing the total active-area of the DAC. On the other hand, the average switching energy of the CR DAC $E_{DAC,CR}$ over 2^n codes is calculated in [30] and is given by (2.1).

$$E_{DAC,CR} = \left(\frac{2^{-n+1} + 2^{n+1}}{3} - 2\right) C_{min} V_{REF} \tag{2.1}$$

From the above equation, it can be inferred that $E_{DAC,CR}$ also increases with n as shown in Figure 2.2. Next, considering that the ADC operates at FMHz irrespective of the value of n, then the time available (T_{av}) for performing one C_{min} switching in a SAR ADC is proportional to $\frac{T_{per}}{n}$, where T_{per} is given by $\frac{1}{F}$, due to the serial conversion employed in SAR ADC. As a result, T_{av} decrease with increasing n as shown in Figure 2.2. Since the size of C_{min} is fixed by technology, low value of R_{ON} of the switch is desirable for achieving high resolution of the ADC at moderate to high frequency. However, since switches are realized using a simple pass transistor, low R_{ON} demands wider transistor, which adds to parasitic capacitors and other non-linearities associated with switches like charge injection.

From the above discussion, it can be concluded that an exponential increase

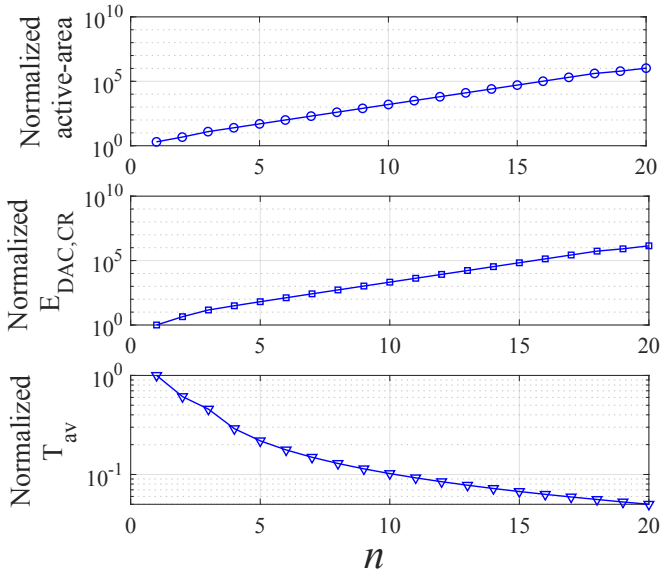


Figure 2.2: **Dependency of active-area, $E_{DAC,CR}$ and T_{av} on the resolution (n) of the ADC.**

in the size of the DAC adds to the increase in its active-area with increasing resolution of the ADC. Moreover, the finite R_{ON} of the sampling and DAC switches, impose limitations on the resolution of the ADC at moderate to high sampling frequency. In addition, the switching energy of the DAC also increases with n. To address these challenges, this research work investigates a hybrid capacitive DAC, which employs two widely used capacitive switching schemes, merged-capacitor switching (MCS) [69] and charge-sharing (CS) [30]. Though, these two schemes follow different algorithms for quantization, the voltages at the input of the comparator converge to the common-mode voltage towards the end of the conversion process. As a result, the two switching schemes can be mixed in a single DAC without employing multiple comparators or modifying its architecture. Before going into the analysis of the hybrid DAC, the MCS and CS switching schemes are discussed briefly in this chapter.

2.1 Merged-Capacitor Switching (MCS) Scheme

The MCS scheme is also known as V_{CM}-based switching scheme [69]. The schematic of the n-bit SAR ADC employing MCS scheme is shown in Figure 2.3. It is the modified and advanced form of the charge-redistribution (CR) based switching scheme. The MCS scheme employs top-plate sampling, which reduces the total DAC size by a factor of two compared to the conventional CR

scheme. Moreover, no switching is performed by the DAC to determine the MSB bit and hence, its switching energy is ideally zero for MSB conversion.

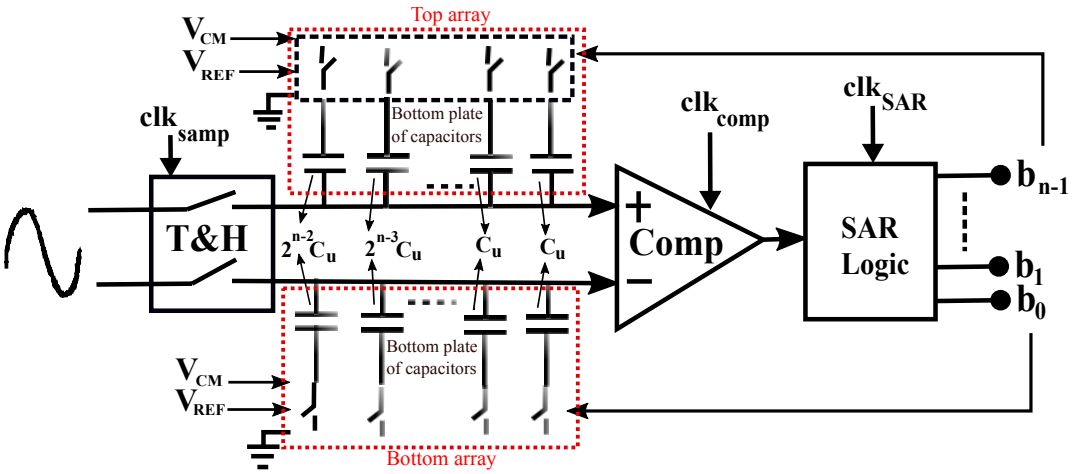


Figure 2.3: **Block Diagram of an n-bit MCS SAR ADC.**

The MCS switching scheme is explained using a 3-bit SAR ADC, whose schematic is shown in Figure 2.4. The output bits of the ADC are represented as b_0, b_1 and b_2, where b_2 is the MSB. Moreover, C_u represents the unit capacitor of the DAC array. When clk_{samp} makes a transition from logic '0' to logic '1', the top plates of the capacitors in the DAC arrays track the differential input analog signal ($V_{IN,P}$ and $V_{IN,N}$), while their bottom plates are connected to the common-mode voltage (V_{CM})=$\frac{V_{REF}}{2}$, where V_{REF} is the reference voltage used by the DAC to perform the conversion. Next, when clk_{samp} makes a transition from logic '1' to logic '0', the input signal is isolated from the DAC capacitors. The voltages at the positive ($V_P[i]$) and negative ($V_N[i]$) input of the comparator at cycle i=0 are given by (2.2):

$$V_P[0] = V_{IN,P},\ V_N[0] = V_{IN,N} \tag{2.2}$$

The comparator compares the voltages at its input on the arrival of the first rising edge of the comparator clock signal (clk_{comp}) and resolves b_2 as logic '1' ($V_P[0] - V_N[0] > 0$) or logic '0' ($V_P[0] - V_N[0] < 0$) using SAR controller. Since no capacitor switching is performed for MSB decision, DAC's switching energy is ideally zero. After b_2 is resolved, its decision is fed back to the DAC arrays and i increments to one. Depending upon the state of b_2, the bottom plate of the largest capacitor ($2C_u$) in the DAC arrays switches from V_{CM} to ground level or V_{REF} and the bottom plates of the remaining capacitors are held at V_{CM}. If b_2 is at logic '1', the bottom plate of $2C_u$ in the top DAC array is switched from V_{CM} to ground level , while the bottom plate of the $2C_u$ in the bottom DAC

array is switched from V_{CM} to V_{REF}. On the other hand, if b_2 is at logic '0', the bottom plate of $2C_u$ in the top DAC array is switched from V_{CM} to V_{REF}, while the bottom plate of the $2C_u$ in the bottom DAC array is switched from V_{CM} to ground level. Therefore, the voltages at the input of the comparators, after the complete settling of the voltages at the bottom plate of $2C_u$, are given by (2.3) and (2.4).

$$\begin{aligned} V_P[1] &= V_{IN,P} - V_{CM} + \frac{(1-b_2)2C_u}{2C_u+C_u+C_u}V_{REF} + \frac{C_u+C_u}{2C_u+C_u+C_u}V_{CM} \\ &= V_{IN,P} - \frac{2C_u}{2C_u+C_u+C_u}V_{CM} + \frac{(1-b_2)2C_u}{2C_u+C_u+C_u}V_{REF} \end{aligned} \tag{2.3}$$

$$\begin{aligned} V_N[1] &= V_{IN,N} - V_{CM} + \frac{b_2 2C_u}{2C_u+C_u+C_u}V_{REF} + \frac{C_u+C_u}{2C_u+C_u+C_u}V_{CM} \\ &= V_{IN,N} - \frac{2C_u}{2C_u+C_u+C_u}V_{CM} + \frac{b_2 2C_u}{2C_u+C_u+C_u}V_{REF} \end{aligned} \tag{2.4}$$

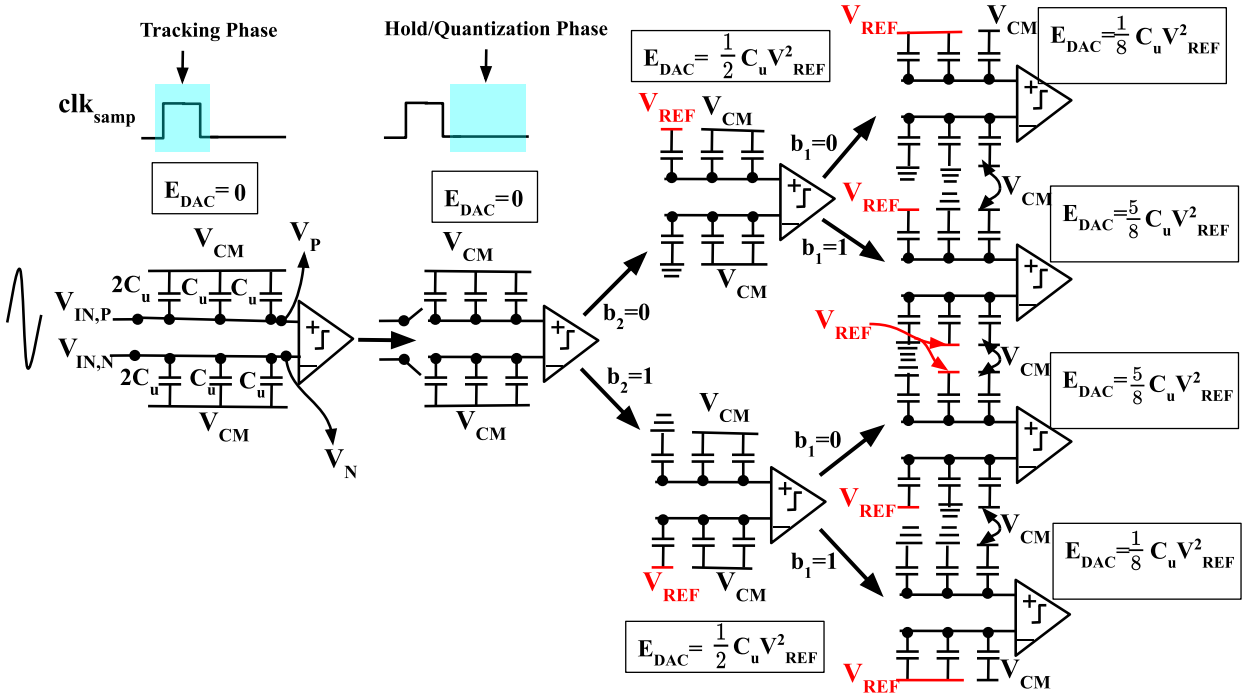


Figure 2.4: Conversion procedure of MCS based switching scheme in a 3-bit SAR ADC.

In the above equations, b_2 is taken as one for logic '1' and zero for logic '0'. Again, comparator compares the voltages at its input on the arrival of the second rising edge of clk_{comp} and resolves b_1 as logic '1' ($V_P[1] - V_N[1] > 0$) or logic '0' ($V_P[1] - V_N[1] < 0$) using SAR controller and i increments to two. The

decision on b_1 is fed back to the DAC arrays to resolve b_0. If b_1 is at logic '1' (logic '0'), the bottom plate of C_u in the top DAC array is switched from V_{CM} to ground level (V_{REF}), while the bottom plate of the C_u in the bottom DAC array is switched from V_{CM} to V_{REF} (ground level). Furthermore, no switching activity is performed on $2C_u$ and its bottom plate is in the same state as it was before the end of cycle i=1. Therefore, the voltages at the input of the comparators, after the complete settling of the voltages at the bottom plate of C_u, are given by (2.5) and (2.6).

$$\begin{aligned} V_P[2] &= V_{IN,P} - V_{CM} + \frac{(1-b_2)2C_u + (1-b_1)C_u}{2C_u + C_u + C_u}V_{REF} + \frac{C_u}{2C_u + C_u + C_u}V_{CM} \\ &= V_{IN,P} - \frac{2C_u + C_u}{2C_u + C_u + C_u}V_{CM} + \frac{(1-b_2)2C_u + (1-b_1)C_u}{2C_u + C_u + C_u}V_{REF} \end{aligned} \tag{2.5}$$

$$\begin{aligned} V_N[2] &= V_{IN,N} - V_{CM} + \frac{b_2 2C_u + b_1 C_u}{2C_u + C_u + C_u}V_{REF} + \frac{C_u}{2C_u + C_u + C_u}V_{CM} \\ &= V_{IN,N} - \frac{2C_u + C_u}{2C_u + C_u + C_u}V_{CM} + \frac{b_2 2C_u + b_1 C_u}{2C_u + C_u + C_u}V_{REF} \end{aligned} \tag{2.6}$$

The comparator compares the above voltages at its input on the arrival of the third rising edge of clk_{comp} and resolves b_0 as logic '1' ($V_P[2] - V_N[2] > 0$) or logic '0' ($V_P[2] - V_N[2] < 0$) using SAR controller. Since C_u performs switching action corresponding to the state of b_1, the switching energy of DAC is given in Figure 2.4. Once the b_0 is resolved, i is reset to zero on the arrival of next rising edge of clk_{samp} and the complete process is repeated for next sampled voltage.

The above method is described for 3-bit SAR ADC and it can be easily extended to n-bit SAR ADC by repeating the process n times before the next cycle of clk_{samp}. Therefore, the voltages at the input of the comparator during any cycle i for n-bit resolution are given by (2.7) and (2.8).

$$V_P[i] = V_{IN,P} - \frac{\sum_{j=1}^{i} C_{n-j-1}}{2^{n-1}C_u}V_{CM} + \frac{\sum_{j=1}^{i}(1-b_{n-j})C_{n-j-1}}{2^{n-1}C_u}V_{REF} \tag{2.7}$$

$$V_N[i] = V_{IN,N} - \frac{\sum_{j=1}^{i} C_{n-j-1}}{2^{n-1}C_u}V_{CM} + \frac{\sum_{j=1}^{i} b_{n-j}C_{n-j-1}}{2^{n-1}C_u}V_{REF} \tag{2.8}$$

where,

$$C_{n-j-1} = 2^{n-j-1}C_u \tag{2.9}$$

The DAC's switching energy at every cycle is calculated using the method described in [70] and the calculated values are shown in Figure 2.4. As shown in the figure, E_{DAC} is zero when no DAC switching is performed. Once the tracking phase is over, $V_{IN,P}$ and $V_{IN,N}$ are sampled on the top plates of top and bottom array of the DAC, and the MSB capacitor $2Cu$ is switched either to zero or V_{REF}. Let the MSB capacitor switching is performed at t = 0 and it settles at $t = T_p$, then the total energy drawn from V_{REF} (E_{DAC}) during i=1 is the sum of energy from top and bottom array of the DAC and it given by (2.10).

$$\begin{aligned} E_{DAC}[1] &= E_{DAC,top} + E_{DAC,bottom} \\ &= \int_{0^+}^{T_p} \big(i_{REF,top}(t) + i_{REF,bottom}(t)\big) V_{REF} dt \\ &= V_{REF} \int_{0^+}^{T_p} -\left(\frac{dQ_{2C_u,top}}{dt} + \frac{dQ_{2C_u,bottom}}{dt}\right) dt \end{aligned} \tag{2.10}$$

Equation (2.10) simplifies to (2.11).

$$\begin{aligned} E_{DAC}[1] &= -V_{REF} \int_{Q_{2C_u}(0+)}^{Q_{2C_u}(T_p)} (dQ_{2C_u,top} + dQ_{2C_u,bottom}) \\ &= -V_{REF}\Big(\big(Q_{2Cu,top}(T_p) - Q_{2C_u,top}(0^+)\big) + \\ &\quad \big(Q_{2C_u,bottom}(T_p) - Q_{2C_u,bottom}(0^+)\big)\Big) \end{aligned} \tag{2.11}$$

According to charge continuity on a capacitor, $Q_{2Cu,top}(0^+) = Q_{2C_u,top}(0^-) = 2C_u(V_{IN,P} - V_{CM})$ and $Q_{2C_u,bottom}(0^+) = Q_{2C_u,bottom}(0^-) = 2C_u(V_{IN,N} - V_{CM})$. Now, if b_2 is one $Q_{2Cu,top}(T_p) = 2C_u(V_P[1] - V_{REF})$ and $Q_{2Cu,bottom}(T_p) = 2C_uV_N[1]$, else $Q_{2Cu,top}(T_p) = 2C_uV_P[1]$ and $Q_{2Cu,bottom}(T_p) = 2C_u(V_N[1] - V_{REF})$. Therefore, the energy drawn form V_{REF} at the end of cycle i = 1 comes out to be $\frac{1}{2}C_uV_{REF}^2$ from (2.11). The same process is followed to calculate the total energy drawn from the V_{REF} at every cycle and it is shown in Figure 2.4.

The average switching energy of the DAC of 2^n codes ($E_{DAC,MCS_{AVG}}$) for a n-bit conversion is calculated in [71] and given by (2.12). It should be noted that the switching energy of the DAC depends on the output codes of the SAR

ADC.

$$E_{DAC,MCS_{AVG}} = \left(\frac{2^{-n} + 2^{n-1}}{3} - \frac{1}{2}\right) C_u V_{REF}^2 \tag{2.12}$$

To make the conversion process more clear, behavioral simulations of a 10-bit SAR ADC have been performed using equations (2.7) and (2.8) for fixed input voltages. The values of V_{REF}, $V_{IN,P}$ and $V_{IN,N}$ have been taken as 1V, 0.9V and 0.1V, respectively for the simulations. The conversion waveform of the SAR ADC with MCS switching scheme is shown in Figure 2.5. It is observed from the figure that the voltages at the input of the comparator converges towards V_{CM} at the end of conversion.

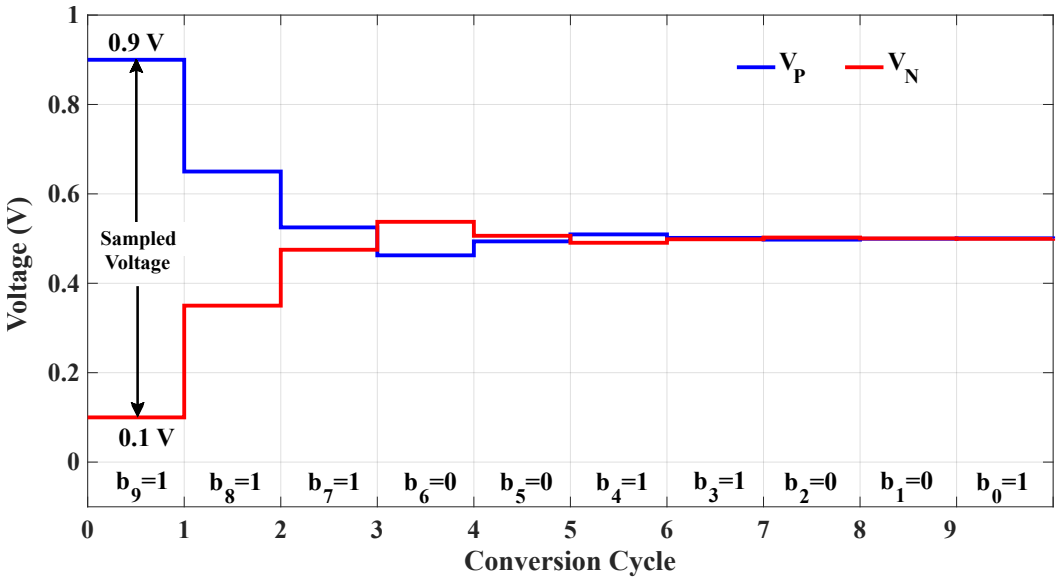


Figure 2.5: Conversion waveform of 10-bit MCS SAR ADC.

2.2 Charge-Sharing (CS) Switching Scheme

The schematic of the n-bit SAR ADC employing the CS switching scheme [30] is shown in Figure 2.6. Like MCS scheme, this scheme also employs top-plate sampling. However, unlike MCS scheme, it has only a single array of binary-weighted capacitors and employs explicit track and hold capacitors (C_{TH}). Moreover, the DAC capacitors are not connected to the reference voltage source during the conversion process, which results in an ideally zero switching energy of the DAC.

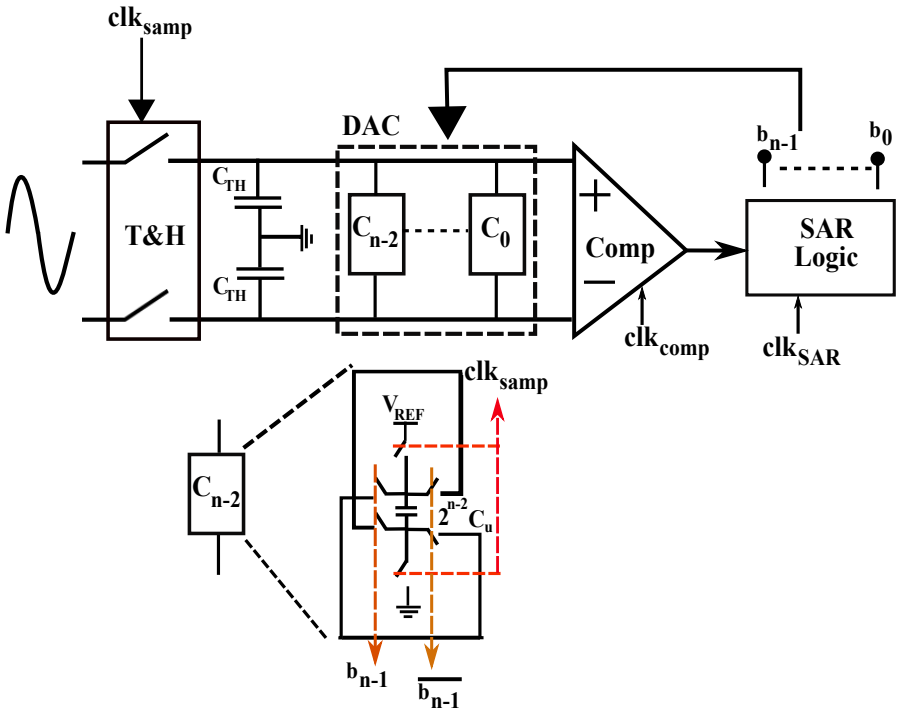


Figure 2.6: Block Diagram of a n-bit CS SAR ADC.

The CS switching scheme is explained using a 3-bit SAR ADC, whose schematic is shown in Figure 2.7. The output bits of the ADC are represented as b_0, b_1 and b_2, where b_2 is the MSB. It should be noted that the DAC capacitors are connected between the two inputs of the comparator. As a result, the top and bottom plate parasitics of the DAC capacitors cannot be avoided, and are assumed to be same (=C_p) for simplification. Moreover, it is also assumed that the inputs to the comparator have an infinite resistance. When clk_{samp} makes a transition from logic '0' to logic '1', capacitors C_{TH} track the differential input analog signal ($V_{IN,P}$ and $V_{IN,N}$), while the DAC capacitors ($2C_u$ and C_u) are pre-charged to the reference voltage (V_{REF}). The switching energy of the DAC is $3C_uV_{REF}^2$. Next, when clk_{samp} makes a transition from logic '1' to logic '0', the input analog signal is isolated from C_{TH} and the DAC capacitors are disconnected from V_{REF}. As a result, the DAC's switching energy is ideally zero, and the conversion process is passive. The voltages at the positive (V_P) and negative (V_N) input of the comparator at cycle i=0 are given by (2.13):

$$V_P[0] = V_{IN,P},\ V_N[0] = V_{IN,N} \tag{2.13}$$

Moreover, the charges stored on the positive (Q_P) and negative (Q_N) terminals

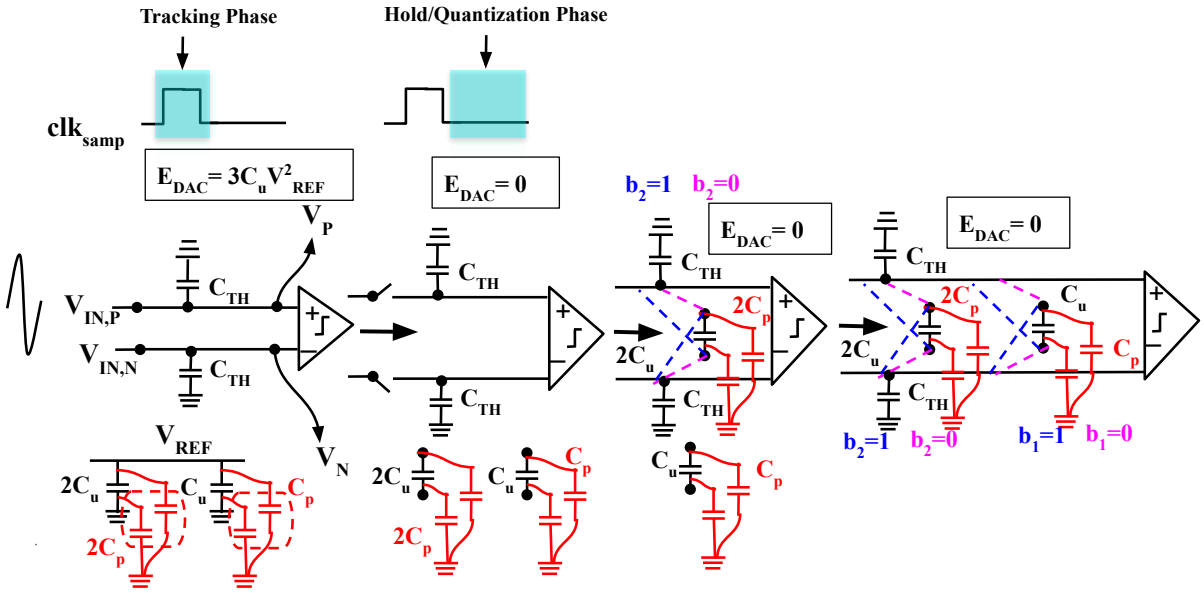


Figure 2.7: Conversion procedure of CS based switching scheme in a 3-bit SAR ADC.

of the DAC unit cells and C_{TH} are described by (2.14).

$$\begin{aligned} Q_{C_{TH},P}[0] = C_{TH}V_{IN,P},\ Q_{C_{TH},N}[0] = C_{TH}V_{IN,N},\\ Q_{2C_u,P}[0] = 2(C_u + C_p)V_{REF},\ Q_{2C_u,N}[0] = -2C_uV_{REF},\\ Q_{C_u,P}[0] = (C_u + C_p)V_{REF},\ Q_{C_u,N}[0] = -C_uV_{REF} \end{aligned} \tag{2.14}$$

The comparator compares the voltages at its input on the arrival of the first rising edge of clk_{comp} and resolves b_2 as logic '1' ($V_P[0] - V_N[0] > 0$) or logic '0' ($V_P[0] - V_N[0] < 0$) using SAR controller. After b_2 is resolved, its decision is fed back to the DAC array and i increments to one. Depending upon the state of b_2, the largest capacitor ($2C_u$) in the DAC array connects parallel (b_2=0) or anti-parallel (b_2=1) to C_{TH}. As a result, the total charges on nodes $V_P[i]$ and $V_N[i]$ are given by (2.15).

$$\begin{aligned} Q_P[1] = (C_{TH} + 2C_p)V_P[1] + 2C_u(V_P[1] - V_N[1]),\\ Q_N[1] = (C_{TH} + 2C_p)V_N[1] + 2C_u(V_N[1] - V_P[1]) \end{aligned} \tag{2.15}$$

According to the charge conservation principle, (2.16) holds if b_2=0 and (2.17) holds otherwise.

$$\begin{aligned} Q_P[1] &= Q_{C_{TH},P}[0] + Q_{2C_u,P}[0], \\ Q_N[1] &= Q_{C_{TH},N}[0] + Q_{2C_u,N}[0] \end{aligned} \tag{2.16}$$

$$\begin{aligned} Q_P[1] &= Q_{C_{TH},P}[0] + Q_{2C_u,N}[0], \\ Q_N[1] &= Q_{C_{TH},N}[0] + Q_{2C_u,P}[0] \end{aligned} \tag{2.17}$$

From equations (2.14), (2.15), (2.16) and (2.17), $V_P[1]$ and $V_N[1]$ are evaluated as given in (2.18).

$$\begin{aligned} V_P[1] = &-\frac{2C_u\Big[C_{TH}V_{IN,N} + \Big((2b_2-1)2C_u + b_2 2C_p\Big)V_{REF}\Big]}{(2C_u)^2 - (C_{TH}+2C_{up})^2} \\ &- \frac{\Big(C_{TH}+2C_{up}\Big)\Big[C_{TH}V_{IN,P} - \Big((2b_2-1)2C_u + (b_2-1)2C_p\Big)V_{REF}\Big]}{(2C_u)^2 - (C_{TH}+2C_{up})^2} \\ V_N[1] = &-\frac{2C_u\Big[C_{TH}V_{IN,P} - \Big((2b_2-1)2C_u + (b_2-1)2C_p\Big)V_{REF}\Big]}{(2C_u)^2 - (C_{TH}+2C_{up})^2} \\ &- \frac{\Big(C_{TH}+2C_{up}\Big)\Big[C_{TH}V_{IN,N} + \Big((2b_2-1)2C_u + b_2 2C_p\Big)V_{REF}\Big]}{(2C_u)^2 - (C_{TH}+2C_{up})^2} \end{aligned} \tag{2.18}$$

where,

$$C_{up} = C_u + C_p \tag{2.19}$$

The comparator compares the voltages at its input on the arrival of the second rising edge of clk_{comp} and resolves b_1 as logic '1' ($V_P[1] - V_N[1] > 0$) or logic '0' ($V_P[1] - V_N[1] < 0$) using SAR controller. The decision on b_1 is fed back to the DAC array and i increments to two. Depending upon the state of b_1, the next capacitor (C_u) in the DAC array connects parallel (b_1=0) or anti-parallel (b_1=1) to C_{TH}. As a result, the total charges on nodes $V_P[i]$and $V_N[i]$are given by (2.20).

$$\begin{aligned} Q_P[2] &= (C_{TH} + 2C_p + C_p)V_P[2] + (2C_u + C_u)(V_P[2] - V_N[2]), \\ Q_N[2] &= (C_{TH} + 2C_p + C_p)V_N[2] + (2C_u + C_u)(V_N[2] - V_P[2]) \end{aligned} \tag{2.20}$$

According to the charge conservation principle, (2.21) holds if b_2b_1=00, (2.22)

holds if b_2b_1=01, (2.23) holds if b_2b_1=10 and (2.24) holds otherwise.

$$\begin{aligned} Q_P[2] &= Q_{C_{TH},P}[0] + Q_{2C_u,P}[0] + Q_{C_u,P}[0], \\ Q_N[2] &= Q_{C_{TH},N}[0] + Q_{2C_u,N}[0] + Q_{C_u,N}[0] \end{aligned} \tag{2.21}$$

$$\begin{aligned} Q_P[2] &= Q_{C_{TH},P}[0] + Q_{2C_u,P}[0] + Q_{C_u,N}[0], \\ Q_N[2] &= Q_{C_{TH},N}[0] + Q_{2C_u,N}[0] + Q_{C_u,P}[0] \end{aligned} \tag{2.22}$$

$$\begin{aligned} Q_P[2] &= Q_{C_{TH},P}[0] + Q_{2C_u,N}[0] + Q_{C_u,P}[0], \\ Q_N[2] &= Q_{C_{TH},N}[0] + Q_{2C_u,P}[0] + Q_{C_u,N}[0] \end{aligned} \tag{2.23}$$

$$\begin{aligned} Q_P[2] &= Q_{C_{TH},P}[0] + Q_{2C_u,N}[0] + Q_{C_u,N}[0], \\ Q_N[2] &= Q_{C_{TH},N}[0] + Q_{2C_u,P}[0] + Q_{C_u,P}[0] \end{aligned} \tag{2.24}$$

From equations (2.14), (2.20), (2.21), (2.22), (2.23) and (2.24), $V_P[2]$ and $V_N[2]$ are evaluated as given in (2.25).

$$\begin{aligned} V_P[2] = &-\frac{\left\{2C_u\left[C_{TH}V_{IN,N} + \Big((2b_2-1)2C_u + b_2 2C_p + (2b_1-1)C_u + b_1C_p\Big)V_{REF}\right]\right\}}{(2C_u+C_u)^2 - (C_{TH}+2C_{up}+C_{up})^2} \\ &-\frac{\left\{\Big(C_{TH}+2C_{up}+C_{up}\Big)\left[C_{TH}V_{IN,P} - \Big((2b_2-1)2C_u + (b_2-1)2C_p + (2b_1-1)C_u + (b_1-1)C_p\Big)V_{REF}\right]\right\}}{(2C_u+C_u)^2 - (C_{TH}+2C_{up}+C_{up})^2} \\ V_N[2] = &-\frac{\left\{2C_u\left[C_{TH}V_{IN,P} - \Big((2b_2-1)2C_u + (b_2-1)2C_p + (2b_1-1)C_u + (b_1-1)C_p\Big)V_{REF}\right]\right\}}{(2C_u+C_u)^2 - (C_{TH}+2C_{up}+C_{up})^2} \\ &-\frac{\left\{\Big(C_{TH}+2C_{up}+C_{up}\Big)\left[C_{TH}V_{IN,N} + \Big((2b_2-1)2C_u + (b_2-1)2C_p + 2b_1C_u + b_1C_p\Big)V_{REF}\right]\right\}}{(2C_u+C_u)^2 - (C_{TH}+2C_{up}+C_{up})^2} \end{aligned} \tag{2.25}$$

Again, the comparator compares the voltages at its input on the arrival of the third rising edge of clk_{comp} and resolves the LSB (b_0) as logic '1' ($V_P[2] - V_N[2] > 0$) or logic '0' ($V_P[2] - V_N[2] < 0$) using SAR controller. Once b_0 is resolved, i is reset to zero on the arrival of next rising edge of clk_{samp} and the complete process is repeated for next sampled voltage.

The above method is described for a 3-bit SAR ADC and it can be easily extended to n-bit SAR ADC by repeating the process n times before the next cycle of clk_{samp}. Therefore, the voltages at the input of the comparator during any cycle i for n-bit resolution are given by (2.26) and (2.27).

$$V_P[i] = -\frac{\left\{\sum_{j=1}^{i} C_{n-j-1}\left[C_{TH}V_{IN,N} + \sum_{j=1}^{i}\left(B_{n-j}C_{n-j-1} + b_{n-j}C_{p,n-j-1}\right)V_{REF}\right]\right\}}{\left(\sum_{j=1}^{i} C_{n-j-1}\right)^2 - C_{tot}^2} - \frac{C_{tot}\left[C_{TH}V_{IN,P} - \sum_{j=1}^{i}\left(B_{n-j}C_{n-j-1} + (b_{n-j}-1)C_{p,n-j-1}\right)V_{REF}\right]}{\left(\sum_{j=1}^{i} C_{n-j-1}\right)^2 - C_{tot}^2} \tag{2.26}$$

$$V_N[i] = -\frac{\left\{\sum_{j=1}^{i} C_{n-j-1}\left[C_{TH}V_{IN,P} - \sum_{j=1}^{i}\left(B_{n-j}C_{n-j-1} + (b_{n-j}-1)C_{p,n-j-1}\right)V_{REF}\right]\right\}}{\left(\sum_{j=1}^{i} C_{n-j-1}\right)^2 - C_{tot}^2} - \frac{C_{tot}\left[C_{TH}V_{IN,N} + \sum_{j=1}^{i}\left(B_{n-j}C_{n-j-1} + b_{n-j}C_{p,n-j-1}\right)V_{REF}\right]}{\left(\sum_{j=1}^{i} C_{n-j-1}\right)^2 - C_{tot}^2} \tag{2.27}$$

where,

$$C_{n-j-1} = 2^{n-j-1}C_u, \quad C_{p,n-j-1} = 2^{n-j-1}C_p, \quad B_{n-j} = 2b_{n-j} - 1, \quad C_{tot} = C_{TH} + \sum_{j=1}^{i}(C_{n-j-1} + C_{p,n-j-1}) \tag{2.28}$$

The average switching energy of the DAC for a n-bit conversion is given by (2.29), considering C_p to be negligible in comparison to C_u. It should be noted that this energy is independent of the output codes of the SAR ADC.

$$E_{DAC,CS} = (2^{n-1} - 1)C_u V_{REF}^2 \tag{2.29}$$

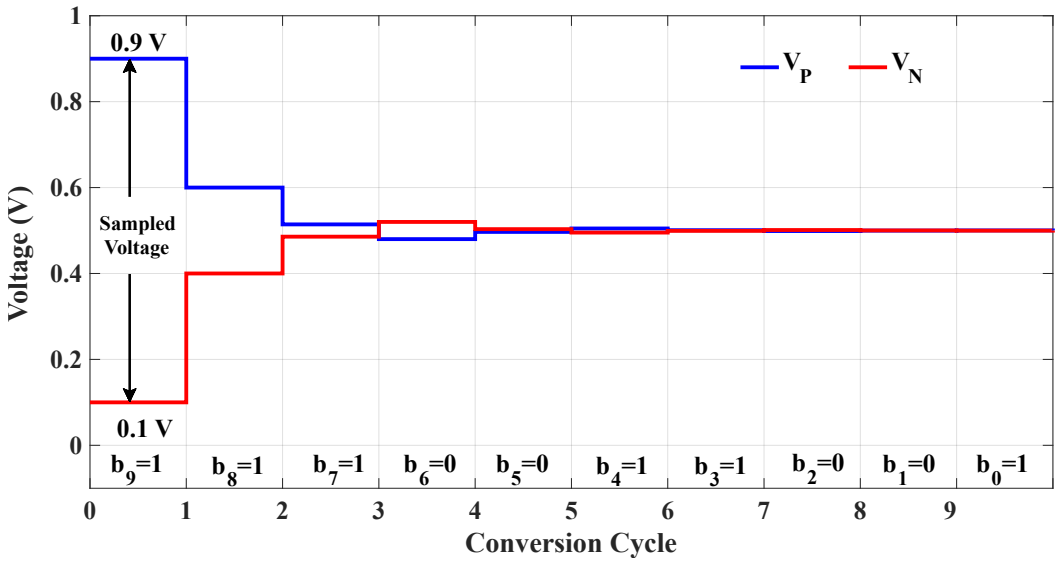


Figure 2.8: Conversion waveform of 10-bit CS SAR ADC.

To make the conversion process more clear, behavioral simulations of a 10-bit SAR ADC have been performed using equations (2.26) and (2.27) for fixed input voltages ignoring the effect of parasitics. The values of V_{REF}, $V_{IN,P}$ and $V_{IN,N}$ have been taken as 1V, 0.9V and 0.1V, respectively for the simulations. The conversion waveform of the SAR ADC with MCS switching scheme is shown in Figure 2.8. It is observed from the figure that like MCS, the voltages at the input of the comparator converges towards V_{CM} at the end of conversion.

It should be noted that in CS switching scheme, the value of C_{TH} exponentially increases with the resolution of the ADC. The expression of C_{TH} is derived in [30] (in terms of C_u and C_p) and it is given in (2.30). Though it employs a single DAC array and performs passive conversion, the presence of explicit C_{TH} has to be included in the total area.

$$C_{TH} = 2^n(C_u + 0.5C_p) \tag{2.30}$$

Moreover, the time-varying behaviour of the DAC capacitance connected to the comparator, makes this switching scheme non-linear in presence of comparator offset. The detailed analysis of the non-linearity associated with CS switching is

presented in [30].

2.3 Conclusions

This chapter presented the working principles of MCS and CS switching schemes, which are employed in the capacitive hybrid DAC SAR ADC. The mathematical equations presented in this chapter for the two schemes are employed for developing the behavioural model of the hybrid DAC SAR ADC.

Chapter 3

The CS-MCS Hybrid DAC in SAR ADCs

The hybrid DAC employing CS and MCS switching schemes can be spilt into the coarse DAC (for MSBs) and the fine DAC (for LSBs), which results into the following two possible architectures of the hybrid DAC:

1) CS coarse and MCS fine hybrid DAC
2) MCS coarse and CS fine hybrid DAC

Since the CS and MCS switching schemes employ top-plate sampling, they perform MSB conversion without performing any capacitive switching from the DAC. As a result, the hybrid DAC shares the LSB of the coarse DAC with the MSB of the fine DAC, *i.e.*, the LSB of the coarse DAC is the MSB of the fine DAC, which results in one-bit redundancy. Therefore, for an $\boldsymbol{n}$-bit hybrid DAC, if $\boldsymbol{x}$-bits are reserved for coarse DAC, then the number of bits allocated to the fine DAC (y) are given by (3.1).

$$y = n - (x - 1) \tag{3.1}$$

The working principles of the two hybrid architectures are discussed in this chapter. Performance of these two architectures are compared to select better design between them. In addition, the segmentation strategy is also presented alongwith the comparison with the state of the art work to choose the optimal partition.

3.1 Hybrid DAC Architectures

3.1.1 CS coarse and MCS fine hybrid DAC

The schematic of the SAR ADC employing x- bit CS coarse and y-bit MCS fine hybrid DAC is shown in Figure 3.1. The unit capacitors of the coarse and the fine DACs are denoted as $C_{u,cs}$ and $C_{u,mcs}$, respectively. For simplicity, the bottom and top plate parasitics of the CS DAC capacitors are considered to be same, and denoted by C_p. Since CS switching scheme employs explicit track & hold capacitors (C_{TH}), there is a possibility to mimic the total capacitance of the MCS DAC ($C_{total,mcs} = 2^{(y-1)}C_{u,mcs}$) as C_{TH}, when the MSB conversion is active. As a result, the relation between $C_{u,cs}$ and $C_{total,mcs}$ can be derived using (2.30) and it is shown in (3.2).

$$\begin{aligned} C_{total,mcs} &= 2^{x}(C_{u,cs} + 0.5C_p) \\ &= 2^{(y-1)}C_{u,mcs} \end{aligned} \tag{3.2}$$

Therefore, from (3.2) the relation between the unit capacitors of the coarse and the fine DAC has been derived as shown in (3.3).

$$C_{u,mcs} = 2^{(x-(y-1))}(C_{u,cs} + 0.5C_p) \tag{3.3}$$

It should be noted that the matching between the two DACs is achieved using two different reference voltages: one for coarse ($V_{REF,MSB}$) and the other for fine DAC ($V_{REF,LSB}$). Once the conversion by the coarse DAC is complete, the reference voltage seen by the fine DAC should be a scaled version of $V_{REF,MSB}$ to perform the correct conversion. Therefore, for n-bit hybrid DAC SAR ADC with y-bit fine DAC, $V_{REF,LSB}$ is given by (3.4).

$$V_{REF,LSB} = \frac{V_{REF,MSB}}{2^{(n-y)}} \tag{3.4}$$

The operation of the SAR ADC with the CS coarse and MCS fine hybrid DAC is explained using a 6-bit SAR ADC with a 3-bit coarse CS DAC and a 4-bit (from (3.1)) fine MCS DAC, and the schematic of the conversion process is shown in Figure 3.2. The output bits of the ADC are represented as b_0, b_1, b_2, b_3, b_4 and b_5, where b_5 is the MSB. When clk_{samp} makes a transition from logic '0' to logic '1', the top plates of the capacitors in the fine DAC (=$C_{total,mcs}$) tracks

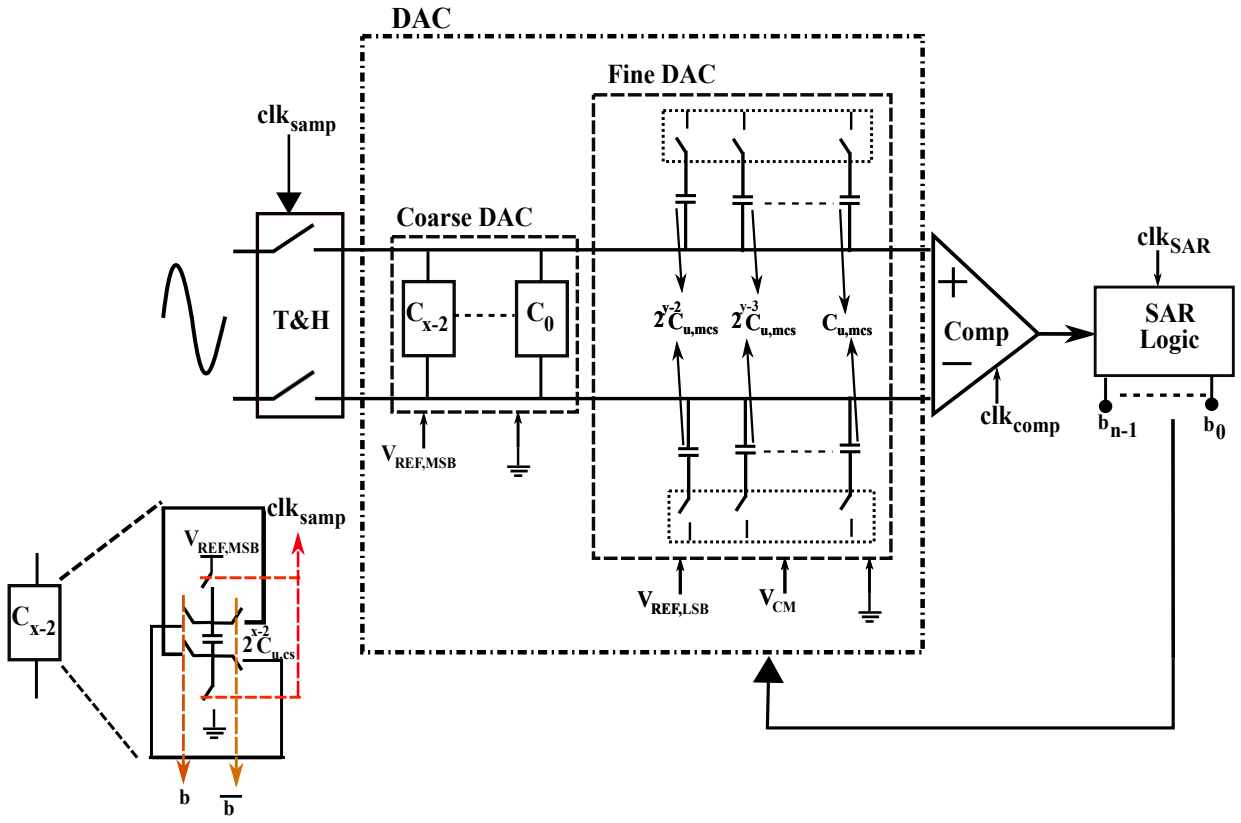


Figure 3.1: Block Diagram of a n-bit CS coarse-MCS fine Hybrid DAC based SAR ADC.

the differential analog input voltage ($V_{IN,P}$ and $V_{IN,N}$), while their bottom plates are connected to V_{CM} (=$\frac{V_{REF,LSB}}{2}$). Moreover, the capacitors of the coarse DAC are pre-charged to $V_{REF,MSB}$. Next, when clk_{samp} makes a transition from logic '1' to logic '0', the conversion begins by the coarse DAC with CS switching principle for three MSBs (b_5, b_4 and b_3). It should be noted that during the conversion by the coarse DAC, the capacitors of the fine DAC will not perform any switching activities, and they will act as a track & hold capacitors for the coarse conversion. The two MSBs (b_5, b_4) are resolved using the CS switching principle explained in Chapter 2 Section 2.2. As a result, the voltages at the input of the comparator (V_{P_h} and V_{N_h}) in a hybrid DAC SAR ADC at the end of cycle i=2 are given by (3.5), which is derived by replacing C_{TH}, b_2 and b_1 with $C_{total,mcs}$, b_5 and b_4, respectively, in (2.26) after two rising edges of the clk_{comp}.

$$V_{P_h}[2] = -\frac{\left\{\begin{array}{l} 2C_{u,cs}\Big[C_{total,mcs}V_{IN,N} + \Big((2b_5-1)2C_{u,cs} \\ \quad + b_5 2C_p + (2b_4-1)C_{u,cs} + b_4 C_p\Big)V_{REF,MSB}\Big] \end{array}\right\}}{(2C_{u,cs}+C_{u,cs})^2 - (C_{total,mcs}+2C_{pu,cs}+C_{pu,cs})^2}$$

$$
\begin{aligned}
V_{N_h}[2] = &-\frac{\left\{\begin{array}{l}\Big(C_{total,mcs}+2C_{pu,cs}+C_{pu,cs}\Big)\Big[C_{total,mcs}V_{IN,P} \\ \qquad -\Big((2b_5-1)2C_{u,cs}+(b_5-1)2C_p \\ \qquad +(2b_4-1)C_{u,cs}+(b_4-1)C_p\Big)V_{REF,MSB}\Big]\end{array}\right\}}{(2C_{u,cs}+C_{u,cs})^2-(C_{total,mcs}+2C_{pu,cs}+C_{pu,cs})^2} \\
&-\frac{\left\{\begin{array}{l}2C_{u,cs}\Big[C_{total,mcs}V_{IN,P}-\Big((2b_5-1)2C_{u,cs}+(b_5-1)2C_p \\ \qquad +(2b_4-1)C_{u,cs}+(b_4-1)C_p\Big)V_{REF,MSB}\Big]\end{array}\right\}}{(2C_{u,cs}+C_{u,cs})^2-(C_{total,mcs}+2C_{pu,cs}+C_{pu,cs})^2} \\
&-\frac{\left\{\begin{array}{l}\Big(C_{total,mcs}+2C_{pu,cs}+C_{pu,cs}\Big)\Big[C_{total,mcs}V_{IN,N} \\ \quad +\Big((2b_5-1)2C_{u,cs}+b_5 2C_p+(2b_4-1)C_{u,cs} \\ \qquad +b_4C_p\Big)V_{REF,MSB}\Big]\end{array}\right\}}{(2C_{u,cs}+C_{u,cs})^2-(C_{total,mcs}+2C_{pu,cs}+C_{pu,cs})^2}
\end{aligned}
\tag{3.5}
$$

where,

$$C_{pu,cs} = C_{u,cs} + C_p \tag{3.6}$$

The coarse DAC resolves its LSB (b_3) on the arrival of the third rising edge of clk_{comp} as logic '1' ($V_{P_h}[2]$-$V_{N_h}[2]$>0) or logic '0' ($V_{P_h}[2]$-$V_{N_h}[2]$<0) using SAR controller. Once b_3 is resolved, its decision is fed back to the fine DAC and i increments to three. Moreover, capacitors of coarse DAC will hold their states and the fine DAC will start the conversion process using MCS scheme described in chapter 2 Section 2.1 by taking voltages $V_{P_h}[2]$ and $V_{N_h}[2]$ (in (3.5)) as the input voltages. Depending upon the state of b_3, the bottom plate of the highest capacitors in the MCS DAC arrays ($4C_{u,mcs}$) switch from V_{CM} to either ground level or $V_{REF,LSB}$, while the bottom plates of the remaining capacitors are held at V_{CM}. It should be noted that the equations derived for MCS DAC in Chapter 2 Section 2.1 ((2.3) and (2.4)) cannot be directly used in the hybrid DAC for deriving V_{P_h} and V_{N_h} of the fine DAC. This is because the total capacitance of the coarse DAC, which is connected between the two inputs of the comparator, provides coupling between the top and bottom arrays of the MCS fine DAC as

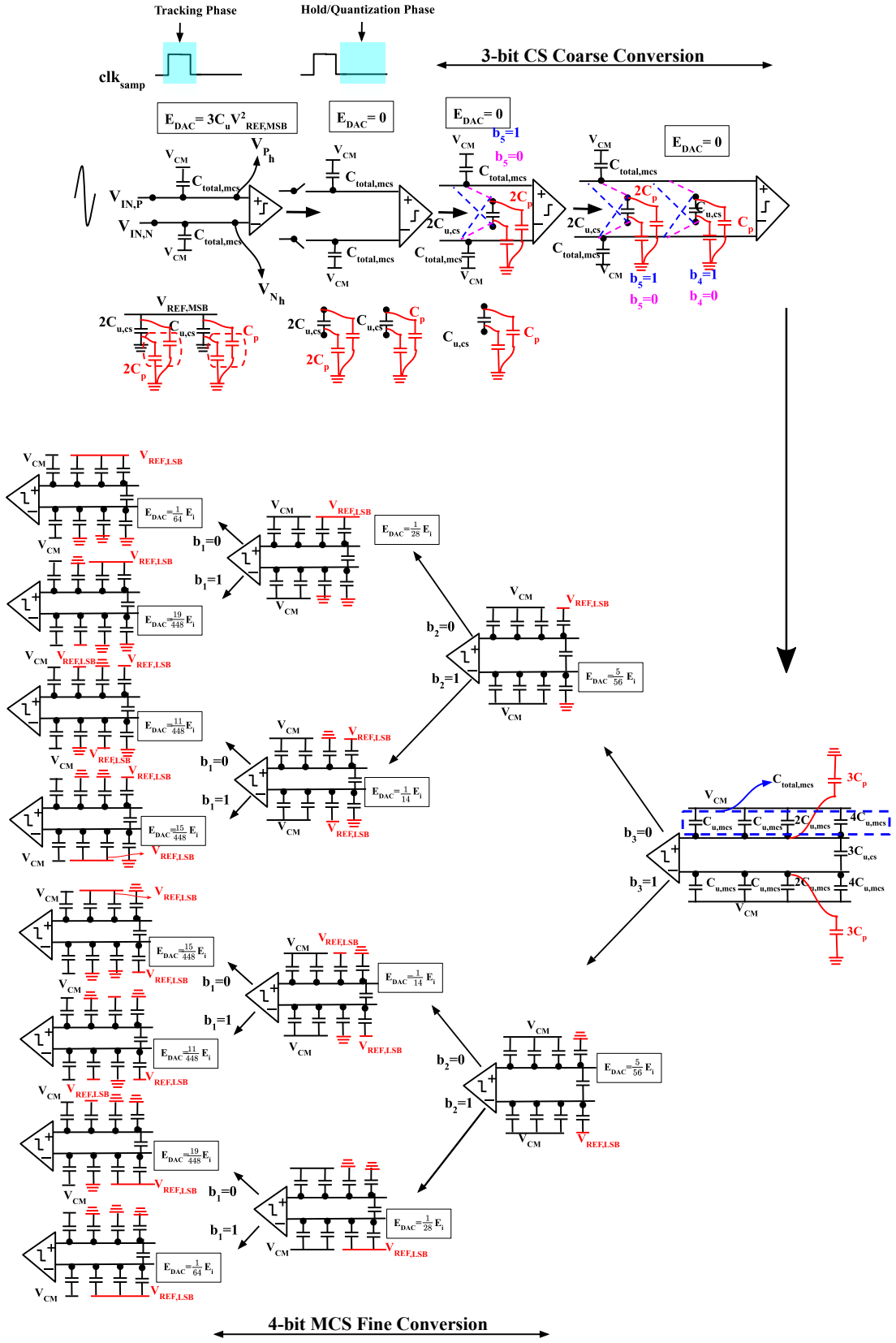


Figure 3.2: Conversion procedure of 6-bit CS coarse-MCS fine hybrid DAC based SAR ADC.

shown in Figure 3.2. As a result, the voltages at the input of the comparator are computed using superposition theorem and charge-redistribution scheme, and they are summarised in (3.7).

$$\begin{aligned} V_{P_h}[3] = V_{P_h}[2] - \left(1 - \frac{4C_{u,mcs}(1+C_{cc_2})}{C_{total,mcs}+C_{p,tot}+C_{cc_1}}\right)V_{CM} \\ + \left(\frac{4C_{u,mcs}\big(1-b_3(1-C_{cc_2})\big)}{C_{total,mcs}+C_{cc_1}}\right)V_{REF,LSB} \\ V_{N_h}[3] = V_{N_h}[2] - \left(1 - \frac{4C_{u,mcs}(1+C_{cc_2})}{C_{total,mcs}+C_{p,tot}+C_{cc_1}}\right)V_{CM} \\ + \left(\frac{4C_{u,mcs}\big(C_{cc_2}+b_3(1-C_{cc_2})\big)}{C_{total,mcs}+C_{cc_1}}\right)V_{REF,LSB} \end{aligned} \tag{3.7}$$

where,

$$\begin{aligned} \mathrm{C}_{cc_1} &= \frac{(2^{(x-1)}-1)C_{u,cs}C_{total,mcs}}{(2^{(x-1)}-1)C_{u,cs}+C_{total,mcs}} = \frac{3C_{u,cs}C_{total,mcs}}{3C_{u,cs}+C_{total,mcs}}, \\ \mathrm{C}_{cc_2} &= \frac{(2^{(x-1)}-1)C_{u,cs}}{(2^{(x-1)}-1)C_{u,cs}+C_{total,mcs}} = \frac{3C_{u,cs}}{3C_{u,cs}+C_{total,mcs}} \end{aligned} \tag{3.8}$$

It should be noted that the values of C_{cc_1} and C_{cc_2} depends only on the total DAC sizes of coarse and fine DAC, which remain constant throughout the conversion process. Again, the comparator compares the voltages at its input on the arrival of the fourth rising edge of clk_{comp} and resolves b_2 as logic '1' ($V_{P_h}[3] - V_{N_h}[3] > 0$) or logic '0' ($V_{P_h}[3] - V_{N_h}[3] < 0$) using SAR controller. Once b_2 is resolved, i increments to four and the decision on b_2 is fed back to the fine DAC. Depending upon its state, the bottom plate of $2C_{u,mcs}$ in the fine DAC arrays switch from V_{CM} to either ground level or $V_{REF,LSB}$, while the bottom plates of the remaining capacitors are held at V_{CM}. Moreover, capacitors $4C_{u,mcs}$ in DAC arrays hold their state. As a result, the voltages at the input of the comparator are computed, and they are given by:

$$V_{P_h}[4] = V_{P_h}[2] - \left(1 - \frac{2C_{u,mcs}(1+C_{cc_2})}{C_{total,mcs}+C_{cc_1}}\right)V_{CM} +$$

$$\frac{\left\{\begin{array}{l} 4C_{u,mcs}\big(1-b_3(1-C_{cc_2})\big)+ \\ \quad 2C_{u,mcs}\big(1-b_2(1-C_{cc_2})\big) \end{array}\right\}}{C_{total,mcs}+C_{cc_1}}V_{REF,LSB}$$

$$V_{N_h}[4]=V_{N_h}[2]-\left(1-\frac{2C_{u,mcs}(1+C_{cc_2})}{C_{total,mcs}+C_{cc_1}}\right)V_{CM}+ \frac{\left\{\begin{array}{l} 4C_{u,mcs}\big(C_{cc_2}+b_3(1-C_{cc_2})\big)+ \\ \quad 2C_{u,mcs}\big(C_{cc_2}+b_2(1-C_{cc_2})\big) \end{array}\right\}}{C_{total,mcs}+C_{cc_1}}V_{REF,LSB} \tag{3.9}$$

Again, the comparator compares the voltages at its input on the arrival of the fifth rising edge of clk_{comp} and resolves b_1 as logic '1' ($V_{P_h}[4]-V_{N_h}[4]>0$) or logic '0' ($V_{P_h}[4]-V_{N_h}[4]<0$) using SAR controller. Once b_1 is resolved, i increments to five and the decision on b_1 is fed back to the fine DAC. Depending upon its state, the bottom plates of $C_{u,mcs}$ in the fine DAC arrays switch from V_{CM} to either ground level or $V_{REF,LSB}$, while the bottom plates of the remaining capacitors are held at V_{CM}. Moreover, capacitors $4C_{u,mcs}$ and $2C_{u,mcs}$ in DAC arrays hold their state. As a result, the voltages at the input of the comparator are computed, and they are given by:

$$\begin{aligned} V_{P_h}[5]&=V_{P_h}[2]-\left(1-\frac{C_{u,mcs}(1+C_{cc_2})}{C_{total,mcs}+C_{cc_1}}\right)V_{CM}+ \frac{\left\{\begin{array}{l} 4C_{u,mcs}\big(1-b_3(1-C_{cc_2})\big)+ \\ \quad 2C_{u,mcs}\big(1-b_2(1-C_{cc_2})\big) \\ \quad\quad C_{u,mcs}\big(1-b_1(1-C_{cc_2})\big) \end{array}\right\}}{C_{total,mcs}+C_{cc_1}}V_{REF,LSB}, \\ V_{N_h}[5]&=V_{N_h}[2]-\left(1-\frac{C_{u,mcs}(1+C_{cc_2})}{C_{total,mcs}+C_{cc_1}}\right)V_{CM}+ \frac{\left\{\begin{array}{l} 4C_{u,mcs}\big(C_{cc_2}+b_3(1-C_{cc_2})\big)+ \\ \quad 2C_{u,mcs}\big(C_{cc_2}+b_2(1-C_{cc_2})\big) \\ \quad\quad C_{u,mcs}\big(C_{cc_2}+b_1(1-C_{cc_2})\big) \end{array}\right\}}{C_{total,mcs}+C_{cc_1}}V_{REF,LSB}, \end{aligned} \tag{3.10}$$

Finally, the comparator compares the voltages at its input on the arrival of the sixth rising edge of clk_{comp} and resolves b_0 as logic '1' ($V_{P_h}[5]-V_{N_h}[5]>0$)

or logic '0' ($V_{P_h}[5] - V_{N_h}[5] < 0$) using SAR controller. Once b_0 is resolved, i is reset to zero on the arrival of next rising edge of clk_{samp} and the complete process is repeated for next sampled voltage.

The switching energy of the hybrid DAC for 6-bit (x=3 and y=4) resolution is calculated, and it is shown in Figure 3.2. It should be noted that this energy depends on the reference voltages, resolution and the ratio of the unit capacitors of the coarse and fine DAC. Since x=3 and y=4, from (3.3), $C_{u,mcs}$=$C_{u,cs}$ (ignoring the effect of C_p). As a result, the energy is calculated in terms of C_u ($C_{u,mcs}$=$C_{u,cs}$=C_u) using the method described in [70] and equations (3.7), (3.1.1), (3.9), (3.10). In addition, V_{CM} is considered to be exactly half of $V_{REF,LSB}$. Since, $V_{REF,LSB}$ ($= \frac{V_{REF,MSB}}{4}$) is the scaled version of $V_{REF,MSB}$, the switching energy for each step in the fine DAC is calculated in terms of $V_{REF,MSB}$. Here, E_i is equal to $C_u V_{REF,MSB}^2$.

The above method is described for a 6-bit hybrid DAC SAR ADC and it can be easily extended to n-bit resolution by repeating the process n times before the next cycle of clk_{samp}. Therefore, the voltages at the input of the comparator during any cycle i (an integer, where $0 \leq i < n$) for n-bit (x-bit coarse and y-bit fine DAC) hybrid DAC SAR ADC with CS coarse and MCS fine DAC are given by (3.11) and (3.12).

$$V_{P_h}[i] = \begin{cases} V_{IN,P} & \text{for } i = 0 \\ -\dfrac{\left\{ \begin{array}{l} \sum_{j=1}^{i} C_{x-j-1}\Big[C_{total,mcs}V_{IN,N}+ \\ \quad \sum_{j=1}^{i}\Big(B_{n-j}C_{x-j-1}+b_{n-j}C_{p,x-j-1}\Big)V_{REF,MSB}\Big] \\ \qquad + C_{tot}\Big[C_{total,mcs}V_{IN,P}- \\ \quad \sum_{j=1}^{i}\Big(B_{n-j}C_{x-j-1}+(b_{n-j}-1)C_{p,x-j-1}\Big)V_{REF,MSB}\Big] \end{array} \right\}}{\Big(\sum_{j=1}^{i} C_{x-j-1}\Big)^2 - C_{tot}^2}, & \text{for } 0 < i \leq (x-1) \\ V_{P_h}[x-1] - \left(1 - \dfrac{(C_{total,mcs} - \sum_{j=x}^{i} C'_{n-j-1})(1+C_{cc_2})}{C_{total,mcs}+C_{cc_1}}\right)V_{CM}+ \\ \qquad \dfrac{\sum_{j=x}^{i}\big((1-b_{n-j})C'_{n-j-1}+b_{n-j}C_{cc_2}C'_{n-j-1}\big)}{C_{total,mcs}+C_{cc_1}}V_{REF,LSB}, & \text{for } x \leq i < n \end{cases} \tag{3.11}$$

$$V_{N_h}[i] = \begin{cases} V_{IN,N} & \text{for } i = 0 \\ -\dfrac{\left\{ \begin{array}{l} \sum_{j=1}^{i} C_{x-j-1}\Big[C_{total,mcs}V_{IN,P}- \\ \quad \sum_{j=1}^{i}\Big(B_{n-j}C_{x-j-1} + (b_{n-j}-1)C_{p,x-j-1}\Big)V_{REF,MSB}\Big] \\ \qquad + C_{tot}\Big[C_{total,mcs}V_{IN,N}+ \\ \quad \sum_{j=1}^{i}\Big(B_{n-j}C_{x-j-1} + b_{n-j}C_{p,x-j-1}\Big)V_{REF,MSB}\Big] \end{array} \right\}}{\Big(\sum_{j=1}^{i} C_{x-j-1}\Big)^2 - C_{tot}^2}, & \text{for } 0 < i \leq (x-1) \\ V_{N_h}[x-1] - \left(1 - \dfrac{(C_{total,mcs} - \sum_{j=x}^{i} C'_{n-j-1})(1+C_{cc_2})}{C_{total,mcs}+C_{cc_1}}\right)V_{CM}+ \\ \qquad \dfrac{\sum_{j=x}^{i}\left(b_{n-j}C'_{n-j-1} + (1-b_{n-j})C_{cc_2}C'_{n-j-1}\right)}{C_{total,mcs}+C_{cc_1}}V_{REF,LSB}, & \text{for } x \leq i < n \end{cases} \tag{3.12}$$

where,

$$\begin{aligned} &C_{x-j-1} = 2^{x-j-1}C_{u,cs}, \quad C_{p,x-j-1} = 2^{x-j-1}C_p, \quad B_{n-j} = 2b_{n-j} - 1, \\ &C_{tot} = C_{total,mcs} + \sum_{j=1}^{i}(C_{x-j-1} + C_{p,x-j-1}), \quad C'_{n-j-1} = 2^{n-j-1}C_{u,mcs} \end{aligned} \tag{3.13}$$

It should be noted that the values of C_{cc_1} and C_{cc_2} are the same as the one given in (3.1.1).

To validate the design equations derived in this section, behavioral simulations of a 10-bit (x=5 and y=6) hybrid DAC based SAR ADC have been performed

using equations (3.11) and (3.12) for fixed input voltages ignoring the effect of parasitics. The values of $V_{REF,MSB}$, $V_{IN,P}$ and $V_{IN,N}$ have been taken as 1V, 0.9V and 0.1V, respectively for the simulations. The conversion waveform of the SAR ADC with CS coarse and MCS fine hybrid DAC is shown in Figure 3.3, which shows equivalent digital bits corresponding to the sampled input voltage. Next, using the input ramp signal, the transfer characteristic of the ADC has been obtained using the derived design equations, and the result is shown in Figure 3.4. It can be observed from the figure that the transfer characteristic of the ADC is linear and monotonic, with zero Differential nonlinearity (DNL) and Integral nonlinearity (INL) errors, thus showing no missing codes and correct operation of the ADC.

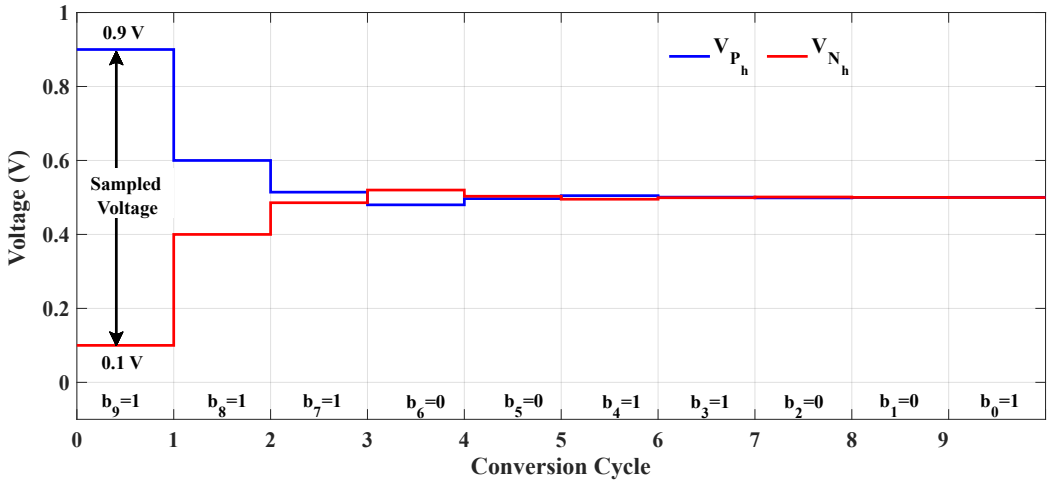


Figure 3.3: Conversion waveform of 10-bit CS-MCS hybrid DAC SAR ADC.

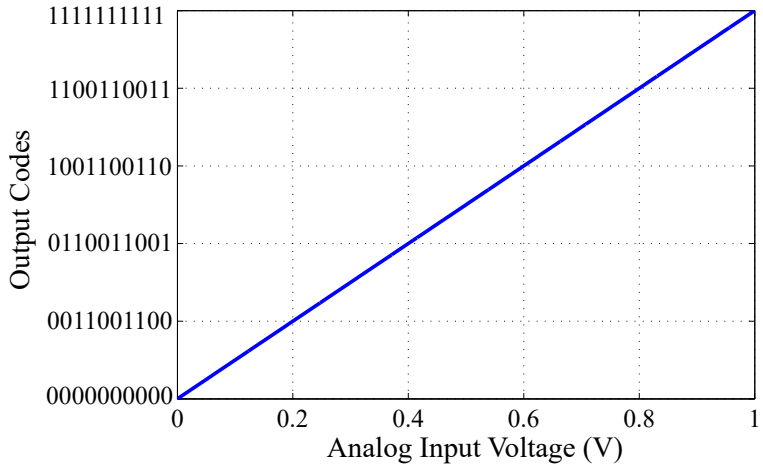


Figure 3.4: Transfer plot of the 10-bit CS-MCS hybrid DAC based SAR ADC with ramp as input.

3.1.2 MCS coarse and CS fine hybrid DAC

The schematic of the SAR ADC with MCS coarse and CS fine DAC is shown in Figure 3.6. Similar to the previously described architecture, x-bits and y-bits are allocated to coarse and fine DAC, respectively. Moreover, for this architecture also $C_{total,mcs}$ (=$2^{x-1}C_{u,mcs}$) mimics as C_{TH} for the CS (fine) DAC. As a result, x and y interchange their place in equation (3.3) for this architecture. Similar to the previous architecture, the matching between the two DACs has been achieved using two different reference voltages: one for coarse ($V_{REF,MSB}$) and the other for fine DAC ($V_{REF,LSB}$), where $V_{REF,LSB}$ is obtained from $V_{REF,MSB}$ using (3.4). However, n in (3.4) will now represent the n-bit CS DAC rather than MCS DAC.

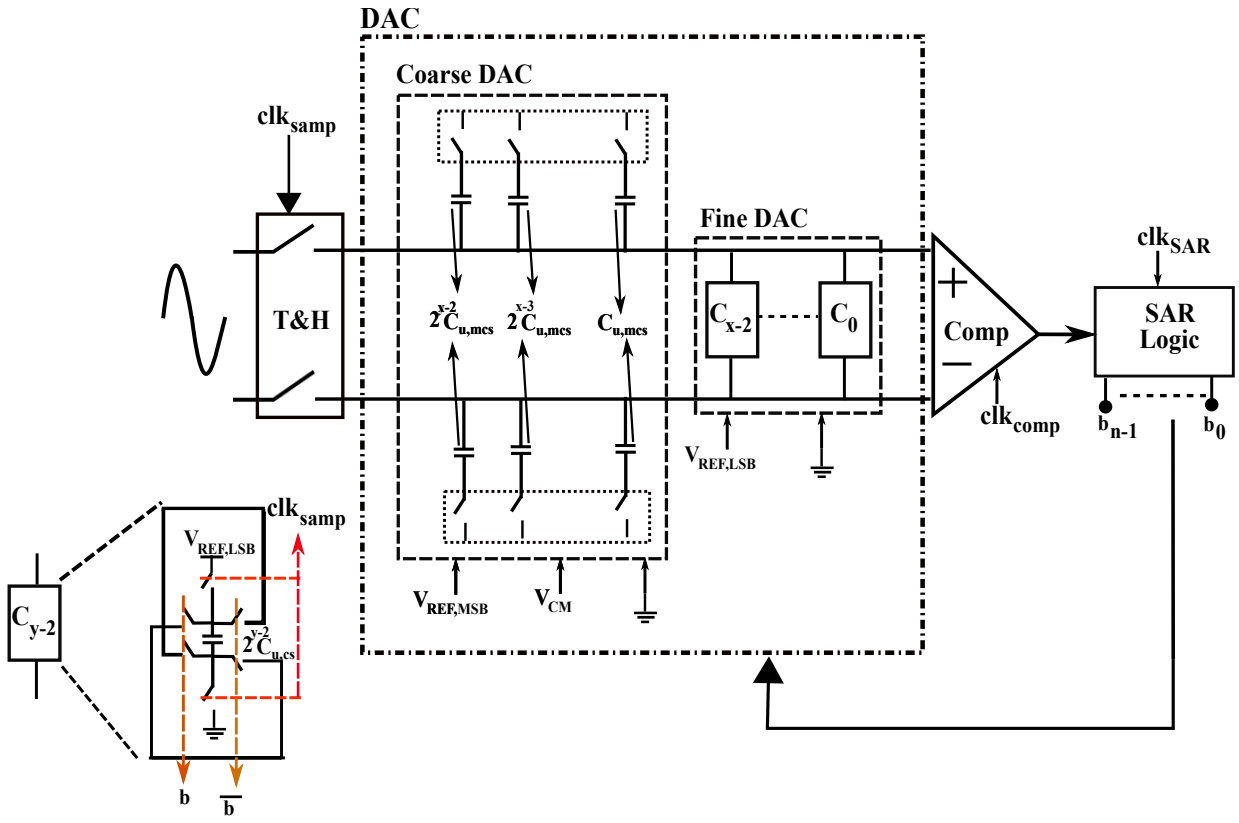


Figure 3.5: Block Diagram of a n-bit MCS coarse-CS fine Hybrid DAC SAR ADC.

The operation of the SAR ADC with MCS coarse and CS fine DAC is also explained using a 6-bit SAR ADC with a 4-bit coarse MCS DAC and 3-bit fine CS DAC, and the schematic of the conversion process is shown in Figure 3.6. The output bits of the ADC are represented as b_0, b_1, b_2, b_3, b_4 and b_5, where b_5 is the MSB. When clk_{samp} makes a transition from logic '0' to logic '1', the top plates

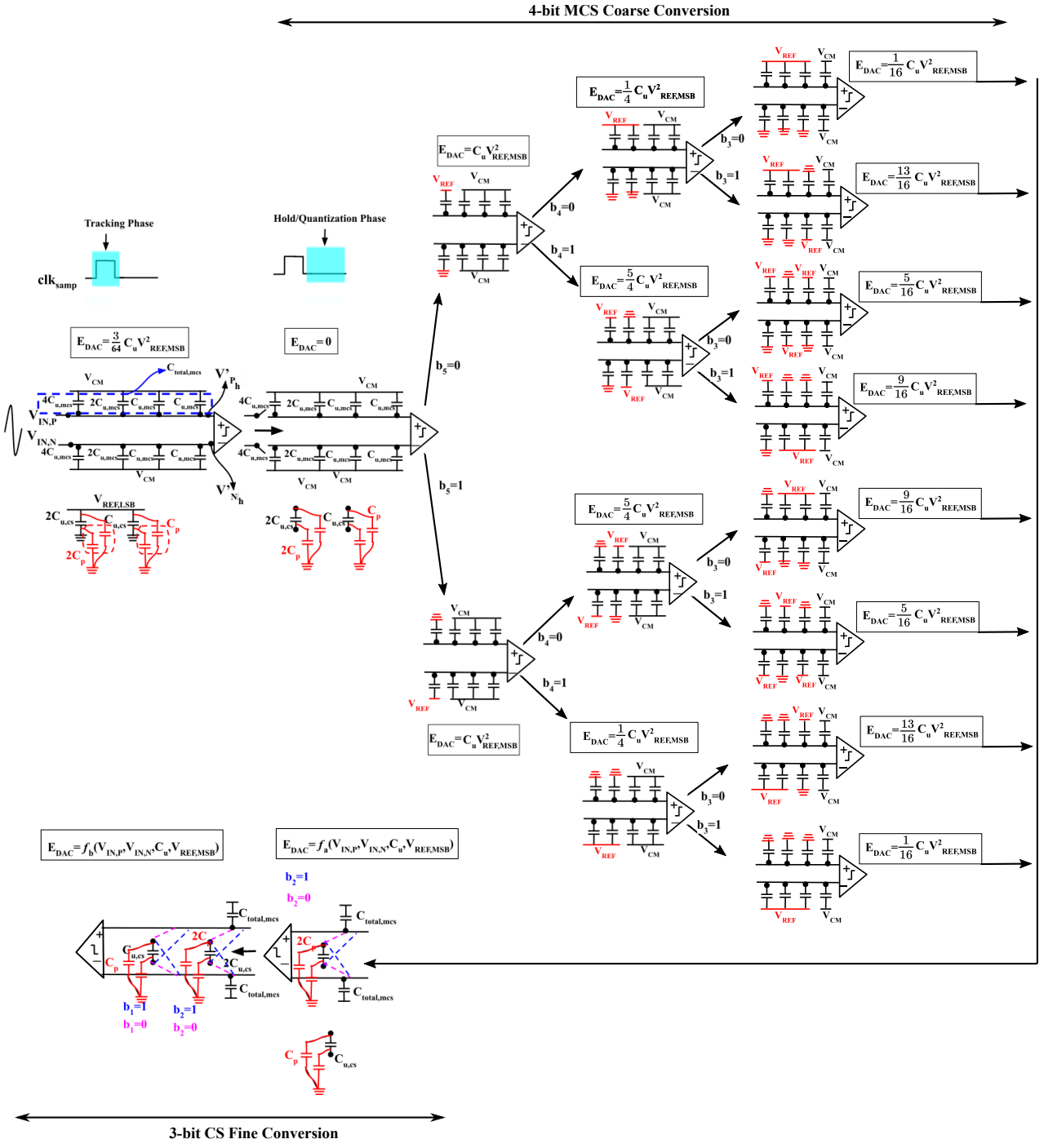


Figure 3.6: Conversion procedure of 6-bit MCS coarse-CS fine hybrid DAC SAR ADC.

of the capacitors in the coarse DAC track the differential analog input voltage ($V_{IN,P}$ and $V_{IN,N}$) while their bottom plates are connected to V_{CM} (=$\frac{V_{REF,MSB}}{2}$). Moreover, the capacitors of the fine DAC are pre-charged to $V_{REF,LSB}$. Next, when clk_{samp} makes a transition from logic '1' to logic '0', the conversion begins by the coarse DAC with MCS switching principle for four MSBs (b_5, b_4, b_3 and b_2). It should be noted that while the coarse DAC is performing the conversion process, the capacitors of the fine DAC are neither connected to $V_{REF,LSB}$ nor connected between the inputs of the comparator. As a result, unlike the previous architecture, no coupling between the two inputs of the comparator is observed, and the equations presented in Chapter 2 Section 2.1 can be directly used in this architecture. Therefore, the voltages at the input of the comparator (V'_{P_h} and V'_{N_h}), after resolving three MSBs (b_5, b_4, b_3) using MCS switching principle in three rising edges of the clk_{comp} and at the end of cycle i=3, are given by (3.14).

$$V'_{P_h}[3] = V_{IN,P} - \left(1 - \frac{C_{u,mcs}}{C_{total,mcs}}\right)V_{CM} + \frac{\Big(4(1-b_5) + 2(1-b_4) + (1-b_3)\Big)C_{u,mcs}}{C_{total,mcs}}V_{REF,MSB}$$

$$V'_{N_h}[3] = V_{IN,N} - \left(1 - \frac{C_{u,mcs}}{C_{total,mcs}}\right)V_{CM} + \frac{(4b_5 + 2b_4 + b_3)C_{u,mcs}}{C_{total,mcs}}V_{REF,MSB} \tag{3.14}$$

The coarse DAC resolves its LSB (b_2) on the arrival of the fourth rising edge of clk_{comp} as logic '1' ($V'_{P_h}[3]$-$V'_{N_h}[3]$>0) or logic '0' ($V'_{P_h}[3]$-$V'_{N_h}[3]$<0) using SAR controller. Once b_2 is resolved, its decision is fed back to the fine DAC and i increments to four. Moreover, capacitors of coarse DAC will hold their states and the fine DAC will start the conversion process using CS scheme described in chapter 2 section 2.2 by taking voltages $V'_{P_h}[3]$ and $V'_{N_h}[3]$ (in (3.14)) as the input voltages. Depending upon the state of b_4, the highest capacitor in the fine DAC ($2C_{u,cs}$) connects parallel (b_2=0) or anti-parallel (b_2=1) to $C_{total,mcs}$. Using the charge equations ((2.11) to (2.14)) presented in chapter 2 section 2.2 for a 3-bit CS SAR ADC, the voltages at the input of the comparator are computed and are given by (3.1.2).

$$V'_{P_h}[4] = -\frac{\left\{\begin{array}{l} 2C_{u,cs}\Big[C_{total,mcs}V_{N_h}[3] + \Big((2b_2-1)2C_{u,cs} + b_2 2C_p\Big) \\ \qquad V_{REF,LSB}\Big] + \Big(C_{total,mcs} + 2C_{pu,cs}\Big)\Big[C_{total,msc}V_{P_h} - \\ \qquad\qquad \Big((2b_2-1)2C_{u,cs} + (b_2-1)2C_p\Big)V_{REF,LSB}\Big] \end{array}\right\}}{(2C_{u,cs})^2 - (C_{total,mcs} + 2C_{pu,cs})^2},$$

$$\mathrm{V}'_{N_h}[4] = -\frac{\left\{\begin{array}{l} 2C_{u,cs}\Big[C_{total,mcs}V_{P_h}[3] - \Big((2b_2-1)2C_{u,cs} + (b_2-1)2C_p\Big) \\ \qquad V_{REF,LSB}\Big] + \Big(C_{total} + 2C_{pu,cs}\Big)\Big[C_{total,mcs}V_{N_h}[3] + \\ \qquad\qquad \Big((2b_2-1)2C_{u,cs} + b_2 2C_p\Big)V_{REF,LSB}\Big] \end{array}\right\}}{(2C_{u,cs})^2 - (C_{total,mcs} + 2C_{pu,cs})^2} \tag{3.15}$$

The comparator compares the voltages at its input on the arrival of the fifth rising edge of clk_{comp} and resolves b_1 as logic '1' ($V'_{P_h}[4] - V'_{N_h}[4] > 0$) or logic '0' ($V'_{P_h}[4] - V'_{N_h}[4] < 0$) using SAR controller. Once b_1 is resolved, i increments to five and the decision on b_1 is fed back to the fine DAC. Depending upon its state, $C_{u,cs}$ in the fine DAC connects parallel (b_1=0) or anti-parallel (b_1=1) to $C_{total,mcs}$. Again, using the charge equations ((2.11) and (2.16) to (2.20)) presented in Chapter 2 section 2.2 for a 3-bit CS SAR ADC, the voltages at the input of the comparator are given by (3.16).

$$V'_{P_h}[5] = -\frac{\left\{\begin{array}{l} (2C_{u,cs} + C_{u,cs})\Big[C_{total,mcs}V_{N_h}[3] + \Big((2b_2-1)2C_{u,cs} + \\ \qquad b_2 2C_p + (2b_1-1)C_{u,cs} + b_1 C_p\Big)V_{REF,LSB}\Big] \end{array}\right\}}{(2C_{u,cs} + C_{u,cs})^2 - (C_{total,mcs} + 2C_{pu,cs} + C_{pu,cs})^2}$$
$$- \frac{\left\{\begin{array}{l} \Big(C_{total,mcs} + 2C_{pu,cs} + C_{pu,cs}\Big)\Big[C_{total,mcs}V_{P_h}[3] - \Big((2b_2-1)2C_{u,cs} \\ \qquad + (b_2-1)2C_p + (2b_1-1)C_{u,cs} + (b_1-1)2C_p\Big)V_{REF,LSB}\Big] \end{array}\right\}}{(2C_{u,cs} + C_{u,cs})^2 - (C_{total,mcs} + 2C_{pu,cs} + C_{pu,cs})^2}$$

$$V'_{N_h}[5] = -\frac{\left\{\begin{array}{l}(2C_{u,cs}+C_{u,cs})\Big[C_{total,mcs}V_{P_h}[3]-\Big((2b_2-1)2C_{u,cs}+\\ \quad (b_2-1)2C_p+(2b_1-1)C_{u,cs}+(b_1-1)C_p\Big)V_{REF,LSB}\Big]\end{array}\right\}}{(2C_{u,cs}+C_{u,cs})^2-(C_{total,mcs}+2C_{pu,cs}+C_{pu,cs})^2}$$
$$-\frac{\left\{\begin{array}{l}\Big(C_{total,mcs}+2C_{u,cs}+2C_p+C_{u,cs}+C_p\Big)\Big[C_{total,mcs}V_{N_h}[3]\\ \quad +\Big((2b_2-1)2C_{u,cs}+b_2 2C_p+(2b_1-1)C_{u,cs}+b_1C_p\Big)V_{REF,LSB}\Big]\end{array}\right\}}{(2C_{u,cs}+C_{u,cs})^2-(C_{total,mcs}+2C_{pu,cs}+C_{pu,cs})^2} \tag{3.16}$$

Finally, the comparator resolves b_0 on the arrival of the sixth rising edge of clk_{comp} as logic '1' ($V'_{P_h}[5]-V'_{N_h}[5]>0$) or logic '0' ($V'_{P_h}[5]-V'_{N_h}[5]<0$) using SAR controller. Once b_0 is resolved, i is reset to zero on the arrival of next rising edge of clk_{samp} and the complete process is repeated for next sampled voltage.

The above method is described for a 6-bit hybrid DAC SAR ADC, and it can be easily extended to n-bit resolution by repeating the process n times before the next cycle of clk_{samp}. Therefore, the voltages at the input of the comparator during any cycle i (an integer, where $0 \leq i < n$) for n-bit (x-bit coarse and y-bit fine DAC) hybrid DAC SAR ADC with MCS coarse and CS fine DAC are given by (3.17) and (3.18).

$$V'_{P_h}[i] = \begin{cases} V_{IN,P} & \text{for } i = 0 \\ V_{IN,P} - \left(1 - \dfrac{(C_{total,mcs} - \sum_{j=1}^{i} C'_{x-j-1})}{C_{total,mcs}}\right) V_{CM} \\ \quad + \dfrac{\sum_{j=x}^{i}(1-b_{n-j})C'_{x-j-1}}{C_{total,mcs}} V_{REF,MSB}, & \text{for } 0 < i \leq (x-1) \\ -\dfrac{\left\{ \begin{array}{l} \sum_{j=x}^{i} C_{n-j-1}\Big[C_{total,mcs}V_{N_h}[x-1]+ \\ \quad \sum_{j=x}^{i}\Big(B_{n-j}C_{n-j-1} + b_{n-j}C_{p,n-j-1}\Big)V_{REF,LSB}\Big]+ \\ \qquad C_{tot}\Big[C_{total,mcs}V_{P_h}[x-1]- \\ \quad \sum_{j=x}^{i}\Big(B_{n-j}C_{n-j-1} + (b_{n-j}-1)C_{p,n-j-1}\Big)V_{REF,LSB}\Big] \end{array} \right\}}{\Big(\sum_{j=x}^{i} C_{n-j-1}\Big)^2 - C_{tot}^2}, & \text{for } x \leq i < n \end{cases} \tag{3.17}$$

$$V'_{N_h}[i] = \begin{cases} V_{IN,N} & \text{for } i = 0 \\ V_{IN,N} - \left(1 - \frac{(C_{total,mcs} - \sum_{j=1}^{i} C'_{x-j-1})}{C_{total,mcs}}\right) V_{CM} + \\ \quad \frac{\sum_{j=x}^{i} b_{n-j} C'_{x-j-1}}{C_{total,mcs}} V_{REF,MSB}, & \text{for } 0 < i \leq (x-1) \\ -\frac{\left\{ \begin{array}{l} \sum_{j=x}^{i} C_{n-j-1} \Big[C_{total,mcs} V'_{P_h}[x-1] - \\ \quad \sum_{j=x}^{i} \Big(B_{n-j} C_{n-j-1} + (b_{n-j}-1) C_{p,n-j-1} \Big) V_{REF,LSB} \Big] + \\ \quad C_{tot} \Big[C_{total,mcs} V'_{N_h}[x-1] \\ \quad + \sum_{j=x}^{i} \Big(B_{n-j} C_{n-j-1} + b_{n-j} C_{p,n-j-1} \Big) V_{REF,LSB} \Big] \end{array} \right\}}{\Big(\sum_{j=x}^{i} C_{n-j-1} \Big)^2 - C_{tot}^2}, & \text{for } x \leq i < n \end{cases} \tag{3.18}$$

where,

$$C_{n-j-1} = 2^{n-j-1} C_{u,cs}, \quad C_{p,n-j-1} = 2^{n-j-1} C_p, \quad B_{n-j} = 2b_{n-j} - 1,$$
$$C_{tot} = C_{total,mcs} + \sum_{j=x}^{i} (C_{n-j-1} + C_{p,n-j-1}), \quad C'_{x-j-1} = 2^{x-j-1} C_{u,mcs} \tag{3.19}$$

The switching energy of the hybrid DAC for 6-bit (x=3 and y=4) resolution is calculated in terms of C_u ($C_{u,mcs}$=$C_{u,cs}$=C_u) using the method described in [70] and equations (3.14), (3.1.2), (3.16). In addition, C_p is considered negligible compared to C_u. Since, $V_{REF,LSB}$ ($= \frac{V_{REF,MSB}}{8}$) is the scaled version of $V_{REF,MSB}$, the switching energy is calculated in terms of $V_{REF,MSB}$. The

calculated energy is shown in Figure 3.6. It should be noted that during the coarse conversion, the calculated switching energy of the hybrid DAC at every switching action, is identical to that of a 4-bit MCS DAC. Now, let us consider the switching energy of the DAC when fine conversion is active. For a code (b_5, b_4, b_3, b_2)=$(0, 0, 0, 0)$, the calculated E_{DAC} is given by (3.20).

$$E_{DAC} = 7C_u V_{REF,MSB}\left(\frac{1}{6}(V_{IN,P} - V_{IN,N}) + \frac{1}{8}V_{REF,MSB}\right) \tag{3.20}$$

From (3.20), it is observed that E_{DAC} depends on differential input voltage ($V_{IN,P}$-$V_{IN,N}$) along-with C_u and $V_{REF,MSB}$. This is because during fine conversion, the DAC capacitors connect between the two inputs of the comparator and perform conversion passively using CS scheme. As a result, the voltages on the top plates of the capacitors in the coarse DAC change according to (3.16), where $V_{IN,P}$ and $V_{IN,N}$ are multiplied by the capacitor term, which changes each time the capacitor from the fine DAC connects between the inputs of the comparator. It should be noted that the dependence of E_{DAC} on $V_{IN,P}$-$V_{IN,N}$ is undesirable as the switching energy changes with the change in the input differential signal. Therefore, the E_{DAC} in Figure 3.6 is expressed as a function of $V_{IN,P}$, $V_{IN,N}$, C_u and $V_{REF,MSB}$ rather than expressing them in equations for fine conversion.

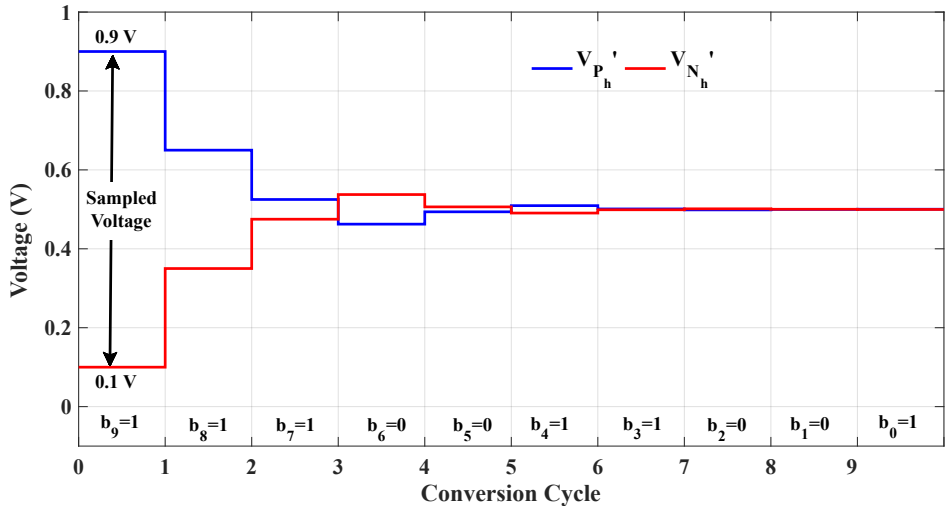


Figure 3.7: Conversion waveform of 10-bit MCS-CS hybrid DAC SAR ADC.

To validate the design equations derived in this sub-section, behavioral simulations of a 10-bit (x=6 and y=5) SAR ADC have been performed using equations (3.17) and (3.18) for fixed input voltages ignoring the effect of parasitics. The values of $V_{REF,MSB}$, $V_{IN,P}$ and $V_{IN,N}$ have been taken as 1V, 0.9V and 0.1V, respectively for the simulations. The conversion waveform of the SAR ADC

with MCS coarse and CS fine hybrid DAC is shown in Figure 3.7, which shows equivalent digital bits corresponding to the sampled input voltage. Next, using the input ramp signal, the transfer characteristic of the ADC has been obtained using the derived design equations, and the result is shown in Figure 3.8. It can be observed from the figure that the transfer characteristic of the ADC is linear and monotonic, with zero DNL and INL errors, thus showing no missing codes and correct operation of the ADC.

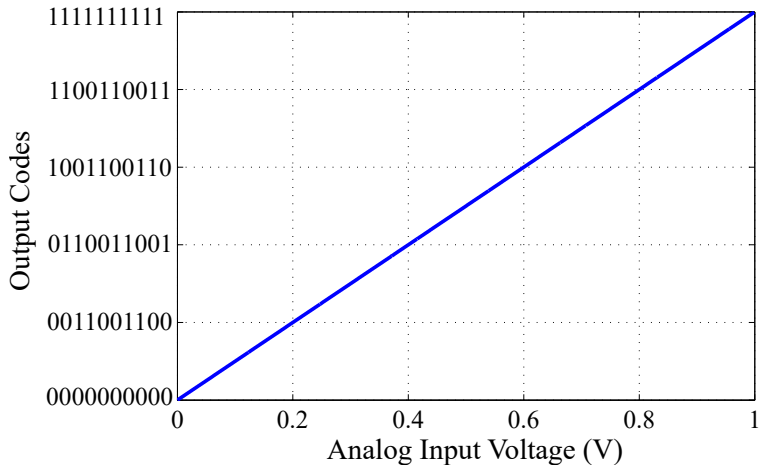


Figure 3.8: Transfer plot of the 10-bit MCS-CS hybrid DAC based SAR ADC with ramp as input.

3.1.3 Selection between the different Architectures

As discussed in the previous section, the hybrid DAC architectures employ two switching principles namely CS and MCS. It can be observed Chapter-2 Section 2.2, which describes the working principles of CS scheme, the total DAC capacitance connected between the inputs of the comparator is time-varying, *i.e.*, it corresponds to C_{TH} before the DAC conversion process begins and increases during the conversion process as the capacitors from the DAC array are connected successively. As a result, the voltage produced by the DAC is attenuated and the conversion becomes non-linear in the presence of comparator offset. Therefore, this switching scheme is more sensitive to comparator offset compared to the MCS switching scheme, where the DAC capacitance is not time varying. To study the impact of the comparator's offset (V_{OS}) on the performance of the two hybrid DAC based SAR ADCs, Differential-non-linearity (DNL) and Integral non-linearity (INL) of the DACs have been calculated as a function of V_{OS} using equations ((3.11), (3.12), (3.17), (3.18)) and method described in [71], and the

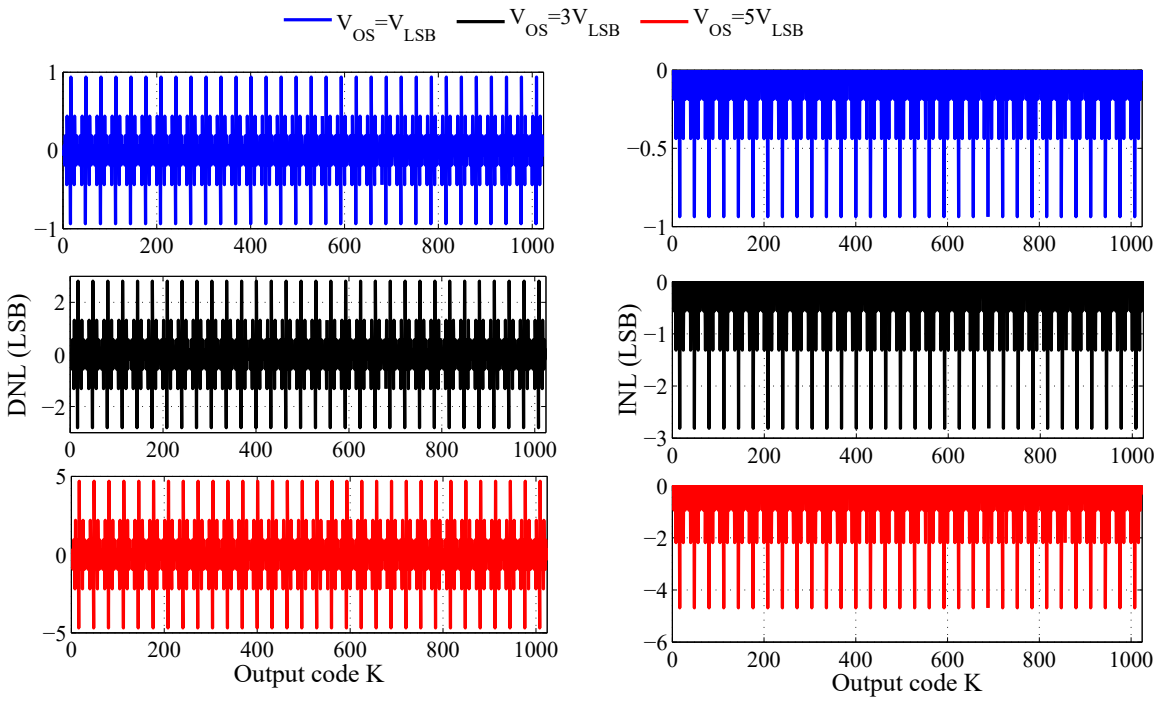


Figure 3.9: DNL and INL plots of 10-bit (6-bits MCS coarse and 5-bits CS fine) Hybrid DAC based SAR ADC for different values of V_{OS} .

plots are shown in Figure 3.9 and Figure 3.10. These plots are obtained for 10-bit hybrid DAC based SAR ADC and considering 5-bits to CS sub-DAC and 6-bits to MCS sub-DAC. Moreover, for simplification, the contribution due to the parasitics are considered negligible in comparison with DAC capacitance value. The V_{LSB} is the resolution of a 10-bit ADC. It can be observed from the figures that the hybrid DAC architecture with MCS as coarse and CS as fine DAC is more sensitive to comparator offset compared to the other design as its DNL and INL values are worst ($\geq$1) in the presence of large V_{OS}, which results in missing codes. The resolution of y-bit fine DAC is $\frac{V_{REF,LSB}}{2^y}$, where $V_{REF,LSB}$ is a scaled version of $V_{REF,MSB}$. Due to the scaled reference voltage, the resolution of the fine CS DAC is very small, which along with the time varying behavior of the DAC capacitance, degrades the performance of the ADC in the presence of V_{OS}. However, when the CS DAC is taken as the coarse DAC, its resolution is decided by the $V_{REF,MSB}$ and number of bits assigned to the coarse DAC. As a result, the attenuation caused by the time-varying behavior of the DAC capacitance will be negligible on the performance of the ADC until the resolution of the coarse CS DAC is greater than V_{LSB}. Therefore, we can conclude that when CS switching scheme is employed as coarse DAC in the hybrid DAC, then the architecture is less sensitive to V_{OS} compared to the architecture where it is employed in the

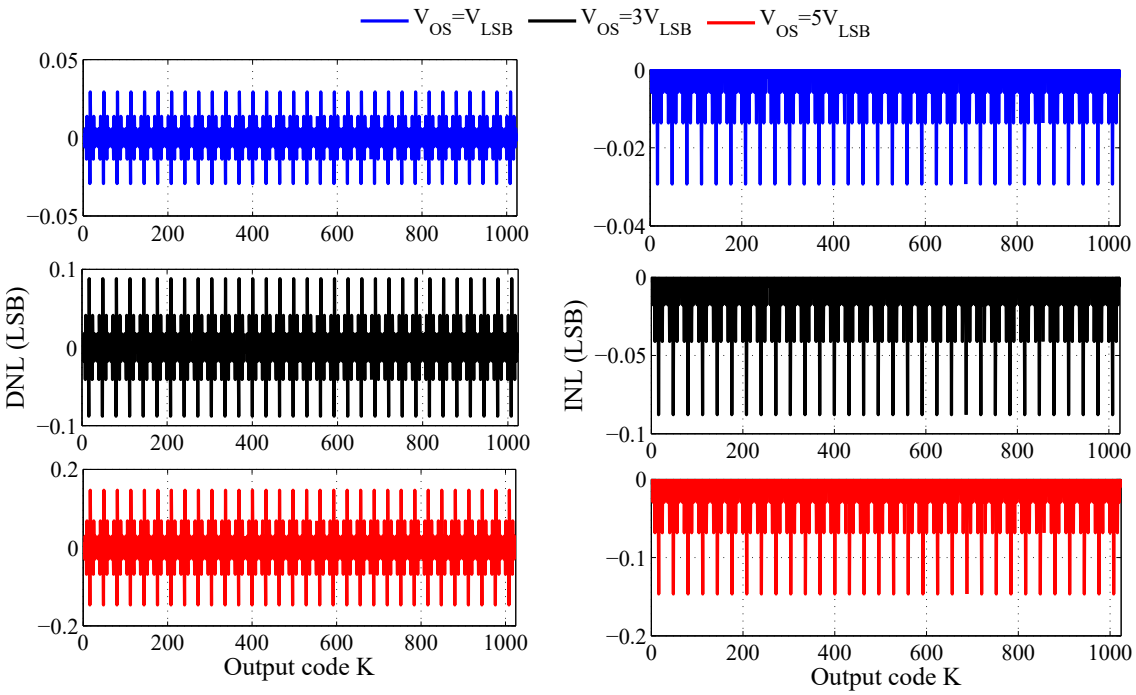


Figure 3.10: DNL and INL plots of 10-bit (5-bits CS coarse and 6-bits MCS fine) Hybrid DAC based SAR ADC for different values of V_{OS}.

fine DAC.

The above discussion is based on a single combination (6-bit MCS DAC and 5-bit CS DAC) of a 10- bit hybrid DAC based SAR ADC. In order to extend the analysis to different combinations, following equations are derived for n-bit hybrid DAC with x- bit CS and y-bit MCS sub-DACs. It should be noted that the following analysis is common to both the above discussed architectures. Considering C_p negligible compared to $C_{u,cs}$, (3.3) is modified as (3.21).

$$C_{u,mcs} = 2^{x-y+1} C_{u,cs} \tag{3.21}$$

Therefore, the relation between x and y in terms of $C_{u,cs}$ and $C_{u,mcs}$ is given by (3.22).

$$x - y = log_2\left(\frac{C_{u,mcs}}{C_{u,cs}}\right) - 1 \tag{3.22}$$

It should be noted that for a n bit resolution hybrid DAC SAR ADC, the relation between x and y is given by (3.1). Therefore, for $C_{u,mcs}$=$C_{u,cs}$, x and y in terms of n is given by (3.23) using equations (3.1) and (3.22)

$$x = \frac{n}{2} \quad and \quad y = \frac{n}{2} + 1 \tag{3.23}$$

It should be noted that for an *odd* value of n, x and y are fractional terms, which should not be the case as these two variables (x and y) represent the resolutions of the sub-DACs. Therefore, in such cases, the next (previous) positive integer close to the fractional value of x (y) should be selected. However, this will make $\frac{C_{u,mcs}}{C_{u,cs}} \neq 1$ for odd values of n. For example, if n = 9 and $C_{u,mcs}$ = $C_{u,cs}$, then x and y will be 4.5 and 5.5, respectively. If we select x as 5 (4) and y as 5 (6), then $C_{u,mcs}$ = $C_{u,cs}$ will no longer hold and the ratio $\frac{C_{u,mcs}}{C_{u,cs}}$ will be 2 (0.5) from (3.22). This has been the case when the unit capacitors of the coarse and fine DACs are considered to be same. On the other hand, the value of $C_{u,mcs}$ can be selected to be either greater or less than $C_{u,cs}$ (see (3.21) depending upon the requirements, and the values of x and y can be calculated. Alternatively, x and y can be selected to obtain the relation between $C_{u,mcs}$ and $C_{u,cs}$ using (3.21). The relation between $C_{u,mcs}$ and $C_{u,cs}$ for different combinations of x and y in a n (9 and 10) bit hybrid DAC is shown in Figure 3.11. In the figure, depending upon the values of x and y, either $C_{u,mcs}$ is a multiple of $C_{u,cs}$ or vice versa. As a result, the smallest out of these two ($C_{u,mcs}$ and $C_{u,cs}$) is represented as C_u and the other as multiple of C_u. For instance, say for n = 10 and $x : y$ = $3 : 8$, $C_{u,cs} = 16C_{u,mcs}$ (from 3.21). Therefore, $C_{u,mcs}$ is represented as C_u and $C_{u,cs}$ as $16C_u$. On the other hand, for n = 8 and $x : y = 8 : 3$, $C_{u,mcs} = 64C_{u,cs}$, and $C_{u,cs}$ is represented as C_u and $C_{u,mcs}$ as $64C_u$. It is observed from the figure that for $C_{u,mcs}$ = $C_{u,cs}$, combination of x and y exists only for even value of n (= 10) as explained before.

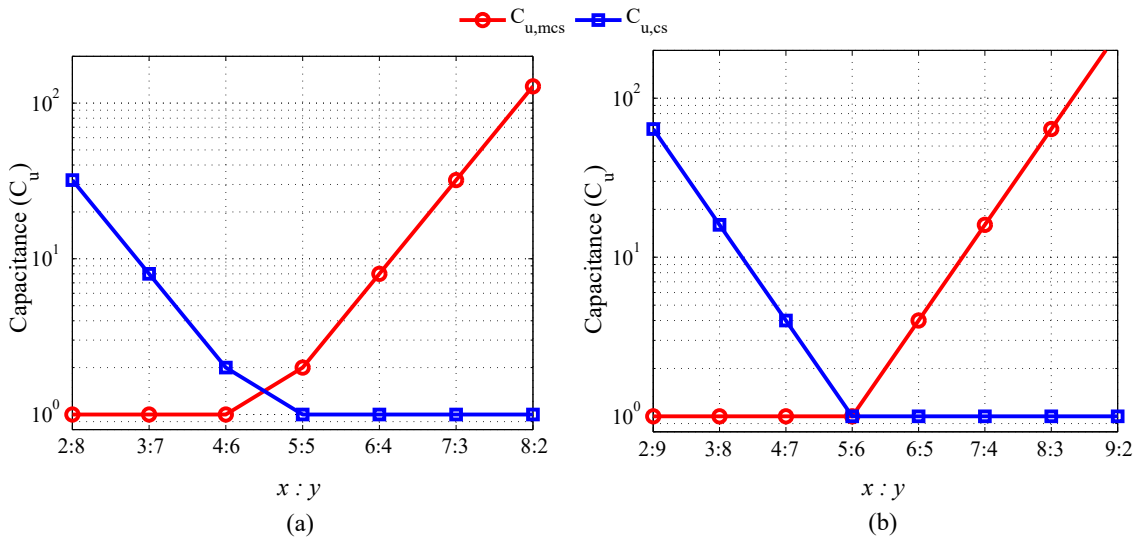


Figure 3.11: Relation between $C_{u,mcs}$ and $C_{u,cs}$ for different combinations of x and y in a n bit hybrid DAC (a) n = 9 (b) n = 10.

Following the above analysis, the DNL errors of the 10-bit hybrid DAC based SAR ADC have been calculated for CS coarse-MCS fine and MCS coarse-CS fine hybrid DACs for V_{OS}=V_{LSB}. The maximum value of the DNL errors (in LSB) are plotted for different combination of x and y and the plot is shown in Figure 3.12. It can be observed **from** the plot that as the number of bits allocated to CS sub-DAC (=x) decreases, the DNL errors reduces in both the architectures. However, still the architecture with CS coarse and MCS fine DAC is less sensitive to V_{OS} compared to the one with MCS as coarse and CS as fine. The performance of the two hybrid architectures are summarized in Table

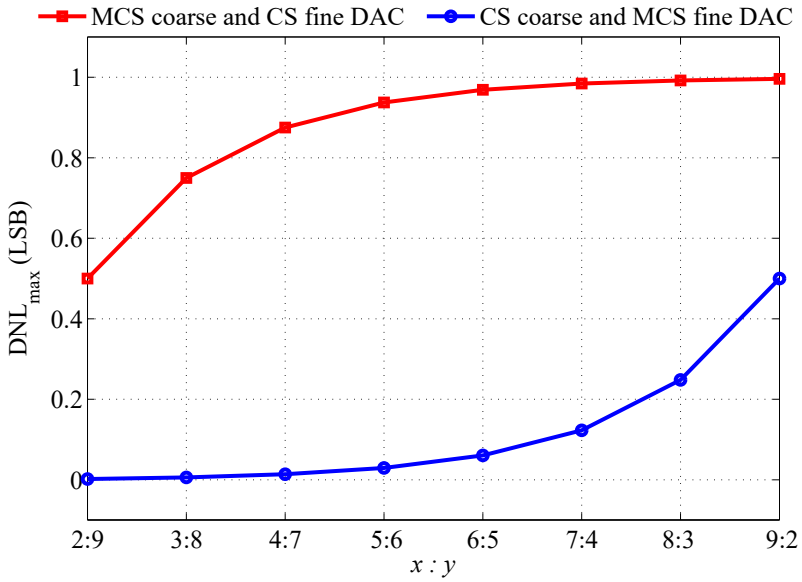


Figure 3.12: DNL plot of 10-bit Hybrid DAC based SAR ADC for different combinations of x and y.

Table 3.1: Performance comparison of two Hybrid DAC architectures

Metrics	**MCS (coarse) CS (fine)**	**CS (coarse) MCS (fine)**
Sensitivity to Comparator offset	High	Low
Worst INL	≥ 1	< 0.5
Worst DNL	≥ 1	< 0.5
Energy drawn from V_{REF}	Additional dependency on input sampled signal	Independent of input sampled signal

3.1. It can be observed from the table that the architecture with MCS coarse and CS fine DAC is more sensitive to V_{OS} and has a worst case INL and DNL $\geq$1, which results in missing codes. In addition, the energy drawn from V_{REF} by this architecture depends on the input sampled signal, which is undesirable.

Therefore, in this work we consider the hybrid DAC architecture with CS coarse and MCS fine sub-DAC as the final architecture for implementing the proposed hybrid DAC based SAR ADC.

3.2 Segmentation strategy of the Hybrid DAC

As discussed in the previous section, the performance of the MCS coarse and CS fine DAC is sensitive to V_{OS}. As a result, the architecture considered in this work for the implementation of the hybrid DAC based SAR ADC is the one with CS coarse and MCS fine hybrid DAC. The hybrid DAC employs two

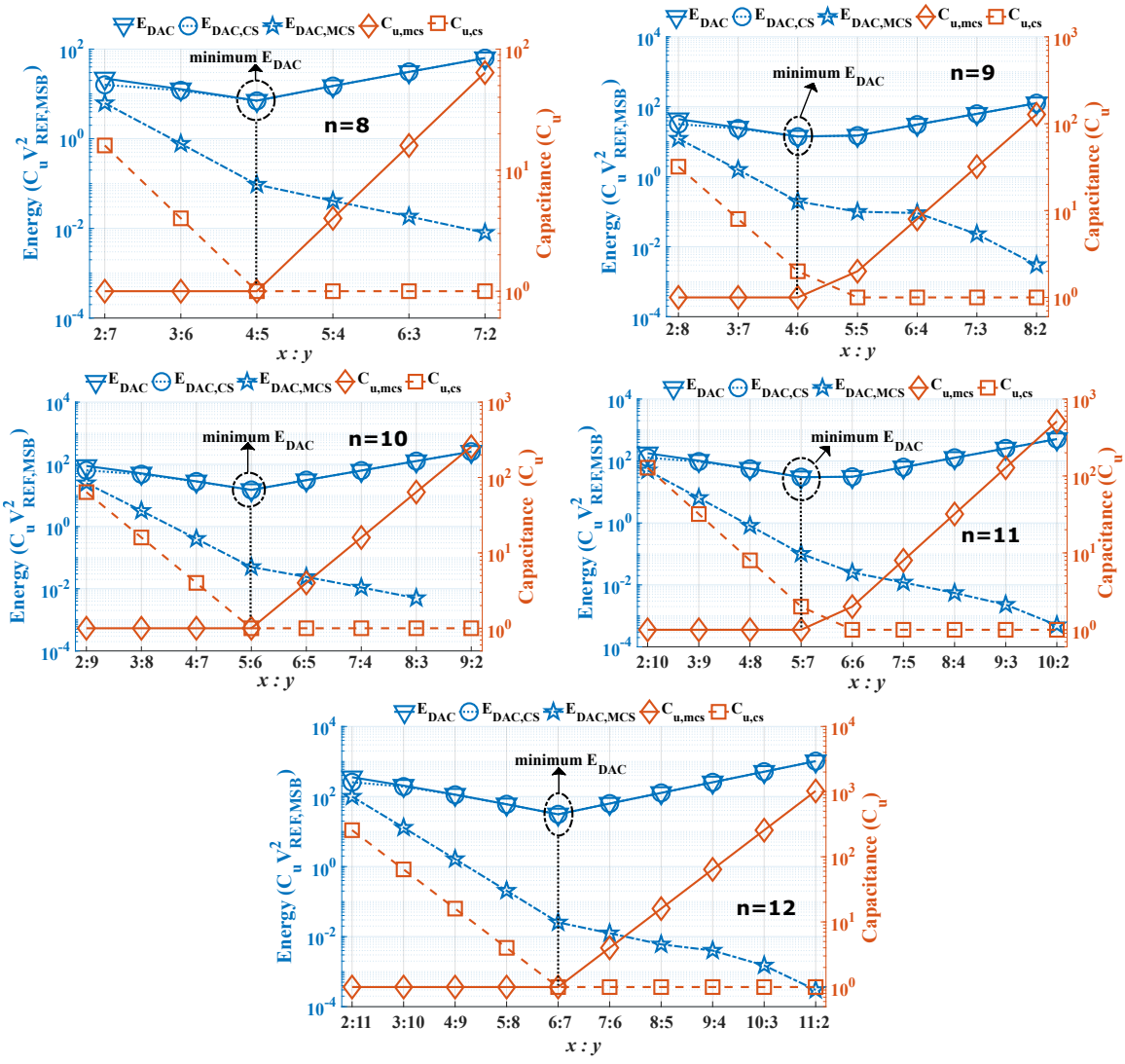


Figure 3.13: Calculated average value of E_{DAC} for different combinations of x and y in (x-bit CS coarse and y-bit MCS fine) n-bit hybrid DAC.

different sub-DACs (x-bits CS coarse and y-bits MCS fine DACs), which makes the division of bits between the two sub-DACs an important decision to design the hybrid DAC. From equations (3.3) and (3.4), it can be inferred that the number of bits allocated to each sub-DAC plays an important role in deciding the relation between $C_{u,cs}$ and $C_{u,mcs}$, and $V_{REF,MSB}$ and $V_{REF,LSB}$. Therefore, using equations (3.4), (3.10), (3.11) and (3.21), average switching energy of the hybrid DAC (E_{DAC}) with resolution (n) ranging from 8 to 12 bits have been calculated using behavioral simulations in terms of $V_{REF,MSB}$ (as $V_{REF,LSB}$ is a scaled version of $V_{REF,MSB}$ (3.4)) and C_u, for different combinations of x and y, and the results are presented in Figure 3.13. In the figure, E_{DAC} is the sum of the average switching energy of the coarse ($E_{DAC,CS}$) and fine ($E_{DAC,MCS}$) DACs. It is observed from the figure that E_{DAC} is almost equal to $E_{DAC,CS}$ as $E_{DAC,MCS}$ is very small compared to $E_{DAC,CS}$. As discussed previously, the reference voltage of the fine DAC ($V_{REF,LSB}$) is a scaled version of $V_{REF,MSB}$ (see (3.4)), which makes $V_{REF,LSB}$ very small as y tends to decrease. As a result, the contribution of $E_{DAC,MCS}$ becomes negligible in E_{DAC} with decrease in value of y. Since, the coarse conversion in the hybrid DAC is performed passively using CS scheme, the switching energy of the coarse DAC is only calculated during pre-charging phase. As a result, $E_{DAC,CS}$ is given by (3.24).

$$E_{DAC,CS} = (2^{x-1} - 1)C_{u,cs}V_{REF,MSB}^2 \tag{3.24}$$

The minimum E_{DAC} is observed for a combination of x and y, where $C_{u,mcs} = C_{u,cs}$ for even values of n, and $C_{u,cs} = 2C_{u,mcs}$ for odd values of n. As we go towards left side from this point (minimum E_{DAC}), $E_{DAC,CS}$ tends to increase as the increase in $C_{u,cs}$ dominates over decrease in the value of x. On the other hand, as we go towards right side from the minimum point, $C_{u,cs}$ is constant but, x increases, which make $E_{DAC,CS}$ to increase exponentially with x (from (3.24)). As a result, E_{DAC} also follows the same behaviour as $E_{DAC,CS}$. Since the focus of the current work is to design an energy efficient SAR ADC with CS-MCS hybrid DAC, the segmentation of the DAC (values of x and y) is selected based on the minimum energy consumption by the DAC for the desired value of n.

3.3 Comparison with other Switching Schemes

As discussed in the previous section, the minimum average switching energy of the hybrid DAC is obtained when $C_{u,cs} = C_{u,mcs}$ for even values of n and

$C_{u,cs} = 2C_{u,mcs}$ otherwise. Therefore, the average switching energy of the hyrbid DAC has been calculated for 10-bit resolution, and it is compared with the state of the art work. For a fair comparison, all the results are compared from behavioral models. The result is summarized in Table 3.2.

Table 3.2: Comparison of Different Switching Schemes for 10-bit SAR ADC

Switching Schemes	**Average Switching Energy** ($C_u V_{REF}^2$)	**Energy Saving**	**Area Reduction**
Conventional [39]	1363.3	Reference	Reference
MCS [42]	170.17	87.54%	50%
CS [30]	511	62.52%	75%*
Tri-level [72]	42.42	96.89%	75%
Rahimi & Yavari [73]	85.05	93.70%	75%
Xie *et al.* [51]	15.88	98.83%	75%
Yazdani *et al.* [74]	31.87	97.66%	50%
Reset & set [57]	23.93	98.24%	93.75%
This work	**15.05**	**98.90%**	**96.15%**

*Excluding C_{TH}.

It is observed from the table that the hybrid DAC shows 98.90% energy saving and 96.15% reduction in the active-area occupancy, which is the highest reduction compared to other reported works.

3.4 Conclusions

This chapter presented two novel hybrid DACs for SAR ADC along with the selection of the best architecture between the two. In addition, the segmentation strategy has been presented to decide the bit allocation between the coarse and the fine DACs. Finally, a comparison of the energy saving and area reduction with the state of the art work is also presented to demonstrate the efficiency of the proposed hybrid DAC.

Chapter 4

CS-MCS Hybrid DAC SAR ADC with CMOS Technology

SAR ADCs operating at a sampling frequency of tens of Mega-Hertz and with moderate resolutions (up to 10-bits), are widely employed in wireless receivers [75–77] due to its high-energy efficiency and switching intensive nature. Therefore, this chapter presents the implementation of a novel hybrid DAC SAR ADC with STM 65nm CMOS technology. The SAR ADC is designed with asynchronous architecture to speed up the conversion process. The clock signals for comparator and SAR controller are generated internally based on the settling time of the DAC, decision time of the comparator and delay from the SAR controller. A linear sampling switch has been proposed for the hybrid DAC SAR ADC, which is discussed in this chapter. The ADC is designed with 10-bit resolution and it is simulated at a V_{DD} and frequency of 0.8V and 40MHz, respectively.

4.1 Proposed CS-MCS Hybrid DAC based SAR ADC

The circuit schematic of the complete 10-bit CS-CR hybrid DAC based SAR ADC is shown in Figure 4.1. Here, clk_samp represents the sampling clock signal of the ADC. The clock signals for the comparator and SAR controller logic is generated using set of logic gates as shown in the figure. This set up for the clock signal generation takes into account the settling time of the DAC, response time of the comparator and the SAR logic controller. The output bits from the SAR controller are used for generating the clock signals (clk) for the comparator, and the outputs from the comparator (V_{op} and V_{on}) are used to generate the clock

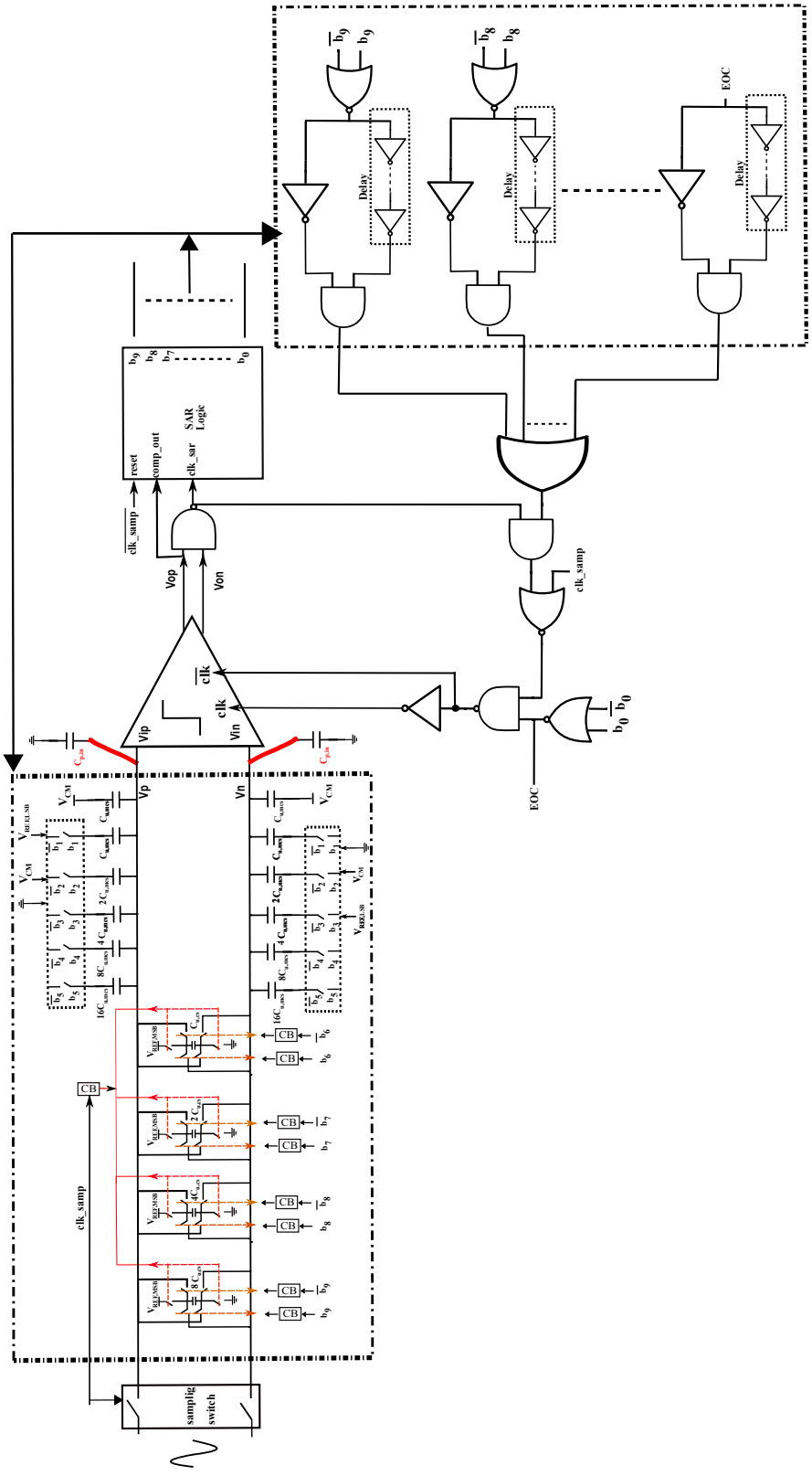


Figure 4.1: Schematic of the proposed 10-bit Hybrid DAC SAR ADC with CMOS technology.

signal for SAR controller (clk_sar) using a NAND gate. This setup ensures that the SAR controller takes the input from the comparator only when its output is completely settled. On the other hand, the comparator is ready to make the next decision after the current bit is resolved. As a result, the comparator gets more time to make the decision when the inputs of the comparator (V_p and V_n) are very close to each other, less time for when they are far apart from each other. This asynchronous structure will make the ADC to work faster compared to the synchronous architecture, where different external clocks with fixed duration are used to synchronize the operation of these blocks.

The hybrid DAC for 10-bit ADC configuration employs a 5-bit CS coarse DAC and a 6-bit MCS fine DAC as with this combination the energy of the DAC is minimum (discussed in Chapter-3). Moreover, this combination yields the ratio of the unit capacitor of the coarse and fine DAC ($\frac{C_{u,cs}}{C_{u,mcs}}$) to one. The hybrid DAC is designed using all unit capacitors, *i.e.,* for binary weighted capacitors, a parallel combination of unit capacitor has been used. Minimum sized NMOS transistors are used as DAC switches to minimize the parasitics associated with the devices. For the fine DAC, since $V_{REF,LSB}$ is a scaled version of $V_{REF,MSB}$ (=V_{DD}), a simple NMOS pass transistor switch can completely pass the reference voltage to charge the bottom plates of the capacitors in the fine DAC. However, for coarse DAC clock boosters (CB) [30] have been used for minimum sized nmos pass transistor switches to minimize the capacitance at the input of the comparator, resistance and charge injection issues with these switches. In addition, since $V_{REF,MSB}$ = V_{DD}, the inherent V_{TH} drop can also be eliminated. It should be noted that $\frac{C_{u,cs}}{C_{u,mcs}}$ is effected by the parasitic capacitances that are lumped at the input of the comparator. Moreover, any mismatches in the unit capacitors of the coarse and fine DAC can degrade the performance of the ADC. The effect of these two non-linearities in the DAC is discussed next.

Parasitics at the input of the comparator:
The parasitic capacitance lumped at the input of the comparator due to the interconnects or the input transistor of the comparator, effects the conversion process of the hybrid DAC. As a result, the voltages generated by the DAC at the inputs of the comparator will deviate from its original values (calculated using (3.10) and (3.11)), resulting into an incorrect conversion. Therefore, the effect of the parasitic should be taken into consideration to avoid incorrect calculation of the voltages. In order to account for this parasitic, $C_{p,in}$ is used to represent the lumped parasitic capacitance at the input of the comparator as shown in Figure

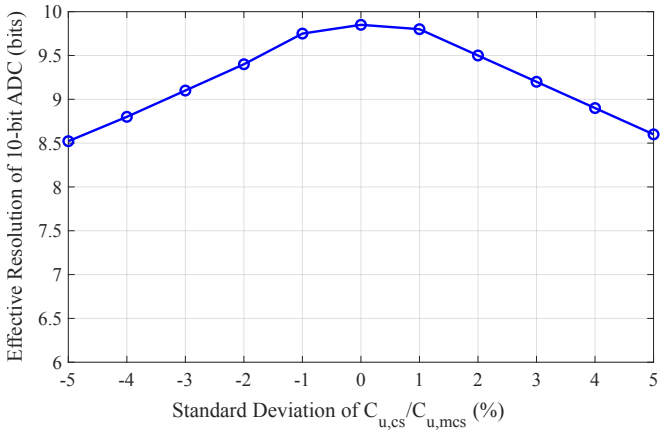


Figure 4.2: Mean effective resolution as function of the standard deviation of the ratio $\frac{C_{u,cs}}{C_{u,mcs}}$ mismatch for hybrid DAC SAR ADC, extracted with a 1024-point FFT and a sample size of 200.

4.1. It is observed from the figure that the sum of $C_{p,in}$ and $C_{total,mcs}$ act as a C_{TH} for coarse conversion by the CS DAC. Neglecting all the other parasitics except $C_{p,in}$, (3.3) is modified as (4.1) for x-bit coarse and y-bit fine hybrid DAC.

$$C_{total,mcs} + C_{p,in} = 2^x C_{u,cs} \tag{4.1}$$

Therefore, the relation between $C_{u,mcs}$ and $C_{u,cs}$ is derived in (4.2), which shows that this relationship between the unit capacitors also depends on $C_{p,in}$ along-with x and y.

$$\begin{aligned} 2^{(y-1)} C_{u,mcs} + C_{p,in} &= 2^x C_{u,cs} \\ C_{u,cs} &= 2^{y-x-1} C_{u,mcs} + \frac{C_{p,in}}{2^x} \end{aligned} \tag{4.2}$$

Since the presence of $C_{p,in}$ modifies the total capacitance of the fine DAC from $C_{total,mcs}$ to $C_{total,mcs} + C_{p,in}$, the factor by which $V_{REF,MSB}$ is scaled to generate $V_{REF,LSB}$ is also modified from (3.4) and it is given by (4.3).

$$V_{REF,LSB} = \frac{V_{REF,MSB}}{\frac{2^{n-1} C_{u,mcs}}{2^{y-1} C_{u,mcs} + C_{p,in}}} \tag{4.3}$$

Hence, for a fixed value of $C_{p,in}$, the ratio of $C_{u,cs}$ and $C_{u,mcs}$, and $V_{REF,LSB}$ should be modified according to (4.2) and (4.3) for correct calculation of the voltages by the DAC at the inputs of the comparator. The value of $C_{p,in}$ can be extracted from the layout and needful modifications can be made in the values of unit capacitors and reference voltage. Moreover, the value of $C_{p,in}$ can be

minimized by employing higher level metal layers for routing the two inputs of the comparator, if active-area is not a constraint.

Effect of mismatch between the coarse and fine DAC:
To study the effect of mismatch between the coarse and fine DACs of the hybrid DAC SAR ADC, all the other non-ideal effects like parasitics are considered to be negligible. Extensive Monte-Carlo behavioral simulations are performed for a 10-bit resolution with different mismatch spreads in the ratio of the unit capacitors of coarse and fine DAC ($\frac{C_{u,cs}}{C_{u,mcs}}$) for quantifing the impact of the mismatches between the two sub-DACs of the hybrid DAC. The simulated ENOB values are obtained using a 1024-point Fast Fourier Transform (FFT) with a sample size of 200. The obtained result is shown in Figure 4.2. Here $\pm 5\%$ mismatch is considered in $\frac{C_{u,cs}}{C_{u,mcs}}$ from its typical value. From the figure it can be seen that the the effective resolution of the hybrid DAC SAR ADC degrades utmost by 1.4 bits when the mismatch percentage is around 5% in magnitude. However, if this percentage is maintained $\leq 3\%$ by using appropriate layout techniques to control capacitor mismatches, then the degradation in effective resolution of the ADC can be reduced to less than one bit.

4.2 Blocks Description of Proposed ADC

4.2.1 Proposed Sampling Switch

The circuit schematic of the proposed switch ($M1$, $M2$) [61] is shown in Figure 4.3(a). This circuit does not employ a charge pump or clock booster to bootstrap the gate voltage of the PMOS transistor. In addition, no additional switches are used to minimize the V_{TH}-variations, as the voltages used for this purpose are generated internally. Here, the sampling clock, clk, oscillates between 0V and V_{DD}. The signal $\overline{clk}$ is obtained from clk using an inverter I_1. C_L and $C_{B1,2}$ are the load and bootstrapping capacitors, respectively.

The R_{ON} of the switch is defined as $R_{ON,M1} \mid\mid R_{ON,M2}$, where $R_{ON,M1}$ and $R_{ON,M2}$ represent the ON-resistances of NMOS ($M1$) and PMOS ($M2$) transistors in the switch, respectively, which are given as:

$$R_{ON} = \frac{1}{\mu_{M1,2} C_{OX} \frac{W_{M1,2}}{L_{M1,2}} (|V_{GS,M1,2}| - |V_{TH,M1,2}|)} \tag{4.4}$$

where, μ, C_{OX} and $\frac{W}{L}$ are the mobility, oxide capacitance and aspect ratios of the transistors, respectively. The effect of the source-to-bulk voltage, V_{SB}, variations on V_{TH} of a p-type or n-type MOS transistor is defined in [78] as:

$$|V_{TH}| = |V_{TH,0}| + \gamma(\sqrt{|2\phi_f| + |V_{SB}|} - \sqrt{|2\phi_f|}) \tag{4.5}$$

where, $V_{TH,0}$, γ, and $2\phi_f$ are the threshold voltage (when $|V_{SB}|$ = 0V), body-effect coefficient and surface potential of the transistor, respectively.

The operation of the proposed switch can be understood in two phases:

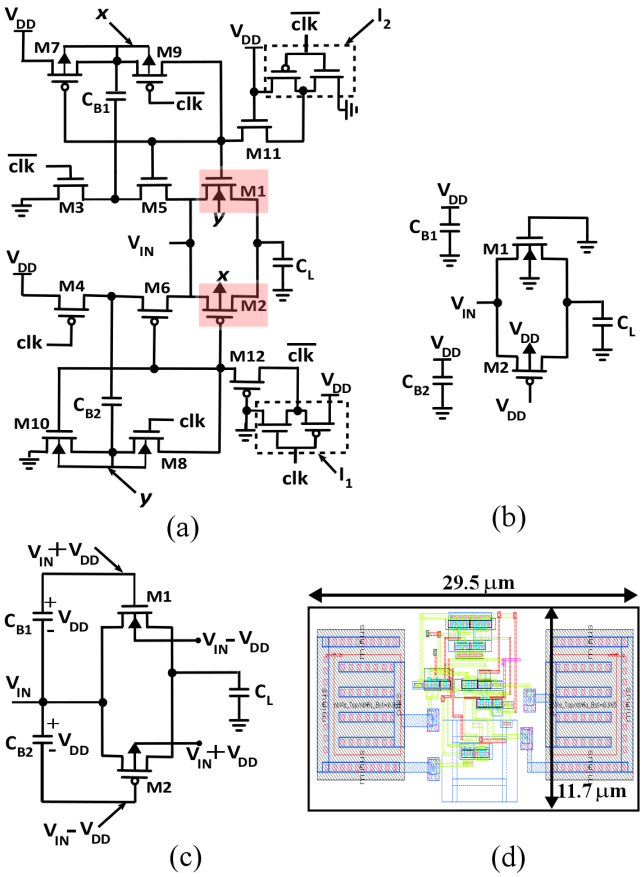


Figure 4.3: Proposed robust linear bootstrapped TG switch (a) Circuit Schematic (b) Equivalent circuit in hold phase (clk=0V) (c) Equivalent circuit in tracking phase ($clk = V_{DD}$) and (d) Layout showing active area occupied.

Hold Phase (clk = 0V): In this phase, $M3$, $M4$, $M7$, $M10$, $M11$, $M12$ are ON, and $M5, M6, M8, M9$ are OFF. Therefore, capacitors, C_{B1} and C_{B2} are charged to V_{DD}. As a result, voltages at node x (V_x) and y (V_y) are at V_{DD} and 0V, respectively. Moreover, the output of inverters I_1 and I_2 are at V_{DD} and 0V, respectively. Therefore, $M11$ and $M12$ set the gate of $M1$ and $M2$ to 0V and V_{DD}, respectively, to turn them OFF. In addition, the bulk of $M1$ is at 0V (=V_y),

and $M2$ is at V_{DD} (= V_x). Thus, C_L is isolated from the input signal, V_{IN}, and the switch is in hold phase. The equivalent circuit is shown in Figure 4.3(b).

Track Phase (clk = V_{DD}): In this phase, $M5$, $M6$, $M8$, $M9$ are ON, and $M3$, $M4$, $M7$, $M10$, $M11$, $M12$ are OFF. As a result, V_x and V_y are defined as:

$$V_x = V_{IN} + V_{DD} \;\; and \;\; V_y = V_{IN} - V_{DD} \tag{4.6}$$

Since V_{IN} is bounded by the power supply rails, V_y can never be a positive value. Therefore, the bulks of NMOS transistors, $M8$, and $M10$ are connected to node y. Similarly, bulks of PMOS transistors, $M7$, and $M9$ are connected to node x. These connections ensure the junction diode between source and bulk to be reversed biased. $M8$ and $M9$ connect the gates of $M2$ and $M1$ to node y and x, respectively. As a result, the gate-to-source voltages of $M1$ and $M2$ are at V_{DD} and $-V_{DD}$, respectively, which turn ON both the transistors. In addition, bulks of $M1$ and $M2$ are connected to nodes y and x, respectively, which ensures $|V_{SB}|$ of $M1$ and $M2$ to be a constant value equal to $|V_{DD}|$ (see (4.6)). Therefore, $M1$ and $M2$, in the proposed switch, provide a constant R_{ON} (from (4.4) and (4.5)) irrespective of the magnitude of V_{IN} while C_L is tracking it. Thus, the switch is in the track phase. The equivalent circuit is shown in Figure 4.3(c).

Due to a constant R_{ON}, the proposed switch also ensures the desired performance without using wider transistors, thus, improving its speed of operation even at low V_{DD}. In addition, no boosters or charge pumps are employed. Moreover, there are no reliability issues noticed with the proposed circuit.

Results and Discussions:
The post-layout simulations are performed using Spectre. Since SAR ADC completes digital conversion serially, the duty cycle of the sampling clock is always kept much less than 50%. As a result, a small-time interval is available for the sampling switch to track the input analog signal. Therefore, in this work, the ON-time of the sampling clock for testing the sampling switch is taken as 5ns. Hence, simulations are performed at a sampling frequency of 100MHz (considering 50% duty cycle), a nominal supply voltage of 0.8V and load capacitance, C_L=1pF.

The layout of the proposed switch is shown in Figure 4.3(d). Deep n-well (DNW) layer is used in the layout to isolate the bulk of the NMOS transistors, $M1$, $M8$, and $M10$ (see Figure 4.3(a)) from other devices. The layout occupies

an active area of only 345.15μm^2. As a first step, transient simulations were performed to plot V_{TH} of NMOS transistor $M1$ and PMOS transistor $M2$ (in Figure 4.3(a)) as a function of V_{IN}. The plots were obtained for two cases:
Case-1: When bulk voltages of $M1$ and $M2$ ($V_{B,M1}$ and $V_{B,M2}$) are at 0V and V_{DD}, respectively.
Case-2: When $V_{B,M1}$ = V_y and $V_{B,M2}$ = V_x as shown in Figure 4.3(a).
The obtained results are shown in Figure 4.4. It can be observed from the figure that a variation of 5% in V_{TH} of $M1$ and $M2$ have been noticed for case-1. On the other hand, only 0.05% of variations are observed in V_{TH} of $M1$ and $M2$

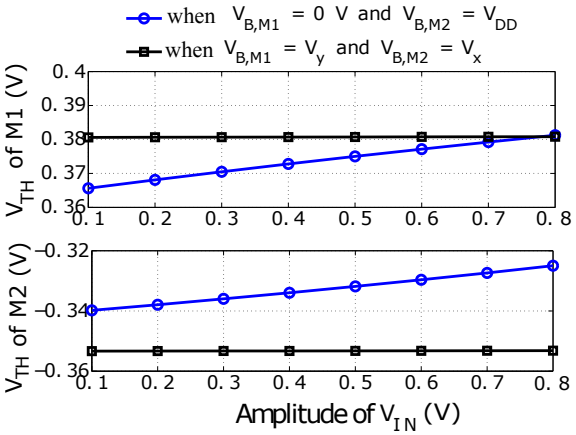


Figure 4.4: Variations in V_{TH} of $M1$ and $M2$ with V_{IN}.

for case-2. Therefore, the proposed design ensures almost constant V_{TH} over the complete input signal amplitude range, as explained in the previous section. Post-layout transient simulations of the switch are performed with a full-scale (FS) input sinusoidal signal with a frequency of 10MHz. The gate voltages (V_G) of $M1$ and $M2$ (see Figure 4.3(a)) are presented in Figure 4.5, which shows that during tracking phase, $V_{G,M1} = V_{IN} + V_{DD}$ and $V_{G,M2} = V_{IN} - V_{DD}$. As a result, the gate-to-source voltages of $M1$ and $M2$ are at V_{DD} and $-V_{DD}$, respectively.

The performance of this design is compared with four sampling switches reported in [79–82]. These switches have been designed with the same technology (STM 65nm), and post-layout simulations are performed under the same conditions (V_{DD}=0.8V) as that of the proposed sampling switch. The aspect ratios of all the transistors in different switches are kept the same to have a fair comparison of the performance metrics. R_{ON} of the proposed and other switches from literature were calculated at the different amplitude of V_{IN} using transient simulations at a clk frequency of 100MHz. Simulation results are presented in Figure 4.6. It can be observed that the proposed switch provides almost

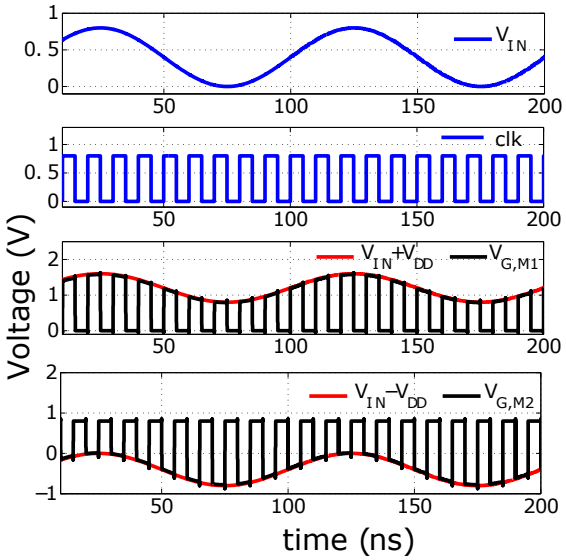


Figure 4.5: Timing diagram showing the gate voltages of $M1$ ($V_{G,M1}$) and $M2$ ($V_{G,M2}$) in the proposed sampling switch.

constant and least value of R_{ON} (=560 Ohms) compared to other designs. The

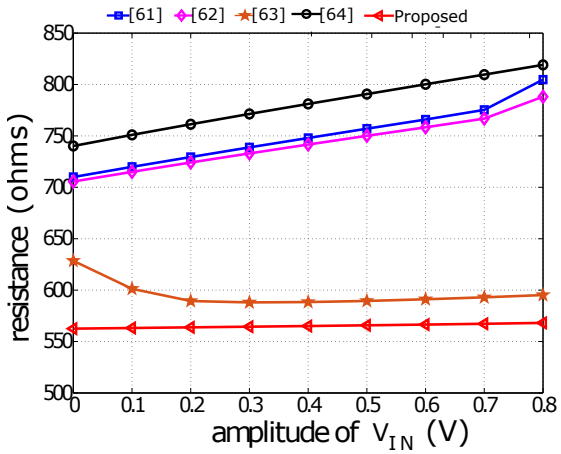


Figure 4.6: Comparison of R_{ON} of proposed switch with state of art work.

least value of R_{ON} is due to the parallel connection of the R_{ON} of PMOS and NMOS transistors compared to the NMOS bootstrapped switches [79, 80, 82], where the resultant R_{ON} is the ON-resistance of NMOS transistor only. On the other hand, R_{ON} of the TG bootstrapped sampling switch [81] is defined in the same manner as that of the proposed sampling switch. However, the R_{ON} of the TG bootstrapped switch is higher due to the degraded gate voltages of $M1$ and $M2$ compared to the proposed design. The degradation is due to the parasitics contributed by continuously ON transistors M5 and M10. Besides, in the tracking phase, the PMOS transistor $M14$ turns OFF, when the magnitude of V_{IN} falls below the magnitude of the threshold voltage of $M14$ and prevents the

bootstrapping operation of $M2$. However, no such degradation is observed in the proposed switch. In our design, the parasitics at the gate of $M1$ and $M2$ due to $M11$ and $M12$ are compensated by turning them ($M11$ and $M12$) OFF using inverters $I1$ and $I2$. To make this point more clear, $V_{G,M1}$ (when $V_{IN} = V_{DD}$) and $V_{G,M2}$ (when $V_{IN} = 0$ V) of the TG bootstrapped and proposed sampling switch in tracking phase, is shown in Figure 4.7. It is observed from the plot that the our design reaches the desired voltage faster than the TG bootstrapped switch without any degradation in gate voltages.

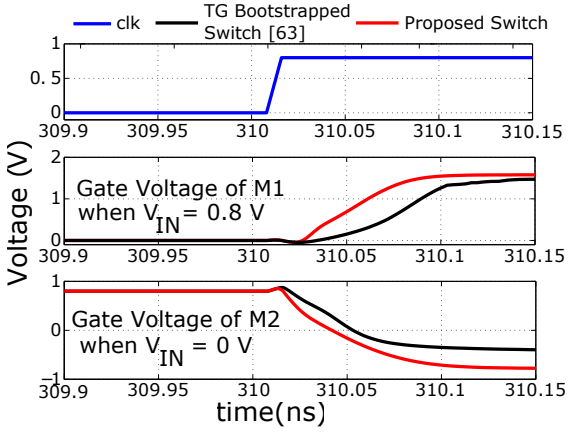


Figure 4.7: Transient Simulations showing $V_{G,M1}$ and $V_{G,M2}$ of proposed and TG bootstrapped sampling switch.

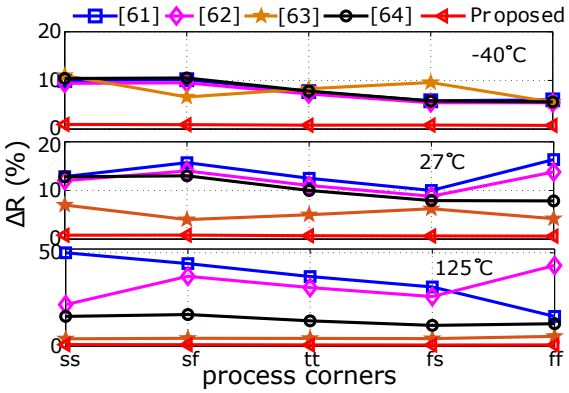


Figure 4.8: Comparison of ΔR_{ON} of proposed switch with state of art work at different process corners and temperatures.

Next, the amount of variations in R_{ON} with the amplitude of V_{IN}, ΔR_{ON}, has been calculated using the following equation:

$$\Delta R_{ON} = 2\frac{R_{ON,max} - R_{ON,min}}{R_{ON,max} + R_{ON,min}} \tag{4.7}$$

Here, $R_{ON,max}$ and $R_{ON,min}$ are defined as the maximum and minimum values

of R_{ON}, respectively, which are obtained from Figure 4.6. The values of ΔR_{ON} of the proposed switch and the switches from the literature, are evaluated at different process corners (ss, sf, tt, fs and ff) and temperature (-40°C, 27°C and 125°C) at a V_{DD} = 0.8V. The results are presented in Figure 4.8. It can be observed from the figure that our design has shown a maximum variation of 1% against different process corners and temperature, which is very low compared to other works reported in the literature. **Low variation will make the R_{ON} of the switch almost constant, which can help in achieving better linearity in the ADC.**

4.2.2 Comparator

A dynamic bias latch type comparator, which has been proposed by *Bindra et al.* [19], is employed in the proposed SAR ADC design. The circuit schematic of the comparator is shown in Figure 4.9. It consists of a dynamic pre-amplifier formed by transistors $M1$ to $M6$ followed by latch stage formed by transistors $M7$ to $M14$. The output of the comparator Vop and Von are obtained from two inverters, which take inputs from the outputs of the latch stage. The comparator sets the two outputs of the comparator Vop and Von to logic '1' in the reset phase, *i.e.*, when the comparator clock clk is at logic '0'. As derived in [19], the input referred noise (INR) of the comparator is given by:

$$INR \propto \frac{1}{C_{p_{Fn|Fp}} \Delta V_{Di,CM} \frac{gm_{M3|M4}}{I_{CM}}} \tag{4.8}$$

where, $C_{p_{Fn|Fp}}$, $\Delta V_{Di,CM}$, $gm_{M3|M4}$ and I_{CM} are thee parasitic at node Fn or Fp, output common-mode voltage drop of the pre-amplifier stage, transconductance and commom mode current, respectively. It can be observed from (4.8) that INR is inversely proportional to $\frac{gm}{I_D}$, and a large $\frac{gm}{I_D}$ (small over-drive voltage) is desirable to improve the noise performance of the comparator. To obtain the lowest noise for a given current, it is desirable to make $M3$ and $M4$ to operate in weak inversion region (large $\frac{gm}{I_D}$) [19] until the latch stage makes a decision. This is ensured by connecting a minimum-sized tail transistor $M5$ as shown in the figure, which bias the differential pair in near weak inversion at the start of comparator operation. When clk is at logic '1' level, the differential pair begins the operation with a specific tail current, which after some time decreases continuously with increase in the voltage across capacitor C_tail. Due to the large resistance of $M5$, the source voltage of the differential pair does not drop

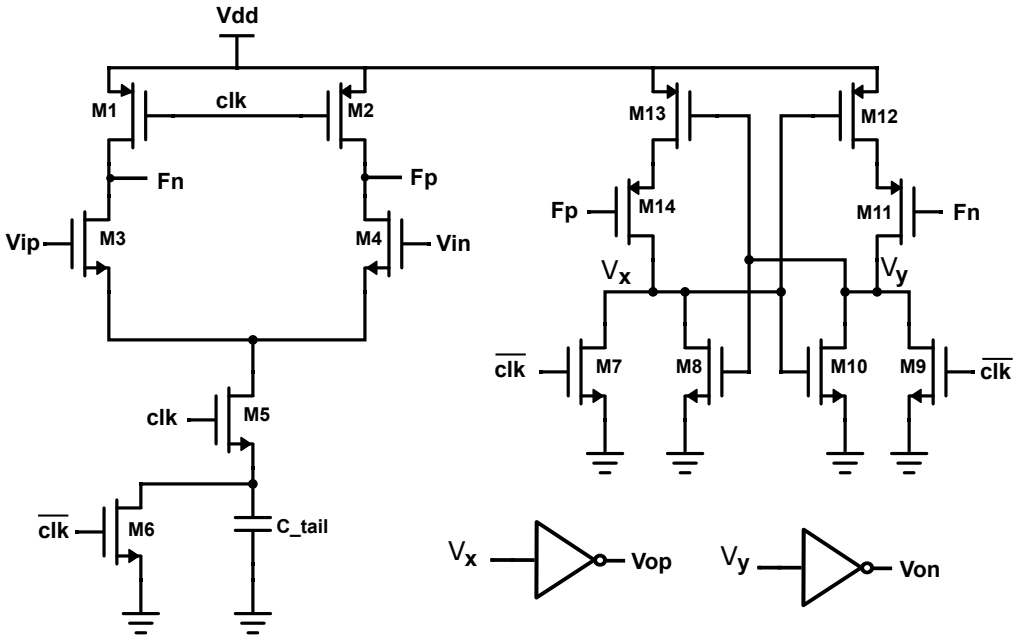


Figure 4.9: Schematic of dynamic bias latch type comparator [19].

to zero instantaneously. As a result, the overdrive voltage of the differential pair decreases with increase in voltage across capacitor C_tail, which results in near weak inversion operation of the differential pair. Therefore, the dynamic bias keeps the pre-amplifier in the weak inversion regime for most of the integration time in order to obtain minimum achievable noise performance for a given capacitive load [19].

Results and Discussions:

The post-layout transient simulations in the presence of transient noise were performed for the comparator at a supply voltage of 0.8V and at a clock frequency of 500MHz to obtain the minimum voltage that the comparator can discriminate. The simulation setup involves a slow rising ramp signal followed by slow falling applied to one terminal of the comparator, and a fixed DC voltage (=0.4V) to its other terminal. The input differential voltage to comparator under this setup and its response is shown in Figure 4.10(a). The offset of the comparator has been calculated as 212μV under typical condition. Using the same setup, the offset of the comparator has been calculated at different process corners, and the results are summarised in Figure 4.10(b). It can be seen from the figure that the worst corner offset of the comparator is around 400μV, which is much less than 1 LSB (=781.25μV) of the 10-bit ADC with reference voltage of 0.8V. In order to depict the dynamic behavior of the comparator, a fully differential signal with

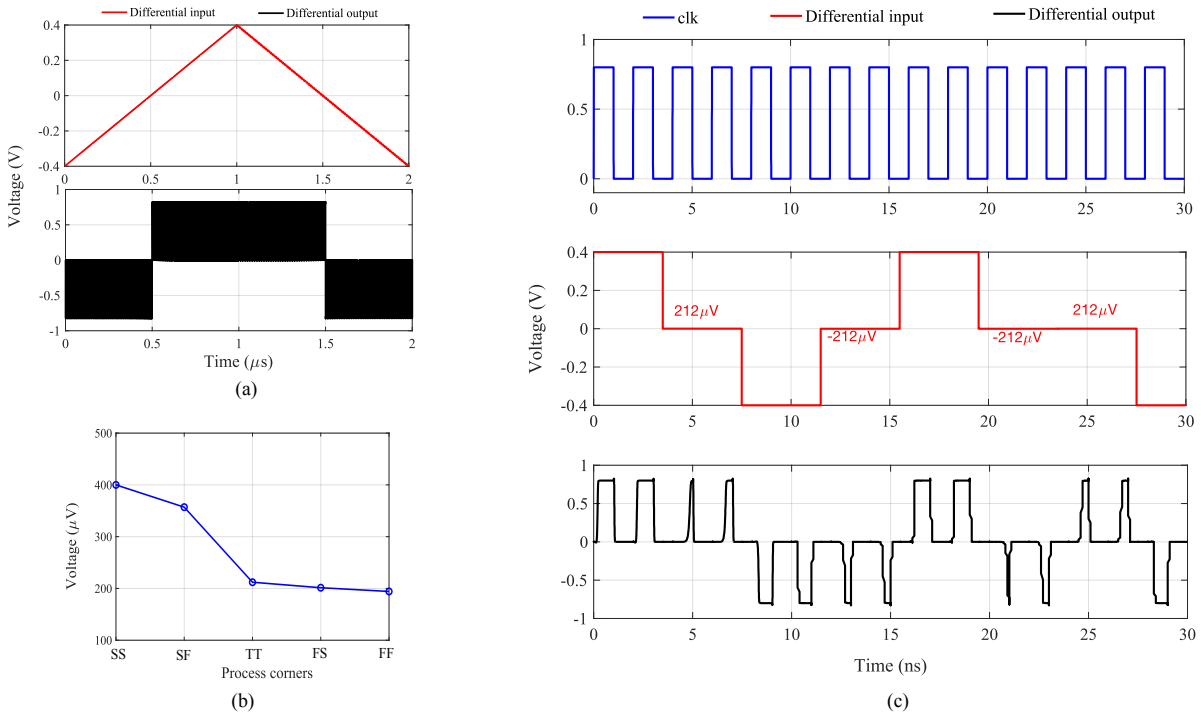


Figure 4.10: Post-layout simulation results of the comparator in presence of transient noise (a) with slow ramp wave (b) Comparator resolution against process corners (c) with worst-case differential input under typical condition.

worst case input has been applied to the comparator as shown in Figure 4.10(c). It can be observed that the comparator decides correctly with worst case decision time of 850ps if the comparator input is $\geq 212\mu$V.

4.2.3 SAR Logic Controller

The block diagram of the SAR controller for 10-bit hybrid DAC SAR ADC (b_9-b_0) is shown in Figure 4.11. This block is constructed using shift registers and basic gates. It can be seen from the figure that the first row of the shift register is clocked using clk_sar, which is the clock signal for the SAR Logic. The outputs from the first row of shift register ($cl9$-$cl0$) are used as clock signals by the second row of the shift register to produce digital bits on every rising edge of clk_sar depending upon the state of comparator output $comp\_out$. As stated in Chapter-3, during the sampling phase, b_9-b_0 and $\overline{b}_9$-$\overline{b}_0$ should be at logic '0'. Alternatively, we can say that during sampling phase none of the bits should connect the CS DAC capacitors to the input of the comparator. Moreover, MCS DAC capacitors should be connected to the common mode voltage. In order to make $\overline{b}_9$-$\overline{b}_0$ to logic '0' during the sampling phase, a set of even number of cascaded inverter stages as a delay element along with NOR and $NAND$ gates

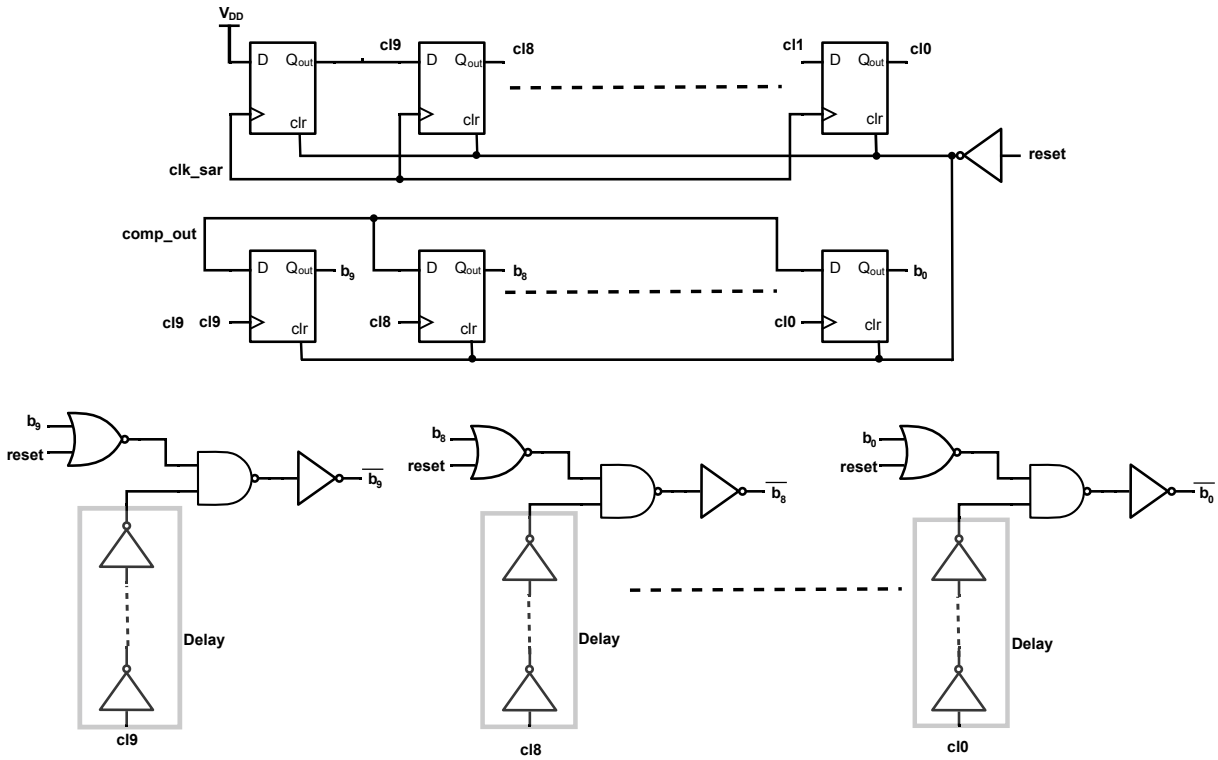


Figure 4.11: Schematic of SAR Logic controller for CMOS design.

are used to obtain the complementary output bits. If b_9-b_0 are passed directly to the inverter to obtain $\overline{b}_9$-$\overline{b}_0$, then, during the sampling phase, when reset pin is activated to make b_9-b_0 to logic '0', $\overline{b}_9$-$\overline{b}_0$ would have been at logic '1', which can disturb the sampling process and make the sampled voltage incorrect. Therefore to avoid this situation, a NOR gates are used with $reset$ and b_9-b_0 as their input. The outputs of the NOR gates give correct result, when b_9-b_0 are set to logic '0'. However, if these bits are at logic 1', then there will be glitches in $\overline{b}_9$-$\overline{b}_0$ due to finite rise and fall time of b_9-b_0 and $reset$. To avoid these glitches, $cl9$-$cl0$ is delayed, and these delayed signals along with the output from the NOR gates, are passed as inputs to the AND gates (formed by $NAND$ and an inverter) to generate $\overline{b}_9$-$\overline{b}_0$. The shift registers in SAR controller is formed by true-single-phase-clock (TSPC) D-flip flop [83], which resets the output to logic '0' when clr is at logic '0'. Since all the bits are reset to logic '0' during the sampling phase, the $reset$ pin of the SAR controller is connected to $samp\_clk$.

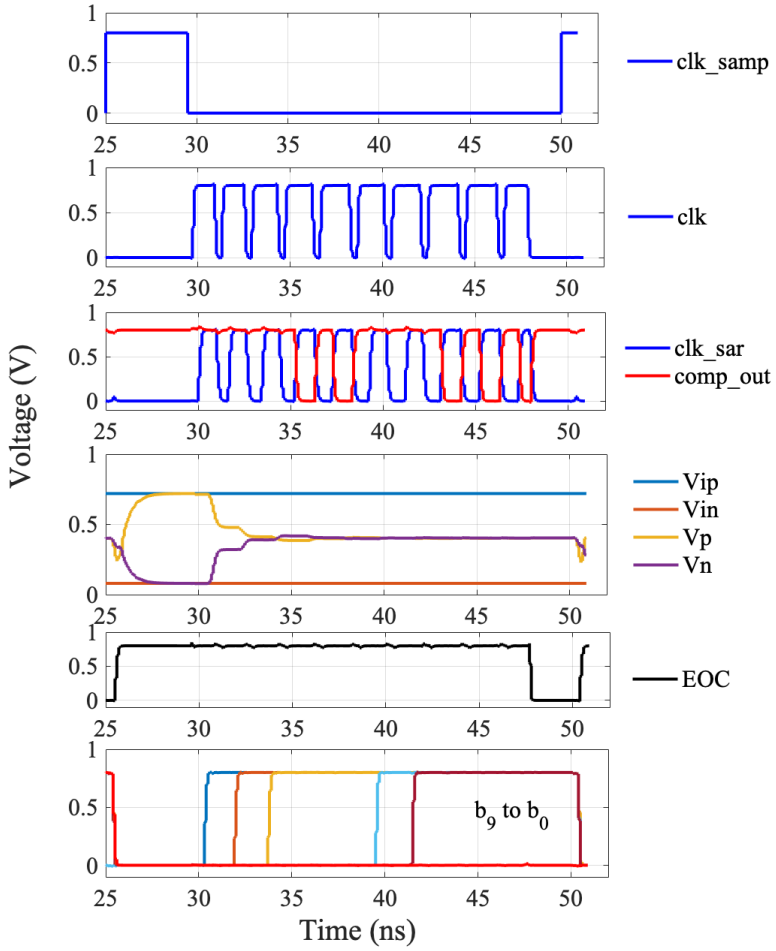


Figure 4.12: Response of Hybrid DAC SAR ADC with CMOS technology for fixed input voltages.

4.3 Results and Discussions of Proposed SAR ADC

The 10-bit SAR ADC is designed using STM 65nm CMOS technology with a 5-bit CS coarse DAC and a 6-bit fine MCS DAC. The segmentation is selected based on the study presented in Chapter-3, which shows the minimum switching energy of the DAC at this point. As result, ideally $C_{u,cs}/C_{u,mcs}$ =1. However, due to the presence of parasitic at the inputs of the comparator this ratio is modified as 1.5, which is calculated using equations derived in the previous section. The post-layout simulations are performed at a sampling frequency of 40MHz and supply voltage V_{DD} of 0.8V. The value of $V_{REF,MSB}$ and $V_{REF,LSB}$ are taken as 0.8V and 0.07V, respectively. Based on the $\frac{KT}{C}$ noise consideration and to minimize the mismatch issues, the value of the unit capacitor is selected as 17fF. First to check the functionality of the ADC, the post-layout simulations are performed for fixed input voltages (0.72V and 0.08V). The obtained results with

transient noise are presented in Figure 4.12. As discusses previously, the clock signals for comparator and SAR logic controller are generated internally using a set of digital logic gates. The figure also shows the generated clock signals during the conversion process of the ADC. It is observed from the figure that the ADC produces correct output bits (b_9 to b_0) for the given fixed voltages, which shows correct operation of the ADC. The layout of the complete ADC is shown in Figure 4.13(a), and it occupies an active area of 0.054mm^2.

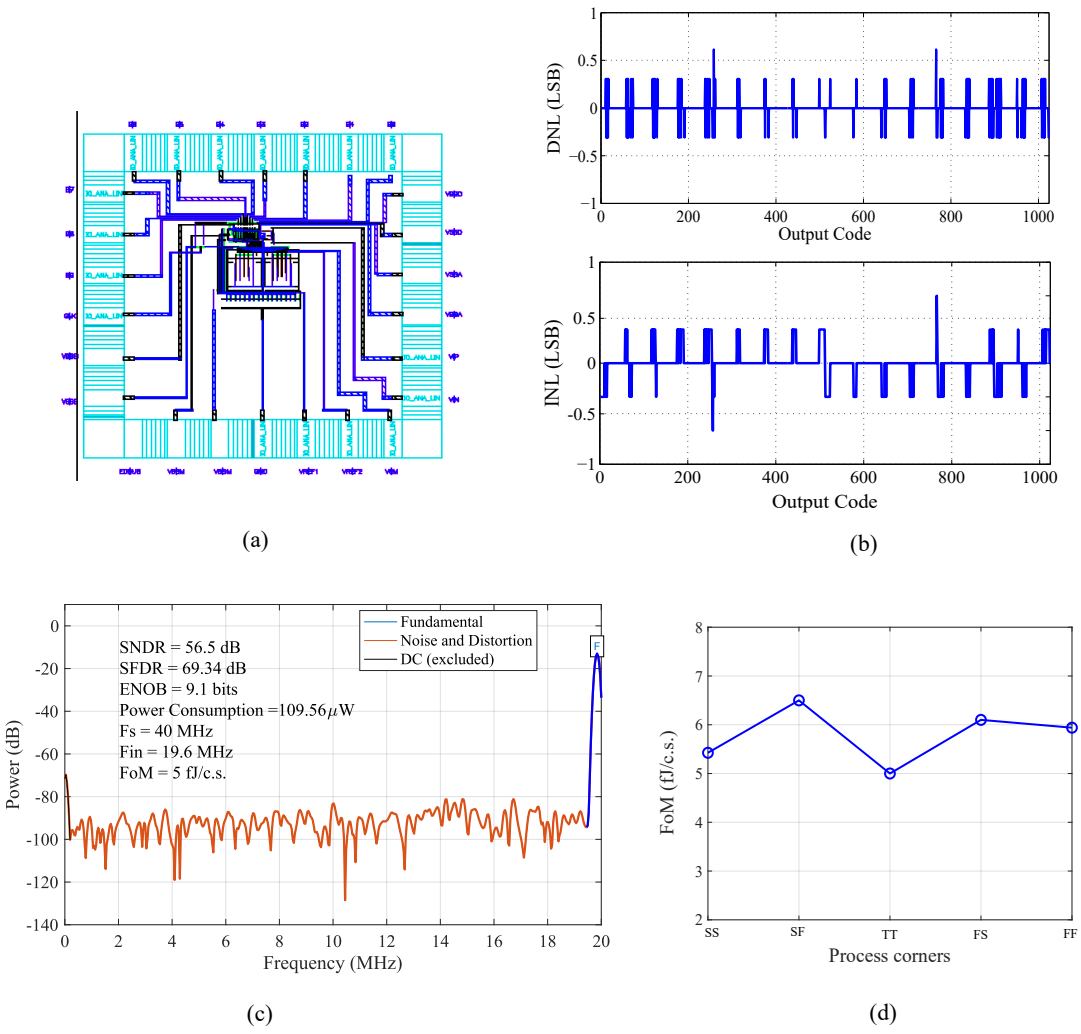


Figure 4.13: Simulated results of 10-bit Hybrid DAC SAR ADC with CMOS technology (a) Layout (b) DNL and INL plots (c) Spectrum under typical condition (d) FoM under different process corners.

Next, the DNL and INL errors of the ADC are obtained using the ramp signal test and the results are shown in Figure 4.13(b). The maximum DNL and INL errors have been observed as 0.6 LSB and 0.7 LSB, respectively, which shows no missing code and monotonic behavior of the ADC. To obtain the dynamic

Table 4.1: **Comparison of the proposed SAR ADC with state of the art work in CMOS technology**

ADC Metrics	[84] 2016	[85] 2017	[86] 2018	[87] 2019	[88] 2020	**This Work****
Resolution (bits)	10	10	10	10	10	**10**
Technology (nm)	90	180	65	180	55	**65**
Supply Voltage (V)	1	1.8	1.2	1.2	1	**0.8**
Fs (MHz)	160	80	150	5	8	**40**
SNDR (dB)	53	56.7	51.1	56.7	58.053	**56.5**
SFDR (dB)	-	72.3	-	-	66	**69.3**
ENOB (bits)	8.48	9.13	8.2	9.13	9.35	**9.1**
Power Consumption (μW)	4300	2610	1400	2360	45	**109.6**
FoM_w **(fJ/c.s.)**	63	74.4	31.8	845	8	**5**
Active-area (mm^2)	0.11	1.61	0.079	0.052	0.19	**0.054**

**Post-layout simulations.

behavior of the ADC, the spectrum is obtained using 1024 FFT bins at an input frequency of 19.6MHz and the result is shown in Figure 4.13(c) . Under typical condition, the simulated FoM has been calculated as 5fJ/c.s. at a sampling frequency of 40MHz, and at a supply voltage of 0.8V. The FoM of the ADC has also been calculated at different process corners and the worst corner FoM has been calculated as 6.5fJ/c.s. as shown in Figure 4.13(d). The performance of the ADC is compared with state of the art work SAR ADCs operating in Mega-Hertz range, and the result is summarized in Table 4.1. It can be observed from the table that the proposed ADC shows least FoM compared to the other reported SAR ADCs, thus, showing high energy efficiency compared to other designs.

4.4 Conclusions

This chapter presented the design details of the CS-MCS hybrid DAC based SAR ADC with CMOS technology. The proposed sampling switch employed in the ADC design is able to compensate the V_{TH} variations in the on-resistance

of the switch, thus maintaining almost constant R_{ON} over complete range of input analog signal. The ADC is designed to asynchronous to improve its operating speed. The post-layout simulation result shows that the proposed ADC delivers least FoM compared to other SAR ADCs operating in Mega-hertz range at a low supply voltage of 0.8V under typical case. Thus the proposed hybrid architecture of the SAR ADC can be employed in various applications like wireleess communication, biomedical etc. to improve the overall energy efficiency of the system.

Chapter 5

CS-MCS Hybrid DAC SAR ADC with Oxide TFT Technology

Amorphous oxide thin-film transistor (TFT) technology empowers low-cost flexible and transparent electronics due to its compatibility with low-temperature fabrication techniques [32–35]. As a result, this technology helps implement wearable electronics with unobtrusiveness, which is difficult to achieve with standard complementary-metal-oxide semiconductor (CMOS) technology, employing rigid substrates to fabricate circuits using a high-temperature fabrication process. Moreover, oxide TFT technology enables circuit fabrication on an insulator substrate, eliminating body effects and body-related parasitics. However, low intrinsic mobility, large device parasitics, high operating voltages [89, 90], and scarcity of high performance, stable and reproducible amorphous p-type transistors [91–93] are the major bottlenecks of the oxide TFT technology. As a result, these bottlenecks impose limitations on the applicability of this technology in the system-level implementation of practical importance. Therefore, there is a need to investigate unique and high-performance designs with unipolar transistors.

ADCs are essential functional blocks in biomedical applications. Literature reports some ADCs [36, 94–96] with amorphous oxide TFT technology. The ADCs reported in [94–96] are oversampled ADCs, which employ off-chip passive elements and an over-sampling ratio (OSR) not less than 100 to achieve high resolution. On the other hand, the SAR ADC presented in [36] reports 5 bits at a sampling frequency in tens of hertz, which limits the bandwidth of input analog signal to a few hertz. Moreover, all these ADCs are designed at a supply voltage not less than 10V, thus, making the power consumption of these designs very high, which is a critical parameter in self-sustainable systems. Besides, a

large OSR of the oversampled ADC demands a high-switching activity in the circuits, which raises the design's switching power and further increases the power consumption of these ADCs. One of the best methods to scale down the power of the ADCs is by scaling down the supply voltage. However, the performance of the ADC [94–96] employing analog blocks (like OPAMP etc.) degrades with supply voltage scaling. As discussed previously for moderate resolutions, a SAR ADC is considered the most energy-efficient ADC and exhibits scaling-friendly behavior due to minimal/no analog design blocks. As discussed in previous chapters, exponential dependence of the DAC size on the resolution and the serial-conversion process of the SAR ADC result in a trade-off between the speed and resolution of the ADC. Therefore, to improve the resolution and extend the application of SAR ADCs for a wide frequency range of biomedical signals [97], a second-order noise shaping (NS) is introduced in the CS-MCS hybrid DAC SAR ADC. The NS process shapes the non-linearities associated with the ADC blocks (noise, mismatch, settling, etc.), and the ADC achieves 7-bits from a 5-bit SAR ADC architecture within a bandwidth of 370Hz at a sampling frequency of nearly 3kHz and over-sampling ratio (OSR) of 4. The ADC is designed and simulated using device models from PragmatIC [98] with a channel length not exceeding 4μm and a low supply voltage of 2V.

As discussed in the previous chapters, a sampling switch, a voltage comparator, a DAC and SAR controller are the primary blocks of the SAR ADC. Since with oxide TFT technology the circuits are designed using only n-type transistors, this chapter presents the novel designs of the sampling switch, comparator and SAR controller, which are employed to build the complete SAR ADC with oxide TFT technology. The design details of the complete SAR ADC is described first, which is followed by the description of the proposed sampling switch, comparator and SAR logic employed in the ADC.

5.1 Second-order Noise-shaping CS-MCS SAR ADC

The schematic of the proposed noise-shaped hybrid DAC SAR ADC is shown in Figure 5.1. The output bits obtained from the ADC are represented as $b4$, $b3$, $b2$, $b1$, and $b0$, where $b4$ is the MSB. The design details of the sampling switch, comparator, SAR logic block, and clock boosters (CB), which are employed in the ADC, have been discussed in the following sections. The clock for the comparator, clk_comp, is generated off-chip to minimize the complexity of the

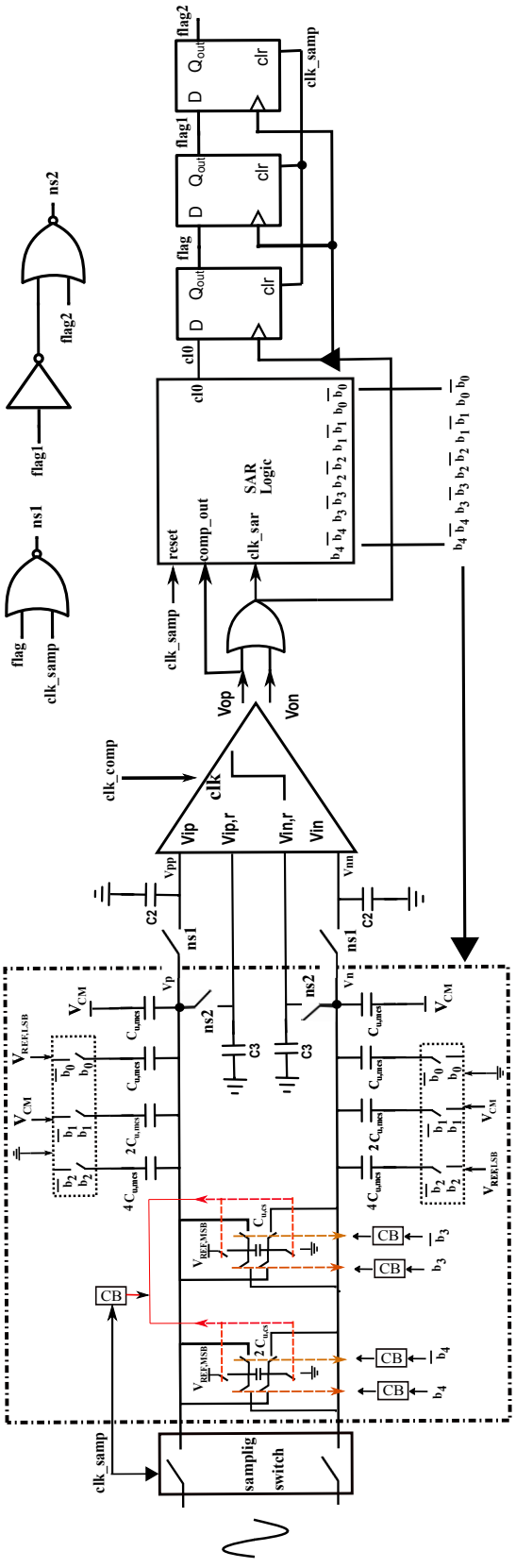


Figure 5.1: Schematic of proposed NS Hybrid SAR ADC.

ADC. Moreover, this clock signal can be generated on-chip using high-speed ring oscillators proposed in [64–66], and discussed in Appendix A. The clock signal for SAR controller clk_sar is generated using OR gate, which takes two inputs from the two outputs of the comparator (Vop and Von). In addition, Vop acts as an input to the SAR controller, $comp\_out$. As discussed previously, the output bits from the SAR controller are fed back to the DAC to control the switching activity of the DAC switches. The hybrid DAC comprises CS coarse and MCS fine DACs. Due to the absence of stable and reproducible p-type transistors in oxide TFT technology, the DAC switches are realized using n-type transistors. As a result, the bits to be fed to the coarse DAC are first passed through the clock boosters to boost the logic high level of the bits. The outputs from these clock boosters are used to control the DAC switches of the coarse DAC to compensate the inherent V_{TH} drop of the n-type switches during the pre-charging process. In addition, this will also help in reducing the on-resistance R_{ON} of the DAC switches employed in the coarse DAC without using wide transistors, which can add parasitics at the input of the comparator and disturb the conversion process (as discussed in the previous chapter). On the other hand, no clock boosters are used with the fine DAC as the n-type DAC switches have to pass $V_{REF,LSB}$, which is the scaled version of $V_{REF,MSB}$ that has a value close to the logic high level of the bits, which controls the switching activity of the fine DAC.

Noise-shaping (NS) in the ADC: According to the Nyquist sampling theorem, the signal should be sampled at a sampling frequency (F_s), which should be at least twice that of the signal bandwidth (BW) to avoid aliasing effect [99]. Once the signal is sampled, it is quantized by the quantizer to output digital bits corresponding to the input sampled amplitude. As a result, the signal-to-quantization noise ratio (SNR) of an n-bit ADC is given by (5.1).

$$SNR = 6.02n + 1.76 \tag{5.1}$$

When the input signal is sampled at a rate greater than the Nyquist rate (Fs>2 BW), then the processing gain (PG) [100] is achieved, which is given by (5.2).

$$PG = 10log_{10}\left(\frac{F_s}{2BW}\right) \tag{5.2}$$

Therefore, due to the presence of PG, the total SNR of the ADC becomes the sum of (5.1) and (5.2) [100], and it is given by (5.3).

$$SNR_{tot} = 6.02n + 1.76 + 10log_{10}(m) \tag{5.3}$$

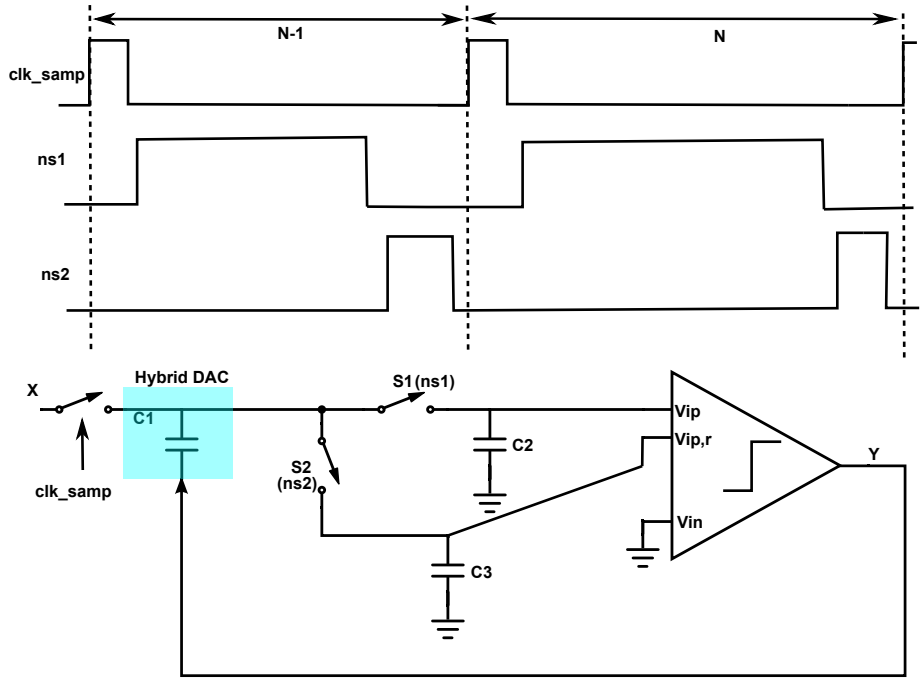


Figure 5.2: Schematic of NS operation in a hybrid DAC SAR ADC.

where, m is OSR and it is given by $\frac{F_s}{2*BW}$. From (5.3), it can be observed that the SNR$_{tot}$ increases by 3dB whenever the value of m doubles. Moreover, if oversampling is used along with NS, it can improve the SNR$_{tot}$ further to achieve higher resolution. Therefore, a second-order NS hybrid DAC SAR ADC is proposed to improve the resolution of the ADC at a higher signal bandwidth and shape the non-linearities associated with the ADC blocks (noise, mismatch, settling etc.) due to the absence of accurate noise and mismatch models with oxide TFTs. The architecture is shown in Figure 5.2 [101] is employed in hybrid DAC SAR ADC for implementing second-order NS passively using switched capacitor circuit. It should be noted that for simplicity, the NS operation is explained using a single-ended architecture, as shown in the figure. Apart from the DAC capacitance ($C1$), two additional capacitors $C2$ and $C3$ are employed along with two switches $S1$ and $S2$, which are controlled by $ns1$ and $ns2$. The sampling phase begins when the clock signal clk_samp transitions from logic '0' level to logic '1' level. As a result, the input signal (X) is sampled on the DAC capacitor $C1$, while $ns1$ and $ns2$ are at logic '0' level, which disconnects $C2$ and $C3$ from $C1$. Once the sampling phase is over (when clk_samp is at logic '0' level), $ns1$ moves to logic '1' level and turns ON switch $S1$ to permit charge-redistribution between $C1$ and $C2$ before the onset of conversion process by the DAC. Moreover, the $ns2$ is at logic '0' and $C3$ remains disconnected

from the DAC. The DAC performs the conversion process depending upon the decision of the comparator, and $C1$ and $C2$ remain connected through $S1$ during the conversion phase. In order to perform the NS operation, residue (= difference between the sampled amplitude (*X(n)*) and voltage generated by the DAC corresponding to the digital equivalent of *X(n)*) should be stored on the top plate of $C1$ at the end of the current conversion cycle. As discussed in Chapter-3, once the LSB bit is resolved, its decision is not fed back to the DAC as the ADC resolves the complete bits, and no further switching is required. As a result, correct residue will not be stored on the DAC and NS capacitors. Therefore, to store correct residue on capacitors, one extra switching is required in the DAC, depending on the state of the LSB. Once the LSB switching is complete, the residue will be stored on the top plates of $C1$ and $C2$, and $ns1$ moves to logic '0' to disconnect $C2$ from $C1$. After this step, $ns2$ goes to logic '1' level, and connects $C1$ and $C3$ through switch $S2$. As a result, the remaining residue is accumulated by the capacitor $C3$. Before the onset of next sampling cycle, *i.e.,* when clk_samp moves to logic '1' level, both $ns1$ and $ns2$ are pulled to logic '0' level to disconnect $C2$ and $C3$ from $C1$, while the residue of the current conversion cycle is stored on $C2$ and $C3$. Since the input X and output Y exploit only $C1$ and $C2$, the input and output relation is determined using charge conservation in $C1$ and $C2$. Therefore, the transfer function is given by (5.4).

$$Y(z) = X(z) - \frac{1 - az^{-1}}{1 - a} V_{res}(z), \quad where \;\; a = \frac{C2}{C1 + C2} \tag{5.4}$$

In this case, the equation consists of the residue only due to $C2$. However, there are two residues left on the top plates of $C2$ and $C3$ after conversion process from previous phase. Since the addition of the two paths is done using two different positive inputs of the comparator, these two paths may have different weights. The weight of path with $C2$ is one, while the weight of path with $C3$ is assumed to be γ. As a result, after addition, the final residue $V_{ref,final}$ is give by (5.5)

$$\mathrm{V}_{ref,final}(\mathrm{z})=\mathrm{V}_{res}(z) + \frac{\gamma b z^{-1}}{1-(1-b)z^{-1}} V_{res}(z), \quad where \;\; b = \frac{C1}{C1 + C3} \tag{5.5}$$

Therefore, using (5.4) and (5.5), the final transfer function of the system is given

by (5.6).

$$Y(z) = X(z) + \frac{(az^{-1} - 1)[1 - (1 - b)z^{-1}]}{1 + (\gamma b + b - 1)z^{-1}} \frac{V_{res,final}(z)}{(1 - a)} \tag{5.6}$$

From the final transfer function of the system, it can be concluded that the system has two zeros (*a* and (*1-b*)) and one pole ($1 - \gamma b - b$). If the value of γ is equal to (*1-b*)/*b*, there will be no pole in the system and only two zeros for second-order NS.

The architecture explained in Figure 5.2 is employed in the proposed hybrid DAC SAR ADC as shown in Figure 5.1. The signals for noise-shaping ($ns1$ and $ns2$) in the hybrid DAC SAR ADC are generated using the output from the SAR controller $cl0$. The $cl0$ is passed through three D-FF to generate $flag$, $flag1$ and $flag2$. Using the output from D-FFs and rail-to-rail logic gates like NOR and NOT, $ns1$ and $ns2$ are generated to control the switching action of the NS capacitors $C2$ and $C3$. For proper NS operation, the relation between the capacitors is maintained as $C1$=$C2$=1.5$C3$ with a path gain of 2, which is realized by making the widths of the transistor with residue input to be two times that of the non-residue input transistors in the comparator. As discussed previously, to store the correct residue on the NS capacitors, the decision of the LSB (b_0) should be fed back to DAC. As a result, the DAC has to perform one extra switching corresponding to the decision on b_0, which was not the case with the 5-bit hybrid DAC SAR ADC without NS. As discussed in Chapter-3, for a 5-bit ADC, 2-bit CS coarse and 4-bit MCS fine DAC are employed to build the hybrid DAC. Since for NS architecture, one extra switching is required (for LSB) to store the residue on the capacitors, the hybrid DAC of the SAR ADC has a 3-bit coarse and 4-bit fine DAC, which results in $V_{REF,LSB}$ = $V_{REF,MSB}$/2.

5.2 Blocks Description of Proposed ADC

5.2.1 Linear Bootstrapped Sampling Switch

The schematic and micrograph of the proposed bootstrapped sampling switch [62] with only n-type transistors is shown in Figure 5.3. In the switch, the clock at the gate of the transistor $M1$ is bootstrapped to a voltage $V_{DD} + V_{IN}$ using a capacitor C_{B1} and transistors $M2$-$M7$ to make V_{GS} of $M1$ independent of

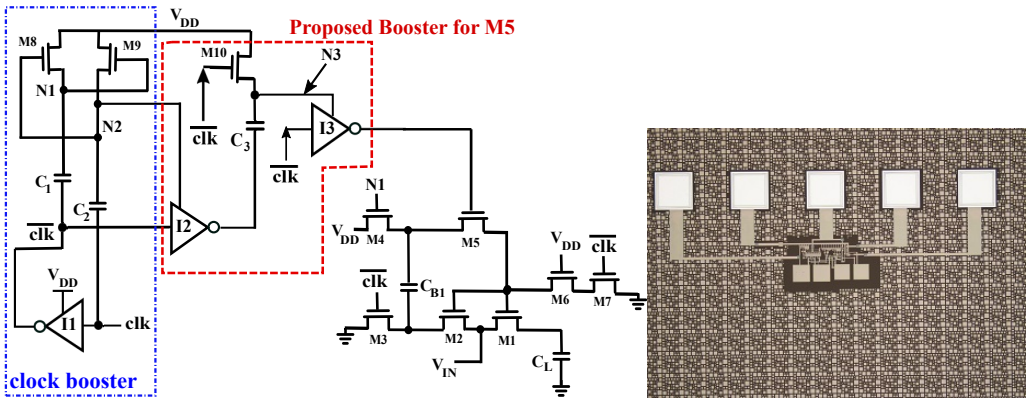


Figure 5.3: Schematic of the proposed sampling switch and its micro-graph.

V_{IN}. A rail-to-rail pseudo-CMOS bootstrapped inverter ($I1$) [102] is used to generate $\overline{clk}$ from clk signal. The switch also employs a clock booster comprises of transistors $M8$-$M9$ and capacitors $C1$-$C2$, to generate signals oscillating between V_{DD} and $2V_{DD}$ at nodes $N1$ and $N2$ from $\overline{clk}$ and clk, respectively. In addition, a clock booster for driving the gate of transistor $M5$ is proposed, which employs two rail-to-rail pseudo-CMOS bootstrapped inverters ($I2$ and $I3$), a transistor $M10$ and a capacitor $C3$. It should be noted that the two inverters ($I2$ and $I3$) take their power supply voltages from nodes $N2$ and $N3$ as shown in Figure 5.3. The operation of the proposed sampling switch is explained using following two phases:

Phase-I: The equivalent circuit of the sampling switch with signals at nodes $N1$ and $N2$ are shown in Figure 5.4(a). In this phase, clk makes a transition from V_{DD} to 0V. As a result, transistors $M3$, $M7$ and $M10$ are turned ON and the output of the inverters ($I2$ and $I3$) will be at logic '0' (=0V). The voltage at node $N1$ (= $2V_{DD}$) is applied to the gate of the transistors $M4$, which charges capacitor C_{B1} to V_{DD} without any V_{TH} drop. Moreover, transistor $M7$ pulls the gate of $M1$-$M2$ to 0V, to turn them OFF in the current phase. Since the output of $I3$ is at 0V, transistor $M5$ is also turned OFF. Thus, the load capacitor C_L is isolated from V_{IN}. In addition, transistor $M10$ charges $C3$ to a voltage equal to $V_{DD} - V_{TH,M10}$.

Phase-II: The equivalent circuit of the sampling switch with signals at nodes $N1$ and $N2$ are shown in Figure 5.4(b). In this phase, clk makes a transition from 0V to V_{DD}. As a result, all the transistors marked with grey colour are turned OFF. Since the input to the inverters $I2$ and $I3$ is 0V, their output will be equal to their power supply voltages. Therefore, output of $I2$ is equal to

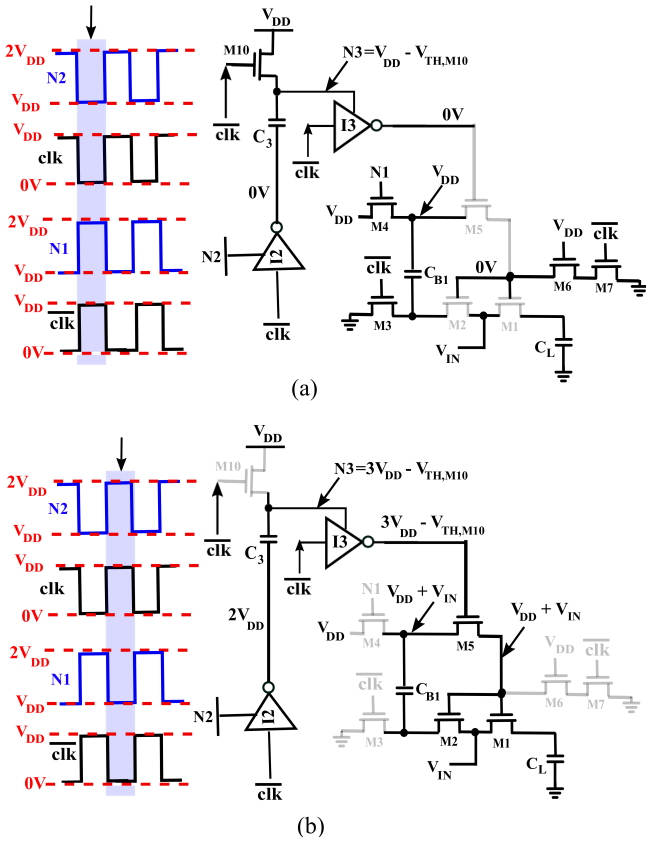


Figure 5.4: Equivalent circuit of the proposed sampling switch in (a) Phase-I and (b) Phase-II.

the voltage at node $N2$ (=$2V_{DD}$), which charges node $N3$ to a voltage equal to $3V_{DD} - V_{TH,M10}$. Since $I3$ takes its power supply voltage from node $N3$, its output will be $3V_{DD} - V_{TH,M10}$ and the gate voltage of transistor $M5$ is boosted in the current phase. As a result, transistor $M5$ is turned ON and it initially passes V_{DD} at the gates of $M1$-$M2$ to turn them ON. Since transistor $M2$ is turned ON, it charges C_{B1} to a voltage $V_{DD} + V_{IN}$ and finally, transistor $M5$ passes complete $V_{DD} + V_{IN}$ to the gate of $M1$-$M2$ without any V_{TH} drop. As a result, V_{GS} of $M1$ will be a constant voltage (=V_{DD}) and R_{ON} will be almost constant over the complete amplitude range of V_{IN}, which can ensure the desired performance without using wider transistor. Moreover, the maximum amplitude of V_{IN} can be as high as V_{DD}. Thus, the proposed linear sampling switch mitigates the limitations of n-type pass transistor switch with oxide TFT technology.

Results and Discussions:
The TFTs employed in the circuit has a channel length of 2μm. The switch is simulated at a V_{DD} of 2V, a sampling frequency of 50kHz and an input signal fre-

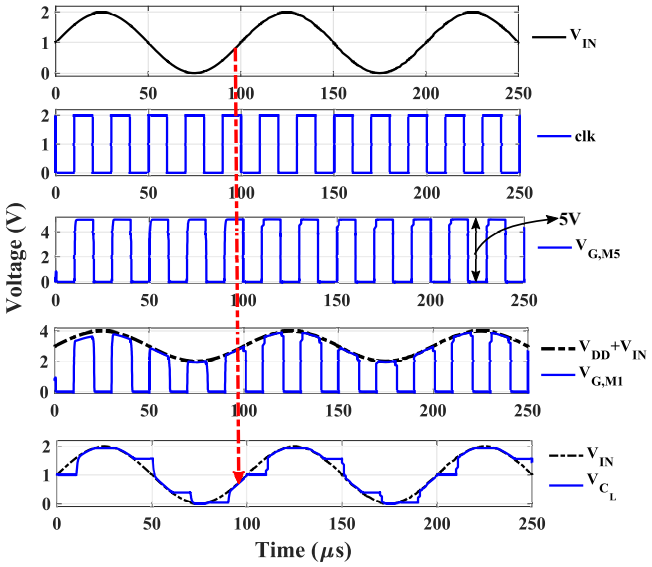


Figure 5.5: Voltage at different nodes of the proposed switch.

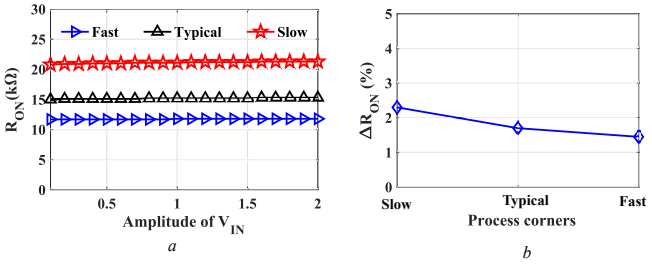


Figure 5.6: Variations across process corners for (a) R_{ON} and (b) ΔR_{ON}.

quency of 10kHz with full-scale range (0V to V_{DD}). The value of load capacitor C_L is kept at 10pF for all the simulations.

The gate voltages of transistors $M1$ ($V_{G,M1}$) and $M5$ ($V_{G,M5}$) were obtained from the transient simulations and they are shown in Figure 5.5. It is observed from the figure that $V_{G,M5}$ is boosted to a voltage close to 5V when clk is at logic '1' (=V_{DD}), which is 0.4V less than the expected result of $3V_{DD} - V_{TH,M10}$. This voltage drop of 0.4 is accounted for the parasitcs at node $N2$, which degrades $V_{G,M5}$. However, $V_{G,M5}$ is large enough to pass the voltage $V_{DD} + V_{IN}$ to $V_{G,M1}$ as can be seen from Figure 5.5. As a result, $V_{GS,M1}$ is made almost independent of the amplitude of V_{IN}. In addition, the maximum amplitude of V_{IN} can be as high as V_{DD}. The red arrow in the figure highlights the transient gate voltages when clk is at V_{DD}. Besides, it also shows that C_L is correctly tracking the input analog signal.

The transient simulations were performed by sweeping the input amplitude of V_{IN} from 0V to 2V (full-scale range) in a step size of 0.1V. The obtained

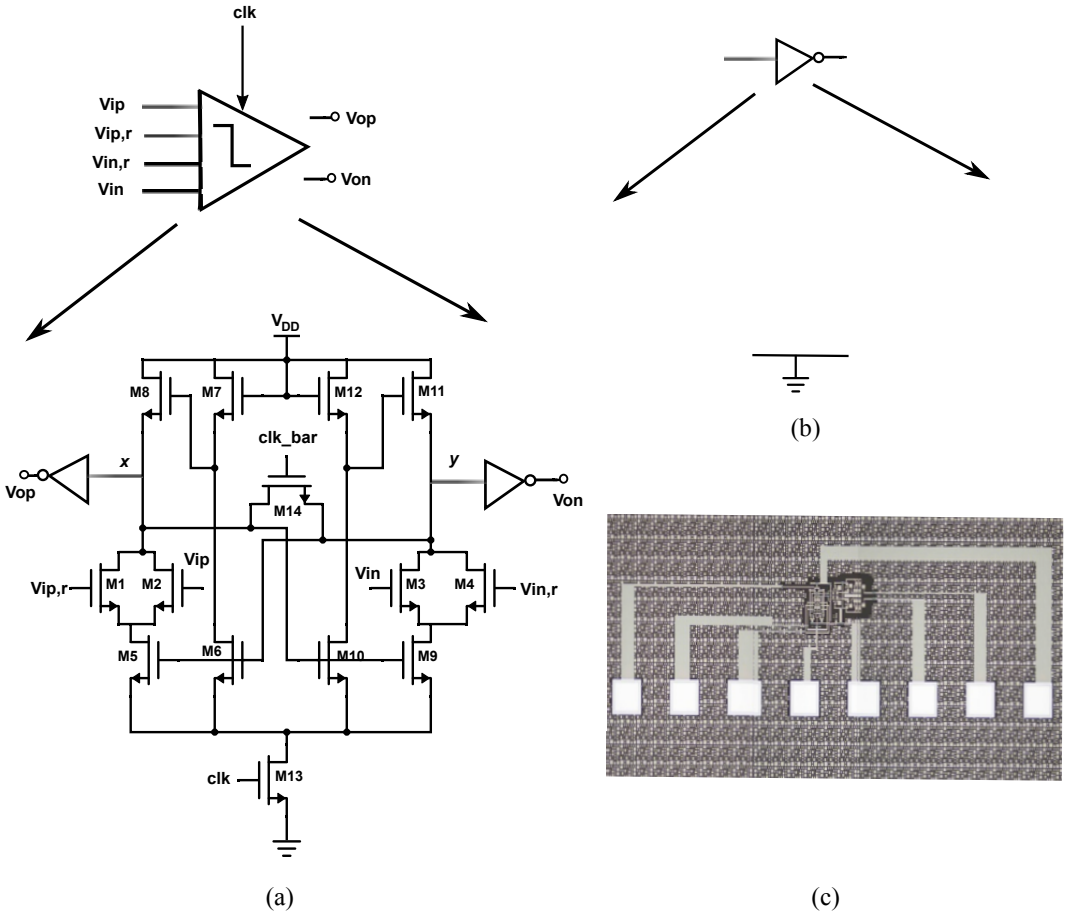


Figure 5.7: Circuit schematic of (a) Proposed comparator (b) Rail-to-rail pseudo CMOS inverter and (c) Micro-graph of complete comparator.

value of R_{ON} from simulations is shown in Figure 5.6(a). The figure shows R_{ON} values at different process corners (slow, fast and typical). In order to study the percentage variations in R_{ON}, ΔR_{ON} is calculated using (4.7) at different process corners, and the plot is shown in Figure 5.6(b). It is observed from Figure 5.6(b) that variations upto 2.2% in R_{ON} have been observed when the simulations were performed at different process corners. It should be noted that the observed percentage variations in R_{ON} is very low considering the large device parasitics of the oxide TFTs.

5.2.2 Proposed 4-input Comparator

In order to have a second-order noise-shaping characteristic in the hybrid DAC SAR ADC, a comparator is proposed with all enhancement n-type transistors, and its schematic is shown in Figure 5.7. It has two additional inputs for residue

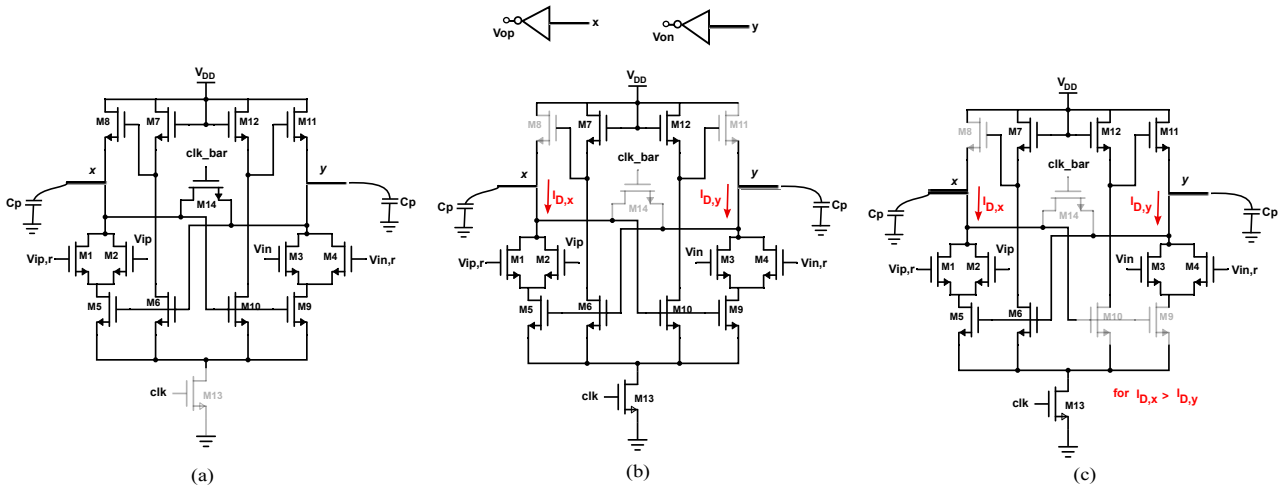


Figure 5.8: **Equivalent Circuit of the proposed comparator in (a) Reset phase (b) Amplification phase (c) Regeneration phase.**

amplification $V_{IP,r}$ and $V_{IN,r}$, along with the two regular inputs, which are represented as V_{IP} and V_{IN}. The residue from the previous state is added by adding the current produced by transistors $M1$ and $M2$ in x branch, and $M3$ and $M4$ in y branch. The operation of the comparator is controlled by clock signal clk. Transistor $M14$ is used to reset the comparator when clk is at logic '0'. As a result, the gate of $M14$ is connected to clk_bar, which is obtained from clk using rail-to-rail pseudo CMOS inverter shown in Figure 5.7(b). The final outputs (V_{op} and V_{on}) of the comparator are obtained using two rail-to-rail pseudo CMOS bootstrapped inverters. The layout of the comparator is presented in Figure 5.7(c). It occupies an active area of about $0.044mm^2$.

Working Principle: The working principle of the comparator can be understood in three phases: *reset*, *amplification* and *regeneration* phases, which are depicted in Figure 5.8. In the figure, transistors represented in gray colour are in OFF state in the respective phases.

Reset Phase: The equivalent circuit of the comparator in this phase is shown in Figure 5.8(a). This phase begins when clk goes to logic '0'. As a result, $M13$ is turned OFF and $M14$ is turned ON. Transistor $M14$ shorts nodes x and y to a voltage close to 0.5 times V_{DD} (considering equal parasitics at nodes x and y). At the end of this phase, both the outputs of the comparator (V_{op} and V_{on}) are at logic '0'.

Amplification and Regeneration Phases: The equivalent circuit of the comparator in this phase is shown in Figure 5.8(b)-(c). If transistors $M1$ to $M4$ are

removed, transistors $M5$ to $M8$, and $M9$ to $M12$ form two separate pseudo-CMOS inverters, which are connected in a cross-coupled fashion to perform the latching operation. The transistors $M1$ to $M4$ are introduced to control the current through these cross-coupled inverters depending upon the amplitude of input signals (V_{ip} and V_{in}). The amplification phase begins when clk goes to logic '1'. As a result, $M13$ is turned ON, and $M14$ is turned OFF. Depending upon the voltage levels of the input signals (V_{ip} and V_{in}) and the residues ($V_{ip,r}$ and $V_{in,r}$), respective drain currents flow through transistors $M1$ to $M4$, which have an amplitude equal to transconductance times the input voltage of the respective transistors. While the drain currents of $M1$ and $M2$ are added in the branch containing node x, drain currents of $M3$, and $M4$ are added in the branch containing node y. Moreover, transistors $M5$, $M6$, $M9$ and $M10$ are also in ON state as their gates are connected to nodes x and y, respectively, which are charged to a voltage greater than V_{TH} of these transistors during the reset phase. As a result, the gates of $M8$ and $M11$ are pulled down to ground level, and they are turned OFF. Now, when there is a small differential voltage between the gates of $M1$ and $M4$, and/or $M2$ and $M3$, the corresponding drain current varies, which causes the node capacitances of x and y to discharge at a different rate. As a result, voltages at these nodes drop at different rates. Since the node voltages at x and y are decreasing at different rates depending upon the current flowing in their respective branch, the one to reach a voltage less than V_{TH} of $M5$ or $M9$ earlier will make $M5$, $M6$ or $M9$, $M10$ to turn off first. For example, if V_x reaches a voltage less than V_{TH} earlier compared to V_y, then $M9$ and $M10$ will turn OFF first. The regeneration phase begins turning OFF $M9$ and $M10$ to push V_y towards V_{DD}, and due to cross-coupling action, transistors $M5$ and $M6$ will be turned ON, and they quickly pull down x to ground. As a result, the final voltages at nodes x and y will be close to V_{DD} and ground. Therefore, the polarity of the input differential voltage decides which nodes (x and y) will be close to V_{DD} and ground. It should be noted that due to the inherent V_{TH} drop of transistors $M7$ and $M12$, the logic high level at node x or y can be close to V_{DD} but, it cannot be equal to V_{DD}. Therefore, V_{on} and V_{op} are obtained by passing voltages at nodes x and y to the rail-to-rail pseudo CMOS inverter (shown in Figure 5.7(b)) to get the complete swing (from 0V to V_{DD}) at the output.

Results and Discussions:
The TFTs employed in the circuit have a channel length of 4μm. Transient post-layout simulations were performed to study the behavior of the comparator

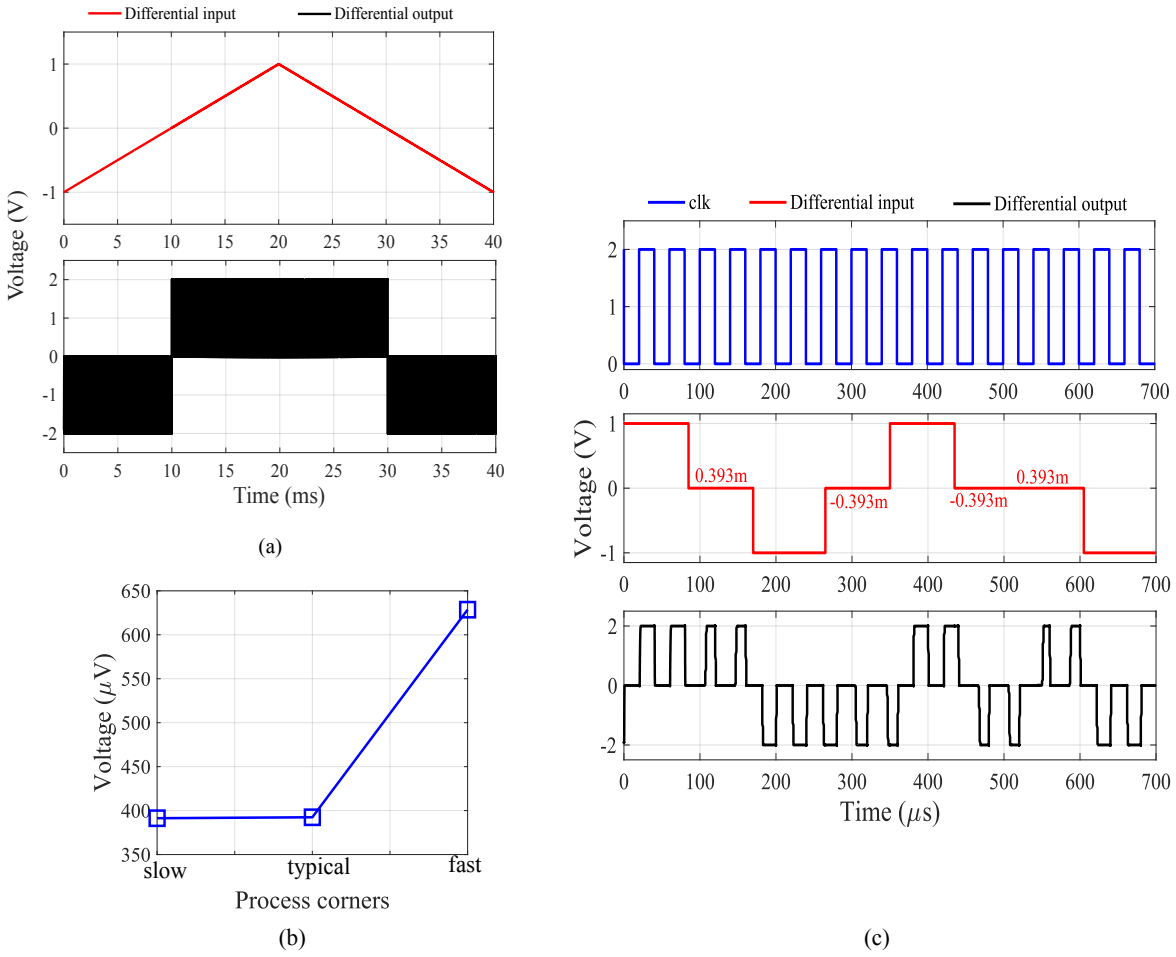


Figure 5.9: Post-layout simulation results of proposed comparator (a) with slow ramp wave (b) Comparator resolution against process corners (c) with worst-case differential input under typical condition.

at a clock frequency of 25kHz. A stimulus with a slowly rising ramp followed by a slow falling ramp is used to identify the static offset of the comparator. The stimulus and the response of the comparator to ramp signal are presented in Figure 5.9(a). The offset of the comparator from this setup has been calculated as 0.393mV under the typical case. The calculated offset against different process corners is presented in Figure 5.9(b). It can be noticed from this figure that the comparator's offset does not exceed 0.63mV under the worst-case process corner. In order to depict the dynamic behavior of the comparator, a fully differential signal with a sequence of worst-case inputs has been applied to the comparator as shown in Figure 5.9(c). It can be observed from the figure that the comparator decides correctly within the worst-case regeneration time of around 1.5μs. In addition, it can detect accurately if the magnitude of the input differential signal is $\geq$ 0.63mV. The power consumption of the comparator has been calculated as 19μW.

Table 5.1: Comparison of the proposed comparator with state of the art work in Oxide TFT technology

Comparator Design	Supply Voltage (V)	Resolution (mV)	Operating Frequency(kHz)	Power Consumption (mW)	Active area (mm^2)
[94](2015)$^{+}$	10	40	50	3.8	-
[103](2017)**	15	500	31.25	-	0.050
[104](2018)$^{+}$	10	50	-	0.3	-
[105](2020)$^{+}$	10	50	50	0.248	-
[95](2021)$^{+}$	10	60	10	0.497	-
This Work*	**2**	**0.63†**	**25**	**0.019**	**0.044**

$^{+}$Simulation results, *Post-layout simulation results, **Measured, †under worst-case process corner

Next, the performance of the proposed comparator has been compared with other state of the artwork with oxide TFTs in Table 5.1. It can be observed from the table that the proposed comparator achieves a resolution of 0.63mV (under worst-case process corner), which is small compared to the state of the artwork at a very low supply voltage of 2V without much degradation in the operating frequency.

5.2.3 SAR Logic Controller and Proposed Clock Booster

5.2.3.1 SAR Logic Controller

This block is designed with shift registers and basic logic gates. The block diagram of the SAR controller for 5-bit hybrid DAC SAR ADC (b_4-b_0) is shown in Figure 5.10. The controller is reset using *reset* pin. It takes the output from the comparator as input to resolve the bits. The comparator output is connected to $comp\_out$ pin of the controller, and its operation is controlled using the clock signal clk_sar. It comprises two rows of shift registers. The first row of the shift register is clocked using clk_sar. The outputs from the first row of the shift register ($cl0$-$cl4$) are used as clock signals by the second row of the shift register to produce output bits. These output bits are produced on every rising edge of clk_sar depending on the state of $comp\_out$. During the sampling phase, none of the bits should connect the CS DAC capacitors to the input of the comparator. Moreover, MCS DAC capacitors should be connected to the common-mode voltage. In order to make $\overline{b}_4$-$\overline{b}_0$ to logic '0' during the sampling phase, a set of even number of cascaded inverter stages are used as a delay element along with full swing NOR and $NAND$ gates to obtain the complementary output bits. The configuration is shown in Figure 5.10. If inverters are used to obtain the

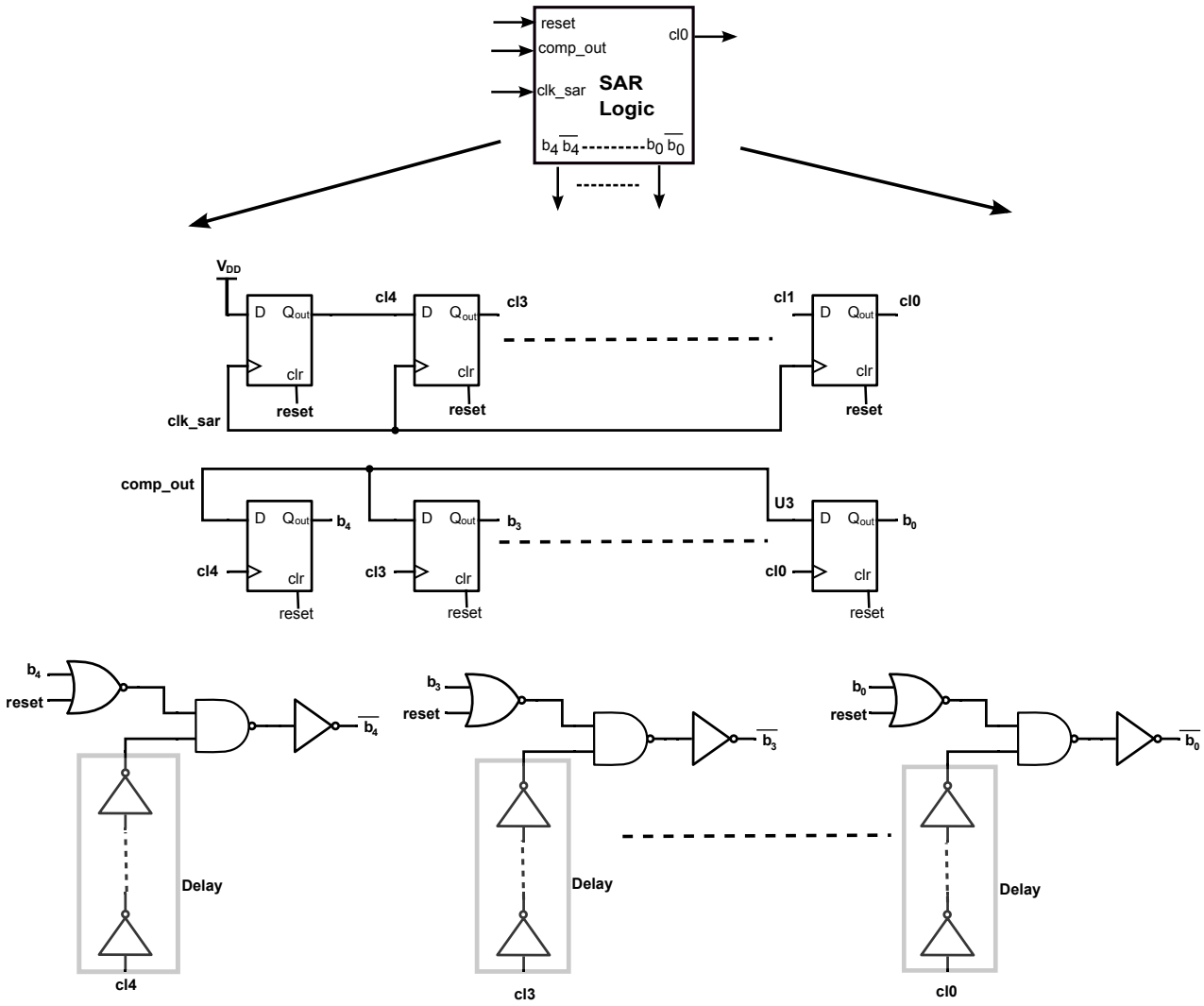


Figure 5.10: Block diagram of SAR Logic Controller.

complementary bits of b_4-b_0, then during the sampling phase, when b_4-b_0 bits are reset to ground, $\overline{b}_4$-$\overline{b}_0$ will be at logic '1'. As a result, the bottom plates of MCS DAC capacitors will be simultaneously connected to V_{CM} and V_{REF} or ground depending upon which voltage is passed using $\overline{b}_4$-$\overline{b}_0$. Similarly, the CS DAC capacitors will see two connections, V_{REF} and the inputs of the comparators, which results in shorting the inputs of the comparator to V_{REF} during the sampling process. This can disturb the sampling process and make the sampled voltage incorrect. Therefore to avoid this situation, NOR gates are used with $reset$ and b_4-b_0 as inputs. The output of the NOR gates gives the correct result when the decision on b_4-b_0 is logic '0'. However, if this decision is logic 1', there will be a glitch in $\overline{b}_4$-$\overline{b}_0$ due to finite rise and fall time of b_4-b_0 and $reset$. To avoid the glitch, $cl0$-$cl4$ are delayed using a set of even number of cascaded

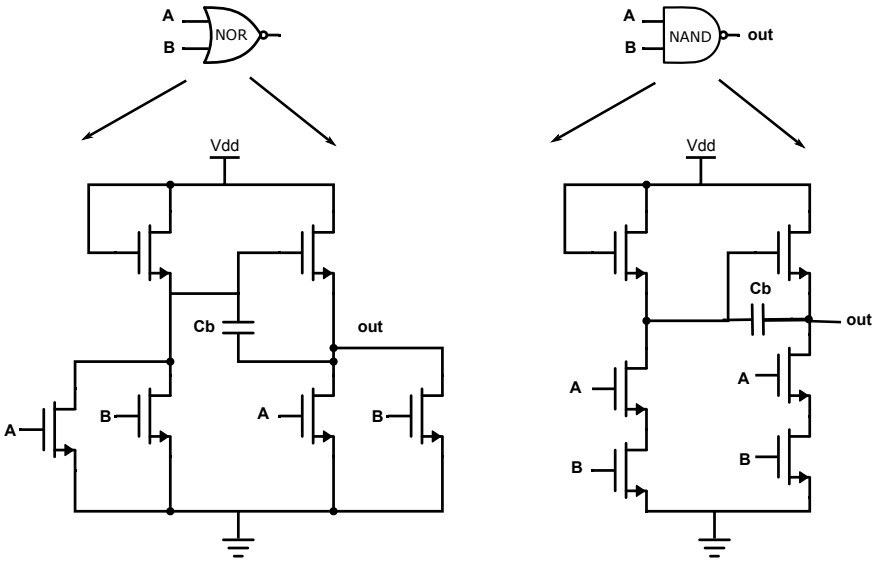


Figure 5.11: Circuit schematic of NOR and NAND gates.

inverter stages. The delayed $cl0$-$cl4$ signals and the output from the NOR gates are passed as inputs to the AND gates (formed by $NAND$ gate and an inverter) to generate $\overline{b}_4$-$\overline{b}_0$. The circuit schematic of NOR and $NAND$ gates are shown in Figure 5.11 and their working principle is described next.

Rail-to-Rail Logic Gates:
Logic gates are basic building blocks in the SAR controller. Therefore, this section focuses on novel logic gates [102], which can give rail-to-rail output voltage swing. Inverter and NAND gates circuit schematics and micrographs with diode connected load and pseudo CMOS configurations are presented in Figure 5.12. The newly proposed gates, where a switch is added for each input to the bootstrapping capacitive load are depicted in Figure 5.13. For the inverter, output rails are given by: diode load (5.7), pseudo cmos (5.8), capacitive bootstrapping load (5.9) and high performance gates (5.10).

$$V_{OHd} \approx V_{DD} - V_{TH}; V_{OLd} \approx V_{DD} - (\frac{1}{g_{mT2}} \cdot I_{DS}) \tag{5.7}$$

$$V_{OHcm} \approx V_{DD} - 2V_{TH}; V_{OLcm} \approx V_{DD} - (r_{offT4} \cdot I_{DS}) \tag{5.8}$$

$$V_{OHbs} \approx V_{DD}; V_{OLbs} \approx V_{DD} - (r_{dsT2} \cdot I_{DS}) \tag{5.9}$$

$$V_{OHprop} \approx V_{DD}; V_{OLprop} \approx V_{DD} - (r_{offT2} \cdot I_{DS}) \tag{5.10}$$

where V_{OH} and V_{OL} are output logic high and low levels, respectively, whereas, r_{ds} and r_{off} are output/drain to source resistance and effective off resistances of the TFT, while g_m represents transconductance of the transistor. The subscripts d, cm, bs and $prop$ represent different logic gate configurations, namely, diode load based, pseudo cmos, bootstrapping load based and proposed gates.

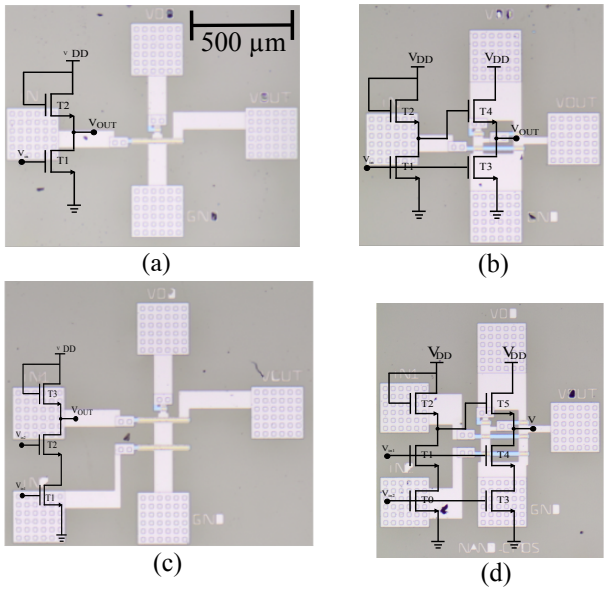


Figure 5.12: Conventional logic gates circuit schematics and micrographs using IGZO TFTs: (a) Inverter with diode load (b) Inverter in pseudo CMOS configuration (c) NAND with diode load (d) NAND in pseudo CMOS configuration.

As per (5.7), an inverter based on diode load (Figure 5.12(a)) limits the swing and demands higher driver size compared to the load to favour some gain. On the other hand, the pseudo CMOS configuration limits the V_{OH} value as per (5.8). The bootstrapped inverter (Figure 5.13) can ensure V_{OH} very close to V_{DD} value due to capacitive bootstrapping operation as the voltage at node v_1 is almost $2V_{DD}$ - V_{TH} - V_{OL}, where V_{TH} refers to the threshold voltage of the biasing transistor T3. However, V_{OL} is limited as per (5.9). In the bootstrapping inverter, by introducing a switch (S_1) between node v_1 and ground, which is controlled by the same input as the inverter, the logic low level can be made almost zero, when the input is logic '1'. For this condition, the switch closes and v_1 is pulled down to ground potential. Therefore, T2 will be turned off, turning the effective load resistance (r_{off}) very high. This leads to complete rail-to-rail operation (V_{OH} = V_{DD} and V_{OL} = V_{SS}/Gnd). Here the switch is implemented with a n-type oxide TFT. The same explanation exists for rail-to-rail NOR gate as well, which along-with with inverter and NAND gates, is used for implementation of the complete SAR logic controller block.

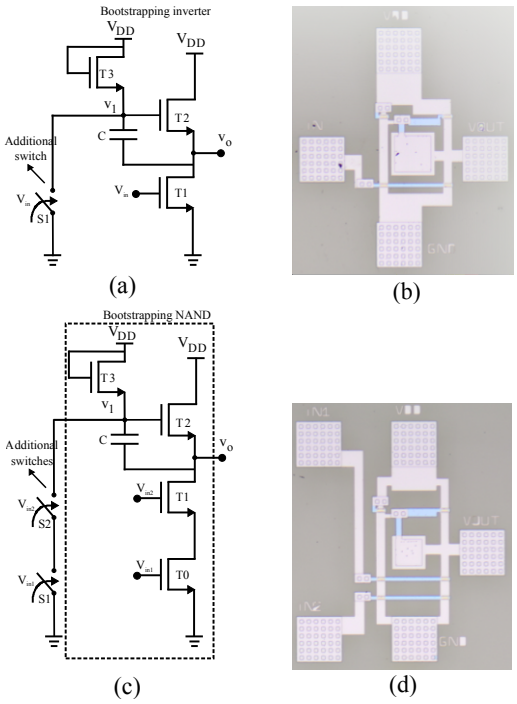


Figure 5.13: High performance logic gates formed by adding a switch for each input to the bootstrapping capacitive load (a) Inverter circuit schematic (b) Inverter micrograph (c) NAND circuit schematic (d) NAND micrograph.

Proposed D-type flip flop:

To construct the shift register for the SAR controller, a compact D-type flip flop (D-FF) has been proposed, whose schematic is shown in Figure 5.14. Transistors $M4$ and $M5$ act as an inverter, which performs the inversion process for clock signal clk_df. Moreover, transistors $M15$ to $M18$ and bootstrapping capacitor Cb act as a rail-to-rail pseudo CMOS inverter to obtain full-swing at the output of the flip-flop. In addition, transistor $M14$ is used to reset the flip-flop to logic '0' if the clr pin is set at logic '1'. The operation of the D-FF can be understood in two phases assuming clr is at logic '0':

Phase I: In this phase, clk_df is at logic '0', which turn ON $M2$ and $M8$, while $M5$, $M6$ and $M12$ are in OFF state. Since $M2$ is in ON state, $M1$ and $M3$ forms a diode-connected inverter, and node x is either charged closed to V_{DD} or discharged to ground depending upon whether input D is at logic '0' or logic '1'. Moreover, node y is charged to V_{DD} by $M8$ and turns ON $M10$. As a result, $M13$ is turned OFF. Since $M12$ is in OFF state, the state of input D is not reflected at the output Q_{out}, and the flip-flop holds its previous state.

Phase II: In this phase, clk_df makes a transition from logic '0' to logic '1' and turns ON $M6$ and $M12$, which turn OFF $M2$ and $M8$. As a result, the changes in D will not reflect node x. Depending upon the state of x in the previous state,

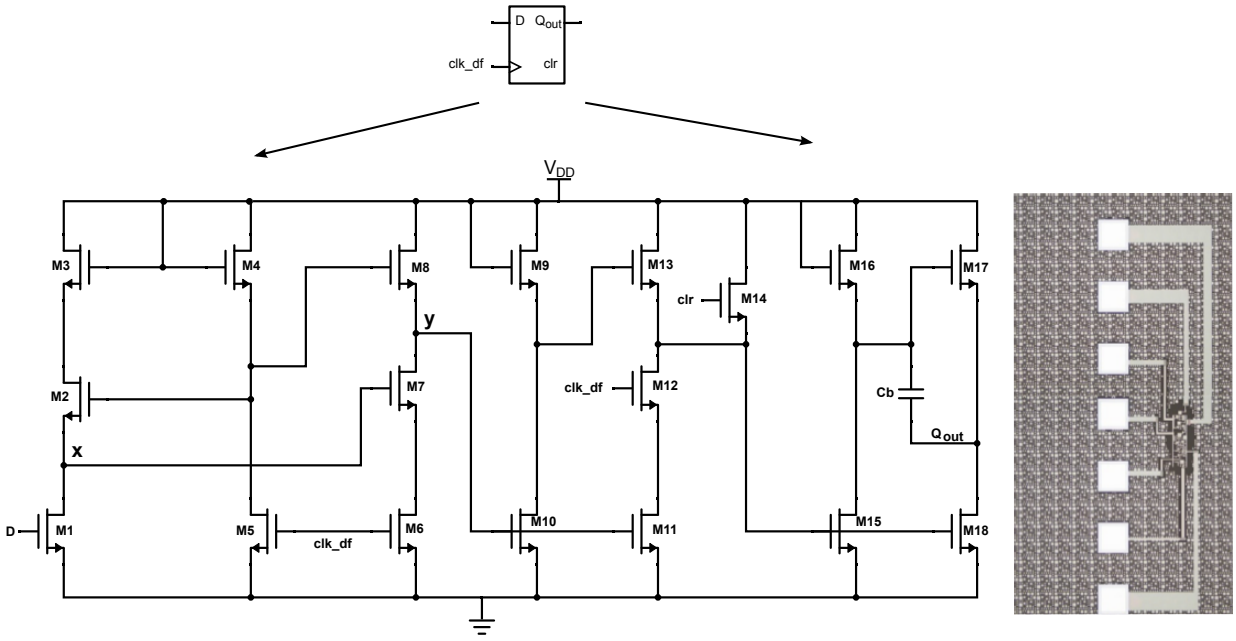


Figure 5.14: Circuit schematic and micro-graph of the proposed D-FF.

say if x is close to logic '1' (logic '0'), $M7$ is tuned ON (OFF), making y to discharge to the ground (or remain close to V_{DD}). Since $M12$ is in ON state, $M9$ to $M13$ form a pseudo-CMOS inverter, whose output is again given to the input of the rail-to-rail pseudo-CMOS bootstrapped inverter formed by $M15$ to $M18$ along with bootstrapping capacitor Cb. As a result, the proposed D-FF follows the change in input D only on the rising edge of clk_df.

5.2.3.2 Clock Booster

The proposed clock booster [63] is used to boost the voltage level from the output of the SAR Logic controller before connecting it to the gate of the n-type transistor switches of the DAC. It employs rail-to-rail inverter (see Figure 5.7(b)) . The circuit schematic of the proposed on-chip clock booster is shown in Figure 5.15. The operation of the clock booster can be understood in two phases (with respect to $b/\overline{b}$ signal):
Phase-I $\{b/\overline{b}$=0V$\}$: Inverter $I1$ makes $V1$ equal to V_{DD}. Therefore, outputs of $I2$, $I3$ and $I4$ are 0V. As a result, $M9$ and $M10$ are turned on and charge capacitors, $C9$ and $C10$, close to V_{DD}-V_{TH}, respectively, considering $M9$ and $M10$ to be identical. Thus, $V2$ and $V3$ will be equal to V_{DD}-V_{TH}. At the end of this phase, Out will be 0V (=output of $I4$). Next, the clock booster moves into phase-II.

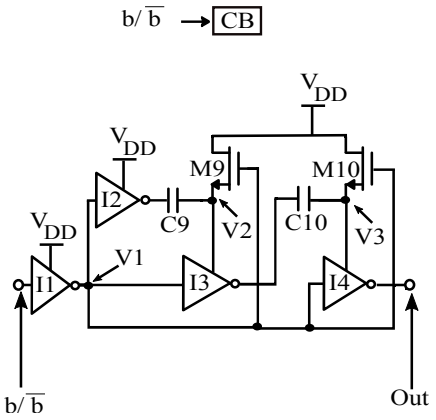


Figure 5.15: Circuit schematic of the proposed clock booster.

Phase-II {$b/\bar{b}$=V_{DD}}: $I1$ makes $V1$ equal to 0V. As a result, $M9$ and $M10$ are turned off and output of $I2$ is at V_{DD}, which raises $V2$ close to $2V_{DD} - V_{TH}$ (=V_{DD} + $V2_{phase-I}$). $V2$ acts as a supply source for $I3$ and makes $V3$ close to $3V_{DD} - 2V_{TH}$ (=$2V_{DD} - V_{TH}$ + $V3_{phase-I}$). Since $V3$ act as a supply source for $I4$, therefore, a final output (= Out) close to $3V_{DD} - 2V_{TH}$ is observed.

The booster is designed to generate $3V_{DD} - 2V_{TH}$ to compensate the V_{TH} drop in the final result and also, the degradation due to the parasitcs at the node voltages.

5.2.3.3 Results and Discussions

The TFTs employed in the circuit have a channel length of 4μm. The D-FF and a 5-bit shift register are simulated using V_{DD} of 2V and clock frequency of 25kHz. The transient post-layout simulation result of D-FF is presented in Figure 5.16(a), which shows the correct behavior of positive-edge triggered D-FF. As can be seen from the figure that the D-FF reflects the input D only at the rising edge of the clock signal clk_df. The propagation delay of the flip-flop has been calculated as 0.85μs with a power consumption of around 11.74μW. Using the proposed D-FF, a 5-bit shift register is designed, which shares a common clock signal clk_sr, and the output of the preceding DFF is the input of the next DFF (similar to the first row of DFF in SAR logic shown in Figure 5.10) before using it in a SAR controller. The post-layout simulation result of the shift register is shown in Figure 5.16(b), where correct shifting operation can be observed. The performance of the 5-bit shift register designed using the

proposed D-FF is compared with other state-of-the-artwork, and the result is summarized in Table 5.2. It should be noted that the work reported in [106] is limited to schematic simulation results and does not account for the degradation in performance of the shift register due to the interconnect parasitics. Therefore, it can be concluded that compared to state-of-the-artwork, the proposed shift register delivers excellent performance at low supply voltage and with a small device channel length without compromising on the operating frequency. The

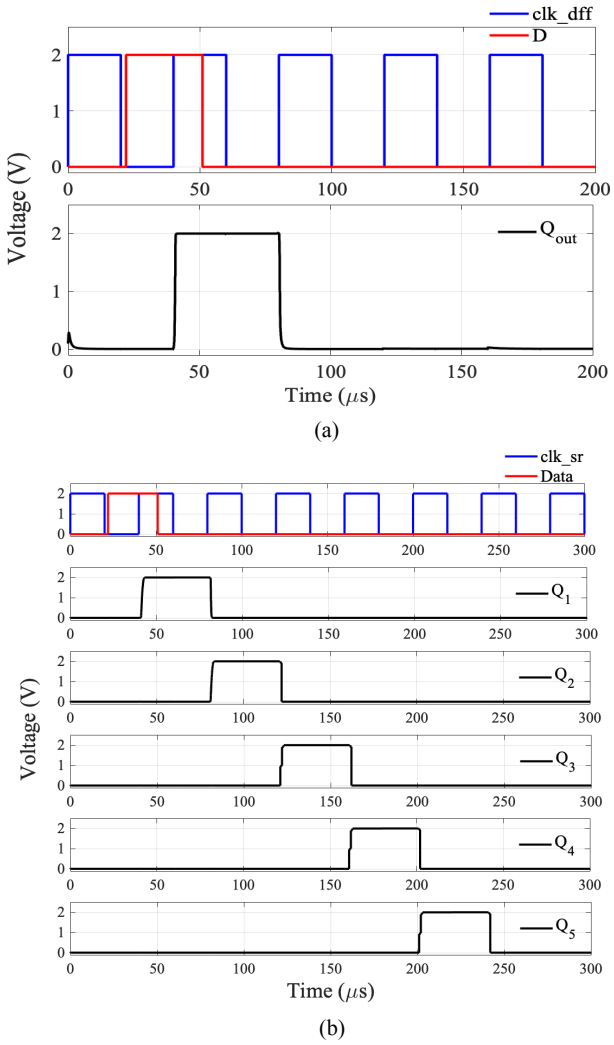


Figure 5.16: Post-layout simulation results (a) Proposed D-FF (b) 5-bit shift register.

post-layout simulation of the complete SAR controller for the 5-bit SAR ADC is performed at a clock frequency (clk_sar) of 25kHz, and the plot is presented in Figure 5.17. It is observed from the plot that the SAR controller delivers correct bits on every rising edge of clk_sar depending upon the state of $comp\_out$. Moreover, in the reset phase, all the bits (b and its complement $\overline{b}$) are reset to

Table 5.2: Comparison of the proposed shift register with state of the art work in Oxide TFT technology.

Parameters	[107] (2010)	[108] (2011)	[109] (2010)	[110] (2012)	[111] (2014)	[112] (2015)	[106]$^{+}$ (2018)	[102] (2020)	**This work***
Supply Voltage (V)	20	20	30	2	26	20	2	8	**2**
Operating frequency (kHz)	40	13.9	13.2	5	22.1	0.24	20	1	**25**
Device Channel Length (μm)	10	10	10	10	11	11	2	10	**4**
Power Consumption (μW)	-	1670	3800	-	-	-	72.15	820	**29.35**

$^{+}$Schematic simulation results, *Post-layout simulation results

logic '0' state, which is required for the proper functioning of the SAR ADC. In addition, the output bits from the logic controller have complete rail-to-rail swing due to the employment of full-swing logic gates discussed previously.

5.3 Results and Discussions of Proposed ADC

The proposed ADC is designed with a channel length not exceeding 4μm and supply voltage of 2V. The post-layout transient simulations have been performed at a sampling frequency close to 3kHz, and with an OSR of 4. The complete ADC occupies an active area of 6.6mm^2. The value $V_{REF,MSB}$ and $V_{REF,LSB}$ are calculated as 2V and 1V. Moreover, the value of unit capacitance is taken as 2pF.

First to check the correct operation of the ADC, transient simulations have been performed for fixed input voltages (1.9V and 0.1V). The obtained result is presented in Figure 5.18(a). It can be concluded from the figure that the comparator input voltage converges near to the common mode voltage (=1V), which is an expected behavior of the ADC as discussed in chapter-3. Next, transient simulation of the ADC is performed using a full-scale sinusoidal signal with an input frequency close to 100Hz to collect 4096 FFT bins for the construction of the ADC spectrum, which is shown in Figure 5.18(c). The output spectrum of the ADC shows signal-to-noise-and-distortion-ratio (SNDR) and spurious-free-dynamic-range (SFDR) of 44.1dB and 57.7dB, respectively. In addition, the effective resolution (ENOB) of the ADC came out to be 7 bits, which shows nearly 2 bits addition to a 5-bit SAR ADC due to noise-shaping

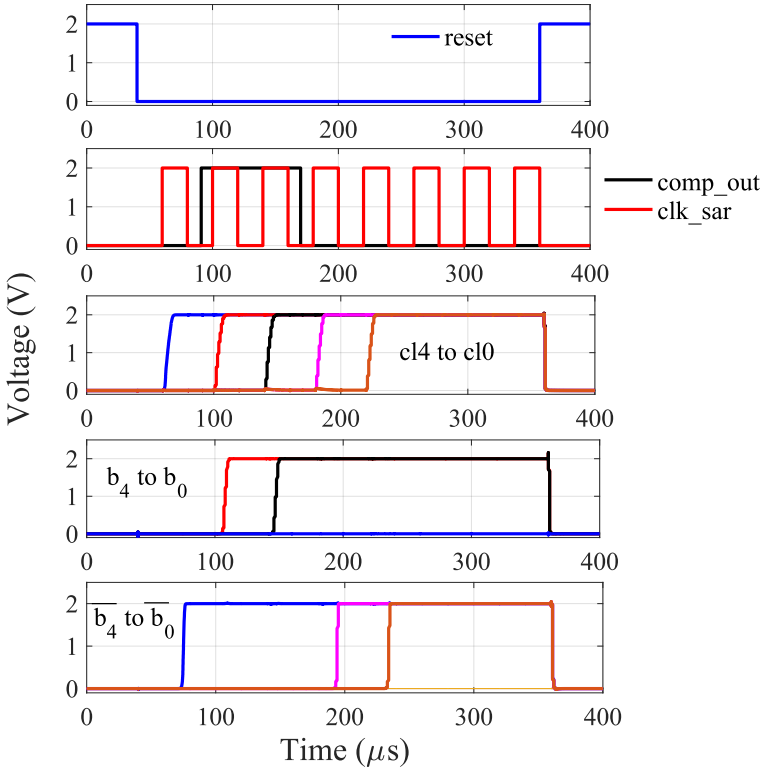
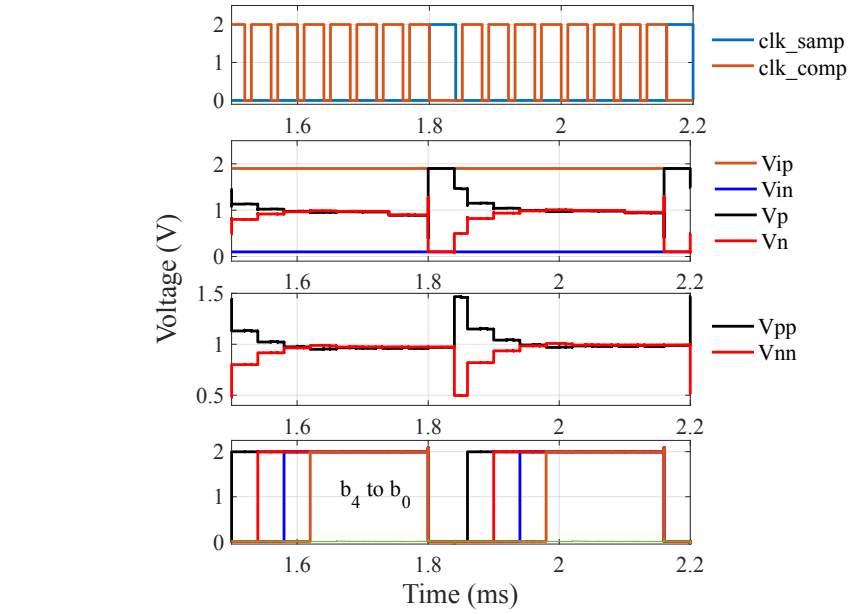


Figure 5.17: Post-layout simulation result of the complete SAR logic controller.

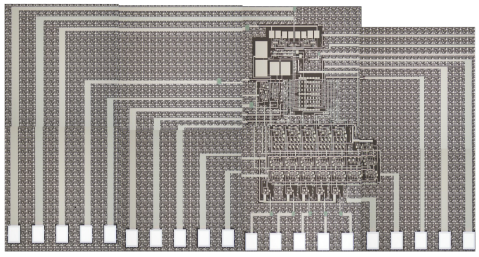
process. The power consumption of the ADC has been calculated as 5mW and the power distribution by each block is shown in Fig. 5.19. The performance of the proposed ADC is compared with other reported ADC with Oxide TFT technology and it is summarized in Table 5.3. It can be seen from the table that the proposed ADC delivers least Figure-of-Merit (FoM) compared to other reported work in the same technology. Though [95] reports effective resolution of the ADC to be 11.2 bit (with schematic simulations), but the ADC is designed using passive components and with only comparator and buffers on-chip. However, the current work integrates all the blocks of the ADC on-chip and delivers excellent performance compared to the state of the art work in the same technology.

5.4 Conclusions

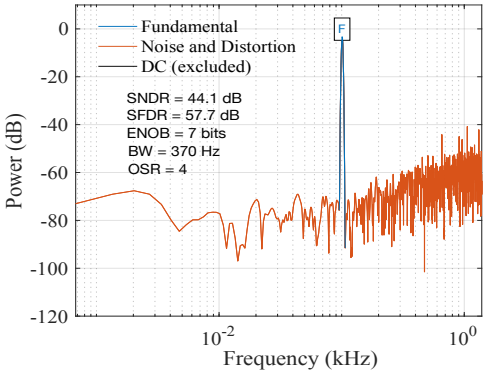
This chapter presented the detailed design of the proposed NS hybrid SAR ADC with oxide TFT technology. The NS process is introduced to suppress the comparator noise, mismatch errors, quantization noise etc. As a result, the 5- bit ADC is able to deliver a resolution of 7-bits from the post layout simulations.



(a)



(b)



(c)

Figure 5.18: NS Hybrid DAC SAR ADC (a) Post-layout simulation results, (b) Micro-graph, (c) Spectrum of the ADC.

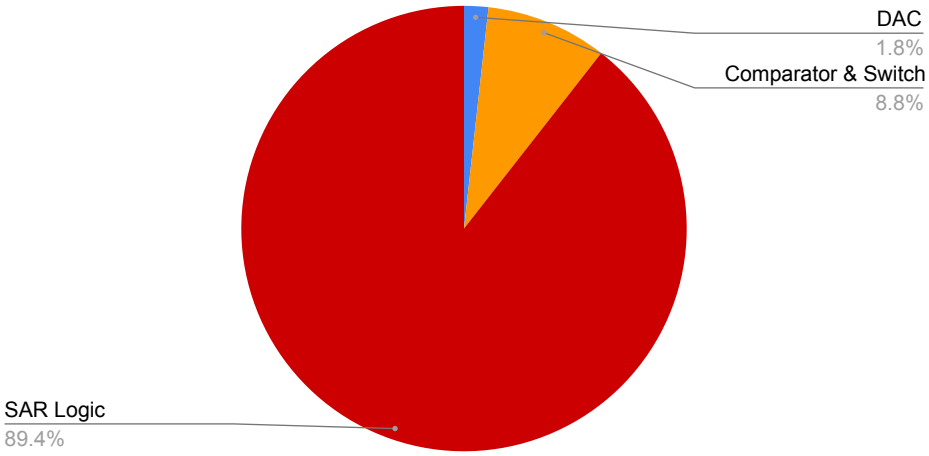


Figure 5.19: Power Distribution of ADC.

Table 5.3: **Comparison of the proposed ADC with state of the art work in Oxide TFT technology.**

ADC Design	$\Delta\sum$ **[94] (2015)**	$\Delta\sum$ **[96] (2017)**	**SAR [36] (2018)**	$\Delta\sum$ **[95] (2021)**	**This work (NS SAR)**
Minimum channel Length (μm)	20	15	15	10	**4**
Supply Voltage (V)	10	20	15	10	**2**
Fs (kHz)	128	1	0.013	2	**3**
ENOB (bits)	9	5.2	5	11.2	**7**
BW (Hz)	500	300	-	10	**350**
OSR	128	-	-	100	**4**
FoM (μJ/c.s.)	6.7	0.39	581.73*	0.15	**0.056****
Active-area (mm^2)	-	-	-	-	**6.6**

*Calculated using given data. **Post-layout simulations.

In addition, the proposed ADC has shown a FoM of 0.056μJ/c.s., which is the least reported FoM compared to state-of-the-artwork in the amorphous-oxide TFT technology. Thus, the proposed hybrid architecture of the SAR ADC can be employed in various applications like smart sensing, biomedical etc. to improve the overall energy efficiency of the system.

Chapter 6

Conclusions & Future Work

This chapter concludes the circuits developed in this **thesis**. In addition, it also focuses on the possible future directions to improve the effectiveness of the proposed designs.

6.1 Conclusions

This research work presented an energy efficient **CS-MCS hybrid DAC SAR ADC**, which employs two different switching principles (CS and MCS) in a single capacitive DAC. The ADC is demonstrated using two different technologies namely deep-submicron CMOS and large-area oxide TFT. The sampling switches in both the technologies have been proposed to obtain the desired performance of the ADC. While the **sampling switch** with CMOS technology compensates the R_{ON} variations with V_{TH} of the transistors, the sampling switch with oxide TFT technology is the first implementation in this technology to the best of author's knowledge. Moreover, a novel **comparator**, a compact SAR controller using proposed **D-FF** and **clock boosters** have been reported to implement the proposed SAR ADC with oxide TFT technology. Due to the lack of stable p-type transistors in oxide TFT technology, the complete ADC is designed using all enhancement n-type transistors. As a part of this research work, various novel ring oscillators with a-InGaZnO TFTs have been proposed, which can be used to generate the over-sample clock signals for the ADCs.

The obtained results of the proposed ADC show FoM to be around 5fJ/c.s and 56nJ/c.s. in CMOS and oxide TFT technologies respectively, which is least (to the best of author's knowledge) compared to the similar state of the art

work reported in a particular technology. Thus, the proposed CS-MCS hybrid DAC SAR ADC design offers high energy efficiency and therefore, finds wide applications in the field of wireless communication, biomedical, smart packaging and sensing systems.

6.2 Future Work

- A possible future investigation of this work can be in the area of producing the reference voltage for the LSB DAC from the reference voltage of the MSB DAC using passive switching schemes that are widely employed in the literature. This will make the complete hybrid DAC to operate passively, thus contributing in energy saving by turning off the reference buffers completely during the conversion process.

- Higher order noise-shaping can be employed to the hybrid architecture for improving its resolution and compensate for the degradation due to mismatches, noise etc.

- To achieve higher conversion-rates, the proposed hybrid SAR ADC architecture can be employed in SAR-assisted pipeline ADCs.

- Characterization of the fabricated circuits.

Appendix A

Technology Table

Table A.1: Technology Comparison Table

Parameters	**CMOS 65 nm** [113]	**In-House IGZO TFT [114]**	**PragmatIC Oxide TFTs [115]**
V_{TH} (V)	0.41	1.35	0.430
Subthreshold slope	-	-	100 mV/dec
I_{ON}	610 μA/μm	-	1.77 μA
I_{OFF}	0.36 nA/μm	-	-
L (min) (μm)	0.060	20	0.8
V_{DD} (V)	1.2 (LP)	8	2

Appendix B

Proposed Ring Oscillators with a-InGaZnO TFTs

B.1 High-Speed Programmable Ring Oscillator

B.1.1 High Speed RO

[1]Negative skewed delay scheme is a simplest way to obtain high frequency of oscillations in RO by prematurely turning on/off one of the transistor in an inverter to speed up the transitions between ground and supply rails. Due to the absence of stable p-type transistors in oxide-TFTs, it is challenging to adapt the negative skewed delay scheme directly into the conventional RO with diode connected load based inverter. This is because providing negative delay to the input of driver transistors, to switch them on/off prematurely, will not reduce delay of an inverter stage as gate of load transistor is connected to power supply voltage. Therefore, transistors of diode connected load inverters in conventional RO, cannot be skewed using negative skewed delay scheme to obtain high frequency of oscillations. In order to take advantage of negative skewed delay scheme, inverter which can mimic a CMOS counterpart is required. Pseudo-CMOS inverter using oxide TFTs can be an option, however, in order to obtain complete rail-to-rail operation two different supply voltages are needed.

Pseudo-CMOS inverter with Bootstrapped load mimics a CMOS inverter and provides rail-to-rail operation without using additional power supply voltage. Figure B.1(a) shows the block diagram of 9 stage RO with Pseudo-CMOS

[1]B. Tiwari et al., "A High Speed Programmable Ring Oscillator Using InGaZnO Thin-Film Transistors," 2018 International Flexible Electronics Technology Conference (IFETC), 2018, pp. 1-6, doi: 10.1109/IFETC.2018.8584006.

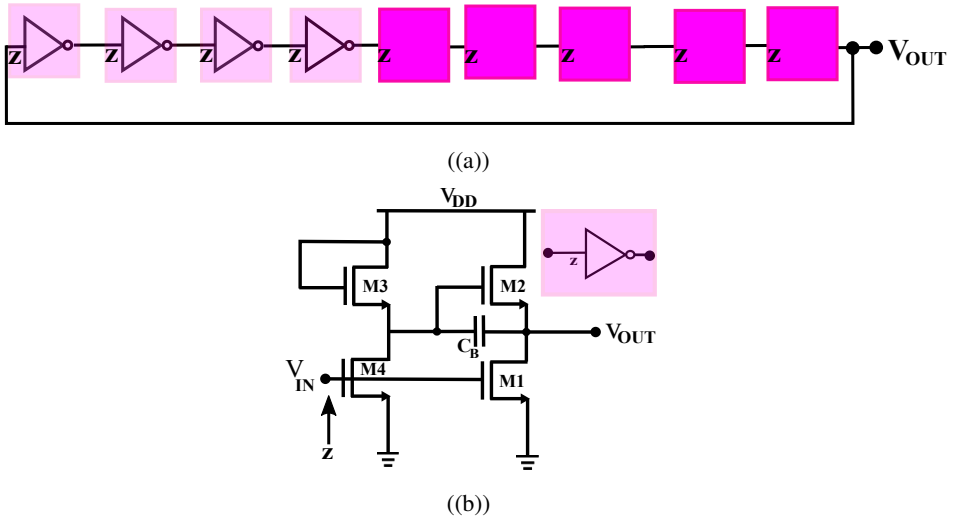


Figure B.1: Block Diagram of (a) 9 stage RO (b) Pseudo-CMOS inverter with Bootstrapped load.

bootstrapped load inverter, whose schematic is presented in Figure B.1(b). In this inverter, bootstrapped capacitor, C_B, is responsible for boosting output voltage to supply voltage, V_{DD}, when logic 0 is applied to the input of inverter. On the other hand, when logic 1 is applied at the input, $M2$ can be turned off completely through $M4$ (typically $\mathrm{W}_{M4} > \mathrm{W}_{M3}$ and the V_{DSM4} is close to 0V) which ensures rail-to-rail operation.

Figure B.2(a) shows the block diagram of proposed high speed RO using negative skewed delay scheme. In this architecture, pseudo-CMOS inverter with bootstrapped load is modified slightly. As shown in Figure B.2(b), gate of transistors M1 and M4 are separated as x and y, respectively, which are connected to the output of $(i-6)^{th}$ stage and i^{th} stage (for this particular case), respectively. This ensures premature triggering of M1 as x arrives earlier than y (Figure B.2(b)), which in turn reduces the propagation delay of each inverter leading to high frequency of oscillations. In addition to high speed of operation, almost rail-to-rail swing can be ensured.

B.1.2 Programmable High Frequency RO

The high speed RO discussed in the previous subsection is made programmable in order to tune oscillator frequency over different frequency range. Frequency of oscillation, f_{clk}, of n-stage RO, is given by:

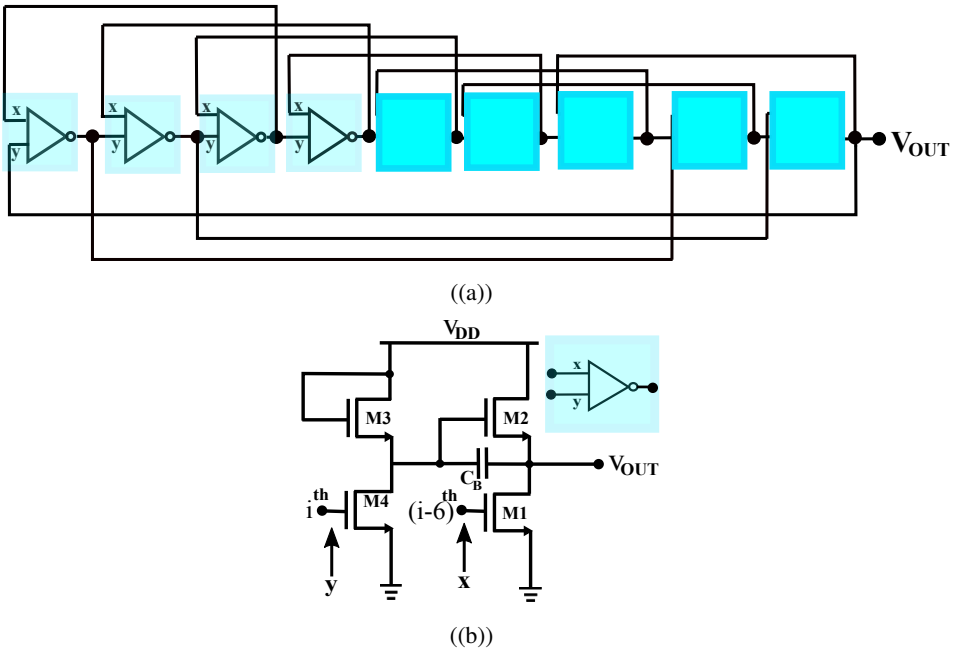


Figure B.2: (a) Proposed high speed 9 stage RO (b) Modified architecture of pseudo-CMOS inverter with boot-strapped load for proposed RO.

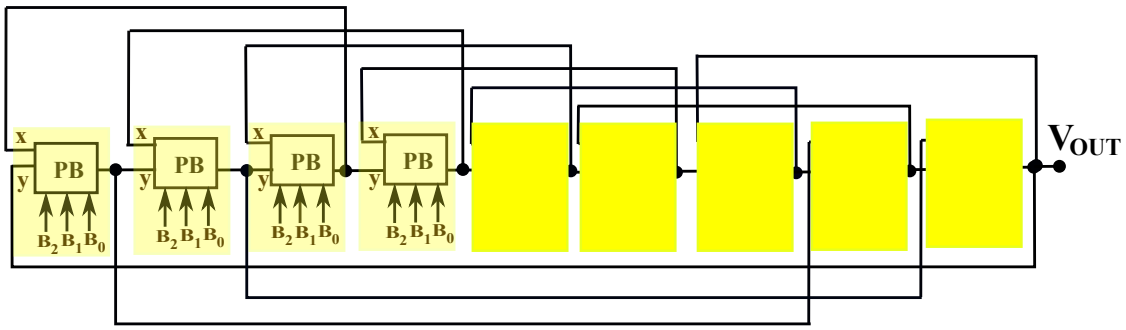


Figure B.3: Proposed High Speed programmable RO.

$$f_{clk} = \frac{1}{2.n.T_{delay}} \tag{B.1}$$

Here, T_{dealy} is propagation delay of an inverter in RO. The propagation delay introduced by each stage is proportional to the load capacitance. Figure B.3 shows the block diagram of proposed high speed programmable RO. Here, the inverters are replaced by programmable blocks (PB) which are controlled by bits B_2 (MSB), B_1 and B_0 (LSB).

Three binary weighted load capacitors controlled by three bits, B_2, B_1 and B_0, are connected at the output of inverter (of Figure B.2(b)), as shown in

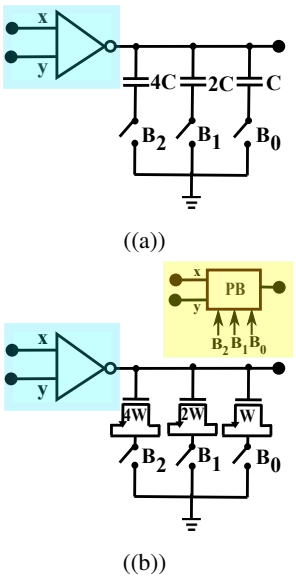


Figure B.4: Programmable block with (a) MIM capacitors (b) MOSCAPs.

Figure B.4(a), to program the oscillator frequency. The load capacitance of an inverter is given by:

$$C_{load} = C(2^2B_2 + 2^1B_1 + 2^0B_0) = 4CB_2 + 2CB_1 + CB_0 \qquad \text{(B.2)}$$

From (B.2), it can be observed that whenever bits are set to logic high level, its corresponding capacitor is added to increase the load capacitance of an inverter. This increases the propagation delay and hence, reduces frequency of oscillation according to (B.1). C is the unit capacitor in (B.2),whose value should be selected carefully, especially when this approach is adopted for negative skewed delay scheme. High value of C will cause excessive delay and make skewed operation difficult. Therefore, value of C is selected close to parasitic capacitors of the inverters in order to avoid any non-linearity in the operation of negative skewed delay RO. As a result, binary weighted capacitors can be realized using MOS capacitors (MOSCAPs), formed by n-type IGZO TFTs, whose widths are in the ratio 4:2:1 as shown in Figure B.4(b) with same channel length. The schematic of Figure B.4(b), hence, act as PB for proposed high speed programmable RO shown in Figure B.3

B.1.3 Results and Discussions

Circuit simulations have been carried out in Cadence Virtuoso using in-house IGZO TFT model at a supply voltage and device channel length of 10V and

10μm, respectively. First, in order to validate 9-stage high speed RO, conventional ROs with diode connected load inverter and pseudo CMOS bootstrapped load inverter have been designed and simulated on the same platform as that of 9-stage high-speed RO. The aspect ratios of the transistors used in different design for simulations are shown in Table 1. In addition, the bootstrapped capacitor, C_B, for pseudo bootstrapped load inverter, is kept as 5pF. From the simulation

Table B.1: Aspect ratios of Transistors used for Simulation of different ROs

ROs		**Width (μm)**	**Length (μm)**
2***With Diode-connected Load Inverter**	Driver	320	10
	Load	40	10
2***With Pseudo-CMOS bootstrapped Load**	M2, M1	160	10
	M3, M4	40	10
2***Proposed**	M2, M1	160	10
	M3, M4	40	10

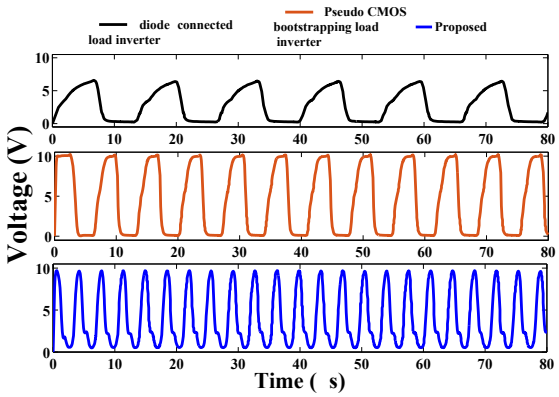


Figure B.5: Simulation Results of conventional and high-speed ROs.

results, shown in Figure B.5, it can be observed that the high-speed RO, designed using negative delay skewed scheme, offers high frequency of oscillations compared to other conventional design. Table II summarizes performance metrics of high-speed RO and compares it with conventional ROs in terms of power, output swing and frequency of oscillations. It can be noticed that the proposed RO provides 95.3% improvement in frequency of oscillations with 33.4% more power consumption compared to conventional RO with pseudo-CMOS bootstrapped load. As a result, power delay product is improved by proposed high speed RO (see Table II).

The high-speed RO is made programmable using external bits, B_2, B_1 and

B_0 and MOSCAPs with binary weighted widths as explained in the previous section. The widths of MOSCAP transistors are selected as 40μm, 20μm and 10μm corresponding to bits B_2, B_1 and B_0 for a channel length of 10μm. Three programmable bits give 8 different frequencies of oscillation ranging from 241.2KHz to 283KHz as shown in Figure B.6 with a step size of almost 6KHz. From the figure, almost linear decrements in frequency of oscillation can be observed when the load capacitance at the output of the inverter is increased with increase in decimal equivalent values provided by programmable bits. For fine resolution (step size), number of bits can be increased. Figure B.7 shows the simulation results of programmable high-speed RO under no load ($B_2B_1B_0$ = 000) and full load ($B_2B_1B_0$ = 111) conditions.

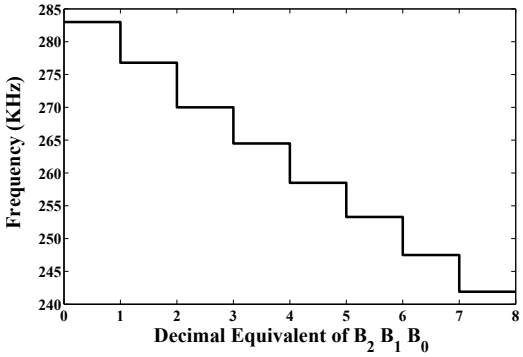


Figure B.6: Staircase showing linearly spaced frequency of oscillations.

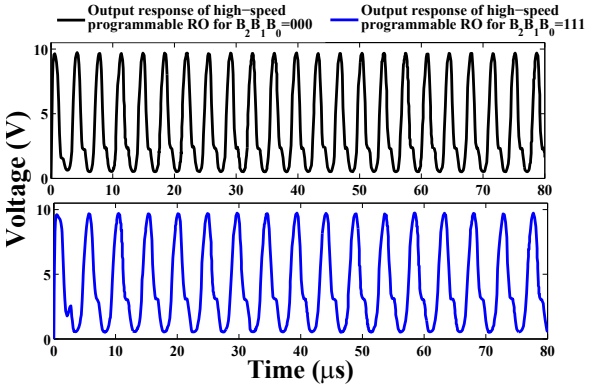


Figure B.7: Simulation result of proposed RO.

B.1.4 Conclusion

This section presented a high speed programmable RO with a-IGZO TFTs that can provide 95.3% improvement in frequency of oscillations compared to

Table B.2: Performance Metrics of Conventional and High-Speed ROs.

9-stage ROs		Power Consumption (mW)	Frequency of Oscillations (KHz)	Output Swing (V)	PDP (nJ)
2*Conv.	with Diode-Connected Load Inverter	0.930	76.52	6.05	0.6
	with Pseudo CMOS bootstrapped load inverter	2.069	144.90	10	0.8
High-speed		2.760	283.00	9.2	0.5

conventional RO at cost of 33.5% increment in the power consumption. In addition, for the first time programmability is introduced in the RO to achieve eight linearly spaced oscillation frequencies ranging from 241.2KHz to 283KHz with a step size of around 6KHz with 3 control bits. The proposed RO is able to provide a voltage swing of 92% of V_{dd}. Compared to state of art, this novel RO is able to deliver good performance parameters for a given technology. Hence it would find potential application as on-chip clock generator in smart packaging and wearable devices.

B.2 Low-Voltage High-Speed Ring Oscillator with a-InGaZnO TFTs

B.2.1 High-Speed Ring Oscillator Design

[2]The schematic of i^{th}-stage inverter employed in a conventional bootstrapped pseudo-CMOS inverter based RO is shown in Figure B.8(a). Here, i varies from 1 to n for a n-stage RO. However, for i=1, the input comes from the output of n^{th}-stage. In bootstrapped pseudo-CMOS inverter, operation of $M2$ is controlled by a diode-load inverter, whose propagation delay is defined as t_d (see Figure B.8(a)). Therefore, signal at node b is delayed by t_d compared to signal at node a, which increases the overall delay of the inverter stage. Since the frequency of oscillation of the RO is inversely proportional to the propagation delay of a single stage inverter in the RO, t_d imposes limitations on its operating frequency.

[2]B. Tiwari et al., "Low-Voltage High-Speed Ring Oscillator With a-InGaZnO TFTs," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 584-588, 2020, doi: 10.1109/JEDS.2020.2997101.

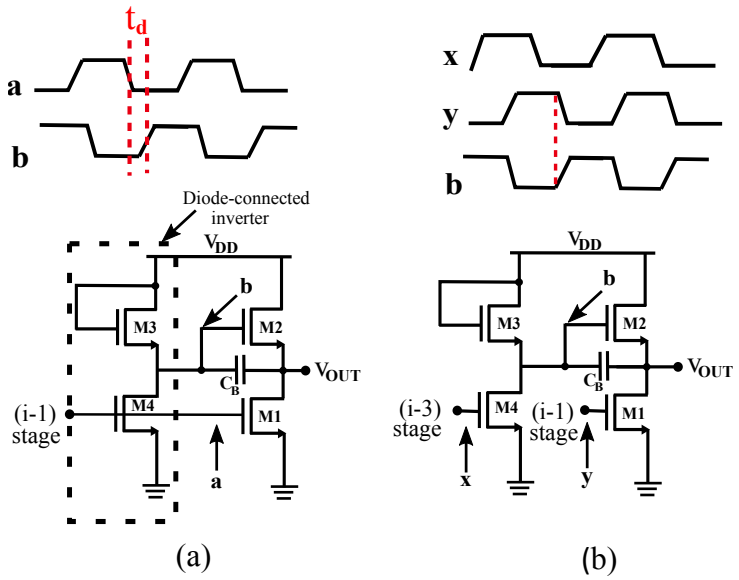
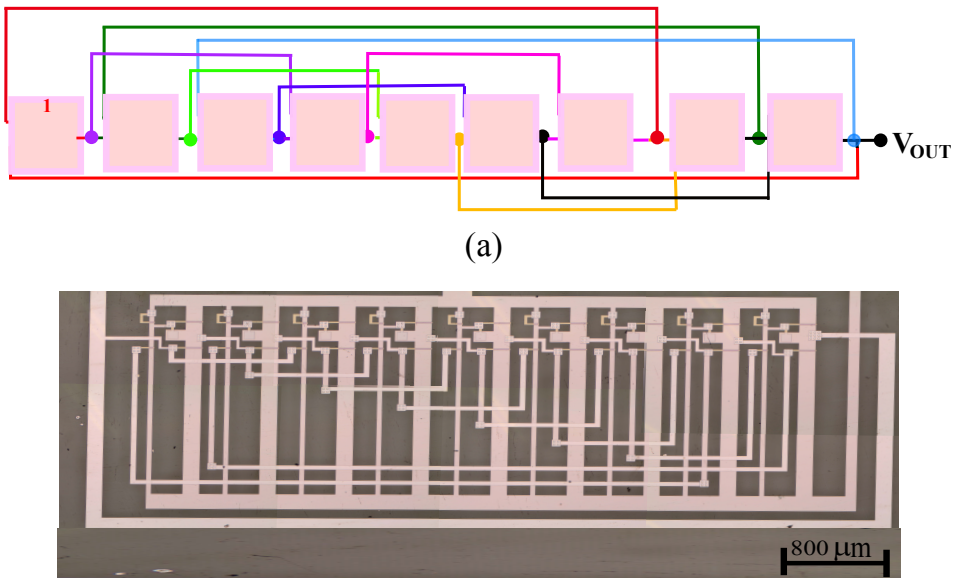


Figure B.8: Schematic presenting i^{th}-stage inverter of (a) conventional bootstrapped pseudo-CMOS inverter based RO (b) High-speed RO.

In order to compensate t_d, the high-speed RO employs bootstrapped pseudo-CMOS inverter stage, which is modified as shown in Figure B.8(b). Here, the gate of $M1$ and $M4$ are separated from each other. The gate of $M1$ (node y) is connected to the output of $(i-1)$-stage inverter, like in the conventional RO. It should be noted that the input to the gate of $M1$ and $M4$ should have nearly the same phase for proper operation. In addition, arrival time of the signal and its inverted form at node y and b, respectively, should be the same. Therefore, the gate of $M4$ is connected to the output of $(i-3)$-stage (if i >3, else $(n-(i-3))$-stage) inverter of a n-stage RO. As a result, signal at the gate of $M4$ arrives earlier than that of $M1$, which ensures almost simultaneous arrival of signals at nodes b and y. Therefore, t_d in Figure B.8(a) will be compensated, hence, improving the frequency of oscillations. However, unlike in Figure B.8(a), the diode-load inverter in Figure B.8(b) turns ON before $M1$ and $M2$ are actually operated and hence, consumes slightly more power. Therefore, the proposed RO ensures improved frequency of operation with a slight increment in the power consumption compared to the conventional RO. The schematic and micrograph of a 9-stage proposed RO is shown in Figure B.9. Two conventional (conv.) 9-stage ROs, with bootstrapped pseudo-CMOS inverter (RO1) and diode-load inverter (RO2), were also fabricated along-with proposed 9-stage RO under same conditions, in order to have a fair comparison from measurements. Micro-graphs of conventional ROs are presented in Figure B.10(a)-(b).



(a)

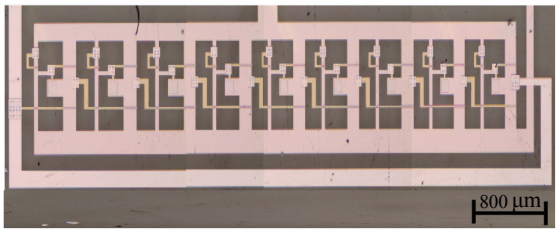
(b)

Figure B.9: Proposed 9-stage RO based on a modified bootstrapped pseudo-CMOS inverter stage (a) Schematic (b) Micro-graph.

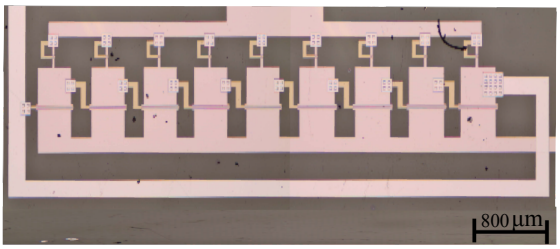
B.2.2 Results and Discussions

The voltage transfer characteristics (VTC) of the inverters employed in the ROs were measured using the probe station. The characteristic had been obtained by linearly sweeping the input voltage of the inverter (V_{IN}) from -5V to 6V in a step size of 0.1V. The measured characteristic plot is shown in Figure B.11(a). The plot shows almost rail-to-rail operation for bootstrapped pseudo-CMOS inverter compared to diode-load inverter.

The measurements of ROs were performed at different values of V_{DD} 3, 6 and 9V under normal ambient using Keysight DSOX2002A, as shown in in Figure B.11(b). These ROs employ TFTs with a channel length of 10μm. From the measurements, frequency of oscillations of RO1, RO2 and proposed RO were observed to be 120kHz, 68kHz and 173.2kHz, respectively, at 6V supply voltage. It can be noticed that the proposed RO has shown nearly 44% (155%) increase in frequency of oscillation by consuming approximately 15% (113%) more power compared to RO1 (RO2). The performance of all the three ROs are compared from experimental characterization, at different supply voltages (V_{DD}) and the plots are shown in Figure B.12(a)-(d). It can be observed from the plot that the proposed RO provides highest frequency, lowest power-delay product (PDP) and per stage propagation delay compared to conventional ROs.

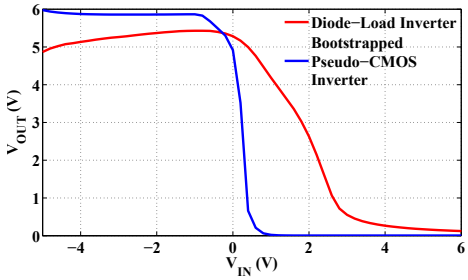


(a)

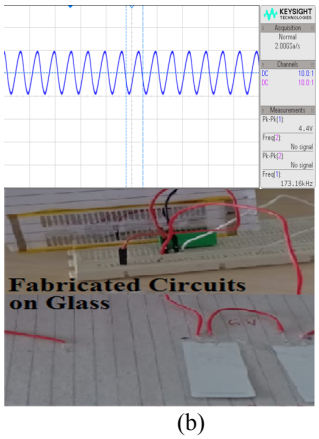


(b)

Figure B.10: Micro-graph of conventional 9-stage ROs (a) with bootstrapped pseudo-CMOS inverters (RO1) and (b) with diode-load load inverters (RO2).



(a)



(b)

Figure B.11: (a) Measured VTC of the inverters employed in ROs at V_{DD}=6V, and (b) Measurement setup showing measured response of the proposed RO at 6V.

However, the voltage swing of the proposed RO is inferior compared RO1. For a 6V supply, the voltage swing of RO was observed to be 73% of supply voltage compared to 91% in RO1. It should be noted that the testing of the ROs have been performed without using any on-chip output buffers. As a result, the large

load impedance offered by the DSO (digital storage oscilloscope) cables during measurements, can effect the performance of the ROs significantly. In order to study the effect of the load impedance on the swing of the proposed and other ROs, simulations were performed at a supply voltage of 6V and the swing is plotted against different loading conditions (see Figure B.12(e)). From the plot it can be observed that under no load condition, RO1 and the proposed RO deliver 100% output voltage swing. However, as the load impedance increases, the voltage swing of the proposed RO degrades more significantly compared to RO1 because the output node of the proposed RO acts as an input to two intermediate stages within the RO (compared to one in RO1). Therefore, the output swing of such stages will also degrade and this degradation in voltage swing propagates through all the stages of the RO, thus, degrading the final output voltage swing. However, by taking into account on-chip output buffers similar to the ones that are used in the literature, almost a complete output voltage swing and higher frequency of oscillations can be achieved from the proposed RO for a given technology.

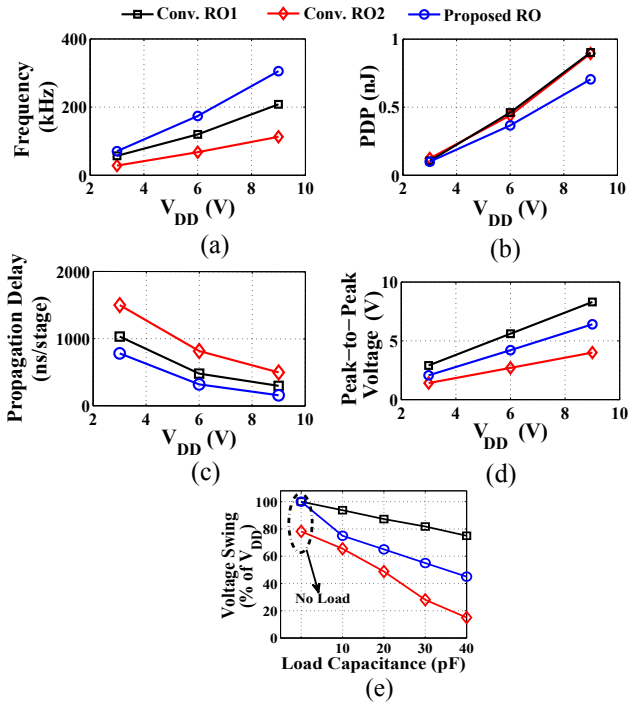


Figure B.12: Performance comparison of conventional and proposed ROs as a function of V_{DD} (a) Frequency (b) PDP (c) Propagation Delay (d) Peak-to-peak Voltage, and (e) Simulation results showing the effect of load capacitance on the voltage swing of the ROs.

B.2.3 Conclusions

This work presents a high-speed RO with a-IGZO TFTs at low-supply voltage. The proposed circuit has shown an improvement in the output frequency of 44% and 155%, and reduction of 24.5% and 14% in the power-delay product compared to RO1 and RO2, respectively, from measurements at a V_{DD} of 6V. Therefore, the proposed RO can be employed in many low-cost applications including smart packaging, biomedical wearable devices, NFC and RFIDs, without requiring miniaturized and/or complex transistor structures.

B.3 Low-Power Ethanol Sensor Read-Out Circuit Using a-InGaZnO TFTs

B.3.1 Low-Power Ring Oscillator

[3]The conventional (conv.) low power RO ensures complete voltage swing, and it has low power consumption. The schematic of the i^{th}-stage inverter of an n-stage conv. low power RO is shown in Figure B.13(a) where, $0 < i \leq n$. Here, $V_{OUT,i}$ represents the output of the i^{th}-stage inverter. It should be noted that the gate of transistor $M4$ (Q_i) has been bootstrapped using a capacitor C_B, to ensure complete voltage swing at the output. The gate of $M1$ (crl_i) is connected to the gate of $M4$ of the k^{th}-stage inverter (Q_k) within the RO. The value of k is expressed in terms of i, as shown in Figure B.13. As a result, $M1$ is turned off, when $M2$ and $M3$ are turned on. Therefore, only overlapping current flows through $M1$, which reduces its power consumption. Since the same signal controls $M2$ and $M3$, time taken by $M2$ to pull down Q_i to ground will increase the overall propagation delay (t_d) of a single inverter stage in a RO and hence degrades the operating frequency of the RO (f_{RO}) according to (1). Here, t_d of a single stage inverter is defined as the average of the time difference between the input and the output of an inverter, when the input falls (rises) and the output rises (falls) to 50% of the supply voltage.

$$f_{RO} = \frac{1}{2nt_d} \tag{B.3}$$

[3]B. Tiwari, P. Bhatnagar, P. G. Bahubalindruni and P. Barquinha, "Low-Power Ethanol Sensor Read-Out Circuit using a-InGaZnO TFTs," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9181093.

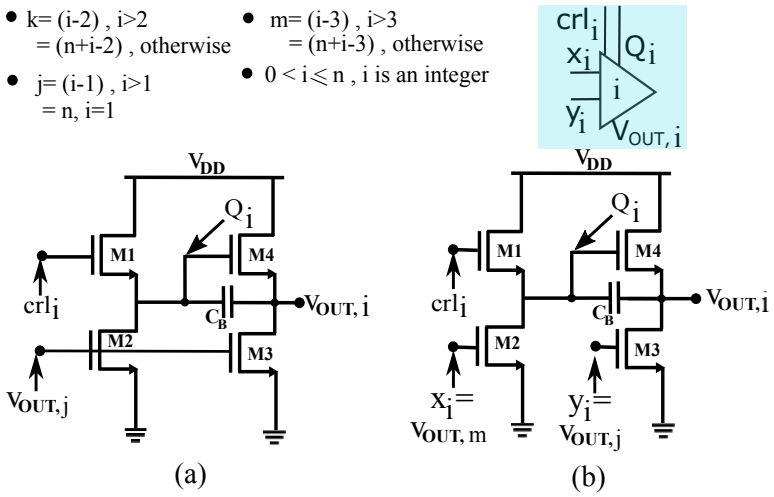


Figure B.13: Schematic of i^{th}-stage inverter of (a) Conv. low power n-stage RO (b) Proposed n-stage RO.

In order to improve the operating frequency of the conv. low power RO, i^{th}-stage inverter of the RO has been modified as shown in Figure B.13(b). Like the conventional design, the gate of $M1$ is controlled by crl_i signal, which is defined as the Q signal of k^{th}-stage inverter. However, unlike conventional design, the gate of transistors $M2$ and $M3$ are separated from each other to minimize the delay introduced by $M2$. The gate of $M2$ is controlled by the output of m^{th}-stage inverter ($V_{OUT,m}$) and like the conventional design, the gate of $M3$ is controlled by the output of j^{th}-stage inverter ($V_{OUT,j}$), in a n-stage RO. The values of j and m are defined in terms of i as shown in Figure B.13. It should be noted that the signal at the gate of $M2$ arrives slightly earlier than the signal at the gate of $M3$ and it is nearly in-phase with it. This minimizes the delay due to $M2$ and ensures almost simultaneous arrival of complementary signals at the gates of $M4$ and $M3$. Therefore, higher frequency of oscillations are obtained. In addition, the overlaps between the signals at the gates of $M1$ and $M2$, and the gates of $M3$ and $M4$, are minimized, which reduces the overlapping current and therefore, the power consumption of the proposed design is lower compared to the conventional design. Complete schematic of the proposed RO is presented in Figure B.14(a), which employs the inverter stage shown in Figure B.13(b). Here, the final output of the RO is defined as $V_{OUT,osc}$.

The schematic of proposed RO as an ethanol sensor read-out circuit is shown in Figure B.14(b). Here, C_s represents the ethanol sensor output capacitance, which changes with respect to the sensed ethanol level. The sensing capacitor changes t_d and, hence changes the frequency of oscillations of the RO according to (1). Therefore, the sensed signal is transformed into frequency variations by the RO.

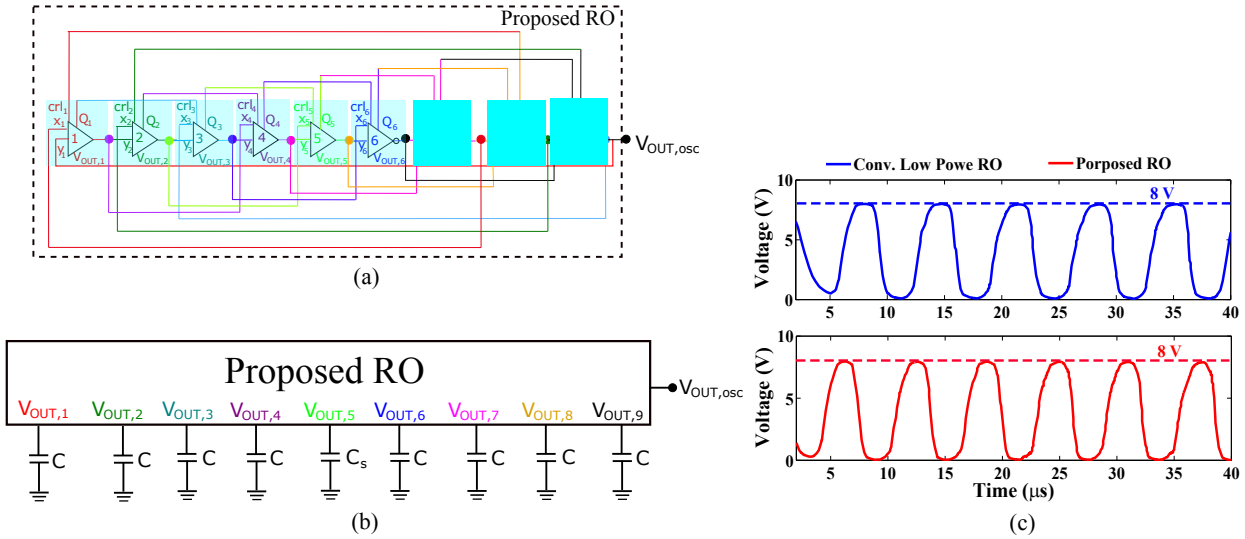


Figure B.14: (a) Schematic of Proposed RO (b) Schematic of Proposed RO as an ethanol read-out circuit, and (c) Simulation results of conv. and proposed 9-stage ROs.

B.3.2 Results and Discussions

The proposed and conv. low power 9-stage ROs have been designed and simulated using in-house a-IGZO TFT models. All the transistors employed in the ROs have a channel length of 10μm. Width of $M1$, $M3$ and $M4$ are kept at 160μm, while width of $M2$ is 10μm. Simulations were performed at a supply voltage (V_{DD}) of 8V.

The simulation results of the conv. and proposed 9-stage ROs are shown in Figure B.14(c). It has been observed from the figure that the frequency of oscillations of conv. and proposed RO came out to be 150.9KHz and 168.7KHz, respectively. In addition, a complete voltage swing has been observed in both ROs. The drain currents (I_D) of $M1$ and $M4$ (for a single inverter stage) are shown in Figure B.15 and Figure B.16, respectively. From the figures, it can be observed that in proposed RO, overlapping currents flowing through the inverter stage due to overlaps between the gate voltages (V_G) of $M1$ and $M2$, and $M3$ and $M4$, are minimized compared to the conventional design. Therefore, low power consumption has been noticed in the proposed RO. The power consumption of proposed and conv. low power RO is calculated as 0.912mW and 1.119mW, respectively, at a supply voltage of 8V.

Next, the performance metrics of the conv. low power and proposed RO have been compared at different V_{DD} and the obtained results are presented in Figure B.17(a)-(c). It has been observed from the figures that the proposed RO has

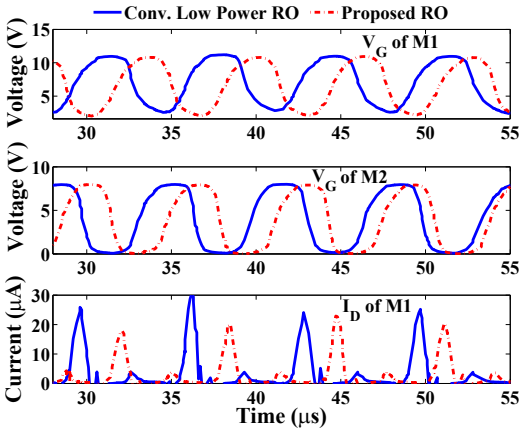


Figure B.15: Simulation results showing the bootstrapped V_G of $M1$ and V_G of $M2$, and I_D of M1 due to overlaps between the gate voltages of $M1$ and $M2$.

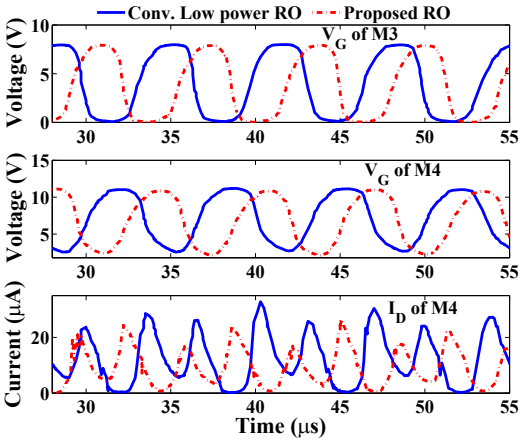


Figure B.16: Simulation results showing V_G of $M3$ and bootstrapped V_G of $M4$, and I_D of M4 due to overlaps between the gate voltages of $M3$ and $M4$.

shown lower power consumption and higher frequency of operation compared to conv. low power RO, even at supply voltages less than 8V. The Power-Delay product (PDP) of a n-stage RO is calculated as: PDP = $\frac{Power\ consumption}{2*n*frequency}$. Therefore, PDP of proposed 9-stage RO is lower compared to conventional design. The proposed and conv. low power RO have been simulated as an ethanol read-out circuit, where C_s is varied between 30pF to 100pF. The frequency of oscillations decreases with increasing value of C_s as shown in Figure B.17(d). From the figure, the slope of the curves, which defines the sensitivity of the conv. low power and proposed RO, has been calculated as 130Hz/pF and 142.3Hz/pF, respectively. Therefore, the proposed RO shows better sensitivity towards the change in capacitance compared to the conventional design.

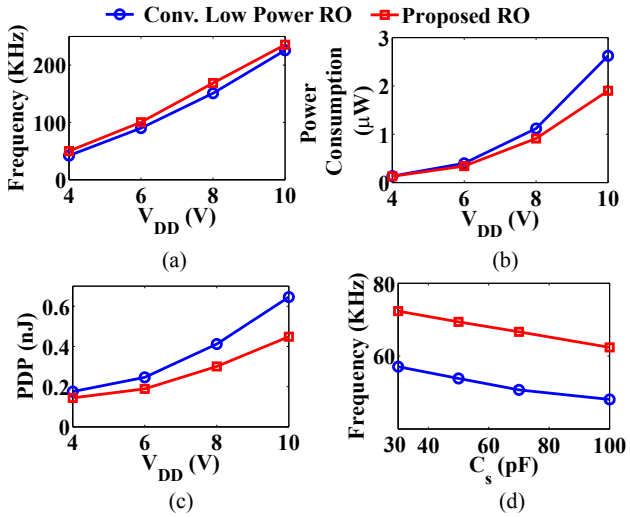


Figure B.17: Performance comparison of conventional and proposed ROs as a function of V_{DD} (a) Frequency (b) Power consumption (c) PDP, and (d) Simulation results showing the variations in frequency of oscillations with varying C_s.

B.3.3 Conclusions

This work presents a low-power ethanol sensor read-out circuit using proposed RO with a-IGZO TFTs. The proposed circuit has shown 11.8% improvement in the frequency of oscillations and 18.5% reduction in power consumption compared to conventional low power RO at a supply voltage of 8V. In addition, when used as an ethanol sensor read-out circuit, the proposed RO has shown 9% improvement in the sensitivity compared to conventional design without compromising on any other performance metrics.

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