Impact of Approximate Adder design choices on Sustainability

by

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14 May 2025

May 2025

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A Thesis Report

submitted by

Thatikonda Gopal Rao

in partial fulfilment of the requirements
for the award of the degree of

Master of Technology

to

Electronics and Communication Engineering
Indraprastha Institute of Information Technology Delhi
New Delhi - 110020

14 May 2025

Certificate

This is to certify that the thesis titled "**Impact of Approximate Adder design choices on Sustainability**" being submitted by **Thatikonda Gopal Rao**, to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of **Master of Technology**, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 21 May 2025

Acknowledgements

I express my deepest gratitude to my thesis advisor, Dr. Anuj Grover, for offering advice and encouragement with a perfect blend of insight and humor. I would also like to thank my friends Najeeb Mohammad Khan, Abhishek Jain, Samriddhi Jain, Abhishek Chaurasiya, and Piyush Kumar for supporting and helping me through the different challenging stages of the project. Most importantly, I am grateful to my parents and friends for their support and love.

Abstract

Recent advancements in the semiconductor industry have paved the way for a broader use of semiconductor chips in various areas such as computing, data processing, and communication. Adders, which are the smallest and most common building blocks in these applications, play a critical role. With the exponential growth in data, there is a significant increase in power demand, leading to a rising interest in approximate adders. These adders are particularly effective in saving power for error-resilient applications like image and video processing, as well as data computation.

As the utilization of semiconductor chips continues to expand, the traditional evaluation framework that focuses on Power, Performance, and Area (PPA) is no longer adequate for assessing the environmental impact of these designs. Consequently, there is a need for a new approach that evaluates designs based on Power, Performance, Area, and Sustainability (PPAS). This sustainability evaluation paradigm broadens the analysis to include the environmental effects of both fabrication and operation, ensuring long-term efficiency and a reduced carbon footprint.

In this study, a set of approximate adder architectures has been benchmarked using a novel sustainability-focused evaluation framework in 65-nm low standby power technology. This benchmarking approach allows designers to choose the most efficient and sustainable approximate adder architecture from the available options.

Keywords: Sustainability ; Error Resilient ; Approximate Adders; Carbon footprint

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Abbreviations

IIITD	Indraprastha Institute of Information Technology Delhi
PPAS	Power, Performance, Area, and Sustainability
IC	Integrated circuit
SoC	System on Chip
PDLC	Product Development Life Cycle
FoM	Figures of merit
GHG	Green House Gas
LCA	Life Cycle Analysis
CFP	Carbon Footprint

Notation

σ	Deviation
M	Mega (10^6)
k	Kilo (10^3)
m	Milli (10^{-3})
μ	Micro (10^{-6})
n	Nano (10^{-9})
p	Pico (10^{-12})
f	Femto (10^{-15})
s	Seconds
h	Hour
v	Volts
MHz	Mega Hertz
C	Coulomb
F	Farad
W	Watt

CHAPTER 1

INTRODUCTION

1.1 Motivation

Recent advancements in various fields, along with the widespread use of chips—from everyday applications to the development of advanced processors—have led to an increased demand for chip manufacturing. A survey conducted in 2022 revealed that TSMC alone consumes more power than the entire country of Sri Lanka[1]. This high energy consumption in semiconductor manufacturing facilities has surpassed the energy usage of entire nations, raising urgent concerns about the environmental impact of such significant energy demands.

In the context of these challenges, major companies such as STMicroelectronics, Apple, Google, TSMC, Meta, and Intel have taken an oath to achieve carbon neutrality, as presented in their sustainability reports[2, 3, 4, 5, 6, 7]. As a result, sustainability has emerged as a vital paradigm that must be integrated with Power Performance Area (PPA) to design environment-friendly chips in the future.

Approximate adders are gaining significance today due to the rising demand for data processing. They offer energy efficiency since there is no strict requirement for precision, and many applications are now more error-tolerant, thanks to advancements in artificial intelligence. Additionally, approximate adders require less physical space, contributing to the development of greener chips and improved overall efficiency.

1.2 Circuit

Approximate adders are similar to full adders, with the main difference being that either the sum output or the carry-out of an approximate adder may have inaccuracies compared to a full adder. In certain applications such as image processing, video processing, and audio processing, slight inaccuracies are acceptable since the final output of the application remains unaffected by these minor errors. To leverage these error-resilient applications and enhance performance, power, and area (PPA) efficiency, approximate adders are used. These adders are typically designed to be more area and power-efficient, which can be advantageous when multiple instances of approximate adders are required for a specific application.

Researchers have conducted several experiments to reduce power consumption, among which supply voltage reduction and dynamic voltage and frequency scaling have emerged as the most popular techniques. Following the innovation of approximate adder designs, designers began using approximate adders in place of full adders for error-resilient applications to further minimize power consumption.

In this work, two different architectures of approximate adders are used, one is a conventional architecture and the other is an advanced architecture, to benchmark the proposed paradigm of sustainability. The architectures used are.

- Approximate Mirror Adders(AMA)[8].
- Low Cost Approximate Full Adders(LCAFA)[9].

In each architecture, three circuits along with reference full adders are considered for the analysis of the proposed Sustainability paradigm.

1.2.1 Approximate Mirror Adders

Approximate Mirror Adders are developed from conventional mirror adders with minor adjustments in the logic circuitry of the Sum and Carry-out to enhance the area and power efficiency of the derived circuits.

1.2.1.1 Conventional Mirror Adder

The conventional mirror adder, as shown in Fig. 1.1, connects the pull-up and pull-down networks in a similar way, which reduces the number of transistors compared to a conventional full adder. While a conventional full adder uses 28 transistors, the conventional mirror adder achieves the same output accuracy with only 24 transistors.

1.2.1.2 AMA1

The schematic diagram of AMA1 is shown in Fig. 1.2. It is derived from the conventional mirror adder shown in Fig. 1.1 by reducing a number of transistors from 24 to 16 transistors and adding inaccuracies in both the Sum and Carry-out circuitry. The sum and carry-out minterms are as shown Sum = $\sum(1,7)$ and Carry-out = $\sum(2,3,5,6,7)$.

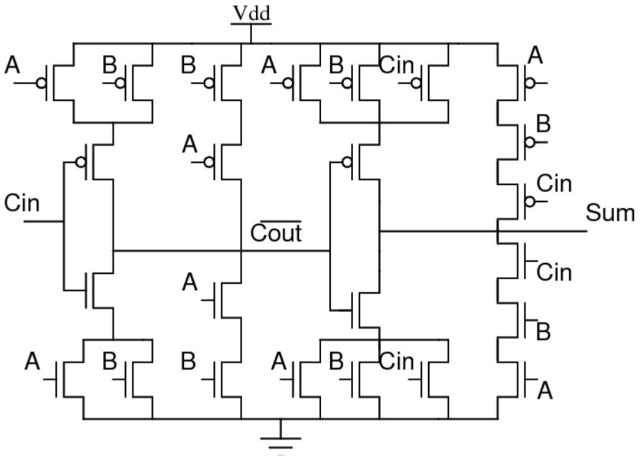

Figure 1.1: Conventional Mirror Adder

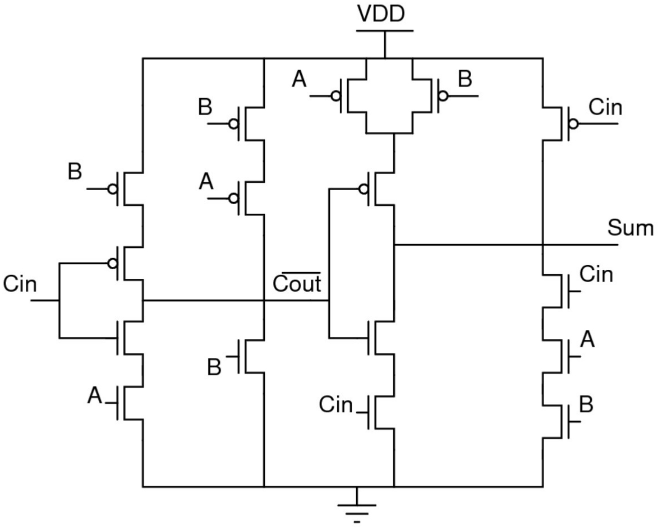

Figure 1.2: AMA1

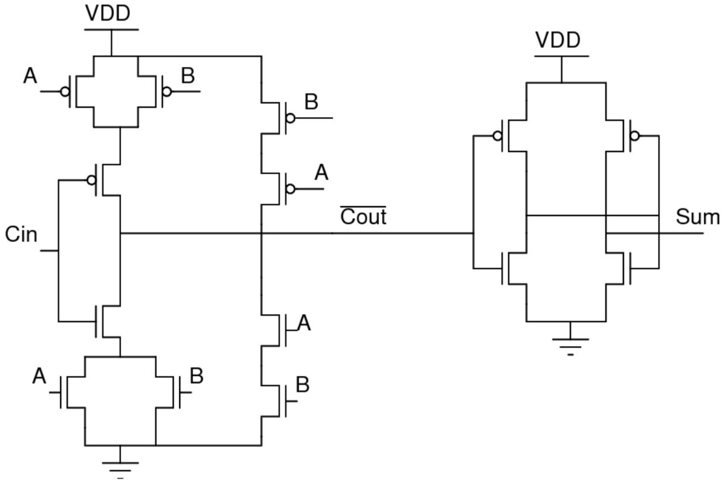

Figure 1.3: AMA2

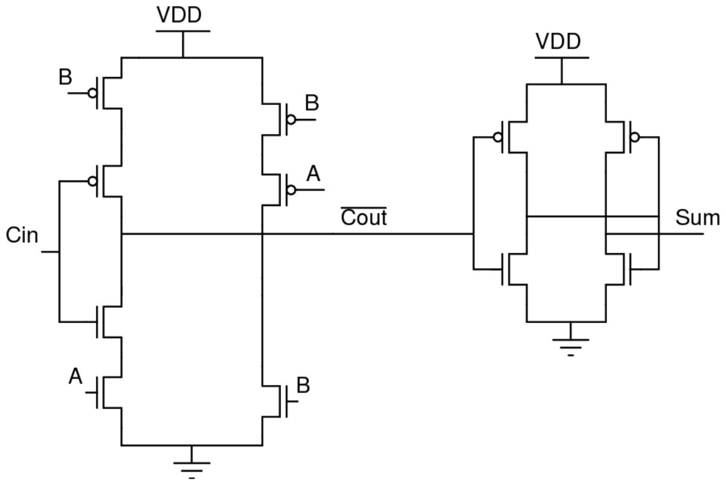

Figure 1.4: AMA3

Table 1.1: TRUTH TABLE OF APPROXIMATE MIRROR ADDER DESIGNS

INPUTS			**Accurate Output**		**Approximate Outputs**					
					AMA1		AMA2		AMA3	
A	B	Cin	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout
0	0	0	0	0	0	0	1	0	1	0
0	0	1	1	0	1	0	1	0	1	0
0	1	0	1	0	0	1	1	0	0	1
0	1	1	0	1	0	1	0	1	0	1
1	0	0	1	0	0	0	1	0	1	0
1	0	1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	1	0	1	0	1
1	1	1	1	1	1	1	0	1	0	1

1.2.1.3 AMA2

AMA2 is the further reduced version of conventional mirror adder using only 14 transistors with only inaccuracy in the Sum circuitry whereas Carry-out remains same as that of CMA. the minterms of AMA2 are Sum = $\sum(0,1,2,4)$ and Carry-out = $\sum(3,5,6,7)$. the schematic of AMA2 is shown in Fig. 1.3

1.2.1.4 AMA3

The schematic of AMA3 is shown in Fig. 1.4 out of all the Approximate Mirror Adders used in this work. AMA3 is the design with the smallest number of transistors and the most area-efficient design. AMA3 has inaccuracy in both the Sum and Carry-out circuitry. The minterms for the Sum and Carry-out logic circuits are Sum = $\sum(0,1,4)$ and Carry-out = $\sum(2,3,5,6,7)$.

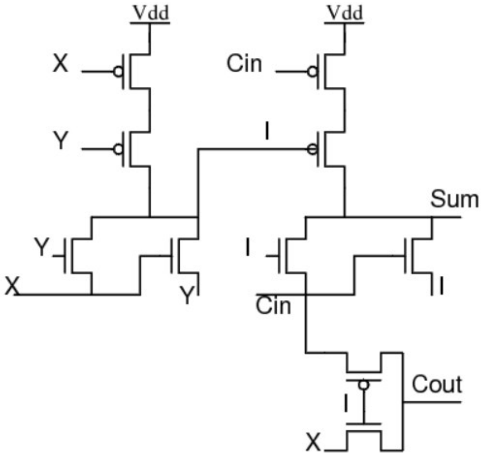

Figure 1.5: Conventional Xor-Xnor Adder

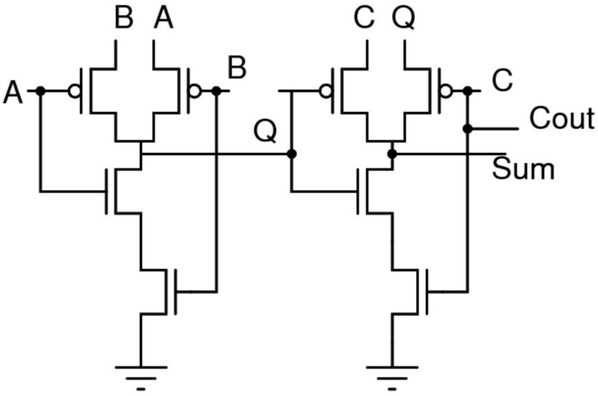

Figure 1.6: LCAFA1

1.2.2 Low Cost Approximate Full Adders

Approximate Adders are being researched to leverage the inaccuracy, suited to the error-resilience of applications in which they are being used. In last section, we have discussed about conventional Approximate adders in this section we will discuss some of Advanced Approximate Adders proposed in ISCAS 2023 [9].

To benchmark this architecture, we used a Conventional Xor-Xnor adder since it uses a relatively small number of transistors and will be best suited for comparison. The Conventional Xor-Xnor adder is shown in Fig. 1.5.

1.2.2.1 LCAFA1

This design has approximation or inaccuracy only in Carry-out circuitry , Sum logic is completely accurate it uses only 8 transistors and the densest design in this work. The LCAFA1 schematic is shown in Fig. 1.6 and the Cout logic is as shown in Table. 1.2, The minterms for the Sum and Carry-out logic circuits are Sum = $\sum(1, 2, 4, 5)$ and Carry-out = $\sum(1, 3, 5, 7)$.

Table 1.2: TRUTH TABLE OF ADVANCED APPROXIMATE ADDER DESIGNS

INPUTS			**Accurate Output**		**Approximate Outputs**					
					LCAFA1		LCAFA2		LCAFA3	
A	B	Cin	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout
0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	1	0	1	1	1
1	0	0	1	0	1	0	1	0	1	0
1	0	1	0	1	1	1	1	1	1	1
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	1	0	1	1	1

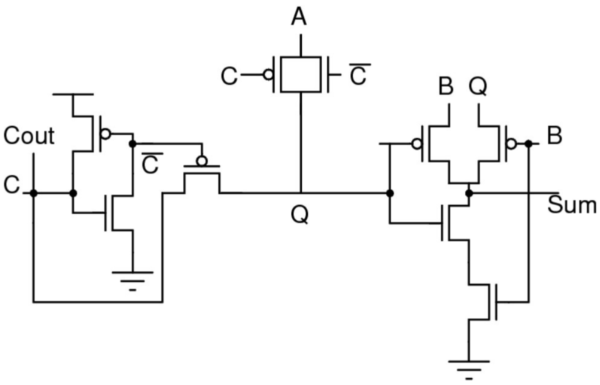

Figure 1.7: LCAFA2

1.2.2.2 LCAFA2

LCAFA2 uses 9 transistors and has inaccuracy in both the Sum and Carry-out circuitry, In LCAFA2, both Cin and $\overline{\text{Cin}}$ work as clock signals.The logic for both Sum and Carry-out is shown in Table. 1.2. The minterms for the Sum and Carry-out logic circuits are Sum = $\sum(1, 2, 4, 5)$ and Carry-out = $\sum(1, 3, 5, 7)$.

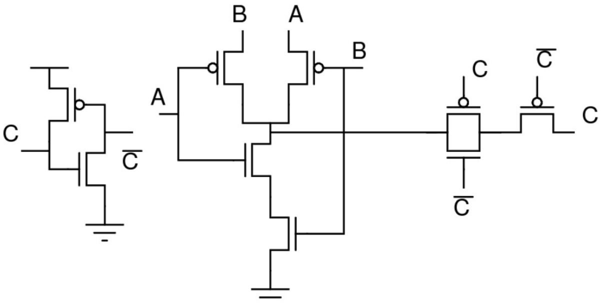

Figure 1.8: LCAFA3

1.2.2.3 LCAFA3

The schematic of LCAFA3 is depicted in Fig. 1.8. It utilizes 9 transistors, similar to LCAFA2, and incorporates both Cin and $\overline{\mathrm{Cin}}$ as clock signals. The minterms for the Sum and Carry-out logic circuits are as follows: Sum = $\sum(1, 2, 3, 4, 5, 7)$ and Carry-out = $\sum(1, 3, 5, 7)$.

CHAPTER 2

Literature Review and Related Work

Sustainability, as a broader concept, originated in 1987 with the Brundtland Report [10] and can be interpreted in various ways. For the purposes of this work, we define sustainability as the design of reliable products that minimize their long-term environmental impact. Today, the analysis of sustainability typically involves conventional life cycle assessment (LCA) and the greenhouse gas (GHG) emission protocol [11].

GHG was established in 1998. It is a standard protocol for quantifying carbon emissions at the organizational level. These emissions are classified into three scopes, depending on the stage of the Product Development Life Cycle (PDLC) in which they occur and who generates them. The scopes are broadly presented in a Table. 2.1[12].

Table 2.1: GHG Protocol Classification

Scope Level	**Emission types**
Scope 1	Direct Emissions from company resources: • Fuel combustion in facilities, refrigerant use • Transportation and chemical emissions
Scope 2	Indirect Emissions from purchased energy: • Running fabs, facilities, and data centers • Energy consumed during operation • Carbon emission released per unit energy consumed
Scope 3	Other Indirect Emissions: • Logistics and Business • Raw material production • Supply chain

One of the first studies to evaluate the sustainability of semiconductor manufacturing processes was published in 2000 [13]. This was around the time when regulations aimed at phasing out toxic materials, such as lead, from the semiconductor supply chain were being implemented. The EE-Toolbox, as described in [13], assesses the sustainability of a System on Chip (SoC) based on material-related parameters. It evaluates products using a variety of metrics, including the Toxic Potential Indicator, Recycling Potential Indicator, energy consumption (which combines energy from raw materials and product usage), and Process Toxicity Screening. While these metrics focus entirely on material-related data and are relevant to sustainability, they do not directly address the GHG protocol.

In 2012, a multiple-criteria decision-making approach was introduced that emphasized the concept of "Eco-reliability" to improve the design optimization process[14]. The authors discuss factors such as product lifetime and life-cycle optimization, considering aspects of reliability, cost, and environmental impact. They utilize multi-criteria life cycle assessment (LCA) evaluations to estimate environmental effects. This work was one of the first to highlight the complexities involved in estimating the carbon footprint (CFP) of electronic products. The paper provides a qualitative perspective on LCA-based CFP assessment; however, it does not include quantitative measures or figures of merit for estimating emissions.

A 2017 study [15] investigates the growing environmental impact of integrated circuit (IC) fabrication, which is increasingly comparable to the energy consumed during operation, especially in low-power computing applications. To tackle this issue, the authors present a scalable parameterized model for assessing the environmental costs associated with fabrication across various technology nodes, ranging from 130nm to 32nm. Their framework emphasizes the effects of modifying the metal stack in a VLSI chip design. Notably, reducing the highest metal routing layer can lead to a nearly 13.8% decrease in manufacturing energy consumption at certain nodes. These findings underscore the necessity of balancing fabrication and operational energy to develop sustainable ICs. It's important to note that this work focuses solely on chip or product-level analysis.

In 2022, a comprehensive research study investigating the carbon footprint (CFP) of computing systems was published [11]. The study presents that, although there have been improvements in energy efficiency due to advancements in algorithms, software, and hardware, the overall environmental impact remains significant. Recently, a major contributor to greenhouse gas emissions has been the production of hardware and infrastructure, rather than the energy consumption during the operational lifetime of these systems. This underscores the importance of adopting sustainable design practices to minimize the environmental impact of computing systems. The research emphasizes the recognition of greenhouse gas emissions related to products throughout their entire product development life cycle (PDLC). It provides a thorough theoretical and statistical analysis of carbon emissions and makes a compelling case for action.

Table 2.2 [12] provides a summary of recent contributions in this field. It is clear that the sustainability frameworks developed so far, while addressing various stages of the Product Development Life Cycle (PDLC), primarily focus on the product or system level. This creates a significant gap for designers who lay the groundwork for the components of a System-on-Chip (SoC) or product. To our knowledge, no existing framework or metric supports designers in making informed decisions during the early stages of the PDLC. The designer-oriented framework proposed in this work aims to bridge this gap.

Table 2.2: Previous contributions in the sustainability evaluation

Work	**Year**	**PDLC Stage**	**Proposals and Key Contribution**	**Limitation**
EE-Toolbox [13]	2000	Material Selection	• EE-Toolbox driven sustainability methodology • Material-based metrics: Toxic Potential, Recycling Potential, etc.	• Focuses only on material selection • No carbon footprint integration
Multi-criteria Eco-reliability [14]	2012	All PDLC Stages	• Introduced 'Eco-reliability' • LCA-based multi-criteria approach • Qualitative CFP evaluation	• No quantitative metrics
Sustainable IC Design [15]	2017	All PDLC Stages	• Parametric framework for 130 to 32nm • Shows impact of metal stack changes	• Chip/product-level only, not cell-specific
Chasing Carbon [11]	2022	Full Product Life Cycle	• Product-level carbon footprint analysis • GHG protocol-based categorization • Highlights manufacturing and operations impact	• No support for development phase • No metric-based analysis • Limited abstraction-level support
ECO-CHIP [16]	2024	System Architecture	• Open-source tool for chiplet-based sustainability analysis	• High-level abstraction only, not cell-specific
Eco-reliability Metric [17]	2024	System Analysis	• Circuit-level sustainability metric • Integrates reliability and environmental factors • Enables footprint comparisons	• No block-level or logic-specific designer tools

CHAPTER 3

Proposed Sustainability Framework

Life Cycle Analysis (LCA) involves evaluating greenhouse gas (GHG) emissions associated with the manufacturing and operation of a product throughout its entire life cycle. This process is crucial for classifying GHG emissions into different scopes, as outlined in Table 2.1.

The carbon footprint of a product can be estimated using two main components [11]:

- **Embodied footprint** - This refers to the carbon footprint (CFP) that is ingrained in the product before it even reaches the point of use. It includes emissions from the entire design and manufacturing process, such as design, prototyping, processing, validation and testing. Additionally, it encompasses emissions related to marketing and shipping.
- **Operational footprint** - This represents the CFP generated when the product is used throughout its life. It accounts for the energy consumed by the product during its operation across all possible modes.

Understanding this broad classification is essential for designers, as the key Figures of Merit (FoM) they consider when making design choices have a significant impact on either the embodied or operational footprint.

The area of a semiconductor chip significantly impacts its embodied footprint. In semiconductor manufacturing, multiple System-on-Chips (SoCs) are arranged in an array on a wafer and manufactured simultaneously. The energy and materials used during the processing of a wafer are distributed among the number of SoCs that can fit on it. When the area of each SoC is larger, fewer chips can be placed on the wafer. As a result, each SoC incurs a larger share of the greenhouse gas (GHG) emissions associated with wafer processing. Additionally, a larger chip area typically leads to a lower yield of functional SoCs. This further decreases the number of chips over which the manufacturing emissions can be spread, ultimately increasing the carbon footprint (CFP) of the SoC.

Performance directly influences the operational footprint of a system. Many advanced System-on-Chip (SoC) designs utilize a power-saving method known as pulse width modulation. In this method, the system is powered up to a high voltage level during operation, while at other times, the power supply is either turned off or reduced to a lower level. This approach helps to minimize power consumption. A high-performance system, with its capability for high throughput, can complete tasks more quickly, allowing it to be turned off sooner. As a result, this decreases overall power usage.

When a system is required to achieve a certain level of performance, multiple copies of a low-performing circuit can be utilized to boost throughput. This approach leads to an increased area, which in turn results in a larger embodied footprint. As a result, performance indirectly affects the size of the embodied footprint

3.0.1 Embodied footprint:

The embodied footprint encompasses all the carbon emissions linked to the manufacturing process of the entire chip, including its testing and validation. Equation (3.1) is utilized to assess the embodied carbon footprint for producing a specific design, offering insights into the carbon emissions associated with the manufacturing process.

$$\text{EFP} = \text{k} \times \text{Cell Area} \times \text{MF} \times \text{CF} \tag{3.1}$$

3.0.1.1 k:

It is a constant that provides information about the average fabrication energy required to manufacture a μm^2 area for a specific technology node. In this work, data from the 65nm technology node is utilized.

3.0.1.2 Cell Area:

This represents the area calculated for each approximate adder design, determined from the layout per μm^2 unit.

3.0.1.3 Mask Factor(MF):

This factor is introduced because additional masks may be necessary for chip fabrication, depending on the type of transistors used in the design. For instance, a High VTH (threshold voltage) transistor requires an extra mask for fabrication compared to a Standard VTH transistor. To account for any effects related to these additional masks in the calculation of the Embodied Footprint (EFP), this mask factor is applied. However, in this work, all designs have utilized only Standard VTH transistors, so there are no extra masks included in the Embodied Footprint calculation.

The Mask Factor serves as a multiplier to represent the additional impact that each extra mask introduces. In this analysis, it is set at 0.045, indicating a 4.5% increase in the associated impact for each mask added. This figure is derived from data in reference [22], which indicates that increasing the metal stack from 6 to 8 layers at the 65nm node leads to approximately an 18% increase in energy consumption.

3.0.1.4 Congestion Factor (CF):

In this work, the layout for the approximate adder is designed using 2 metal layers M1 and M2. This choice results in increased congestion at the system-on-chip (SoC) level, as the metal 2 layer becomes unavailable for routing purposes. The limited routing resources increase the design complexity at the SoC level, potentially leading to higher energy consumption during chip manufacturing. To address the impact of congestion on the manufacturing process, a congestion factor has been introduced.

3.0.2 Operational footprint:

The Operational footprint gives information about to the carbon emissions generated during the entire functional lifetime of a chip. This aspect is important because certain designs may consume considerably less power while in use compared to others, even within the same application, such as IoT, over an equivalent timeframe. Therefore, it is important to calculate the carbon emissions produced throughout a chip's operational life as well, in order to asses a design on sustainability.

$$\text{OFP} = (\text{Dynamic Power} + \text{Leakage Power}) \times T_{\text{total}} \tag{3.2}$$

The operational footprint is determined by considering both the dynamic power and leakage power consumed by a design throughout its functional lifetime (T_{total}). In this work, static power is ignored since all the designs used are digital and do not require any biasing. Hence, static power is not considered.

The dynamic power of a design is calculated using Equation (3.3). To analyze the operational footprint, the entire lifespan of a chip is divided into three modes: Active, Standby, and Switched Off. The total duration of the chip's life is denoted as T_{total}, with the ratios for each mode represented as follows: $\frac{T_{\text{active}}}{T_{\text{total}}}$, $\frac{T_{\text{standby}}}{T_{\text{total}}}$, and $\frac{T_{\text{switchedoff}}}{T_{\text{total}}}$.

$$\text{Dynamic power} = Q_{\text{dyn}} \times \alpha \times V_{\text{active}} \times f_{\text{operation}} \times \frac{T_{\text{active}}}{T_{\text{total}}} \tag{3.3}$$

The leakage power of a design is determined using Equation (3.4), as OFP comprises both dynamic and leakage power. Therefore, both types of power need to be calculated for a specific design.

$$
\begin{aligned}
\text{Leakage Power} = \Bigg(I_{\text{standby}} \times V_{\text{standby}} \times \Bigg(\frac{\text{STR}}{100} + \Bigg(\text{PWM} \times \frac{\text{ATR}}{100} \times (1 - \text{PF})\Bigg) \\
+ \Bigg(I_{\text{active}} \times V_{\text{active}} \times \frac{\text{ATR}}{100} \times \text{PF}^{\text{PWM}}\Bigg)
\end{aligned}
\tag{3.4}
$$

3.0.2.1 $Q_{\textbf{dyn}}$

It refers to the dynamic charge consumed during the switching operations of approximate adder designs.

3.0.2.2 α

It denotes the switching factor, which depends on the type of application for which the design is used.

3.0.2.3 $V_{\textbf{active}}$

It represents the operating voltage during active mode.

3.0.2.4 $V_{\textbf{standby}}$

It indicates the operating voltage during standby mode.

3.0.2.5 Performance Factor(PF)

It refers to the ratio of time taken by given design to the ratio of time taken to complete same operation by the Reference Design.

3.0.2.6 $f_{\textbf{operation}}$

It denotes the operating frequency of the design.

3.0.2.7 $I_{\textbf{active}}$

It indicates the current drawn during active mode of operation.

Table 3.1: Application-based operating time ratios

Operating Modes	**IoT**	**HPC**	**Auto**	**PE**
Active - ATR	5%	40%	15%	10%
Standby - STR	25%	40%	45%	30%
Switched off - SOTR	70%	20%	40%	60%
Operational Lifetime (hours)	20000	25000	10000	35000

3.0.2.8 $I_{\textbf{standby}}$

It represents the current drawn during standby mode of operation.

3.0.2.9 PWM

It refers to pulse width modulation when a design can operate in different mode based upon the requirement for example while doing compute going into active mode while idle going to standby mode etc. if a design supports PWM then this factor is set to 1.

By using the sustainability paradigm to calculate Embodied Footprint (EFP) and Operational Footprint (OFP), each design will be evaluated for sustainability.

3.0.2.10 Application Profiles

In this work, we explore four key applications in electronics: the Internet of Things (IoT), High-Performance Computing (HPC), Portable Electronics (PE), and Automotive (Auto). These application profiles encompass nearly 90% to 95% of all existing electronic applications, each with different timing ratios.

The operational lifetime of any chip will vary based upon the application in which the chip is being used, because of the variation of different modes of operation for a mode in an application. These different applications are considered to validate the robustness of the proposed sustainability paradigm. The timing ratios for different applications are presented in the Table. 3.1.

CHAPTER 4

Post-Layout Analysis

All architectures in this study are simulated using a supply voltage of 0.7V (VDDH) under typical (TT) conditions at a temperature of 27°C. The following details outline the considerations for evaluating the key figures of merit (FOMs) of the approximate adders:

The layouts for each design illustrated in Chapter 1 are as follows.

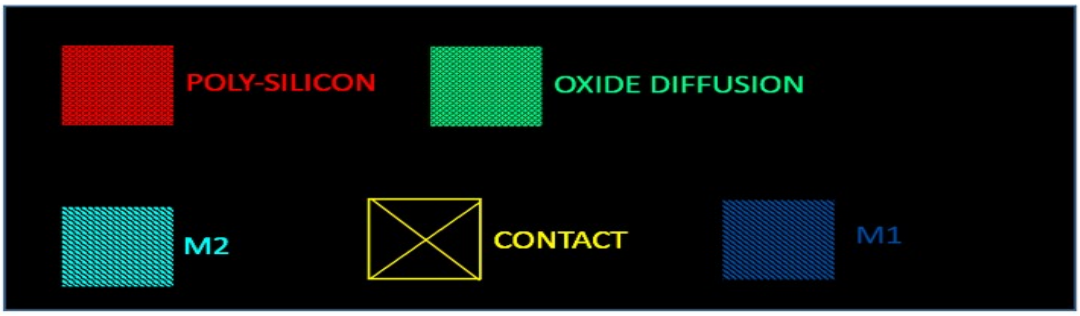

Figure 4.1: Layer Information of Layout

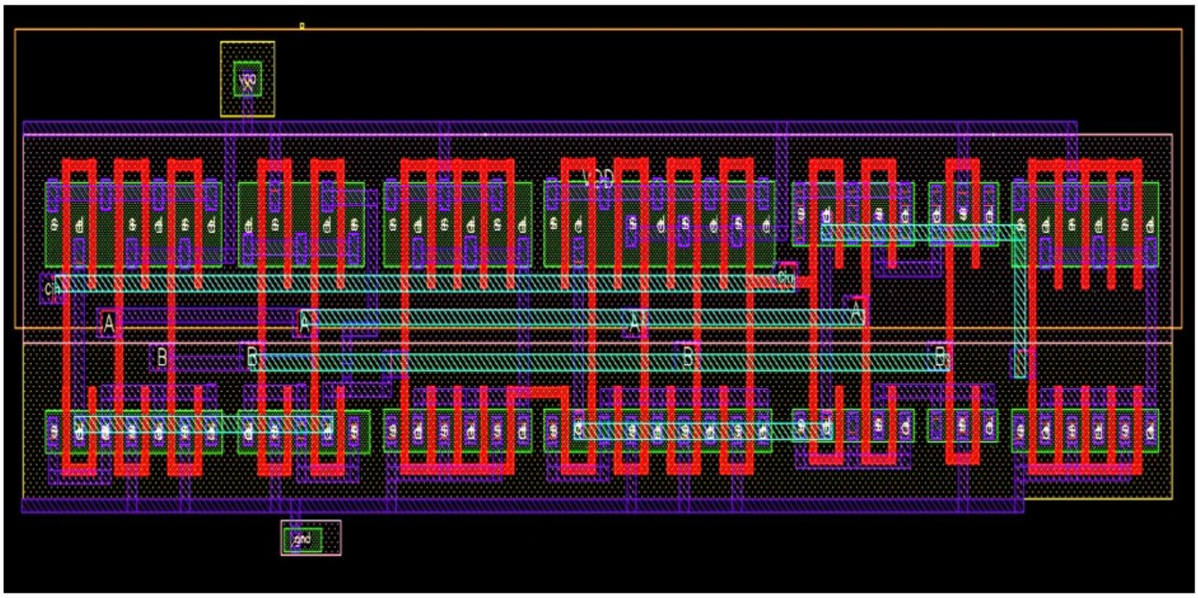

Figure 4.2: Layout of Conventional Mirror Adder

All the layouts shown from Fig. 4.2 to Fig. 4.5 belong to Approximate Mirror Adder Architectures. Further, the advanced approximate adder layouts are presented as follows.

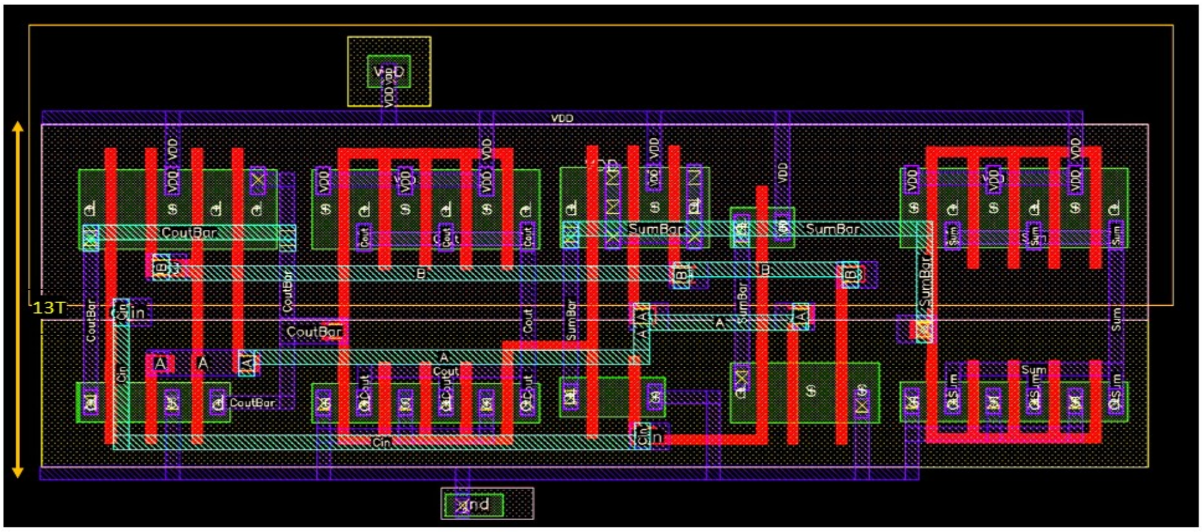

Figure 4.3: Layout of AMA1 design

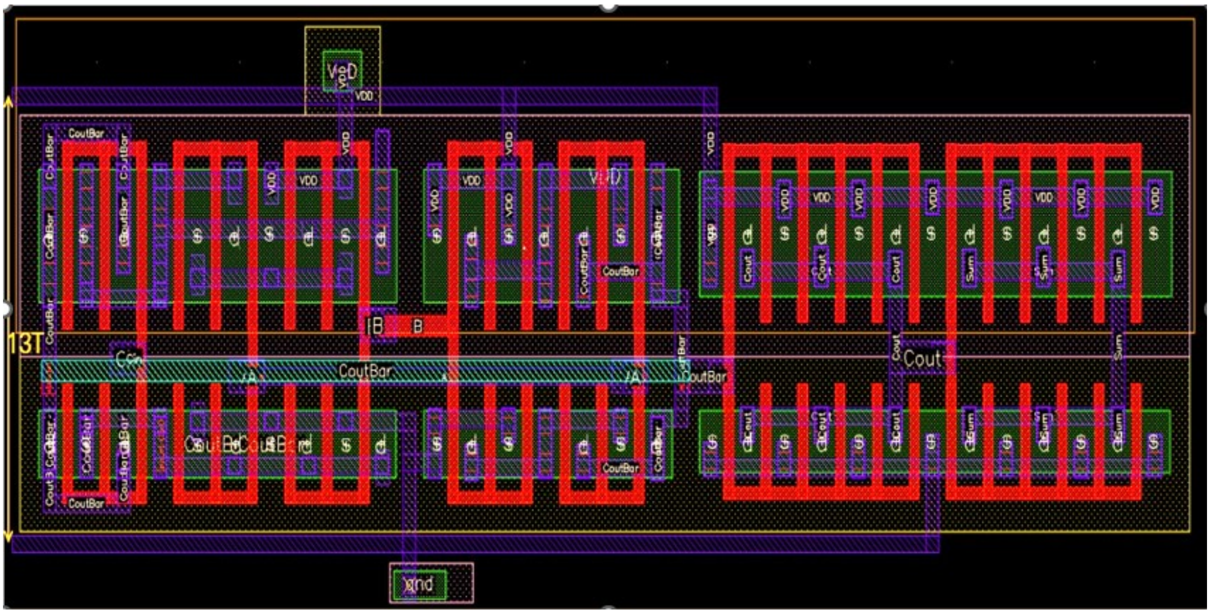

Figure 4.4: Layout of AMA2 design

4.0.0.1 Area

In this work, all layouts are designed to maintain a constant height of 13 tracks, as illustrated in Figures 4.3 and 4.7. This consistent height allows us to evaluate which design is the most area-efficient based on the width of each layout. From Table 4.1, it is clear that LCAFA3 has the smallest area among the designs. Notably, the areas of AMA1 and AMA3 are equal, despite the significant difference in the number of transistors between the two. This similarity in area arises from the utilization of the M2 layer, which enabled the layout of AMA1 to be as dense as that of AMA3, even with fewer transistors. The use of M2 tracks for each design is detailed in Table 4.1.

To maintain a consistent height in the layouts, we have utilized larger transistors by dividing

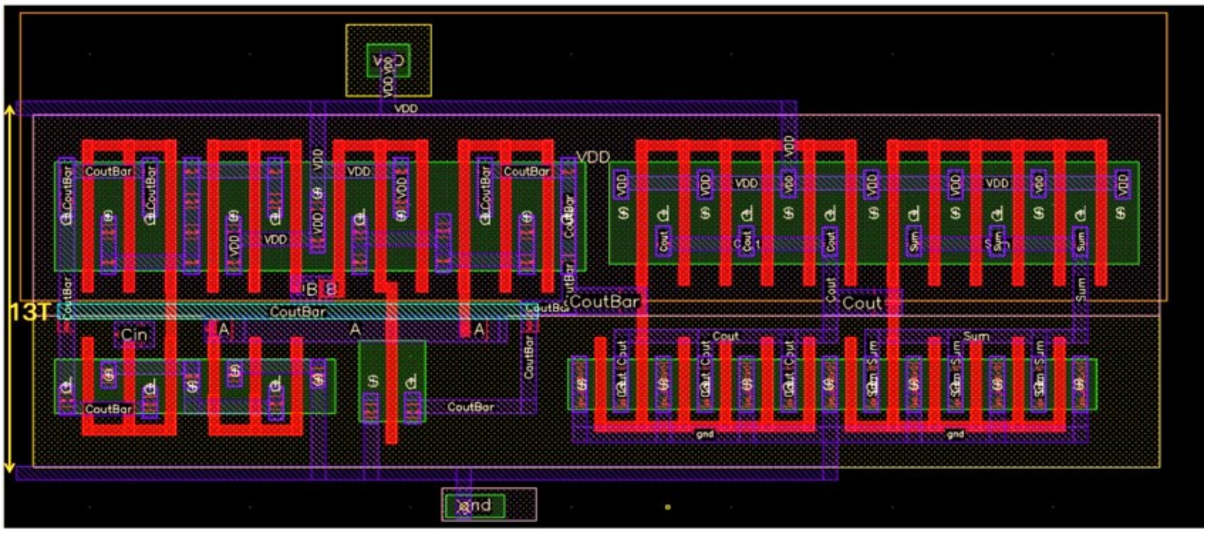

Figure 4.5: Layout of AMA3 design

Table 4.1: Post-layout simulation results of some of key Figure of Merits (FOMs) for approximate adder designs for IoT application

Design Name	**Area (μm^2)**	**# M2 Tracks used**	**Dynamic Power (nW)**	**Leakage Power (nW)**	**Total Power (nW)**	**Error Rate (%)**
CMA	29.38	7	237	486.75	724	0
AMA1	18.20	10	308	33.48	341	25
AMA2	21.32	1	214	22.54	237	25
AMA3	18.20	1	232	21.30	253	37.5
CXA	16.90	10	155	90.01	245	0
LCAFA1	18.20	11	5.98	84.05	90	0
LCAFA2	23.40	2	6.65	104.02	111	25
LCAFA3	9.41	2	9.06	67.20	76.26	25

them into smaller fingers, as illustrated in Fig 4.3.

4.0.0.2 Iso Delay

In this work, we have fixed the propagation delay of each approximate adder to be $275\,\text{ps}\pm 10\%$. By keeping this parameter constant in the PPA (Power-Power Area) analysis, we can ensure a fair comparison of power and area across all designs.

4.0.0.3 Dynamic Power

Dynamic power refers to the power consumed during the operation of a circuit. It is influenced by the supply voltage (VDD), which is set at 0.7 volts. For this analysis, we use a switching factor (α) of 5%, based on typical IoT applications, and operate at a common frequency of 100

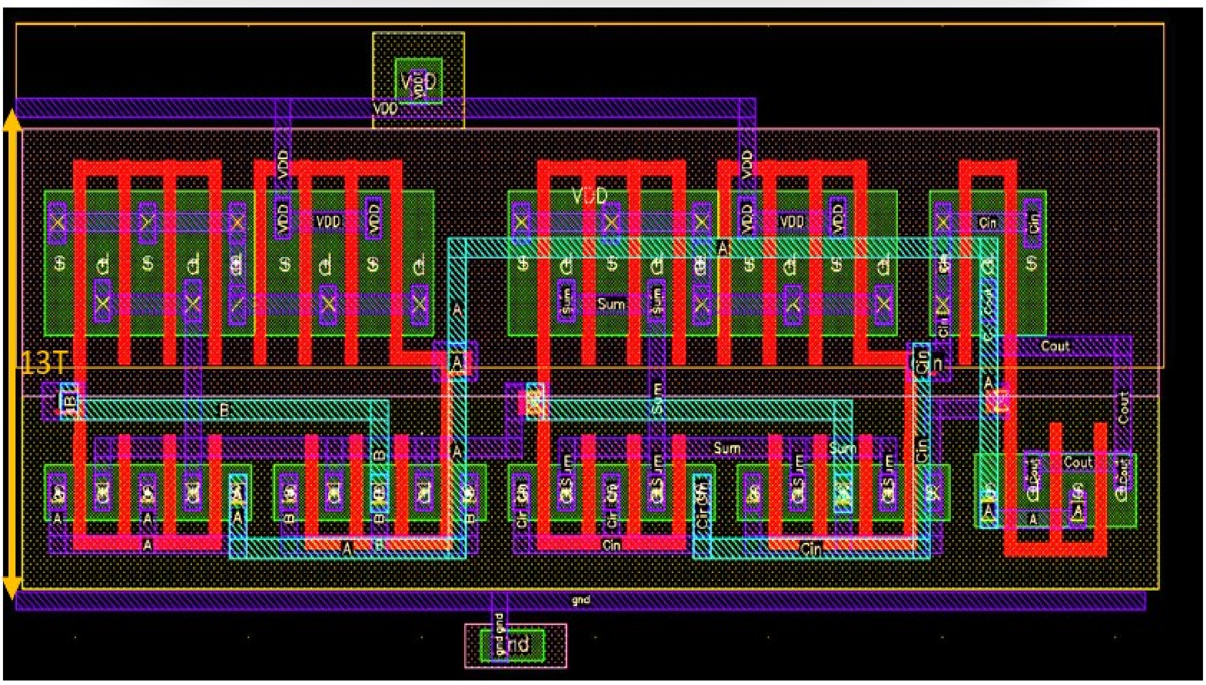

Figure 4.6: Layout of CXA design

MHz, which is frequently used by most IoT devices. From Table 4.1, it is clear that LCAFA3 emerges as the most power-efficient design among those considered in this study.

4.0.0.4 Leakage Power

In this work, leakage power is defined as the power that dissipates when transistors are in the OFF state. The leakage power for various designs is presented in Table 4.1.

4.0.0.5 Total Power

In this study, total power is defined as the sum of dynamic power and leakage power. Since all the circuits examined are digital and do not require biasing, static power is not considered.

Having completed all post-layout observations, we can now proceed to analyze which design is more sustainable in the following chapter.

All post layout Simulations are done by considering VDD as 0.7 V and 100MHz frequency of Operation and 5% switching factor across all the designs.

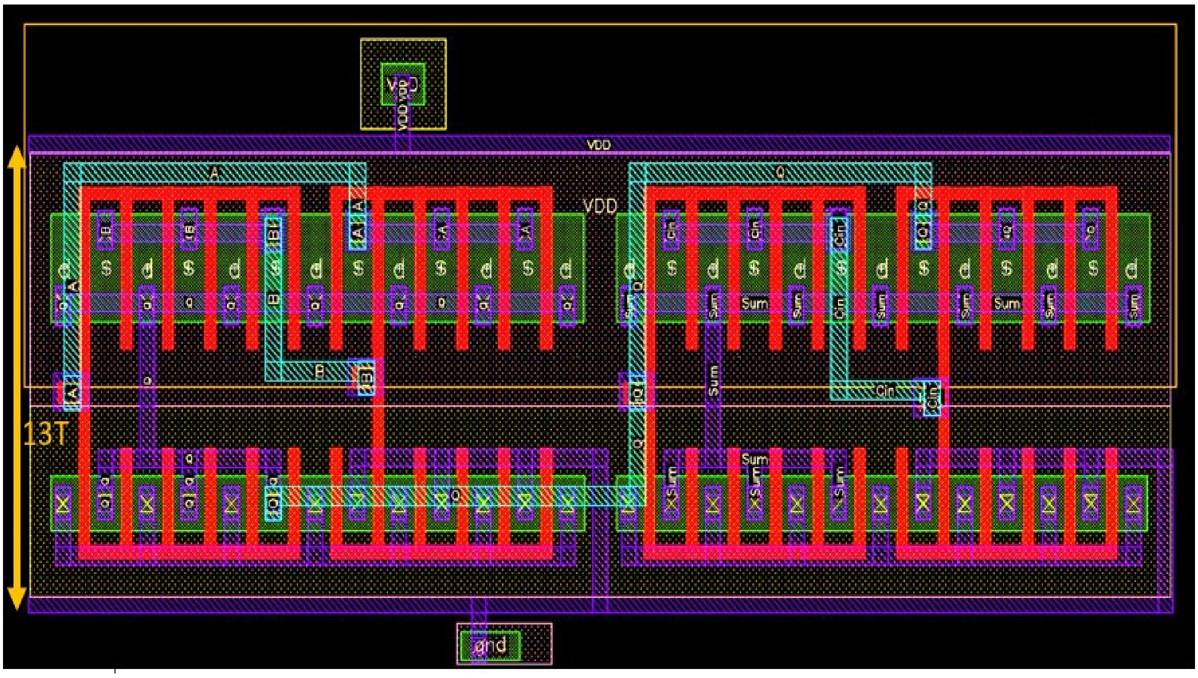

Figure 4.7: Layout of LCAFA1 design

Table 4.2: Post Layout Observations of Embodied Footprint

Design	**IP Area** (μm^2)	**Ref. Masks**	**Extra Masks**	**Total Masks**	**# M2 Tracks**	**# Metal Tracks in Porous Layer**	**Embodied Footprint** (mWh/IP)
CMA	29.8	36	0	36	7	56.5	2.36
AMA1	18.2	36	0	36	10	35	2.17
AMA2	21.32	36	0	36	1	41	1.30
AMA3	18.2	36	0	36	1	35	1.11
CXA	16.9	36	0	36	10	32.5	2.01
LCAFA1	18.2	36	0	36	11	35	2.87
LCAFA2	23.4	36	0	36	2	45	1.47
LCAFA3	9.41	36	0	36	2	18.09	0.59

Table 4.3: Post Layout Simulation results of Operational Footprint

Design	**IP Area** (μm^2)	**Dynamic Charge** (fC/transition)	**Leakage Current @0.7V**	**Dyn. Power** (nW)	**Leak. Power** (nW)	**Operational Footprint** (mWh/IP)
CMA	29.8	67.8	17715	237	486	17.50
AMA1	18.2	88	418	308	33	1.71
AMA2	21.32	61.2	395	214	22	1.16
AMA3	18.2	66.4	301.8	232	21	1.15
CXA	16.9	44.29	1649	155	90	3.42
LCAFA1	18.2	1.7	90	5.98	84	2.95
LCAFA2	23.4	1.9	39	6.65	104	3.65
LCAFA3	9.41	2.59	36	9.06	67	2.37

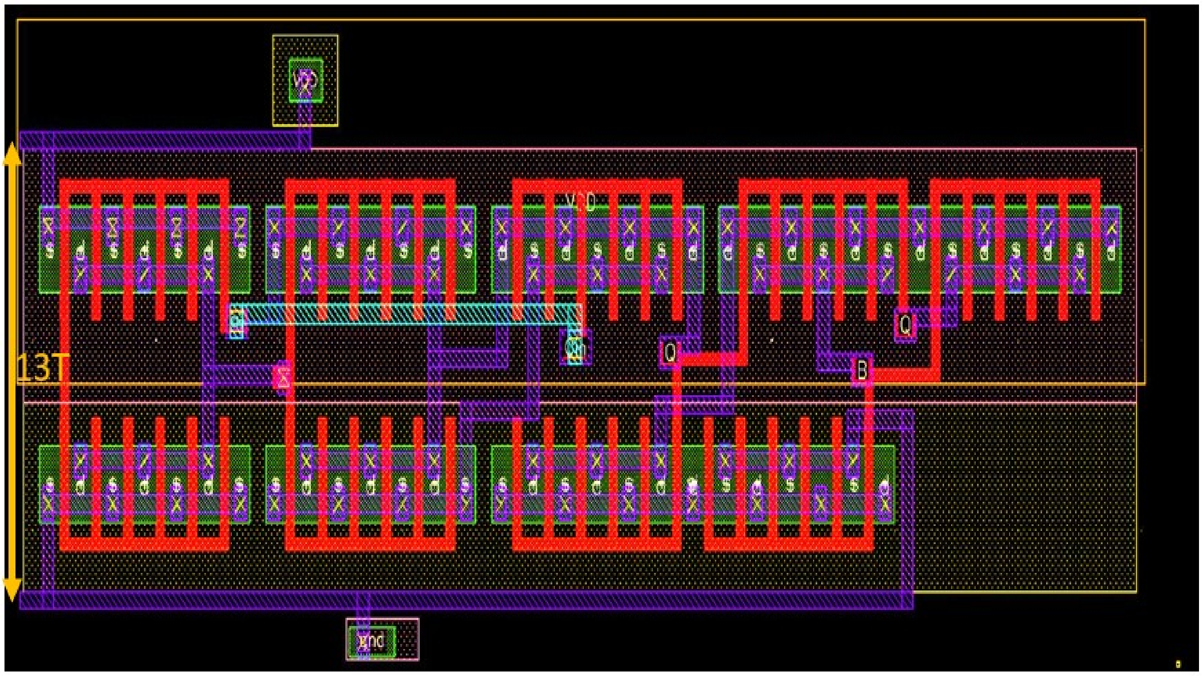

Figure 4.8: Layout of LCAFA2 design

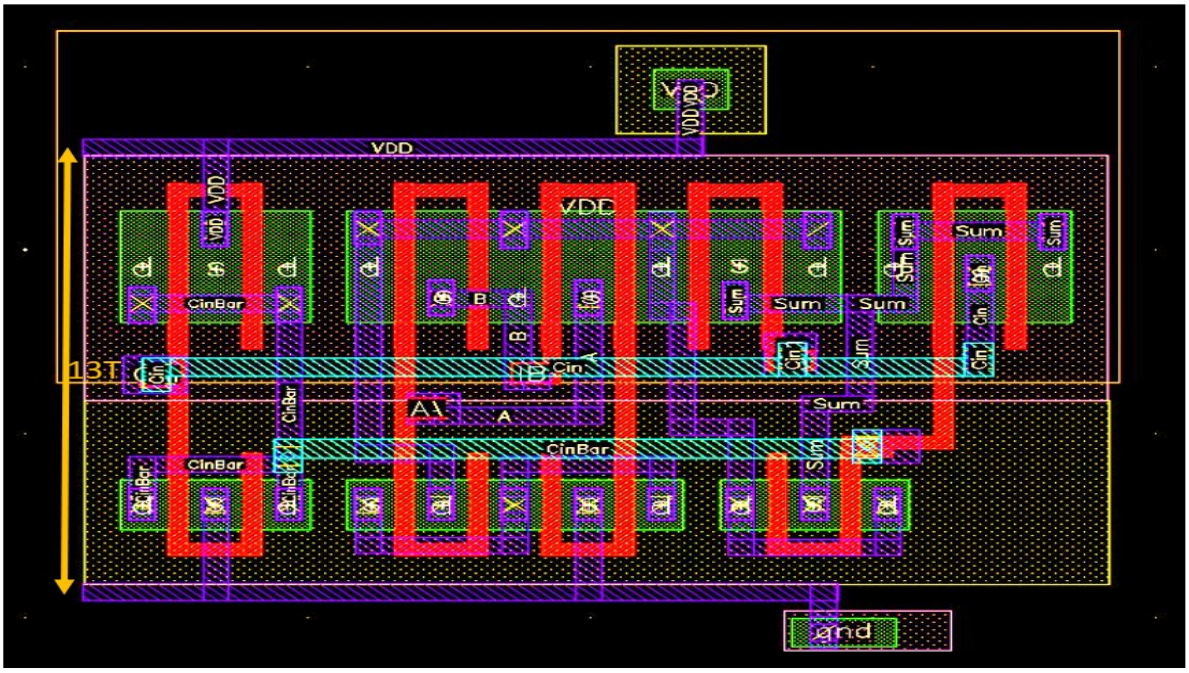

Figure 4.9: Layout of LCAFA3 design

CHAPTER 5

Sustainability Assessment of Approximate Adder Designs

5.1 Embodied Analysis of Approximate Designs

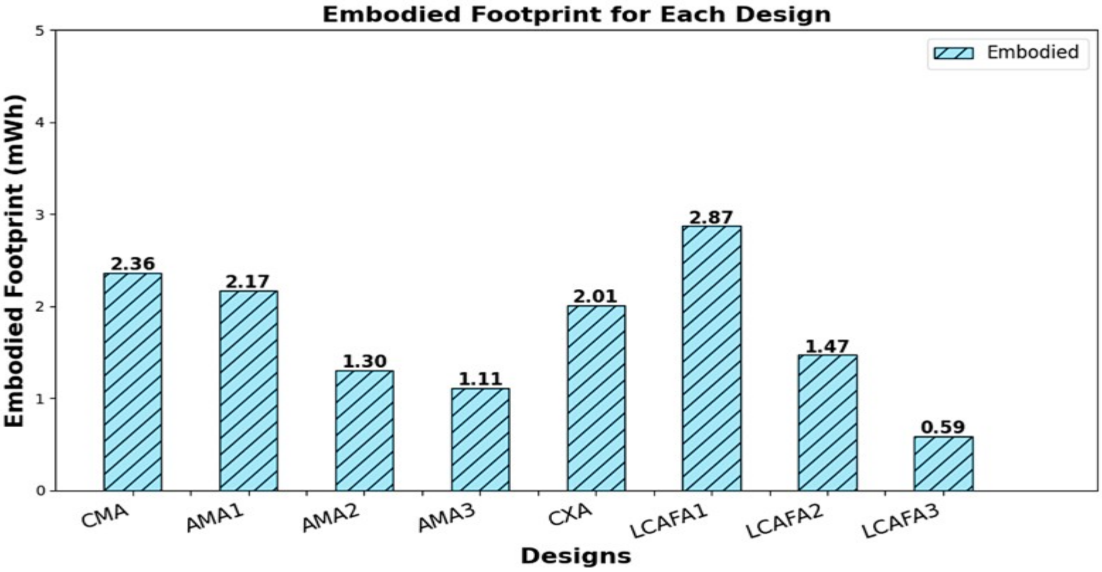

Figure 5.1: Embodied Footprint results of Approximate Adder Designs

The embodied footprint of the LCAFA1 design is the highest indicating LCAFA1 requires more energy for manufacturing, despite its area not being larger than that of a conventional mirror adder (CMA), as shown in Table 4.1. This is primarily due to the congestion factor considered in the analysis. The LCAFA1 design utilizes 11 out of 13 M2 tracks, as depicted in Fig. 4.7, which results in increased congestion at the System on Chip (SoC) level. Consequently, the LCAFA1 design is the least sustainable option due to this heightened congestion.

From Table 4.1, we can see that while both designs, AMA1 and the conventional Xor-Xnor Adder (CXA), utilize same number of M2 routing tracks, they differ in area efficiency. Consequently, CXA emerges as the more sustainable option between the two designs, as embodied in this case, has more weightage on area efficiency.

The LCAFA3 design emerged as the most sustainable option due to its lowest embodied footprint value, as it achieves the highest density with the fewest M2 tracks in this study.

5.2 Operational Analysis of Approximate Designs

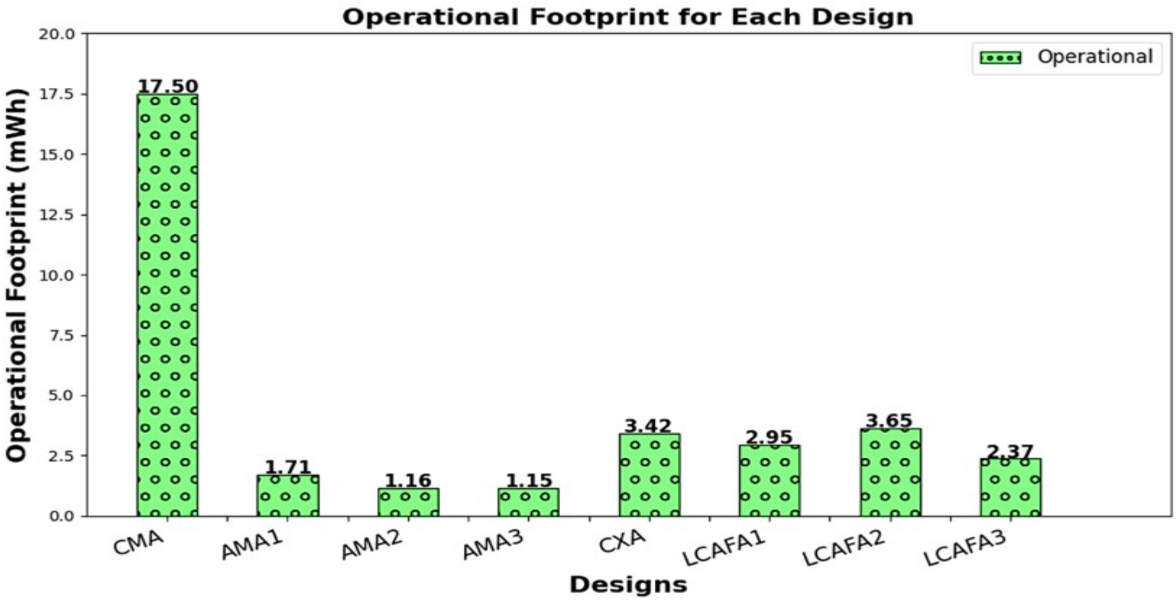

Figure 5.2: Operational Footprint results of Approximate Adder Designs

From Fig. 5.2, the operational footprint of the CMA design is the largest among the options. This is further supported by Table 4.1, which illustrates that the CMA has the highest total power consumption compared to the other designs in this study. Consequently, this suggests that the CMA is the least sustainable option based on its operational footprint.

The results shown in Fig. 5.2 highlight an interesting finding: the operational footprint of the LCAFA3 design is greater than that of the AMA3. This difference is noteworthy, particularly given that, as indicated in Table 4.1, the total power consumption of the AMA3 is significantly higher than that of the LCAFA3.

This discrepancy is due to the operating modes considered for IoT applications. While the dynamic power of the AMA3 is higher, which leads to its increased total power consumption, the active mode only accounts for about 5% of the total time in IoT applications. In contrast, the LCAFA3, which has greater leakage power, remains in the off mode for roughly 70% of the time during these applications. Consequently, the LCAFA3 has a larger operational footprint.

Therefore, the choice of a sustainable design may differ based on the specific type of application.

Upon examining Table 4.1, we observe that the leakage power of Approximate Mirror Adders (AMA1, AMA2, AMA3) is lower than that of the advanced approximate adders (LCAFA1, LCAFA2, LCAFA3). This characteristic makes Approximate Mirror Adders more suitable for applications with longer idle times, where the design is primarily in a switched-off mode. In contrast, for applications with higher active times, such as those involving artificial intelligence, the advanced approximate adders prove to be more sustainable based on their operational footprint.

5.3 Total Footprint Analysis of Approximate Designs

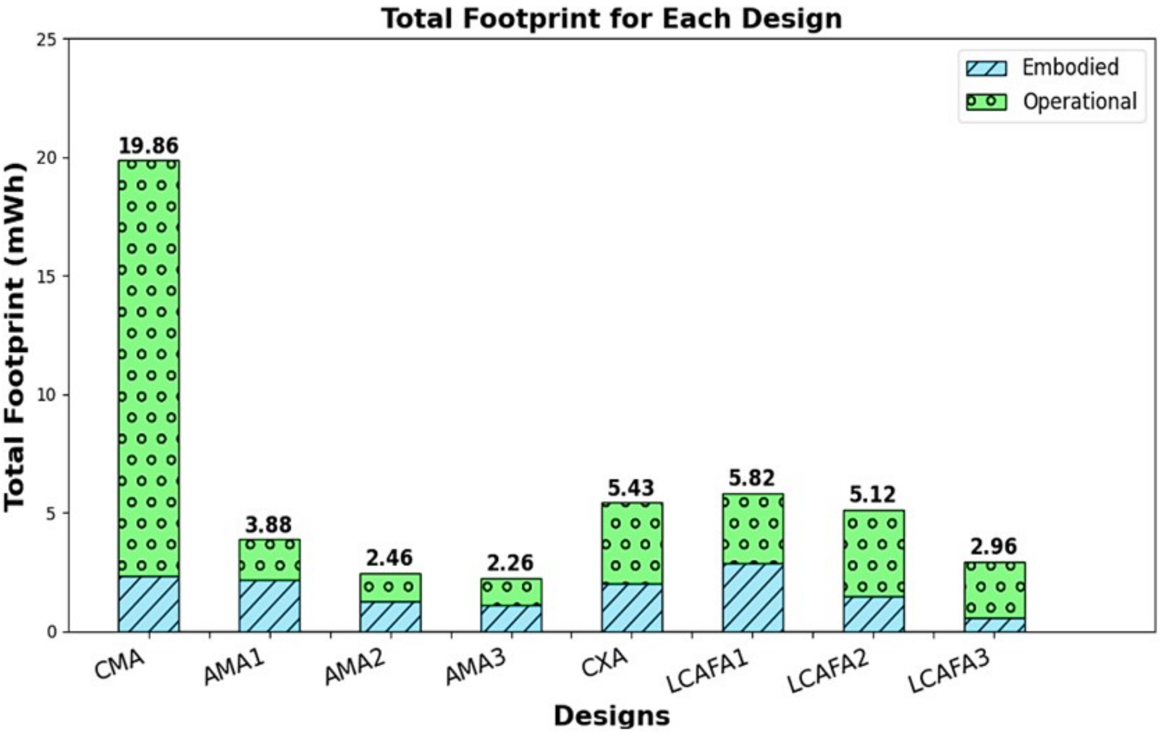

Figure 5.3: Total Footprint results of Approximate Adder Designs

Observing Fig. 5.1, it is clear that LCAFA3 is a sustainable option. Furthermore, Fig. 5.2 indicates that the AMA3 design is also sustainable. The total footprint presented in Fig. 5.3 reinforces the conclusion that the AMA3 design is the most sustainable choice. It is crucial to highlight that when making a final decision regarding sustainable design, the designer should always consider the total footprint. Relying solely on one type of footprint—whether embodied or operational—can lead to an incomplete and inefficient sustainability assessment.

The Total footprint plot in Fig. 5.3 shows that approximate mirror adders are a more sustainable option compared to advanced approximate adders for IoT applications.

When a designer must choose between two adders, AMA1 and LCAFA3, for a sustainable solution, they should opt for LCAFA3. The total footprint of LCAFA3 demonstrates that it is the more sustainable choice compared to simply selecting approximate adders, especially in the context of an IoT application. Therefore, the findings suggest that the proposed approach to sustainability is effective, as it considers both embodied and operational footprints, leading to a fair decision.

5.4 Other Results

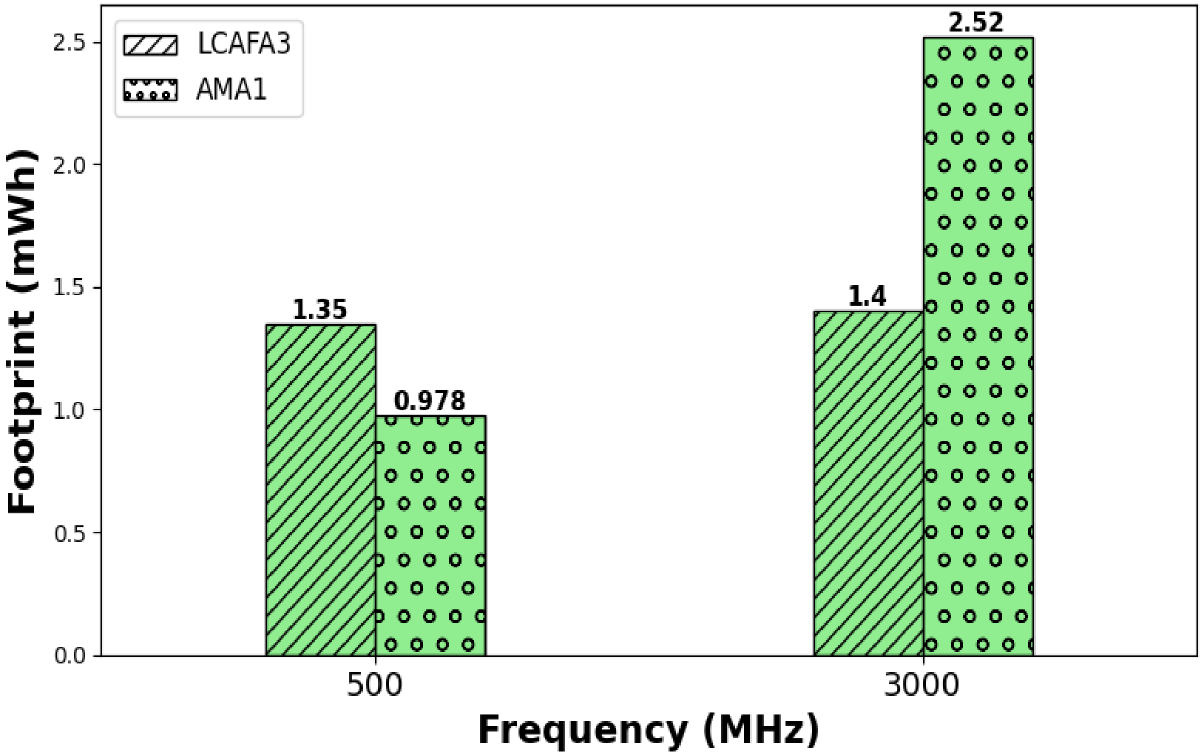

Figure 5.4: Impact of frequency of operation on operational footprint

The Fig. 5.4 is a plot depicting different Operational footprints at different frequencies of operation for two designs, LCAFA3 and AMA1.

When both designs are operated at 500 MHz, AMA1 has the lowest operational footprint, making it the most sustainable choice. However, when both designs are operated at 3000 MHz, the operational footprint of AMA1 increases significantly, which makes LCAFA3 the more sustainable option. This variation occurs because the operational footprint includes dynamic power consumption, which is influenced by the frequency of operation. Thus, it is evident that the most sustainable design choice can change based on the frequency at which the design is operated.

The Fig. 5.5 depicts the opeartional footprint of two design across different applications at frequency of 500 MHz and 1% switching factor.
We evaluated four different applications, as discussed in the previous chapters, each consisting of varying ratios of timing modes. From the results, we can observe that if a designer aims to

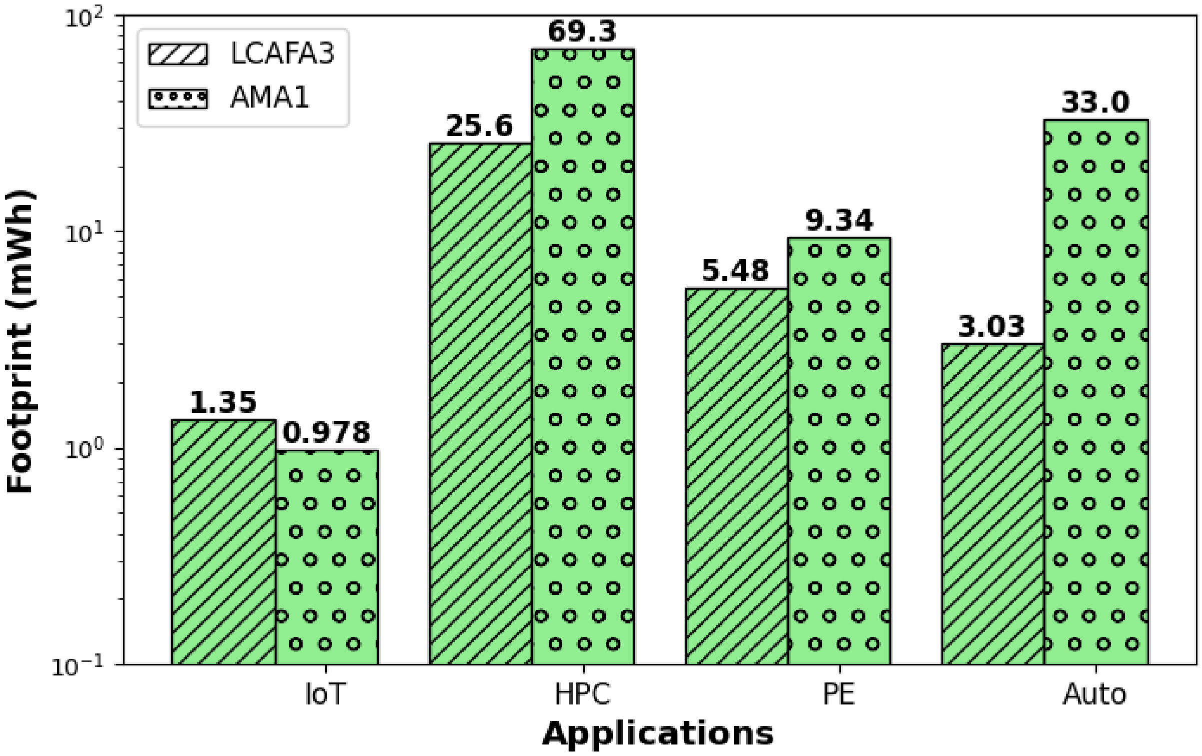

Figure 5.5: Composite Application analysis results of Approximate Adder Designs

implement a design for IoT applications, they should choose AMA1, as it has the lowest operational footprint. For all other applications, the designer can opt for LCAFA3, as its operational footprint is smaller compared to the others. So, based on the type of application in which the design will be used, a sustainable choice can further vary.

The results presented above include various footprints, such as the embodied footprint, operational footprint, and total footprint, along with different outcomes related to operating frequency and application types. These findings conclude that the proposed sustainable paradigm is robust, and designers can utilize it to make sustainable choices across different designs, ensuring long-term reliability.

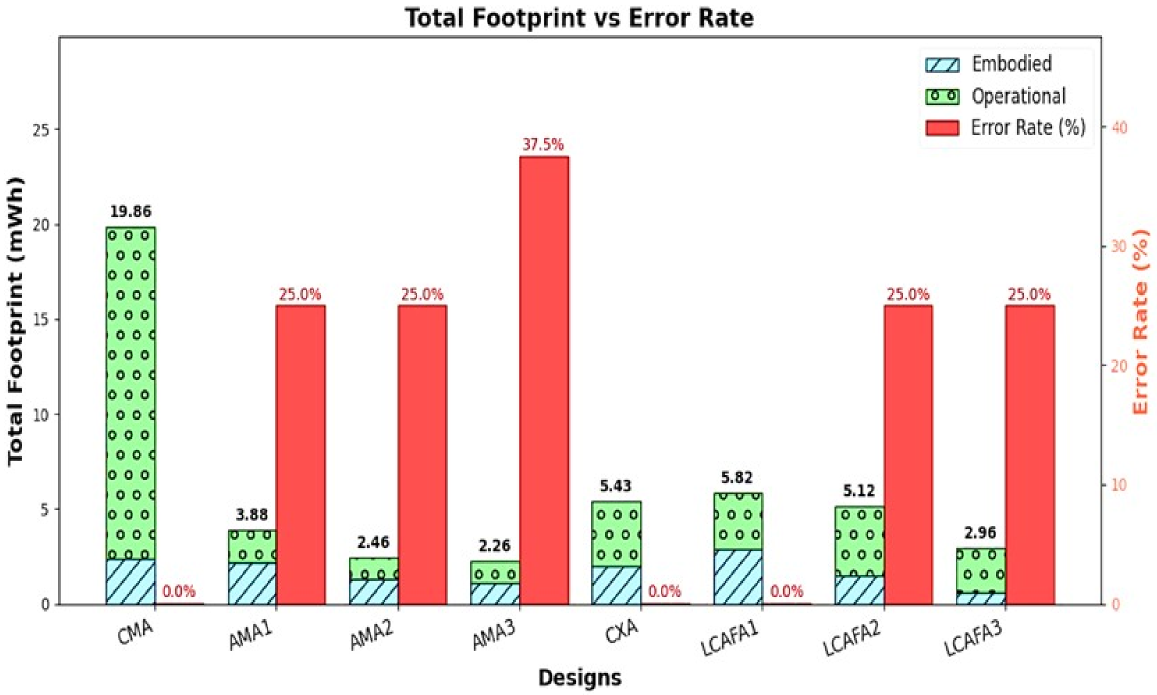

Figure 5.6: Total Footprint vs Error Rate Comparison for Sustainable design choice

The comparison of Total Footprint with Error Rate in Figure 5.6 presents some fascinating insights regarding design choices. Here are the key considerations:

- If the adder's sum must be precise for the intended application, then the conventional XOR-XNOR adder is a sustainable choice, as it has a total footprint that is smaller with an error rate of 0%.
- If the application can tolerate a 25% error rate, the AMA2 design becomes a more sustainable option due to its significantly lower total footprint, albeit with a 25% error rate.
- For applications that are more error-resilient and can accept an error rate greater than 37.5%, the AMA3 design is the most sustainable choice. Therefore, depending on the specific application and its error resilience, the optimal sustainable design for an approximate adder can vary.

CHAPTER 6

Conclusion

Traditional IC evaluation using Power, Performance, and Area (PPA) metrics is no longer sufficient in light of rising energy demands. Existing sustainability approaches focus mainly on manufacturing or high-abstraction levels, excluding cell-level designers. This work proposes a sustainability framework that empowers designers to assess environmental impact during early design stages. Validated on various logic cell architectures, the framework reveals insights beyond conventional FoMs and supports sustainability-aware design choices.

The sustainability framework proposed in this work thoroughly analyzes design based on various parameters. These parameters include the area, switching factor, no.of masks required, frequency of operation, and the number of M2 tracks used in the design layout. All of these factors are considered to make a sustainable design selection that aligns with the specific application requirements.

The proposed pardigm can be extended and customized to meet the needs of the designer's organization, aiding their journey towards net zero emissions in the VLSI industry.

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List of papers based on Thesis

1. A. Grover et al., “Sustainability Framework for Computing Element Design,” 2025 International Conference on ICT for Sustainability (ICT4S), Dublin, Ireland, June 2025.
2. A. Grover et al., “Framework to Estimate and Benchmark Sustainability of Circuit Design,” 2025 IEEE Region 10 Symposium (TENSYMP), New Zealand, July 2025.