IIIT DELHI

M.TECH THESIS

Noise Suppression Techniques using Active Decoupling Capacitors in a Power Distribution Network

Submitted By:
Pankhuri, MT15102

Supervisor:
Dr. Mohammad S. Hashmi

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Declaration of Authorship

This is to certify that the dissertation titled "Noise suppression techniques using Active Decoupling Capacitors in a Power Distribution Network" submitted by Pankhuri for the partial fulfillment of the requirements for the degree of Master of Technology in Electronics and Communication is carried out by me under the guidance and supervision of Dr. M. S. Hashmi at Indraprastha Institute of Information Technology, Delhi.The results obtained in this thesis work has not been submitted anywhere else for the reward of any other degree.

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This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Dr. Mohammad. S. Hashmi, IIIT Delhi

IIIT Delhi

Abstract

Dr. Mohammad S. Hashmi
Department of ECE

M.Tech

Noise Suppression Techniques using Active Decoupling Capacitors in a Power Distribution Network

by Pankhuri, MT15102

The reduction in the device dimensions, the increasing switching activity and the high power consumption in the IC design cause large currents to flow in a Power Distribution network(PDN). The switching currents cause the fluctuations in the supply voltage due to high voltage drops such as IR drop and Ldi/dt drop. These fluctuations cause failures and affect the reliability of System on Chip. Therefore, a robust Power Distribution Network is essential for the effective and reliable operation of a chip.
Due to the variations in power supply, the PDN suffers from timing fluctuations, thus affecting the propagation delay of a circuit. This thesis addresses the delay variations in a CMOS inverter. The high to low and low to high propagation delays have been analyzed using mathematical models and simulations. Thus the challenge lies in reducing the delay variations due to the changes in power supply. Hence, a power delivery network needs to be modeled in order to have reduced supply variations.
The capacitance between the power and ground networks known as decoupling capacitance(decap) in a PDN acts as a charge storage and helps in reduction of supply drop. Various intrinsic decaps like MIM(metal insulator metal) decaps incorporated in previous works offer limitation of large area consumption and have been ineffective in reducing the drop. Hence there is a necessity to model the passive decap effectively.
This dissertation mainly focuses on the analog and digital techniques to model the decoupling capacitance in a PDN. Firstly, the work aims at increasing the effective decap value with aid of operational amplifier and miller effect which results in the reduction of supply drop by 20%. Moreover, a sleep transistor technique has been implemented to dampen the resonance because of the addition of resistance in the circuit. Secondly, a digital technique known as charge injection method addresses the overshoot and undershoot detection and reduces the drop by 75%. The work is carried out in Cadence Virtuoso environment using 65nm technology at IIIT Delhi.

Acknowledgements

The work for the thesis was carried out at IIIT Delhi, during 2016-2017. I wish to thank my advisor, Dr. Mohammad. S. Hashmi for providing guidance for this work, without which it would not have been successful. I have a deep sense of gratitude towards him for providing constant support and valuable feedback that enabled successful completion of the thesis. I would also like to thank Mr. Shashwat Kaushik for his constant encouragement and assistance during the period of the thesis and at last my parents and friends for supporting me during the entire post-graduation period.

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Chapter 1

INTRODUCTION

1.1 Power Distribution Network

A Power Distribution Network is responsible for delivering power from Voltage Regulator Module to a system on chip.Due to the increase in the switching frequency, reduced device dimensions and increased power consumption, there is a flow of large switching currents in the power and ground networks. These fast switching currents can produce timing failures and can affect the performance and reliability of a PDN. An efficient and robust power delivery network is essential for proper functioning of a system on chip.
The PDN is useful in the following ways:

- Provides a constant supply voltage to a system-on chip.
- Provides reduced area overhead.
- Easy to lay out and consumes less wiring
- Meets peak and average power requirements.

1.1.1 Causes of variation in supply voltage

- Due to the presence of the resistive on chip and power supply networks, the supply voltage delivered to various devices on a die is not ideal.This drop in the supply voltage is referred to as the IR drop. IR drop is caused due to the resistance of the interconnects and wires and resistance constituting the package and printed circuit board. There are two types of IR drop: One is the static drop and other is the dynamic drop. Static drop is due to the voltage drop between power and ground pads based on the average power/current.The dynamic drop is due to the simultaneous switching phenomenon i.e RC transient behavior when there is a sudden increase/decrease in the demand of current.
- The package model constituting the PDN has a significant amount of inductance which causes a voltage drop due to the switching currents drawn by devices. This voltage drop is referred to as the Ldi/dt drop. Ldi/dt is present only at high frequencies. It can be reduced by adding decoupling capacitors at certain locations in a die.
  So, the total voltage drop can be accounted as:

$$V_{\text{drop}} = IR + L\frac{di}{dt}$$

1.1.2 Problems due to variation in supply voltage in a PDN

- Voltage fluctuations over a range of frequency.
- Reduced switching speeds and noise margins of the circuits
- Electromigration issues like wearing out of metals due to high current densities.
- Return path discontinuity: high impedance path for the return currents to flow.
- Producing radiated emissions due to high currents leading to EMC failures.

1.1.3 Decoupling Capacitors in a PDN

Capacitors between power and ground networks are referred to as decaps or decoupling capacitors[7]. These decaps act as a medium for storing the charge and helps in stabilizing the power supply voltage. There are two types of decoupling capacitance in a PDN:

- Intrinsic Decap: Parasitic capacitance between the the metal interconnects of the supply lines, device capacitances and the capacitance between substrate and N-well accounts to intrinsic decap.
  The intrinsic decoupling capacitance is not sufficient to constraint the voltage drop within prescribed safe limits. So, designers have to add explicit decap on the die at supply points.
- Extrinsic Decap: The explicit decap added occupy more area and consume more power in a chip.

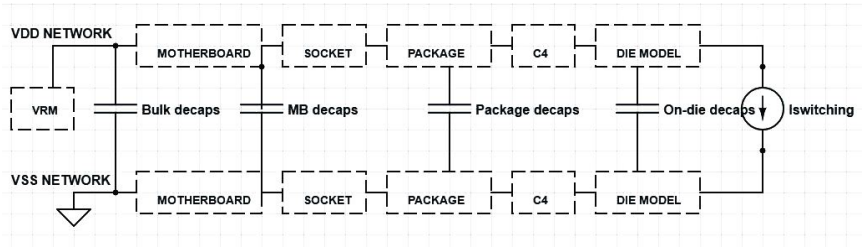

FIGURE 1.1: Power Distribution Network of a chip

The Figure 1.1 shows the simple model of a Power Distribution Network including all the elements of a chip. The voltage regulator provides voltage to all the elements of the chip through wire bond pads or capacitor bumps. Decoupling capacitances are placed at various locations to mitigate Ldi/dt noise in the supply.

1.2 Need for modeling Power Distribution Networks

- Due to increase in the design growth and power consumption, The di/dt effects have become a growing concern.
- Moreover, for reducing the supply drop, use of intrinsic and extrinsic decaps have been made for the overall chip. Hence, It is necessary to accurately model a chip keeping in mind the estimation of the amount of the decap added to the die.

1.3 Impact of supply variation on circuit performance

The voltage fluctuations in a PDN can lead to a noisy circuit and can produce timing failures in a circuit. Also, with the decrease in the voltage the delay of the circuit also changes. The circuit delay becomes sensitive to the voltage variation as the difference between the threshold voltage and the supply voltage becomes less. Hence, there is a need for the analysis of supply voltage variation on the circuit performance. Power supply variation can affect the circuit delay in two ways. First is the reduction in the drive strength due to reduced voltage leading to increase in the delay. Secondly, a difference in the supply voltage between a transmitter and receiver pair creates an offset voltage and thus produces a time shift in the signal transition. The increase in the voltage drop at one gate may degrade the delay of one gate while improving the delay of another. Hence, the analysis of delay with a transmitter and a receiver block is one of the major challenges.

1.4 Decoupling capacitance modeling

The following sources of capacitance affect the circuit supply in a PDN:

- Wire capacitances of the signal nets, power/ground interconnects.
- parasitic capacitances of MOS transistors
- Extrinsic decoupling capacitors

The device capacitances have much larger magnitude than the wire capacitances. The particular state of the signal also determines the effect of these capacitances on the circuit. There are 5 device capacitances associated with a transistor: C_{gs}(gate to source), C_{gd}(gate to drain), C_{db}(drain to bulk), C_{sb}(source to bulk), C_{gb}(gate to bulk). The C_{sb} can be neglected as source and bulk are at the same potential for both NMOS and PMOS.

Figure 1.2 shows the remaining capacitances for a CMOS inverter in the Inverter chain[5]. Assuming the first inverter to be switching and the other two as non switching, the device capacitance in Figure 1.2 can be modeled into equivalent RC circuit as shown in Figure 1.3. The resistance R_{pm} is the net pull up resistance of inverter 1, R_{nm} corresponds to the pull down resistance for Inverter 2. The resistance R_{pwell} and R_{nwell} are the resistances of the p well and n well. Since net A is low capacitances C_{gbn}, C_{gsn} and C_{dbn} are discharged and do not account for the decoupling in the circuit. The approximate model for device capacitances can be seen in Figure 1.4. The effective resistance is seen as the sum of the high and low resistances of the gates[18].

$$R_{\text{eff}} = R_{\text{pm}} + R_{\text{nm}}$$

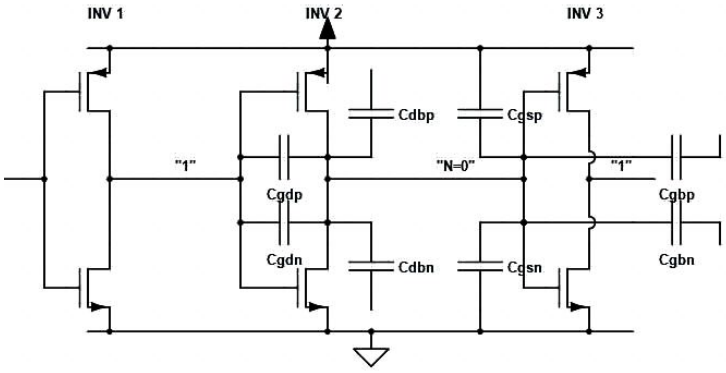

FIGURE 1.2: Device capacitance in a PDN

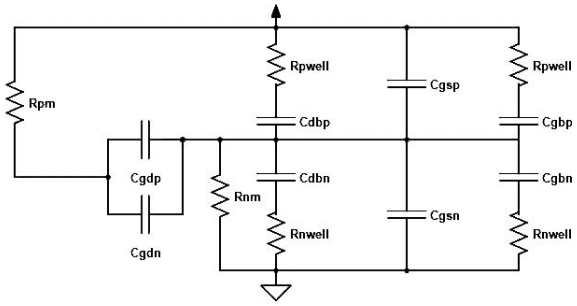

FIGURE 1.3: Equivalent RC model for the device capacitances

The intrinsic decap is not sufficient for the drop to be in safe limits. Hence, various techniques have been developed to add decap explicitly. But these extrinsic decap offers some limitations:

- Area overhead and increase in the chip's cost.
- Increase in the leakage power consumption due to increase in the gate leakage

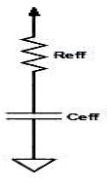

FIGURE 1.4: Approximate model for device capacitance

1.5 Undesirable effect of supply noise

- The decoupling capacitance in the on chip network along with the inductor causes the supply resonance due to the sudden change in the load currents. These sudden changes cause voltage fluctuations in the Power Distribution network and can be seen in the form of **ringing** in power supply networks.
- The power supply noise degrade the performance of the logic blocks connected by by affecting the timing of the clock signals in the switching circuits. It is observed that a small amount of fluctuations in the supply voltage can lead to timing failures and can be seen in the form of **jitter** in the supply networks.
- Due to the presence of decap at various locations, multiple resonance frequencies are seen in the supply network. The different resonance frequency are seen at the VRM level, motherboard level and the die level.

1.6 Motivation

The main aim of a designer should be to minimize the inductance, and allocate decaps to minimize the supply drop. Secondly, the second aim should be to have a maximum difference between the operating frequency and the resonant frequency of the design.
Several techniques have been developed to regulate the supply voltage. The objective of these methods is to reduce the voltage drop with aid of the modeling of a decap by increasing the amount of effective decap. A switched capacitor circuit with series and parallel configurations [10] was used to reduce to supply drop.
A linear regulator has been used to deliver currents in the case of sourcing/sinking of currents. Moreover, a shunt regulator has been incorporated which was connected to supply grid when the logic sub-circuits wake up from the sleep state.
A major portion of this work is dedicated to developing novel techniques for suppression of Ldi/dt noise using various active analog and digital techniques. Active circuits employ techniques to increase the amount of charge during the supply fluctuation. The main objective is to obtain a small drop for the same amount of decoupling capacitance.

1.7 Thesis Organization

This dissertation focuses on modeling of the decoupling capacitor in a power distribution network. It also focuses on the delay analysis for the supply variations. In the second half of the work, the circuit techniques for measurement and suppression of supply noise has been presented.
In chapter 2, the modeling and analysis of delay has been incorporated due to the supply variations. The chapter 3 describes an analog technique for modeling a decap using operational amplifier and miller technique. In chapter 4, two digital techniques have been proposed for analyzing the supply drop variations. Finally the thesis concludes with chapter 5 consisting of conclusions and future work.

Chapter 2

ANALYSIS OF SUPPLY NOISE INDUCED DELAY VARIATIONS

2.1 Introduction

Delay analysis is recognized as a primary tool for verifying the timing of PDN. Growth in the size of the design and scaling of interconnects have led to the increase in current demand. At the same time, increase in the voltage supply levels of the circuit has increased the sensitivity of the circuit to supply induced delay variations. Furthermore, increase in the chip level design scaling and the packaging standards for semiconductor technology have led to localized supply voltage variations so that a sub-circuit at one supply level is driving another sub-circuit at different supply level.
Under such conditions, power level induced delay changes affect the circuit performance and reliability. Thus, there is a need to analyze the voltage variations due to the noise and thereby relate it to the delay variations. In this work, delay analysis has been carried out on a cascade of inverter with the varied power supply with one inverter acting as a source and other as a load.

2.2 Supply Variations in Power Delivery Network affecting the Inverter Load

A Power distribution network consists of resistive, inductive and capacitive components and is connected to a load consisting of a cascade of inverters. PDN provides noise to the incoming voltage from the voltage regulator module (VRM) to the load.

A PDN with lumped RLC with inverter load is depicted in Fig. 2.1 and the transient response of the schematic depicted in Cadence Virtuoso environment using 65nm technology is shown in Fig.2.2

It can be observed from Fig. 2.2 that the output voltage generated suffers from L(di/dt) noise and the IR drop and the resulting magnitude of the voltage suffers from 10% variations from the ideal supply and the ideal supply being 1.2V. The output switches due to the switching of the inverter load. This simulation result provides the amount of noise generated due to PDN which will affect the timing(delay) characteristics of the inverter load.

This gives an insight to the analysis of the delay in a CMOS inverter and to observe the variations of the delay due to the change in the supply voltage which will be seen in subsequent section.

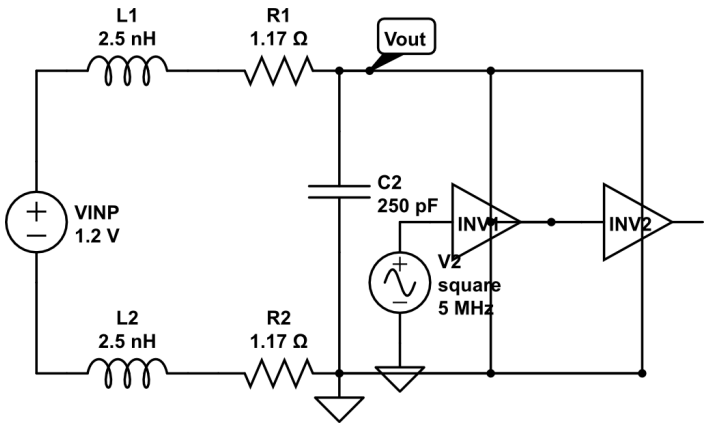

FIGURE 2.1: PDN with a cascaded Inverter Load

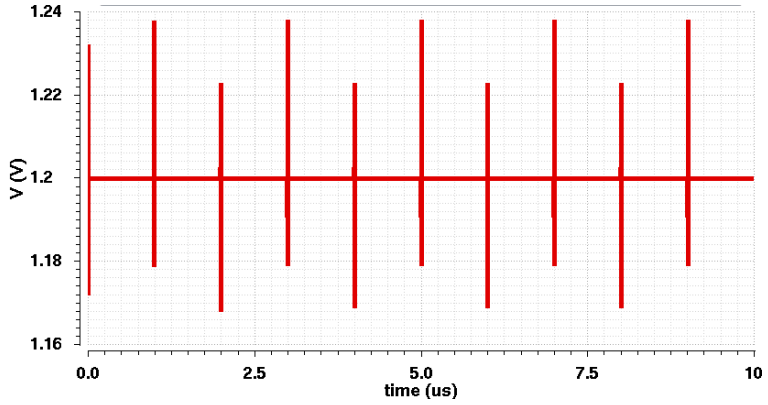

FIGURE 2.2: Output Voltage waveform under Inverter Load

2.3 Delay of a CMOS Inverter

The delay is defined as how quickly the output is affected by the input transitions. It is measured between 50% transitions from input to output. The two delays are defined as follows:

- Falling propagation delay(t_{phl})- t_{phl} defines output going from high to low.
- Rising propagation delay(tplh) defines output going from low to high.

The schematic of a simple CMOS inverter is shown in Fig. 2.3.

It is simulated with an input pulse of 1.2V with rising and falling times equal to 100psec and at a nominal supply voltage of 1.2V. The transient simulations are carried out in Cadence Virtuoso. The rising and falling propagation delay is found out to be as 49.34psec and 55.14psec respectively. Simulation parameters for the inverter are as shown in Table 2.1. There are various parameters affecting the delay of a inverter:

- Supply voltage(V_{dd})
- Circuit parameters, such as capacitive loads and fan-outs
- W/L ratio

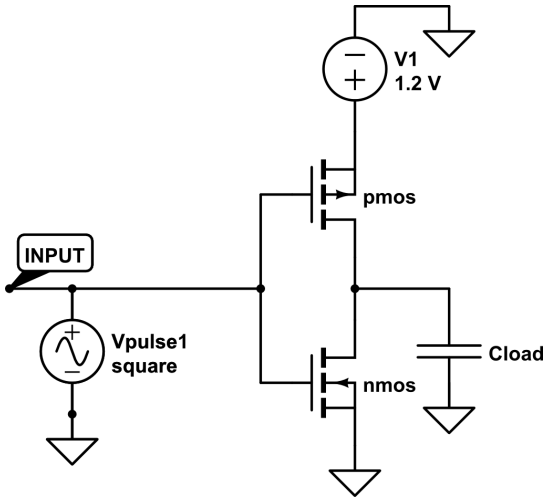

FIGURE 2.3: Simulation of CMOS Inverter

TABLE 2.1: Simulation parameters

Technology	65nm	Input	1.2V
Vdd(nominal)	1.2V	(W/L)NMOS	2
Rise time(input)	100psec	(W/L)PMOS	5.6
Fall time(input)	100pec	Load cap.	5fF

- Long channel and short channel effects in MOSFET.

2.4 Mathematical Model for Propagation Delays

1. Low to high propagation delay- Carrying out the first order analysis assuming an RC network and ignoring the channel length modulation, yields the following expression[3] for t_{plh}

.

$$t_{\text{plh}} = \frac{0.52 * C_{\text{load}} * V_{\text{dd}}}{(\frac{W}{L})_{\text{p}} * \mu_{\text{p}} * |V_{\text{dsat}}|(V_{\text{dd}} - |V_{\text{tp}}| - V_{\text{dsat}}/2)}$$

Sustituting the values of C_{load} = 5fF, V_{dd} = 1.2V, $(W/L)_p$=5.6,u_pC_{ox} = 0.00005283, V_{dsat}=0.553 and V_{tp} = 0.4813 in the above equation, we get,

$$T_{plh} = 60.37 \text{ ps}$$

TABLE 2.2: Propagation Delays

Propagation Delays		
V_{dd}(V)	T_{plh}(nsec)	T_{phl}(nsec)
1.1	59.52psec	49.8psec
1.2	49.34psec	55.14psec
1.3	40.28psec	60.34psec

The result for T_{plh} obtained by mathematic model matches approximately with the simulation results as shown in Table 2.2 with an error of 18.2%. The delay is calculated at 50% transition.

2. High to low propagation delay- Carrying out the first order analysis out assuming an RC network and ignoring the channel length modulation, yields the following expression for t_{phl}[3]

$$t_{\text{phl}} = \frac{0.52 * C_{\text{load}} * V_{\text{dd}}}{(\frac{W}{L})_{\text{n}} * \mu_{\text{p}} * |V_{\text{dsat}}|(V_{\text{dd}} - |V_{\text{tn}}| - V_{\text{dsat}}/2)}$$

Sustituting the values of C_{load} = 5fF, V_{dd} = 1.2V, $(W/L)_n$=2, u_nC_{ox} = 0.00008716, V_{dsat}=0.5V and V_{tn} = 0.409V in the above equation, we get

$$T_{plh} = 66.16 \text{ ps}$$

The result for Tphl obtained by mathematic model matches approximately with the simulation results as shown in Table 2 with an error of 16.6%. The delay is calculated at 50% transition.

2.5 Variations in Capacitive Loads for a CMOS Inverter

With the increase in the capacitive load at the output terminals, the effective time to charge up the capacitor will increase and hence the delay increases as shown in Table 2.3.

TABLE 2.3: Delay values for various capacitive loads

Capacitive load(C_{load})	T_{plh}	T_{phl}
1pF	5.018	6.336
2pF	10.01	12.65
4pF	20.01	25.27
8pF	40.00	50.52
16pF	79.97	101
32pF	159.8	202
64pF	284.1	402.3

The linear plot for the delay vs propagation delay is summarized in Fig. 2.4.

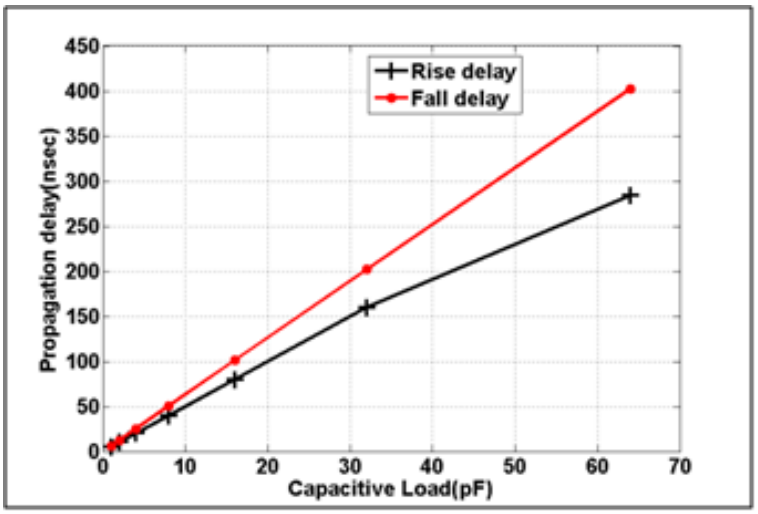

FIGURE 2.4: Propagation delay vs Capacitive load

Observations:
Low to High propagation delay(T_{plh}): It can be seen from Table 2.2 that the t_{plh} reduces with the increase in the supply voltage(V_{dd}). With the increase in V_{dd}, the amount of current increases, and hence the time taken to charge the capacitive load decreases and therefore the delay reduces. By the equation of charge,

$$Q = CV$$

$$I * \tau = CV$$

$$\tau = CV/I$$

Keeping capacitive load as constant,

For V_{dd}=1.2V, I= 128uA

For V_{dd}=1.3V, I=167.5uA

Which shows that delay time τ reduces with increase in current. The variation in the current corresponding to two voltages is about 30.8% which corresponds to 22% variation in the low to high propagation delays at two supply voltages.

High to Low propagation delay(t_{phl}): It can be seen from Table 2.2 that the t_{phl} increases with the increase in the supply voltage(V_{dd}). This is due to the net increase in the charge as the voltage changes from 1.2 to 1.3 V.

$$Q_1 = C_1V_1 = C_2V_2$$

So for the same amount of capacitive load, the charge stored in the capacitor is higher for higher voltage.

$$Q_{2(1.2V)} = CV_1$$

$$Q_{2(1.3V)} = CV_2$$

At V_{dd} = 1.2V

$$Q_1 = 1.2 * 5 = 6fC$$

$$Q_2 = 0.6 * 5 = 3fC$$

$$Q_2 - Q_1 = 3fC$$

At V_{dd} = 1.3V

$$Q_1 = 1.2 * 5 = 6fC$$

$$Q_2 = 0.6 * 4.6 = 2.76fC$$

$$Q_2 - Q_1 = 3.24fC$$

Hence, there is a net increase in the charge from (6-3)= 3fC to (6-2.76)= 3.24fC.
Now, from the equation of delay,

$$\tau = \frac{\Delta Q}{I}$$

$$\tau = \frac{Q_2 - Q_1}{I}$$

Which shows that the delay increases with increase in charge, and hence t_{phl} increase with increase in V_{dd}. The delay is directly proportional to the change in the charge. The change in the charge, ΔQ at 1.3V with respect to at 1.2V vary by 8% corresponding to the 9.4% variation in the delay at the two supply voltages(Table 2.2).

2.6 Cascade of Two Inverters

The delay analysis can be extended to a cascade of inverters where one inverter acts as a source and another inverter acts as a load. The variations in supply voltage of both the inverters affect the rising and falling propagation delays. With the increase in Vdd the rising propagation delay reduces. The increase in the current due to increase in the supply voltage leads to the charging of the capacitive load at early times, thereby reducing the delay. On the other hand, the falling propagation delay increases. The Tphl and Tplh values have been shown in Table 4 for different values of Vdd. The nominal voltage is 1.2V with variations of Vddmin of 1.1V and Vddmax of 1.3V.

The schematic for the variations in Vdd is as shown in Fig. 2.5.
Vdd1 and Vdd2 represent the supply voltages for Inverter 1 and Inverter 2 respec-

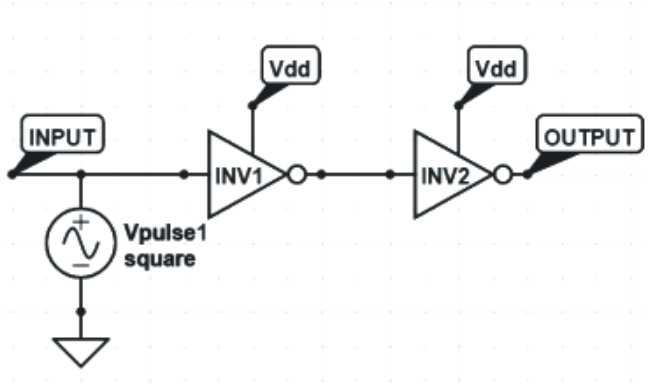

FIGURE 2.5: Simulation of cascaded Inverter

tively. The table shows the simulation results of the cascade of two inverters and the delay for low to high and high to low transition are as shown:

TABLE 2.4: where Tphl1- High to low delay for 1st inverter; Tplh2- Low to high delay for 2nd inverter; Tplh-low to high delay for the cascaded inverters.

T_{plh}			
$V_{dd1}=V_{dd2}$(V)	T_{phl1}(nsec)	T_{plh2}(nsec)	T_{plh}(psec)=$T_{phl1}+T_{plh2}$
1.1	16	38.67	54.67
1.2	19.43	35.63	55.06
1.3	23.34	29.05	52.39

TABLE 2.5: where T_{plh1} - Low to high delay for 1st inverter; T_{phl2}-High to low delay for 2nd inverter; T_{phl}-High to low delay for the cascaded inverters.

T_{phl}			
$V_{dd1}=V_{dd2}$(V)	T_{plh1}(nsec)	T_{phl2}(nsec)	T_{phl}(psec)=$T_{plh1}+T_{phl2}$
1.1	27.02	42.02	69.04
1.2	18.97	43.16	62.12
1.3	11.52	44.29	55.81

As we can see from Table 2.4 and Table 2.5 , The low to high propagation delay remains nearly constant for the change in the supply voltage. But the high to low propagation delay has variations of 19% approximately from the nominal delay value.

Observations: Assuming the voltage drop in the power supply network to be restricted and to be 20% of the nominal supply voltage(1.2V), the rise and fall delays characteristic plots as a percentage of Vdd are as shown in Fig. 6. It can be observed that the two plots have a different slope and hence different variation patterns as observed by simulation in Table 2.4 and Table 2.5 Owing to the different slopes for

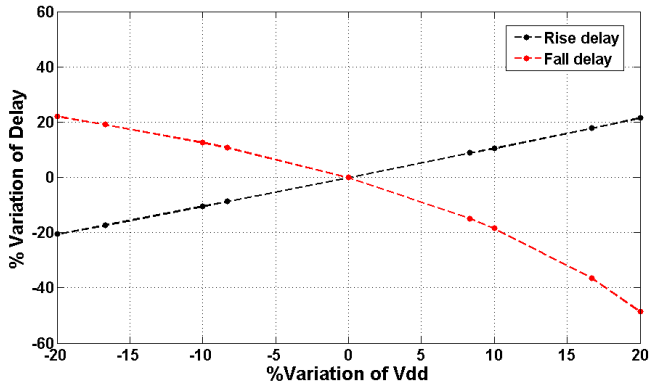

FIGURE 2.6: Variation of rise/fall propagation delays of a gate with respect to V_{dd}

the two delays, the reduction of the variations is a critical task[9]. Hence, these variations have to be minimized in order to have a robust power distribution network. In order to minimize the variations, two techniques have been proposed in the next section

Chapter 3

SUPPLY NOISE SUPPRESSION-ANALOG TECHNIQUE

3.1 Introduction

A Power Distribution Network comprising of the resistive, inductive and capacitive components is modeled for the suppression of noise. The inverter load is replaced with the equivalent switching current source load. The inductive drop (Ldi/dt) caused due to large switching currents constitute a dominant portion of the noise in the circuit. This noise creates variations in the power supply coming from VRM and affects the operation of the circuit. So, this noise has to be minimized for reducing the variations in power supply. The first method is to employ a decoupling capacitor in the circuit known as passive decaps at various locations in the die. This decap acts as a local charge storage and reduces the voltage drop at the supply points. On the other hand, these passive decaps provide more area overhead and increase the power consumption. Over the years, the MIM decoupling capacitors were added onto the die.They occupy less area and consume less power. But they require extra processing and have low capacitance to area efficiency. So, the explicitly added decaps are referred to as passive(extrinsic) decap.
Further active decaps have been used in the recent work to increase the amount of the charge in the power supply network due to voltage variations. The main aim of using the active decaps was to have the lesser supply drop for the same amount of explicitly added decap.

3.2 Proposed Active Circuit

In this work, we have proposed an analog active decap technique to mitigate the Ldi/dt drop in a PDN. The active circuit amplifies the voltage drop in the supply and ground lines of a PDN. This amplified and inverted supply drop is then applied to a decap terminal. This pumps more charge into the PDN as compared to passive decaps.

3.2.1 Power Delivery Network with Passive Decap

A power delivery network consists of parasitic resistances, lumped inductors, and passive decaps as depicted in Fig. 3.1. The lumped inductors denote the inductance attributed to the supply network in the dies and packages whereas resistors model the resistive parasitic in the circuit.

I_{die} is the current drawn from the supply network by the switching devices connected. The time varying current I(t) produces a transient voltage drop across the

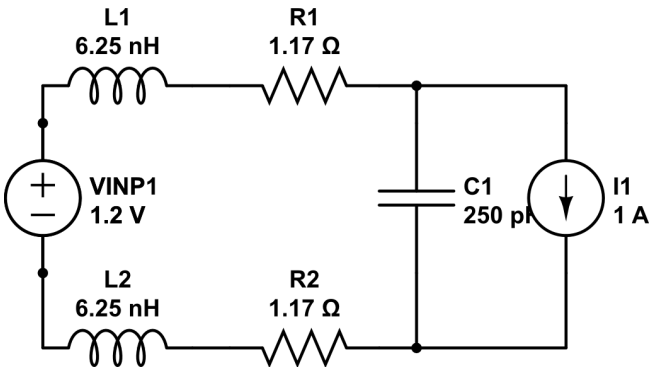

FIGURE 3.1: Power Distribution Network with Passive decap

die. The decap sees a potential difference across its two terminals and provides charge to both ground and power planes. The current provided by decaps is given by

$$I_{\mathrm{Cd}}(t) = 2C_{\mathrm{d}}.\frac{d}{dt}\Delta V(t) \tag{3.1}$$

where C_{d} is the value of decap and $\Delta V(t)$is the transient voltage drop. The voltage drop is given by :

$$\Delta V(t) = I(t).R + Ldi/dt$$

It can be observed from the equations that the voltage drop reduces as the amount of decap increases. The resonant frequency due to the inductance and decaps is given by:

$$\omega_{\mathrm{r}} = \frac{1}{\sqrt{LC}}$$

As the value of on die decap increases, the resonant frequency and the noise peak reduces.

Observations: The frequency domain analysis has been carried out and the voltage drop is depicted as shown in Fig. 3.2. The resonant frequency of the grid due to package inductance with passive on-die decaps is observed to be 5.81MHz.

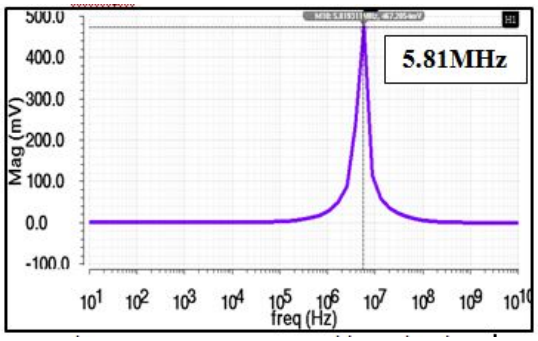

FIGURE 3.2: Frequency Response with Passive decap

3.2.2 Active Decap Circuit

The active decap circuit is composed of two operational amplifiers which amplify and invert the voltage drop across the V_{dd} and V_{ss} of the supply network. The total decap is divided among the power and ground lines of the PDN. The two opamps drive one terminal of each decap as shown in Fig. 3.3. The opamps operate on a

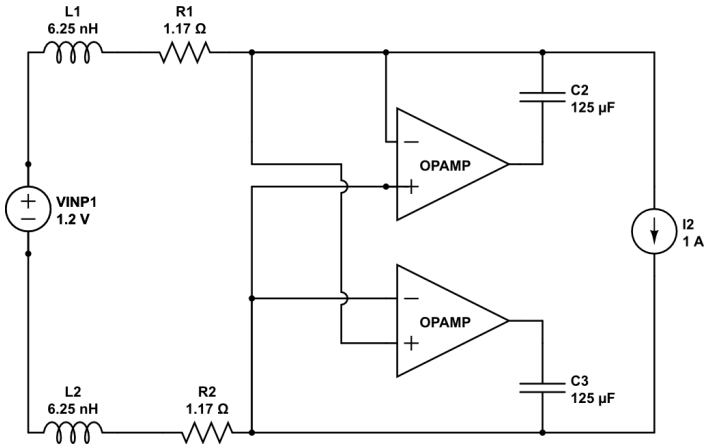

FIGURE 3.3: Proposed Active Decoupling Capacitor circuit

separate(active) supply and that supply is ideal and does not affect the gain of the opamps.
The voltage drop $\Delta V(t)$ is amplified to a voltage of $2A\Delta V(t)$ and $-2A\Delta V(t)$ by two opamps. Therefore, two decaps undergo a potential difference of $(2A+1)\Delta V(t)$.The current as seen through the two decoupling capacitors is:

$$I(t) = (2A+1)\frac{C_{\mathrm{d}}}{2}\frac{d\Delta V(t)}{dt} \tag{3.2}$$

From the above equation, we can observe that the active decaps provides more current as compared to Eq. 3.1 if the gain is higher. The effective amount of decap as seen through the circuit is

$$C_{\mathrm{eff}} = (2A+1)\frac{C_{\mathrm{d}}}{2} \tag{3.3}$$

where, C_{eff} is the amount of decap and A is the gain of opamps.

3.2.3 Opamp Design

The gain of an opamp is a function of frequency and reduces as the frequency is increased. Hence the net effective capacitance decreases as the frequency increases. The operational amplifier should be designed in such a way that the gain of the amplifier should be as high as possible to reduce the impedance. The bandwidth of the opamp should also be high to suppress the Ldi/dt noise.
The opamp can drive large currents to drive the large decaps. The opamp consists of three stages.:

- The first stage consists of a level shifter stage to bring the inputs to the common mode voltages of V_{dd} and V_{ss}.

- The gain stage constitutes the second stage of the opamp. This stage is composed of a differential amplifier.
- Further a buffer used for providing high drive strength is connected after the gain stage.

Figure 3.4 shows the schematic of opamp which is connected to the terminal of a decap.
The O/P's from the level shifter are applied to two inputs of opamp V1 and V2. Then comes the single ended differential amplifier formed by transistors M3 and M4. Transistor M1 and M2 are active current mirror loads and M6 provides the biasing current.The differential amp is followed by an O/P stage comprising of M7 and M8 to provide high drive capability to the opamp.

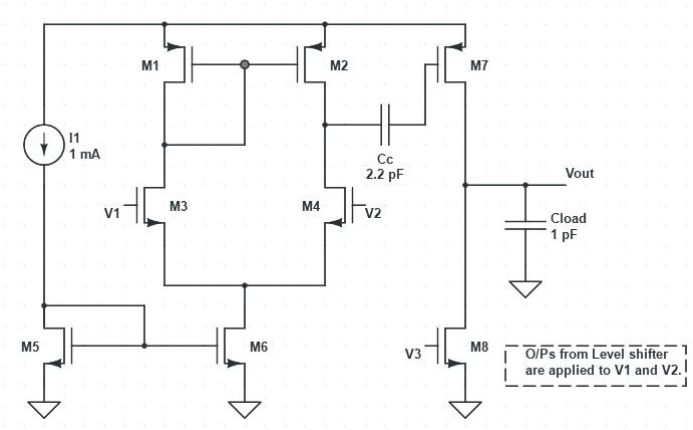

FIGURE 3.4: Schematic of Op-amp

The gain of the opamp can be given by :

$$A = \frac{A_o}{1 + j\frac{\omega}{\omega_o}} \tag{3.4}$$

where A is the gain of opamps and ω_o being the dominant pole. The opamp is simulated in 65nm technology in Cadence Virtuoso. The supply voltage is taken as 1.2V.

The active circuit is simulated with a decap connected through a negative feedback to the opamp. The effective capacitance increases resulting in less voltage drop across the output terminals as shown in equation 3.1. The circuit has a pulse-type drive current across the output terminals which acts as the load current.

3.2.4 Simulation Results

The active circuit is simulated in the Cadence Virtuoso environment. It is designed with 65nm technology with the supply of 1.2V. The total amount of decap is 250pF for both passive and active simulations. All the sub-circuits used in the active circuit are simulated in the same environment and the simulation results are discussed in the following sections.

3.2.5 Opamp Simulations

Figure 3.5 shows the simulation gain of the opamp as the function of frequency. The gain of the operational amplifier is found to be 40dB. The 3-dB bandwidth is found to be 4MHz. The phase margin is calculated as 98 degrees.

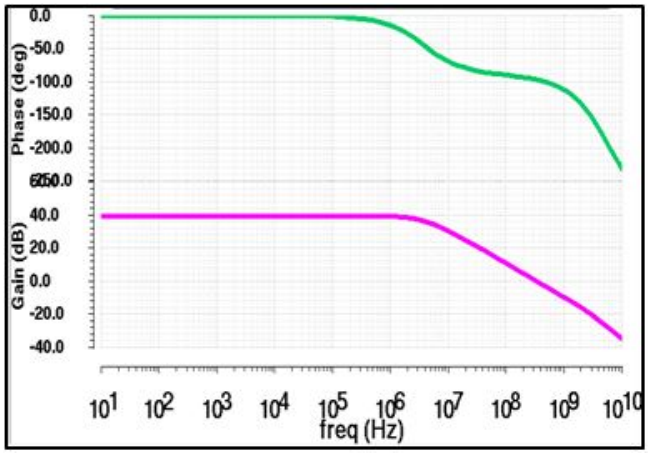

FIGURE 3.5: Voltage gain and phase plot for OPAMP

3.2.6 Active circuit simulations

The load in the circuit is modeled as a current source. The transient profile of the current source is as shown in Figure 3.6 .

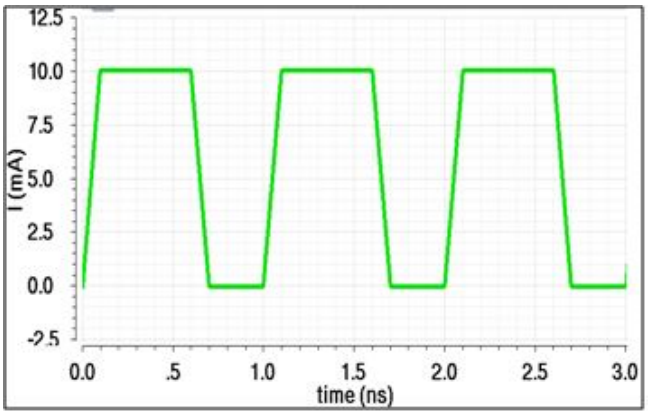

FIGURE 3.6: Current profile wrt time

The current profile is a ramp pulse of magnitude 10mA. The frequency domain analysis is carried out and the output is shown as in Fig.3.7. The resonance occurs at around 4MHz.
The voltage profiles are plotted as shown in Fig.3.8. From the voltage profile, it can

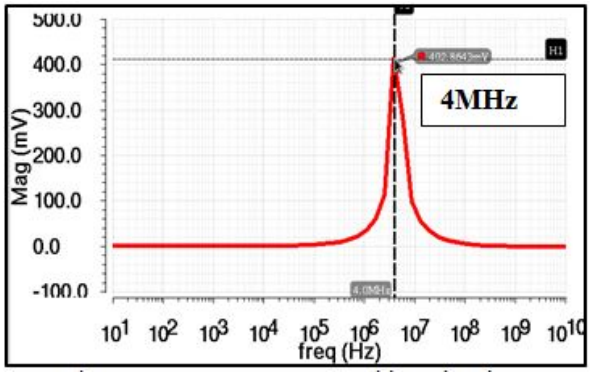

FIGURE 3.7: Frequency response with active decap

be concluded that the voltage drop is around 348mV as seen across output terminals as compared to 403mV in the case of passive decap which shows an effective decap of 10nF in the case of the active circuit.

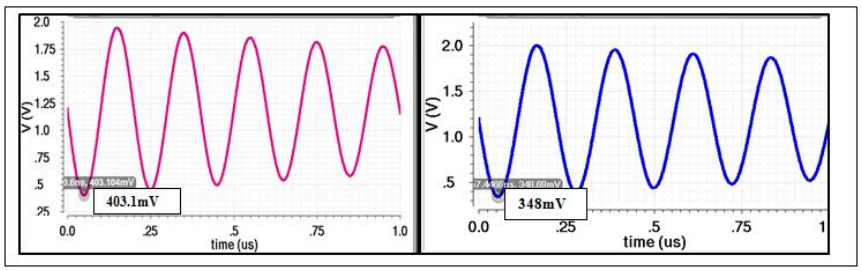

FIGURE 3.8: Voltage profiles for passive and active decap

It can be concluded from the above analysis that the active circuit produces less voltage drop across the output because of the increase in the value of effective decap.

Furthermore, the resonant frequency is a function of gain. In the active circuit, the presence of large gain lowers the resonant frequency. The resonant frequency is lowered to 4MHz for the active circuit from 5.8MHz in case of passive circuit.

It finally shows that the active circuit mitigates the Ldi/dt noise and lowers the resonant frequency. Using this proposed method, the supply drop is reduced by 20% corresponding to an increase in the effective decap.

Chapter 4

DIGITAL CIRCUIT-TECHNIQUES FOR INDUCTIVE SUPPLY-NOISE SUPPRESSION

4.1 Introduction

Due to the increase in the scaling of transistors and their clock frequencies, the power distribution network suffers from increased Ldi/dt drop. The passive decaps (lumped capacitor) were used to reduce the inductive drop but they proved disadvantageous due to the large area and leakage overhead. Moreover, the analog active decap technique explained in the previous chapter suffers from various limitations.

1. The analog active technique makes use of an operational amplifier to amplify the supply noise and transfer charge from the decaps. The efficiency of circuit depends on the bandwidth and the gain characteristics of the operational amplifier.

2. As we know, The gain of the opamp is a function of operating frequency and it drops after a certain frequency. The reduction in the gain reduces the efficacy of the amplifier and reduces the effective decap of the circuit.

3. Moreover, the scaling of the supply voltage with the technology leads to the difficulty in designing the high gain single stage amplifiers. Increasing the stages leads to increase in the amplification delay which affects the stability of the circuit at high frequencies.

Due to the above mentioned reasons, the digital techniques have been proposed for supply noise reduction.

4.2 Digital Technique 1- Sleep Transistor Sizing for Resonant Supply Noise Damping

Power supply noise is a major issue in power distribution networks. The sudden demand in the current also leads to increase in the resonance thus affecting the reliability and timing of a circuit. The large on die decaps were used traditionally to lower the impedance over a range of frequencies.But these decoupling capacitors produce leakage in the gate terminal of the scaled devices. One of the methods to reduce the supply drop in the PDN is to make use of sleep transistors[8]. The sleep transistors lead to the addition of additional resistance in the circuit which is effective in dampening the resonance.

4.2.1 Principle of the Sleep transistor technique

A sleep transistor can operate in the active(linear) region. The current through an NMOS transistor can be expressed as

$$I_{\text{circuit}} \approx \mu_{\text{eff}} C_{\text{ox}} \frac{W}{L} (V_{\text{dd}} - V_{\text{t}}) V_{\text{VGND}}$$

where, μ_{eff} is mobility of the carrier, C_{ox} is oxide capacitance, V_{t} is threshold voltage and V_{VGND} is the virtual ground voltage.

The sizing of the sleep transistor is related to the circuit current and ground current as follows:

$$\frac{W}{L} \propto \frac{I_{\text{circuit}}}{V_{\text{VGND}}}$$

It can be observed from the above equation that a large sleep transistor(having a large W/L ratio) offers less resistance and ground offset. As we know, The supply noise is caused by the resonance between the inductance and on die capacitance, the supply noise increases with a large sleep transistor due to the reduced damping effect. So, a small sleep transistor should be used to reduce the supply noise.

4.2.2 Sleep Transistor Sizing and Resonance Supply Noise

A model of the power distribution network with the sleep transistors is depicted in Fig.4.1 which consists of package inductance, resistance and on chip and circuit capacitance. The PDN drives the current load resulting from different load circuits. The following circuit has been simulated with two sleep transistor widths i.e footer/header with transistor widths as 500μm,200μm and 1000μm,400μm. The simulations are carried out with the following parameters as shown in Table 4.1. The impedance vs frequency plots is shown in Fig 4.2 and 4.3. which denotes that the supply noise is directly proportional to supply frequency.

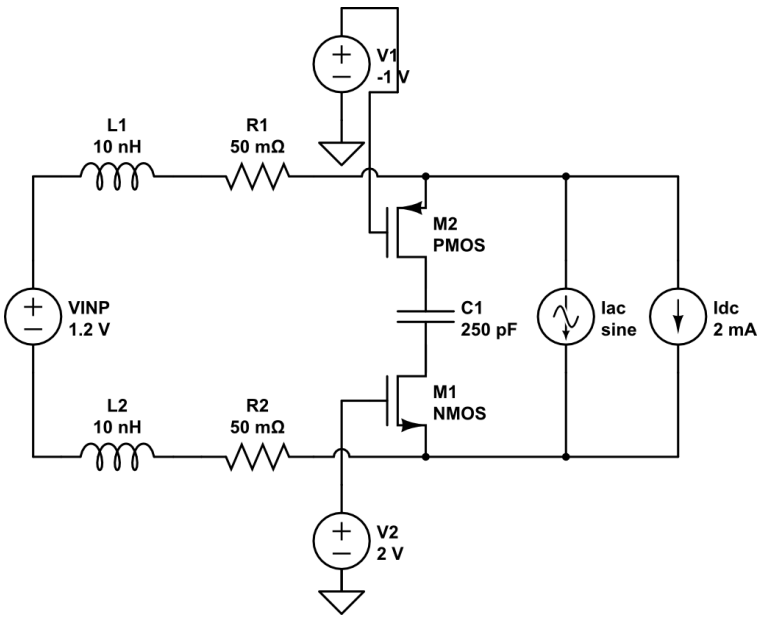

FIGURE 4.1: Schematic of sleep transistor technique

TABLE 4.1: Simulation parameters

Technology	65nm	C_{decap}	250pF
L	20nH	R_{wire}	10m/ohm
I_{DC}	2mA	I_{AC}	1mA
$Freq_{res}$	208MHz	V/textsubscriptdd	1.2V

OBSERVATIONS:

From the frequency plots for different transistor sizes shown in Figure 4.2 and 4.3, it can be inferred that :

- The frequency supply noise increases for small sleep transistors.
- The resonant peak decreases for small sleep transistors

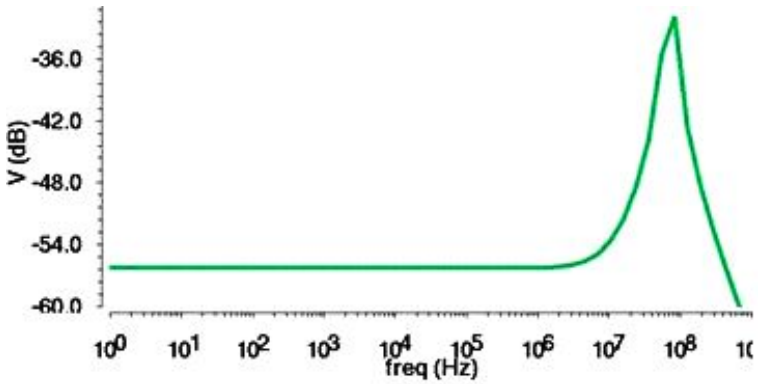

FIGURE 4.2: Frequency spectrum of supply noise with large transistor widths

The impedance associated with the network is characterized as the series combination of R and L in parallel with the decap. The resistance and inductance determine the total impedance at low frequencies and as frequency reaches the resonant frequency, the capacitance dominates the impedance. Therefore at high frequencies, changing the resistance doesn't affect the total noise.

Thus for analyzing the sleep transistor technique, the major focus is on the two

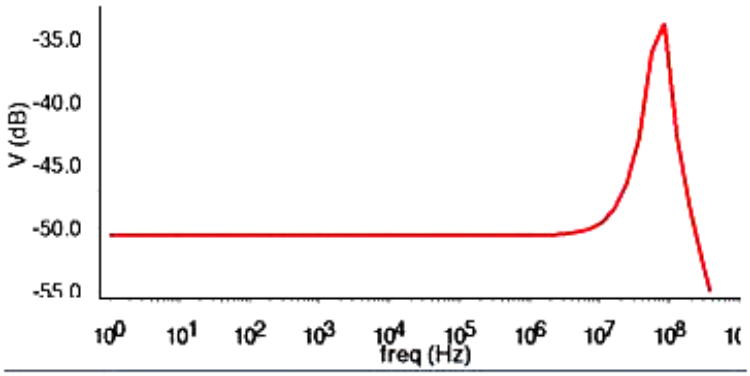

FIGURE 4.3: Frequency spectrum of supply noise with small transistor widths

major noise components- resonant supply noise and DC supply noise. From the frequency plots, it can be seen that, Smaller sleep transistor reduces the resonant noise peak by 1.3dB compared to the large sleep transistor due to the additional damping provided by the increased resistance.

The smaller sleep transistors offer various advantages. First is the less area overhead due to the small size. Second is the better leakage reduction capability as the virtual rails will collapse more with weak sleep transistors.

4.2.3 Demerits of the sleep transistor method

1. It can be seen that the small sleep transistor reduces the resonant noise in the case when resonant noise is dominating. But the resonant noise is quite random in nature and occurs when a current component occurs near resonating frequency.

2. Small sleep transistors are used in case of circuits during the resonance and large sleep transistors can be used in the circuits where IR supply noise is more prominent.

3. The above technique delivers only limited charge and does not have undershoot/overshoot detectors.

   Hence there has to be a technique which detects the resonance and can eliminate the IR drop penalty during the anti resonance periods.

4.3 Digital Technique 2: Charge injection based active decoupling circuit

To overcome the problems faced in the sleep transistor method, A new digital technique has been developed to detect the suppress the overshoots and undershoots due to the sudden increase in the supply transients. The charge injection based active decoupling circuit consists of an active decap bank C_a and a nominal active supply V_{dd}. The capacitor C_a acts as a passive capacitor when the supply voltage is within safe limits. The simplified model of a conventional power distribution network is shown in Fig. The impedance of the network is shown in terms of Inductance L and Resistance R.The lumped capacitance in the network represents the total switching and non switching decap. The current source represents the switching currents of all the blocks in the chip.

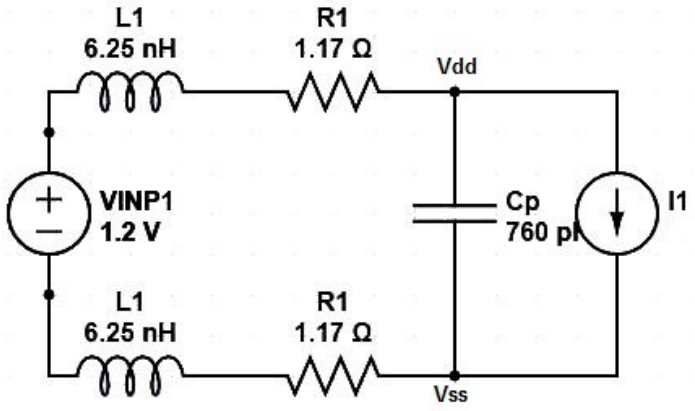

FIGURE 4.4: A power delivery model- Unregulated technique

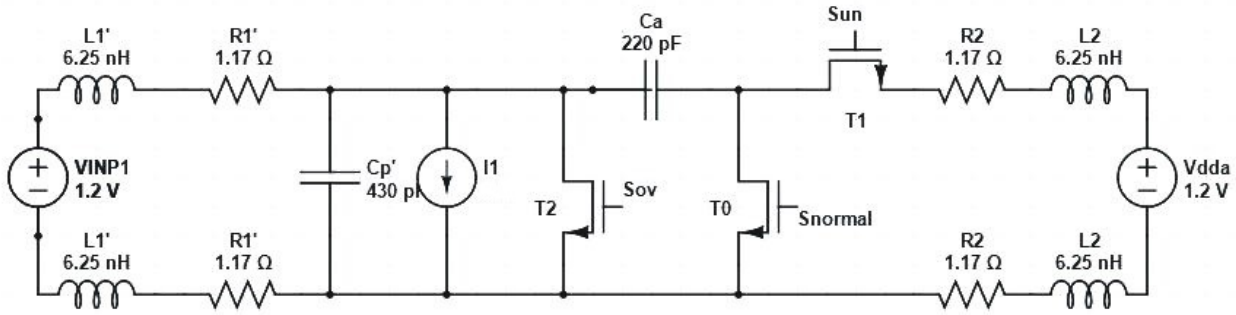

FIGURE 4.5: Proposed Technique- Regulated technique

The schematic for charge injection technique is as shown in Fig. 4.5 The total pads available for Vdd in the simplified model is allocated to Vdd_a in the proposed model so that number of supply pads remain constant.

$$N1_{\text{Vdd}}.L1_{\text{Vdd}} = N1_{\text{Vdd}}.L1'_{\text{Vdd}} + N2_{\text{Vdd}}.L2_{\text{Vdd}}$$

where $N1_{\text{Vdd}}$ and $N2_{\text{Vdd}}$ denote the number of pads for Vdd and Vdd_a, $L1_{\text{Vdd}}$ and $L2_{\text{Vdd}}$ are the inductances of Vdd and Vdd_a respectively. Moreover,

$$C'_{\text{p}} = C_{\text{p}} + C_{\text{a}} + \Delta A$$

where ΔA is the area overhead of the circuit.

TABLE 4.2: Decap Allocation

Decap Allocation				
Test Case	Passive(C_p)	Active(C_a)	VDD_a Decap	Total Decap
Unregulated	760pF	0	-	760pF
Regulated	430pF	220pF	90pF	740pF

4.3.1 Working of the proposed circuit

The analysis of the PDN circuit gives us the two limits on the power supply- one for the undershoot and another for the overshoot. C_a is connected between power and ground rails and behaves as a normal passive decap when the supply voltage is withing the voltage limits. There are 3 modes of operation as explained:

1. Normal operation- C_a acts as the passive decap when the supply voltage is within safe limits.
2. Undershoot operation- When the supply drop below a certain limit is detected , transistor T_o in Fig. is turned off and T1 charges up the negative terminal of C_a from 0 to Vdd_a and the charge equivalent to $C_aVdd_a$is injected into the network.
3. Overshoot operation- During the overshoot, shunt load T2 is turned on and simultaneously To is also on thereby charging C_a.Therefore the excess charge goes to the remaining section of the network.

4.3.2 Supply noise undershoot and overshoot detection

For proper and fastest overshoot and undershoot detection, the detection speed is one of the major concern. Analog techniques are slow and consume a large amount of current. So, a digital technique is proposed with a lesser response time.

- Firstly, a ring oscillator is used to generate a 5.6 GHz clock. Then, the Supply voltage is sampled at the rising edge of the clock
- Secondly, two clocked comparators have been used to sample the noise at high frequencies for both undershoot and overshoot detection.
- A level shifter is used to convert the supply noise to a common mode voltage i.e. V_{ref} of 600mV. The translated waveforms are then fed as the inputs to the clocked comparator. The delay of the comparator is found to be 115psec. In the comparator, transistors M1 and M2 are skewed to create a switching threshold.

- Output from the comparator used for undershoot and overshoot detection gives the undershoot signal, S_{un} and overshoot signal S_{ov} and if inverted gives the S_{normal}

4.3.3 Design of a Ring Oscillator and V_{dd}/V_{ss} level shifter

A Ring Oscillator is a cascade combination of a chain of inverters forming a closed loop[3]. A ring oscillator provides multi-phase outputs because of its basic structure. The frequency of an RO depends on the number of stages and the propagation delay per stage. The schematic of a 7 stage ring oscillator generating 6 phases(p1-p6) is as shown in Figure 4.6. The frequency of RO is approximately 5.6 GHz. The first phase output from the RO is fed as the latch input to the comparator. The supply voltage

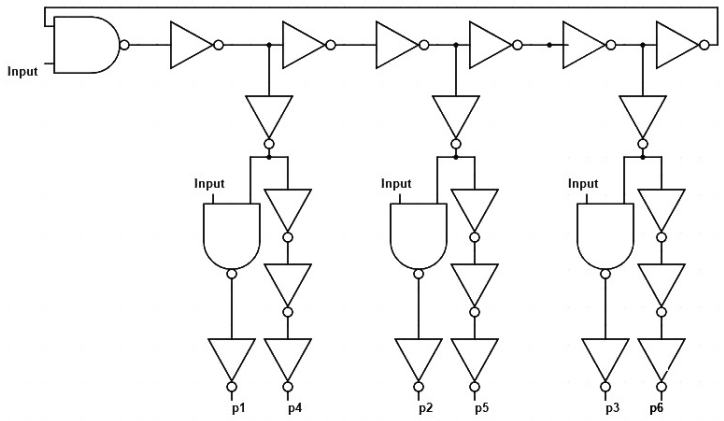

FIGURE 4.6: Ring Oscillator

is brought to a common mode voltage level with the help of V_{dd}-V_{ss} level shifter as shown in Figure 4.7. The common mode reference voltage is around 600mV. The RC time constant is 1ns.The two translated voltages V+ and V- are generated and fed as inputs to the latched comparator.

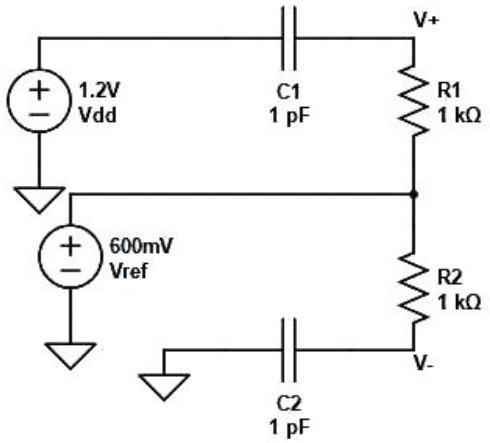

FIGURE 4.7: V_{dd}/V_{ss} level shifter

4.3.4 Design of a CMOS latched Comparator

A latched comparator is an essential circuit in all VLSI architectures. The digital technique makes use of a latched comparator which works synchronously with the clock signal to generate a digital signal[1]. This comparator uses a positive feedback to convert an analog signal into a digital output. The schematic of the comparator is as shown in Figure 4.8

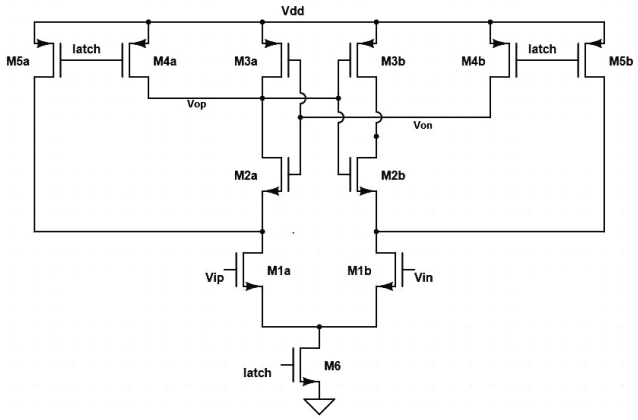

FIGURE 4.8: Latched Comparator Schematic

The Comparator works in two phases:

- The reset phase: when the latch is low, the transistor M_{4a} and M_{5a} forces the O/P nodes and the drains of differential transistors (M_{1a}/M_{1b}) to V_{dd}. The transistor M_6 is off and no current exists.
- The regeneration phase: When the latch goes high, the reset transistors become off, the current starts flowing in the differential transistors and M_6. After the input is applied, one of the cross coupled inverters that make the regeneration, M_{2a}/M_{3a} and M_{2b}/M_{3b} has more current and the final state is achieved. Figure depicts the schematic for a latched comparator which is used in the active technique

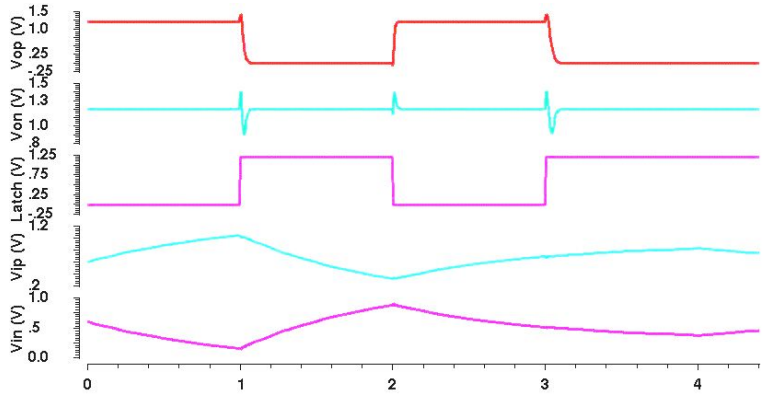

FIGURE 4.9: Output of Comparator

After the regeneration stage, one output is at V_{dd} and the other at 0V. The output is as shown in Figure 4.9. The delay of the comparator is found to be around 115psec.The above explanation is for undershoot comparator. The working for overshoot comparator can be done on same principle described above and has been omitted for simplicity.

The outputs from comparator is fed to series of inverters to generate the respective signals for detecting the overshoot, undershoot and normal operation as shown in Figure 4.9. The time delay for generation of these control signals is found to be 400psec.

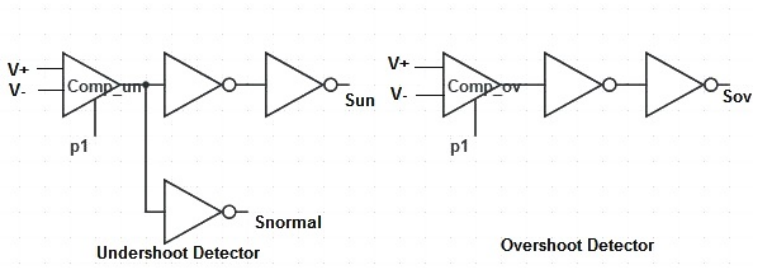

FIGURE 4.10: Generation of normal, undershoot and overshoot signals

The output from the undershoot and overshoot detector is sent to the switches connected in the active circuit for detecting the change in the supply. The switches operate as shown in Table 4.3.

TABLE 4.3: Modes of operation for charge injection technique

Modes of Operation		
Undershoot Operation	Normal operation	Overshoot Operation
S_{ov}=0, S_{un}=1, S_{norm}=0	S_{ov}=0, S_{un}=0, S_{norm} =1	S_{ov}=1, S_{un}=0, S_{norm}=1

4.3.5 Simulation Results

Figure 7.2 shows the regulated and unregulated supply waveforms with respect to time.

This graph depicts the variation in the supply noise and the safe margins associated

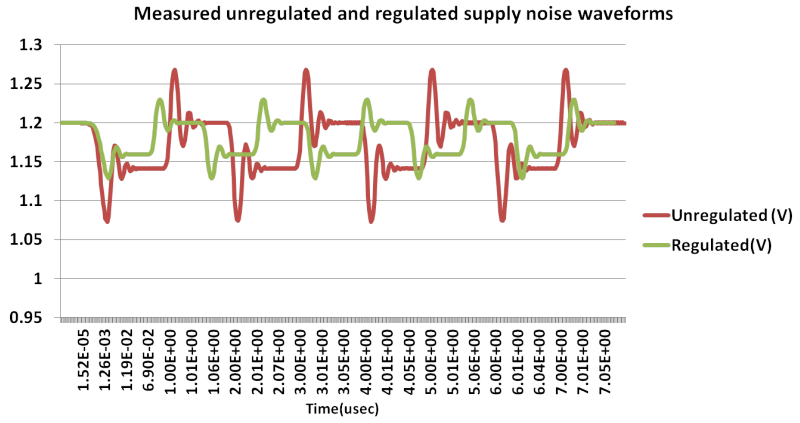

FIGURE 4.11: Simulated unregulated and regulated supply waveforms

with the supply.

The two threshold voltages V_H and V_L for overshoot and undershoot detection respectively can be seen as 1.24V and 1.13V respectively.

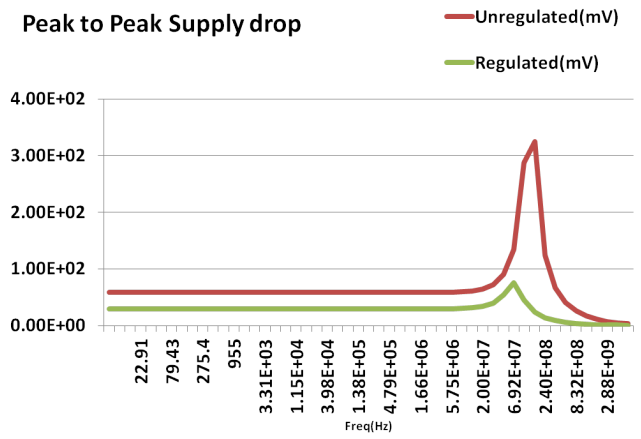

FIGURE 4.12: Frequency Response for unregulated and regulated technique

It can be observed that, the regulated supply waveform has reduced variations in supply voltage as well as less overshoot and undershoot levels.

Figure 4.10 shows the frequency response of the supply drop with and without the regulation. The regulated supply drop is less than the unregulated one by approximately 75%. The resonant frequency has also been reduced from 241.7 MHz to 101.01 MHz.

The measurements regarding the different load currents of peak magnitudes varying from 10mA to 60 mA have been done and are shown in Figure 4.11.

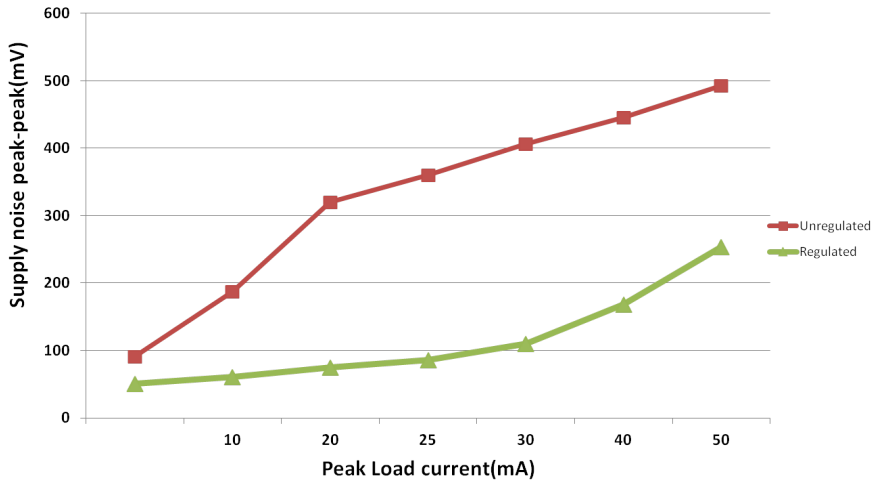

FIGURE 4.13: Measured unregulated and regulated peak-to-peak supply noise for varying peak load-currents

It can be observed from the curve, at lower currents the supply drop is within safety limit of 100mV, but as the load current increases, the active circuit has to inject more charge for the increased drop which results in less drop and improved performance. The best improvement of 75% is seen in the case of 25mA.

Advantages of this method are as follows:

- Occupy less area: The comparator, level shifters and ring oscillators and switches contribute to the active area. They occupy less area as compared to a lumped passive decap used.
- It has less overhead of any instability unlike that of the analog technique.
- Less wastage of power resources as the circuit functions whenever there is an undershoot/overshoot.

Chapter 5

CONCLUSIONS AND FUTURE WORK

The following chapter gives the overall summary of the thesis work and the possible future developments which can be carried out in the due course of research.

5.1 Conclusion

This work highlights the importance of replacing the passive(lumped) decoupling capacitor with the active circuit techniques to overcome the area overhead and timing issues related to the circuit. The two techniques have been explained and carried out: The analog and digital active decoupling capacitance techniques have been extensively simulated with various load currents which show much better and enhanced results in terms of less peak to peak supply noise and increased percentage improvement. The analog technique makes use of opamps to increase the effective value of capacitance and shows an improvement of approximately 20% in suppressing the peak to peak supply noise. Further, The two digital techniques ave been proposed i.e the sleep transistor technique and the charge injection technique. The charge injection technique shows an improvement of approximately 75% in the reduction of supply noise. Moreover, the delay analysis has been taken into account to highlight the effect of the variation in delay and timing characteristics of a circuit due to variations in power supply. As the propagation delay is an important factor in determining the robustness of PDN, this factor needs to be addressed and therefore, effective circuit techniques have been proposed to minimize the supply variations and in turn will lead to less timing violations in a circuit.

5.2 Future work

The following section lists some of the future challenges of this work. The proposed digital technique can be implemented in the real environments involving the use of analog pads, boards, chip and oscilloscope for supply noise measurement, Moreover, the technique can be automated to detect the supply noise overshoot and undershoot switches thus making the operation more reliable and easy to operate. Secondly, as the frequency of operation is increasing from few hertz to GHz, and the complexity of the circuits and microprocessors is also increasing, there is a need to integrate multiple processors in a core and build multi core designs to improve power efficiency. Moreover, there will be a need to develop efficient algorithms for supply analysis on a large scale in an extensive power grid.

Chapter 6

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