High Resolution Low Power Discrete-Time Sigma-Delta ADC with Input Offset Compensation Technique

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Submitted in partial fulfillment of the requirements for the Degree of M.Tech. in Electronics and Communication, with specialization in VLSI and Embedded Systems

Certificate

This is to certify that the thesis titled **"High Resolution Low Power Discrete-Time Sigma-Delta ADC with Input Offset Compensation Technique."** submitted by **Shivam Kalla** for the partial fulfillment of the requirements for the degree of *Master of Technology* in *VLSI & Embedded Systems* is a record of the bonafide work carried out by him under my guidance and supervision in the ADC design Group at ST Microelectronics, Greater Noida. This work has not been submitted anywhere else for the reward of any other degree.

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Abstract

Audio applications necessitate precise data conversion from analog to digital domain. This high resolution conversion can be achieved by using Sigma-Delta architecture, which operates at over-sampling rate and exhibits noise-shaping characteristics. The intent of this thesis involves design of discrete-time and continuous-time Sigma-Delta modulator using Input Common Mode Compensation Circuit. The proposed topology is 2nd order Sigma-Delta modulator, which employs a Cascade of Integrators in Feed-forward manner (CIFF). The initial stage of this work involves behavioral modeling of Sigma-Delta modulator, which is performed using VerilogAMS followed by circuit level implementation of the architecture using CMOS $28nm$ technology. The important aspect of the design involves compensation of input common mode variation on the performance of the operational amplifier and improving the resolution of the converter in discrete time ADC. The performance measurements achieved using proposed discrete-time modulator are SNR $97dB$ over signal bandwidth $28.8KHz$ and power dissipation of $0.3mW$ and performance measurements achieved using proposed continuous-time modulator are SNR $92dB$ over signal bandwidth $28.8KHz$ and power dissipation of $270\mu W$

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List of Abbreviations

IC	Integrated Circuits
DSP	Digital Signal Processing
ADC	Analog to Digital Converter
SDM	Sigma-Delta Modulator
CIFF	Cascade of Integrators in Feedforward
CIFB	Cascade of Integrators in Feedback
F_S	Sampling Frequency
F_{IN}	Input Signal band
DNL	Differential Non-linearity
INL	Integral Non-linearity
LSB	Least-Significant Bit
S/H	Sample and Hold
ENOB	Effective Number of Bits
MSV	Mean Square Value
SNDR	Signal to Noise and Distortion Ratio
SFDR	Spurious Free Dynamic Range
THD	Total Harmonic Distortion
OSR	Oversampling Ratio
A/D	Analog to Digital
STF	Signal Transfer Function
NTF	Noise Transfer Function
PSD	Power Spectral Density
PVT	Process Voltage Temperature
OTA	Operational Transconductance Amplifier

Chapter 1

Introduction

In today's IC world, the majority part of signal which takes place in IC is of digital domain because of fast working and very few voltage level. However, the external world signal is in analog form which is interfaced to the system through an interface known as Analog to Digital converter. The block diagram for Digital Signal Processing(DSP) system with interface is shown in Fig. (1.1). ADC plays an important role in high precision audio devices which requires high precision representation of analog data in digital format . The analog interface and digital blocks reside on the same design chip, where digital blocks are generally operated at higher speed, makes the design of ADC even more challenging. The important challenge which is faced during designing of an ADC is trade-off between resolution and speed. The selection of speed or resolution is addressed over the other parameter based on the requirement of the application for example: Audio application requires lower bandwidth data conversion which is achieved by using oversampling Sigma-Delta converters and we use Nyquist-rate converters for higher bandwidth.

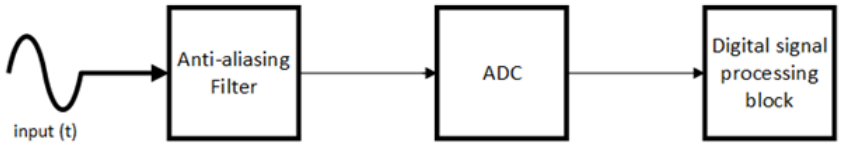

Figure 1.1: Interaction of DSP with external world through ADC interface

1.1 Basic principle of Sigma-Delta ADC

In sound recording and reproduction systems, digital audio refers to a digital representation of the audio waveform for processing, storage or transmission. This process requires conversion of analog signal to digital data with high-precision. The digital audio applications generally make use of sigma-delta converters as it provides better linearity and noise performance for a low-frequency audio signal conversion which results in accurate representation of audio signal

[1]. Sigma-Delta architecture consist a modulator and an digital filter as shown in Fig. (1.2). The accuracy of the sigma-delta modulator is defined by analog circuits which are designed to yield better noise performance and linearity. Sigma-Delta modulator belongs to the category of oversampled converters where input signal is sampled at a frequency, $Fs > 2Fin$. Using oversampling rate relaxes the resolution requirements of the quantizer example:1-bit quantizer results in high resolution modulator output. The total resolution achievable can be further enhanced by improving the noise shaping characteristics produced by the Sigma-Delta loop i.e.,higher order loop filter produces better noise shaping within the input signal band.

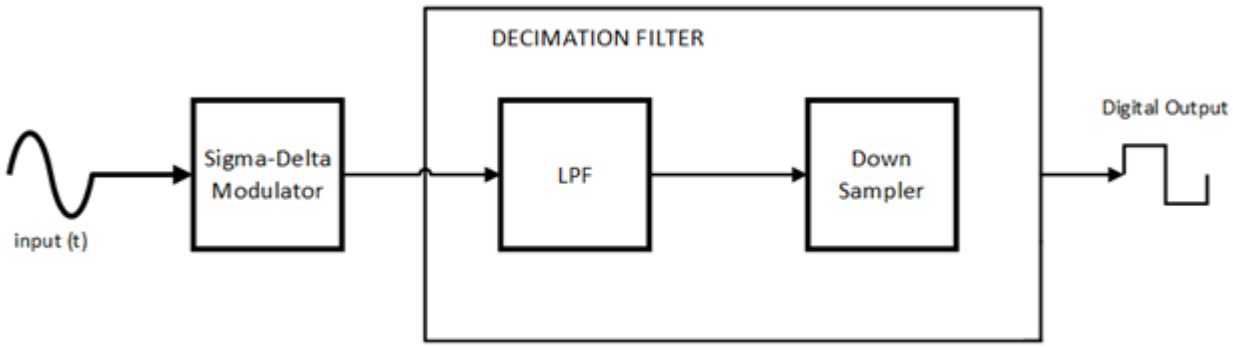

Figure 1.2: General block diagram of Sigma-Delta ADC

1.2 Literature Review

In recent years, many authors had proposed the different strategies to design discrete time and continuous time Sigma-Delta and few of them are listed below:

- In this paper authors have presented a high resolution low power Sigma-Delta modulator for 5 MHz band [2]. They have realised a 3rd order modulator working on 1Ghz sampling frequency. In this paper a Discrete Time Switched Capacitor based design is implemented, which achieves a Signal to Quantization Noise Ratio (SQNR) of 95.3dB, leading to a 15 bit resolution of the ADC with power consumption of 2.3 mW.

- This paper examines the design of full feed-forward Sigma-Delta modulator which is much more suitable for the CMOS digital process with low supply voltage than the traditional second-order feedback loop [3]. The full feed-forward system reduces the modulator's sensitivity of the circuit non-idealities and decreases the internal signal swing to half the full scale. An implementation in a 0.35um CMOS technology achieved dynamic range of 88dB, bandwidth of 48 KHz and power consumption of 5mW. It can operate from supply voltages ranging from 2.4v–3.3v. The architecture is quite useful for low voltage SOC applications, such as portable biomedical system.

- This paper proposes a full differential and low-noise chopper-stabilized amplifier for input signal amplification of Sigma-Delta analog to digital converter (ADC) [4]. Based on chopper stabilizing and dynamic matching techniques, folded-cascode structure with class AB output stage is adopted and chopper switches are used at low-resistance nodes in the current paths to improve the signal bandwidth and output voltage swing. The simulation results based on chartered 0.35um CMOS process show that with the power supply of 3.3V, the chopper-stabilized amplifier has open-loop gain of 84 dB and gain bandwidth (GBW) of 483 kHz. Between 1 Hz and 1 kHz, the input equivalent noise is 1.6uV/vhz without chopper signals and is reduced to 40nV/vhz after chopper signals of 38.4 kHz are added.

- In this paper, a high-resolution medium-frequency single-loop fourth-order 1-bit Sigma-Delta modulator is implemented in 0.18µm CMOS technology. The modulator has been presented with an oversampling ratio of 50, clock frequency of 31.25MHz, 312.5 kHz bandwidth, and achieves a peak SNR of 101.7dB, which is 16.6-bit resolution, 103dB dynamic range [5]. The whole circuits consume 58.55-mW from a single 1.8V supply voltage. The experimental results show a figure-of-merit (FOM) of 170.27dB. A system to circuit level design is finished in this paper.

- A switched-capacitor low-distortion 15-level Selta-Delta ADC is described [6]. It achieves third-order noise shaping with only two integrators by using quantization noise coupling. Realized in a 0.18 mum CMOS technology, it provides 81 dB SNDR, 82 dB dynamic range, and -98 dB THD in a signal bandwidth of 1.9 MHz. It dissipates 8.1 mW with a 1.5 V power supply (analog power 4.4 mW, digital power 3.7 mW). Its figure-of-merit is 0.25 pJ/conversion-step, which is among the best reported for discrete-time delta-sigma ADCs in wideband applications.

1.3 Thesis Contribution

This thesis presents a high resolution Sigma-Delta modulator with Cascade of Integrators in Feed Forward (CIFF) architecture. It features a $2nd$ order discrete-time filter and low power $1-bit$ quantizer using latch comparator. The different phases of clock needed are generated by phase generator. The effect of input common-mode variation on the loop filter performance is also discussed and an efficient way to minimize it is proposed. The design is most suited for audio applications .i.e., input signal band of $28.8KHz$, sampling frequency $14.4MHz$ and oversampling ratio(OSR) of 270. It also features a continuous time Sigma-Delta modulator with same specification but with less power.

1.4 Outline of Thesis

Chapter 1 gives the basic idea of Sigma-Delta data converter. It also discuss some work done in the area of discrete time Sigma-Delta converter.

Chapter 2 presents origin of Sigma-Delta converters and its noise shaping property. It also distinguishes between discrete time and continuous time sigma-delta modulators.

Chapter 3 includes the entire design methodology used for the high performance implementation of the converter. The whole design of discrete time and continuous time modulator includes high gain operational amplifier , comparator, phase generator and DAC. In this chapter we also discuss the results of the each blocks of modulator and also final modulator output. Also performance summary of the design is discussed here.

Chapter 4 presents the bias generation for modulator which has very low deviation with respect to process, voltage and temperature(PVT) variation.

Chapter 5 presents the conclusion and also future scope of work related to Sigma-Delta modulator.

Chapter 2

Basic principle of Sigma-Delta modulator

2.1 Origin of Sigma-Delta modulators

The block diagram describing A to D conversion is shown in Fig.(2.1)

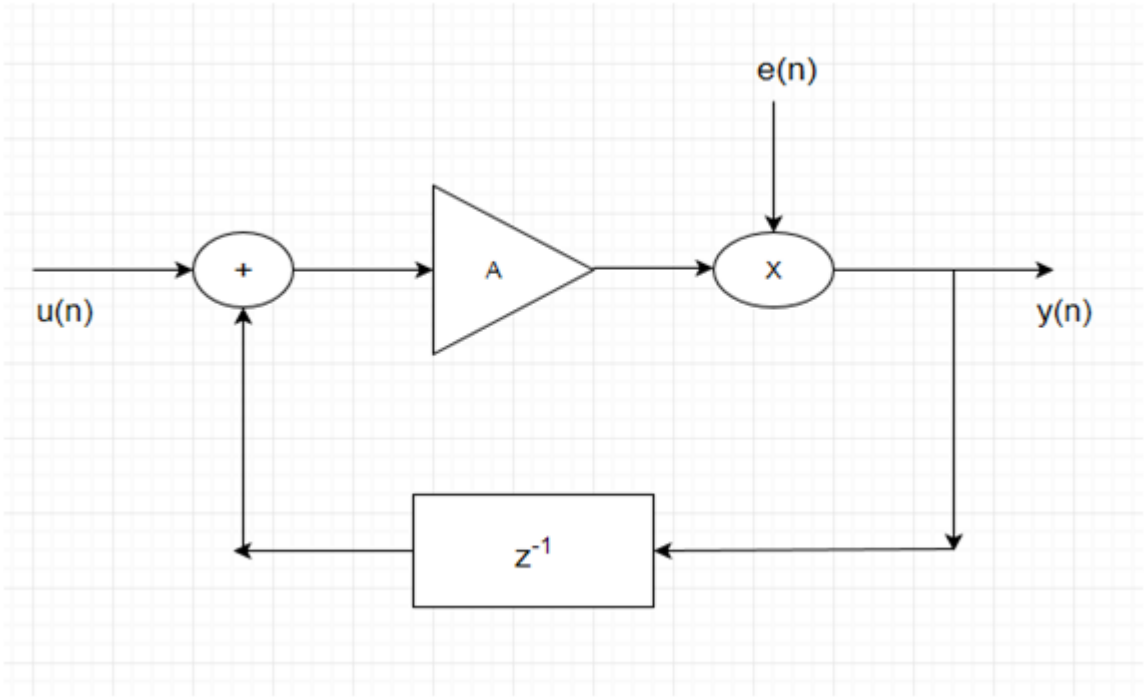

Figure 2.1: Block diagram realizing A to D conversion

The STF for the system shown in Fig. (2.1) is given by

$$STF = \frac{A}{1 + Az^{-1}} \tag{2.1}$$

NTF for the system shown in Fig. (2.1) is given by

$$NTF = \frac{1}{1 + Az^{-1}} \tag{2.2}$$

STF is measured from u(n) to y(n) with quantization error e(n)=0,with pole at z=A where as the NTF is measured from e(n) to y(n) with u(n)=0. Here e(n) is assumed to be input signal independent and has uniform PSD .i.e., white noise. The magnitude of the NTF can be reduced to zero ,provided the gain of the amplifier is very high. However, from the stability point of view with pole z=A, as gain of the amplifier increases, pole moves away from z=1. Hence, system becomes unstable. In order to meet requirement in terms of stability and gain, a amplifier A is replaced by a filter with low pass characteristics which provide high gain at low-frequency .i.e., Integrator which acts as low pass filter. This kind of modification leads to Sigma-Delta modulator architecture which is shown in Fig.(2.2). The STF and NTF for the SDM descibed

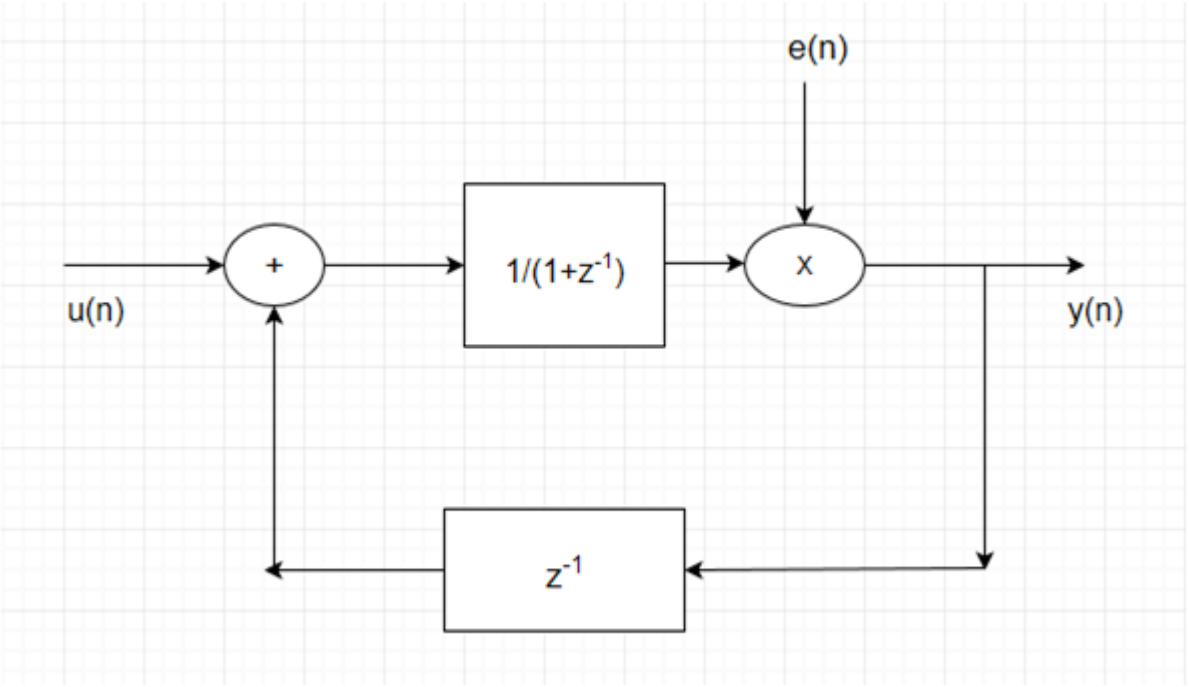

Figure 2.2: Basic Sigma-Delta modulator

in Fig. (2.2) can be derived as

$$STF = z^{-1} \tag{2.3}$$

$$NTF = 1 - z^{-1} \tag{2.4}$$

From the STF we can observe that gain of the system is unity whereas from the NTF it can be seen that modulator behaves as high pass filter to noise components in the system which helps in achieving noise shaping within desired signal band.

2.2 Noise shaping characteristics

Noise performance of the Sigma-Delta system can be further enhanced by shaping most of the noise left in the signal band by increasing the OSR. This is achieved by using a decimation filter consisting of digital low-pass filter and a down-sampler after modulator operating at oversampling rate reduces the in-band noise further [3]. The NTF for an nth order system is given by

$$NTF = (1 - z^{-1})^n \tag{2.5}$$

For a second order modulator n=2,

$$NTF = (1 - z^{-1})^2 \tag{2.6}$$

As 'n' increases , amount of noise power within signal band is reduced. The noise shaping curves represented for higher order systems is as shown in Fig. (2.3). The in-band noise power for at

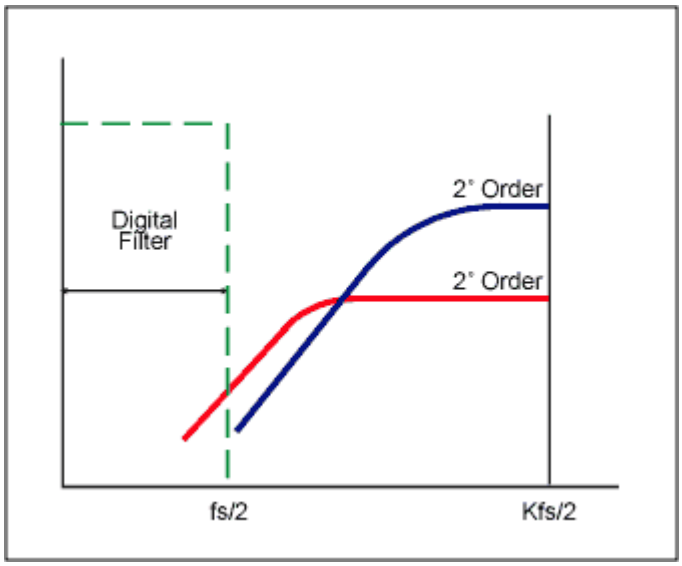

Figure 2.3: Output noise shaping characteristics for 1st and 2nd order modulator

the output of the Sigma-Delta system can calculated as

$$Noise - power = \frac{\Delta^2 \Pi^2}{36 OSR^3} \tag{2.7}$$

The noise-shaping and hence SNR can be further improved by increasing OSR and order of the

modulator. As OSR is doubled , Noise power is reduced by 8-times (9db) which increases overall resolution by 1.5bits.The feedback configuration will give a NTF which behaves as a noise shaping circuit and hence now doubling OSR, Noise is reduced by factor 8 i.e.,1.5bit improvement.

2.3 Discrete-time SDM

A general block diagram describing principle of SDM is shown in Fig. (2.4) consisting of Integrator, Comparator and a feedback DAC .Basic principle of working involves sampling of input signal and the difference between the sampled and feedback signal is accumulated using an integrator. The integrated signal is then quantized by a comparator .i.e., the output of the comparator is high if integrator output is greater than zero and it is low when integrator output is less than zero.

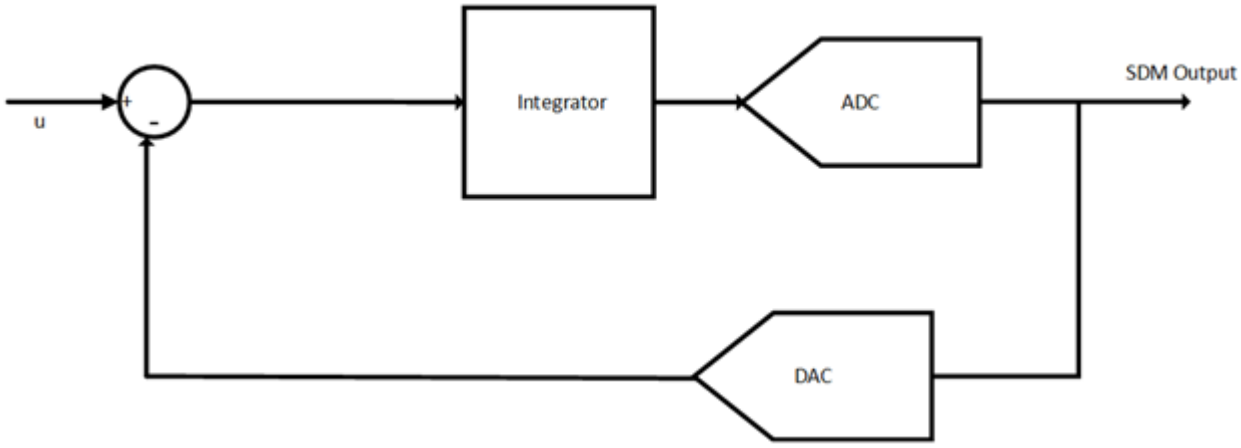

Figure 2.4: Principle block diagram of SDM

The feedback configuration is used to achieve a NTF which is high pass in nature and STF which has unity gain. The STF and NTF for a second order modulator is given by

$$STF = (z^{-1})^2 \tag{2.8}$$

$$NTF = (1 - z^{-1})^2 \tag{2.9}$$

From the STF it can be seen that input signal is delayed by two units(cycles) which is realized by using cascade of two integrators. Hence increase in order results in better resolution but the order of the system is chosen such that there is no overloading of the quantizer. Overloading is a situation where the input amplitude to a quantizer is too high such that it is unable to resolve properly to the precise levels.

2.4 Continuous-time SDM

A general block diagram describing principle of continuous time SDM is shown in Fig. (2.5). The main difference between the continuous time and discrete time Sigma-Delta modulator is sampling and realisation of integrator.

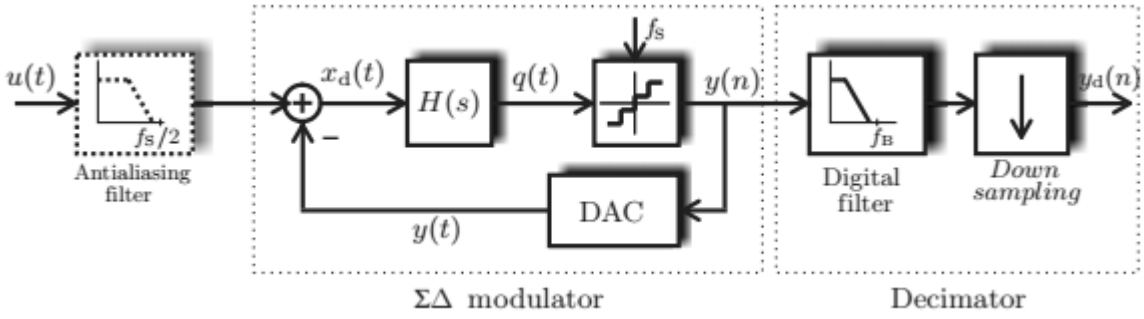

Figure 2.5: Principle block diagrbm of CT-SDM

2.5 Differences between Discrete-time and Continuous-time Sigma-Delta ADC

The block diagrams describing DT and CT SDM are shown in Fig. (2.6) and Fig. (2.7) respectively

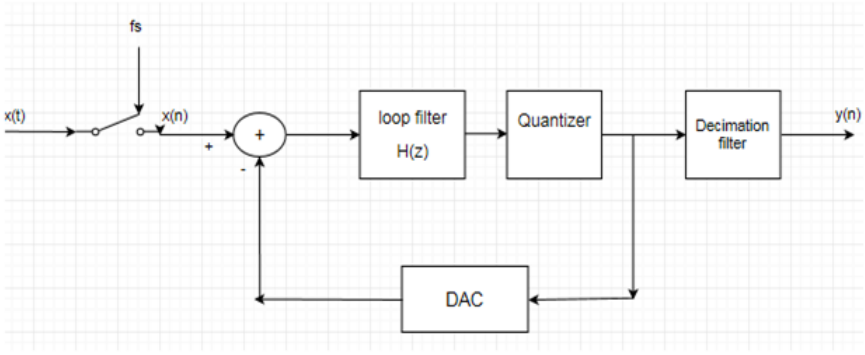

Figure 2.6: Discrete-time Sigma-Delta ADC

Loop filter is realized using switched-capacitor integrator in discrete time realization and in continuous time realization RC-integrators are used. Continuous-time realization requires physical resistors whose values must be kept small to minimize resistor-noise (thermal noise). Since time constant in continuous-time is dependent of product of R and C, it is more prone to process-

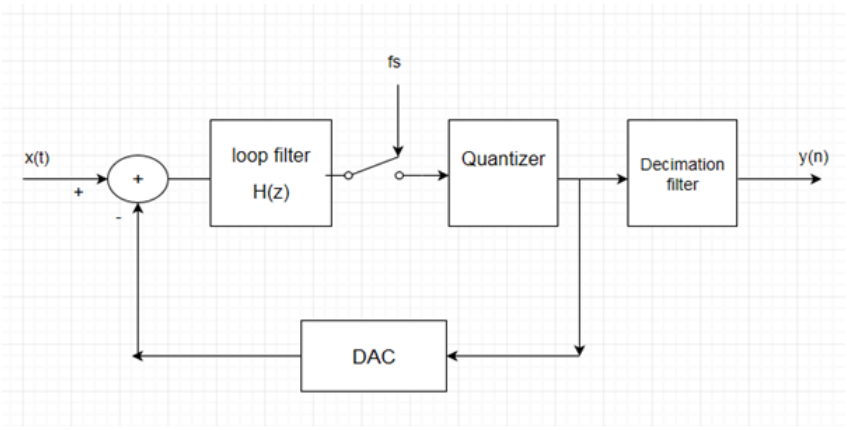

Figure 2.7: Continuous-time Sigma-Delta ADC

variations where as in discrete-time implementation, time constant is defined by the ratio of capacitance and sampling frequency. The variation of capacitance with respect to process in less compared to that of resistors [4]. Discrete-time realization is less sensitive to clock-jitter compared to that of continuous-time. The bandwidth requirement of op amp in continuous time is very less compared to that of discrete time. Therefore , continuous time is said to power efficient realization of SDM. Discrete-time modulator requires anti-aliasing filter at the input stage where as Continuous-time system has inherent anti-aliasing feature and hence does not require an anti-aliasing filter , where loop-filter attenuates the high-frequency components i.e., multiples of sampling frequency responsible for aliasing. This leads to reduction in overall power consumption.The advantages that we obtain by using continuous time(CT) and discrete time(DT) loop filter are shown in Table (2.1).

Discrete time	**Continuous Time**
Low sensitivity to clock jitter	Implicit antialiasing filter
Low sensitivity to excess loop delay	Attenuated (noise shaped) S/H errors
Low sensitivity to DAC waveform	Higher sampling frequency possible
Accurately defined integrator gains and transfer functions	Relaxed OpAmp speed requirements
Highly linear SC integrator	Reduced supply and ground noise impact
Capacitive loads only	Less glitch sensitive and digital noise
Lower simulation time (High level)	Lower simulation time (Circuit level)

Table 2.1: Advantages obtained by using CT and DT loop filter

Chapter 3

Design of Discrete-time and Continuous-time Sigma-Delta modulator

In this chapter we discuss design methodology involved in implementing second-order discrete time SDM and a novel method to reduce the effect of input common-mode variation on the op amp performance is discussed later. We have also discussed designing of continuous time Sigma-Delta modulator.

3.1 Architecture of Sigma-Delta modulator

A Sigma-Delta modulator can be implemented in several ways which is defined by the use of integrators in feed-forward or feedback manner depending on the requirement. For low-power application, we prefer using CIFF over CIFB [5]. The advantages of using CIFF is low-swing requirements of the op-amp and low-noise performance.

Illustration of swing requirement in both CIFF and CIFB structure:Consider Fig. 3.f1 and Fig. (3.2) which represents a SDM in both CIFB and CIFF configuration respectively. In both figures, 'x' is the input signal, 'v' is the feedback signal, 'e' is the error signal given by e=x-v and 'q' is noise component introduced by the quantizer. Since it is a negative feedback loop, error will be almost equal to zero. To make this happen, in CIFB structure feedback signal should contain the input signal component 'x'. 'v' gets signal component only from integrator/amplifier output as 'q' is assumed to be white noise . For the large input swing at the input of the op amp, its output should follow large signal swing at its output terminals. This leads to variation in gain as a result of which non-linearity occurs. Therefore, CIFB structure is more prone to non-linearity and also consumes more power. In CIFF structure, the large-swing requirement of the

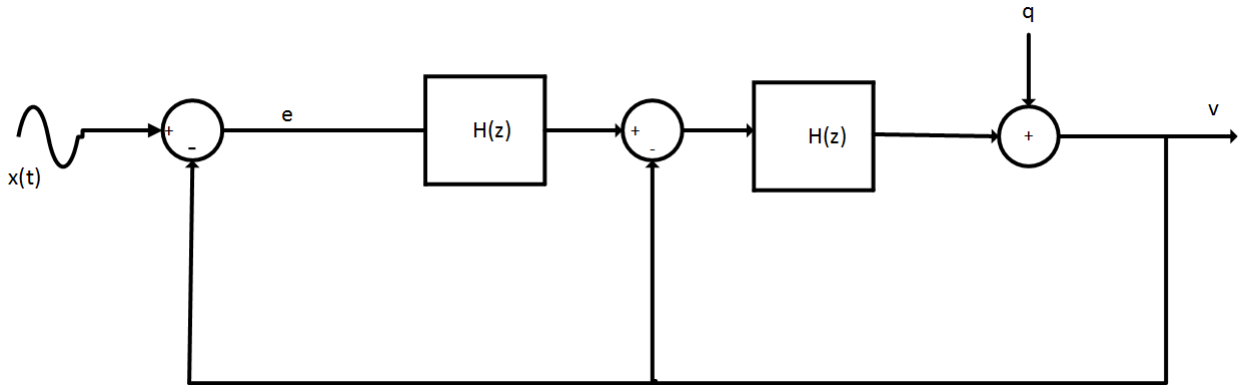

Figure 3.1: 2nd order SDM in CIFB configuration

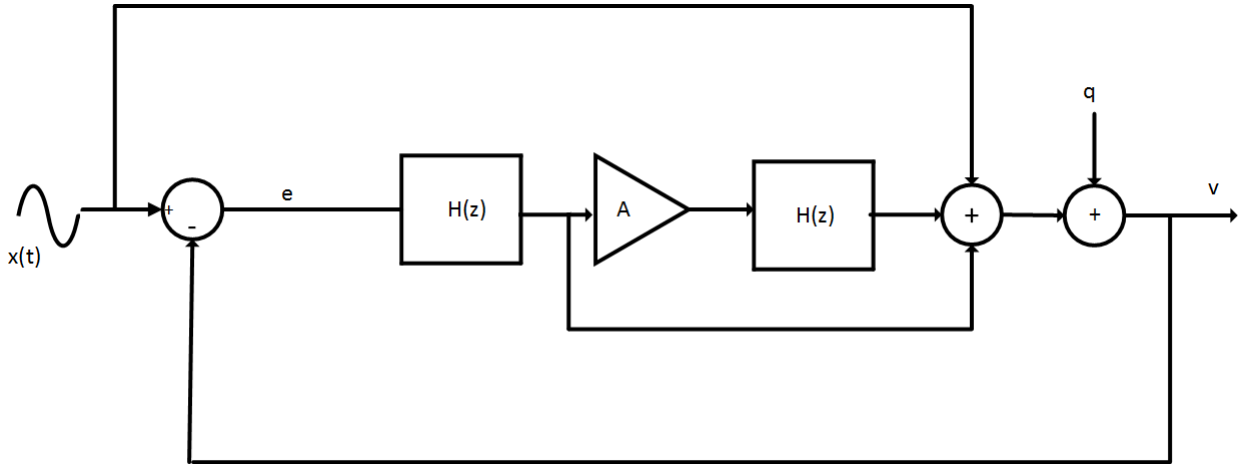

Figure 3.2: 2nd order SDM in CIFF configuration

op amp is overcome as 'v' and 'y' gets input signal component from fixed point (feed forward 'x'). Therefore, amplifier does not need to have high swing/high slew rate in order to keep 'e' to nearly zero. The proposed SDM in CIFF configuration is described in Fig. (3.3).

The values of coefficients will decide the power dissipation of operation amplifier and noise transfer function of total architecture [6]. The value of $a1$ should be minimal to get low swing at output of integrator but it cannot be very low because it will degrade stability due to overloading.

Thus coefficient values are chosen such that its meets both stability and power dissipation requirement. The suitable coefficients values used in the proposed implementation are $a1 = 7/8$,$a2 = 8/3$,$b0 = 1$,$b1 = 16/3$ and $b2 = 13/7$. The values of coefficients can be more than 1 which cannot be achieved with the help of passive circuit and hence active circuit(summation) is used to achieve these values which will results in high SNR with slight increase in power consumption. The NTF and STF of proposed model is found to be

$$STF = 0.428 + 1.142z^{-1} + 0.285z^{-2} \tag{3.1}$$

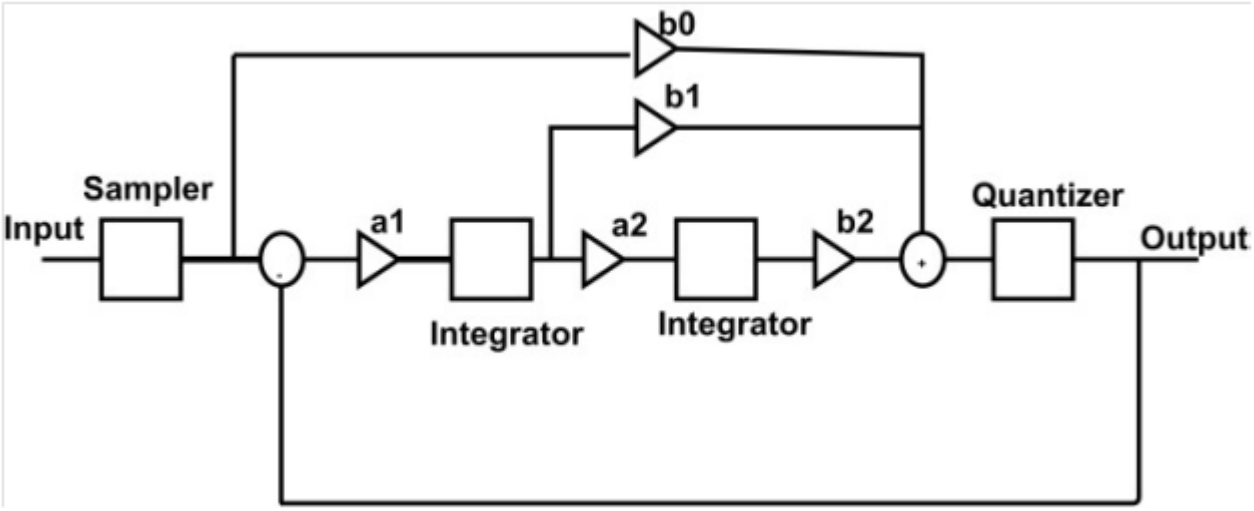

Figure 3.3: Proposed CIFF structure

$$NTF = 0.571(1 - z^{-1})^2 \tag{3.2}$$

3.2 Circuit design methodology for discrete time Sigma-Delta modulator

In the proposed Sigma-Delta modulator a switch capacitor circuit for input common mode compensation circuit is used. Also it has been proposed to use the double sampling [7] in the input path to reduce the input capacitor non-idealities. The proposed model of Sigma-Delta modulator following CIFF structure contains cascade of two integrators, comparator and an additional operational amplifier for summing coefficients. The operational amplifier used for summation does not require high gain hence it consumes much less power. The circuit level description of the proposed Discrete-time Sigma-Delta modulator is shown Fig. (3.4).

As the integrator is realized in SC-configuration, the requirement of S/H circuit prior to integration is avoided as sampling is done implicitly by integrator in first phase which will be discussed later. The SC integrator includes sampling switches, capacitors, op amp.The sampling switches are operated by non-overlapping clock signals generated by non-overlapping phase generator. Clock generator is realized using a logic gates, where required non-overlapping time is achieved by adjusting logic delays. 1-bit quantizer is implemented using Strong-Arm latched comparator. Latched comparator is preferred over other implementation is due to its quick response time and low power consumption. Also latched comparator is free from hysteresis effect. The reference voltages for the integrator is selected by the 1-bit DAC based on the quantizer output.

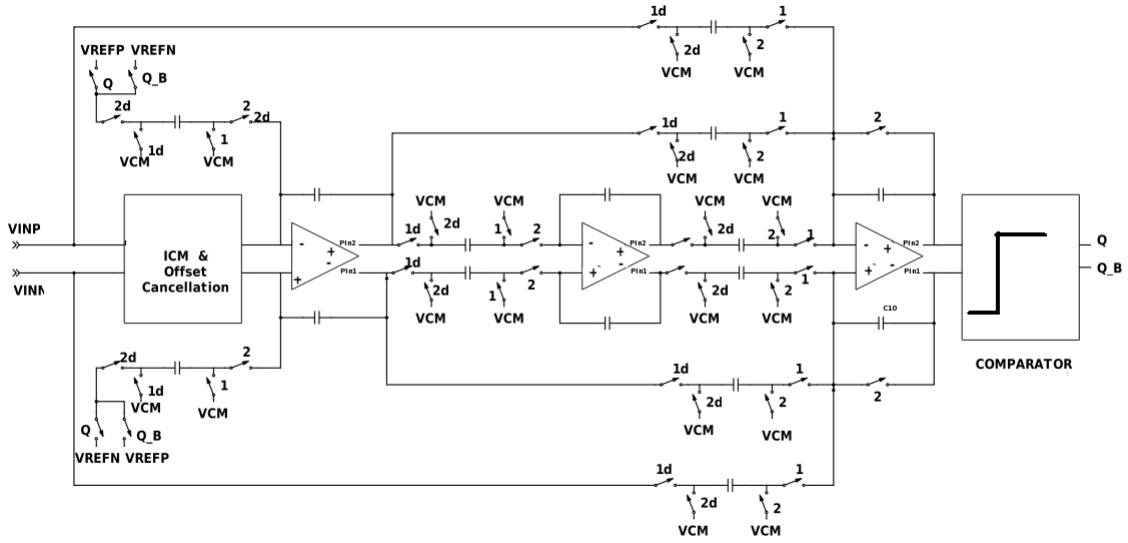

Figure 3.4: Discrete-time Second-order Sigma-Delta Modulator

3.2.1 Discrete-time Integrator

The switched-capacitor realization of loop filter is represented in Fig. (3.5) [8]. The SC integrator shown in Fig. (3.5) operates in two phases:

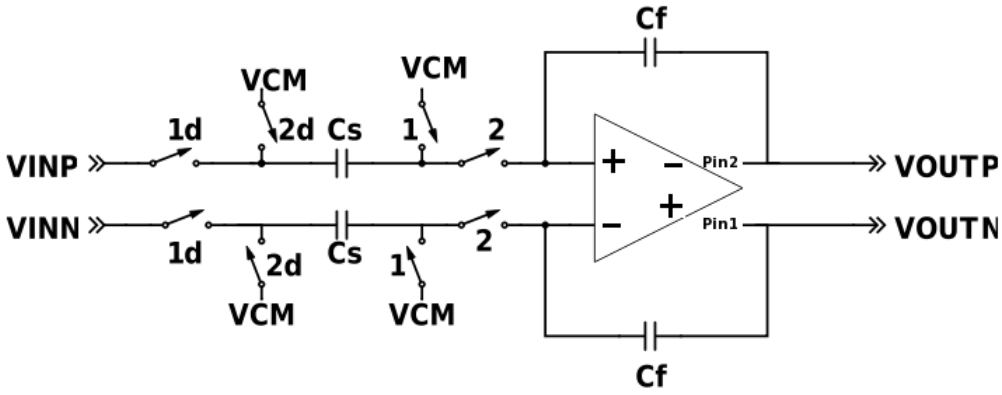

Figure 3.5: Switched Capacitor Integrator

In Phase 1 , op amp is disconnected from the input and the charge on the feedback capacitor C_F is retained to its previous value. The input signal is now sampled on to sampling capacitor C_S. The charged stored in this phase is given by

$$Q = C_S Vin \tag{3.3}$$

Initial charge on the C_S can be assumed to be zero. This phase is known as Sampling phase.Integrator operating in this phase is shown in Fig. (3.6)

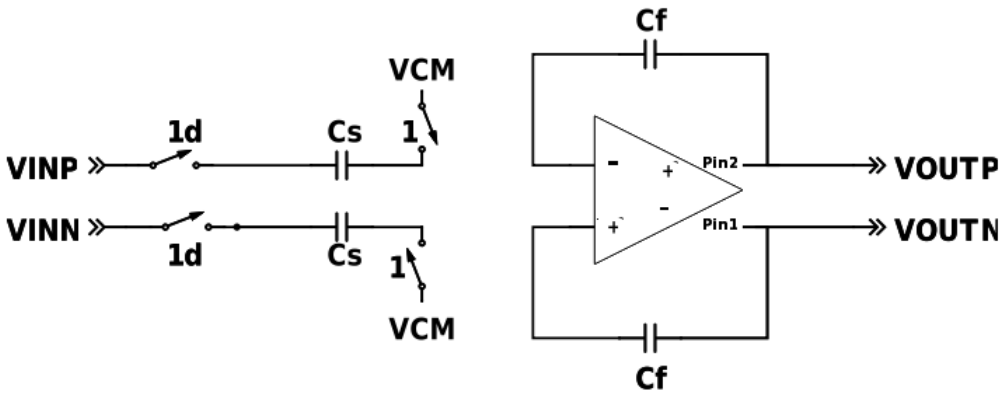

Figure 3.6: Sampling phase of integrator

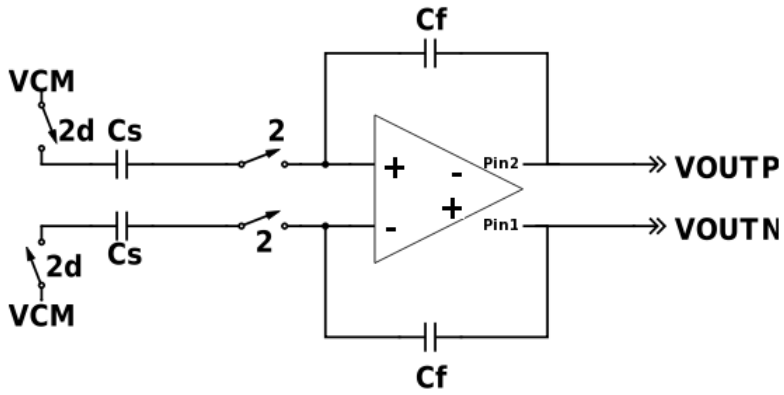

Figure 3.7: Integrating phase of the integrator

In Phase 2, polarities of C_S is reversed as voltage on bottom-plate becomes higher than that of top-plate.The charge stored during Phase1 is now transferred to the feedback capacitor C_F. This phase is know as Integrating Phase represented in Fig. (3.7)

Therefore,the Transfer function of the discrete time integrator can be derived as follows: Applying charge conservation theorem at op amp virtual ground terminals, Total charge during phase1 will be equal to the total charge during phase2. V indicates the potential at op amp input terminal assuming op amp has very high gain such both terminals are at same potential

$$-C_S(Vinp1 - V)\breve{}C_F(Voutp1 - V) = +C_S(V) - C_F(Voutp - V) \tag{3.4}$$

where $Vinp1 = z^{-1}Vinp$
On solving above equation,

$$C_F Voutn(1 - z^{-1}) = C_S Vinnz^{-1} \tag{3.5}$$

Similarly

$$C_S(Vinn1 - V) - CF(Voutn1 - V) = +C_S(V) - C_F(Voutn - V) \tag{3.6}$$

and

$$C_F Voutn(1 - z^{-1}) = C_S Vinnz^{-1} \tag{3.7}$$

Therefore ,

$$H(z) = \frac{Vout_p(z) - Vout_n(z)}{Vin_p(z) - Vin_n(z)} = +\frac{z^{-1}}{1 - z^{-1}}\frac{C_S}{C_F} \tag{3.8}$$

Where C_S/C_F is the called the gain of the integrator and z^{-1} in the numerator indicates the delay between input and output . With reference voltages the differential output voltages can be related to its inputs and reference voltages as

$$Voutp(z) - Voutn(z) = [Vinp(z) - Vinn(z)]\frac{C_S}{C_F}\frac{z^{-1}}{1 - z^{-1}} - [Vrefp(z) - Vrefm(z)]\frac{C_S}{C_F}\frac{1}{1 - z^{-1}} \tag{3.9}$$

The negative sign associated with reference signal indicates the negative feedback voltage decided by DAC. To overcome the charge-injection effect of the MOS switch, delayed version of the clocks are used along the original phase.i.e., PH1D and PH2D. PH1D turns off after PH1 turns off. This makes sampling capacitor floating at the end of phase1 which avoids charge injection effect on the load voltage.

3.2.2 Operational Amplifier

The noise transfer function of Sigma-Delta which is quantization noise shaping behaviour is defined by transfer function of loop filter. The complete loop of Sigma-Delta consist several first order filters which are realised with the help of switched capacitor integrator. The integrator is realised with the help of operational amplifier so performance of operational amplifier is very critical in Sigma-Delta loop [9].

Performance metrics of Op amp	**Effects on SDM**
Gain	Noise Floor and Harmonic Distortion
Bandwidth	Noise Floor and Stability of the Loop
Slew Rate	Quantisation noise and Harmonic distortion
Thermal and Flicker noise	Noise Floor

Table 3.1: Effect of op amp performance on SDM

The performance of Sigma-Delta modulator is related to various parameters of operational amplifier can be seen in the Table (3.1).So good performance Sigma-Delta loop, requires operational amplifier which has high gain, bandwidth slew rate so the noise floor should be as low as it can but it will increase our current requirement so power will increase so a trade-off exists between power and all other parameters.

We used folded cascode architecture for operational amplifier because it has high swing (than telescopic), high gain and single stage architecture so easy to stabilize. The main problem of folded cascode is high input noise and offset which are compensated using one novel technique which is discussed later. In the design of operational amplifier positive and negative slew rate equal. The schematic of folded cascode is described in Fig. (3.8).

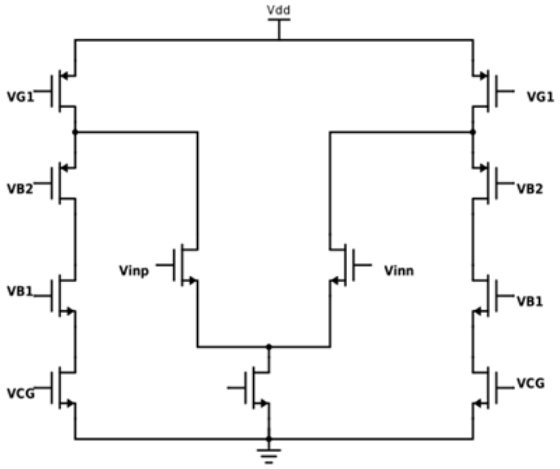

Figure 3.8: Schematic of folded cascade amplifier

In the fully differential amplifier [9] the output node is set with the help of common mode feedback circuit. The sensing of output common mode is done with the help of switched capacitor sensing circuit because with resistive sensing circuit there is problem of gain loss. The schematic for sensing circuit is described in Fig. (3.9).

The biasing of operational amplifier is done in such a way that the main schematic will adapt all the changes with process, voltage and temperature and operational amplifier is working across all the corners. The biasing voltages are generated using reference current which is generated with the help of band-gap reference. The schematic of biasing circuit is described in Fig. (3.10).

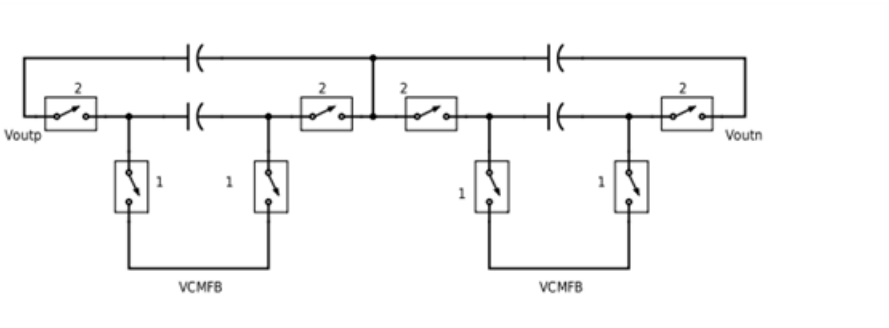

Figure 3.9: Schematic of sensing circuit

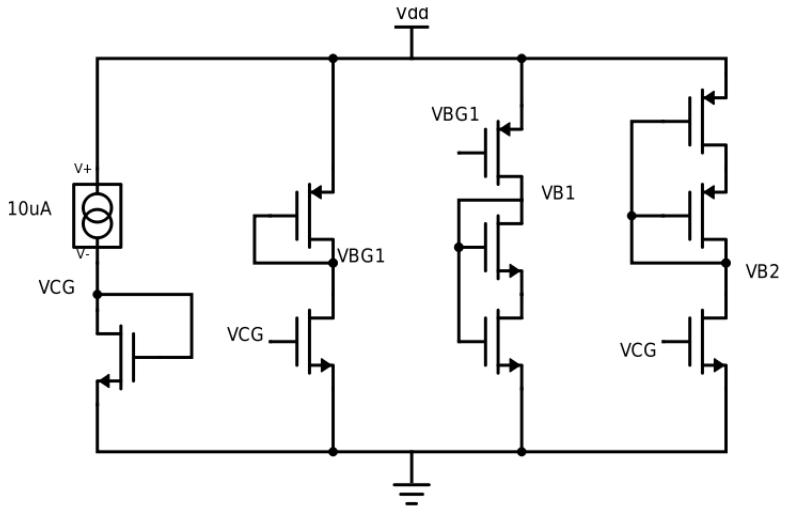

Figure 3.10: Schematic of biasing circuit

3.2.3 MOS Switches

The design of sampling switches used in the ADC plays important role in the overall performance of a converter. Switches are designed in such a way that,it resistances should match with that of an ideal switch.i.e.,zero ON resistances and infinite OFF resistance. However, practically we would be able achieve finite resistance when switch either on or off. Here MOS transistor are used as a pass transistor which operates in linear region. There is also parasitic capacitance associated with a MOS switch resulting in charge injection, clock feed through error, which causes non-linearity in the output such as gain error and offset error. Therefore, design of sampling switch proves to be more challenging in achieving high performance data converter. The commonly used switch is a NMOS switch shown in Fig. (3.11).The one of the important issue to be addressed in NMOS switch is that it passes weak logic 1's and PMOS switch passes weak logic 0's.

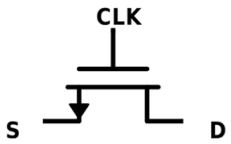

Figure 3.11: NMOS switch

Another issue is that NMOS switch , ON-resistance is signal dependent.R_{ON} for a MOS transistor in linear region is given by

$$R_{\mathrm{ON}} = \frac{1}{\mu_n C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_t)} \tag{3.10}$$

For V_G=V_{DD} and V_S = Vin,

$$R_{\mathrm{ON}} = \frac{1}{\mu_n C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{DD}} - V_{\mathrm{IN}} - V_t)} \tag{3.11}$$

This variable resistance leads to non-linearity in the output. The voltage dependent resistance problem of the NMOS switch along with its swing limit can be overcome by using a Transmission gate as a switch which requires two control signals (normal and its complementary signal). It consists of a NMOS and PMOS transistors connected in parallel form shown in Fig. (3.12).

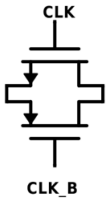

Figure 3.12: Transmission-Gate Switch

This type of switch has minimum ON-resistance variation with respect with V_{GS} and hence able to produce rail-rail swings. The sizes of the PMOS is almost twice as that of NMOS such that both the transistors operates at the same speed . Even we can increase a linearity of the switch i.e.,V_{gs} is constant using Boot-strap method at the same time achieve maximum swing, in the proposed architecture we use Transmission gate switch as Boot-strap switch fails SOA test , with gate voltage of MOS switch exceeding supply.

3.2.4 Comparator

In the proposed Sigma-Delta modulator, 1-bit quantizer is realized using a Strong-Arm comparator [10]. This topology is chosen over others due to its less recovery time , high speed of operation which is the main requirement for an oversampling converters as clock frequency is very high. The other important advantage is low hysteresis effect .The strong-arm latch comparator is described in Fig. (3.12) and with node capacitance described in Fig. (3.13)

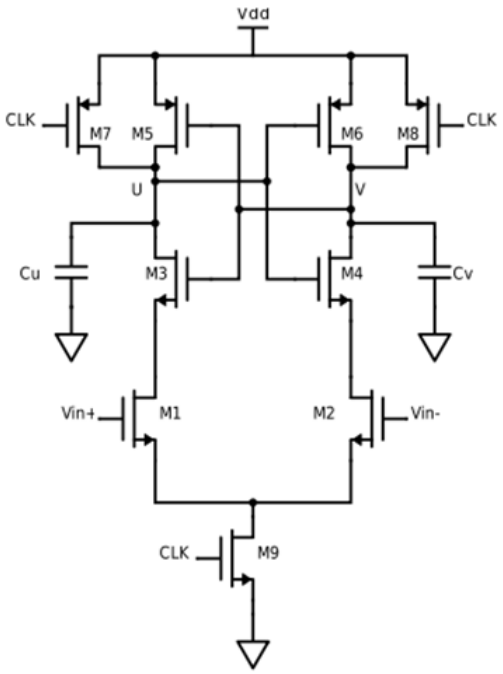

Figure 3.13: Latch comparator with node capacitances C_U and C_V

The topology consists of a pseudo-differential input pair transistors M1 and M2 across which the inputs are applied . Transistors M3-M6 acts as cross-coupled inverters which forms a regenerative latch. M7,M8 and M9 are switches operated by CLK. The circuit resolves the input difference between rail-to-rail. When CLK=0 , this phase is known as pre-charge phase, M9 is turned off so no current flows from V_{DD} to Ground . Hence M1 and M2 also remains off as their source nodes are left floating.M7 and M8 are ON , which charges the node capacitors U and V to V_{DD} .

In second-phase, when CLK is high M7 and M8 are off. M9 is ON, But M5 and M6 is still off as its V_{GS} is zero. This causes the flow of differential current from Supply to Gnd, causing the Capacitance at nodes U and V to discharge such that V_U-V_V is proportional to Vin_+-Vin_-. This phase is known as sampling phase as output capacitance discharges to a certain value determined by the input difference. The discharging slope of the voltages V_U and V_V is dependent on the amplitude of the input difference. If Vin_+ is higher than Vin_- , then C_U discharges faster than

C_V. The timing diagram representing the Comparator operation in each phase is described in Fig. (3.14).

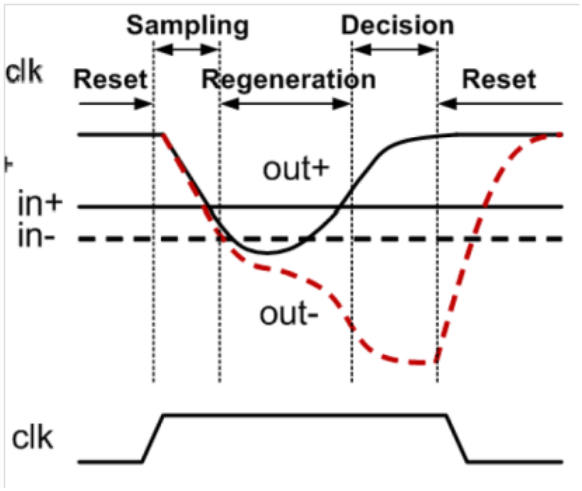

Figure 3.14: Timing diagram of latch comparator indicating different phases

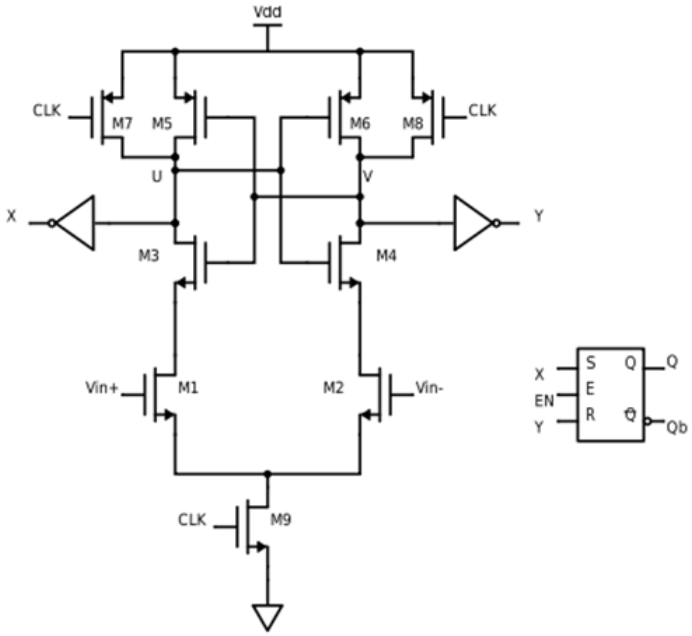

Figure 3.15: Strong-Arm latch comparator with RS latch

As V_U and V_V becomes less than V_{DD}-V_{TP}, M5 and M6 are turned on as its V_{GS} is less than V_{TP}. This leads to the formation of inverters connected in back to back manner. They function as a regenerative latch with positive feedback. The input to these inverters are the sampled values of V_U and V_V obtained during sampling phase. The regenerative latch try to resolve the

sampled output values to V_{DD} and Gnd. M3 and M4 are used to provide path between V_{DD} and Gnd and also to avoid static current flow from V_{DD} and Gnd. M5 and M6 are used to reinstate the output value to V_{DD}. Switches M7 and M8 are used to precharge nodes U and V to V_{DD} so that pull-up transistors of the cross-coupled inverters are off during the sampling phase. This latch will have its output in invalid state (i.e.,$V_U = V_V = V_{DD}$) during first half of clock cycle. To translate the output the output of the regenerative-comparator , an RS latch is connected after the differential stage through inverters . Inverter allow the RS latch to toggle only if output nodes U and V falls. The complete circuit of Strong-Arm latch comparator with RS latch at its output stage is shown in Fig. (3.15)

The power consumption in the strong-Arm comparator is contributed primarily by charging and discharging of the capacitances which is approximately equal to

$$Power = {V_{DD}}^2 f_{CLK} C_{U,V} \tag{3.12}$$

where f_{CLK} is the clock frequency and $C_{U,V}$ is the node capacitance at U or V. The sizing of the transistors are done in such a way that comparator operates with less response time. Input transistors M1 and M2 should be large such that input signal is sensed faster at the same time gate capacitance should not exceed to a large value. M3-M5 should be sized large enough such that regenerative time is less , at the same time it does not slows down the comparator operation. The output inverters are sized such that it is large enough to drive RS latch at the same time it does not slows down comparator operation. The length of the M9 which is used as a switch is kept high to avoid leakage current , as this causes flow of static current when clock is low. Lengths of regenerative inverters should be kept low such that is trans-conductance is high which defines the regenerative time and gain. Widths are decided according to lengths such that comparator operates faster. Regenerative time-constant is given by,

$$\tau_r = \frac{C_{out}}{g_{m3} + g_{m4}} \tag{3.13}$$

Regeneration gain is given by

$$G_r = exp\frac{t_2 - t_1}{\tau_r} \tag{3.14}$$

where t_2-t_1 is regeneration time.

3.2.5 Non-overlapping phase generator

The phase generator circuit for producing non-overlapping clock phases used for control switches is shown in Fig. (3.16).

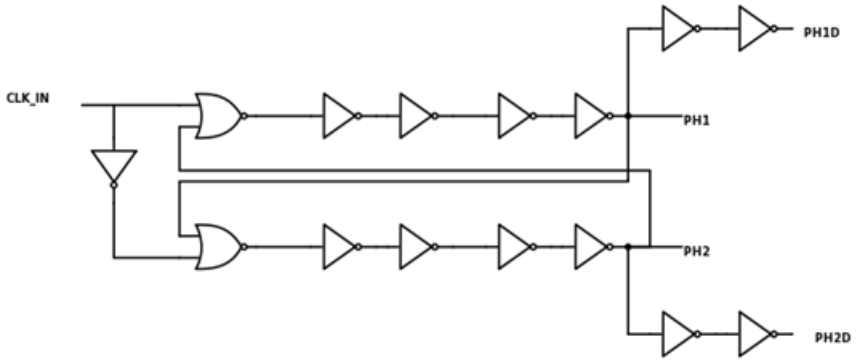

Figure 3.16: Non-overlapping clock generator

It is basically a cross-coupled NAND-gates along with inverters. The delayed versions of the clocks are used to avoid charge injection is realized using Buffers. Also the complementary clock phases of each delayed versions can be generated if necessary. The timing diagram of non-overlapping phases and their delayed versions is given in Fig. (3.17)

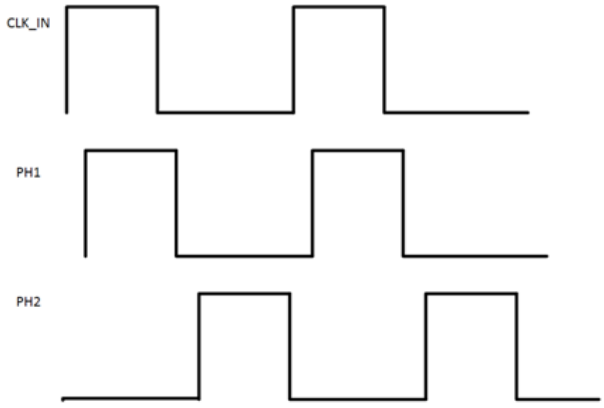

Figure 3.17: Timing diagram of non-overlapping phases

The sizes of the logic gates are chosen to achieve required delays which decide the non-overlapping time. Non-overlapping time is defined as the time between the rising edge of phase1 and falling edge of phase2 or vice-versa. This time difference is chosen to be high such that it accommodates PVT variation .The duty cycle of the generated phases remains almost same as input clock.i.e., 50%.

3.2.6 Feedback-DAC

The 1-bit DAC is used in the feedback as the quantizer is of the resolution 1-bit .The DAC is realized with the help of multiplier which will generate a positive reference if the output of

the quantizer is high and it will generate negative reference if the output of the quantizer is low. As the DAC has two-levels of resolution , It is highly linear and is very less subjective to non-idealities such as DNL or INL.

3.2.7 Novel Implementation

The proposed Sigma-Delta architecture is resistant to variation in the input common mode. Even though if the common-mode quantity vary from 0 to V_{DD} , the performance of the op amp is unaffected by this disturbance .The novel Switched-capacitor technique which is used at the input stage helps in tuning the common mode level of the op amp to a fixed value in the presence variation in input common model level. This technique is known as Input common mode compensation scheme. The proposed model of the compensation scheme is described in Fig. (3.18).

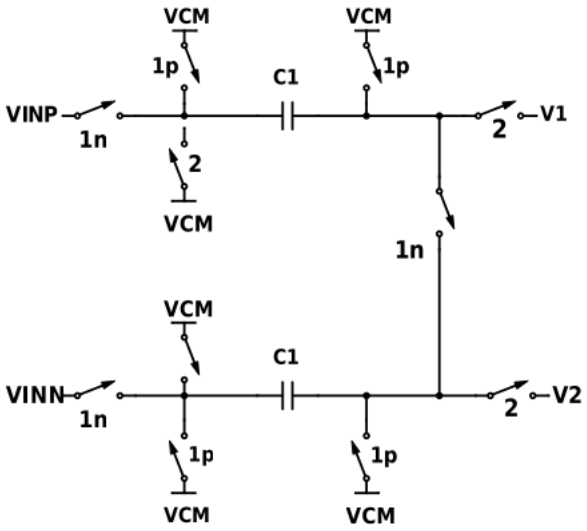

Figure 3.18: Input common mode compensation circuit

This makes the design of input stage of operational amplifier to be of high input common mode range (ICMR). Most of the reported architectures for high ICMR either have more current consumption along with more area or have high non linearity. In this method the input common mode cancellation is done by using the equalization method.

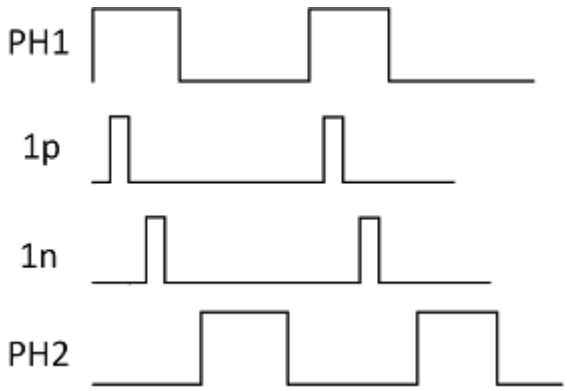

Figure 3.19: Clock Phases used in compensation circuit

The main purpose of input common-mode compensation is to generate differential input signals for op amp whose input common-mode is independent of the overall system. In conventional implementation input common-mode of the system is directly applied to the input of operational amplifier so any change in their common mode will directly reflect on the performance of operational amplifier as shown in Fig. (3.4). Using the proposed compensation circuit as shown in Fig. (3.18), a differential voltage is produced from the input signal whose common-mode is fixed and any variation in the input common-mode of the system will be will not affect system performance. The working of the compensation circuit involves, discharging of both capacitors in phase 1p and in phase 1n, inputs are applied across top-plates of both capacitors while bottom-plates are shorted together. The different phases of clocks used are defined as shown in Fig. (3.19). According to charge conservation rule, In phase 1p , Q=0. In phase 1n ,

$$Q = C(V - Vinp) + C(V - Vinn) \tag{3.15}$$

Equating above two equations,

$$V = \frac{Vinp + Vinn}{2} \tag{3.16}$$

This implies that at the end of phase 1n capacitors will be charged with $C\frac{Vinp-Vinn}{2}$ and $C\frac{Vinn-Vinp}{2}$. Now in phase 2 this charge will set the values of inputs for operational amplifier which can be calculated as follows: In phase 2 ,

$$Q = C(Vcm - Voutn) \tag{3.17}$$

and

$$Q = C(Vcm - Voutp) \tag{3.18}$$

Now equating above two equations,

$$Voutp = \frac{Vinp - Vinn}{2} \tag{3.19}$$

and

$$Voutn = \frac{Vinn - Vinp}{2} \tag{3.20}$$

Last two equations proves that operational amplifier's input common-mode is fixed and is insensitive to variation in the input common-mode of the system.

3.3 Circuit design methodology for continuous time Sigma-Delta modulator

The schematic of continuous time Sigma-Delta modulator is shown in Fig. (3.20).The architecture used for this modulator is also CIFF architecture. In the schematic we can see that integrator is realised with R and C. The coefficients $b0$, $b1$ and $b2$ are realised using resistances.

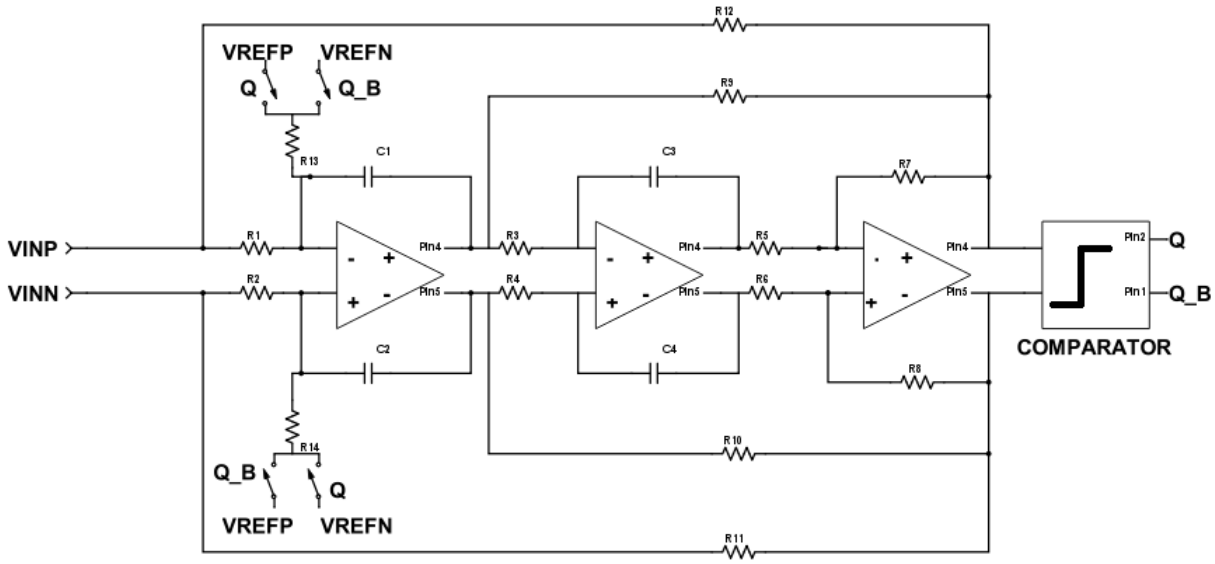

Figure 3.20: Schematic of CT Sigma-Delta modulator

The implemented architecture is fully differential in order to minimise even order harmonics as well as common mode noise. The configuration of operational amplifier and comparator is same as discrete time Sigma-Delta ADC. The feedback is applied with resistance and it is controlled by the output of comparator Q and Q_B. The advantage of CT Sigma-Delta modular over DT Sigma-Delta modulator is that sampling operation takes place inside the loop so all

the non-idealities of the sampling circuit will be applied to noise shaping circuit. The values of resistances are determined by the power constraints so for low power constraints noise will be also low. One more advantage of using this approach is high linearity. The operational amplifier for the integrator shown in Fig. (3.21) is folded cascode same as DT sigma-delta because of high gain and slew rate.

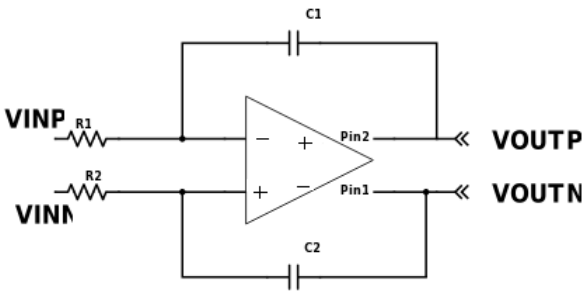

Figure 3.21: Schematic of RC integrator

Effect of error induced by comparator like offset, non-linearities and hysteresis are negligible. The comparator is located within the sigma-delta loop so these non-idealities are compressed by loop gain. But the performance of CT Sigma-Delta can be affected by timing induced errors like propagation and signal dependent delay, which are dependent on the input signal amplitude and slope of comparator.

The main performance parameter for feedback DACs in CT Sigma-Delta modulators are linearity, propagation delay and inter symbol interference. Fortunately, we have used 1-bit DAC which is inherently linear. The architecture of CT-time has several advantages which are already discussed. The results of CT Sigma-Delta are discussed later.

3.4 Results and Discussion

In this chapter we have discussed about simulation results of the designs that we discussed in the previous sections. Also we have analysed the results of behavior model of Sigma-Delta modulator. Also we have analysed the performance measurements of each blocks such as Op amp and Quantizer. We have discussed about different trade-off exists and how they can be optimized to achieve better overall modulator performance in terms of resolution and stability. Also we have discussed the result of proposed input common-mode compensation technique. At the end of this chapter we have discussed the results of the second order discrete time Sigma-Delta modulator using CIFF architecture and continuous time Sigma-Delta modulator. Different performance metrics of the implemented modulator is illustrated in a table at the end of this section.

3.4.1 AMS modeling of the Sigma-Delta modulator

The block diagram of the second order discrete time modulator realized using Verilog AMS model. The input signal is sine wave with amplitude 100mV and frequency 1kHz with Supply of 1.8V.The design is implemented in CIFB configuration i.e., Feedback decides reference voltage of only first integrator. The 1-bit DAC is realized using a simple wire logic. Each blocks such as op amp, comparator and elements such as resistance, switches, capacitors are described at behavioral level using Verilog AMS language, which is used to describe behavior any AMS blocks [11]. The input signal is processed through cascade of two integrators and is connected to output through a comparator. Gain stages in the integrator is chosen to meet overall performance of the system.

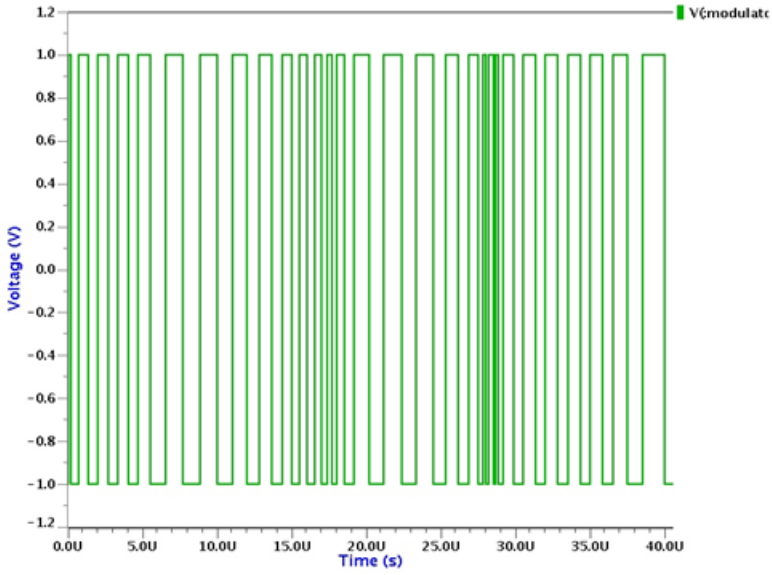

Figure 3.22: 2nd order Sigma-Delta modulator behavior model output

The second order modulator output is shown in Fig. (3.22) The output signal is sampled at same oversampling rate. The number of simulation cycles for the modulator is chosen such that the difference in sampled amplitudes will be averaged over the complete simulation period. This reduces non-linearities in the output spectrum.

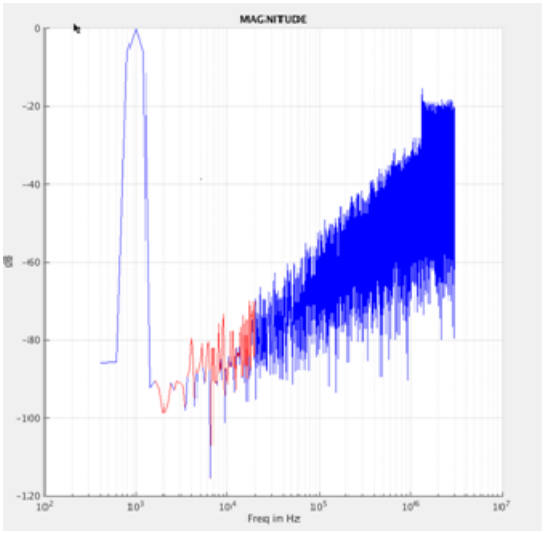

Figure 3.23: Output spectrum of 1st order SDM modulator

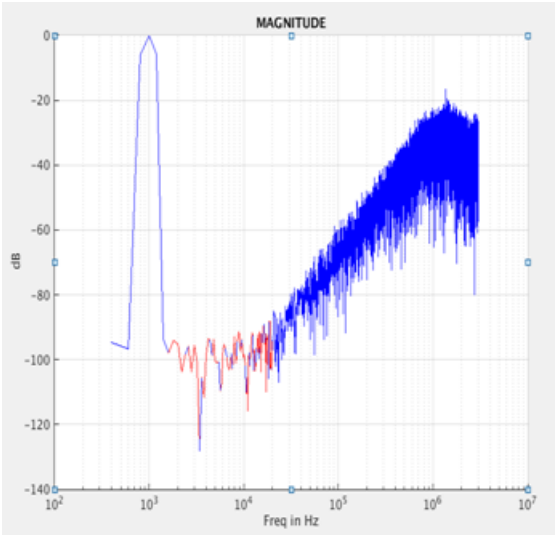

Figure 3.24: Output spectrum of 2nd order SDM modulator

The Fast Fourier Transform(FFT) of the of the sampled output signal is performed using MATLAB to measure the SNR of the modulator. The FFT spectrum of first order and second order behavior model SDM is shown in (3.23) and Fig. (3.24) respectively

The amplitude in log scale is plotted versus the frequency .The SNDR for 1st order modulator is found to be 61.68 dB where as for the 2nd order modulator it is 77.6 dB.

Op Amp	Specification
Open loop gain	69.54dB
UGB	60MHz
Input Impedance	10GΩ
Output Impedance	100Ω
I_{max}	$100\mu A$

Table 3.2: Op amp Behavioral model Specifications

Gain(dB)	SNR(dB)	UGB(MHz)	SNR(dB)
60	70.596	1	66.68
60	74.9	5	70.7836
80	77.91	10	70.78
90	78.12	30	71.12
100	78.39	40	72.34

Table 3.3: Variation of SNR with respect to Gain and UBW of the op amp

By comparing the output spectrum of both the 1st and 2nd order modulators, it can be observed that the noise shaping in second order is improved where large amount of the noise is shifted to the higher frequency bands.The specifications of the op amp used in this model is shown in Table (3.2). The AMS model has been simulated for the effect of Gain and Bandwidth of the op amp on the output SNR. The comparison table for the same is shown in Table (3.3).

3.4.2 Operational Amplifier

The folded cascode design is simulated for the values discussed earlier in this chapter and the results are obtained as follows. The transient simulation of the Op amp is performed for sinusoidal input signals of differential amplitude 200mVpp and frequency 7.2 kHz. The transient response of the folded cascade op amp is shown in Fig. (3.25). The output common mode is adjusted to 0.9V which is half the supply voltage (1.8V), using Switched-capacitor CMFB circuit.

The AC simulation results of the OTA include open loop gain around 100dB and the unity gain-bandwidth for this configuration was 99.68 MHz as shown in Fig. (3.26).

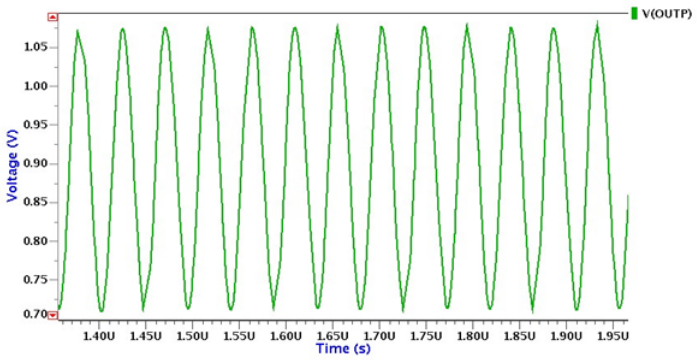

Figure 3.25: Transient output of OTA

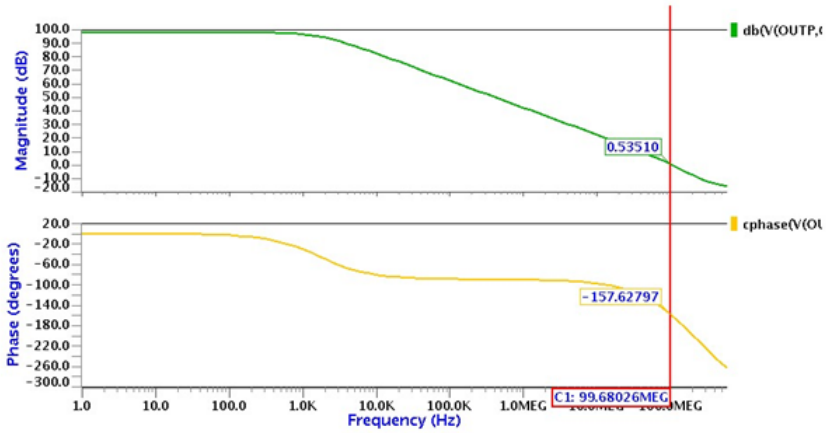

Figure 3.26: AC response including DC gain and phase results of OTA

The phase margin measured is around 23°. The performance metrics table for the OTA is given in Table (3.4).

Performance parameter	**Result**
DC Gain	100dB
Unit gain bandwidth	99.68MHz
Phase margin	23°
Slew rate	$3V/\mu S$
Power Consumption	$184\mu W$
I_{max}	$80\mu A$

Table 3.4: Performance matrix of Folded Cascode Op amp

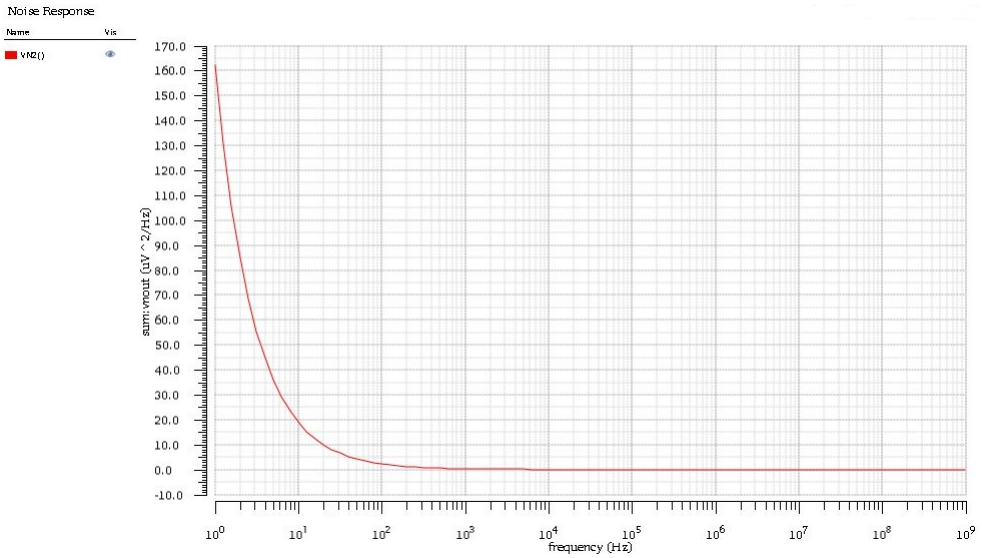

Figure 3.27: Noise behaviour of operational amplifier

3.4.3 1-bit Quantizer

A 1-bit quantizer realized using Strong-Arm comparator, resolves the input difference voltage to supply and gnd. The design methodology of the comparator is discussed in previous chapter. The transient simulation result of the 1-bit quantizer is shown in Fig. (3.28) for one input is applied as sine wave varying around a DC of 0.9V and the other input is given as a DC of 0.9V.

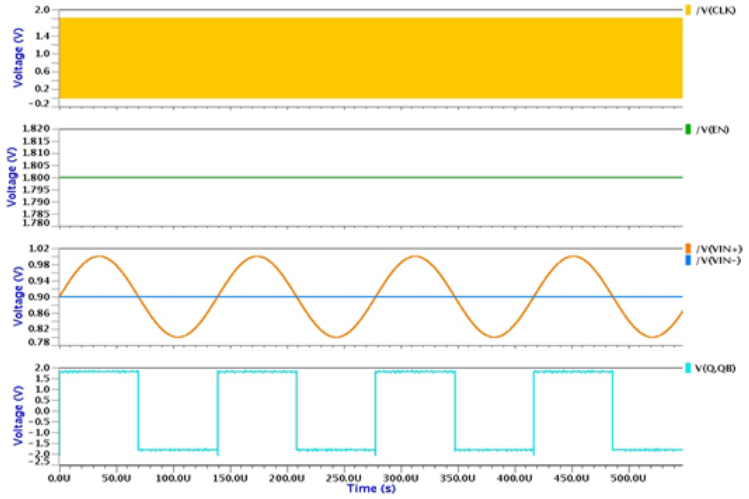

Figure 3.28: 1-bit Quantizer output

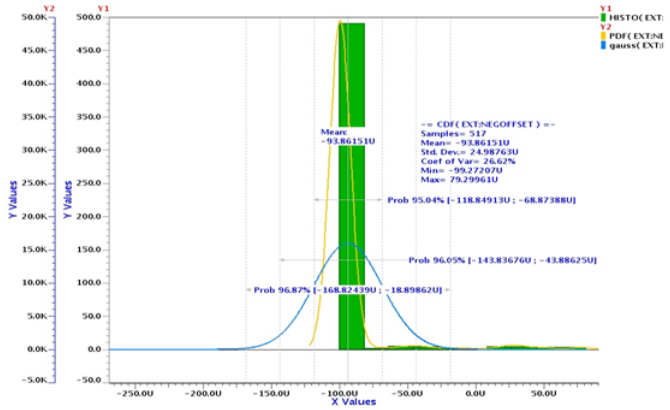

Figure 3.29: Monte-carlo simulation for offset max deviation of $79\mu V$

The output of the comparator is evaluated after each clock cycle.The offset of the comparator is found to be around 100 μV.The monte-carlo simulation results for the offset extraction is shown in Fig. (3.29)

3.4.4 Non-overlapping Phase generator

The results of the non-overlapping phase generator whose design discussed in previous chapter is shown in Fig. (3.30).

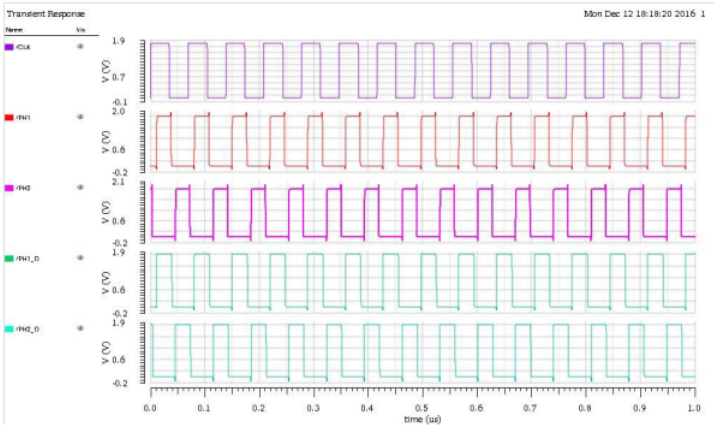

Figure 3.30: Non-overlapping phase generator Output

From the Fig. (3.30) it can be seen that PH1 and PH2 are the Non-overlapping clocks with non-overlapping time of 6ns. The input clock is the system clock with frequency 14.4MHz and duty cycle of 50%. Delayed versions of PH1 and PH2 .i.e., PH1D and PH2D are used to avoid charge injection.

3.4.5 Sigma-Delta Modulator

The simulation result for the second order discrete-time Sigma-Delta modulator described in Fig. (3.6) using CIFF configuration is shown in Fig. (3.31)

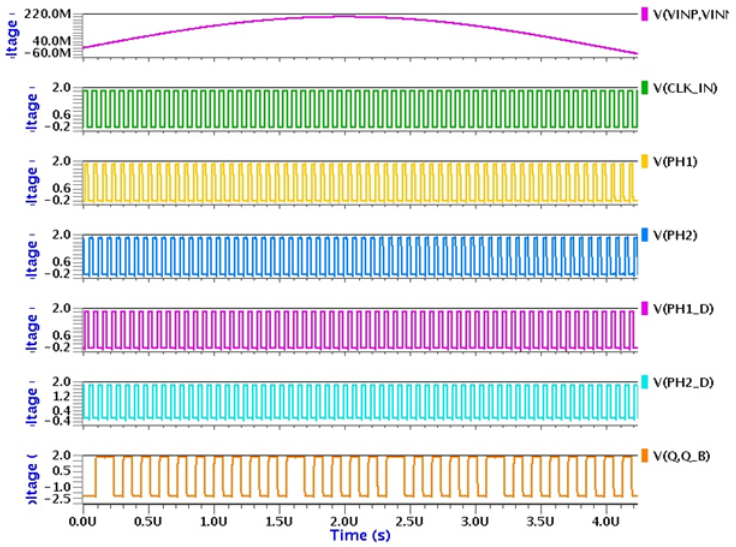

Figure 3.31: Discrete-time Second order Sigma-Delta modulator output

The modulator is simulated for input signals of 200mVpp and frequency of 7.2kHz.Vinp applied to negative terminal of the integrator and Vinn to the positive terminal of the integrator such that integrator has zero phase difference between its input and output.

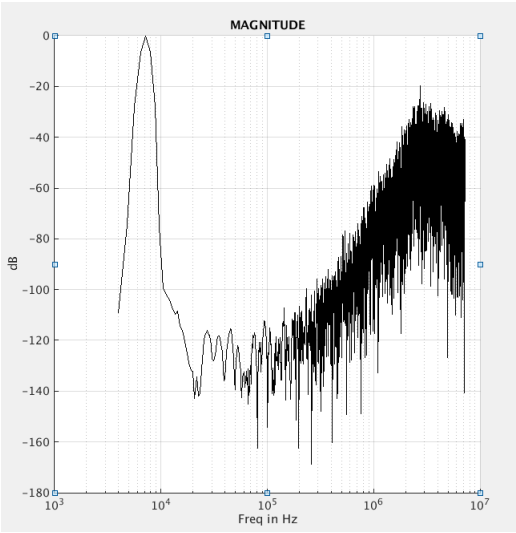

Figure 3.32: Output spectrum of 2nd order discrete time SDM

From the simulation result shown in Fig. (3.32) it can be concluded that the modulator can successfully convert analog input into its digital equivalent.The FFT spectrum of the digital output is carried out using MATLAB to calculate SNR and SNDR. The output spectrum of the modulated output is shown in Fig. (3.32). The performance metrics of the designed Sigma-Delta modulator is shown in Table (3.6)

Technology	cmos 28nm
Power Supply	1.8V
Order	2
Resolution	16
SNR	97dB
SNDR	86dB
Signal Bandwidth	28.8kHz
Power	0.3mW
Sampling Frequency	14.4MHz
OSR	250

Table 3.5: Performance matrix of 2nd order Discrete-time SDM

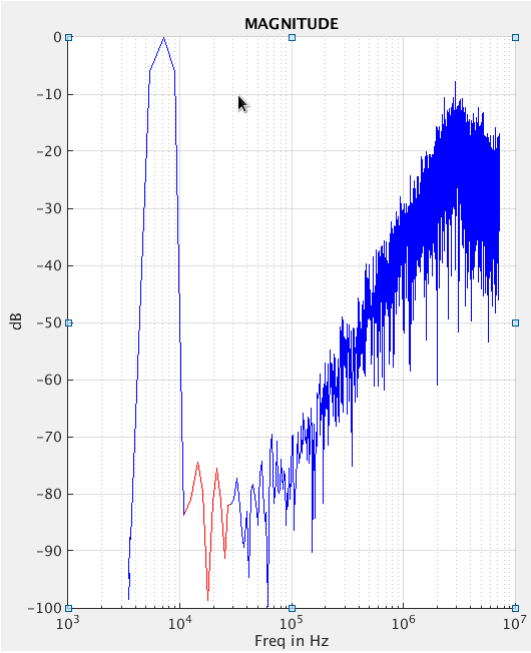

Figure 3.33: Output spectrum of 2nd order continuous time SDM

Technology	cmos 28nm
Power Supply	1.8V
Order	2
Resolution	15
SNR	92dB
SNDR	84dB
Signal Bandwidth	28.8kHz
Power	$270\mu W$
Sampling Frequency	14.4MHz
OSR	250

Table 3.6: Performance matrix of 2^{nd} order Continuous-time SDM

3.4.6 Input Common mode Compensation

The result of proposed input common-mode compensation circuit is shown in Fig. (3.34) .

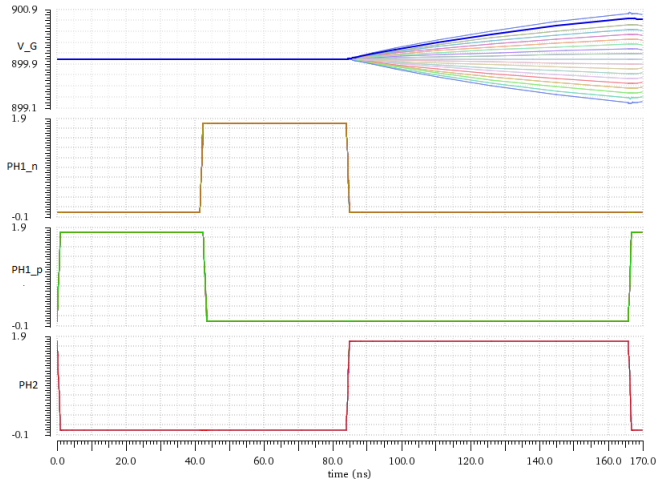

Figure 3.34: Effect of Input common-mode compensation circuit

The circuit model was simulated with input common mode bias is varied from 0 to V_{DD} . As it can be observed from Fig. (3.34) input common-mode at the virtual-ground node of the op-amp is almost remains at a fixed value of 0.9V with respect to variations in the common-mode at the input of the SDM . Hence , the proposed circuit model can be used to compensate for the input common mode variation. From the above discussion , the ICMR of the SDM can be increased to a wider range.

Chapter 4

Bias Generation

In our Sigma-Delta modulator we require reference voltage to define input and output DC level and reference current for biasing of operational amplifier. These reference should have little dependency on process, voltage and temperature.

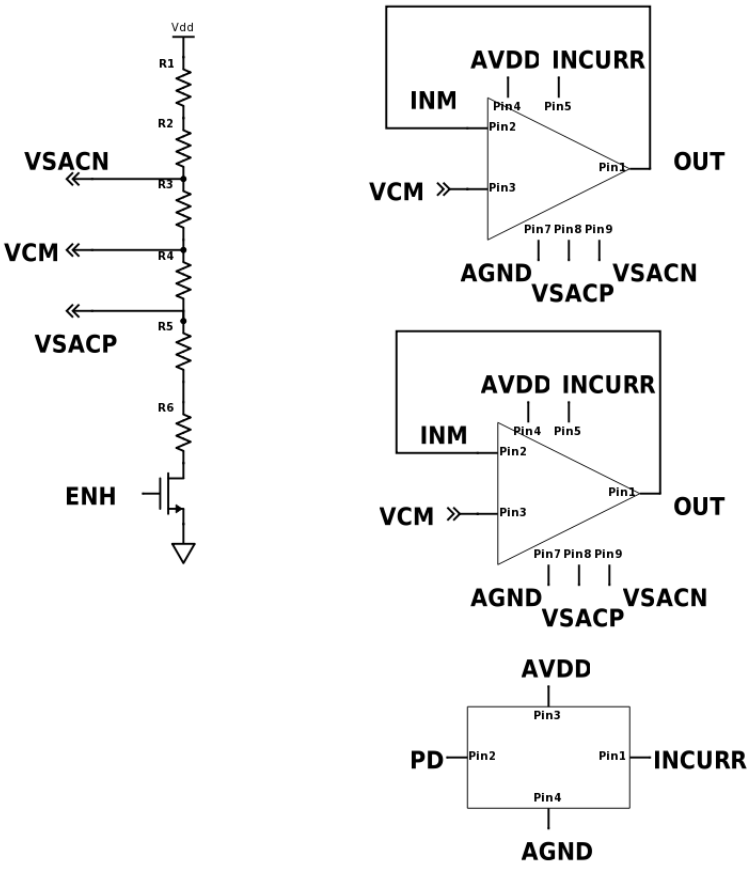

Figure 4.1: Bias generation circuit for Sigma-Delta modulator

Our bias circuit as shown in Fig. (4.1) consist of bandgap reference for current and two operational amplifier as buffer for common mode voltage generation for reference and input common voltage respectively. We will now study these three configuration in detail.

4.1 Bandgap Reference

The main operating principle of bandgap reference voltage is that if we add two quantities with opposite temperature coefficients(TCs) with proper weighting then we can generate zero temperature coefficient quantity.

4.1.1 Negative-TC voltage

The forward voltage of a p-n junction diode has negative temperature coefficient. Expression of TC can be obtained with the help of some readily-available quantities.

We can write I_c for any bipolar device as

$$I_c = I_s \exp(V_{BE}/V_T) \tag{4.1}$$

where

$$V_T = \frac{kT}{q} \tag{4.2}$$

The saturation current I_s is proportional to $\mu \mathrm{KTn}_i^2$ where μ is proportional to $T^{(\frac{-3}{2})}$ and n_i^2 is proportional to $T^3 \exp \frac{-E_g}{KT}$. Thus

$$I_S = bT^{2.5} \exp \frac{-E_g}{KT} \tag{4.3}$$

Where b is propotionality constant. We have

$$V_{BE} = V_T \ln(\frac{I_C}{I_S}) \tag{4.4}$$

When we calculate TC using (4.1),(4.3) and (4.4) then we can write

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - 2.5V_T - \frac{E_g}{q}}{T} \tag{4.5}$$

Equation (4.5) gives TC of V_{BE} for given T and revealing dependence on the V_{BE} itself. With $V_{BE} \approx 750\mathrm{mV} and T = 300 \circ K$

$$\frac{\partial V_{BE}}{\partial T} \approx -1.5 * \frac{mV}{\circ K} \tag{4.6}$$

4.1.2 Positive-TC voltage

The positive TC voltage quantity can be generated using difference of V_{BE} of two identical transistors($I_{S1} = I_{S2}$) having different current densities.

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{I_0}{I_{S2}} = V_T \ln n \tag{4.7}$$

Thus positive TC will be

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n \tag{4.8}$$

4.1.3 Bandgap Reference

Equations (4.6) and (4.8) represent negative and positive TC respectively. So if we add both with weighing then we can get

$$V_{REF} \approx 1.25V \tag{4.9}$$

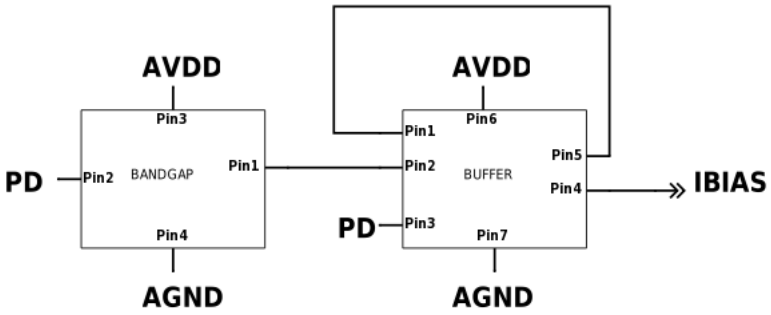

Figure 4.2: Bandgap and Buffer

In Fig. (4.2) we can see after bandgap there will be one buffer to prevent loading and output of buffer will be reference current. The schematic of bandgap reference is shown in Fig. (4.3), it can be seen that output of bandgap is VBG and it is applied to positive input of buffer. Schematic of bandgap can be divided in three part, first one is bandgap reference which is realised with *pnp* transistors and second part is start up circuit which is required to start working of bandgap and last one is rectifier from where we are taking output. The buffer is realised with two stage operation amplifier in feedback architecture. The operational amplifier is compensated using RC compensation. The output of buffer is VREF and a PTAT bias current.

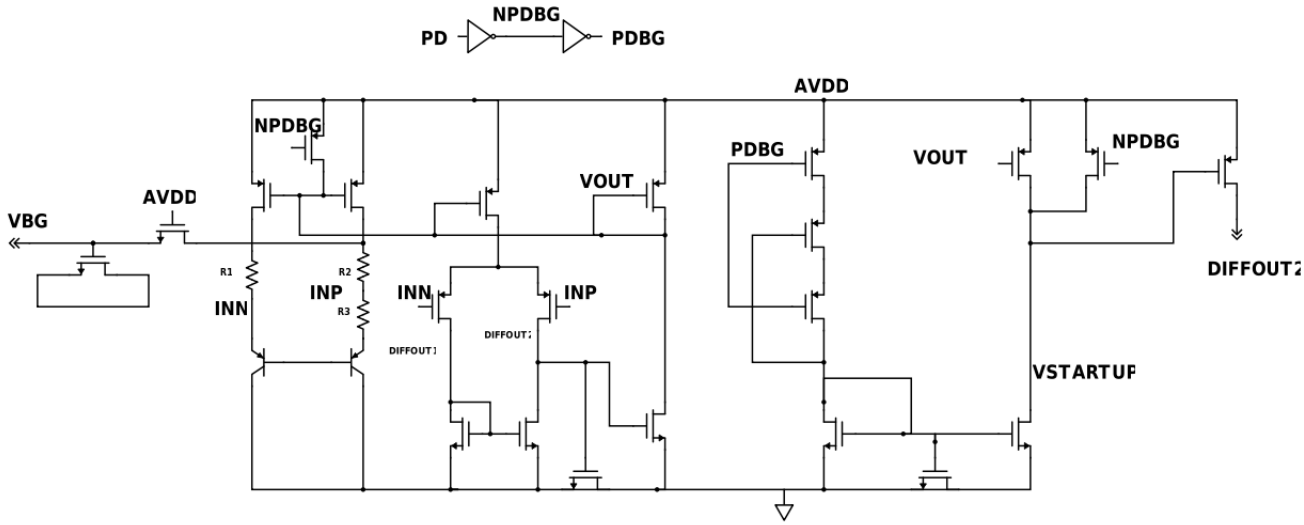

Figure 4.3: Schematic of bandgap reference

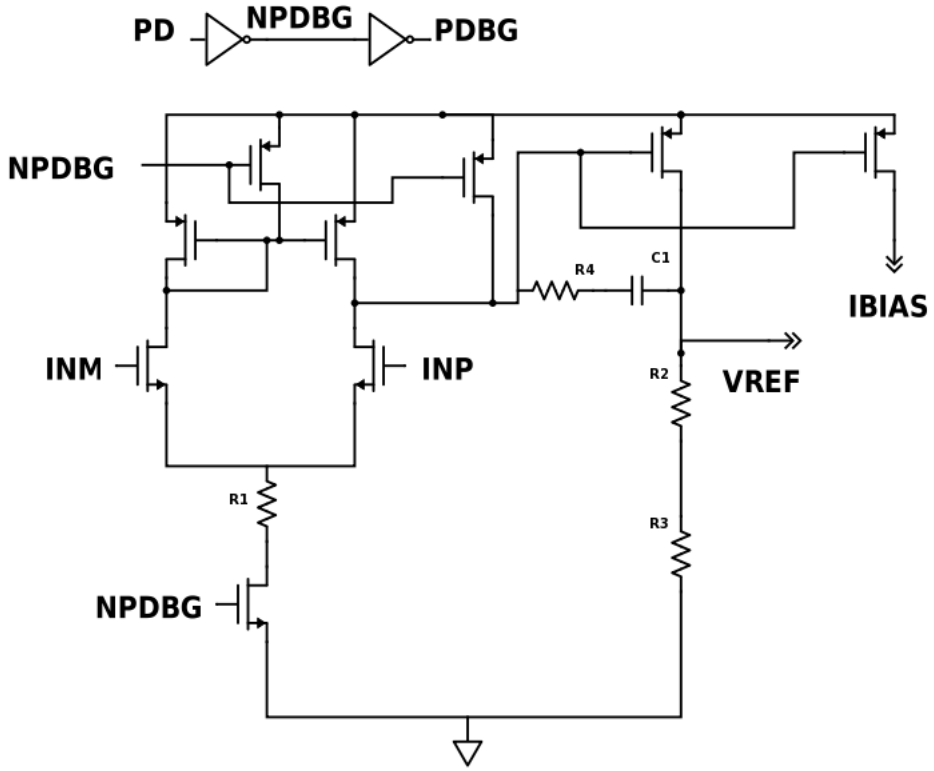

Figure 4.4: Schematic of buffer

The variation of reference voltage with temperature is shown in Fig. (4.5). It can be seen that

reference voltage is almost constant around temperature and there is only $3mV$ variation. The variation of Ibias with temperature is shown in Fig. (4.6) and it is constant with respect to temperature.

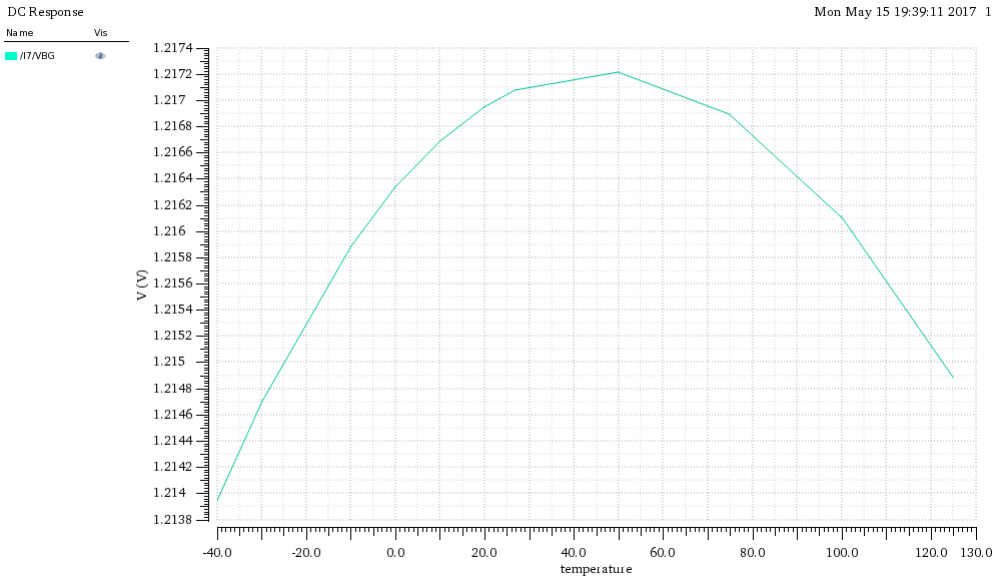

Figure 4.5: Variation of reference voltage with temperature

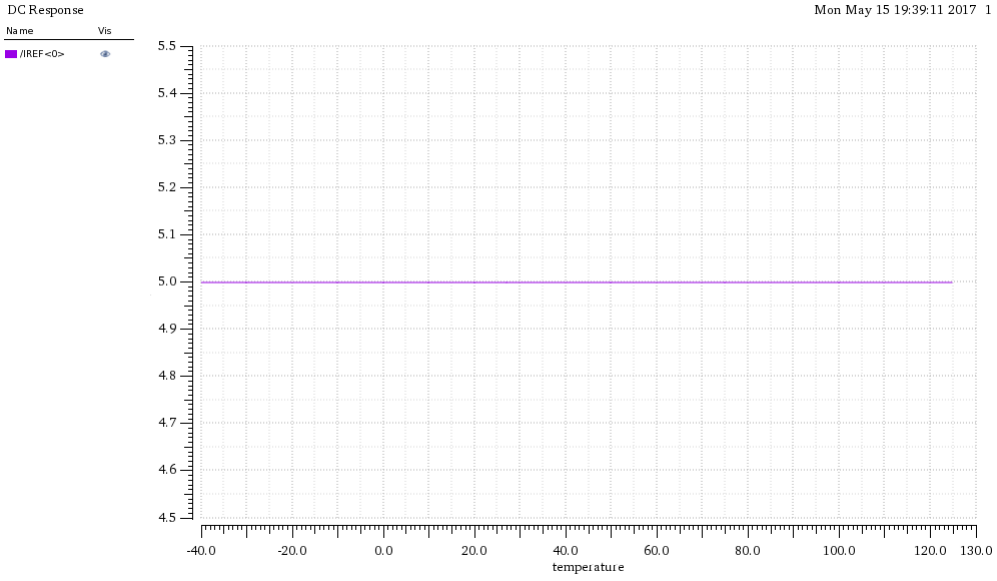

Figure 4.6: Variation of output current with temperature

The variation of output for any circuit with supply is represented by power supply rejection ratio(PSRR). The PSRR of our circuit is shown in Fig. (4.7). It can be seen from figure that PSRR of our circuit is 80 dB. This output current is applied as biasing current for operation amplifier used in our modulator.

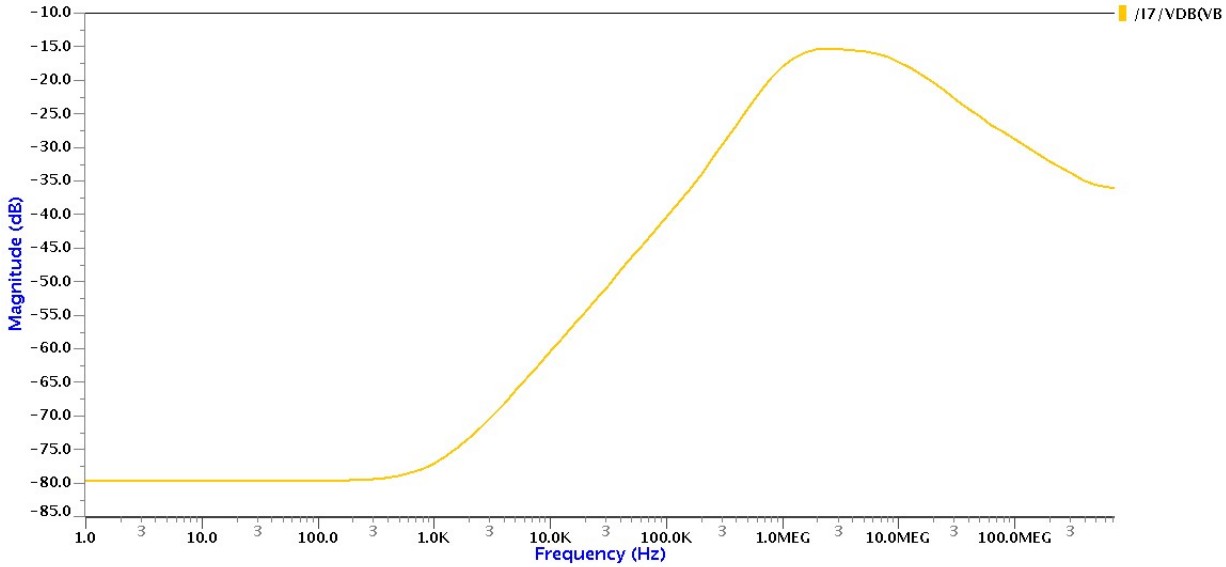

Figure 4.7: PSRR of bandgap with buffer

4.2 VDC generation for DC bias

Input signal for our modulator is AC signal so we require a DC bias across which we can apply our main signal. The DC bias is generated using resistor ladder as shown in Fig. (4.1) but if we apply this DC level direct to our modulator then there will be loading effect and this DC level will change abruptly so we add one buffer. Schematic of operation amplifier used in realisation of buffer is shown in Fig. (4.8). In the figure, biasing of operational amplifier is also given. We require two biasing voltages for NMOS and these are generated with help of current mirror and NMOS load. The buffer works on principle of virtual ground which is achieved by very high gain amplifier so we have used two stage operational amplifier. There are two stages so we have used RC compensation so that phase margin is positive and our system is stable. First stage of operational amplifier is simple five transistor circuit and second stage of operational amplifier is class B stage. The AC response of this operational amplifier is shown in Fig. (4.9). We are getting gain of 75 dB with unity gain bandwidth around $55MHz$.

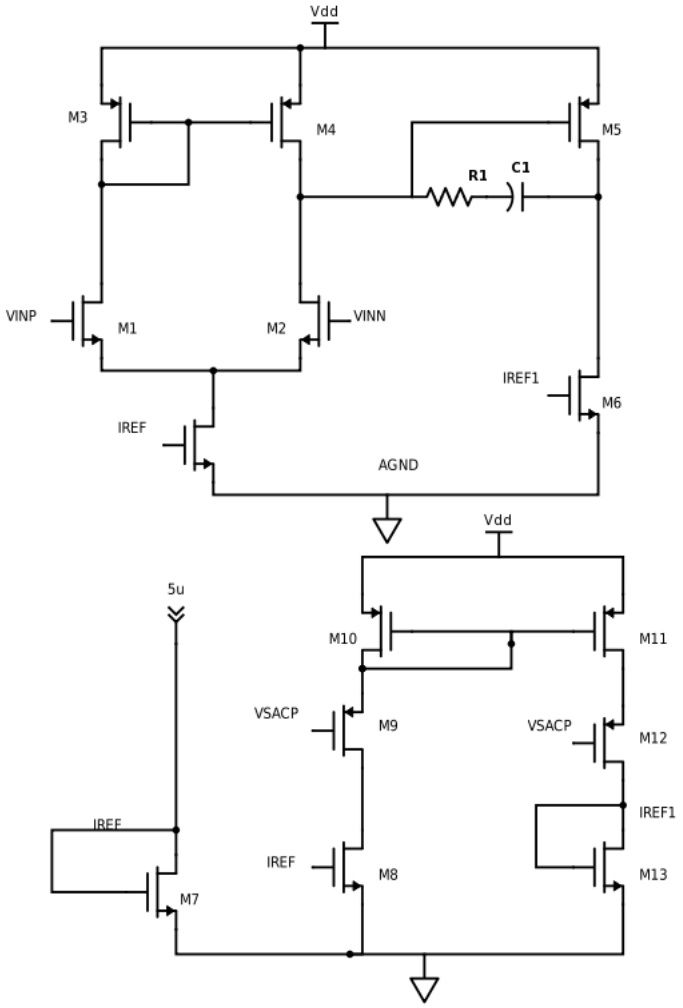

Figure 4.8: Schematic of operational amplifier used as buffer for DC level generation

The phase margin of operational amplifier is around 74°. In the Fig. (4.10), variation of offset which is difference of level generated using ladder circuit and output level of operational amplifier is shown using Monte-Carlo simulation. The mean of offset is $0.20535mV$ and standard deviation of 3.20 mV. Monte-Carlo simulation is done for 100 samples. Maximum and minimum values of offset are 6.86495 mV and -9.58651 mV respectively.

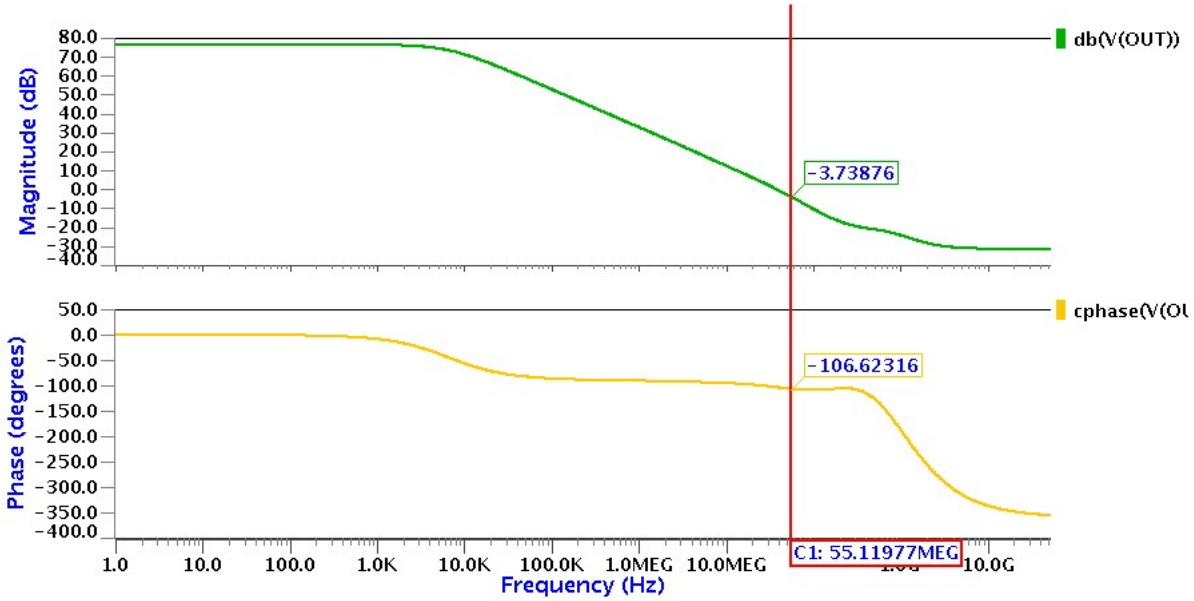

Figure 4.9: AC response of operational amplifier used as buffer for DC level generation

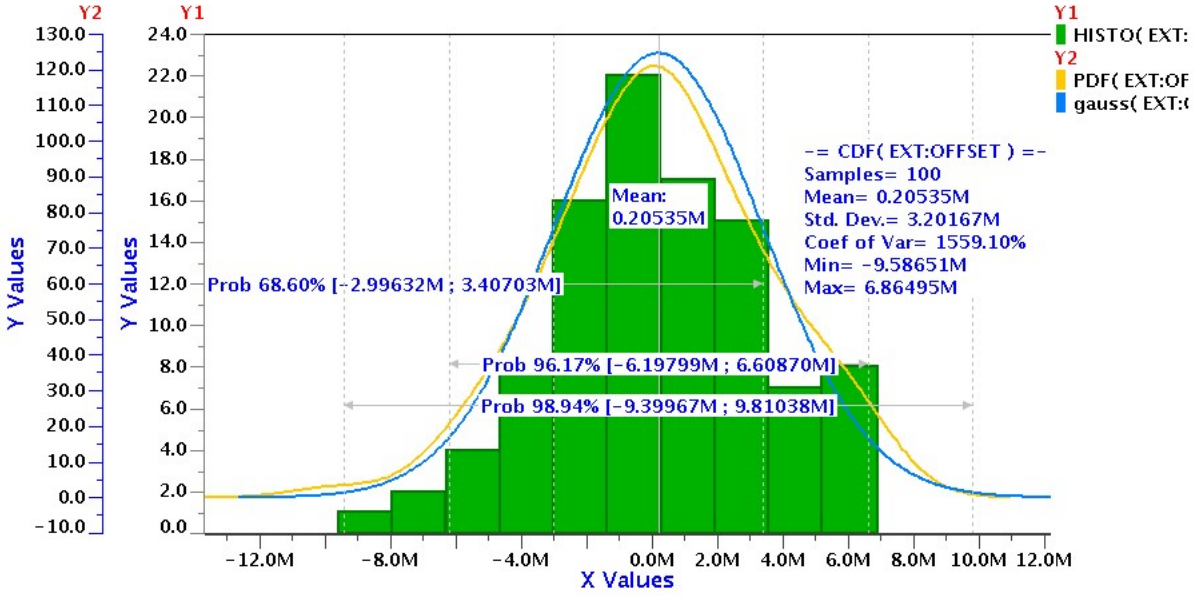

Figure 4.10: Gaussian spectrum of offset for operational amplifier used as buffer for DC level generation

4.3 VCM generation for DC Reference

In discrete time Sigma-Delta modulator we require a reference voltage for switch capacitor circuits so that variation of voltage swing can be minimised. This VCM is connected in main modulator so noise of VCM generation circuit should be low as well as it should also have high swing so we have used class-AB operational amplifier with Monticelli biasing. The schematic of operational amplifier is shown in Fig. (4.11). The biasing of this operational amplifier is done as shown in

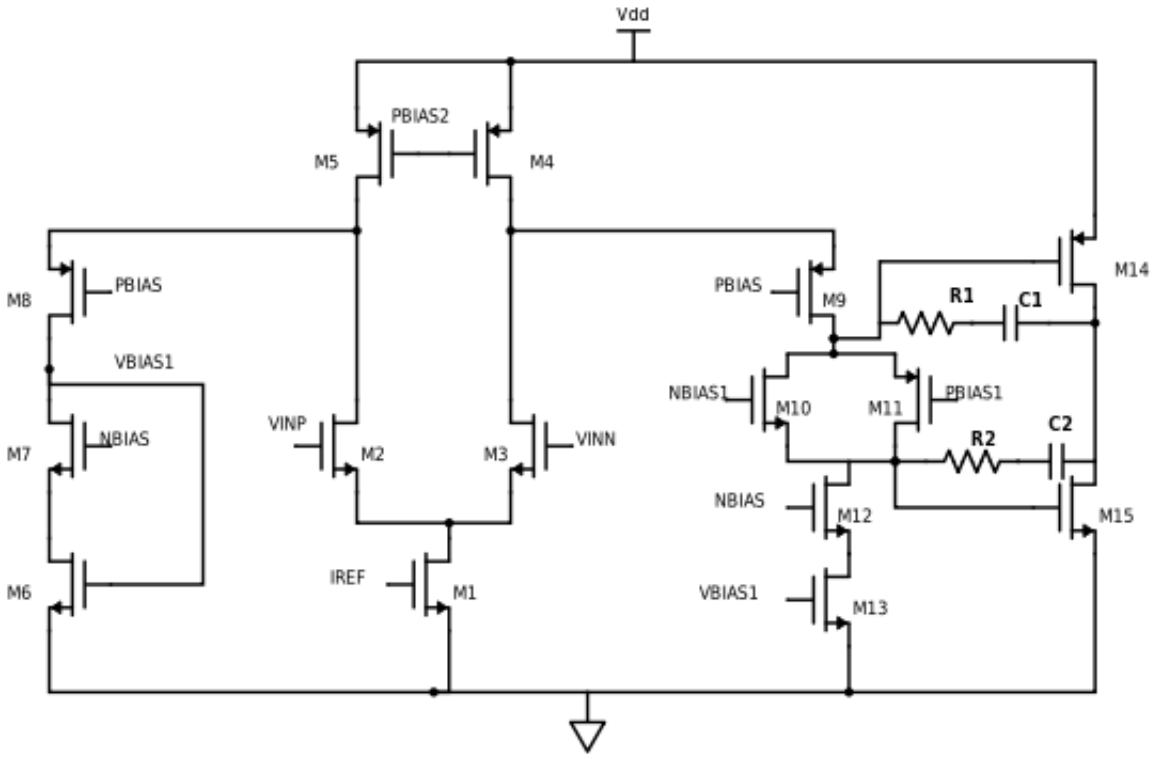

Figure 4.11: Schematic of class-AB operational amplifier

Fig.(4.12). The biasing of this operational amplifier is also a big challege as there are three same type of transistors are connected in series. In the schematic of opamp transistor M10 and M11 called as Monticelli transistors require bias level of $V_{gs} + 3V_{th}$ so we are generating bias for this transistors by two NMOS and PMOS load so this level will have $2V_{gs} + 2V_{th}$ and we can adjust aspect ratio such that it can be equal to $V_{gs} + 3 * V_{th}$ value.

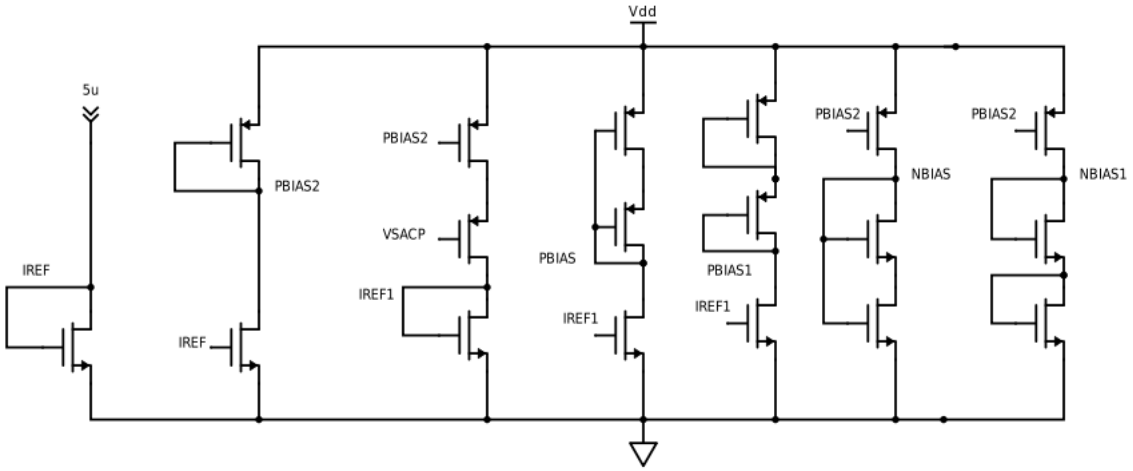

Figure 4.12: Bias generation circuit for class-AB operational amplifier

The AC response of this operational amplifier is shown in Fig. (4.13). It has DC gain of 107 dB and unit gain bandwidth around 22 Mhz with phase margin of 64°.

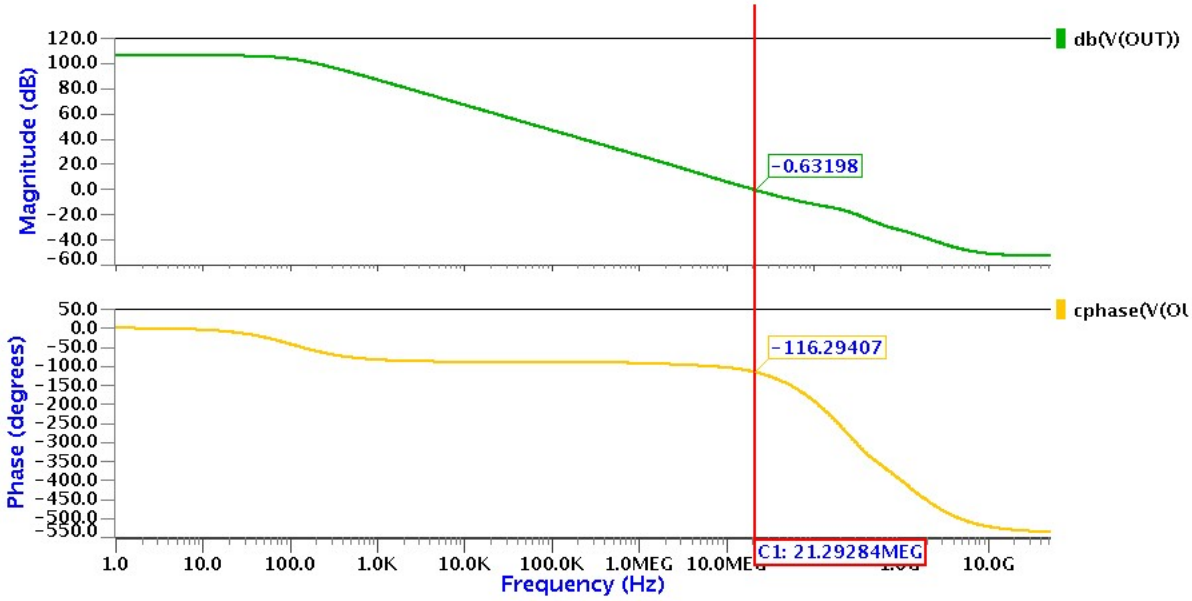

Figure 4.13: AC response of class-AB operational amplifier

In the Fig. (4.14), variation of offset which is difference of level generated using ladder circuit and output level of operational amplifier is shown using Monte-Carlo simulation. The mean of offset is 1.18783mV and standard deviation of 3.92mV. Monte-Carlo simulation is done for 100 samples. Maximum and minimum values of offset are 9.97mV and -9.60402 mV respectively.

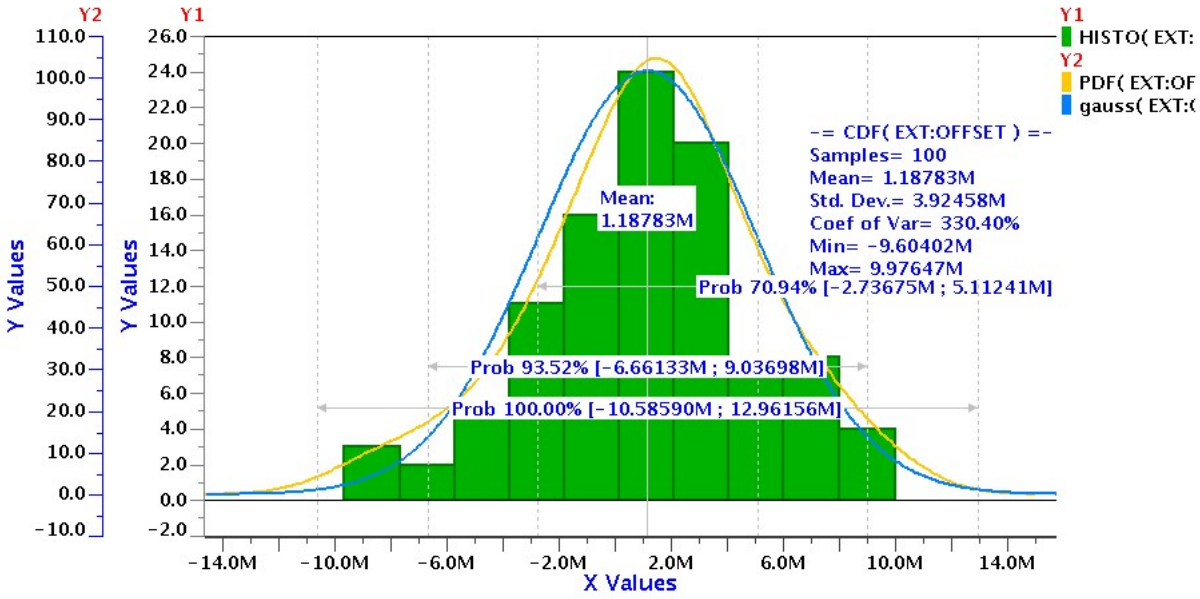

Figure 4.14: Gaussian distribution for offset of class-AB operational amplifier

Chapter 5

Conclusion and future scope

5.1 Conclusion

In this thesis work an effcient discrete-time and continuous-time Sigma-Delta modulator design has been presented, which met the desired performance specifications suitable for audio-applications. The differential mode discrete-time and continuous -time second-order modulator design was implemented in 28nm for a supply voltage of 1.8V. The design was able to meet the required specifications of SNR 97dB, Resoultion of 16-bits and power consumption of around 0.3mW for Sampling frequeny of 14.4MHZ and Bandwidth of 28.8KHz in discrete-time and SNR of 92dB, Resoultion of 15-bits and power consumption of around 250 μW for Sampling frequeny of 14.4MHZ and Bandwidth of 28.8KHz in continuous-time. The behavioral modeling simulations gives the importance of behavioral modeling in any Analog and Mixed signal design. The simulation of the model with added non-idealities and noise gives an intuition of circuit behavior and suitable modifications can be be made before starting with the circuit design. Behavioral model simulation of the SDM was performed using Verilog-AMS. From the circuit simulation of the modulator, it was analysed that loop filter performance plays vital role in the overall performance Sigma-Delta modulators. The integrator output has dependency on the reference voltage and input voltage variations. This dependency leads to the harmonics in the output spectrum which may degrade the modulator performance if the issue is not addressed. Also the OTA gain used in the integrator is chosen to be high such that noise floor at the output is limited. The non-linearity in the output due to input-common mode variation can be compensated by the proposed model of input common-mode compensation technique.

5.2 Future scope

Future scope of work is to address the non-linearities [10] in the design and to optimize it. The non-linearities are Reference voltage variation causing distortion in the output and harmonics introduced by the Transmission gate switches whose ON resistance varies with the input signal. So a switch with full-swing, constant ON resistance is necessary with reduce harmonics. Also the current design can optimized for higher resolution.i.e., by using multi-bit ADC and DAC.

Table 5.1: Comparison of proposed Sigma-Delta ADC with state-of-the-art designs

Work	Process (nm)	Frequency Band-width (MHz)	ENOB	Power(mW)	Order	FOM(dB)
[2]	CMOS 130nm	5	15	9	3	177
[3]	CMOS 180nm	.312	17	58.5	4	168
[4]	CMOS 180nm	6	10	6	4	150
[5]	CMOS 180nm	1.92	10	2.8	3	148
[6]	CMOS 180nm	1.9	13	8.1	3	161
[7]	CMOS 180nm	5	15	2.3	3	183
This work, DT	CMOS 28nm	0.03	16	0.3	2	186
This work, CT	CMOS 28nm	0.03	15	0.27	2	188

SNR: Signal to noise ratio, sim: Simulated results FOM: FIgure of Merit

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