High Voltage Tolerant ESD Protection Circuit for Plug and Play Devices

by

Mranal Kulshreshtha

A thesis submitted in partial fulfillment for the
degree of Master of Technology

under supervision of
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Certificate

This is to certify that the thesis titled "High Voltage Tolerant ESD Protection Circuit for Plug and Play Devices" being submitted by Mranal Kulshreshtha (Roll No.- MT16098) to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original work carried out by him under my supervision. In my opinion, thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The results contained in the thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

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Abstract

ESD (Electrostatic Discharge) protection circuits are widely used in the semiconductor industry generally as on-chip solution to protect main circuit or Design Under Test (DUT) against electrostatic discharge. This electrostatic charge can be accumulated due to number of reasons such as mis-handing of machinery equipment, charge transfer from human body etc. If this charge is not bypassed, then it might result in the permanent failure of core integrated circuits or DUTs. Therefore, some efficient circuit design must be placed to discharge this high ESD stress. Typically, Electrostatic charge is in the range of kV, hence large sized devices are needed to discharge this high voltage. In addition to this, bias voltage stress above 1.8 V may lead to device breakdown in lower technology nodes such as 16 nm FINFET technology in spite of its unique advantage of allowing high speed operation with low power consumption. The major design challenges in designing ESD protection circuits are clamp area, which is the major area hungry block, high inrush current due to large sized devices, hot insertion problem and false triggering issues.

In the state of art, existing ESD protection circuit are not able to survive for high voltage in sub-micron technology as it may lead to oxide breakdown due to low thickness. Further, these circuits are more sensitive to the hot insertion. In order to mitigate these design challenges, high voltage tolerant cascoded ESD protection circuit is proposed with a supply voltage of 3.3 V using 16 nm FINFET technology for devices such as flash drives, mobile devices etc. This circuit is designed keeping all constraints in mind such that the voltage stress across any device should not go beyond 1.8 V, which is breakdown voltage for the device. This ESD protection circuit can support 4 kV HBM and least inrush current in normal power on condition for specification of 10 mA per instance. This proposed design has reduced the clamp area around 38 % and static current approximately 4 times as compared to the baseline circuit. This design supports plug and play feature, which generally suffers from hot insertion problem. Simulation results shows that the proposed design is robust against PVT variations.

Acknowledgements

I would like to thank my supervisors Dr. Pydi Ganga Mamba Bahubalindruni and Mr. Shiv Mathur for their guidance and corrections made in the scope of this work.

This work is dedicated to my parents Mr. Jaideep Kulshreshtha and Mrs. Abha Kulshreshtha for their teachings and values passed on to me. I thank their understanding even in those moments in which my immaturity prevailed. To my sister Yashi Kulshreshtha for all her support and friendship throughout these years.

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Dedicated to my beloved parents...

Chapter 1

Introduction

1.1 Background

With the advancement in scaling down the semiconductor technology, designing of Input/Output (I/O) circuits is becoming more challenging with the relatively thinner gate oxide. I/O circuits are placed at the periphery of chip and work as an interface between chip and outside world. In this modern era when speed and efficiency of the circuitry is increasing exponentially, matching of I/O circuits becomes more critical. Typical goals of I/O circuit design involves high current driving capability, voltage level shifting, efficient receiver and transmitter, impedance matching, ESD protection and high voltage tolerant design.

ESD is basically defined as transfer of charge between two different objects maintained at different potential. ESD events are natural ones and can be easily observed in our daily routine e.g. a person is walking on dry carpet and suddenly touches a metal door knob results in brief mild shock. ESD events generally results in mild shocks to human beings however, if the IC is subjected to same ESD stress, it may result into the permanent damage of an IC. ESD events are different than normal power up pulses in terms of faster rise time and higher peak voltages. ESD events involves high voltage up to several KV and high current up to 10 A on small devices. ESD events comes for very short interval and thus they impose reliability concern for semiconductor industry. To ensure reliability, ESD must be controlled through all phases of devices life cycle [5]. Designing of ESD protection circuits becomes more challenging as technology node shrinks due to thinner oxide and hence chances of IC damage increases because of higher current density and lower supply voltage tolerance. There are two main consequences of ESD/EOS (Electrical Overstress). One is breakdown of gate oxide due to high voltage

during ESD event and other is excessive heat generated by carriers result in device failure [7].

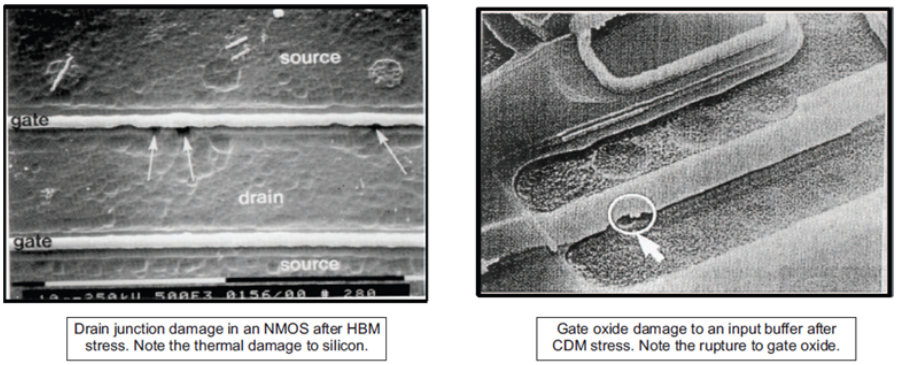

FIGURE 1.1: ESD failure in an IC (a) Faliure due to HBM stress (b) Failure due to CDM stress [copyright by ESD Association].

With the trend of scaling down CMOS process nodes, ESD has been a major reliability concern in the semiconductor industry [8]. Typically, modern ICs with lower technology nodes have thinner oxide layers due to the technology scaling, which makes ESD protection circuits as unavoidable building blocks. It has been reported that around 35 % of IC failures are just because of ESD failure with an estimated cost of several billion dollars for IC industry [9]. Fig. 1.1(a) and Fig. 1.1(b) shows the junction damage of device under HBM (Human Body Model) stress and oxide damage under CDM (Charged Device Model) stress respectively. One important concern for ESD circuits in plug and play devices is the hot insertion effect. Hot insertion or hot plugging refers to the addition or removal of any extra component without stopping or shutting down the system. For plug and play devices such as flash cards, this effect is prominent. Huge amount of current flows through an IC when such devices are added or removed without shutting down the power supply.

Though reduction of supply voltage is slowing down with the technology scaling, the decrease of ESD transistor breakdown voltage is still significant in lower technology nodes. Consequently, it is becoming quite challenging to design robust ESD circuits. The increase in number of gates on the chip can be accomplished by shrinking the size of the device. As per Rent's Rule, if number of devices are increased, it will correspond to an increase in the number of I/O pins required. This increases the ESD susceptibility of future integrated circuits [10]. Physically smaller devices are more vulnerable to ESD damage than larger devices. Increase in the total number of I/O pins and power supply increases the chance of an ESD. Thus, ESD can be seen as a major concern for the semiconductor industry in the coming future.

There are different ways to reduce IC failure resulting from ESD. One approach to limit ESD failure is to ensure proper handling and grounding of workforce and equipment

Table 1.1: Electrostatic charge stored for different events [4].

Event	**Average voltage stored (V)**
Person walking across linoleum floor	5000
Person walking across carpet	15000
Ceramic dips in plain plastic tube	700
Ceramic dips in plastic set-up trays	4000
Circuit packs as bubble plastic cover removed	20000
Circuit packs (packaged) as returned for repair	600

during the manufacturing and packaging of integrated chip. Another important way to reduce ESD failure is to connect ESD protection circuits to the periphery of an IC, which will take away all the high current and clamp the high voltage during ESD event and thus ESD protection circuits are important [11].

1.2 Motivation

In todays era, ESD protection circuits are vital in IO periphery. As already discussed, around 35 % of the total IC failures are resulting from ESD. Thus, ESD failure has significant impact on reducing the actual yield of semiconductor ICs. During the wafer-fabrication process, uncontaminated rooms can generate charge over 20 kV [3]. Electrostatic charge generated for some events are presented in Table 1.1 [4]. The electrostatic charge can also be generated during the transportation of these wafers, which can damage thin gate oxide. The ESD hazards can also be present during the assembling of an IC. ESD events may occur during all these operations and results in IC failure.

In todays world, gate oxide thickness has been reduced to few angstrom to realize high switching speed. With the technology scaling, thinner gate oxide has made the chip more vulnerable to ESD damage because of oxide breakdown due to high electric field. As operating frequency is increasing, the I/O pad parasitic capacitance is influencing the delay of driving gates. Hence, parasitic capacitance should be as small as possible [12]. Further, hot insertion problem in plug and play devices is becoming more prominent. Many IC failures are reported due to the addition or removal of devices without turning off the power supply. Thus, a circuit must be designed that does not allow huge current flow to support the plug and play feature. A chip manufacturer has not much control over a customers handling of its product, so it is essential to incorporate effective ESD protection circuitry. As the spectrum of device stress under ESD is wide and the amplitude of stress is not actually limited, to ensure total ESD immunity is not possible. However, the threshold of sustainable stress can be significantly increased through the

proper design of ESD protection circuit, which results in improved reliability of semiconductor ICs. With all these constraints, ESD protection circuit design becomes more difficult and significantly important.

1.3 Thesis outline

There are still many challenges in the ESD design engineering inspite of significant progress that has been made in understanding ESD related issues [10]. The main objective of this thesis is to design a high voltage tolerant clamp based ESD protection circuit for plug and play devices. The goal of this thesis is to improve design for higher reliability of ESD. Several state of art techniques have been studied and incorporated within the design to address the open design challenges such as clamp area, high inrush current and hot insertion problem mainly with sub-micron technologies. Use of FINFET 16 nm technology has been emphasized because it represents the leading edge of the semiconductor industry nowadays. This thesis primarily introduces the behavior of ESD events and circuit's design challenges.

This research work has been primarily focused on improving the state of art ESD design challenges, which majorly includes clamp area, static current, hot plugging problem and inrush current. Several techniques have been studied and implemented to ensure immunity for false triggering, latch up robustness and to support plug and play feature.

As per industry standard to support mobile devices, flash drives etc., the specifications for the supply voltages ranges from 2.7 V to 3.6 V and inrush around 10 mA per instance. The common test methods namely HBM (Human Body Model), MM (Machine Model) and CDM (Charged Device Model) have been studied and verified with different zapping modes. As per TSMC 16 nm FINFET datasheet, the thermal breakdown of the device under ESD (transient) condition is 3.94 V.

This proposed ESD protection circuit for aforementioned specifications has been designed in 16 nm FINFET technology. Its performance has been compared with state of art work. An RC network is designed to ensure clamp remains active till the complete ESD stress discharges for the given size of a clamp device. If RC delay is small and clamp size is not sufficient, then it may result in the large voltage build up across the device, which may further cause oxide breakdown. This proposed circuit is able to address the existing design challenges of ESD circuit. This circuit can support the supply voltage range from 2.7 V to 3.6 V inspite of using 1.8 V device and minimum ramp rate of 70 ns in normal power on condition. Further, this proposed work is able to overcome the situation of false triggering and hot insertion. Its robustness has been

verified against different PVT variations from the simulation, whose outcome has been presented in chapter 6.

1.4 Structure of the Work

In this chapter, we have discussed about behavior of ESD/EOS event, motivation behind ESD protection circuit design and their design challenges with scaling of technology nodes. Further, we have discussed the thesis outline and objectives. Rest of the thesis work is organized as below:

- **Chapter 2: ESD Protection Methods**
  This chapter gives an insight on various ESD protection methodologies, such as snapback and non-snapback based protection and their comparisons.
- **Chapter 3: ESD Protection Methods and Devices**
  This chapter discusses about various ESD protection devices used by an IC industry. It contains brief description about snapback and non-snapback devices. It also describes the usage of these devices for different ESD environment.
- **Chapter 4: ESD Test Models**
  This chapter describes different standard ESD test models to verify the circuit robustness. These models include HBM, MM and CDM, where ESD events have been simulated by these test models to depict real ESD environment.
- **Chapter 5: ESD design techniques**
  This chapter presents proposed ESD protection circuit design, techniques incorporated and its detailed analysis.
- **Results**
  This chapter shows the results of the proposed ESD protection circuit, comparisons of different ESD techniques at different PVT conditions.
- **Conclusions**
  This chapter concludes all the outcomes and contributions of this dissertation and also highlights possible future work to improve the ESD performance of the existing circuit.

Chapter 2

ESD Protection Methods

This chapter presents ESD protection methodologies that are widely used in semiconductor industry to protect on chip ESD. Section 2.1 discusses the different zapping modes, which can be applied across the IC to verify the ESD condition. Then, section 2.2 majorly focuses on on-chip ESD protection methodologies.

2.1 ESD zapping modes

IC pins are majorly categorized into three namely V_{DD} pin, V_{SS} pin and I/O pin. Generally we have four possible zapping modes for an ESD event depending on the polarity of electrostatic charge and the discharge path in the IC. These typical modes are known as PS-mode, NS-mode, PD-mode and ND-mode [13]. These zapping modes are presented in Fig. 2.1 [1], which represents the polarity of an ESD event with respect to the power supply pin (V_{DD}) or ground pin (V_{SS}).

In PS-mode zapping method, a positive ESD voltage is applied at the I/O pin of the chip and V_{SS} pin must be grounded as shown in Fig. 2.1 (a). All other pins will remain floating including V_{DD}. Whatever ESD voltage is applied at the I/O pin, it must discharge through V_{SS} pin effectively. Similarly in the NS-mode of ESD zapping, a negative ESD voltage is applied to the I/O pin of an IC with V_{SS} remain grounded as shown in Fig. 2.1 (b) and rest of the conditions are same as mentioned in the previous zapping mode. In this method, ESD voltage must be completely discharge through V_{SS} pin. Third zapping mode is PD-mode in which positive ESD voltage is applied at I/O pin and V_{DD} pin must be grounded as shown in Fig. 2.1 (c). Whole ESD event must discharge through V_{DD} pin of an IC. Fourth and last method is ND-mode in, which negative ESD zap is applied at I/O pin with V_{DD} as ground as shown in Fig. 2.1 (d). Rest other pin will remain floating and ESD must discharge through V_{DD} pin.

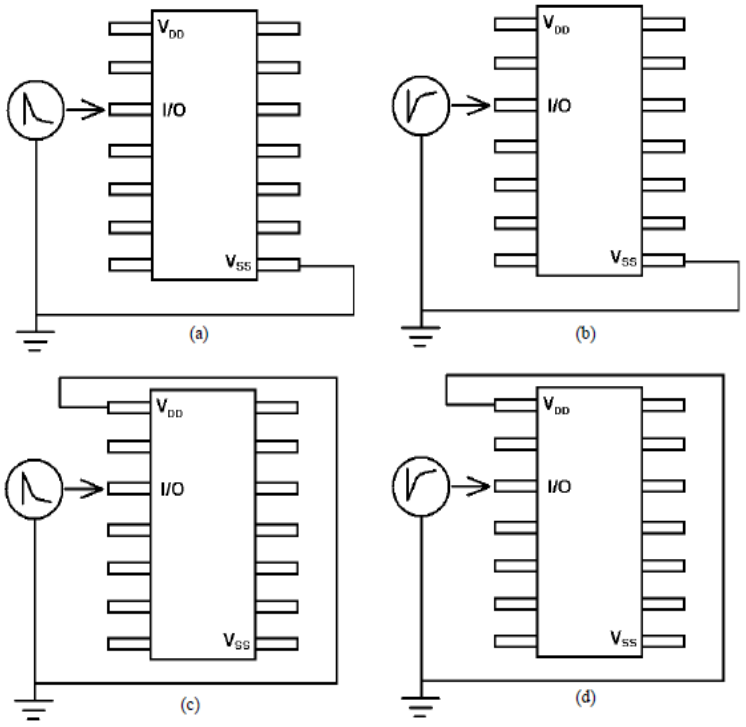

FIGURE 2.1: ESD zapping modes (a) PS-Mode (b) NS-Mode (C) PD-Mode (d) ND-Mode [1].

The maximum ESD tolerant voltage is decided by the minimum ESD threshold among the four zapping modes discussed above. Assuming that PS, NS and ND-mode has 4kV as ESD threshold but, PD-mode has 1 kV as ESD threshold, then final ESD tolerant voltage would be 1 kV. In lower technology nodes, we have to ensure that ESD event discharges through both V_{DD} and V_{SS} pins for large size IC having longer power rails, which offer high parasitic capacitances.

2.2 ESD Protection Methodologies

During fabrication, shipping and handling of an IC, the ESD related reliability problems may occur. As already discussed that almost 25% - 35% failures of an IC are ESD induced failures [9], hence ESD events should be protected to increase the manufacturing yield by reducing the total cost and improving the reliability of an IC. Generally, there are two ways to reduce IC failures induced due to ESD conditions. The first way is to reduce the amount of ESD induced charges during fabrication and handling of semiconductor ICs and redistributing them through proper handling of equipment and personnel. The second approach is to design on-chip ESD protection circuits to improve the ESD robustness of the integrated circuit.

From the previous discussion, it is clear that ESD protection circuit must be placed between V_{DD} and V_{SS} rail lines to avoid thermal breakdown at ESD condition. The major functionality of ESD protection circuits is to limit down the I/O pad voltage below the thermal breakdown of the gate oxide by bypassing the ESD current [14]. There are certain on-chip ESD protection methodologies, which provides complete protection against all the ESD zapping modes. In more complex ICs, more than one ESD protection circuits should be added between power supply pads as well where more than one supply voltage exists.

2.2.1 Snapback based ESD protection

Majorly, there are two types of ESD protection methodologies. Among them, most popular is snapback based ESD protection mechanism. The first approach to provide protection against ESD stress is to add a protection circuit between I/O pad and V_{SS}. This ESD protection circuit should be capable enough to handle a large amount of current under ESD conditions, while having least impact on the normal behavior of the circuitry. Fig. 2.2 shows the protection scheme and also the discharge path is highlighted.

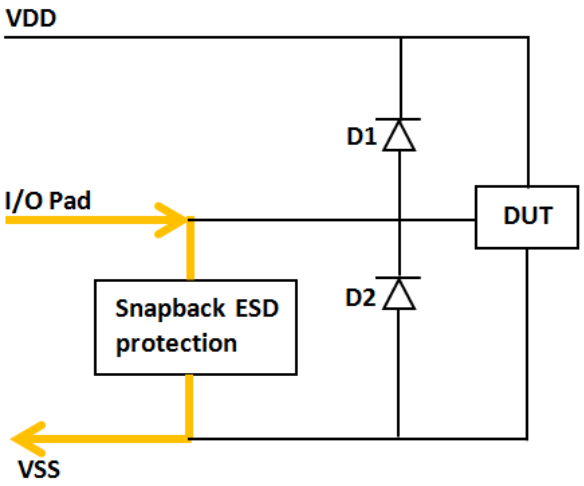

FIGURE 2.2: Snapback based ESD Protection.

It can be observed that an extra block refer to as PS-mode protection is added in parallel with the diode D2 as shown in Fig. 2.2. As we considered the zapping mode as PS-mode, thus ESD protection block has been placed between the I/O pad and V_{SS} pin of the chip. For ND-mode protection, a similar kind of circuit should be added between I/O pad and V_{DD} pin (in parallel with the diode) to discharge the ESD stress. Similarly, different ESD protection can be added for NS-mode and PD-mode [4].

In snapback based ESD protection method, the ESD protection circuit is designed using avalanche junctions. These circuits are generally designed using snapback based devices. Silicon Controlled Rectifier (SCR) is the most popular devices, which falls under the category of snapback device and are used as the protection circuit. Snapback devices operate in their breakdown region under ESD conditions. Their breakdown has a snapback characteristic curve, hence this method is called as snapback protection method. Detailed discussion regarding snapback devices and their characteristics will be presented in the later chapter.

2.2.2 Non-snapback based ESD protection

In addition to the previously discussed snapback-based ESD protection methodology, ESD protection can also be realized by transferring the charge induced due to the ESD event to the V_{DD} node using the forward-biased diode D1 as shown in Fig. 2.3. After this, the induced ESD charge is completely discharged to V_{SS} pin through another ESD protection circuit, which is known as ESD clamp. This method is called non-snapback protection scheme because the ESD clamp should work without going into the avalanche breakdown and hence snapback curve cannot be realized. Non-snapback ESD protection topology is shown in Fig. 2.3 and discharge path for the ESD event is also highlighted [4].

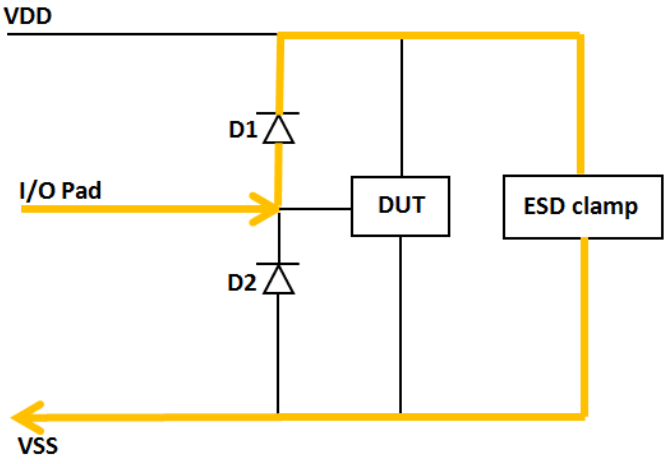

FIGURE 2.3: Non-Snapback based ESD Protection.

This type of ESD protection involves ESD clamp, which is supposed to turn on at the time of an ESD event to completely discharge the ESD voltage. Generally, bigger NMOS clamp is used as an effective ESD clamp circuit to clamp down the voltage to the V_{SS} pin. In addition, this topology requires an RC network to detect the high rising pulse of an ESD event and accordingly turn on the clamp device to discharge the ESD stress. For ND-zapping mode, the ESD current will be discharged through the forward-biased diode

D2 as shown in Fig. 2.3 and the ESD clamp circuit. For this protection methodology, just one clamp circuit is required, which is placed between V_{DD} and V_{SS} rails and can be shared among all other I/O pins on the chip [15].

2.2.3 Comparison between snapback and non-snapback ESD Protection

As previously discussed, there are generally two types of ESD protection methodologies. One is snapback based and another one is non-snapback based protection scheme. Each of them has their own pros and cons. Some of them are listed below:

Snapback based ESD protection

- Snapback based ESD design is immune to the false triggering as no delay element is present to detect the ESD event.
- It is not stable as device has to be operated under avalanche breakdown during an ESD event.
- It is much sensitive to process and layout variations.
- Some bulky device level simulators are needed to verify the performance.
- It cannot be designed with minimum design rules.

Non-Snapback based ESD protection

- These ESD design are sensitive to false triggering as RC delay element is present to detect the ESD event.
- This design is stable due to the presence of ESD detection network and trigger circuit, which is controlling the state of clamp.
- Relatively, it is not much sensitive to layout and process variations.
- Simple SPICE simulations are needed to verify the performance.
- It can be easily designed with minimum design rules.

2.3 Summary

A detailed description about ESD protection methodologies has been given in this chapter. Further, snapback and non-snapback based ESD protection mechanism has been explained. In the next chapter, a detailed version of different ESD protection devices will be presented, which is generally used by the semiconductor industry for the on-chip ESD protection.

Chapter 3

ESD Protection Devices

In this chapter, we have presented the detailed description of the ESD protection devices available in the industry based on ESD protection methodologies. These devices are majorly categorized into two types namely snapback and non-snapback devices. An overview of these devices have been given in the later section of this chapter.

3.1 Snapback devices

As already discussed in the previous chapter, snapback devices are those devices, which are used in the avalanche breakdown region during an ESD event. This chapter will briefly cover the different types of snapback devices, which are generally used in the semiconductor industry. The most commonly used snapback devices are modified versions of MOSFET and SCR (Silicon Controlled Rectifier).

Though, diode is not a part of snapback devices, it can be efficiently used as an ESD protection device. It is the simplest form of ESD protection device. In forward biased condition, it has very low turn on voltage and hence can carry large amount of current making it a perfect candidate for ESD protection scheme. However, in the reverse biased mode, it has high breakdown voltage and high resistance due to which it has lower current carrying capacity. Thus, it is not suitable for ESD protection as it cannot handle the bidirectional ESD stress.

The typical characteristics of snapback devices is demonstrated in Fig. 3.1 [2]. The ESD device will trigger only when the ESD voltage becomes higher than the triggering voltage (V_{t1}). Once the device get triggered and turns on, the net voltage will drop to value of holding voltage (V_h). The device will carry the ESD current stress in this region. The thermal breakdown of the device will occur at second breakdown point

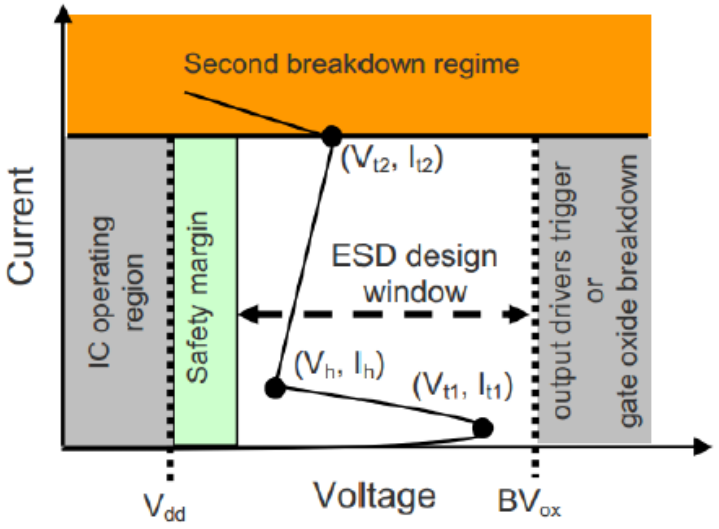

FIGURE 3.1: Characteristic curve for snapback devices [2].

(V_{t2},I_{t2}). This breakdown current is the measurement of ESD protection robustness and hence it should be as high as possible. With the scaling of technology nodes, gate oxide becomes thinner and results in the narrowing of voltage boundaries [2]. Later section briefly discusses the different type of snapback devices and their behavior.

3.1.1 Grounded Gate NMOS (GGNMOS)

The Grounded Gate NMOS (GGNMOS) is the simplest form of ESD protection device in the category of the snapback devices. For this device, the gate of NMOS is connected with body and source to the ground as shown in Fig. 3.2 [3]. As the drain voltage of MOSFET starts increasing, the drain-substrate junction becomes more reverse-biased and finally goes into avalanche breakdown region. At this point of time, the drain current increases significantly and the generated holes starts to drift towards the body. Due to this, the base voltage (V_{BE}) of the parasitic BJT increases and hence the base-emitter junction of the BJT becomes more forward biased. As soon as V_{BE} reaches the threshold voltage of BJT, it will turn on the bipolar junction transistor. The drain voltage of NMOS at this point known as first breakdown voltage (V_{t1}). Even if the ESD stress at drain terminal reduces from V_{t1}, the drain current will sustain as this bipolar action will generate more current. Therefore, the drain voltage (ESD stress) of NMOS will reduced to the holding voltage (V_h) and hence snapback behavior is observed. After the BJT turns on, if the drain voltage increases, it will further increase the current, until thermal runaway occurs. This is second breakdown point and the drain voltage and current through the device are V_{t2} and I_{t2} respectively.

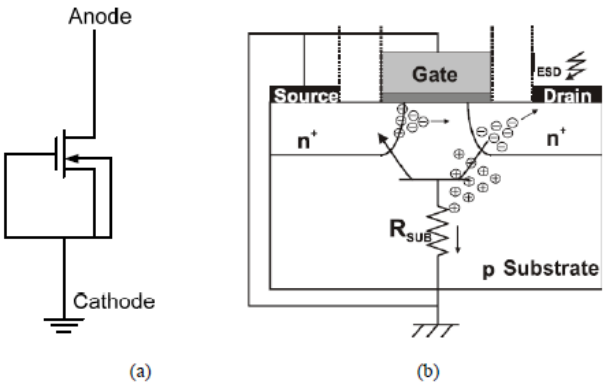

FIGURE 3.2: GGNMOS (a) Schematic (b) cross-sectional view [3].

The drain of the GGNMOS must be connected to the I/O pad to use it as ESD protection device. Under normal operating conditions, the NMOS transistor is off and the current through the device is very small, so that it does not effect the normal functionality of the core IC. Under ESD conditions, as soon as I/O pad voltage exceeds the first breakdown voltage, the transistor goes into the snapback mode. After this, ESD current is discharged through GGNMOS. The value of second breakdown current is used to determine the maximum ESD current that can be discharged through this device.

The GGNMOS is not a suitable candidate for providing the ESD protection in sub-micron technologies because triggering voltage (V_{t1}) is very high and is not appropriate to provide ESD protection for thinner gate oxides. Further, it is not suitable for pads that are sensitive to a leakage current [4]. This is because the leakage current of the NMOS is increasing exponentially with scaling down the technology.

3.1.2 Silicon Controlled Rectifier (SCR)

In addition to the GGNMOS, Silicon Controlled Rectifier (SCR) is another type of snapback type device, which is often used for ESD protection. This device consists of a pn-pn structure and cross-sectional view is presented in Fig 3.3 [4]. The diffused p+ in the n-well forms the anode and the diffused n+ in the p-sub forms the cathode of the SCR. The anode of SCR is connected to the I/O pad and the cathode of SCR is connected to the ground respectively. SCR is generally represented with the parasitic bipolar junction transistors as shown Fig. 3.3

The n-well p-substrate junction becomes more reverse biased as the anode voltage increases and finally goes into avalanche breakdown region. The generated carriers (current) can turn on either of the two BJT. Generally, the gain of the npn transistor is somewhat higher than that of the pnp transistor. Therefore, the npn transistor will

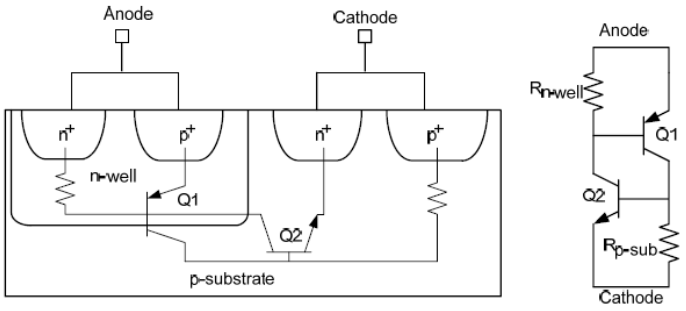

FIGURE 3.3: SCR (a) cross-sectional view (b) schematic [4].

turn on easily. When the npn transistor turns on, it will generate the current results in voltage drop across Rn-well and easily turns on the pnp transistor. Due to this, a voltage drop across Rp-sub is observed, which keeps the npn transistor in the on state. Due to the current flowing through pnp transistor, there is no need of any voltage at the anode to provide the npn transistor biasing. Therefore, the anode voltage can be reduced to holding voltage and similar characteristics as GGNMOS can be observed.

The triggering of SCR is initiated by avalanche breakdown of the well-substrate junction, while GGNMOS triggering is initiated by avalanche breakdown of the n+-substrate junction. Therefore, the first breakdown voltage (V_{t1}) for these two devices is different. Due to high breakdown voltage of SCR device, this is generally used in a modified configuration, which is known as Low Voltage Triggered SCR [16]. Keeping in mind the holding voltage of SCR and GGNMOS, it is clear that SCR needs some alterations to increase its holding voltage and to avoid the latch-up.

3.2 Non-snapback devices

In this section, we have discussed the different non-snapback devices, which are widely used by an IC industry for ESD protection. Among them, the most commonly used non-snapback devices are diodes and MOSFET based clamps. Non-snapback devices do not enter into the avalanche breakdown during the ESD stress. These devices are more stable than snapback devices and can be adapted from one technology node to another with some changes. These devices are generally connected between power rails V_{DD} and V_{SS}, hence they are known as Power Clamps. Basic structure of power clamp is shown in Fig. 3.4

ESD clamps are usually divided into two categories namely static clamps and transient clamps. Static clamps maintains steady-state voltage and current response. If the voltage goes beyond the limit, these clamps limit the ESD stress by carrying huge

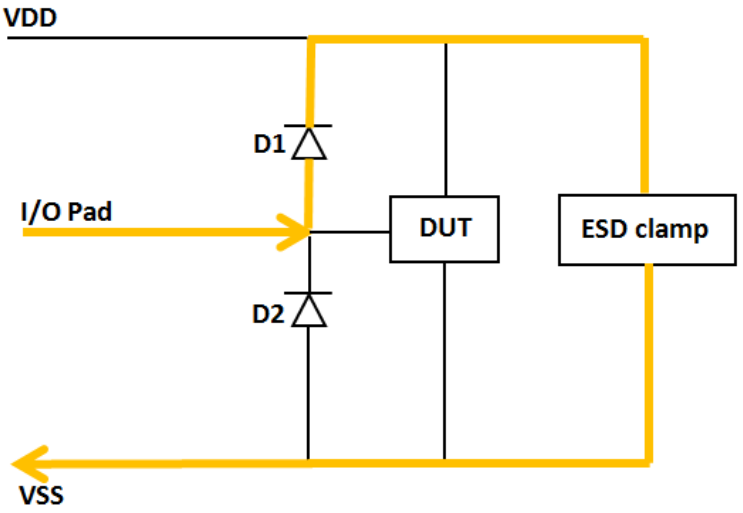

FIGURE 3.4: ESD Protection using non-snapback devices.

current by providing low impedance path. Most common static clamps are realized through diodes. Another type of ESD clamp is the transient clamps, which are designed to sense the sudden rise in voltage or current and therefore turns on the ESD clamp to discharge the ESD stress. These circuits consists of RC network and delay element followed by the big MOSFET. RC network senses the rapid change and turn on the MOSFET for the limited time to discharge the stress. Static clamps occupies less area and generally immune to false triggering while having more reaction time, more leakage and longer turn on time. While transient clamps are faster and have lesser turn on time. However, they occupies more area and is sensitive to false triggering [17].

3.2.1 Static ESD clamps

The diode string is commonly used as static clamp for the ESD protection. Static clamps turns on when the ESD stress becomes greater than the trigger voltage, which is defined as the threshold voltage set by the diode string as presented in Fig. 3.5. It should be noted that trigger voltage always remains lower than the oxide breakdown voltage. Diode in the forward biased mode can carry more current. The diode string should be placed between power rails. However, this configuration requires more time to respond to ESD stress. The criteria of using static clamp depends on various factors such as current carrying capability of device, leakage current, turn-on time, reaction time of the devices etc.

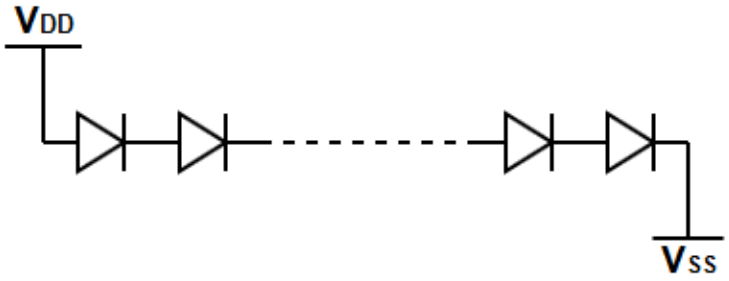

FIGURE 3.5: Stack of diodes as static clamp.

3.2.2 Transient ESD clamps

Transient clamps detects the sudden changes in the voltage or current and behaves accordingly. These clamps are designed to respond very quickly in case any rapid change is sensed. During this fast response, a semiconductor device, which is generally MOSFET is turned on very quickly and then turned off slowly to discharge the complete ESD stress. In general, a transient clamp consists of a bigger NMOS transistor that discharges the ESD stress after it gets triggered with an RC circuit as shown in Fig. 3.6 [4]. This type of clamp conducts for a fixed amount of time when it gets triggered. The important advantages of such clamps are the capability to provide ESD protection even at low voltages, quicker reaction and turn-on time etc. One of the major drawback of these clamps is that they also respond to any fast event such as noise. Hence, these clamps are more sensitive to false triggering where they can even trigger during normal power-up mode [18].

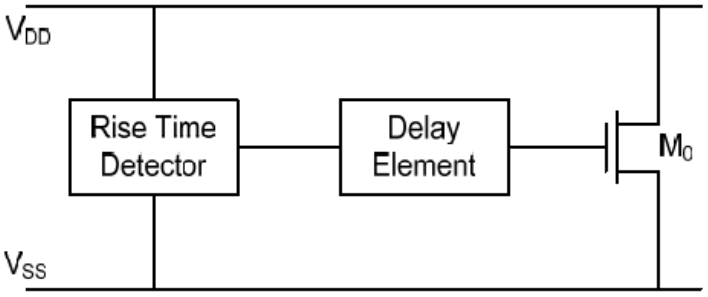

FIGURE 3.6: Transient clamp [4].

To avoid the false triggering of clamp during normal power-up condition, the trigger circuit must be able to detect the difference between the rise time of an ESD event and the rise time of a normal power-up condition. It can be observed that this design requires large transistors and capacitors and therefore, occupies a very large on-chip area [19]. However, the benefit is that only one transient clamp is sufficient for the whole chip and remaining pads can be connected to V_{DD} and V_{SS} through diodes.

The major task in transient clamp is to design a delay element, which makes the clamp to turn on for the sufficient time for complete discharge of the ESD stress. Hence, the delay is generally designed to be around $1\mu s$. If the clamp turns off before the ESD stress is discharged completely, it will result in residue build up at the clamp, which in turn could be a reason of device failure.

3.3 Summary

In this chapter, we have discussed the different types of devices, which can be used for ESD protection. Further, behavior and characteristics of different snapback devices have been studied. A detailed description about static and transient clamps is also presented. In next chapter, ESD test models will be discussed, which are required to verify the ESD performance of any design.

Chapter 4

ESD Test Models

In this chapter, we have presented the various ESD stress models, which are used by the semiconductor industry to check the robustness of the ESD design. In order to verify the susceptibility of DUT for ESD damage, there are certain ESD models suggested by JEDEC (Joint Electron Device Engineering Council) as presented in Table 4.1 [6]. These models mimic real-world ESD events in circuit simulations. These models are used as an industry standard and helps in designing of ESD protection circuit. In order to qualify ESD protection, DUT should undergo these tests and must pass them [20].

Table 4.1: Comparison of ESD test models [6].

Parameter	**HBM**	**MM**	**CDM**
Test Levels (V)	500-4000	100-200	250-1000
Pulse Width (ns)	150	80	1
Peak Current at 2 kV	1.33	-	5
Rise Time	10 ns	-	250-400 ps

4.1 Human Body Model

One of the most often observed ESD stress events is the transfer of electrostatic charge from a charged human body to DUT due to improper handling of an IC [21]. The ESD stress model, which is developed to present this ESD stress situation is known as Human Body Model. It is one of the most classical methods, which is commonly used by the semiconductor industry. As per HBM ESD model, it is assumed that a certain amount of an electrostatic charge is already stored in the human body and the charge is transferred to the device through any body part when there is a physical contact between human body and the DUT.

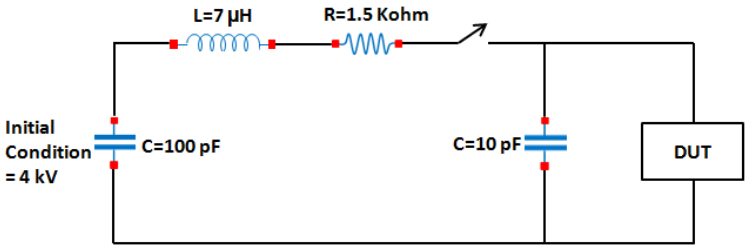

FIGURE 4.1: Human Body Model.

Human Body Model actually mimics the impact of a charged human body touching a grounded device. It should be noted that the human body can typically accumulate very high charge by its postures. The amount of charge accumulated in the human body vary from human to human depending on certain situations. The susceptibility of charge accumulation in HBM makes it very clear that some standard model is required to check the consistency.

Equivalent circuit of HBM model is shown in Fig. 4.1. It consists of a charging capacitor and a resistance between the charged source capacitor and DUT. As per HBM standard, the components used in the circuit to simulate the charged human body model consists of a 100 pF capacitor and the resistance value of 1500 Ω in the discharging path. It electrically looks as an independent current source if the DUT provides low impedance path. The effective inductance of the discharge path is set to 7 μH in a real test situation. It should be noted that HBM has the longest pulse among all three primary ESD test models. The rise time of the HBM pulse nearly lies from 5 ns to 10 ns with decay time (pulse width) of around 150 ns [5].

4.2 Machine Model

Another fundamental model is the Machine Model, which is used to simulate the ESD events caused by automated handling. Machine Model emulates the discharge of a charged equipment through the grounded DUT. In this way, it models the handling of ICs by an automated assembly equipment.

Similar to the HBM model, an input capacitor of value 200 pF represents a conductive object, which is initially charged up to a high voltage value and then discharged through the pins of device. For Machine Model, it is assumed that a sudden discharge occurs between the charged source and the device. An arc discharge primarily has a resistance value of 10 to 20 Ω, which is significantly lower than the HBM resistance, which is 1500 Ω. In addition, the inductance of the discharging path becomes 0.5 μH. Equivalent circuit of MM model is shown in Fig. 4.2. Hence, the MM response is quite rapid

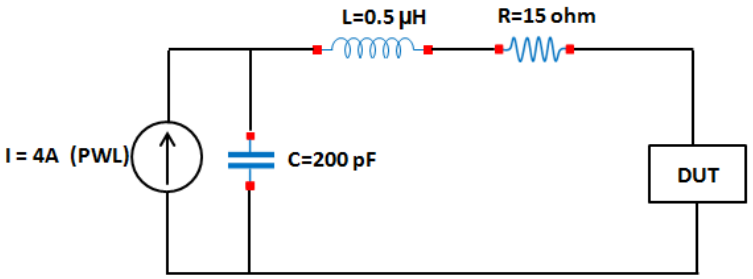

FIGURE 4.2: Machine Model.

than the HBM response. It has a type of bidirectional damped oscillation [3]. The MM modeled ESD stress shows a considerably higher current than the HBM stress. Since the input resistance in MM is quite small, the stray capacitance and inductance of test machine and the impedance of the DUT may change the current waveform. Therefore, it is more difficult to make MM standards compare to that of HBM. Although, the failure signs of the Machine Model is almost the same as that of the HBM. It is because the discharging processes are similar in both types of ESD models. Generally in most of the cases, MM ESD robustness can be assured by the HBM test. Experimentally, the supportable voltage stress level of Machine Model has been found to be around 10 times lower as compared to HBM stress level.

4.3 Charged Device Model

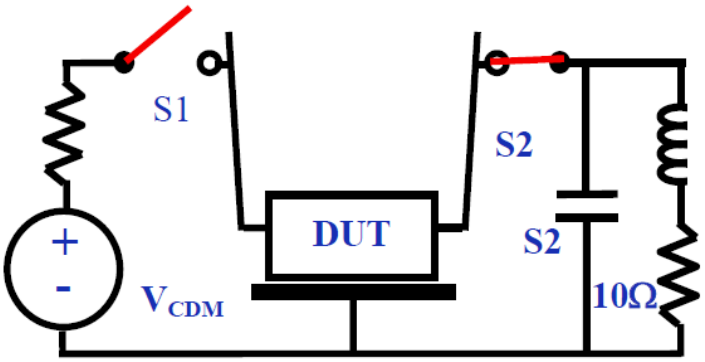

FIGURE 4.3: Charged Device Model (CDM) [5].

The Charged Device Model is also one of the ESD testing model. This model possesses the highest ESD stress among all three types and it is the most difficult ESD stress model to realize. Therefore, this model is becoming a concern for sub-micron technologies because of high ESD stress. This model tries to simulate the environment, which is

related to the packaging of an IC on the assembly line. During packaging mechanism, the IC can be charged by a number of ways.

In a CDM event, an IC gets charged and then discharged to the ground through single pin. The discharging process of a CDM event requires only single pin unlike HBM and MM event, which need two pins to discharge. When the device or an IC moves during the assembly of an IC, some electrostatic charge gets accumulated. The charging process could be a direct charging or field induced. The equivalent circuit of typical Charge Device Model is shown in Fig. 4.3. Generally, CDM events are very short duration events and generates a large amount of current. Further, discharging process in CDM is also very fast and IC get discharged within 5 ns of time interval. The rise time of a CDM event is around 250 ps. As the waveforms of CDM is much different than that of HBM and MM, hence the failure mechanism are also not identical. Dielectric failure is a reason of CDM failure unlike HBM and MM, where thermal breakdown is a primary reason [5].

4.4 Comparison between HBM, MM and CDM

The current waveform of HBM, MM and CDM events, which can be applied to DUT is shown in Fig. 4.4. It is clearly observed that MM has higher peak current and much smaller rise time than HBM. The MM has quite high peak current due to higher parasitic capacitance. Thus, it lower down the overall impedance of the path and results in higher current density during the time of discharge of MM. Hence, even though MM failures are similar to that of HBM event, the ESD failures caused by MM may occur at lower threshold levels. It is also observed that the CDM stress current has highest ESD peak stress and smallest rise time around 250 ps to 400 ps as compared to MM and HBM ESD events. The HBM stress current has quite large rise time, large decay time around 150 ns and smallest peak current.

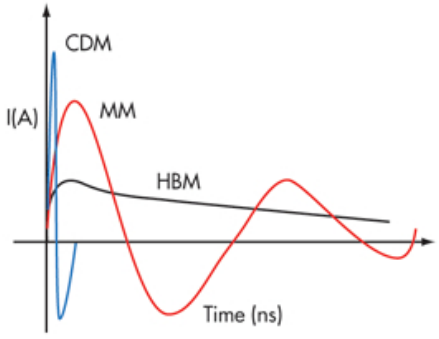

FIGURE 4.4: HBM, MM and CDM current stress.

4.5 Summary

In this chapter, we have briefly discussed the different types ESD test models to simulate the real ESD environment. These models are widely used in the semiconductor industry to verify the ESD reliability of a device. In addition, comparison between HBM, MM and CDM is presented in terms of peak current and rise time. In next chapter, proposed ESD design will be discussed to deal with the existing challenges of ESD protection circuit.

Chapter 5

ESD Protection Circuit Design

In this chapter, we have presented the traditional ESD protection circuit and its challenges in the modern world. Further, the detailed description of the proposed work is given. Some of the existing ESD design techniques have been incorporated within the proposed work to get the optimum results. This thesis is mainly focused on high voltage tolerant ESD protection design, which has its application in mobile phones, flash drives etc.

Major research area of this thesis work is to optimize the area of clamp, which is the most area hungry block in the ESD protection circuit. Further, it aims to reduce the inrush (surge) current to the larger extent, while supporting to the high supply voltages. This circuit design is also able to minimize the hot insertion effect to support plug and play feature. During hot insertion, DUT typically receives the power supply with ramp rate of 500 ns. To support plug and play, ESD circuit should not get triggered at the given ramp rate. In addition to this, proposed ESD protection design is immune to the false triggering, which is the major challenge of transient ESD protection [22]. As per industry standards, the specifications used for ESD protection circuit design is given in Table 5.1. The advantages and disadvantages of the existing and proposed work is also discussed in the later section of this chapter.

Table 5.1: Specifications

Technology	TSMC 16nm FINFET
Supply Voltage	3.3V (2.7V to 3.6V)
Max HBM stress	4 kV
Max MM stress	200 V
Max CDM stress	500 V
Worst Inrush @ 500 ns	10mA
To support	Hot Insertion (Plug and Play)

5.1 Related Work

There are many traditional transient ESD clamp circuits, which are widely used in the industry for ESD protection. As already discussed in the chapter 3, basic ESD clamp circuit consists of ESD detection circuit followed by the delay element, which is connected to the ESD clamping NMOS. The typical RC based ESD clamping circuit is shown in Fig. 5.1.

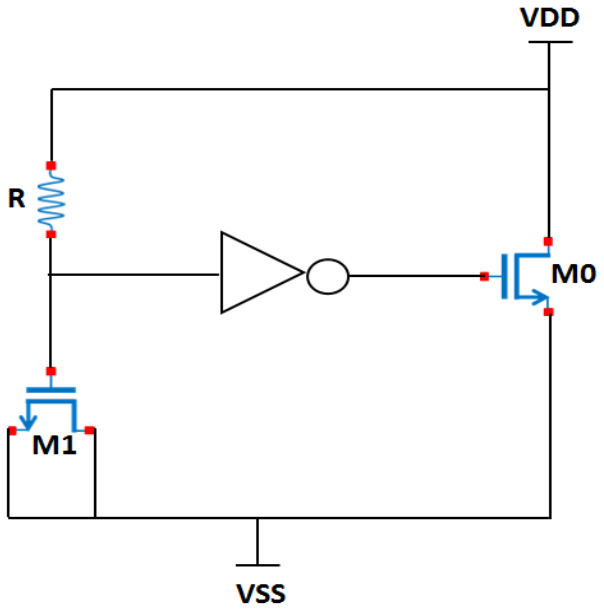

FIGURE 5.1: Typical RC based ESD protection circuit.

The ESD event detection circuit consists of a RC network. RC time constant is set in such a way that it is able to detect rise time of an ESD event. This detection circuit is then followed by the delay element and ESD clamping NMOS. The size of an inverter is sufficiently large to drive bigger ESD clamp. MOSFET is placed to provide the low impedance path between V_{DD} and V_{SS} power rails in case any ESD event comes. This MOSFET clamps down the overstress ESD voltage and effectively protects the main circuit. Typically, ESD clamps consists of big NMOS at the output stage, which can tolerate the ESD current stress without going into thermal breakdown condition. The turn-on time of the ESD clamp depends on the RC time delay. Thus to meet the ESD requirement, turn-on time is generally set around 1 μs so that clamp can remain in turn-on state for sufficiently long time to get the ESD stress discharged. Under normal power on condition, this ESD protection circuit should be in the off state to avoid any power consumption.

This is the most basic circuit of ESD protection, however it has many disadvantages. The first major limitation is its sensitivity to the high voltage. As technology is scaling down, oxide thickness is also decreasing. Thus, ESD clamping NMOS is not able to stand

at high voltages due to oxide breakdown. As RC time constant has to be around 1 μs, it requires larger MOSCAP, which causes high leakage and high inrush current. If RC time delay is not sufficiently high, then clamp size required is much large which occupies large on-chip area. Other major challenge is the Hot Insertion effect (Hot plugging) as this circuit will trigger at 500 ns supply ramp rate.

5.2 Proposed Work

In order to mitigate the above stated limitations of ESD protection circuit, high voltage tolerant ESD protection circuit has been proposed, whose circuit schematic is presented in Fig. 5.2. The proposed clamp design can be successfully operated at supply voltage range of 2.7 to 3.3 V. In 16 nm FINFET technology, thick gate device has a DC stress limit of 1.8 V. In order to support high supply voltage, proposed design employed cascode structure.

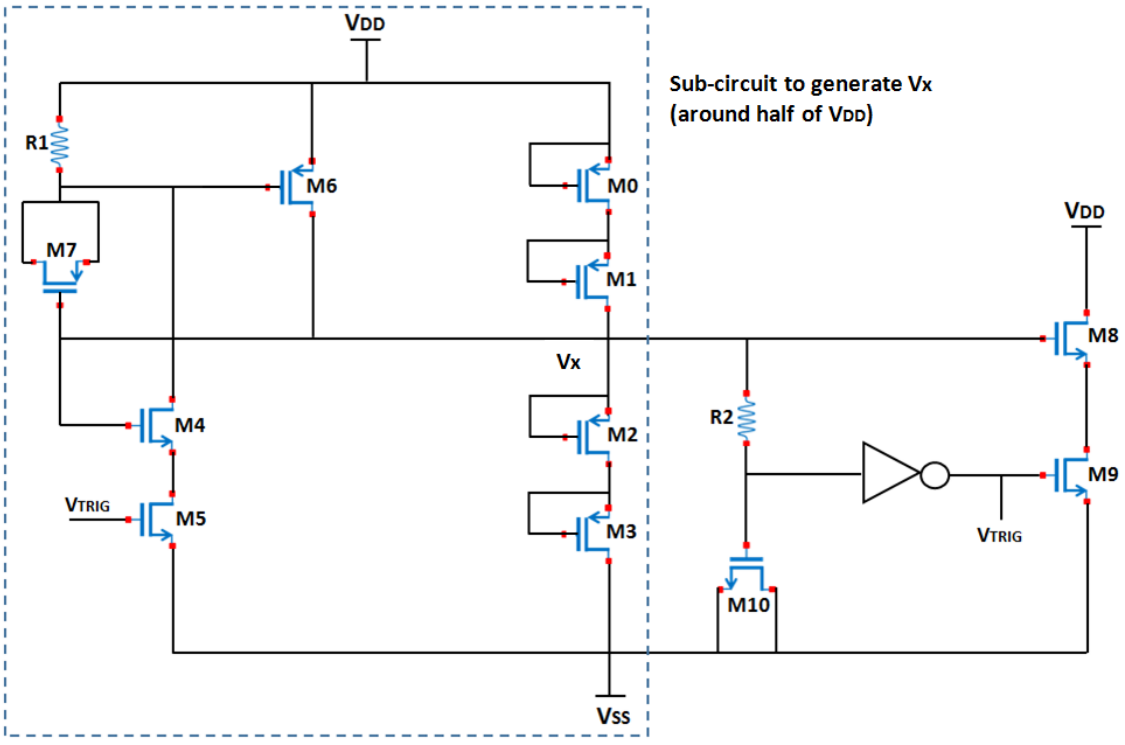

FIGURE 5.2: Baseline high voltage tolerant ESD protection circuit.

As shown in the Fig. 5.2, drain of device M8 is connected to V_{DD} (ESD stress), while gate is operated at V_X (around half the voltage of V_{DD}). As M8 has a stress limit of 1.8 V, it is cascoded with M9. Gate of M9 is the output of the RC detection network, which is operated at V_X. RC delay is realized using components R2 and M10 for the delay of around 1 μs to turn on the clamp for sufficient time to discharge the ESD stress.

The size of an inverter is sufficiently large to drive big NMOS M9 at the output stage. Generally, M8 is always in the on state, however the low impedance path between V_{DD} and V_{SS} depends on the state of M9.

Sub-circuit, which is used to generate V_X out of the V_{DD} is highlighted in the Fig. 5.2. It is realized using PMOS ladder as local biasing from source to bulk is possible. If local biasing is not done, then it may result in different threshold for each device that may further lead to the V_X value not equals to $V_{DD}/2$. Here, RC network (using R1 and M7) is deployed to bypass the V_{DD} to V_X node through PMOS M6 in case when ESD event comes. This is done to generate V_X voltage instantly, which can further trigger the clamping NMOS M9 as soon as ESD event comes. In addition, it will increase the gate voltage (V_X) of clamping NMOS M8 and thus requires small W/L to pass the ESD current stress. Relation between clamp size and gate voltage is shown in the current equation 5.1. More is strength of PMOS M6, lesser will be its reaction time to bypass V_{DD} to the V_X node. In case of DC supply, RC element (R1 and M7) in the resistor divider will not work and PMOS ladder will maintain V_X node at half the voltage of V_{DD} i.e. $V_{DD}/2$.

$$I_D = K_N \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2 \tag{5.1}$$

The key advantage of this circuit is its ability to support high supply voltages. However, time constant of around 1 μs and large size clamping NMOS is needed to discharge the stress. Thus, it relatively occupies more area and has more inrush current. Therefore, some ESD optimization technique can be implemented to further reduce the clamp area. As only one RC delay element is used for ESD event detection as well as for on-time of the clamp, this circuit will suffer from false triggering and hot insertion problem.

5.2.1 Design Techniques incorporated

In order to optimize the aforementioned ESD design challenges with the nano-scale applications, some effective ESD design techniques is also implemented along with this proposed high voltage tolerant ESD circuit design. Compared to the baseline circuit, this proposed ESD protection circuit is capable of dealing with the major design challenges such as ESD clamp area, high inrush current, false triggering issue and hot insertion effect.

5.2.1.1 Boost Trigger Technique

One of the major design challenges in the field of ESD circuit design is the clamp size. Generally, clamp circuit consists of the bigger MOSFET that is capable enough to discharge the complete ESD stress. Hence, clamp is the most area hungry block and need to be optimize for effective circuit design. One way to reduce the clamp size (W/L of MOSFET) is to increase the gate voltage V_{GS} as shown in equation 5.1.

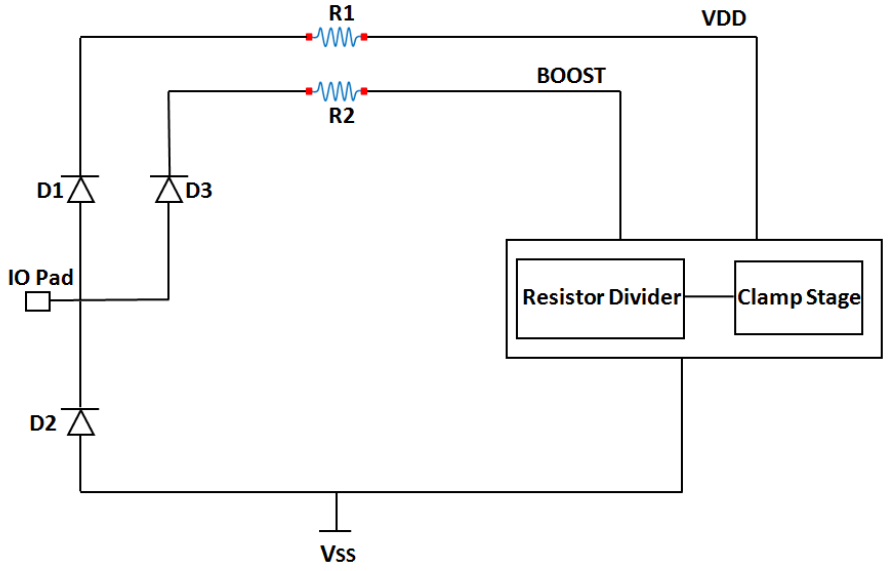

FIGURE 5.3: Proposed design with Boosted Rail configuration.

The basic concept of the boosted rail configuration is that for a given V_{DS} value, the conductance of an NMOS starts increasing as V_{GS} is increased [23]. Simple boosted configuration is shown in Fig. 5.3. Here, one extra diode D3 is placed at the I/O pad to bypass the V_{DD} to the trigger circuit. R1 and R2 are the parasitic resistances. ESD clamping NMOS, which is biased at V_{DD}, will provide a low impedance path in case of any ESD event and thus able to discharge all the current stress. Therefore, all current will flow through R1, which is also biased at V_{DD} and hence result in voltage drop across R1. However, no current will flow through R2, which results in the BOOST voltage more than the V_{DD}. Therefore, gate voltage of the clamp becomes more than the drain voltage and hence small sized device can be placed to discharge the same current stress.

In our proposed work, this boosted topology is only implemented in the resistor divider sub-circuit as shown in Fig. 5.4 while clamp stage remains unchanged. Here, RC network is maintained at higher voltage BOOST as compared to PMOS resistor ladder V_{DD}. This is done to increase the V_X voltage, which is the gate voltage to the clamp as shown in Fig. 5.2. In this way, gate voltage to the lower clamp (V_{TRIG}) is also increased. Therefore, NMOS clamp with smaller size can be placed to discharge the

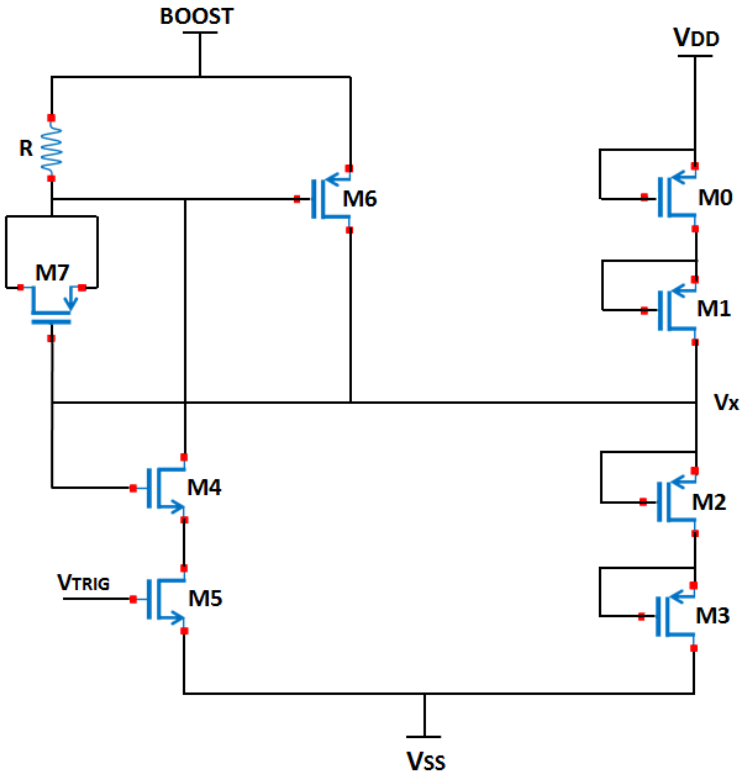

FIGURE 5.4: Resistor divider sub-circuit with boosted V_X.

same ESD stress. This topology reduces the clamp area, which is the major challenge in designing ESD protection circuit and thus reduces the static current to the smaller values.

The important concern with the boosted rail configuration is that the clamping MOSFET is more susceptible to the thermal breakdown as the gate voltage is more than the drain voltage. The MOSFET gate oxide is permanently damaged if voltage at the gate increases more than the breakdown voltage, independent of the applied V_{DS}. It should be noted that threshold voltage and breakdown voltage defines the safe ESD operating regime of the MOSFET. Proposed baseline circuit with boost trigger topology is able to reduce the clamp area and static current, however still some design challenges such as false triggering, high inrush current and hot insertion need to be addressed. For any ESD optimization technique, we have to ensure that the MOSFET must stay within the permissible boundaries of safe operation.

5.2.1.2 2 stage RC topology

As discussed in the previous section, another major challenge of ESD protection design is to limit the inrush current and to deal with the issue of false triggering. The simple trigger circuit in ESD protection uses just one RC time constant for both ESD detection

and on-time control of the ESD clamp. Hence, RC time constant must be quite large in range of 1 μs to ensure that clamp should remain turn on for the entire duration of the ESD event. For this purpose, we need large R and C devices that actually increases the vulnerability to the false triggering during power-up condition because the ESD detection range is unnecessarily wide due to large RC. It also increases the inrush current to due large size of the device M1.

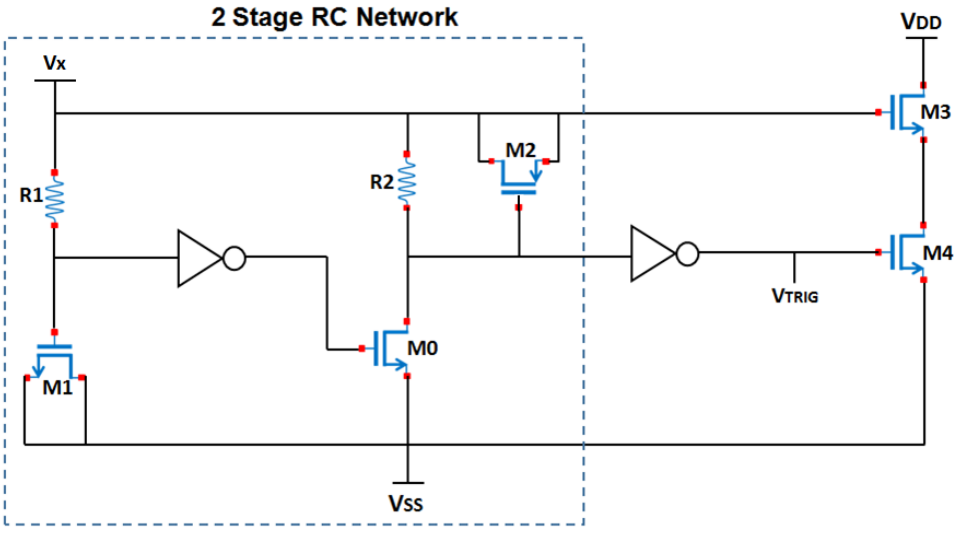

FIGURE 5.5: Proposed ESD protection circuit with 2 stage RC.

Some other transient trigger circuit, which requires the separate RC time constants for ESD detection and on-time control can be used to overcome above problem [23]. Single RC stage can be replaced with the 2 stage RC network as shown in Fig. 5.5. To detect the ESD event, first stage RC (R1 and M1) is set to detect the desired ESD event. This results in smaller R and C devices, hence improving the immunity to false triggering. It also results in much smaller inrush current due to small sized devices. The on-time of the clamp can be controlled with the second RC stage (R2 and M2).

As shown in Fig. 5.5, rise time detector provides some short time voltage pulse that triggers the on-time control circuit by turning on the MOSFET M0 and then finally the clamping NMOS M4 through the last inverter. The on-time of the ESD clamp is set by the second RC stage with the device sizes of R2 and M2. At the end of the voltage pulse provided by the rise time detector, M0 will turn off. Capacitor M2, which is connected to the input of the last inverter is slowly discharged through the resistor R2 till the time inverter finally flips its state and turns off M4. As very small RC is required in the first stage to detect the ESD event, this results in smaller R1 and M1. Hence, this topology limits down the inrush current and is immune to the false triggering due to smaller capacitance values. It also eliminates the hot insertion problem for plug and play devices as it does not allow the ESD circuit to trigger even at 500 ns supply ramp rate.

Thus, proposed circuit is implemented using boost trigger topology and 2 stage RC within the proposed cascoded ESD protection circuit. Resistor divider to generate V_X (around half of V_{DD}) is designed using boost trigger while clamp stage is designed using 2 stage RC. This finally addresses all the existing design challenges of the ESD protection circuit. This proposed circuit can work for high voltages with low inrush current. Further, this circuit is immune to the false triggering and hot insertion.

5.3 Summary

In this chapter, we have briefly discussed the different ESD protection techniques required for the ESD design optimization. Further, we have discussed the existing and proposed work in the detailed manner. Optimization of the ESD design is done by incorporating various techniques within the proposed design. Proposed ESD protection circuit is better in terms of clamp area, inrush current and immunity to the false triggering. In the next chapter, we have presented the simulation results of proposed ESD protection circuit.

Chapter 6

Results and Discussions

This chapter presents the simulation results of the proposed transient ESD clamping circuit and comparison of the same by implementing various optimization techniques. The circuits are implemented in Cadence Virtuoso TSMC 16nm FinFET technology and simulations took place using HSPICE simulator. The characterization has been done on basis of many variables such as supply voltage variation for 2.7/3.3/3.6 V and temperature variation of -40°C to 125°C. Simulations have been performed for 81 cross corners with variation in MOSFET intrinsic parameters, temperature and resistance. The combination of NMOS and PMOS could be FF, TT, SS, SF and FS with resistance value as R_{min} and R_{max}. As per industry standards, all the HBM simulations have been performed for 4 kV ESD stress and MM simulations for 200 V stress.

6.1 High Voltage Tolerant Cascoded ESD clamp (Baseline Circuit)

This section contains the simulation results of cascoded clamp based baseline ESD protection circuit as shown in Fig. 5.2. Transient simulations have been performed to verify the ESD performance of the circuit using HSPICE simulator. RC time delay is set around 1 μs and clamp size to 1475 μm/0.15 μm.

6.1.1 HBM Test Results

As already discussed in the chapter 4, there are three common ESD test methods. In this section, HBM simulations are presented. It should be noted that maximum stress across the MOSFET devices is 3.94 V in transient condition with 1.8 V as DC stress limit as per TSMC 16 nm datasheet.

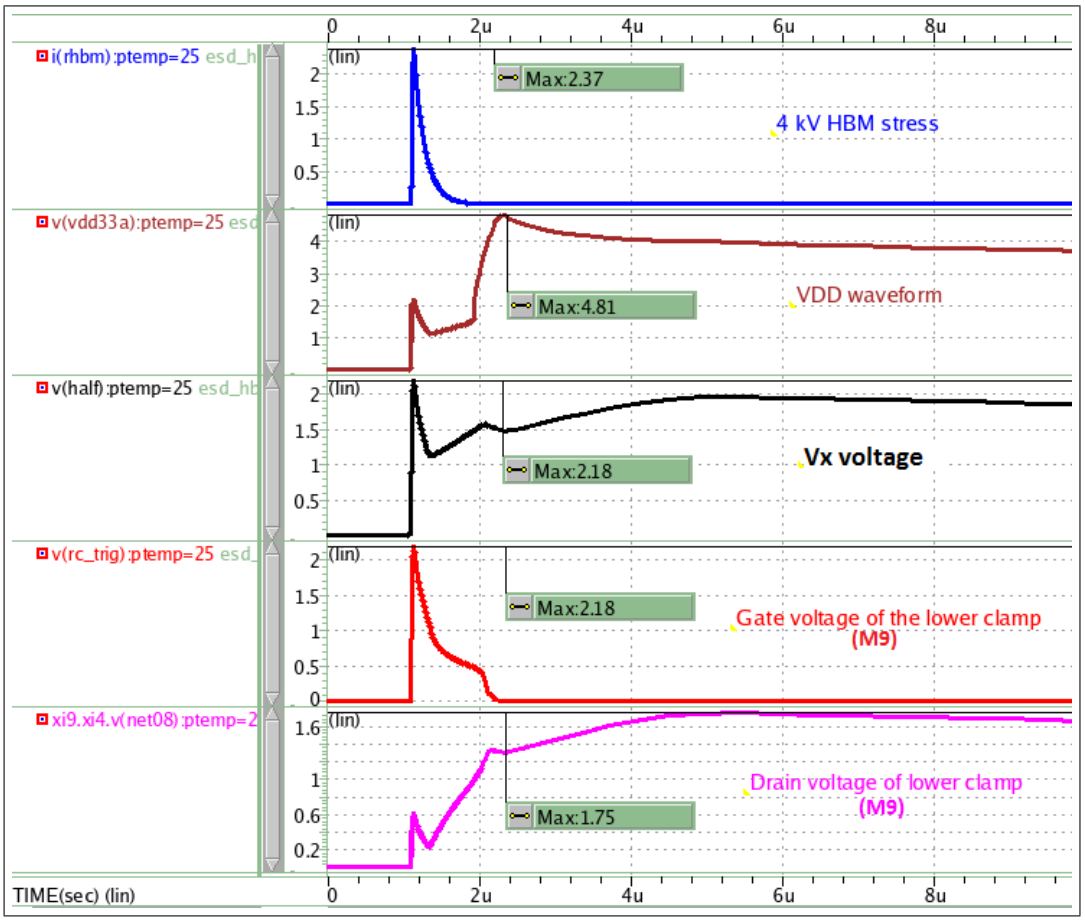

FIGURE 6.1: HBM simulation at TT corner for baseline circuit.

Fig. 6.1 shows the HBM simulation results with 4 kV ESD stress at TT corner for circuit schematic presented in Fig. 5.2. It clearly shows that the clamp is able to discharge the ESD stress at corresponding 2.67 A of current stress. As soon as ESD event comes, clamp is triggered by the RC circuit. Therefore, first peak in the V_{DD} waveform goes down as clamp turn on. However as soon as clamp turns off, it results in some voltage buildup across clamp. We have to ensure that this voltage buildup should be within the safe limits of device operation. Fig. 6.2 shows the cross corner (PVT variations) result of HBM simulation with maximum device stress of 3.61 V, which is less than the transient breakdown voltage.

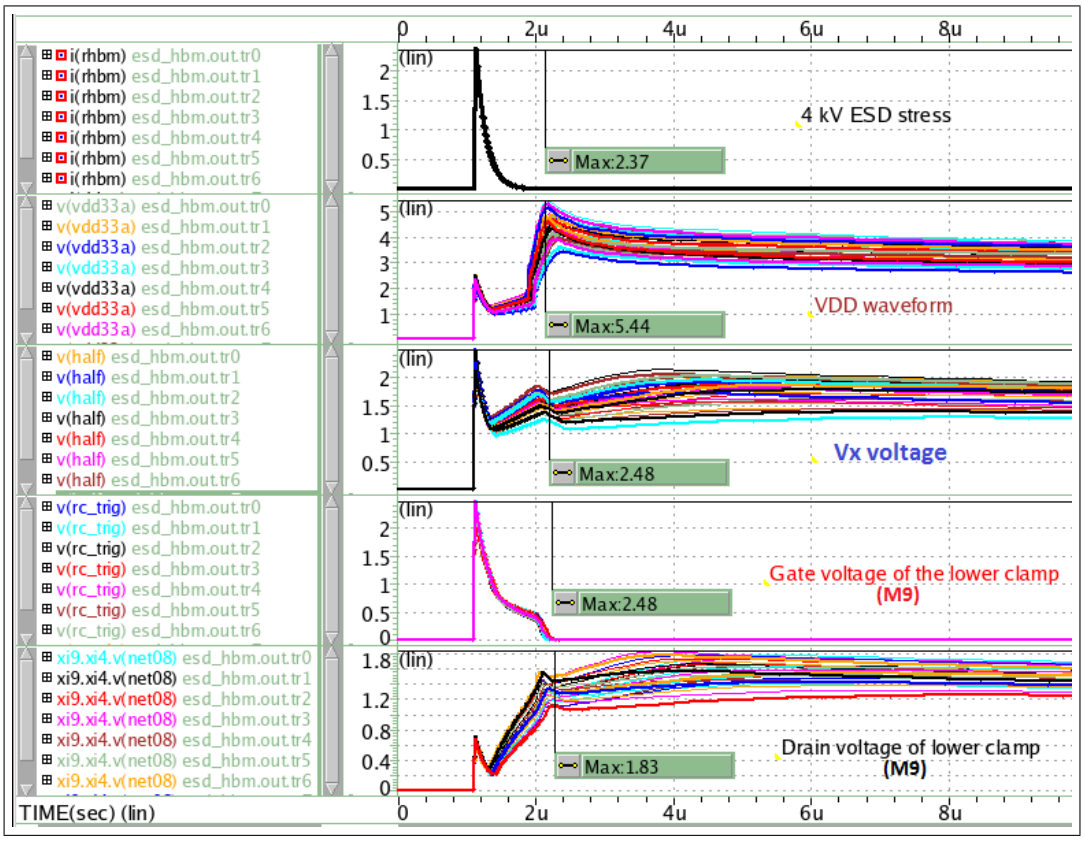

FIGURE 6.2: HBM cross corner (PVT) simulation for baseline circuit.

6.1.2 MM Test Results

In this section, MM simulations are presented for 200 V ESD stress or corresponding 4 A ESD current stress. Oscillatory behavior of voltage and current can be noted due to LC circuit.

Fig. 6.3 shows the MM simulation results for 4 A ESD current stress at TT corner. It can be observed from the simulations that the clamp is able to discharge the ESD stress at corresponding 4 A of applied input current stress. In case of any ESD event, voltage starts building across the clamp and clamp should be able to discharge the stress within RC time delay keeping in mind that voltage buildup should be within the safe limits. It can be noted that HALF voltage follows V_{DD} for few nanoseconds and then settles at half of the ESD stress. Fig. 6.4 shows the cross corner result of MM simulation with maximum device stress of 3.44 V across lower NMOS clamp.

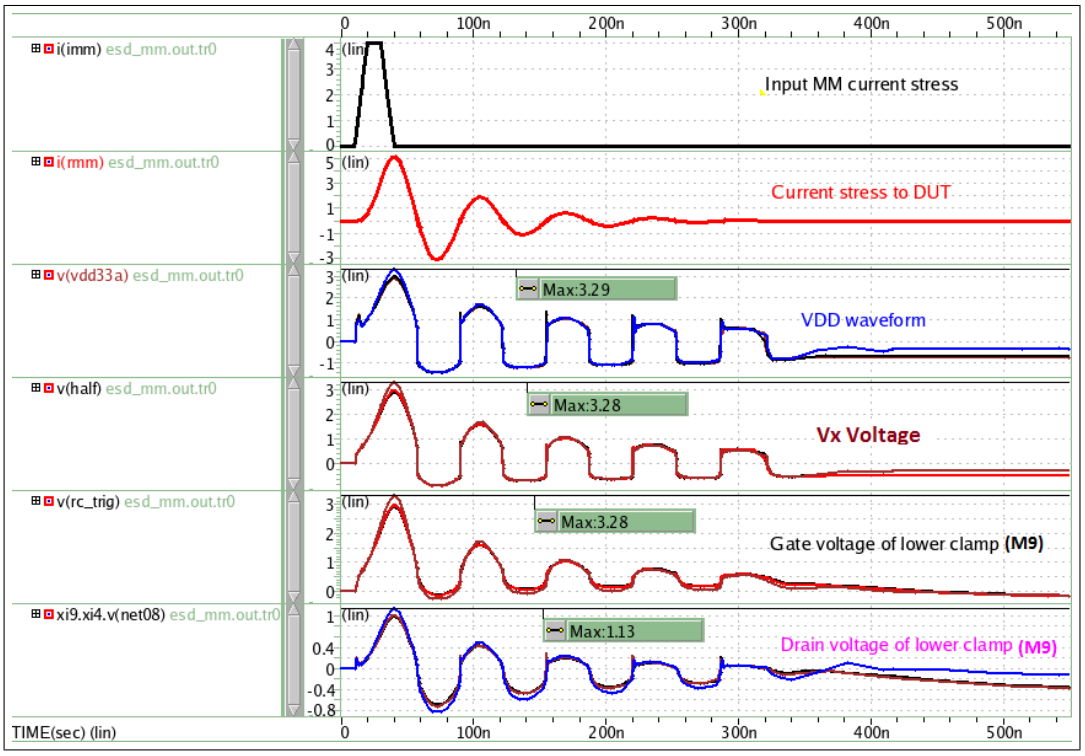

FIGURE 6.3: MM simulation at TT corner for baseline circuit.

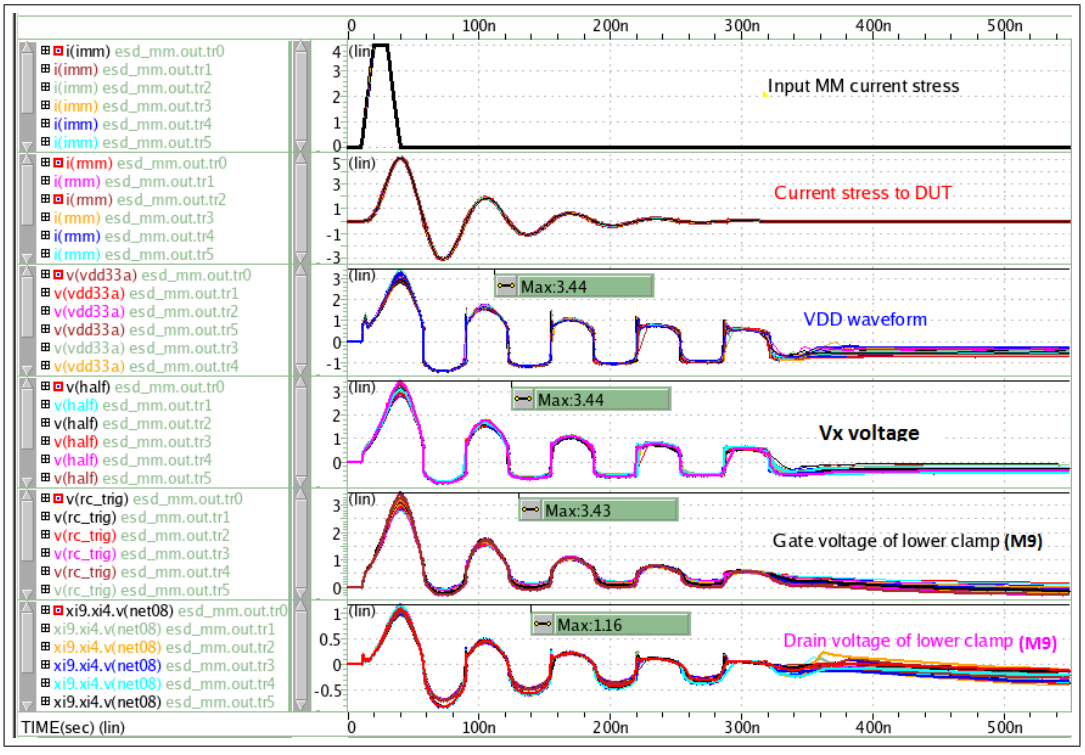

FIGURE 6.4: MM cross corner simulation for baseline circuit.

6.1.3 Current Analysis

This section contains the DC and inrush current analysis of the proposed ESD protection circuit. This performance parameter of the ESD protection circuit provides the idea of ESD design robustness.

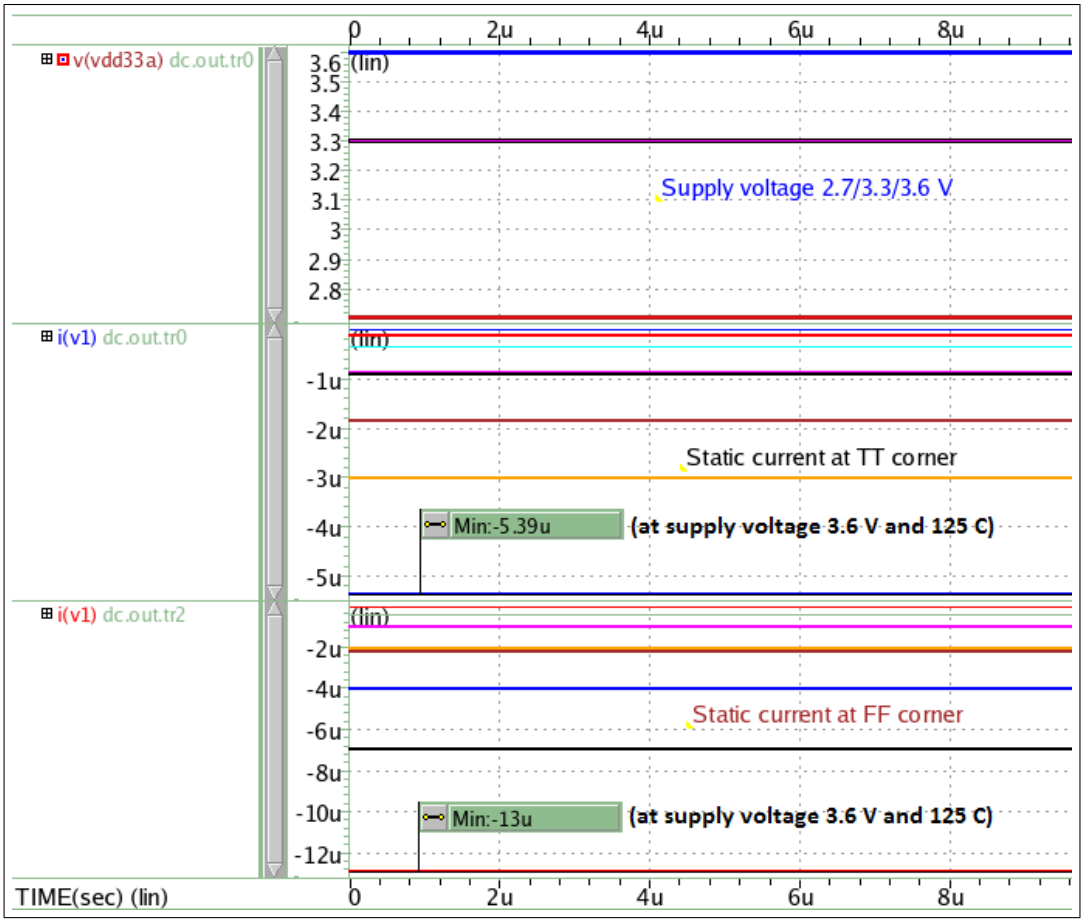

FIGURE 6.5: Static current at TT and FF corner for baseline circuit.

Fig. 6.5 shows the static current through the design at normal power on condition. It also gives the approximation of power consumption. This simulation is done for voltage variation of 2.7/3.3/3.6 V at TT and FF corner with temperature variation from -40°C to 125°C. The worst case static current is observed at FF corner 125°C with the current value of 13μA at supply voltage of 3.6 V. Under similar conditions, maximum current at TT corner is 5.4μA.

Fig. 6.6 and Fig. 6.7 shows the cross corner inrush current characteristics with the applied voltage. Inrush current measures the design performance in case of fast ramp supply voltage. Simulation is carried out for 1μs and 4μs ramp rate in supply voltage with maximum voltage range from 2.7 V to 3.6 V. It can be noted that first peak in the current characteristics is due to the partial on-state of PMOS of an inverter in clamp

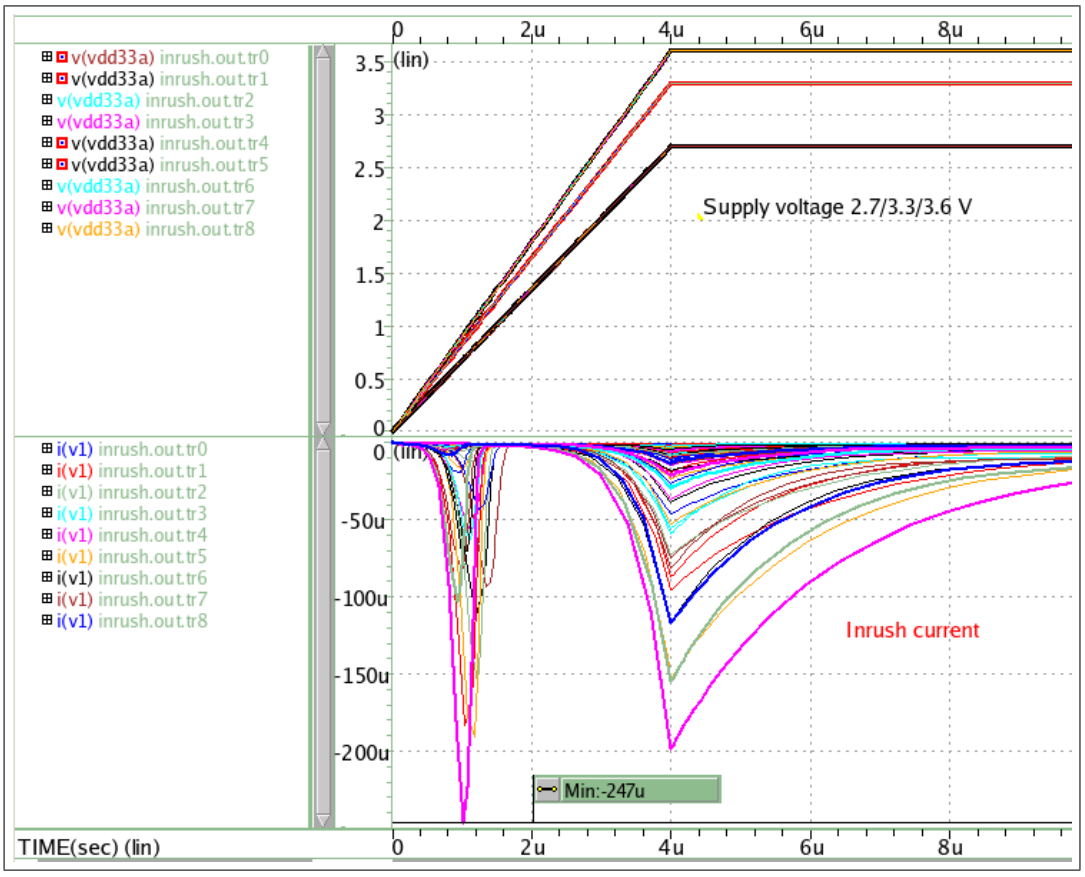

FIGURE 6.6: Inrush current cross corner plot at $4\mu s$ ramp rate for baseline circuit.

stage and second peak is due to the leakage from MOSCAP as supply voltage increases (see Fig. 5.2). Maximum inrush at $4\mu s$ ramp rate is found to be 247 μA at 125 C and supply voltage of 3.6 V. Further, it can be noted from Fig. 6.7 that ESD clamp triggers at $1\mu s$ ramp rate, which result in flow of huge inrush current. Therefore, this IO design can support of minimum $4\mu s$ ramp rate. Anything faster than this ramp rate will trigger the RC element.

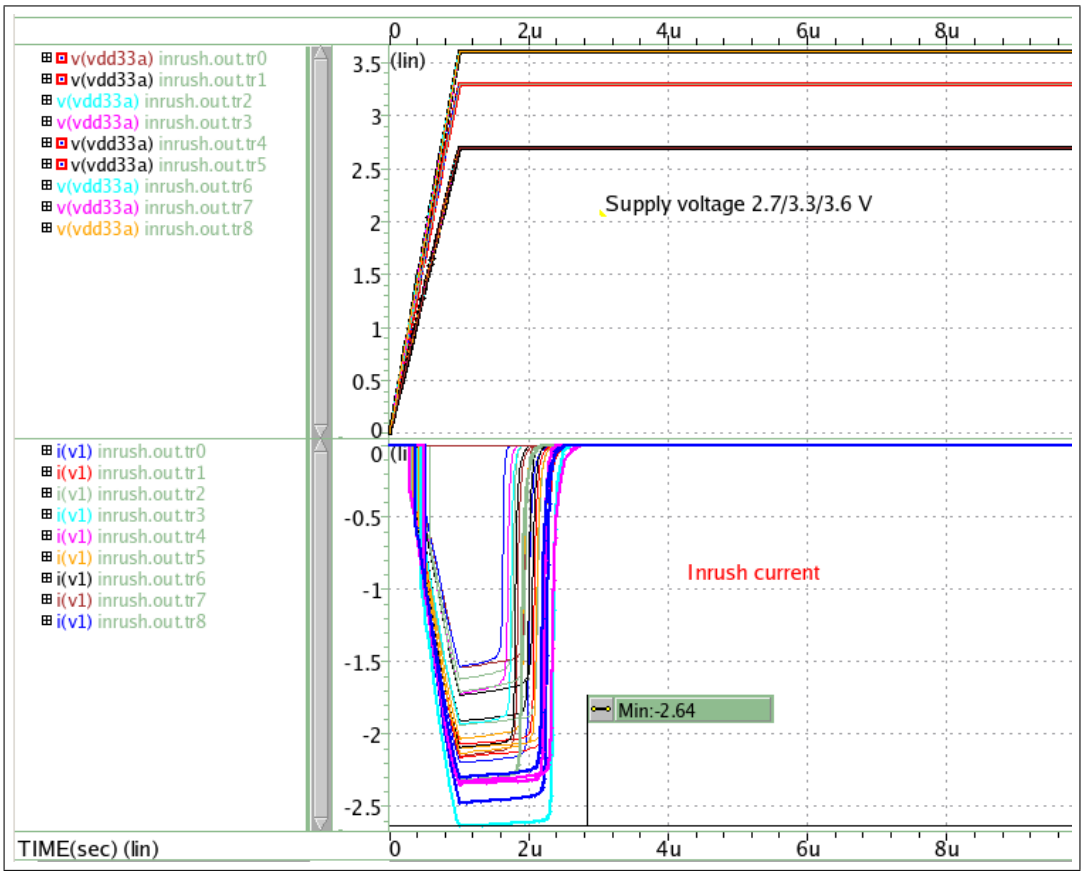

FIGURE 6.7: Inrush current cross corner plot at $1\mu s$ ramp rate for baseline circuit.

6.2 Baseline circuit With Boosted Rail Clamp Topology

As discussed in the previous chapter, various ESD optimization techniques have been incorporated within the baseline design to deal with the ESD design challenges. One of the discussed topology is boost trigger in which RC network is maintained at higher potential than the ESD clamping MOSFET to increase the gate voltage of the clamp. This topology is implemented for the resistor divider sub-circuit that is used to generate HALF as shown in Fig. 5.4. This enables the designer to place small size clamping NMOS to discharge the same ESD stress. Here, clamp size is reduced to 922 μm/0.15 μm while all other parameters are kept same as previous one.

6.2.1 HBM Test Results

In this section, HBM test simulations are presented for 4 kV ESD stress. Fig. 6.8 shows the HBM simulation results at TT corner with the aforementioned changes. It clearly depicts that the ESD clamp is still able to discharge the ESD stress at even lesser size of the clamping NMOS. Though, gate of the clamp and HALF voltage increases a bit

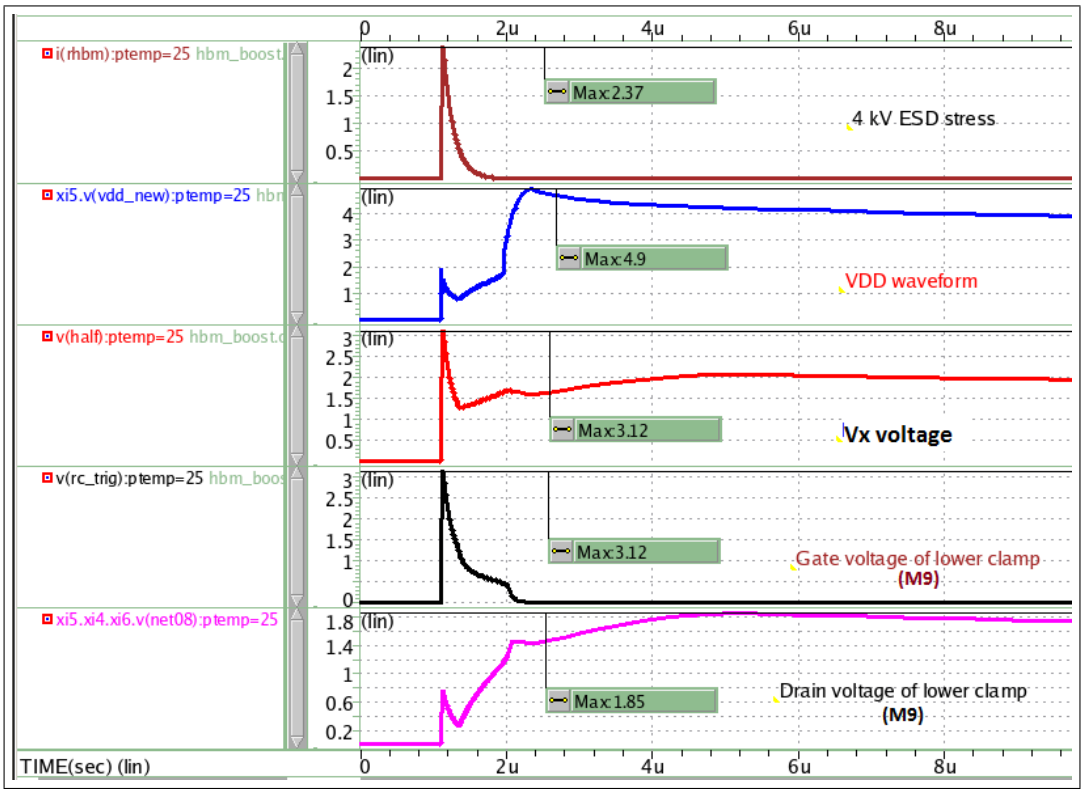

FIGURE 6.8: HBM simulation at TT corner with boost trigger topology.

but the increase is within the safe limits of operation. Fig. 6.9 shows the cross corner simulation result of HBM test model with maximum device stress of 3.7 V, which is lesser than the thermal breakdown of device.

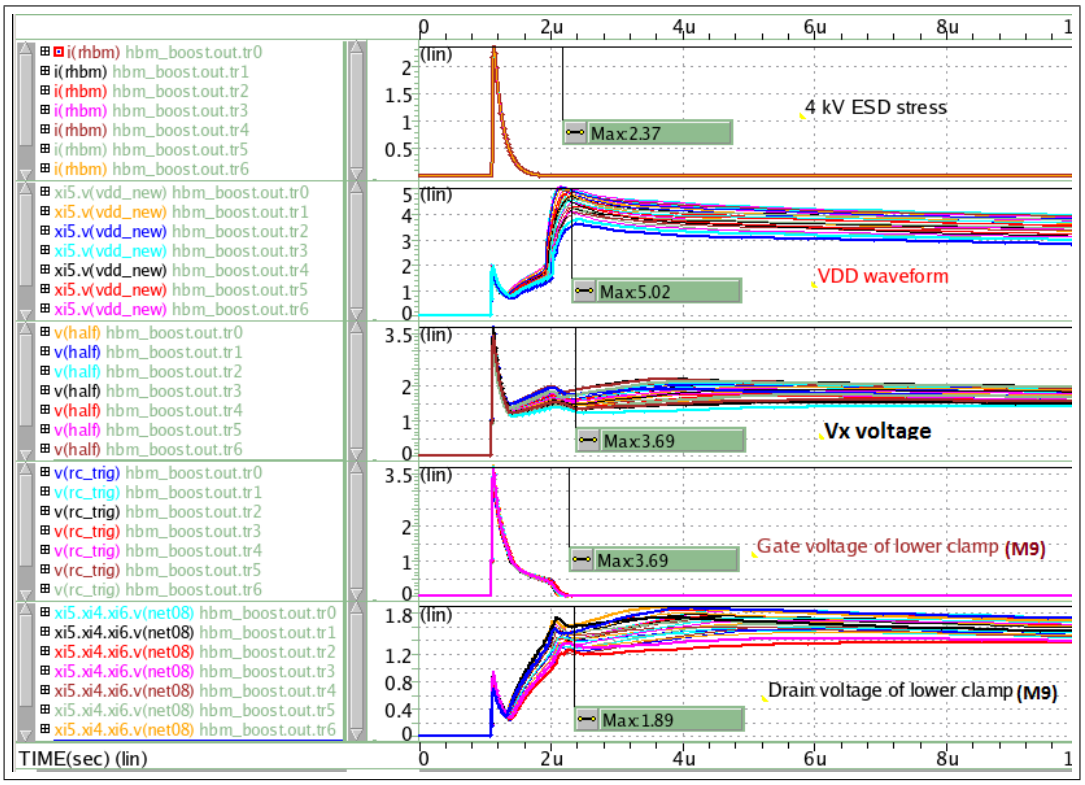

FIGURE 6.9: HBM cross corner simulation with boost trigger topology.

6.2.2 MM Test Results

In this section, MM simulations are shown for 200 V ESD stress. Fig. 6.10 presents MM simulation for corresponding 4 A current stress at TT corner. It is clear from the simulation result that the given clamp is able to discharge the ESD stress even at relatively smaller clamp size. Fig. 6.11 shows the cross corner result of MM test with maximum voltage stress of 3.64 V across lower clamp. This increase in voltage stress is due to the fact that gate voltage is actually increased in boost trigger topology but this increase is within the safe limits of device operation.

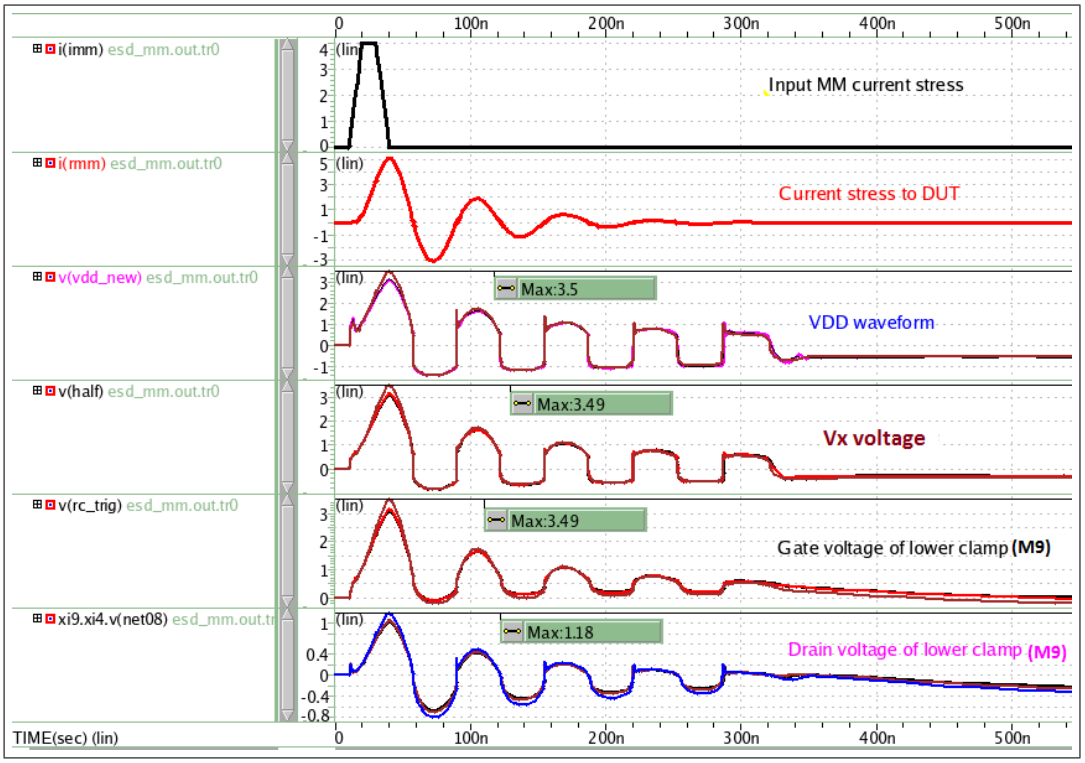

FIGURE 6.10: MM simulation at TT corner with boost trigger topology.

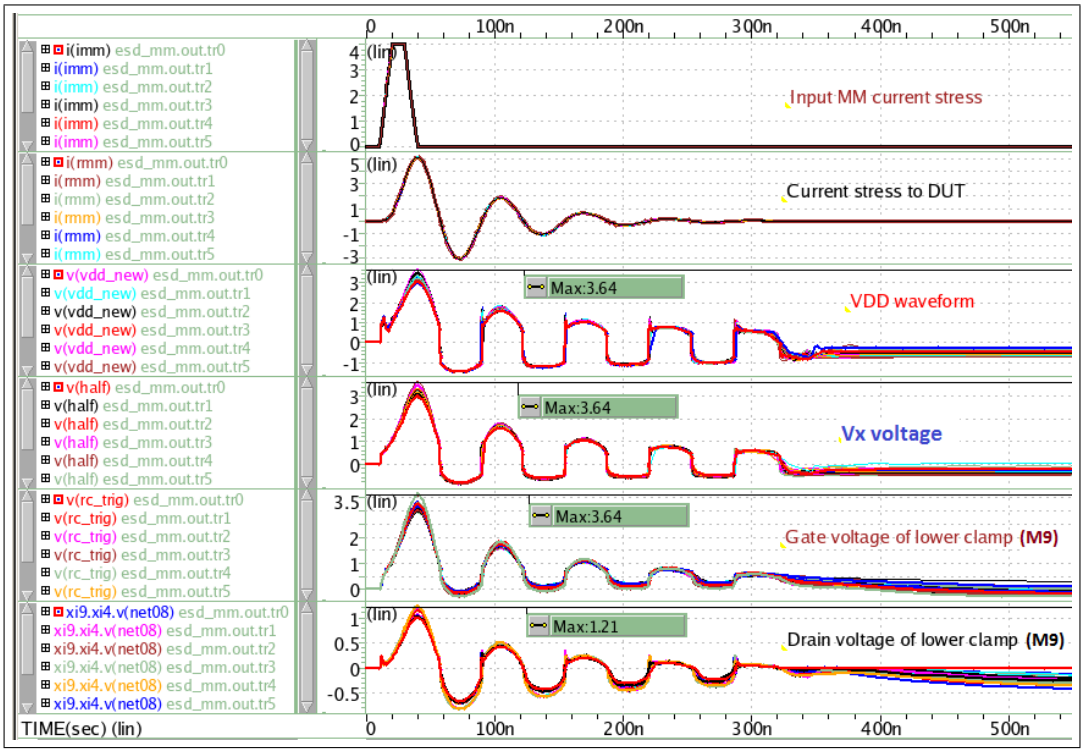

FIGURE 6.11: MM cross corner simulation with boost trigger topology.

6.2.3 Current Analysis

In this section, DC and inrush current simulations of the proposed ESD protection circuit with boosted rail topology is presented.

Fig. 6.12 shows the static current waveform of the circuit at normal power-on condition. It clearly shows that static current through the circuit is reduced by almost 4 times as compared to previous design because of smaller clamp size. The worst case static current is observed at FF corner $125°C$ with the current value of 3.48 μA at supply voltage of 3.6 V. Maximum current at TT corner is 1.69 μA.

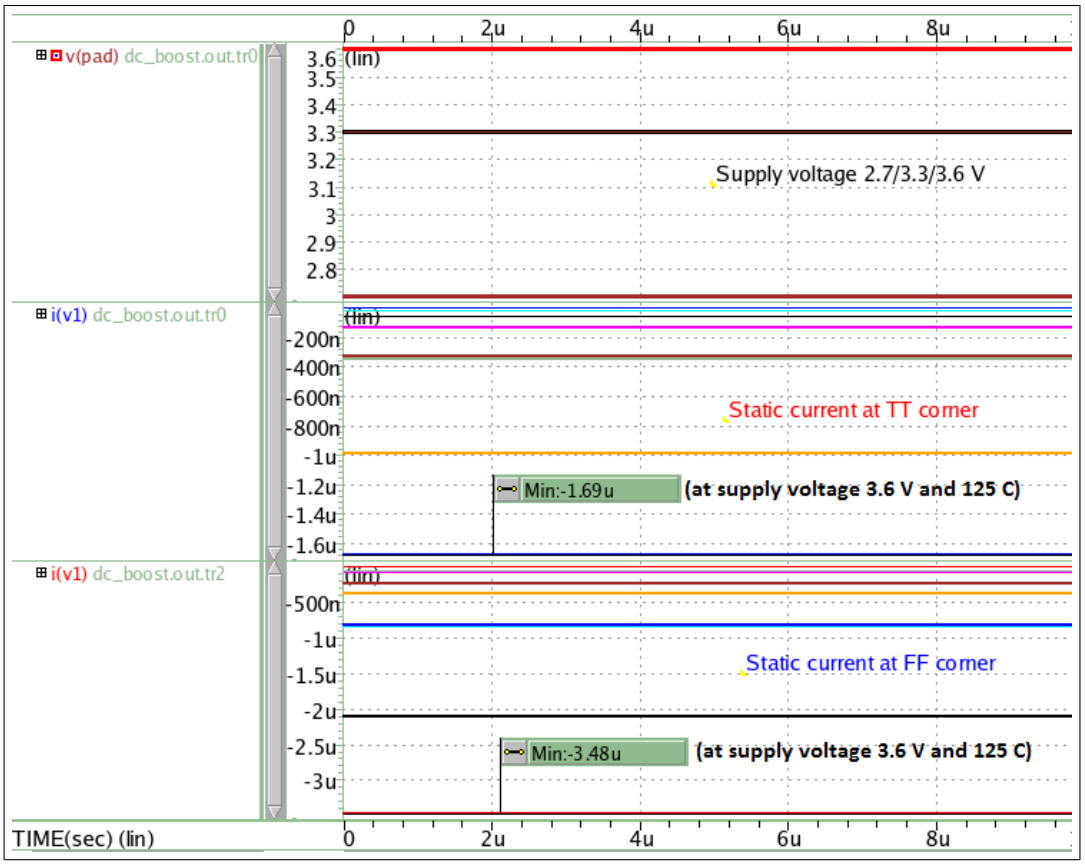

FIGURE 6.12: Static current at TT and FF corner with boost trigger.

Fig. 6.13 and Fig. 6.14 shows the cross corner inrush current characteristics with the applied voltage for the improved design. Maximum inrush at $4\mu s$ ramp rate is found to be 112 μA at $125°C$ and supply voltage of 3.6 V, which is almost 2.5 times lesser than the previous design. This is because of the reduction in clamp size. Further, as shown in Fig 6.14 that ESD clamp triggers at $1\mu s$ ramp rate, which result in large inrush current similar to the basic proposed design. Therefore, this IO design can also support of minimum $4\mu s$ ramp rate.

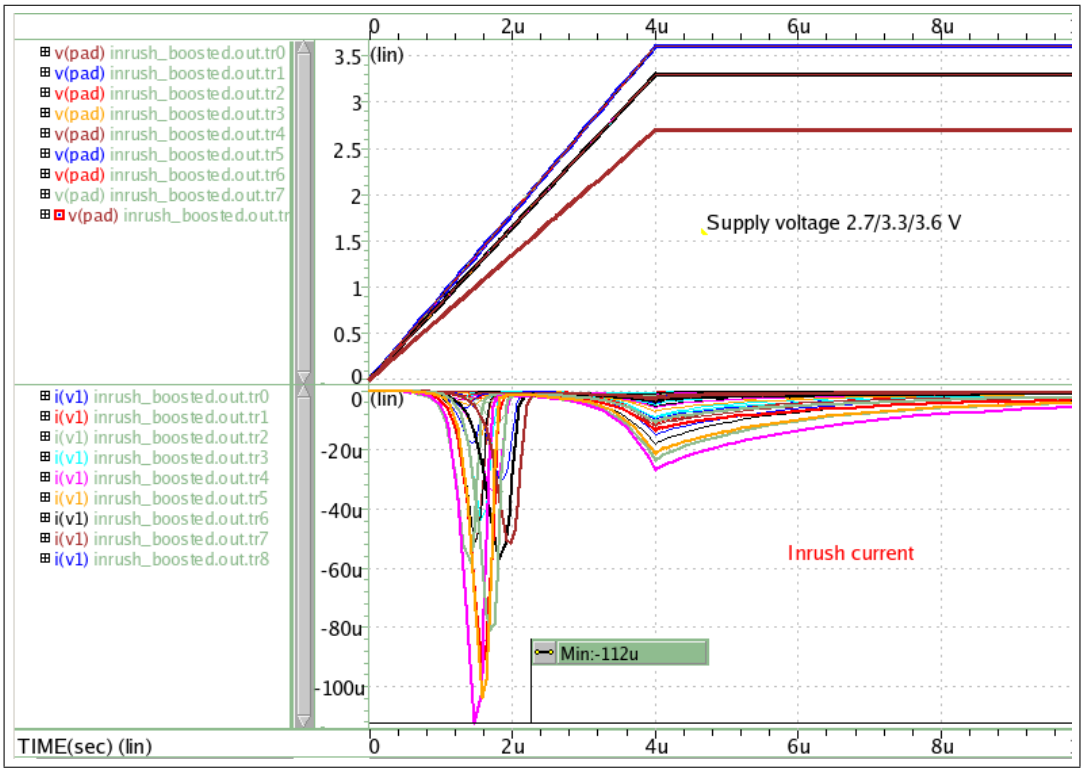

FIGURE 6.13: Inrush current cross corner plot at $4\mu s$ ramp rate with boost trigger.

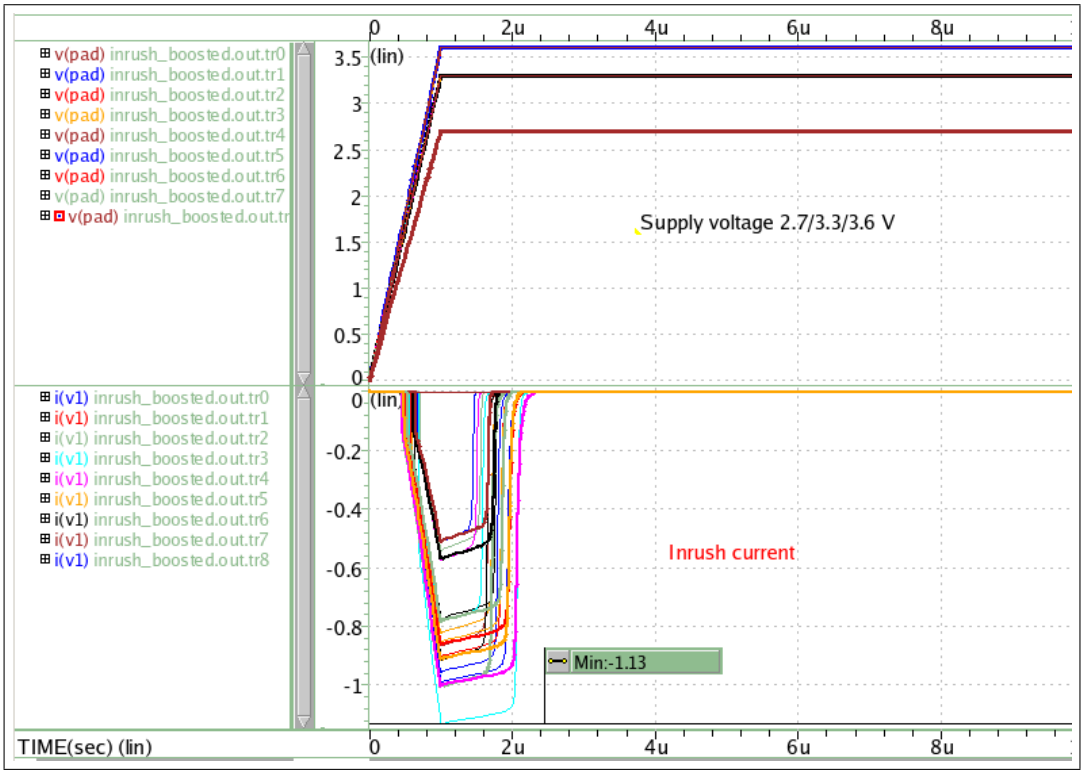

FIGURE 6.14: Inrush current cross corner plot at $1\mu s$ ramp rate with boost trigger.

6.2.4 False Triggering

One of the important challenge in the ESD protection design is the false triggering issue. Because RC delay is wide enough, which increases the susceptibility to false triggering during power-up condition.

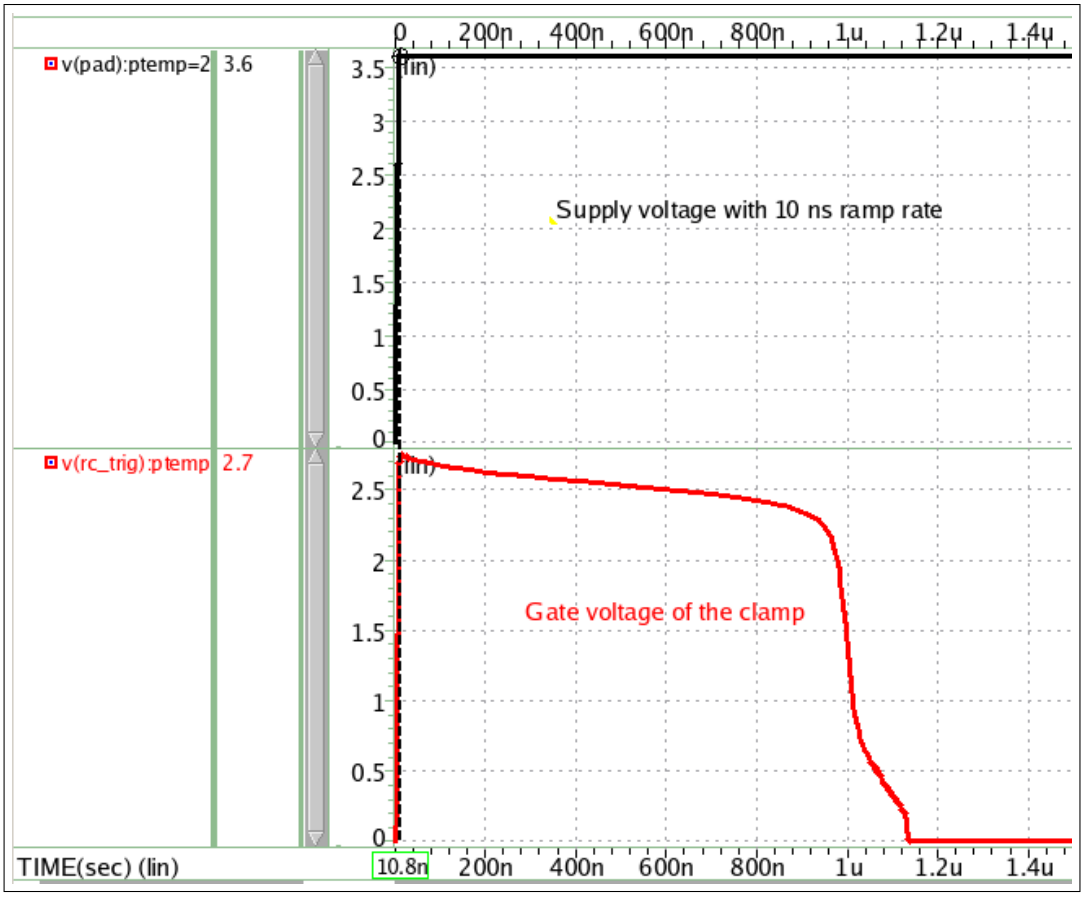

FIGURE 6.15: Turn on time of clamp at 10ns rise time.

Fig. 6.15 shows the turn on time of the clamp in case of any event with ramp rate of 10 ns that is equivalent to HBM rise time. It can be noted that clamp is in the on state around 1 μs of time interval, which is ideally required to discharge the ESD stress. However, clamp is still in on state for the same time, if any other event with ramp rate more than HBM rise time strikes as shown in Fig. 6.16. It is evident from the simulation results that this design is sensitive to the false triggering.

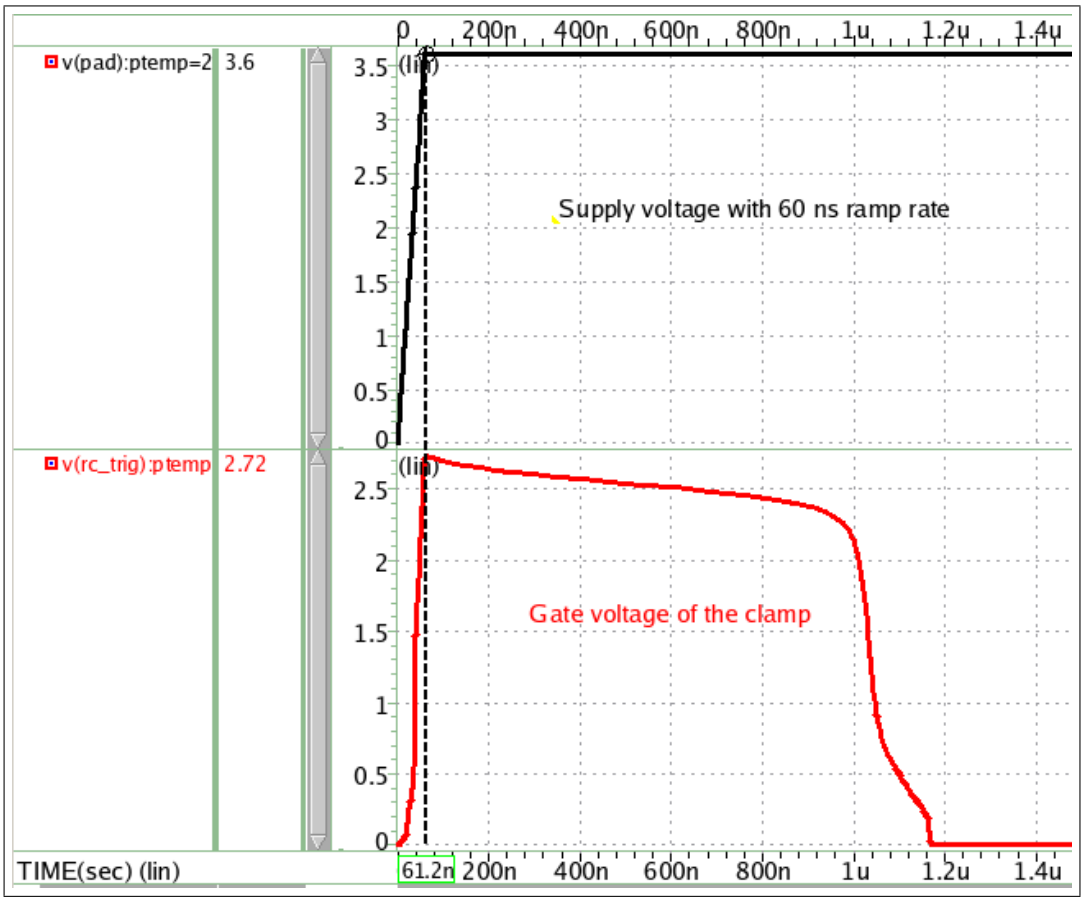

FIGURE 6.16: Turn on time of clamp at 60ns rise time.

6.3 Proposed High Voltage Tolerant ESD Protection Design with 2 Stage RC and Boost Trigger

This section presents simulation results of the proposed cascoded ESD design with boost trigger topology (see Fig. 5.4) and 2 stage RC network (see Fig. 5.5). One RC element is used to detect the ESD event and other RC network to control the on-time of the clamp. This final proposed circuit takes the advantage of high voltage tolerance, boosted rail clamp technique and 2 stage RC topology. Design parameters are kept same as previous one. These simulations are presented for the cascoded ESD protection circuit in which resistor divider to generate HALF is implemented using boost trigger topology as shown in Fig. 5.4, while clamp stage is implemented using 2 stage RC as shown in Fig. 5.5.

6.3.1 HBM Test Results

In this section, HBM test simulations are presented for 4 kV ESD stress for final proposed design. Fig. 6.17 shows the HBM simulation results at TT corner. HBM simulation results are much similar to that of HBM results of boost trigger circuit. Fig. 6.18 shows

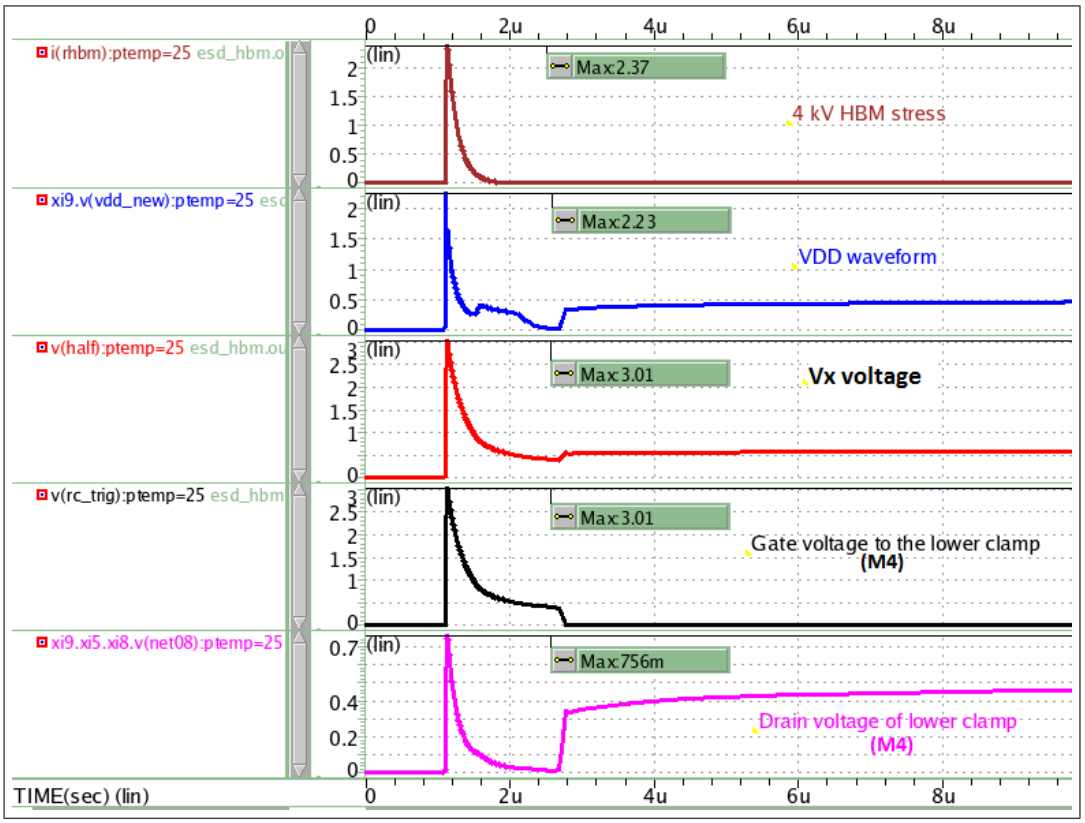

FIGURE 6.17: HBM simulation at TT corner for proposed design (Fig. A.1).

the cross corner simulation result of HBM test with maximum stress of 3.57 V, which is least as compared to the previous designs.

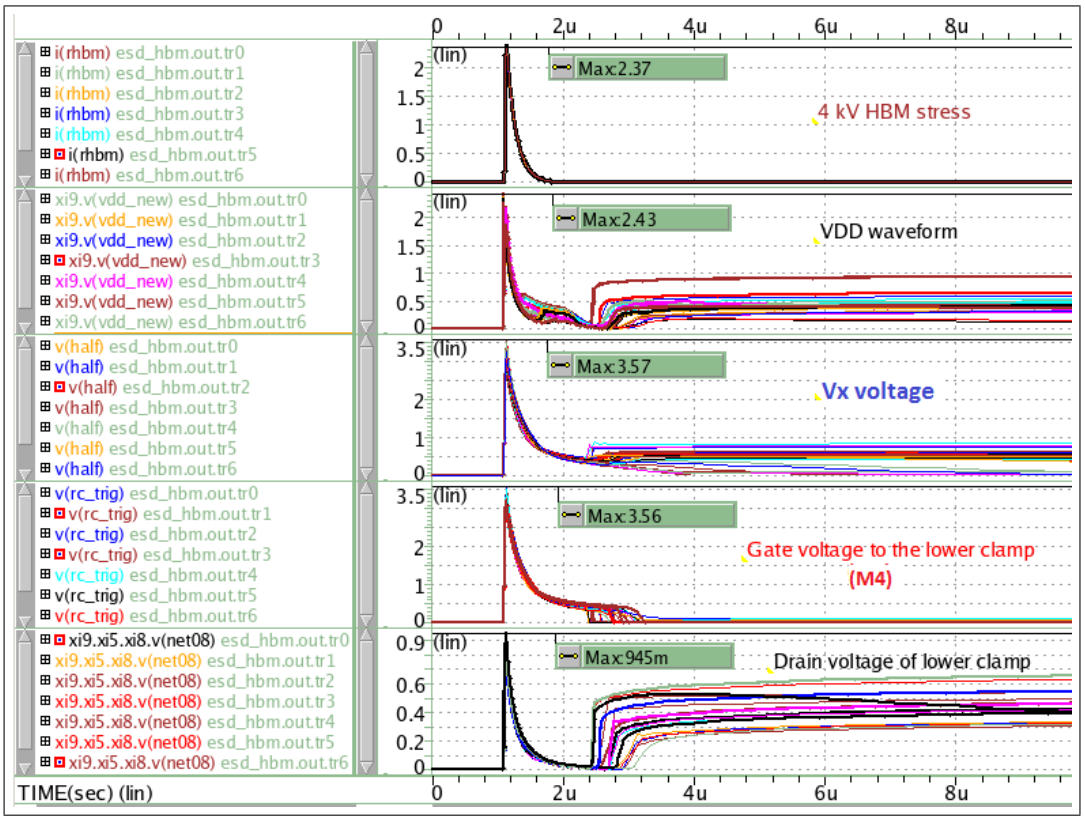

FIGURE 6.18: HBM cross corner simulation for proposed design (Fig. A.1).

6.3.2 MM Test Results

In this section, MM simulations are presented for 200 V ESD stress. Fig. 6.19 shows the MM simulation results for corresponding 4 A ESD current stress at TT corner. It can be noted that the clamp is able to discharge the ESD stress at corresponding input current stress. Further, MM response of this design decays much faster as compared to the previous design because of sufficient RC delay and enough clamp size. Fig. 6.20 shows the cross corner result of MM test with maximum voltage stress of 3.42 V, which is within the safe limits of device operation.

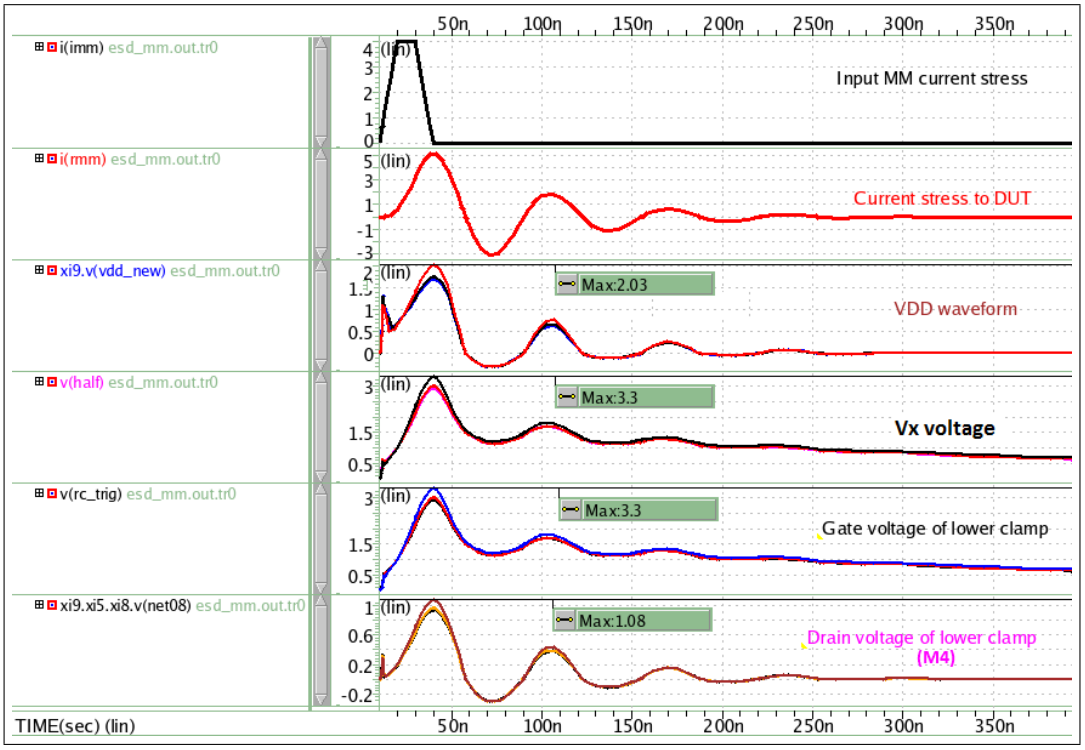

FIGURE 6.19: MM simulation at TT corner for proposed design (Fig. A.1).

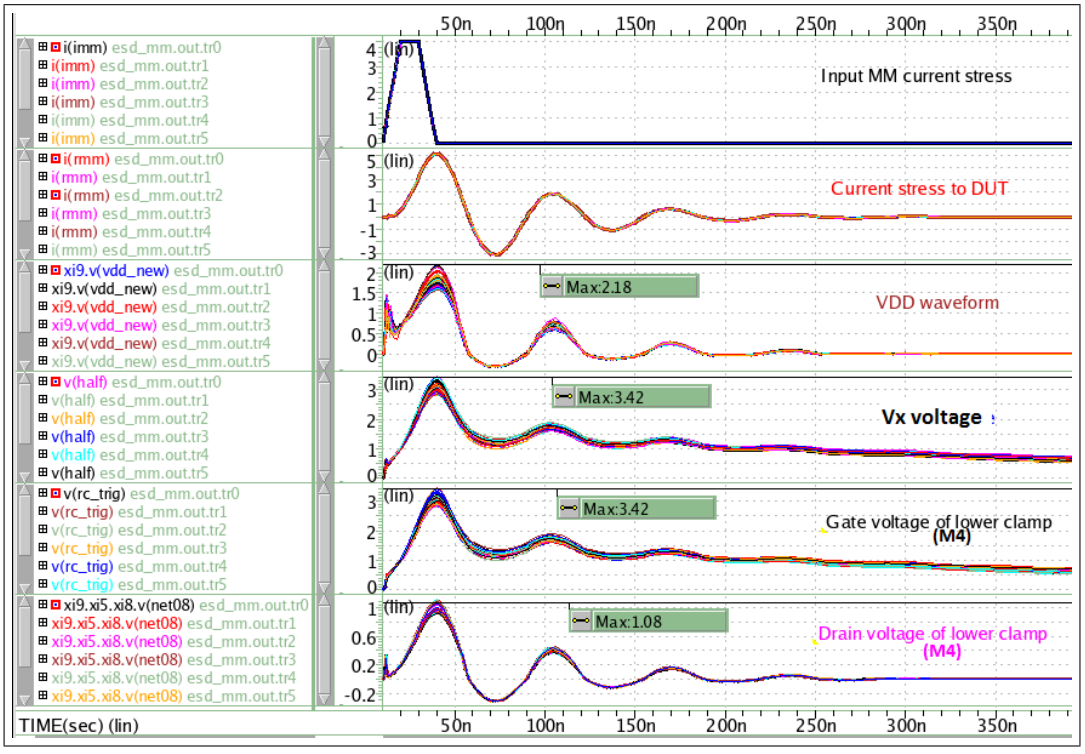

FIGURE 6.20: MM cross corner simulation for proposed design (Fig. A.1).

6.3.3 Current Analysis

In this section, DC and inrush current simulations of the proposed ESD protection circuit with boost trigger and 2 stage RC is presented.

Fig. 6.21 shows the static current through the design at normal power on condition. The DC current characteristics of this design is similar to the previous one with maximum current of 3.74 μA at FF corner and 125°C. Static current almost remains the same because of same clamp size and PMOS resistor ladder as previous design.

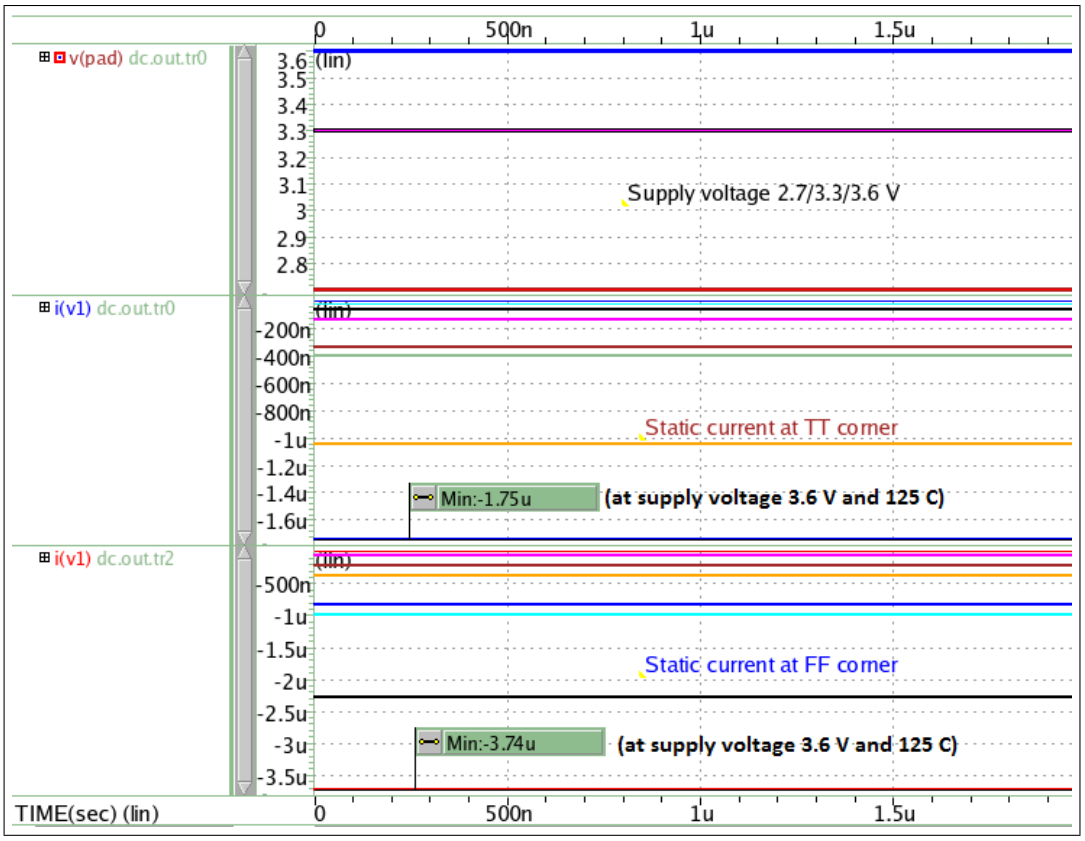

FIGURE 6.21: Static current at TT and FF corner for proposed design (Fig. A.1).

Fig. 6.22 and Fig. 6.23 shows the cross corner inrush current characteristics for the proposed complete design at 4μs and 70 ns ramp rate respectively. It can be observed that inrush current is reduced to larger extent. This is because of reduction in capacitance value in the first stage RC. Maximum inrush at 4μs ramp rate is just 5.76 μA, which is much lesser as compared to the previous designs. Further, as shown in Fig. 6.24 that ESD clamp triggers at 60 ns ramp rate. Therefore, this IO design can support minimum of 70 ns ramp rate, which is the best possible result in state of art for the given inrush specification.

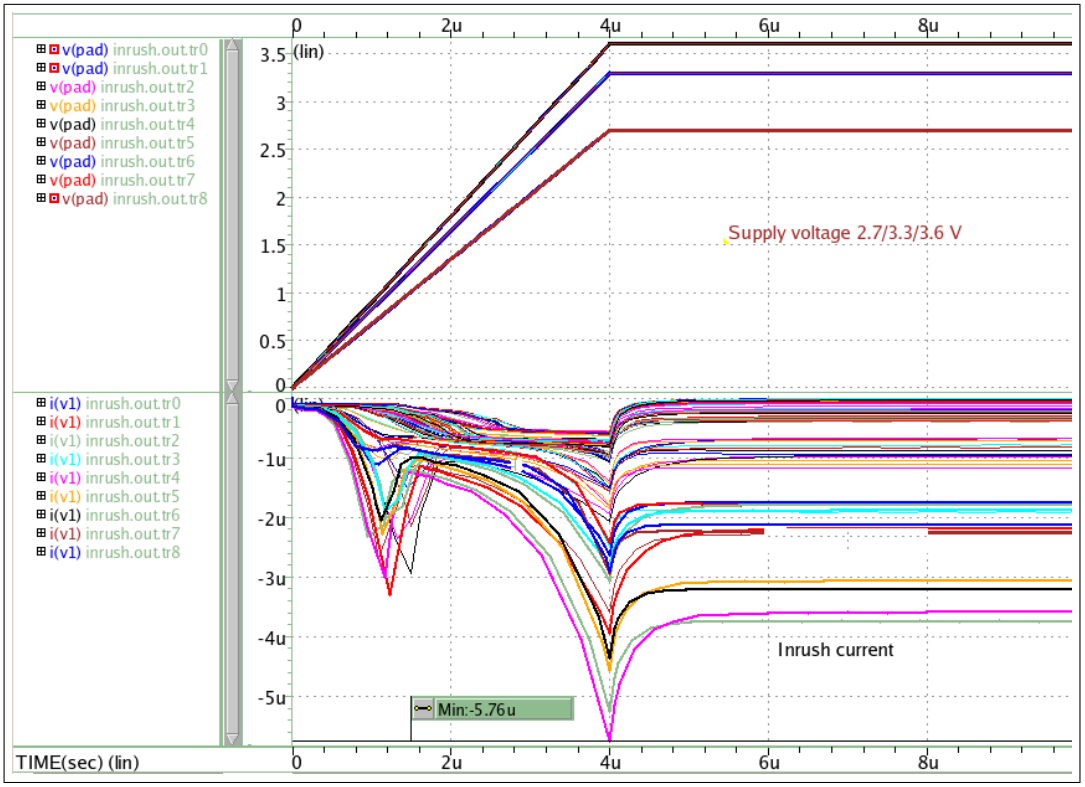

FIGURE 6.22: Inrush current cross corner plot at $4\mu s$ ramp rate for proposed design (Fig. A.1).

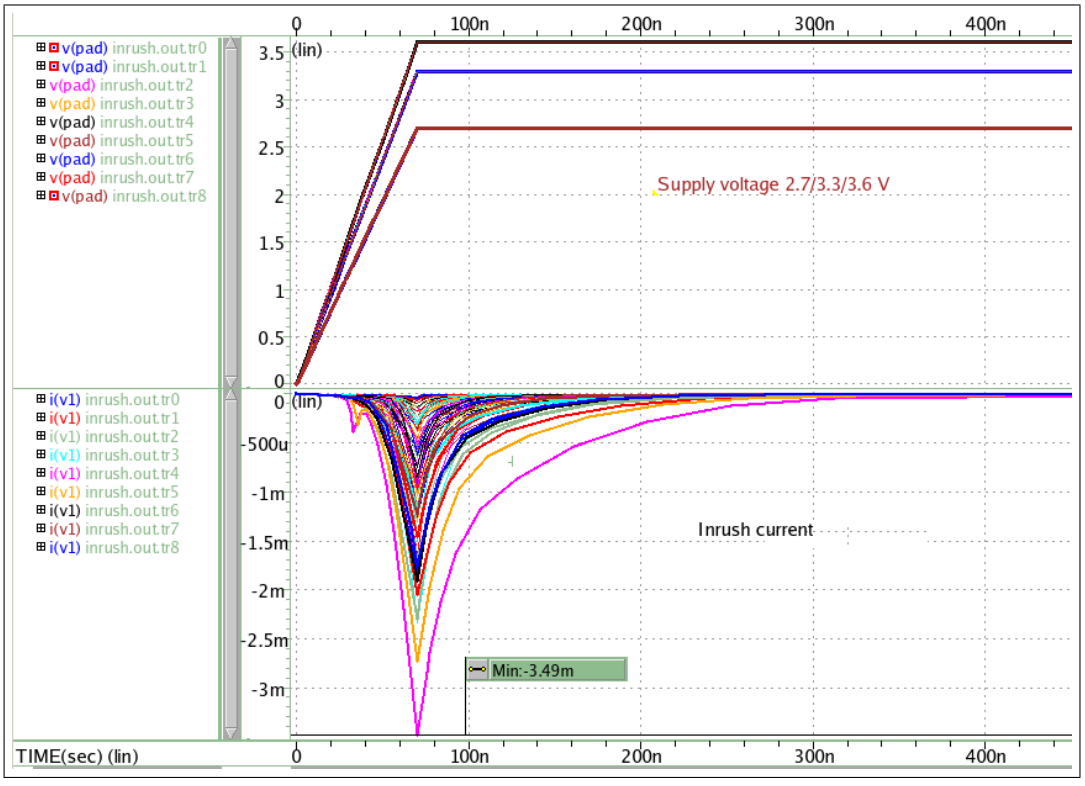

FIGURE 6.23: Inrush current cross corner plot at 70ns ramp rate for proposed design (Fig. A.1).

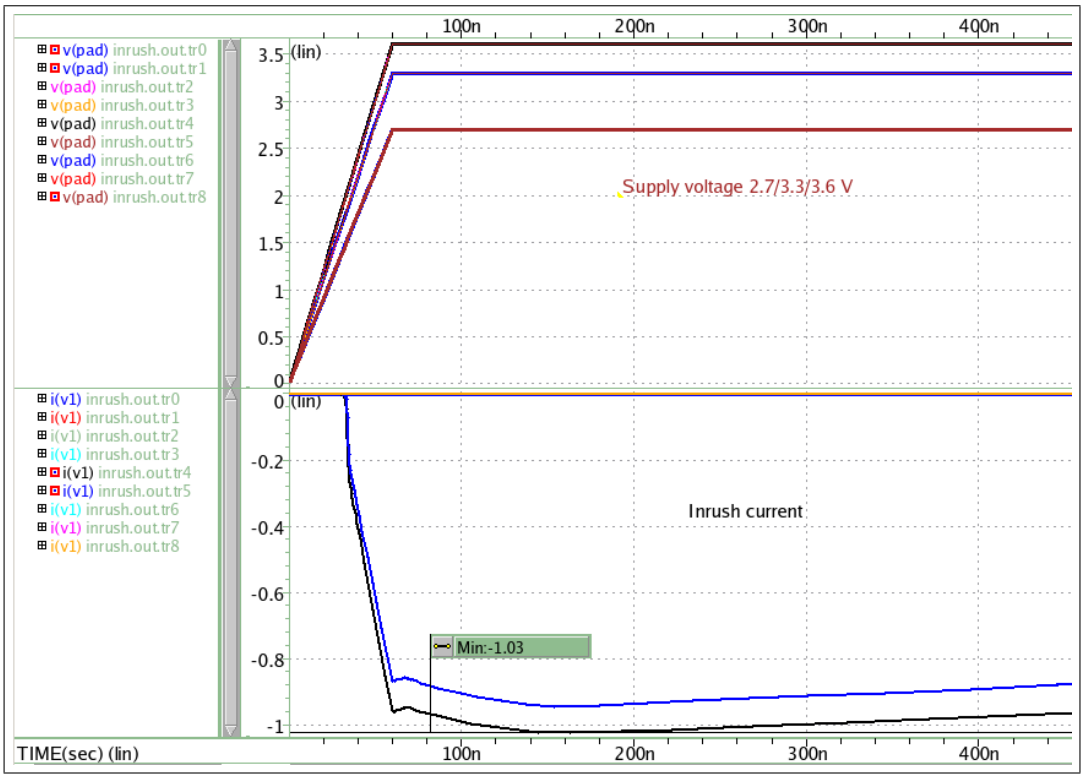

FIGURE 6.24: Inrush current cross corner plot at 60ns ramp rate for proposed design (Fig. A.1).

6.3.4 False Triggering

Fig. 6.25 shows the turn on time of the clamp for ramp rate equivalent to HBM rise time. It is obvious that clamp must be in the on state for this ramp rate. It can be noted that for any ramp rate more than HBM rise time does not trigger the clamp in any situation as shown in Fig. 6.26. It is clear from the simulation results that this design is immune to the false triggering and will only triggers in case of any ESD event. In case of 2 stage RC, first stage RC is in the range of 10-20 ns so it will not trigger at any rising pulse more than ESD rise time.

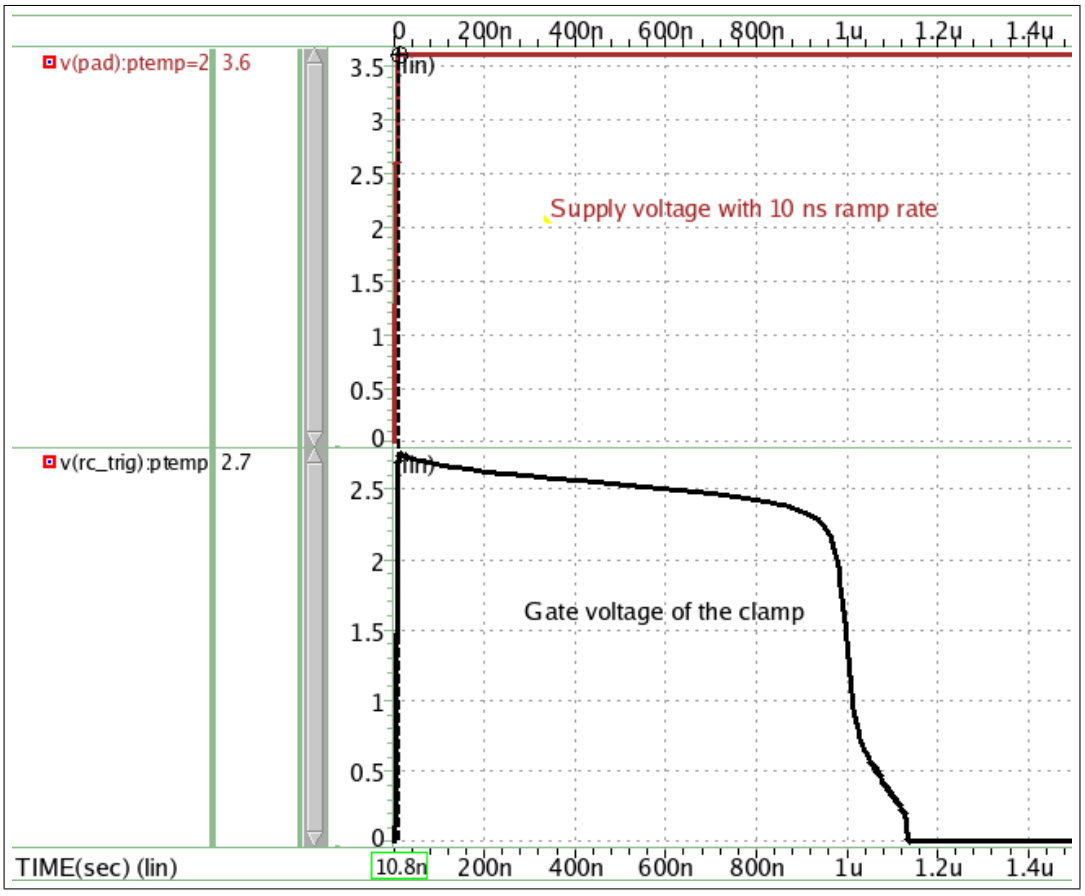

FIGURE 6.25: Turn on time of clamp at 10ns rise time.

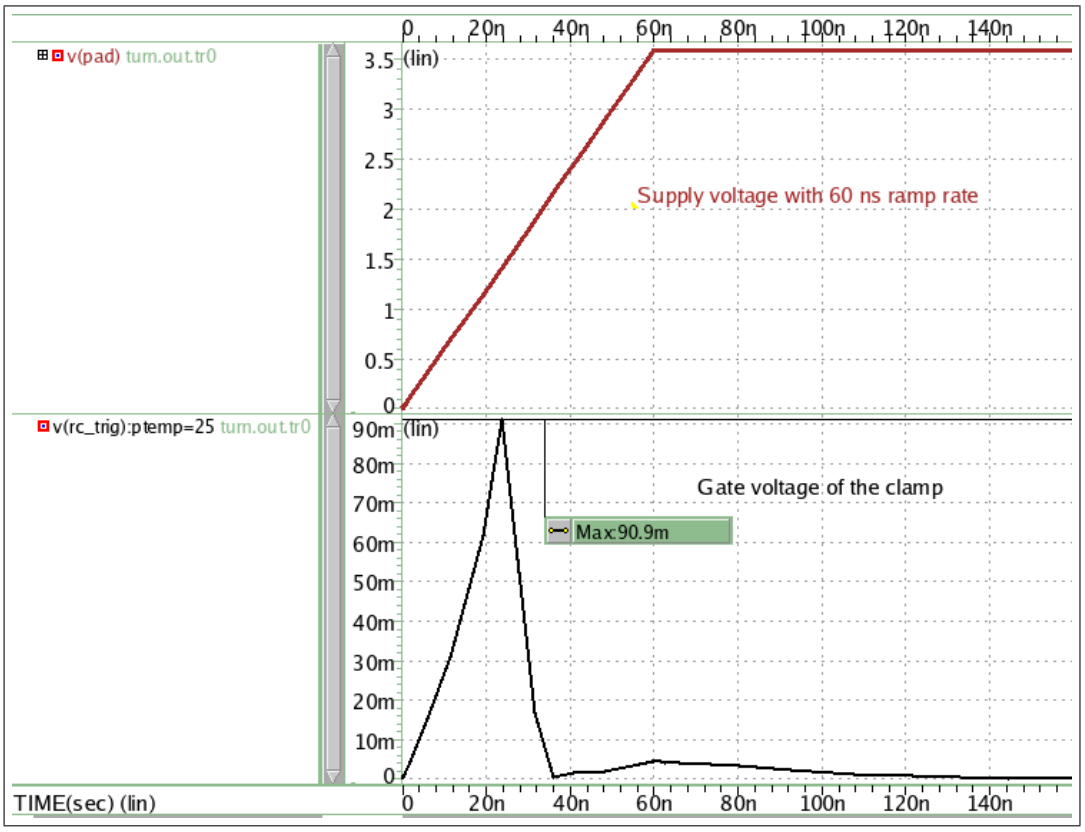

FIGURE 6.26: Turn on time of clamp at 60ns rise time (which is much higher than the typical ESD rise time).

6.4 Discussions

Table 6.1 presents the inrush comparison with the state of art work [24]. For DC biasing of 3.3 V, inrush current for $4\mu s$ ramp rate is $3.94\mu A$, which is much lesser than the $4.49\mu A$ inrush current at $10\mu s$ ramp rate for the design reported in [24]. The state of art work is reported to get trigger at 100 ns ramp rate for DC biasing of 1.2 V. While, this proposed design is getting triggered at 50 ns ramp rate, even at 3.3 V. This design can support minimum ramp rate of 60 ns in normal power-on condition for 3.3 V (nominal supply voltage), which is the best possible supportable ramp rate of I/O design in the state of art.

The performance parameters for the proposed design with different ESD optimization techniques is reported in Table 6.2. It can be clearly observed that the maximum inrush current at $4\mu s$ ramp rate is reduced to large extent due to smaller capacitance value for proposed design with 2 stage RC. Further, static current is reduced by approximately 4 times due to smaller clamp size. In addition, this proposed design is immune to the false triggering and can support minimum ramp rate of 70 ns against PVT variations.

Table 6.1: Inrush comparison with state of art

Voltage ramp rate	**This work (V_{DD}=3.3 V)**	**[24] (V_{DD}=1.2 V)]**
10μs	less than 3.9 μA	4.49 μA
1μs	12.8 μA	14.7 μA
100 ns	1.31 mA	Mistriggers
60 ns	2.96 mA	Mistriggers
50 ns	Mistriggers	Mistriggers

Table 6.2: Comparison with baseline circuit

Parameter	**Proposed work with boost trigger and 2 stage RC**	**Baseline circuit with boost trigger**	**Proposed baseline circuit (cascoded clamp)**
Max inrush at 4 μs ramp rate	5.76 μA	112 μA	247 μA
Minimum ramp support	70 ns and above	4 μs and above	4 μs and above
Clamp size	922 μm/0.15 μm	922 μm/0.15 μm	1475 μm/0.15 μm
False Triggering	Immune	Sensitive	Sensitive
Static Current	3.74 μA	3.48 μA	13 μA

Table 6.3 presents the overall design comparison with the state of art work. This proposed design is implemented in 16 nm FINFET technology, which consists of cascoded clamp type structure. It is a novel design structure, which can support 3.6 V bias stress (double the V_{DD} value) inspite of 1.8 V V_{DD} device. Further, this design can support maximum of 4 kV HBM stress as per industry standards. Clamp size used in the design for 4 kV stress is much lesser than the state of art design. This proposed design is immune to the false triggering as shown in Fig. 6.26. Further, this design can support minimum ramp rate of 70 ns against PVT variations for normal power-on mode as shown in Fig. 6.23, which is the best possible supportable ramp rate of I/O design in the state of art work.

TABLE 6.3: Overall design comparison with state of art

Parameter	**This work (Cross corner)**	**[25]**	**[26]**	**[27]**	**[24]**	**[28]**
Process	16nm FINFET	65nm	65nm	180nm	90nm	40nm
Clamp type	Cascoded	Single	Single	Single	Single	Single
Supply voltage	2*V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
Max HBM Stress	4 kV	4 kV	1 kV	10 kV	3 kV	2 kV
Clamp size	922 μm/0.15 μm	1.2 mm/0.28 μm	1.2 mm/0.28 μm	2 mm/0.18 μm	4 mm/0.9 μm	1.64 mm/0.1 μm
Minimum ramp support	70 ns	-	-	-	1 μs	200 ns
False Triggering	Immune	Immune	Immune	Sensitive	Sensitive	Partially immune
Static Current	3.74 μA	2.18 μA	4.97 μA	-	-	2.54 μA

Chapter 7

Conclusion

The designs and challenges of the ESD protection circuit were studied in detail. Further, several ESD design optimization techniques were analyzed and implemented to get the robust ESD performance to eliminate the existing design challenges.

Various topologies have been presented to address limitations such as clamp area, high inrush current and false triggering. Initially, a high voltage tolerant circuit design is proposed, which has its applications in mobile phones, flash drives etc. Then to reduce the clamp area and optimize the design, boosted rail clamp topology is implemented along with the proposed design. Layout of the design shows that it has reduced the clamp area around 38% and static current by approximately 4 times (observed from simulations). In order to get rid of the challenges, such as high inrush current and false triggering issues, the RC stage has been implemented using 2 stage RC. Finally, this proposed design is able address almost all the existing design challenges of the ESD protection circuit. This circuit can work at double supply voltage i.e. 3.6 V (inspite of 1.8 V_{DD} device), has less area, least inrush current as per given specifications and can support minimum ramp rate of 70 ns in normal power-on condition, which is the best possible supportable ramp rate of I/O design in the state of art. In addition, this proposed circuit supports hot insertion as it is not getting triggered at given 500 ns ramp rate. Thus, this design supports plug and play feature. This circuit design is completely immune to the false triggering and can support for 4 kV HBM test model as per the setup used. So far, no work has been reported for high supply ESD protection circuit in 16 nm FINFET technology.

Complete ESD protection circuit design is developed in TSMC 16nm FinFET technology at Western Digital and variations with process, voltages and temperatures have been thoroughly studied and presented.

7.1 Future Work

In the current work, transient clamp is used to realize the ESD protection circuit and simulations have been performed at schematic level. As a future work, post layout simulations can be done to verify the design robustness against parasitic capacitances and resistances.

Appendix A

Circuit Schematics

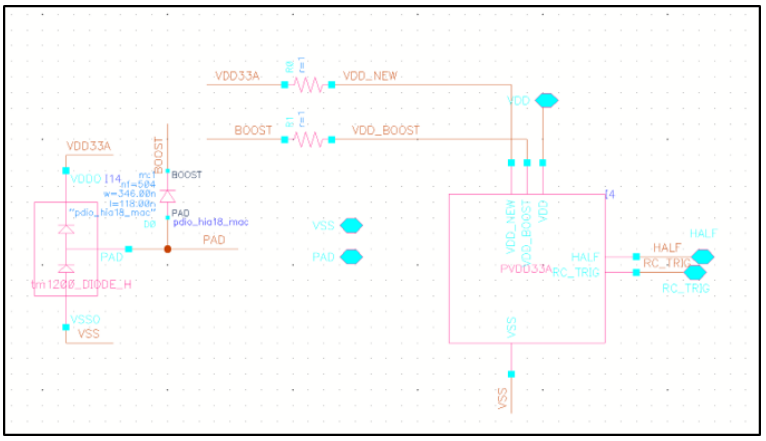

FIGURE A.1: Overview of proposed circuit.

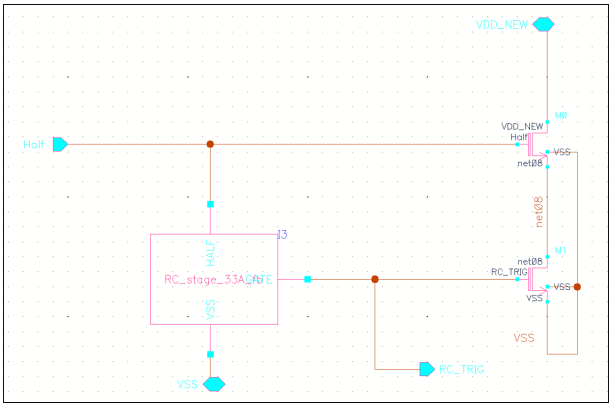

FIGURE A.2: Clamp stage.

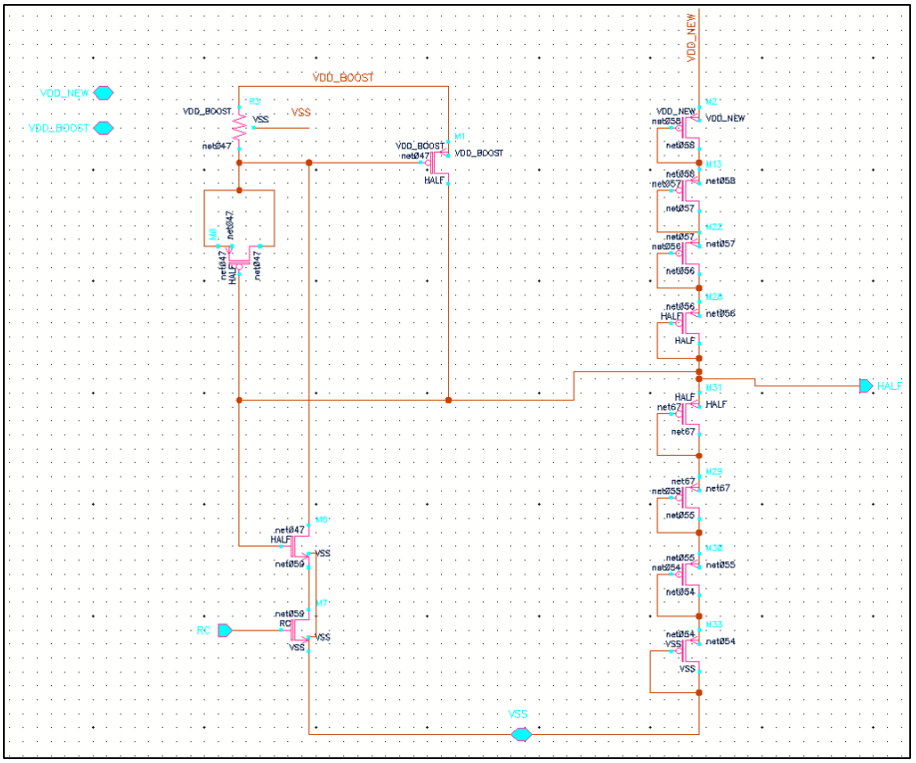

FIGURE A.3: Resistor divider network to generate V_X.

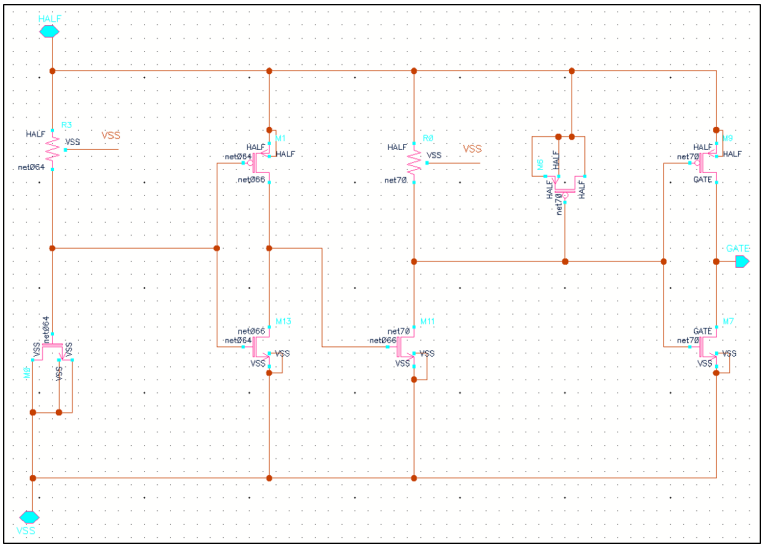

FIGURE A.4: 2 stage RC network.

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