DESIGNING IMPEDANCE MATCHING NETWORKS FOR RF AND MICROWAVE DEVICES AND APPLICATIONS

By

VIKAS VIKRAM SINGH

Under the Supervision of Dr. M. S. HASHMI

Indraprastha Institute of Information Technology Delhi
April, 2020

DESIGNING IMPEDANCE MATCHING NETWORKS FOR RF AND MICROWAVE DEVICES AND APPLICATIONS

By

VIKAS VIKRAM SINGH

Submitted

in partial fulfillment of the requirements for the degree of
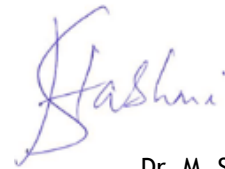
Master of Technology

to

Indraprastha Institute of Information Technology Delhi
April, 2020

Certificate

This is to certify that the thesis titled "Designing Impedance Matching Networks for RF and Microwave Devices and Applications" being submitted by Vikas Vikram Singh to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

April, 2020

Dr. M. S. Hashmi

Department of Electronics and Communication Engineering

Indraprastha Institute of Information Technology Delhi

New Delhi 110 020

ACKNOWLEDGEMENTS

First of all, I would like to thank Professor **Dr. M. S. HASHMI** for providing me an opportunity to work on this project under his supervision and guiding me throughout the project. I would also like to thank Mr. Rahul Gupta for the help and advice throughout the project. I also wish to thank my family for their continuous support and encouragement throughout my studies. I especially wish to thank my mother Mithla Singh, my father Saket Kumar Singh for continuous encouragement and support.

I am also thankful to all my friends at IIIT Delhi for encouraging and supporting me whenever I needed their help.

Table of Contents

List of Figures

List of Tables

1. Introduction

Impedance matching or impedance transforming circuits (networks) are one of the most ubiquitous blocks in a host of RF/microwave components and systems. One of the motivations to use impedance matching networks comes from the ***maximum power transfer theorem***. A voltage source V_s with its source resistance connected to the load R_L is shown in Fig. 1.1(a). Variation of the power delivered to the load, P_L is shown in Fig. 1.1(b). It is evident from Fig. 1.1(b) that P_L is maximum when $R_L=R_S$. This result is known as the condition for maximum power transfer. If the source and the load were a complex quantity, $R_L=R_S^*$ holds true, where asterisk denotes a complex conjugate quantity. Since, in general, in RF/microwave components such as in amplifier, the impedance looking into the gain device is different than the source impedance; a matching network is required to transfer maximum power from the source side to the load side. Two points must be noted in this context. First, need of matching is not always motivated from the maximum power transfer theorem. Sometimes, such as in low-noise amplifiers or in wideband amplifiers, matching (other than conjugate) is used to trade- off among noise, bandwidth and gain requirements [2-3]. Second, amplifiers are not the only devices where a matching circuit is required. In fact, matching network is such a ubiquitous block in RF/Microwave devices and systems that "***they are everywhere***". Some applications of matching networks in RF/microwave devices are highlighted in the next few paragraphs.

(a)   (b)
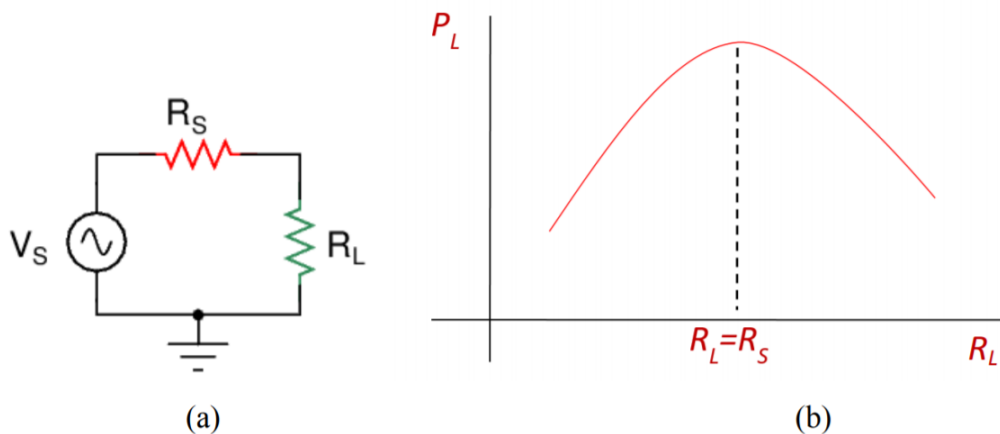
Figure 1.1 (a) Voltage source connected to a load (b) Power delivered to the load versus the load value.

1.1 Contributions Of This Thesis

After an extensive research survey on impedance transformation circuits, presented in the coming chapters, it was identified that the existing state-of-art has severe limitations. It is, therefore, extremely important to investigate and propose novel solutions to address those limitations in the existing design approaches. This thesis has been pursued to contribute into this direction and to address some of the concerns. The scope, objectives, and the contributions of this thesis are briefly outlined below.

1.2 Scope Of This Work

With regard to the scope and limitations of this thesis, few important points must be borne in mind. Firstly, the impedance matching networks presented in this thesis are intended for establishing matching at fundamental frequencies. Passive components, such as the Wilkinson power divider, shown later in Fig. 1.2 require matching at fundamental frequencies. The power amplifiers, especially the high efficiency PAs, however, require proper matching at harmonic frequencies as well. Fortunately, as reported in [4], the fundamental matching network could always be designed independent of the required harmonic terminations and, therefore, the techniques discussed in this thesis would also be of significant interests to the PA designers.

Secondly, the bandwidths of matching networks are not emphasized as is customary in the literature of multi-frequency matching network. The reason is that the notion of bandwidth is a vague idea when the loads become frequency dependent. And, more importantly, this figure of merit is not that crucial in multi-frequency design as it is in wide-band design. If the same bandwidth performance is sought from a multi-frequency circuit as it is mandated in wideband design, then there is no need to go for multi- frequency design in the first place. It is perhaps this reason that the reported multi- frequency designs have as low as 30MHz bandwidth [5-6].

Finally, it must be noted as well that the impedance matching network prototypes shown in this thesis are essentially one-port devices terminated into the considered loads. Therefore, only the measured return-losses, that is, reflection in terms of S_{11} or Gamma have been depicted for them. It should also be noted that insertion loss is

direct function of the return loss assuming that no radiation/conductive/dielectric losses exist in structure. These losses are often negligible at low RF frequencies and for transmission line-based structures built properly in low loss dielectric substrate.

1.3 Outline Of The Thesis

Chapter 1 is the Introduction of the thesis. It contains the brief discussion on why impedance matching is needed in various areas. In this section scope, objective and outline of this thesis is also discussed.

Chapter 2 contains background and related works associated with impedance matching. In this section some devices in which impedance matching is a must requirement such as Low Noise Amplifier, Power Dividers, Antenna Feed lines etc. are discussed briefly.

Chapter 3 discuss about High Impedance Transforming Dual-Band Wilkinson Power Divider in details. We looked at the proposed architecture followed by even-odd mode analysis. We have also discussed about prototype and its measurement results.

Chapter 4, High Impedance Transforming Dual-Band Balun with Isolation and Output Ports Matching are discussed. Its design analysis and procedure have been discussed in this chapter. Application these impedances matching network is also discussed here.

Chapter 5 discuss about Utilization of Stepped Impedance Transformer in High Frequency Power Divider for Real/Complex Port Terminations. A clear analytical approach to design dual-band balun that caters to a wider range of load impedances are presented for real as well as frequency dependent complex impedances.

Chapter 6 contains Summary and conclusion of this thesis. Afterwards List of publications and References are presented in the later section of this thesis.

2. Background And Related Work

In this section we will look about the areas where Impedance matching plays a vital role. Almost all RF devices require impedance matching. Some key devices in which impedance matching is must have been discussed in below. These are some related areas of work where impedance matching is must needed.

Power Dividers: A Wilkinson power divider is shown in Fig. 1.2(a). This configuration is used for splitting power equally or for power combining. It may not be apparent if the concept of matching has to do anything here. For this purpose, even- mode equivalent circuit of the Wilkinson divider is shown in Fig. 1.2(b). It is evident now that the idea in such a situation is to *match* a real load impedance of Z_0 to $2Z_0$ using a quarter-wave line [7]. It is a fact that the characteristic impedance of the quarter-wave line must be $\sqrt{(Z_0 * 2Z_0)} = \sqrt{2}\ Z_0$ and that is exactly shown in the Wilkinson power divider of Fig. 1.2(a) [2].
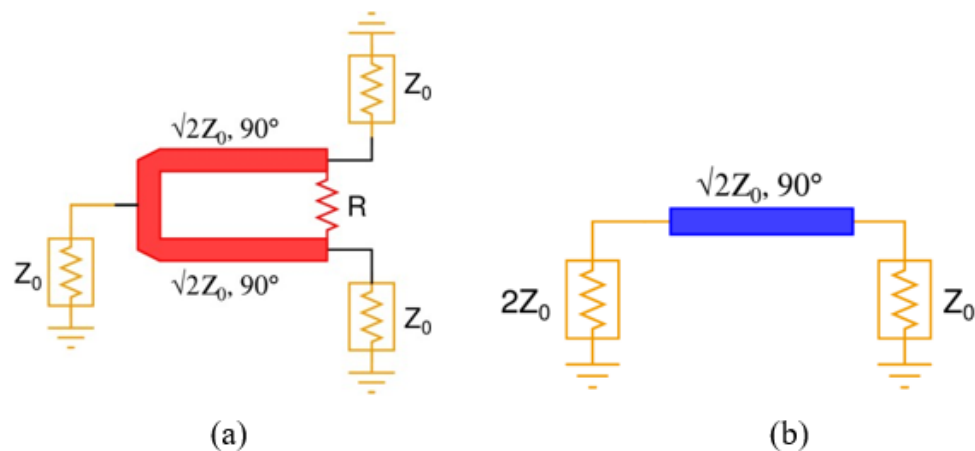
Figure 2.1 (a) A Wilkinson power divider and its (b) even-mode half circuit.

Low Noise Amplifier: Since the first aim of LNA design is to obtain minimum noise figure, input matching should be done accordingly. For an amplifier, there is an optimum source impedance, Гopt, which leads to minimum noise figure. In order to obtain minimum noise figure, input impedance of an amplifier should be matched to this optimum source impedance value. It is important to note that, however, optimum source impedance that gives minimum noise figure is not necessarily the optimum impedance for the maximum power transfer. Therefore, one must sacrifice the power gain, and therefore return loss, to obtain minimum noise figure, and vice versa in

order to optimize output signal-to-noise ratio unless those impedances are same by coincidence.

In addition to obtain minimum noise figure, one of the other challenges in LNA design is to obtain the maximum available gain. Therefore, conjugate matching should be done at the output of the amplifier in order to get the best S/N at the output of the system. If the load impedance is Z_L, then for maximum power transfer source impedance Z_S is equal to a conjugate of load impedance.

$$Z_S = Z_L^*$$

The reflection coefficient Γ is a normalized measure of the relationship between source impedance and load impedance. Input and output impedance matching is given by the input and output return loss. Return loss (RL) is the relationship between the reflected power wave at a port to incident power wave at the same port. A perfect match will have no reflection and an SWR of 1.

Antenna Feed Line: A patch antenna is shown in Fig. 1.4. The feed lines can be attached as shown in figure [7]. As one moves away from the centre of the antenna, the impedance looking into the antenna also varies. Thus, to couple maximum power from the power amplifier (PA, serving as a source to the antenna with Z_0 as the source impedance) to the antenna, the

impedance of PA and the antenna must be matched. Moreover, if the impedance level at the patch edge is matched to Z_0, it results into very thin feed lines. Therefore, an inset feed is often used.
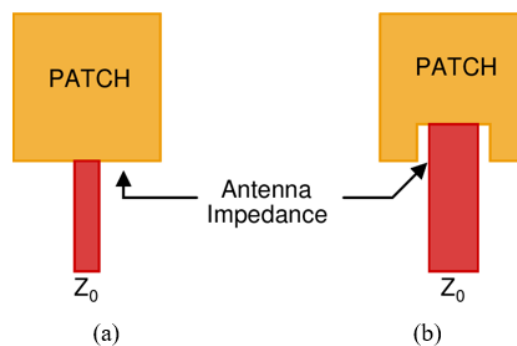
Figure 2.2 Patch antenna with feed lines. (a) edge-feed (b) inset feed

Energy Harvesting: There has been immense interest in RF energy harvesting systems. This essentially entails extraction of energy from cell phone towers or other ambient RF radiations. The motivation is to supply power to the low-energy wireless sensor nodes and wearable electronic devices whose manual maintenance would be very challenging [8-11]. Fig. 1.6 shows a typical block diagram of an RF energy harvesting system. It is obvious that an antenna would capture the ambient RF energy and pass it to a non-linear device, normally a Schottky diode, followed by a filter to suppress the ripples. This part of the system is usually termed as *rectenna*. The load includes a power management module (PMM) that would be required to store the energy. However, a very crucial block is the impedance matching network. Its purpose is to match the complex input impedance of the rectifier to the 50Ω impedance of antenna for maximum power transfer. Design of an energy harvesting system essentially involves design of the rectifier and associated matching networks.

Figure 2.3 Block diagram for RF energy scavenging system.

3. High Impedance Transforming Dual-Band Wilkinson Power Divider

In any RF/Microwave communication system, the Wilkinson Power Divider (WPD) is one of the most commonly used components. A WPD finds its application as a power divider or combiner in a phased array antenna, balanced mixers, power amplifiers and the I/Q vector modulators. The impedance transformation is the key in most of these applications [12]-[13]. Several recent reports [14]-[17] have presented the dual- and multi-band operation of a WPD in detail where miniaturized

size, low insertion loss, good isolation, wide band-ratio and high impedance ratio is the center of interest. The WPD [14] consists of complex isolation structure with lumped components though demonstrating good performance. The inherent impedance transformation, in addition, is discussed in [15]-[17] but is limited to a small range of Impedance Transformation Ratios (ITR) only. In this project, a dual-band WPD utilizing coupled-lines and Two-Section Transmission Lines (TSTL) is proposed which provides inherent impedance transformation with very high ITR. The proposed design is very useful in eliminating the need of an additional impedance transformer [IT] at the input and output ports. The design equations are provided to compute the design parameters of the design. To validate the proposed concept, subsequent sections are provided with several design examples and a working prototype. The measurement results demonstrate a good agreement with the EM simulation results.

3.1 Proposed Structure And Theoretical Analysis

Figure 1 shows the proposed dual-band WPD architecture with different input and output ports impedances. Here, port 1 is the input port, with port impedance ZS, and port 2 and port 3 are the output ports, with equal port impedance ZL. The power division at the output ports is achieved using two coupled-lines Fig. 1. The proposed Wilkinson Power Divider with Ze1 and Zo1 as the even-odd mode impedances respectively, and two TSTLs with impedances Z1 and Z2. The electrical length for the coupled-lines and the TSTLs is θ1. Another coupled-line, with Ze2 and Zo2 as the even-odd mode impedances respectively and θ2 as the electrical length, is used along

with a resistor R for the isolation between the output ports. The coupled line, here, provides a degree of freedom due to its even- and odd-mode impedances. All the characteristics impedances, in Ω, and the electrical lengths, in degrees (°). Here all the electrical lengths are defined at first frequency, i.e. f1.
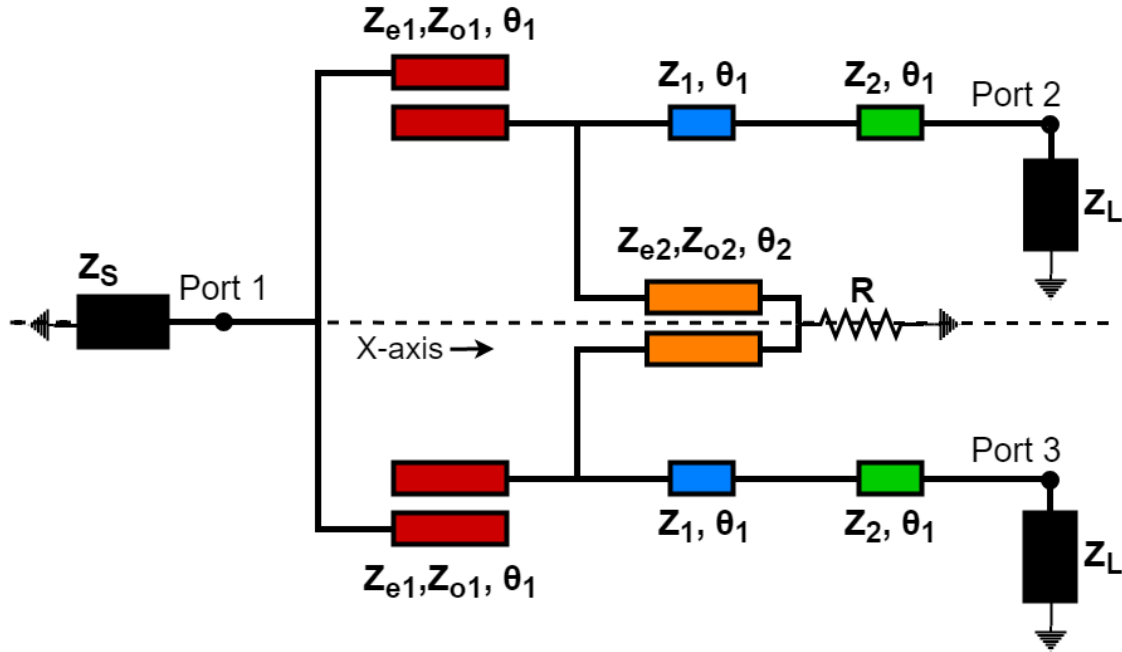
Figure 3.1 Proposed Wilkinson Power Divider Circuit

A. Even-mode analysis

Owing to the symmetry property of the proposed circuit, the even-odd mode analysis is utilized here to analyse the proposed circuit. The even-mode equivalent circuit is demonstrated in Fig. 2. In the even-mode analysis, the resistor across the X-axis is shorted to ground whereas the coupled-line is reduced to a TL with effective characteristic impedance Ze2, the even-mode impedance of the coupled-line. The respective input admittances are mentioned as Yin1e, Yin2e, and Yin3e. The term Yin1e can be expressed as (1), where Gin1e and Bin1e are mentioned in (2) and (3). The term ρ (=Ze1/Zo1) is the coupling factor of a coupled-line i.e. ratio of the even and odd mode impedance of the coupled line.

$$Y_{in1e} = G_{in1e} + jB_{in1e} \tag{1}$$

$$G_{in1e} = \frac{4Z_S(\rho-1)^2}{4\left[Z_S^2(\rho+1)^2 - 2\rho(\rho-1)^2Z_o^2\right]cos^2\theta_1 + (\rho-1)^4Z_o^2sin^2\theta_1 + 16\rho^2Z_o^2cos^4\theta_1/sin^2\theta_1} \tag{2}$$

17

$$B_{in1e} = \left(\frac{\rho+1}{Z_o}\right)\left(\frac{\left[4Z_S^2 - (\rho-1)^2 Z_o^2\right]\sin^2\theta_1 + 8\rho Z_o^2 \cos^3\theta_1 / \sin\theta_1}{4\left[Z_S^2(\rho+1)^2 - 2\rho(\rho-1)^2 Z_o^2\right]\cos^2\theta_1 + (\rho-1)^4 Z_o^2 \sin^2\theta_1 + 16\rho^2 Z_o^2 \cos^4\theta_1 / \sin^2\theta_1}\right) \tag{3}$$
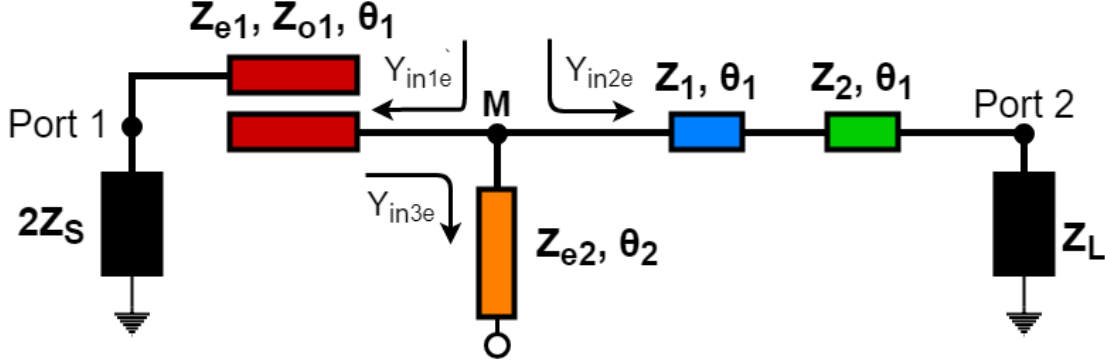
Figure 3.2: Even-mode equivalent circuit

From (2) and (3), it is apparent that the electrical length θ1 should follow (4) for the dual-band operation of the WPD [18].

$$\theta1 = \frac{(n+1)}{(r+1)}\pi \tag{4}$$

Where, the term r is the frequency ratio f2/f1. Similarly, the input admittance is $Y_{in2e} = G_{in2e} + jB_{in2e}$ where,

$$G_{in2e} = \frac{Z_L^2\left(Z_1^2\left(1+\tan^2\theta_1\right)^2\right)}{Z_L^2\left(Z_1 - Z_2\tan^2\theta_1\right)^2 + Z_1^2\left(Z1+Z2\right)^2 \tan^2\theta_1} \tag{5}$$

$$B_{in2e} = \left(1+\frac{Z_1}{Z_2}\right)\tan\theta_1\left(\frac{Z_1^2\left(Z_1 - Z_2\tan^2\theta_1\right) - Z_1^2\left(Z_2 - Z_1\tan^2\theta_1\right)}{Z_1^2\left(Z_1 - Z_2\tan^2\theta_1\right)^2 + Z_1^2\left(Z_1 + Z_2\right)^2 \tan^2\theta_1}\right) \tag{6}$$

Now in order to provide a match between the input and output ports, the real parts of Yin1e (i.e., Gin1e) and Yin2e (i.e., Gin2e) are equated. This resulted in an expression of Zo1 in (7), where Z1 and Z2 are independent variables.

$$Z_{O1} = \sqrt{\frac{4Z_S\left[(\rho+1)^2 - 4\rho + (\rho-1)^2 \tan^2\theta_2\right]\left[Z_L^2\left(Z_1 - Z_2\tan^2\theta_2\right)^2 + Z_1^2\left(Z_1 + Z_2\right)^2 \tan^2\theta_2\right] - 4Z_S^2 Z_L Z_1^2\left(\rho+1\right)^2\left(1+\tan^2\theta_2\right)^2}{\left[Z_L Z_1^2\left(1+\tan^2\theta_2\right)^2\right]\left[(\rho-1)^4 \tan^2\theta_2 + 16\left(\rho^2\tan^2\theta_2\right) - 8\rho(\rho-1)^2\right]}} \tag{7}$$

Furthermore, the stub with characteristics impedance Ze2 is used to cancel the effective imaginary admittance at node M (in Fig. 2), i.e. j(Bin1e + Bin2e)@f1 and −j(Bin1e + Bin2e)@f2. This cancellation can be achieved using a dual-band short or open-stub at this node [18].

$$
\left.\begin{aligned}
\text{Im}\left(Y_{in3e}\right) &= j\left(B_{in1e} + B_{in2e}\right) = j\left(1/Z_{e2}\right)tan\theta_2 \ @ \ f_1 \\
\text{Im}\left(Y_{in3e}\right) &= -j\left(B_{in1e} + B_{in2e}\right) = j\left(1/Z_{e2}\right)tan\left(r\theta_2\right) @ \ f_2
\end{aligned}\right\}
\tag{8}
$$

This expression can be simplified to determine the values of Ze2 and θ2 for dual-band operations.

$$
\theta_2 = \frac{(n + 1)}{(r + 1)}\pi
\tag{9}
$$

$$
Z_{e2} = tan\theta_2 / \left(B_{in1e} + B_{in2e}\right)
\tag{10}
$$

B. Odd Mode Analysis

The odd-mode equivalent circuit of the WPD is demonstrated in Fig. 2. The resistor across the X-axis is effectively R/2 now, and the coupled-line is reduced to a TL with effective characteristic impedance Zo2, the odd mode impedance of the coupled line. The respective input admittances are mentioned as Yin1o, Yin2o, and Yin3o. Here, Zo2 and R are the only unknown design parameters to be computed. The admittances Yin1o and Yin2o can be derived similarly as Yin1e and Yin2e in the even-mode analysis and can be written as (11) and (12) respectively, where $G_{in1o}=0$ and B_{in1o} is expressed in (13).

$$
Y_{in1o} = G_{in1o} + jB_{in1o}
\tag{11}
$$

$$
Y_{in2o} = Y_{in2e} = G_{in2e} + jB_{in2e}
\tag{12}
$$

$$
B_{in1o} = \left(\frac{\rho + 1}{Z_o}\right)\left(\frac{8\rho Z_o^2 cos^3\theta_1 / sin\theta_1 - (\rho-1)^2 Z_o^2 sin^2\theta_1}{(\rho-1)^4 Z_o^2 sin^2\theta_1 - 8\rho(\rho-1)^2 Z_o^2 cos^2\theta_1 + 16\rho^2 Z_o^2 cos^4\theta_1 / sin^2\theta_1}\right)
\tag{13}
$$
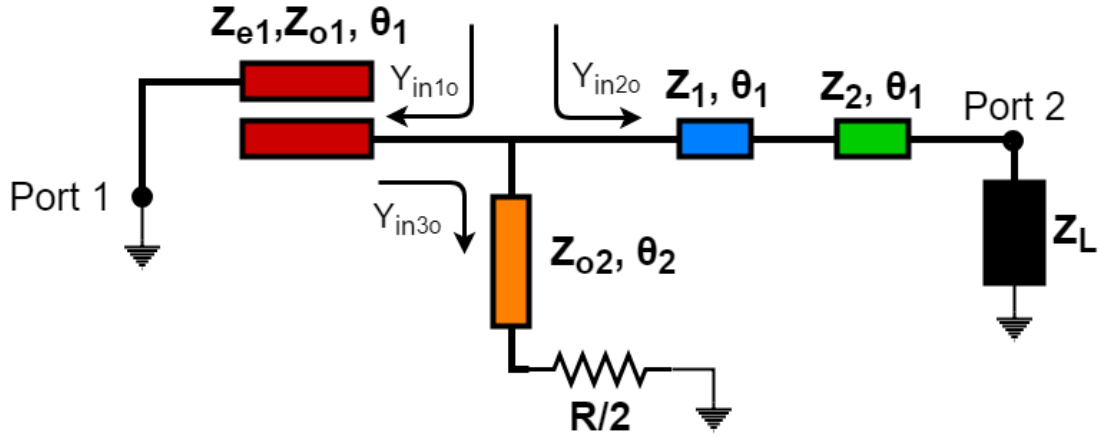
Figure 3.3: Odd-mode equivalent circuit

Now the effective admittance due to the combination of Yin1o and Yin2o, should be matched with the effective admittance offered by Yin3o, which can be expressed as (14).

$$Y_{in3o} = G_{in3o} + jB_{in3o} \tag{14}$$

$$G_{in3o} = \frac{(R/2)\left(1 + tan^2\theta_2\right)}{\left(R^2/4\right) + Z_{o2}^2 tan^2\theta_2} \tag{15}$$

$$B_{in3o} = \frac{\left(\left(R^2/4\right) - Z_{o2}^2\right)tan\theta_2}{\left(R^2/4\right) + Z_{o2}^2 tan^2\theta_2} \tag{16}$$

Following (17) and (18) the design parameters R and Zo2 can easily be computed.

$$G_{in3o} = G_{in1o} + G_{in2e} \tag{17}$$

$$B_{in3o} = -\left(B_{in1o} + B_{in2e}\right) \tag{18}$$

3.2 Design Procedure And Design Examples

The systematic design procedure of the proposed WPD is elaborated in this section as follows: -

1. At first the independent design parameters Z1, Z2 and ρ are chosen. The source and load impedances ZS and ZL are as per the design requirement. Also, the electrical length θ1 is calculated from (4) for the required frequency ratio.
2. The design parameter Zo1 is computed from (7).
3. Subsequently, Ze2, and θ2 are calculated from (9) and (10) respectively.
4. Finally, R and Zo2 are computed by solving (17) and (18).

To validate the proposed design and design analysis, a few design cases are provided in Table 1 with varying frequency ratio (r= f2 /f1) and impedance transformation ratio (k=ZL/ZS). The design parameters are computed following the design procedure. It is apparent in the table that the design has realizable parameters for a wide range of frequency ratio and the impedance ratio. The point of interest is the possibility of the extreme impedance ratios as the design can match the impedances as high as 500Ω (case 4) and as low as 5Ω (case 5 and case 6). This demonstrates the inherent impedance transformation capability of the design for energy harvesting and WPT applications [19].

3.3 Prototype And Measurement Results

To validate the design concept and inherent impedance transformation of the design, Case 2 from Table 1 is prototyped with input port impedance 30Ω and the output ports impedance 50Ω. The prototype, working at f1=1.8GHz and f2=3.6GHz is fabricated on RO5880 substrate with height 1.575 mm, copper cladding 35µm on both the sides and permittivity (ε_r) 2.2. The dissipation factor (tan δ) for the substrate is 0.0009. The fabricated prototype is shown in fig. 4. The effective WPD is of dimension 7.1x6.6 cm2 only which is extended with a redundant stepped impedance transformer [20] at the input port for the commercially available 50Ω connector for the measurement purpose.
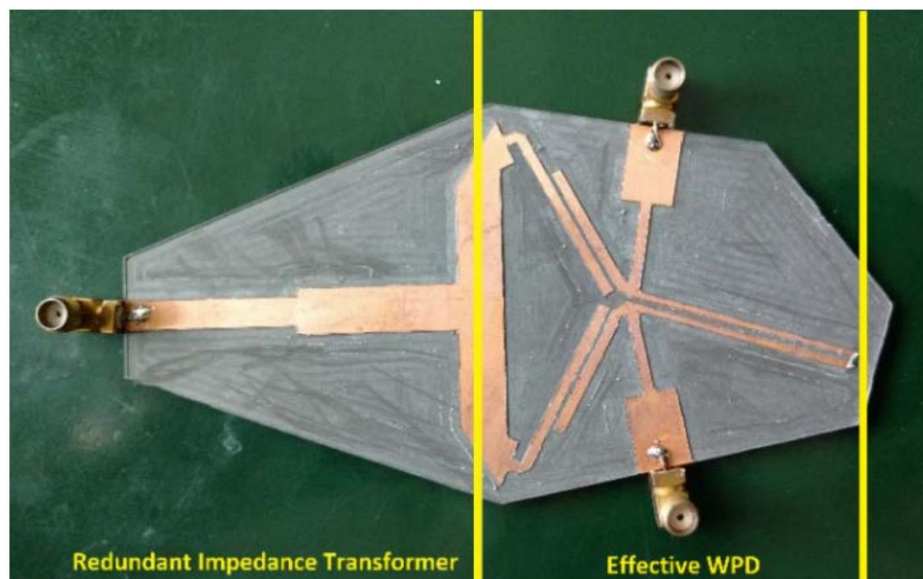

Figure 3.4: The fabricated Wilkinson Power Divider with redundant IT

The design is simulated on Keysight ADS tool and the design parameters are optimized due to TL discontinuities and the commercially available resistor, i.e. R. The measurement results in comparison with the EM simulation results are demonstrated in fig. 5. The performance metrics of the designed prototype is mentioned in Table II where the design is compared with the recently published WPDs. The matching at all three ports is approximately measured to be better than -10dB for 1.73-1.86GHz@f1 and 3.54-3.63GHz@f2. The measured isolation performance is below -10dB at almost all the frequencies. The phase difference between the two output ports and the amplitude imbalance is less than 3º and 0.5dB respectively for more than 100 MHz (1.6-2.03GHz@f1 and 2.92-3.62GHz@f2) of bandwidth. These measurement result matches very well with the EM Simulation results and hence validates the proposed design.

TABLE I
Various Design Cases For The Proposed WPD

Cases	k (=Z_L/Z_S)	r (=f_2/f_1)	Z_{e1}/Z_{o1} (Ω)	θ_1 (º)	Z_1 (Ω)	Z_2 (Ω)	Z_{e2}/Z_{o2}(Ω)	θ_2 (º)	R (Ω)
1	1 (50/50)	3	137.8/59.0	45	150	150	85.8/66.1	135	1.78k
2	1.66 (50/30)	2	87.7/57.4	60	135	35	84.7/71.0	120	3.64k
3	4 (200/50)	2	97.9/52.0	60	135	40	102.7/55.9	120	8.55k
4	50 (500/10)	2	87.6/58.3	60	100	60	108.7/100.6	120	4.04k
5	10 (50/5)	2	87.3/55.3	60	135	30	69.4/67.6	120	4.71k
6	0.1 (5/50)	2	81.6/60.2	60	90	35	114.0/57.5	120	4.79k
7	2 (100/50)	3	139.8/45.0	45	150	150	78.3/42.9	135	0.89k
8	0.5 (25/50)	3	97.2/52.2	45	150	125	73.7/63.3	135	3.02k

TABLE II
Comparison With State-Of-The-Art Techniques

Ref.	Frequency f_1/f_2 GHz	S_{11} @f_1/f_2 dB	S_{22}, S_{33} @f_1/f_2 dB	S_{23} @f_1/f_2 dB	Amplitude Imbalance @f_1/f_2 dB	Phase Diff @f_1/f_2 deg	Frequency ratio	Impedance ratio*
[4]	1.5/2.4	-28/-37	-18/-14, NA	-15/-16	<0.8	<5	1.1-2.9	1.5
[5]	0.5/3.65	-38/-16	-3.1/-3.2	-30/-25	<0.5	<5	2.44-7.31	2
[6]	1.0^	-20	-20, -20	-23	<0.5	<5	Single-band	2
[This Work]	1.8/3.6	-19/-17	-3.78/-3.71	-26/-28	<0.5	<3	1.5-3.0	>(0.1-50)
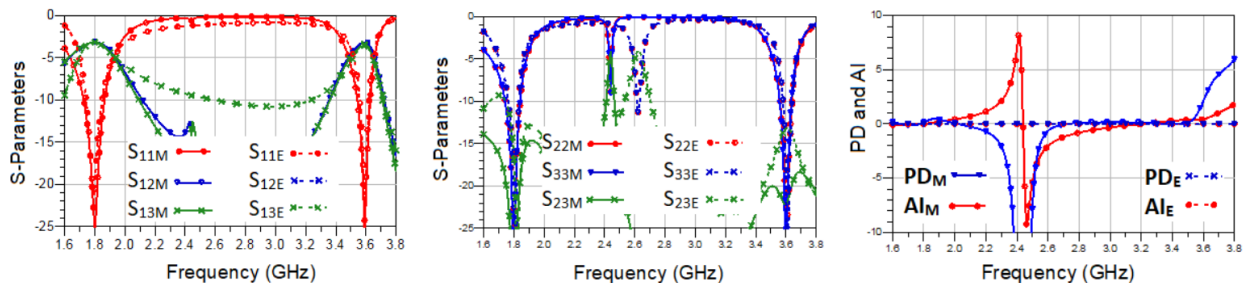
Figure 3.5: S-Parameters Simulation Results

3.4 Conclusion

In this project, a dual-band WPD with very high ITR capabilities is presented. The independent variables due to the coupled-lines and the TSTL provide the additional degree of freedom for flexible design requirements. The proposed design eventually eliminates the need of an impedance transformer at the both the input and output ports of WPD while possessing inherent impedance transformation and thus reducing the overall size of any communication system. Several design examples are provided to demonstrate the range of all the design parameters within the realizable limit for a wide range of frequency ratio and ITR. Another advantage of the design is a single lumped resistor used for isolation which is frequency independent too. The proposed WPD is compared with the recent papers and provides a wide range of ITR, i.e. very low as well as very high impedance transformation ratios.

4. High Impedance Transforming Dual-Band Balun With Isolation And Output Ports Matching

Balun finds usefulness in wide ranging applications such as antenna arrays, balanced mixers, and amplifiers [21]. The key metrics for a balun are balanced phase and magnitude at the differential outputs and the impedance matching at all the ports. The emergence of wireless communication devices has also necessitated miniaturized baluns, with good isolation between the output ports, able to provide good performance at multiple frequencies [22–25]. Furthermore, an added feature of baluns is their impedance transformation ability as this could be extremely useful in applications such as power amplifiers and rectifying antennas in energy harvesting [21, 26,27]. An added degree of flexibility can be obtained in the DGS structure in [26] whereas the additional burden on impedance transformer could be avoided in [27] with an inherent impedance transforming component in RF front end system. Another importance of high impedance transformation ratio (ITR) with the baluns can be easily identified in on-chip antennas and antenna feedings [26, 28–32].

However, the reported multi-band balun design techniques are not able to provide good impedance transformation and therefore have limited usefulness in niche and emerging energy harvesting applications. A step by step procedure is given in [28] enforcing need of fixed feedline of 50Ω impedance which can be relaxed using the proposed balun in the case of a differential feeding. The reports in [29–32] illustrate the need of an additional impedance transformer which can be avoided using the proposed DBB. There are reports on the impedance transforming baluns [33–35]; however, impedance transformations with dual-band operations are rare.

In this project, a dual-band balun (DBB) with matching at all the ports and very good isolation between the output ports is reported. A simplified analysis and design scheme augmented by the even-odd mode technique facilitates the presented concept. The capability of the presented design technique is demonstrated through a very good agreement between the EM simulated and experimental results. Furthermore, it has been shown that the proposed design can provide high ITR between the input and output port impedances, i.e., high transformation between Z_L and Z_S.

4.1 Proposed Circuit And Analysis

The architecture of the proposed DBB, in Fig. 1, is symmetric to the X-axis and consists of port 1 as input port and ports 2 and 3 as output ports. It incorporates stubs to short the two coupled line sections perpendicular to the X-axis. An isolation resistor R (Ω) is incorporated to provide the isolation between the output ports. The characteristic impedances denoted by Z and the electrical lengths denoted by θ of all the transmission lines (TL) are in Ohms (Ω) and degrees (◦), respectively. Apparently, even-odd mode analysis can be carried out to simplify the design process. Here, the even mode (e) and odd-mode (o) parameters must satisfy conditions in Eq. (1) for a balun architecture to ensure matching at all the ports, balanced outputs, and good isolation between output ports.

$$S_{21e} = 0; \quad S_{22e} = 0; \quad S_{11o} = 1/3 \tag{1}$$
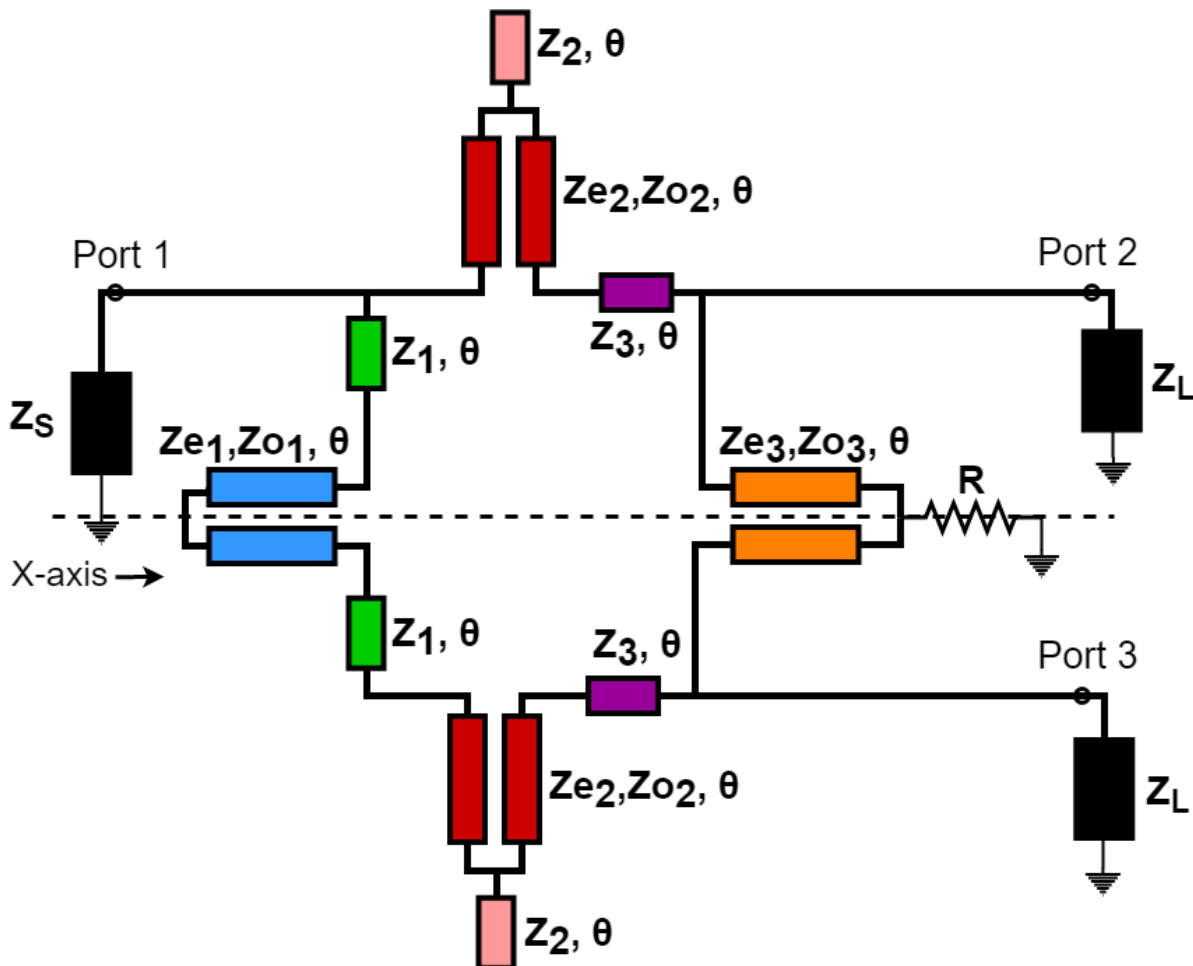
Figure 4.1: The proposed dual-band balun architecture.

4.2 Design Analysis And Procedure

All the TL are considered ideal in the analysis stage. In the even mode circuit, Fig. 2, no signal flows in from port 1, and this is ensured by achieving ZINe = 0. For this, the node M should be short circuited, and this results in Eq. (2). Here, Z1 is an independent variable and should be chosen in the range of [20–150 Ω] so that all the design parameters are realizable. Here, the electrical length follows θ = π/1 + r and r being the desired frequency ratio.

$$Z_{e1} = Z_1 \tan^2 \theta \tag{2}$$
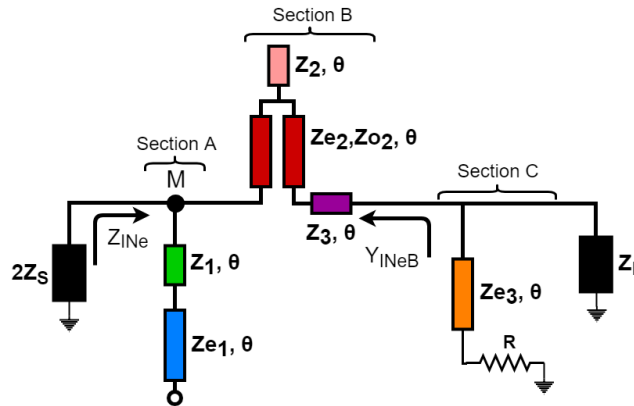
Figure 4.2: Even mode equivalent circuit.

In the odd mode circuit, Fig. 2, the term YINoB is of the form RBo ± jXBo. It is the combined admittance of ZS, Section A, and Section B looking towards Section B. It is matched by an L type impedance transformer, the Section C having Ze2, Zo2, Z2 as independent variables, which is considered good for high ITR [16]. Subsequently, the dependent parameters are computed from Eqs. (3) and (4).
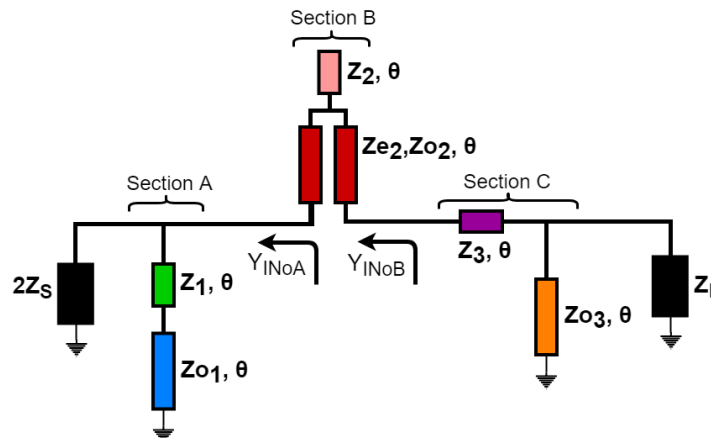
Figure 4.3: Odd mode equivalent circuit.

$$Z_3 = \frac{-1 \pm \sqrt{1 - \left(R_{Bo}^2 + X_{Bo}^2 - Z_o R_{Bo} - Z_o R_{Bo} \tan^2\theta \right)}}{\tan\theta} \tag{3}$$

$$Z_{o3} = \frac{Z_3^3 \tan^2\theta + 2Z_3^2 \tan\theta + Z_3 R_{Bo}^2 + Z_3 X_{Bo}^2}{Z_3 X_{Bo} \left(\tan^2\theta - 1 \right) \tan\theta + \left(R_{Bo}^2 + X_{Bo}^2 - Z_3^2 \right) \tan^2\theta} \tag{4}$$

Furthermore, for the matching at the output ports and for isolation between the output ports, the sufficient condition in even mode is S22e = 0. Here, node M is shorted, and hence the input impedance Y_{INeB}, in the form $0 \pm jX_{Be}$, in parallel with the section C can be matched using the calculated values of Ze3 and R as outlined in Eqs. (5) and (6).

$$Z_{e3}^2 \left(2Z_L^2 R + 2X_{Be}^2 R \mp Z_L X_{Be}^2 \right) + Z_{e3} \left(2Z_L^2 R + 2RX_{Be}^2 \mp \frac{4R^2 Z_L X_{Be}}{Z_{e3}} \right) \tan^2\theta = 0 \tag{5}$$

$$Z_{e3}^2 \left(Z_L^2 X_{Be} - Z_L^2 \tan\theta - X_{Be}^2 \tan\theta \right) + 4R^2 \tan\theta \left(Z_L^2 X_{Be} \tan\theta - Z_L^2 - X_{Be}^2 \right) = 0 \tag{6}$$

4.3 Fabrication And Measurement

A prototype working at 1/2 GHz is designed on Rogers RO5880 to validate the presented concept. The source (load) impedance is taken as 50 Ω so that they gel with the impedances of the SMA connectors and to discard the need of additional impedance transformer. The design equations are used to determine the design parameters as (units: Ω) Z1 = 30, Ze1 = 90, Zo1 = 62.1, Z2 = 118.7, Ze2 = 58.4, Zo2 = 41.3, Z3 = 74.5, Ze3 = 57.5, Zo3 = 52.9, and R = 55.4. Electrical lengths of all the TL are chosen as 60∘ for the dual-band operation. The EM simulations are carried out in CAD tool, and the design parameters are optimized for the TL discontinuities and substrate losses. The prototype with the optimized parameters is shown in Fig. 3 with dimensions as (units: mil) W1 = 185, L1 = 1227.4, W2 = 45, L2 = 1276.7, W3 = 190, S3 = 40, L3 = 1076.7, W4 = 91.7, L4 = 739.8, W5 = 350, L5 = 960.1, W6 = 95, L6 = 861.2, S6 = 30, W7 = 140, S7 = 185, L7 = 992.1, W8 = 185, L8 = 1208.1, and R = 56.2Ω.

The EM simulation results and measurement results are shown in Fig. 4. The EM results confirm equal power distribution and matching at all the ports along with good isolation for a broad range of frequencies at both the chosen bands. The measured responses for the amplitude (phase) imbalance are 0.1 dB (0.8∘) at 1.0 GHz and 0.0 dB (−3.6∘) at 2.0 GHz, and the matching responses S11, S22, and S33 are −23.4 dB (−18.9

dB), −44 dB (−30.6 dB), −27.8 dB (−22.2 dB), respectively at 1.0 GHz (2.0 GHz). The insertion losses S21 and S31 are better than −3.4 dB (−4.5 dB) at the operating frequency of 1.0 GHz (2.0 GHz).

(a)   (b)
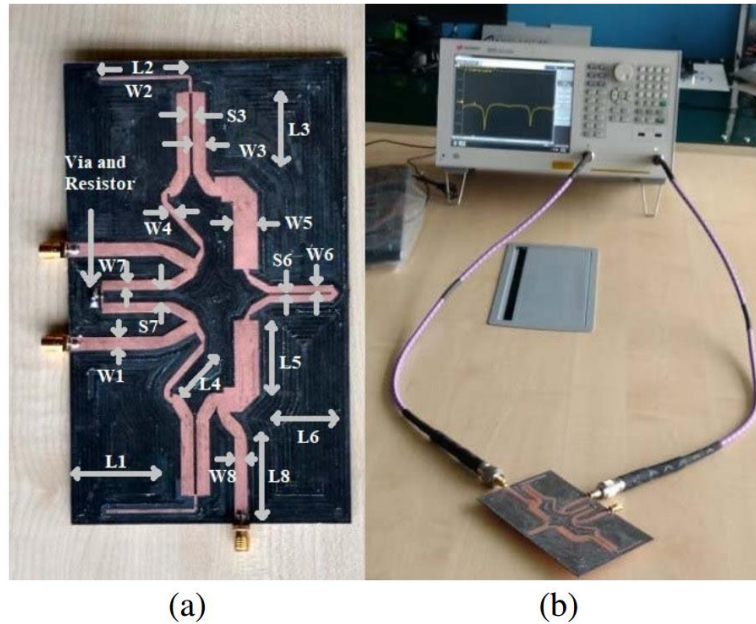
Figure 4.4: The fabricated prototype (a) and measurement setup (b).

(a)   (b)
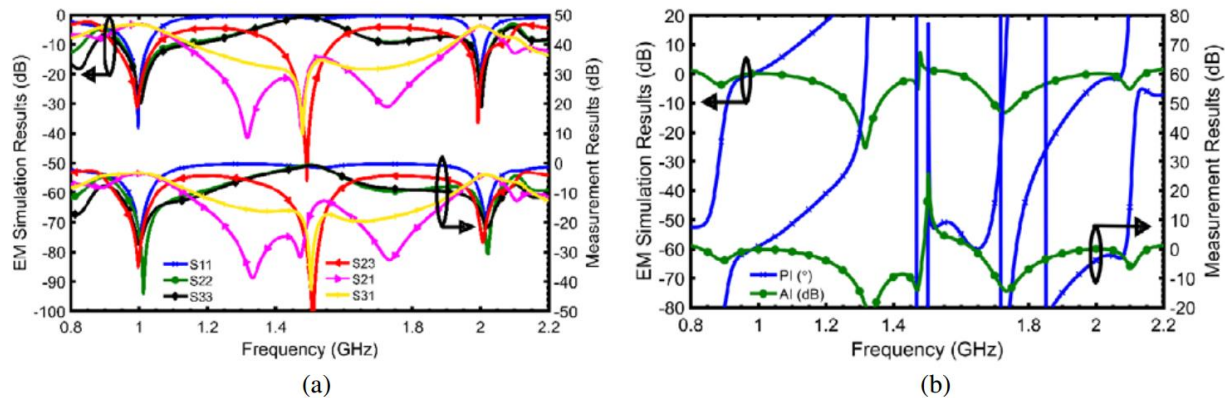
Figure 4.5: S-parameters (a), Amplitude Imbalance (AI) and Phase Imbalance (PI) (b) results of the fabricated prototype

Extremely good isolation of −35.1 dB (−26.8 dB) at 1.0 GHz (2.0 GHz) is also achieved in the proposed DBB. Moreover, the 10dB bandwidth for S11 (S22, S33 and S23) at 1 GHz is 0.969-1.034 GHz (0.95– 1.17 GHz, 0.94 – 1.20 GHz, and 0.927-1.06 GHz) and at 2GHz is 1.99-2.04 GHz (1.97-2.06 GHz, 1.94– 2.08 GHz, and 1.96-2.06 GHz). The amplitude (phase) imbalance of 1 dB (5◦) is also achieved for a BW of 0.95-1.1 GHz (0.929-1.06 GHz) at 1 GHz and of 1.92-2.06 (1.98-2.10 GHz) at 2GHz. These results

apparently match very well with the simulation results and thereby validate the design concept.

4.4 Application For Impedance Transformation

An added feature of the proposed DBB is its potential to operate at wide range of distinct load and source impedances. For example, the design parameters (units: Ω) of the DBB for two design cases of maximum achievable ITR of 0.4 and 4.0 are given in Table 1. Electrical lengths of the TL are again 60◦ for its dual-band operation at 1/2 GHz.

TABLE III

Design Parameters For Two Cases Of Very High ITR

ITR (ZL/ZS) = 20/50				ITR (ZL/ZS) = 200/50			
Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
Z1	40	Z2	105	Z1	29.1	Z2	149.8
Ze1	120	Z3	35.7	Ze1	87.3	Z3	89
Zo1	87.6	Ze3	22.2	Zo1	79	Ze3	117
Ze2	75.2	Zo3	20.2	Ze2	47.5	Zo3	112
Zo2	57.6	R	14.5	Zo2	29	R	377.7
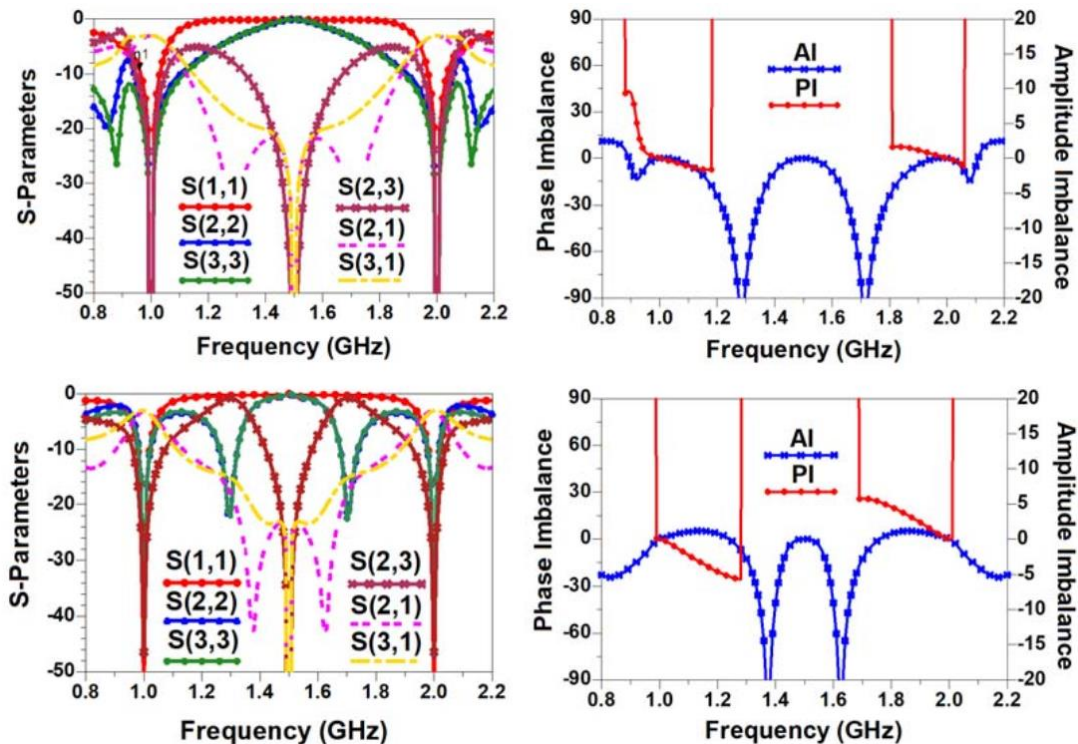
Figure 4.6: Simulation results of the design for ITR as 0.4:1 (top two) and ITR as 4.0:1 (bottom two).

The simulation results, in Fig. 5, for these cases also demonstrate the effectiveness of the proposed technique. The two figures on the top demonstrate the performance of the balun for ITR 0.4. One figure, on the left, demonstrates the return loss at all the three ports, i.e., S11, S22, and S33, isolation between the two output ports, i.e., S23, and the insertion losses at the two output ports, i.e., S21, and S31. Another figure, on the right, demonstrates the amplitude difference between the two output ports, i.e., amplitude imbalance (AI) and the deviation in the phase from the required phase difference of 180◦ between the two output ports, i.e., phase imbalance (PI). Similarly, the bottom two figures of Fig. 5 demonstrate all the performance parameters for ITR 4.0. These results therefore confirm the capability of the design to provide inherent impedance transformation integrated with the operation of a balun for a wide range of impedance transformation ratios. However, the design follows a trade-off between the bandwidth and the impedance transformation ratio [37].

4.5 Conclusion

An interesting DBB architecture capable of enhancing all the figures of merit has been proposed. One of the key features of the proposed DBB is its potential to operate at wide range of distinct load and source impedances. It has been shown that the ITR from 0.4 to 4.0 are achievable using the proposed design. A direct application of the proposed DBB is the RF energy harvesting system and on-chip antennas where wide range of ITR could be extremely beneficial.

5. Utilization Of Stepped Impedance Transformer In High Frequency Power Divider For Real/Complex Port Terminations

A Power Divider (PD) is a key passive component in any RF/Microwave system and is used for distribution/combination of the power to/from multiple ports. For example, applications of a PD can be found in push-pull amplifiers, mixers, phase arrays, antennas transceiver systems, etc. Some of these may need to have these PDs terminated at distinct real and/or frequency dependent complex impedances. This helps in the reduction of the size of the overall system as it discards the need of additional impedance transformer as depicted in Fig. 1.
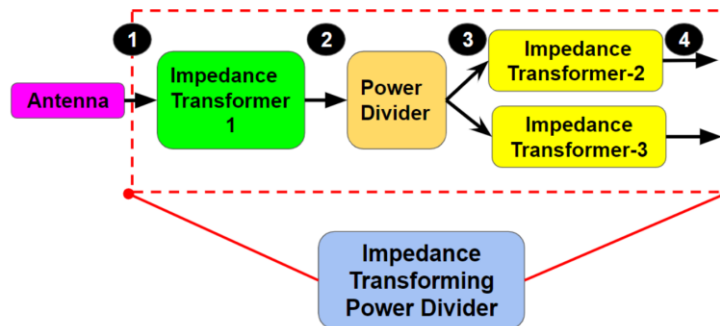
Figure 5.1: Example of a block diagram of a telecommunication system.

For example, the impedance requirement at labels 1 and 4 is generally any arbitrary real/complex value which can be matched directly with a impedance transforming PD (shown outside dotted red box) instead of using three respective impedance transformers (I.T.s) at labels 2 and 3. There have been numerous reports of Power Divider (PD) schemes to cater to various features and functionalities. For example, the wideband operation of a PD is discussed in [38], [39], and the impedance transforming features of a PD can be found in [40], [41], [42]. However, most of these reports address real-real impedance transformation at the ports, whereas there are situations requiring real-complex impedance transformation at the ports of PDs [43], [44], [45]. Although some recent reports have started looking into this aspect [44], [45], but still there is a clear need to investigate this issue further to fulfil the needs of existing communication infrastructure to support the ever-advancing communication standards. Therefore, this project revisits the generic scenario of impedance environment, real or complex, and proposes design of a 3-port high frequency equal-power PD with equal output-port terminations. The key interesting

feature of the proposed PD is its ability to inherently provide complex impedance transformations for a wide range of real and/or complex port terminations. A thorough analysis is augmented with analytical formulations that aid in deducing the design parameters of the proposed PD. Subsequently, a number of design examples are included to support the presented theory and the design methodology. Finally, a prototype is developed on RO5880 (Γ_r = 2.2, copper thickness = 35μm) to validate the proposed PD architecture and the design concept. The succeeding sections include theoretical postulations and analysis, design procedure, prototype development, measurement results, and conclusion.

5.1 Proposed Architecture

The architecture of the proposed PD, shown in Fig. 2, comprises of a coupled line with an isolation resistor, R, as the core of the power divider. The respective odd- and even-mode impedances and the electrical length of the coupled-line are Z_{o3}, Z_{e3}, and θ_1. The core of the PD then consists of two-section stepped transmission lines (TSTL), marked by respective Z and θ, at all the three ports. To maintain symmetry, the TSTLs at ports 2 and 3 have similar electrical properties. This enables a simplified even-odd mode analysis of the proposed PD structure. During the analysis it will be shown that the input (port 1) and output (ports 2 and 3) impedances could be distinct over a wide range of complex and real values.
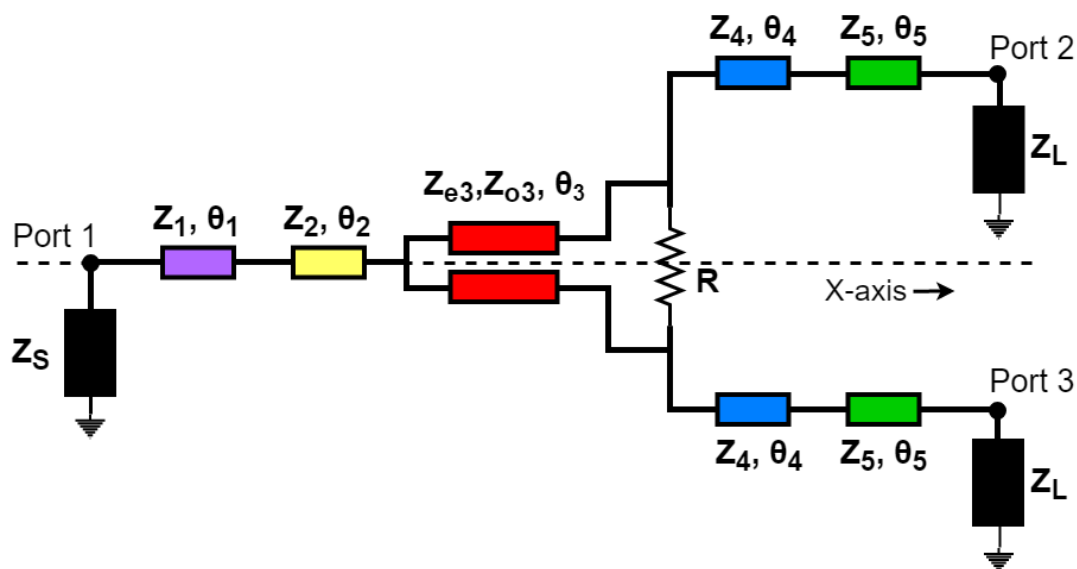

Figure 5.2: Proposed power divider with a coupled-line. input port: port 1, output ports: port 2 and port 3.

A. Odd Mode Analysis

The odd-mode equivalent of the proposed PD is obtained by shorting the symmetric axis and is shown in Fig. 3. Apparently, it is a parallel combination of odd-mode characteristic impedance Zo3, R=2, and TSTL characteristic impedances Z4 and Z5. Now, it can be seen in Fig. 3 that Y_{oa}, expressed in (1), is the admittance generated by the parallel combination of Zo3 and (R=2). The role of TSTL is to provide a match between Y_{oa} and the real or complex port admittance (Y_L = 1=ZL = G_L +jB_L) for the maximum power transfer It is imperative to note that Y_L = G_L for a real port impedance.

$$Y_{oa} = \frac{2}{R} + \frac{-j}{Z_{o3} \tan \theta_3} = G_{oa} + jB_{oa} \tag{1}$$
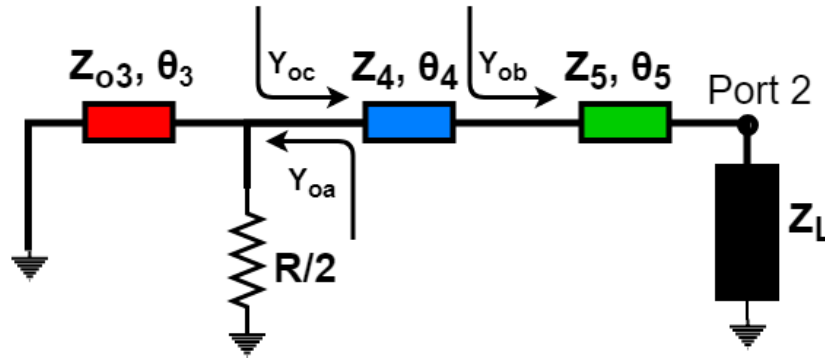
Figure 5.3: Odd-mode equivalent circuit of the proposed power divider.

The intermediate admittance, Yob, and the admittance, Y_{oc}), are expressed in (2) and (3). Subsequently, the real and imaginary parts of Y_{oc} in terms of Y4 and Y5 are given in (4) and (5). Here, α = tanθ4 and β = tanθ5. Finally, expressions (6) and (7) need to be satisfied for the impedance matching between Y_{oc} and Yoa. During this analysis, it is assumed that parameters of the core, i.e., Zo3 and R, are known and it will be shown in the design section that the proposed technique exhibits four independent design variables, including θ4 and θ5, for realizable impedances using a micro-strip line.

$$Y_{ob} = Y_5 \left(\frac{Y_L + jY_5 \tan \theta_5}{Y_5 + jY_L \tan \theta_5} \right) \tag{2}$$

$$Y_{oc} = Y_4 \left(\frac{Y_{ob} + jY_4 \tan \theta_4}{Y_4 + jY_{ob} \tan \theta_4} \right) = G_{oc} + jB_{oc} \tag{3}$$

$$G_{oc} = \left(\frac{Y_4^2 Y_5 Y_L \left[1 + \alpha^2 + \beta^2 + \alpha^2 \beta^2 \right]}{\left(Y_4 Y_5 - Y_5 \alpha\beta \right)^2 + \left(Y_4 Y_L \beta + Y_L \alpha \right)^2} \right) \tag{4}$$

$$B_{oc} = Y_4 \left(\frac{\alpha\beta \left(Y_4^2 Y_L^2 \beta - Y_5^2 \beta - Y_4 Y_5^2 \alpha + Y_4 Y_L^2 \alpha \right)}{\left(Y_4 Y_5 - Y_5 \alpha\beta \right)^2 + \left(Y_4 Y_L \beta + Y_L \alpha \right)^2} \right) + Y_4 \left(\frac{Y_4 \left(Y_5^2 \beta + Y_4 Y_5^2 \alpha - Y_L^2 \beta \right) - Y_L^2 \alpha}{\left(Y_4 Y_5 - Y_5 \alpha\beta \right)^2 + \left(Y_4 Y_L \beta + Y_L \alpha \right)^2} \right) \tag{5}$$

$$G_{oc} = G_{oa} \tag{6}$$

$$B_{oc} = -B_{oa} \tag{7}$$

B. Even Mode Analysis

Fig. 4 shows the even-mode equivalent of the proposed PD and it is obtained by opening the junctions at the symmetric axis. It is a very simple series configurations of five characteristics impedances of Z1, Z2, Ze3, Z4, and Z5 between the input and output ports. Here, the admittance Yea is a known quantity as the design parameters Z4 and Z5 are already computed from the odd-mode analysis and Ze3 is one of the independent variables. Here, the role of TSTL, with characteristics impedances 2Z1 and 2Z2, is to create matching environment between Yea and the equivalent even-mode input admittance, i.e. 1=2ZS. The unknown design parameters Z1 and Z2 although have similar forms to expressions (4) and (5) but require appropriate customization.
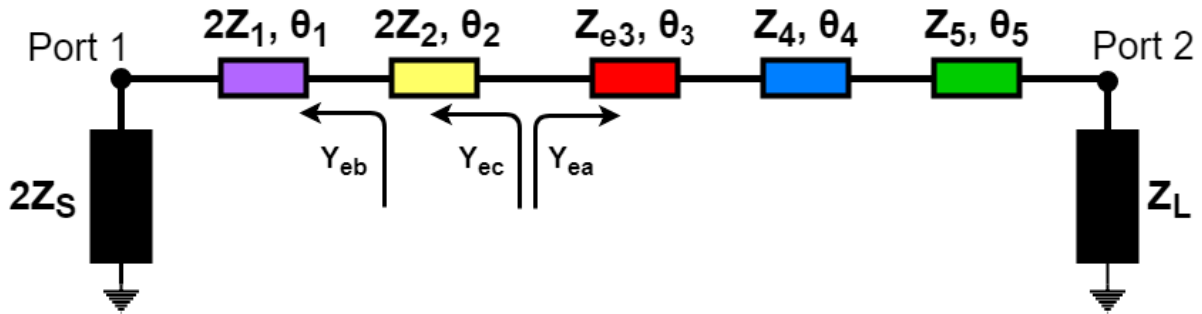

Figure 5.4: Even-mode equivalent circuit of the proposed power divider.

5.2 Design Procedure And Case Study

The design procedure for the proposed high frequency power divider can be summarized as: -

1. Choose appropriate independent design parameters Ze3, Zo3, θ3, and R. Then calculate Yoa using (1).

2. Compute parameters Z4 and Z5 by solving (6) and (7) by choosing a suitable value of θ4 and θ5 so that these are within the realizable limits of a micro-strip transmission line i.e. [20-140] Ω.

3. Follow above steps to compute Z1 and Z2.

Presence of several independent variables make the design very flexible for wide range of port impedances. However, in case the computed design variables are not within the realizable limits, the independent variables opted in step 1 can be altered and the process repeated. The next sub-sections provide a number of design examples to verify the design procedure and the capability of the proposed PD possessing port impedances which are distinct real and complex as well as far apart.

A. Real to Real Impedance Transformation

Most of the reported designs in RF/Microwave components entail port terminations of 50Ω as the available commercial ports and test instruments mostly cater to 50Ω environment. However, it is often beneficial to terminate impedances to arbitrary values in a communication system to discard the need of additional impedance transformers. Therefore, a design case with very high impedance transformation of ZL=ZS = 0:2, i.e. input port impedance 50Ω and output ports impedance 10Ω, is analysed to demonstrate the working of the proposed PD. As per the stated design procedure, the design parameters are chosen as Ze3= 55Ω, Zo3= 35Ω, θ3= 60Ω, and R=600Ω. The term Yoa can be calculated easily from (1). Further, for a known real port impedance Yoc, (3) can only be expressed in terms of Z4 and Z5. Here, the electrical lengths are chosen as θ4=35◦ and θ5=75◦. Now, simply following (6) and (7) will result in Z4=31.4Ω and Z5=63.3Ω. Similarly, the values of Z1=71.8Ω and Z2=15.5Ω is calculated for chosen values of θ1=70◦ and θ2=70◦. All of these design parameters are tabulated as case 1 in Table 1.

B. Real to complex Impedance Transformation

Since the peripheral devices often possess complex impedances at ports, this scenario is very pertinent. This saves the additional need of an impedance transformer at the ports. To demonstrate the flexibility of the design, the port terminations are chosen as a high complex value of 155:9 − j27:0 Ω in case 2 and as a very low complex value of 5+ j10Ω in case 3 mentioned in Table 1. To reiterate, both the output ports have the same impedances, but the input port termination is kept 50 Ω for the real to complex impedance transformation. The design parameters are then calculated for both the cases as per the design procedure.

C. Complex to complex Impedance Transformation

An example of widely separated complex port terminations is considered where both the input as well as output ports are complex. The output port impedance is 100 + j200Ω and the input port impedance is 40+j10Ω. The design case along with the design parameters is tabulated as case 4 in table 1. All of the above design examples from case 1 to 4 are chosen with variety of low and high as well as real and complex terminations to claim the high flexibility of the proposed architecture.

The working of these design examples is also verified with the ideal simulation results shown in Fig. 5. These simulations provide very good clarity about the all port matching, in-phase and equal power division, and excellent isolation between the output ports. It, therefore, provides a very good demonstration of the operation of the proposed design for wide ranges of the port impedances at different real/complex impedances.

TABLE IV
Design Cases of the Proposed High Frequency Power Divider

Case	ZS (Ω)	ZL (Ω)	Design Parameters											
			Z1 (Ω)	Z2 (Ω)	Zo3 (Ω)	Ze3 (Ω)	Z4 (Ω)	Z5 (Ω)	Θ1 (°)	Θ2 (°)	Θ3 (°)	Θ4 (°)	Θ5 (°)	R (Ohm)
1	50	10	71.81	15.51	35	55	31.40	63.33	70	70	60	35	75	600
2	50	155.9-j27	67.67	30.7	38	50	58.04	74.25	45	60	60	65	15	50
3	50	5+j10	62.15	16.81	40	65	34.11	33.85	40	65	60	30	70	400
4	40+j10	100+j200	109.8	18.44	40	55	41.19	68.71	60	25	60	55	65	10

TABLE V
Comparison with Recently Published Impedance Transforming Power Dividers

Ref	Venue	Operating Frequency (GHz)	FBW (%)	Impedance Transformation	Input Return Loss (dB)	Isolation (dB)	No of TL	Isolation Element	Size ($\lambda 2\ g$)
[3]	EuMC 2015	2.6	18.4	Real	-16.4	-11.4	4	R	0.07
[4]	MTT 2018	2	37	Real	-37.84	-41	10	2R	0.78
[5]	EL2017	2.6	4.6	Real	-20	39.2	4	R	0.05
[7]	Access 2017	2	36	Real and Complex	-30	-17	4	R	0.35
[8]	TMTT2018	2	27	Complex	-20	-20	7	R & 2 T.L.	0.115
This Work		5.8	14.5	Real and Complex	-25	-23	7	R	0.25
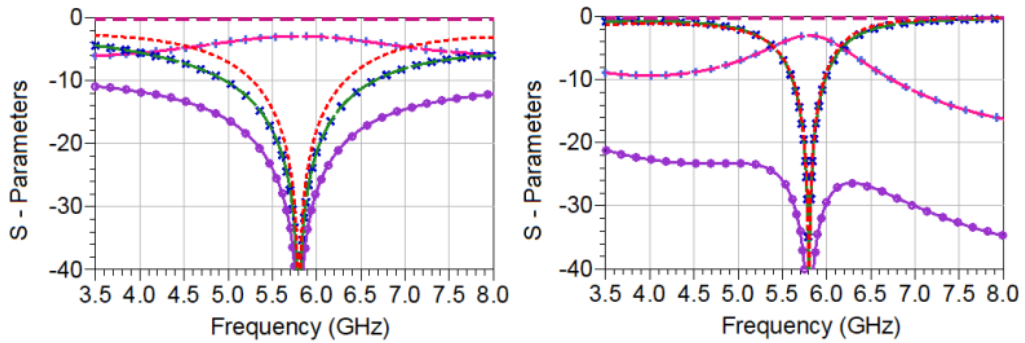
(a) case 1 (left) and case 2 (right)
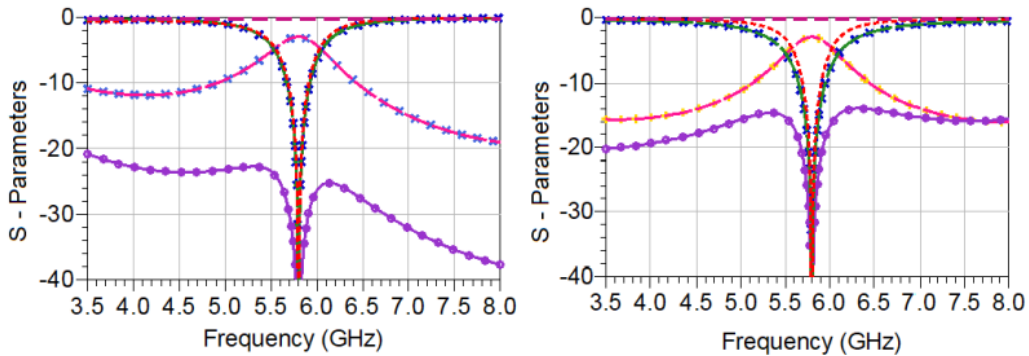
(b) case 3 (left) and case 4 (right)

Figure 5.5: EM Simulation vs Measurement Results: (a) S11, S12, S13, and Phase difference (P.D.) between the two output ports; (b) S23, S22, and S33

5.3 Measurement Results

To validate the working of the high frequency PD, Case 2 from table 1 is prototyped on RO5880 with substrate thickness of 1.575mm, permittivity of 2.2. The loss tangent

of the substrate is 0.0009 and the copper cladding on the PCB board is of 35µm on both the sides of the substrate. The prototype along with its dimension is shown in 6. It should be noted that appropriate optimizations in ADS is required to account for the substrate losses and shaping at the coupled-line junction.
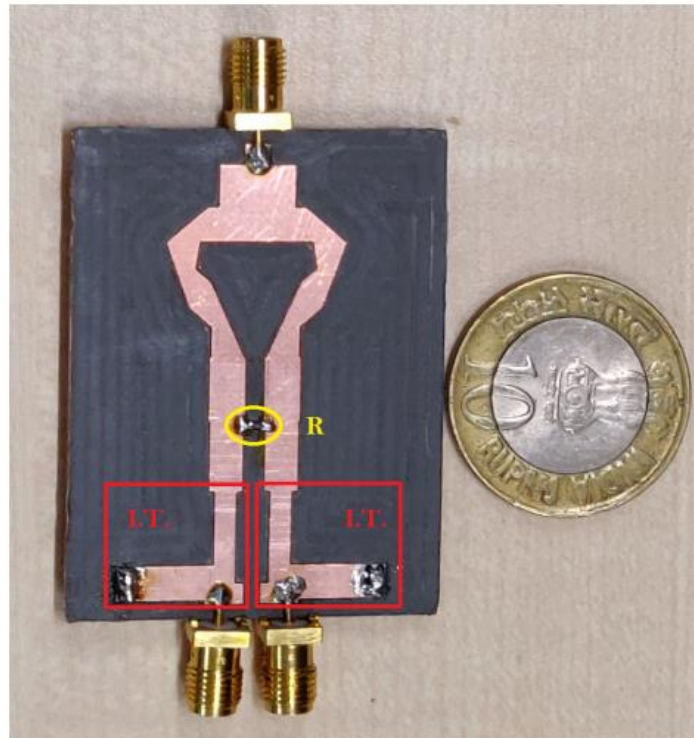
Figure 5.5: Fabricated prototype of the proposed power divider (Size excluding I.T.: 33mmx20mm). I.T.: Impedance Transformer, R: Isolation Resistor

The measured results (M) and EM simulation results (E) are plotted in Fig. 7. It is apparent from Fig. 7a that the input return loss of over -25dB is achieved for the fabricated prototype at the design frequencies of 5.8 GHz. The fabricated prototype has a wide 10dB bandwidth of more than 800MHz. The equal power division is also achieved for the whole measurement band. The measured (EM simulated) insertion loss at port 2 and port 3 of the fabricated prototype is (3.7dB) at the design frequency and the equal power division is ensured by a maximum amplitude difference between the output ports 2 and 3 of 0.1dB for the whole bandwidth from 5.41GHz to 6.3GHz.
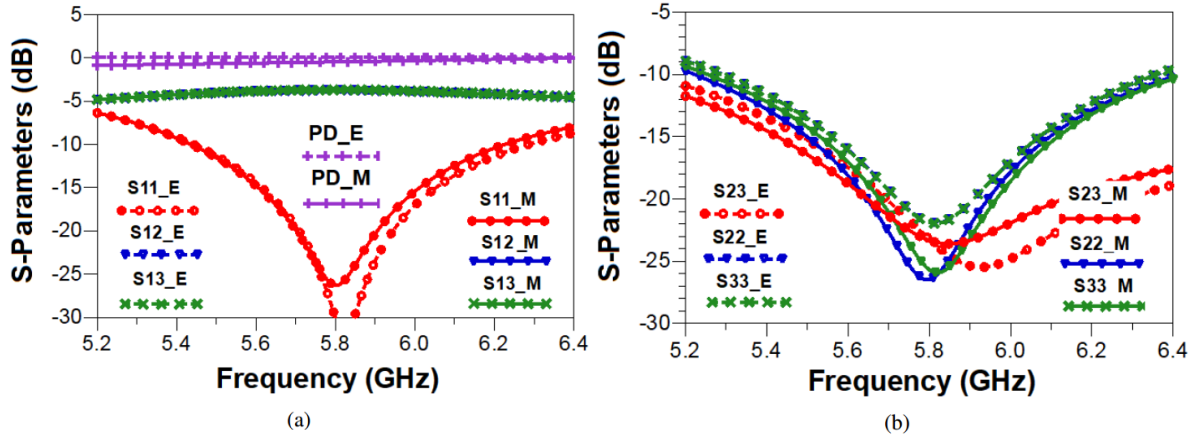
Figure 5.6: EM Simulation vs Measurement Results: (a) S11, S12, S13, and Phase difference (P.D.) between the two output ports; (b) S23, S22, and S33

It is apparent from Fig. 7b that this prototype also exhibits a very good isolation performance. The measured isolation between the output ports, S23, is better than -23dB at the design frequency. The results of the measured prototype are also compared favourably with the state-of-the-art [40], [41], [42], [44], [45] as can be seen in Table 2.

5.4 Conclusion

This paper presents a high frequency equal PD, built around a coupled-line core, with real/complex port terminations. A number of design examples with widely separated port terminations demonstrate its ability to provide excellent performance in varied impedance environments. A prototype fabricated to validate the working of the PD at the frequency of 5.8GHz with equal and complex output port impedances provides performance that matches well with the EM simulated performance and thus validates the presented theory and design technique.

6. Summary And Conclusion

Due to the rapid developments in multi-frequency/multi-standard wireless communication systems during the last decade, the design of RF front-ends has become a very challenging affair while designing wideband components, especially those requiring adequate operation over multi-octave bandwidth has always been considered difficult. However, the alternative architecture employing multi-frequency components is also by no means an easier task. Whether wideband or multi-frequency; most of RF front-end components employ impedance matching networks as a key component, and therefore their analysis and design are of the paramount importance. To that end, the most important contribution of this thesis work has been using of coupled lines and two-section transmission lines for the design of high impedance transforming dual-band Wilkinson power divider. The advantage of this technique lies in providing inherent impedance transformation with very high impedance transformation ratio from many of those reported in the literature. A very troublesome scenario in dual- frequency impedance matching network is the limited load of range that could be matched to a real source impedance. Since, a circuit designer has no control over the input/output impedances of a transistor or other active device at given set of frequencies, the existing dual-frequency matching networks may not yield a physically realizable design. If any of the constituting line impedance is beyond a specific range, there is no other way except to change the matching network topology or to use multiple stages of matching networks. Coupled lines are very important for matching network design as they facilitate miniaturization. Therefore, future was devoted to novel dual-frequency matching networks employing parallel coupled lines. Due to the high potential of this work, here are other works done using same technique in those design such as implementing high impedance transforming dual-band balun with isolation and output ports matching.

The major focus of this work has been into mitigate the issue of limited frequency and transformation ratios of dual-frequency networks by advanced network topologies. In addition, this work can be explored further for the tri-frequency impedance matching network which puts forward a scheme to establish matching at three arbitrary frequencies concurrently. The same technique could be extended to multi-frequency scenarios.

List Of Publications

1. V. V. Singh, R. Gupta, and M. Hashmi, "A Power Divider Utilizing Stepped Impedance Transformers for Real/Complex Port Terminations," 2019 IEEE Asia-Pacific Microwave Conference (APMC), Singapore, Singapore, 2019, pp. 312-314.

2. V. V. Singh, R. Gupta, and M. S. Hashmi, "High Impedance Transforming Dual-Band Wilkinson Power Divider," 2018 IEEE MTT-S International Microwave and RF Conference (IMaRC), Kolkata, India, 2018, pp. 1-4.

3. Vikas Vikram Singh, Rahul Gupta, M. H. Maktoomi and M.S. Hashmi, "High Impedance Transforming Dual-Band Balun with Isolation and Output Ports Matching", Progress In Electromagnetics Research Letters, Vol. 81, 121–126, 2019

References

[1]. W. H. Hayt, J. E. kemmerly, and S. M. Durbin, Engineering Circuit Analysis, 6th ed., New Delhi: TMH, 2003.

[2]. D. M. Pozar, Microwave Engineering, 3rd ed., New Delhi: J. Wiley & Sons, 2010.

[3]. G. Gonzalez, Microwave Transistor Amplifiers: Analysis and Design. 2nd ed., Englewood Cliffs, NJ: Prentice Hall, 1996, chap. 2 and 3, pp. 92–175.

[4]. Y. Wu, L. Jiao and Y. Liu, "Comments on "novel dual-band matching network for effective design of concurrent dual-band power amplifiers"," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 9, pp. 2361–2361, Aug. 2015.

[5]. K. Rawat and F.M. Ghannouchi, "Dual-band matching technique based on dual-characteristic impedance transformers for dual-band power amplifiers design," IET Microwaves, Antennas & Propagation, vol.5, no.14, pp.1720–1729, Nov. 2011.

[6]. O. Manoochehri, A. Asoodeh, and K. Forooraghi, "Pi -model dual-band impedance transformer for unequal complex impedance loads," IEEE Microw. Wireless Compon. Lett., vol.25, no.4, pp.238–240, Apr. 2015.

[7]. L. Wu, Z. Sun, H. Yilmaz, and M. Berroth, "A dual-frequency Wilkinson power divider," IEEE Trans. Microw. Theory Tech., vol.54, no.1, pp.278-284, Jan. 2006.

[8]. R. P. Gordon, "A directional coupler with very flat coupling," IEEE Trans. Microw. Theory Tech., vol.26, no.2, pp.70-74, Feb. 1978.

[9]. I. Ohta and T. Kawai, "Design of quadrature hybrids and directional couplers based on the equivalent admittance approach," IEICE transaction, vol.E88-C, no.1, 2005.

[10]. M. Pinuela, P. D. Mitcheson, and S. Lucyszyn, "Ambient RF energy harvesting in urban and semi-urban environments," IEEE Trans. Microw. Theory Tech.,, vol.61, no.7, pp.2715-2726, Jul. 2013.

[11]. M. Pinuela, P. D. Mitcheson, and S. Lucyszyn, "Ambient RF energy harvesting in urban and semi-urban environments," IEEE Trans. Microw. Theory Tech.,, vol.61, no.7, pp.2715-2726, Jul. 2013.

[12]. Z. Liu, Z. Zhong, and Y.-X. Guo, "Enhanced dual-band ambient RF energy harvesting with ultra-wide power range," IEEE Microw. Wireless Compon. Lett., vol. 25, no. 9, pp. 630–632, Sept. 2015.

[13]. K. Niotaki, A. Georgiadis, A. Collado, and J. S. Vardakas, "Dual-band resistance compression networks for improved rectifier performance," IEEE Trans. Microw. Theory Tech., vol. 62, no. 12, pp. 3512–3521, Nov. 2015.

[14]. N. Shariati, W. S. T. Rowe, J. R. Scott, and K. Ghorbani, "Multi-service highly sensitive rectifier for enhanced RF energy scavenging," Nature Sci. Rep., vol. 5, p. 9655, 2015.

[15]. H. R. Ahn and I. Wolff, "General design equations, small-sized impedance transformers, and their application to small-sized three-port 3-dB power dividers," IEEE Trans. Microw. Theory Techn., vol. 49, no. 7, pp. 1277-1288, Jul. 2001.

[16]. R. Darraji, A. K. Kawan, F. M. Ghannouchi, and M. Helaoui, "Digitally equalized Doherty RF front-end architecture for broadband and multistandard wireless transmitters," IEEE Trans. Microw. Theory Techn., vol. 63, no. 6, pp. 1978–1988, 2015.

[17]. X. Wang, I. Sakagami, Z. Ma, A. Mase, M. Yoshikawa, and M. Ichimura, "Miniaturized dual-band Wilkinson power divider with self-compensation structure," IEEE Trans. Compon., Packag., Manuf. Technol., vol. 5, no. 3, pp. 389–397, Mar. 2015.

[18]. M. B. Liao, Y. L. Wu, Y. A. Liu, and J. C. Gao, "Impedance transforming dual-band out-of-phase power divider," IEEE Microw. Wireless Compon. Lett., vol.24, no.8, pp.524–526, 2014.

[19]. W. Zhang, Z. Ning, Y. Wu, C. Yu, S. Li and Y. Liu, "Dual-band out-of-phase power divider with impedance transformation and wide frequency ratio," IEEE Microw. Wirel. Compon. Lett., vol. 25, no. 12, pp. 787-789, Dec. 2015

[20]. M. Zhou, Y. Gu, X. Li, S. Fu and B. Arigong, "A symmetrical two-way power divider with impedance transforming property," Texas Symposium on Wireless and Microwave Circuits and Systems, pp. 1-4, 2018.

[21]. M. A. Maktoomi, and M. S. Hashmi, "A Coupled Line based LSection DC-Isolated Dual-band real to real impedance transformer and its application to a dual-band T-junction power divider," Progr. Electromagn. Res. C, Vol. 55, pp. 95-104, 2014

[22]. R. W. Porto, V. J. Brusamarello, I. Müller, F. L. Cabrera Riaño and F. Rangel De Sousa, "Wireless power transfer for contactless instrumentation and measurement," IEEE Instrumentation & Measurement Magazine, vol. 20, no. 4, pp. 49-54, Aug. 2017.

[23]. C. Monzon, "A small dual-frequency transformer in two sections," IEEE Trans. Microw. Theory Techn., vol. 51, no. 4, pp. 1157- 1161, Apr. 2003.

[24]. [21]. Oh, H., W. Lee, and H. Lee, "A better balun? done the design of a 4 : 1 wideband balun using a parallel-connected transmission-line balun," Microw. Magaz., Vol. 18, No. 1, 85–90, 2017.

[25]. Zhang, W., Y. Wu, W. Wang, and X. Shen, "Planar compact dual-band coupled-line balun with high isolation," China Commun., Vol. 14, 40–48, 2017.

[26]. Yao, L., Y. Wu, M. Li, and Y. Liu, "Three-dimensional high-isolated dual-band balun using doublesided parallel strip line with inserted conductor plane," Electron. Lett., Vol. 53, 1211–1213, 2017.

[27]. Ahn, H.-R. and T. Itoh, "New isolation circuits of compact impedance-transforming 3-dB baluns for theoretically perfect isolation and matching," Trans. Microw. Theory Techn., Vol. 58, No. 12, 3892– 3902, 2010.

[28]. Wu, Y., L. Yao, W. Zhang, W. Wang, and Y. Liu, "A planar dual-band coupled-line balun with impedance transformation and high isolation," IEEE Access, Vol. 4, 9689–9701, 2016.

[29]. Aboualalaa, M., A.-B. Abdel-Rahman, A. Allam, H. Elsadek, and R.-K. Pokharel, "Design of a dual-band microstrip antenna with enhanced gain for energy harvesting applications," Antennas Wirel. Propag. Lett., Vol. 16, 1622–1626, 2017.

[30]. Kanaya, H., T. Nakamura, K. Kawakami, and K. Yoshida, "Design of coplanar waveguide matching circuit for RF-CMOS front-end," Electron. Commun. Jpn II, Vol. 88, No. 7, 1017–1023, 2005.

[31]. Li, X., L. Yang, S.-X. Gong, and Y.-J. Yang, "Dual-band and wideband design of a printed dipole antenna integrated with dual-band balun," Progress In Electromagnetics Research Letters, Vol. 6, 165– 174, 2009.

[32]. Xian, J. Z., X. Q. Lin, L. Y. Nie, J. W. Yu, and Y. Fan, "Wideband dual-polarization patch antenna array with parallel strip line balun feeding," IEEE Antennas Wireless Propag. Lett., Vol. 15, 1499– 1501, 2016.

[33]. Yu, J., Y. Sun, H. Zhu, F. Li, and Y. Fang, "Stacked-patch dual-band and dual-polarized antenna with broadband baluns for WiMAX and WLAN applications," Progress In Electromagnetics Research M, Vol. 68, 41–52, 2018.

[34]. Zhang, Z., M. F. Iskander, J. C. Langer, and J. Mathews, "Dual-band WLAN dipole antenna using an internal matching circuit," IEEE Trans. Antennas Propagat., Vol. 53, No. 5, 1813–1818, 2005.

[35]. Gao, J. P., X. X. Yang, J. S. Zhang, and J. X. Xiao, "A printed volcano smoke antenna for UWB and WLAN communications," Progress In Electromagnetics Research Letters, Vol. 4, 55–61, 2008.

[36]. Ahn, H., and T. Itoh, "Isolation circuit of impedance-transforming 3-dB compact baluns for near perfect output matching and isolation," IEEE MTT-S International Microwave Symposium, Anaheim, CA, 113–116, 2010.

[37]. Zhang, W., Y. Liu, Y. Wu, W. Wang, M. Su, and J. Gao, "A Complex Impedance-Transforming Coupled-Line Balun," Progress In Electromagnetics Research Letters, Vol. 48, 123–128, 2014.

[38]. Gupta, R., and M. S. Hashmi, "High impedance transforming simplified Balun architecture in microstrip technology," Microw. Optical Technol. Lett., Vol. 60, No. 12, 3019–3023, 2018.

[39]. Nikravan, M.-A., and Z. Atlasbaf, "T-section dual-band impedance transformer for frequencydependent complex impedance loads," Electron. Lett., Vol. 47, No. 9, 551–553, 2011.

[40]. Monzon, C., "Analytical derivation of a two-section impedance transformer for a frequency and its first harmonic," IEEE Microw. Wirel. Compon. Lett., Vol. 12, No. 10, 381–382, Oct. 2002.

[41]. K. Song, Y. Mo, and Y. Fan, "Wideband four-way filtering-response power divider with improved output isolation based on coupled lines," IEEE Microw. and Wirel. Compon. Lett., vol. 24, no. 10, pp. 674-676, 2014.

[42]. L. Guo, H. Zhu, and A. M. Abbosh, "Wideband tunable in-phase power divider using three-line coupled structure," IEEE Microw. and Wirel. Compon. Lett., vol. 26, no. 6, pp. 404-406, June 2016.

[43]. P. Kim, J. Jeong, G. Chaudhary, and Y. Jeong, "A design of unequal termination impedance power divider with filtering and out-of-band suppression characteristics," in European Microw. Conf. (EuMC), Sep. 2015, pp. 123–126.

[44]. Y. Wu, Z. Zhuang, M. Kong, L. Jiao, Y. Liu, and A. A. Kishk, "Wideband filtering unbalanced-to-balanced independent impedance-transforming power divider with arbitrary power ratio," IEEE Trans on Microw. Theory Techn., vol. 66, no. 10, pp. 4482–4496, Oct 2018.

[45]. P. Kim, G. Chaudhary, and Y. Jeong, "Analysis and design of an unequal termination impedance power divider with bandpass filtering response," Electron. Lett., vol. 53, no. 18, pp. 1260-1262, 2017.

[46]. S. Rosloniec, "Three-port hybrid power dividers terminated in complex frequency-dependent impedances," IEEE Trans. Microw. Theory Techn., vol. 44, no. 8, pp. 1490–1493, Aug 1996.

[47]. Y. Wu, Z. Zhuang, L. Jiao, and Y. Liu, "A novel balanced-to-unbalanced complex impedance-transforming in phase power divider," IEEE Access, vol. 5, pp. 16 205–16 213, 2017.

[48]. W. Hallberg, M. zen, D. Kuylenstierna, K. Buisman, and C. Fager, "A generalized 3-db wilkinson power divider/combiner with complex terminations," IEEE Trans. Microw. Theory Techn., vol. 66, no.10, pp. 4497–4506, Oct 2018.

[49]. D. Banerjee, A. Saxena and M. Hashmi, "A Novel Design of a Bandwidth Enhanced Dual-Band Impedance Matching Network with Coupled Line Wave Slowing," 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 2019, pp. 1770-1773.

[50]. A. Saxena, D. Banerjee, M. Hashmi and M. Auyenur, "A Dual-Band Impedance Transfomer for Matching Frequency Dependent Complex Source and Load Impedances," 2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Lausanne, Switzerland, 2019, pp. 173-176.

[51]. A. Saxena, D. Banerjee, R. Gupta and M. Hashmi, "Design of π-Structure Dual-Band Matching Network With Unequal Susceptance Cancellation Stubs," 2018 IEEE MTT-S International Microwave and RF Conference (IMaRC), Kolkata, India, 2018, pp. 1-3.

[52]. D. Banerjee, A. Saxena, M. Hashmi and F. Ghannouchi, "A Compact Dual-Band Impedance Matching Network Based on All-Pass Coupled Lines," 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS), Windsor, ON, Canada, 2018, pp. 937-939.

[53]. D. Banerjee, M. Hashrni and F. Ghaanouchi, "A Novel Design of a Tri-Band Impedance Matching Network Based on the Concept of an Impedance Bridge," 2018 Asia-Pacific Microwave Conference (APMC), Kyoto, 2018, pp. 318-320.

[54]. A. Saxena, D. Banerjee, M. Hashmi and F. Ghannouchi, "Design of Compact Dual-Band Matching Network with Single Unequal Susceptance Cancellation Stub," 2018 Asia-Pacific Microwave Conference (APMC), Kyoto, 2018, pp. 300-302.

[55]. D. Banerjee, A. Saxena and M. S. Hashmi, "A Simple Robust Equal-Split T-Junction Power Divider at Three Frequencies," 2018 Twenty Fourth National Conference on Communications (NCC), Hyderabad, 2018, pp. 1-4.

[56]. A. Saxena, D. Banerjee and M. S. Hashmi, "A Novel Meandered Coupled-Line Tri-Band Impedance Matching Network," 2018 Twenty Fourth National Conference on Communications (NCC), Hyderabad, 2018, pp. 1-4.

[57]. D. Banerjee, A. Saxena and M. S. Hashmi, "A Novel Concept of Virtual Impedance for High Frequency Tri-Band Impedance Matching Networks," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 9, pp. 1184-1188, Sept. 2018.

[58]. M. H. Maktoomi, D. Banerjee and M. S. in, "An Enhanced Frequency-Ratio Coupled-Line Dual-Frequency Wilkinson Power Divider," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 7, pp. 888-892, July 2018.

[59]. D. Rano, D. Banerjee and M. S. Hashmi, "A Miniaturized Three-Stage Dual-Frequency Matching Network," 2017 IEEE MTT-S International Microwave and RF Conference (IMaRC), Ahmedabad, 2017, pp. 1-5.

[60]. D. Banerjee, A. Saxena and M. Hashmi, "A novel compact tri-band matching network utilizing two dual-band transformers at a common reference frequency," 2017 IEEE Asia Pacific Microwave Conference (APMC), Kuala Lumpar, 2017, pp. 1080-1083.

[61]. D. Banerjee, A. Saxena and M. Hashmi, "A Novel Compact Tri-Band Impedance Matching Network with Enhanced Frequency Ratios," 2017 IEEE MTT-S International Microwave and RF Conference (IMaRC), Ahmedabad, 2017, pp. 1-4.

[62]. M. A. Maktoomi, R. Gupta, M. H. Maktoomi, M. S. Hashmi and F. M. Ghannouchi, "A genaralized multi-frequency impedance matching technique," 2016 16th Mediterranean Microwave Symposium (MMS), Abu Dhabi, 2016, pp. 1-4.

[63]. M. A. Maktoomi, M. H. Maktoomi, A. P. Yadav, M. S. Hashmi and F. M. Ghannouchi, "Dual-frequency admittance property of two sections transmission-line and application," 2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), Abu Dhabi, 2016, pp. 1-4.

[64]. R. Gupta, M. S. Hashmi and M. H. Maktoomi, "An Enhanced Frequency Ratio Dual Band Balun Augmented with High Impedance Transformation," in IEEE Transactions on Circuits and Systems II: Express Briefs.

[65]. R. Gupta, M. A. Maktoomi and M. S. Hashmi, "A new high frequency balun with simplified impedance matching technique," 2016 Asia-Pacific Microwave Conference (APMC), New Delhi, 2016, pp. 1-4.

[66]. M. A. Maktoomi, V. Panwar, M. S. Hashmi and F. M. Ghannouchi, "A dual-band matching network for frequency-dependent complex loads suitable for dual-band RF amplifiers," 2014 IEEE International Microwave and RF Conference (IMaRC), Bangalore, 2014, pp. 88-91.

[67]. M. A. Maktoomi and M. S. Hashmi, "A CAD assisted design methodology for wide-band arbitrary power division coupler implemented in microstrip technology," 2016 Twenty Second National Conference on Communication (NCC), Guwahati, 2016, pp. 1-4.

[68]. M. A. Maktoomi, M. Akbarpour, M. S. Hashmi and F. M. Ghannouchi, "A Theorem for Multi-Frequency DC-Feed Network Design," in IEEE Microwave and Wireless Components Letters, vol. 26, no. 9, pp. 648-650, Sept. 2016.

[69]. R. Gupta, A. Saxena, M. A. Maktoomi and M. S. Hashmi, "An high impedance transformation ratio dual-band matching network with DC isolation capability," 2017 IEEE Asia Pacific Microwave Conference (APMC), Kuala Lumpar, 2017, pp. 1069-1072.

[70]. M. A. Maktoomi and M. S. H. Indraprastha, "A novel power divider structure using the gysel and wilkinson power dividers with only one grounded resistor," 2015 IEEE MTT-S International Microwave and RF Conference (IMaRC), Hyderabad, 2015, pp. 227-229.

[71]. M. A. Maktoomi, M. S. Hashmi and F. M. Ghannouchi, "Theory and Design of a Novel Wideband DC Isolated Wilkinson Power Divider," in IEEE Microwave and Wireless Components Letters, vol. 26, no. 8, pp. 586-588, Aug. 2016.

[72]. R. Gupta, M. A. Maktoomi and M. S. Hashmi, "Dual-Band Wilkinson Power Divider with Port Extensions," 2018 IEEE MTT-S International Microwave and RF Conference (IMaRC), Kolkata, India, 2018, pp. 1-4.

[73]. M. H. Maktoomi, D. Banerjee and M. S. in, "An Enhanced Frequency-Ratio Coupled-Line Dual-Frequency Wilkinson Power Divider," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 7, pp. 888-892, July 2018.

[74]. M. A. Maktoomi, M. S. Hashmi, A. P. Yadav and V. Kumar, "A Generic Tri-Band Matching Network," in IEEE Microwave and Wireless Components Letters, vol. 26, no. 5, pp. 316-318, May 2016.

[75]. M. A. Maktoomi, R. Gupta and M. S. Hashmi, "A dual-band impedance transformer for frequency-dependent complex loads incorporating an L-type network," 2015 Asia-Pacific Microwave Conference (APMC), Nanjing, 2015, pp. 1-3.

[76]. M. A. Maktoomi, M. Akbarpour, M. S. Hashmi and F. M. Ghannouchi, "On the Dual-Frequency Impedance/Admittance Characteristic of Multisection Commensurate Transmission Line," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 6, pp. 665-669, June 2017.

[77]. M. A. Maktoomi, A. P. Yadav, M. S. Hashmi and F. M. Ghannouchi, "Dual-frequency impedance matching networks based on two-section transmission line," in IET Microwaves, Antennas & Propagation, vol. 11, no. 10, pp. 1415-1423, 16 8 2017.

[78]. M. A. Maktoomi, M. S. Hashmi and F. M. Ghannouchi, "Improving Load Range of Dual-Band Impedance Matching Networks Using Load-Healing Concept," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 2, pp. 126-130, Feb. 2017.

[79]. M. A. Maktoomi and M. S. Hashmi, "A Performance Enhanced Port Extended Dual-Band Wilkinson Power Divider," in IEEE Access, vol. 5, pp. 11832-11840, 2017.

[80]. M. A. Maktoomi, M. S. Hashmi and F. M. Ghannouchi, "A Dual-Band Port-Extended Branch-Line Coupler and Mitigation of the Band-Ratio and Power Division Limitations," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 7, no. 8, pp. 1313-1323, Aug. 2017.

[81]. M. A. Maktoomi, M. S. Hashmi and F. M. Ghannouchi, "Systematic Design Technique for Dual-Band Branch-Line Coupler Using T- and Pi-Networks and Their Application in Novel Wideband-Ratio Crossover," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 6, no. 5, pp. 784-795, May 2016.

[82]. R. Gupta, A. P. Yadav and M. S. Hashmi, "Symmetric tri-band balun architecture with a systematic design procedure," 2017 Twenty-third National Conference on Communications (NCC), Chennai, 2017, pp. 1-5.