Title of Thesis

Capacitor-less Low Dropout Regulator (LDO)

By

Ravi Kumar Gupta (MT18171)

Under the Supervision of

Dr. G.S.Visweswaran

Indraprastha Institute of Information Technology Delhi
July, 2020

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Submitted
in partial fulfillment of the requirements for the degree of
Master of Technology

to
Indraprastha Institute of Information Technology Delhi
July, 2020

Certificate

This is to certify that the thesis titled "***Capacitor-less Low Dropout Regulator (LDO)***" being submitted by **Ravi Kumar Gupta (MT18171)** to the *Indraprastha Institute of Information Technology Delhi*, for the award of the Master of Technology, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

July, 2020

Dr. G.S.Visweswaran
Department of Electronics and Communication Engineering
Indraprastha Institute of Information Technology Delhi
New Delhi 110020

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Abstract

An output capacitor-less low-dropout (LDO) regulator with a wide range of load currents is proposed. It is based on the requirement of static comparator and current sinking circuit to control the gate of pmos pass gate. High gain and high UGB error amplifier is crucial in deciding the dc regulation of capless circuit. An error amplifier, current sink circuit and a high SR static comparator is sufficient for controlling the output in load transient. For 5pf output capacitance 600mV of output voltage is maintained for 0-4mA of load current. Current sink circuit works only for the time when output is low and comparator and error amplifier feedback circuit has not yet responded. After they responded to transients the current sink circuit gets turned off using the internal state of comparator. Comparator also works only for output reaches 50mV lower else error amplifier is sufficient to handle the small ripples. For dc regulation of 1% of output voltage the setup is made to respond faster. A 65nm tech with 900mV of supply is used for the design. Using gm/id technique each circuit was able to works in subthreshold region, allowing us to work on lower voltages. Pmos input subthreshold opamp of 67dB gain, 59degree PM, 1.29MHz of UGB and quiescent current of 10uA is used as error amplifier. SR of 6V/us is used for the comparison. Output voltage with settling time of 7nsec is obtained for the capless LDO.

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Chapter 1

Introduction

1.1 Motivation

In SoC there is a need of efficient and reliable power delivery for proper working of different modules. One of them is DC to DC converter or Voltage regulator. In Power management Integrated Circuit (PMIC) the power delivery range varies from a few of uW to 10W. PMIC enables us to have efficient power supply module in IC with small size on SoC. PMIC allows us to have multiple supplies of different values w.r.t . voltage and current. These ICs plays an important role in small size electronics e.g. wearable devices, automobile, phone etc. In smart phones for back light display it requires +ve and –ve supplies both, for battery charging it requires a constant current supply, for LED flash it requires 1A to 2A of currents i.e. it requires a current regulator apart from voltage regulator. Wearable need ultra low power circuits as PMIC for small size battery and area. A DC to DC converter helps us in getting a constant voltage supply for any load.

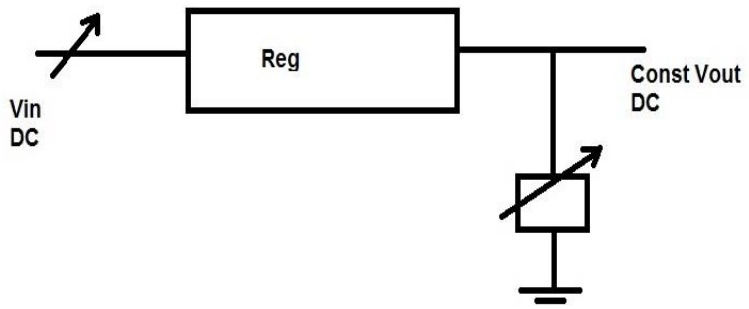


Fig 1: DC-DC Converter or Voltage Regulator

1.2 Thesis Organization

The thesis comprises of 8 chapters. Chapter 2 has the background of the regulator and it's performance parameters. Chapter 3 shows the challenges in the capless LDO. Chapter 4 guides us about the design method and techniques for the appropriate design.

Chapter 5 has the building block designs that requires for a system of capless LDO i.e. Opamp, Comparator, BGR etc. Chapter 6 has the layout of the design.

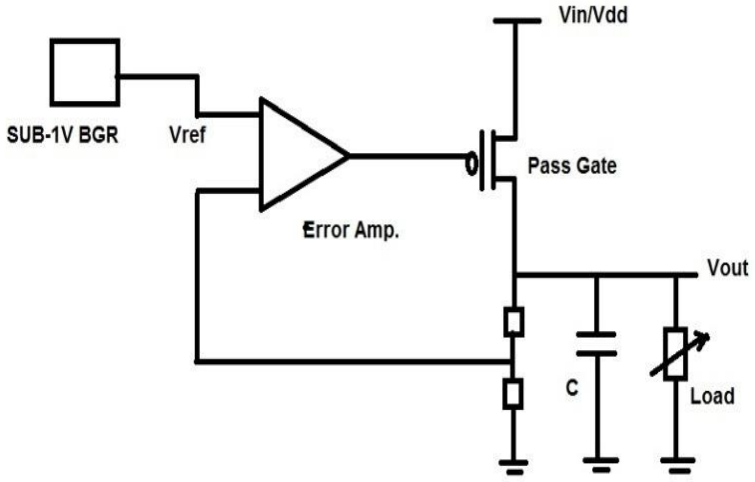
Chapter 7 depicts about the result and it's comparison. At the last we have chapter 8 about the conclusion and future work.

Chapter 2

Background

2.1 Linear Regulator

One of a type of regulator is linear regulator, which is continuous time regulator with no switching and where output voltage is lower than the input supply. Linear regulator requires passfet as a switch between input and output supply. It also requires a **capacitor to stabilize the output** from the load transients.



Vout = (1+(R1/R2)) Vref

Fig 2: Linear Regulator

Error Amplifier controls the gate of passfet. When load varies the Current from the passfet is controlled by error amplifier. It is important to note here that vin is different from vref.

- Pout = Vout * Iout
- Ploss = (Vin – Vout) * Iout = Vdrop * Iout

For less power loss there must be much lesser drop in passfet. When a linear regulator works in low drop mode it is said to be a Low dropout regulator. It is efficient only at low dropout. There is no noise from switching circuit. It is suitable for low power delivery and low load current. Also it has low cost as compared to other regulator types.

- Efficiency w.r.t. Power = Pout/(Pout+Ploss)
- Efficiency w.r.t Votage = Vout/Vin

2.2 Regulator Performance Parameter

2.2.1 DC Regulation

It is measure of an error in output voltage.

$$\text{Regulation} = \frac{\text{Change in Output Voltage}}{\text{No-load Output Voltage}}$$

$$\therefore \text{Regulation} = \frac{V_{(\text{no-load})} - V_{(\text{full-load})}}{V_{(\text{no-load})}}$$

For good dc regulation high gain error amplifier, low offset error amplifier and a constant vref w.r.t. process, voltage and temperature is required.

2.2.2 Line regulation

It is a measure of error in output voltage due to change in the input supply (line)

- Line Regulation = ΔVout / Δvin (at low freq)

2.2.3 Load regulation

It is a measure of error in output voltage with change in load current.

- Load Regulation = ΔVout / Δiout

Cumulative high gain of error amplifier and passfet is desired for the good load regulation i.e less change in vout with change in load current.

2.2.4 Line transient

When there is up and down step change in line supply, it result in over and undershoot respectively in the vout of regulator. The reason is the feedback doesn't respond quickly.

- Line Transient = ΔVout / Δvin (step change)

For a good regulator ΔVout because of line transient should be less than 5% of Vout and tsettle will be calculated when it will reach to 1% of Vout. For a good line transient generally a

large capacitor at output is used. Also feed forward from line is taken with feedback to decide the gate control of passfet and high bandwidth regulator is made for loop to respond faster.

2.2.5 Load transient

It is a measure of error in output voltage with step change in load current.

- Load Transient = ΔVout / Iload (step change)

When there is up and down step change in load, it result in under and overshoot respectively in the vout of regulator. The reason is the feedback doesn't respond quickly and the capacitor draws and gets respectively the extra current. **Large capacitor** and high bandwidth regulator is useful in less load transient. Large Capacitor will act as transient filter because any fast change at output will be filtered out by it.

2.2.6 Power supply rejection ratio (PSRR)

It is the ability to reject any change in vout w.r.t. ac change in vin.

- PSRR = ΔVout/ΔVin

Large output capacitor value will allow less ripple to go at load. It is calculated in dB. A large –ve dB PSRR value is good.

2.2.7 Efficiency

- Efficiency w.r.t. Power = Pout/(Pout+Ploss)

2.2.8 Quotient current

It is an internal current consumption of the regulator at no load condition. It should be as low as possible for better current efficiency.

- Iq = as minimum as possible from the design along with correct operation
- Efficiency w.r.t. Current = Iout/(Iout+ Iq)

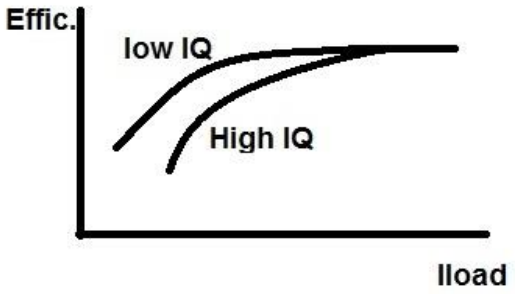
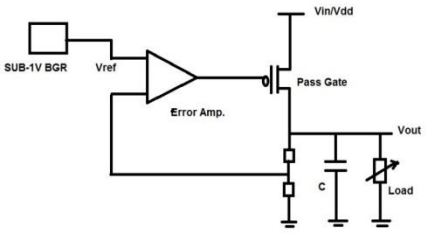


Fig 3: current efficiency

It is evident from the graph that at low load there must be a regulator of low quotient current should be used for good current efficiency.

2.3 Pass Element

2.3.1 pmos as passfet



Vout = (1+(R1/R2)) Vref

At vout we see high ro at drain of pmos.

Advantage:

Vout is at drain of pmos i.e for 600mV output we can use supply of 700mV and there is pmos gets on because of negative vgs value. So pmos passfet can be used for low voltage operation.

2.3.2 nmos as passfet

At vout we will see output impedence of 1/gm at source of nmos.

Advantages :

1. When there is change in line voltage, there is change in vds not in vgs, so if it is biased in saturation there in no change in the load current i.e. a good supply rejection is seen.

2. If load current increases, then the cout decreases which result in increase in vgs value of nmos passfet, thus the passfet current increases automatically or we can say that there is good feedback i.e. load transient is improved.

Disadvantage:

vg = vt + vout

Let vt = 500mV, Vov = 100mV then Vgs = 600mV i.e if vout is 600mV required then there must be gate voltage of passfet should be 1.2V. So we can't use nmos as passfet for low voltage supply availability.

Chapter 3

Challenges in the Capless LDO

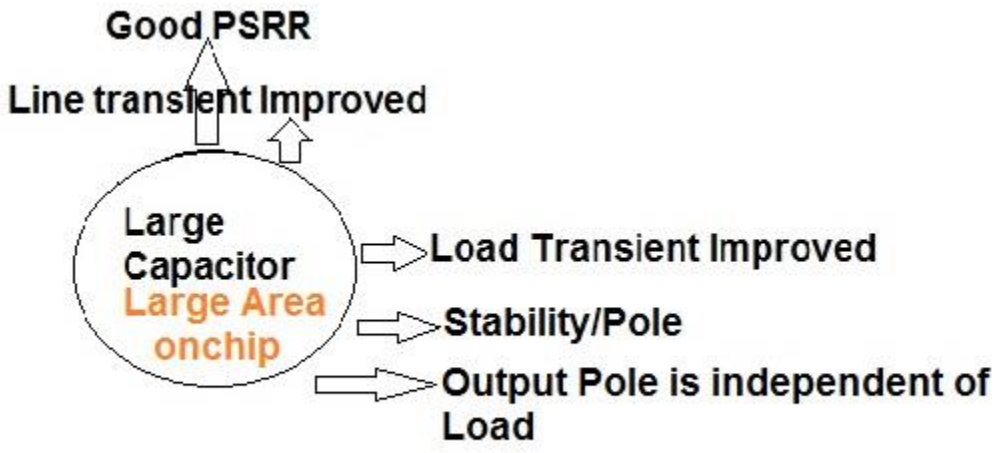


Fig 4: Usage, advantage and disadvantage of large capacitor in LDO

Large capacitor helps in compensating the line & load transient. A stable system needs a capacitor to make the poles at desired location. Also for large load capacitor it gives us the liberty to vary the resistive load in a wide range and our system remains stable.

In capless LDO the benefits of Large capacitor is not available as in handy. It requires different methods and circuits to avail the same results as of large capacitor based LDO.

Chapter 4

Design Method

4.1 Design Method

4.1.1 Feedback and stability

We know that for negative feedback circuit to be a stable there must loop gain less than 1 at phase loop of -180. For second order system we compensate the second pole by making second pole out of UGB i.e. dominant pole method or we cancel the second pole i.e. pole zero cancellation. Dominant pole method by moving first pole more inside is not suitable because it lead to lesser bandwidth.

We try to have the phase margin above 60degree for no ringing and good settling at output. Usually it is made above 45 degree for fast response with some ripple. System with PM > 90degree is over damp and PM<45degree is marginally stable. While for 1^{st} order system PM is 90.

Also while designing it should be noted that there shouldn't be any zero near -180degree phase to avoid less gain margin.

Stability => |Loop gain|< 1 at -180° loop phase, 2° Sys, PM>45°, Gain > 60dB

4.1.2 Poles analysis

2.1. In capless LDO since the output capacitor is less, the dominant pole is due to parasitic and it is made fix by proper sizing of the error amplifier output node and passfet so that the regulator operation can be made fix.

For moving the pole at the gate of passfet inside we make the output resistance of error amplifier large. And to move it at higher frequency we make the output resistance low by introducing a voltage buffer between error amp and passfet.

2.2. When output capacitance is large then the dominant pole is decided by it. But in our design we will use 5pF as load capacitance which is low, so it's pole will be far.

2.3. Conventional LDO loop gain includes two poles, one at the gate of passfet and other at load.

2.4. Note that the output pole is dependent on the load resistance, hence it is variable. But for capless LDO output capacitor is low i.e pole is far enough, so the dependency of load resistance in capless is less. Pole by load is calculated in no load case because for this the pole is minimum of it's all values.

2.5. In capless when both the poles are near either we will make pole due to passfet gate out of UGB or make it dominant such that pole by load is out of UGB. Secong has a few advantages such as UGB is fixed, output pole can be made more farther by making drain resistance of pmos passfet low by suitable size.

4.1.3 Voltage Buffer

Source follower or common drain can be used as voltage buffer where we need to adjust the resistance and to have no loading effect. For source follower rout is approx 1/gm which is low.

4.1.4 Stability

When dominant pole is made of passfet gate capacitance is near to output pole, we try to make it more dominant so that output pole can be seen as far by it. For this extra capacitor is attached from the supply to gate so that supply rejection can also be made possible.

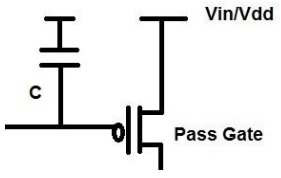


Fig 5: Method to make dominant gate pole

But for this capacitor requirement is large, to avoid it we use miller capacitor in circuit.

But again there is problem of bandwidth, for this we use pole zero cancellation i.e either we will cancel lower freq pole due to gate capacitance using left hand zero by Rz in series with miller capacitor because output pole is dependent of load resistance which is variable or insert the left hand zero by Rz in between two poles. If required we can move the gate capacitance using buffer in-between error amplifier and passfet.

4.1.5 Load Regulation

Load regulation can be analyzed by calculating rout at no load condition. By this we need large output capacitor but is not possible in capless we will use other method to compensate it. In our design we have used high slew rate comparator and pmos based comparator in feedback to make transient better.

4.1.6 PSRR

One way to improve PSRR if dominant pole is by passfet gate capacitance (i.e in capless LDO) is to have Large UGB to avoid peaking in the PSRR.

4.2 Design Techniques

We need a set of equations for the comparative analysis of the design and make it usable, so that every specification can be made.

1. gm = f(W/L, Id, Vgs-Vt)

   Vgs-Vt = $\sqrt{(2\mathrm{Id}/(\mathrm{unCoxW}/\mathrm{L}))}$

   Vdsat = Vds min for saturation = Vgs-Vt

2. gm = f(a variable, a constant)

   $\mathrm{gm} = \frac{\mathrm{unCoxW}}{\mathrm{L}}(\mathrm{Vgs} - \mathrm{Vt})$

   $\mathrm{gm} = \sqrt{\left(\frac{2\mathrm{unCoxW}}{\mathrm{L}}\right)\mathrm{Id}}$

   gm = 2Id/(Vgs- Vt)

3. At a constant Vov :

   gm/id = const

   gm2/gm1 = id2/id1 = W2/W1 = constant

4. In subthreshold gm=Id/nVt

   gm α Id

5. if W/L = const then gm α Vgs- Vt

   If Id = const then gm α 1/Vgs-Vt

6. In saturation region ro = 1/λId

7. To have suitable W at short channel we use gm/id technique:

   From gm, Id, W, Vov if we have two values available, we can get other two values. After characterization of a model we have “gm/Id Vs Vov” and “Id/W Vs gm/Id” graph, this help us to design the circuit efficiently.

Chapter 5

Designs

5.1 Subthreshold Pmos Input Opamp

5.1.1 Schematic

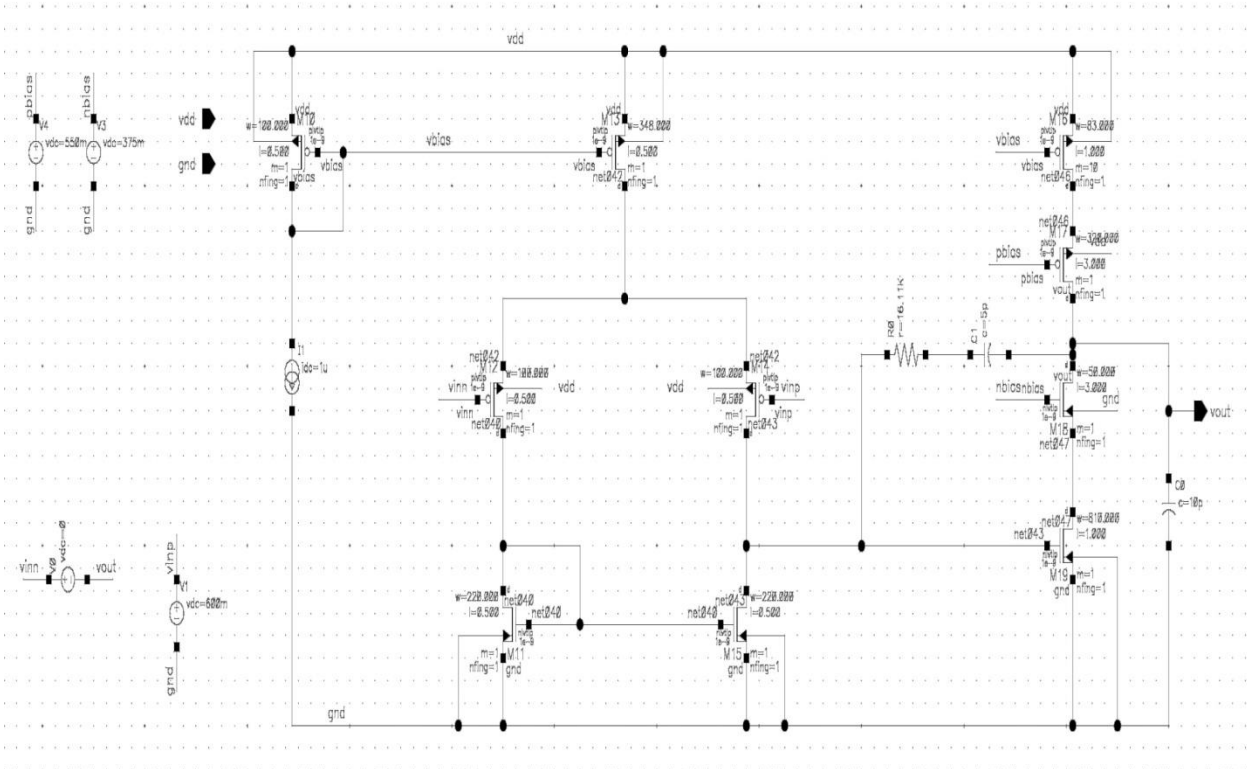


Fig 6: Pmos input Opamp

In second stage we have used cascode transistors for improved gain. We have used gm/id technique for efficient size of the transistors.

Advantage of using pmos input:

1. We can have as small as input voltage because we can apply low voltage at the gate of pmos and it work correctly.

2. In second stage gm of nmos is large which helps in high frequency application.

3. We have less effect of output load capacitance on the pole at the output because gm of nmos is large which has major affect.

wp2 = gm7/(C1+C2) and C2 = f(Cload)

4. For less load resistance also we have a large gain.

5. Low freq noise is less because holes are less trapped in surface states.

5.1.2 Result

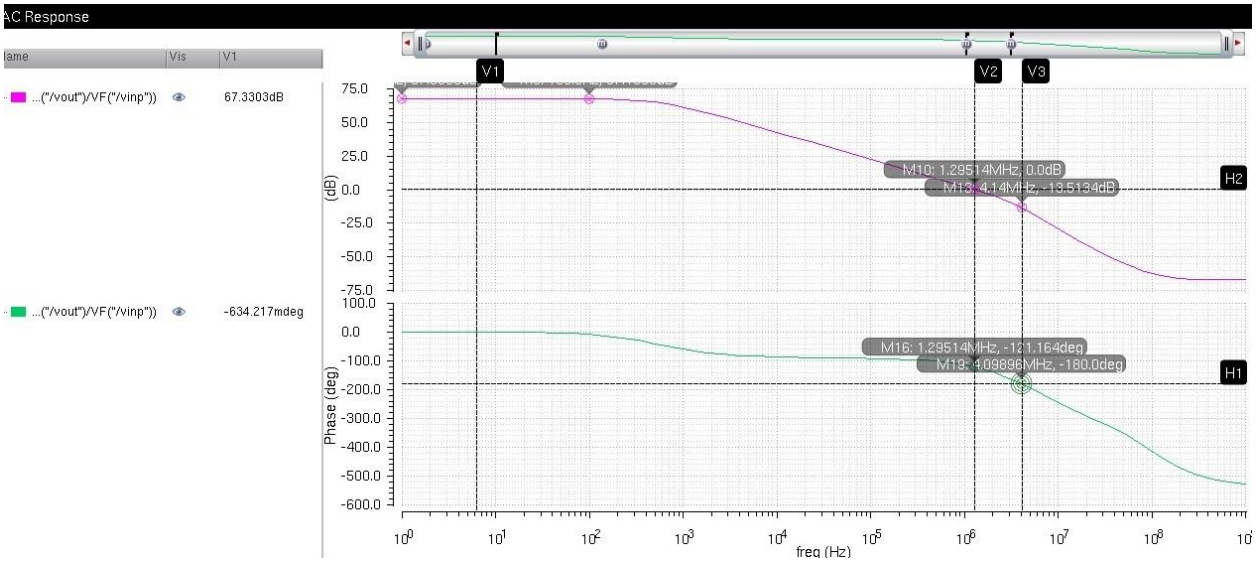


Fig 7: AC Response of Opamp

We need to observe here that the most of the parasitics are out of the second pole and we have made the system stable only using 10uA of current. The BW of 1.29 MHz is made possible with PM of 59degree but we need better GM also. The 5pf of coupling capacitor is used to move the pole at sufficient point for the better stable opamp.

Op Amp Load	10pF
Cc	5pF
Rc	16.11Kohm
BW	1.295Mhz
Av	67dB
PM	59degree
GM	13.51dB
Bias Current Total	10u
ICMR+	631mV
ICMR-	514mV
CMMR	45dB
Offset	24uV
Power Dissipated	9uW
PSSR	-60dB
SR	1.1 V/us

Table 1: Specifications obtained for Subthreshold pmos input Opamp

5.2 High SR Comparator

5.2.1 Schematic

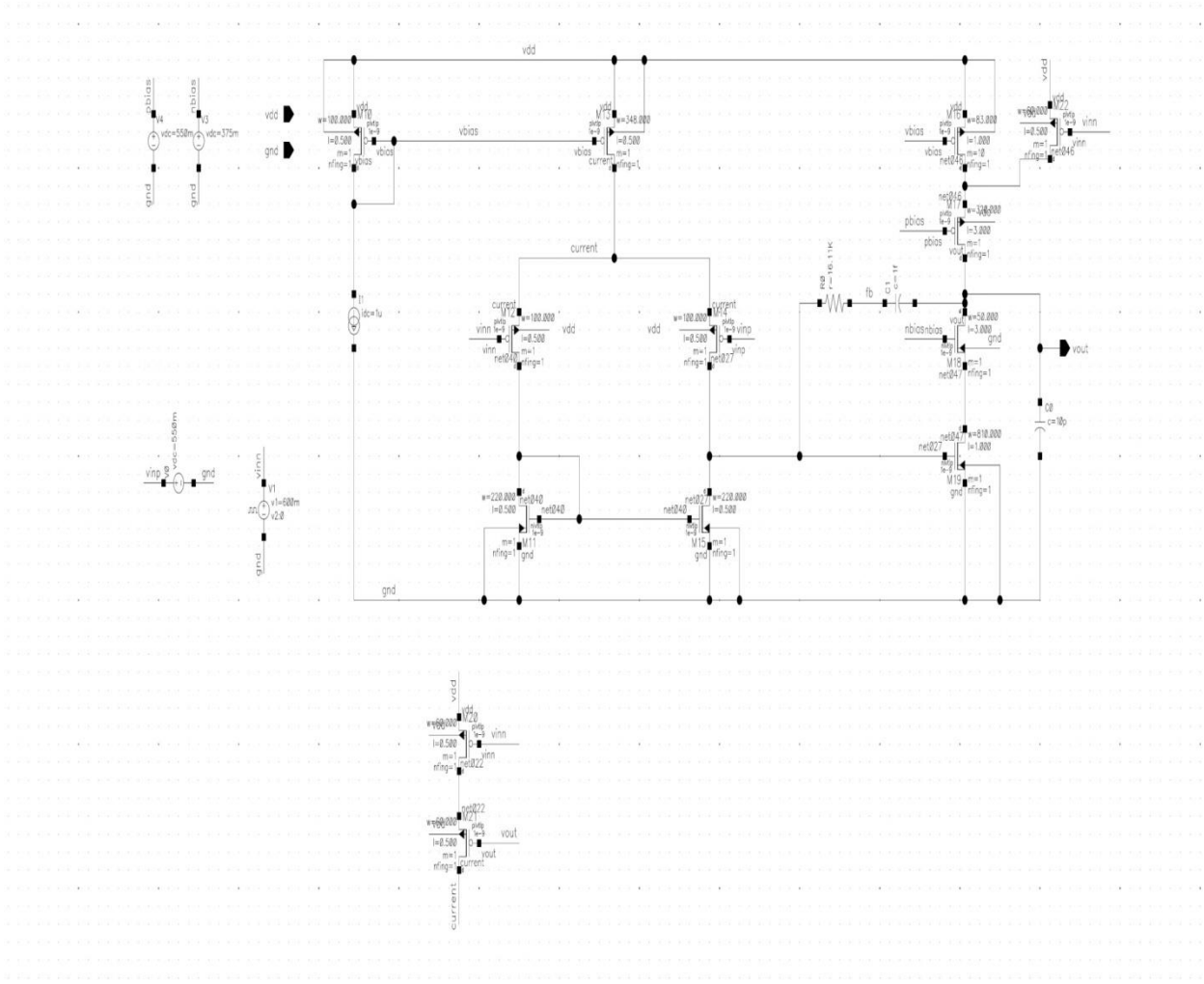


Fig 8: Schematic High SR Comparator

For high slewing we have added a transient current in the branch such that there is extra current will flow until vout reached to its desired value of vdd. There is two pmos connected in series which have input of vout and vinn, the drain terminal is directly connected to source of pmos input. Also there is extra pmos in the output branch which has input of vinn for giving sudden current in the output.

5.2.2 Result

We have obtained SR of 6V/us, which was sufficient for a good regulation purpose.

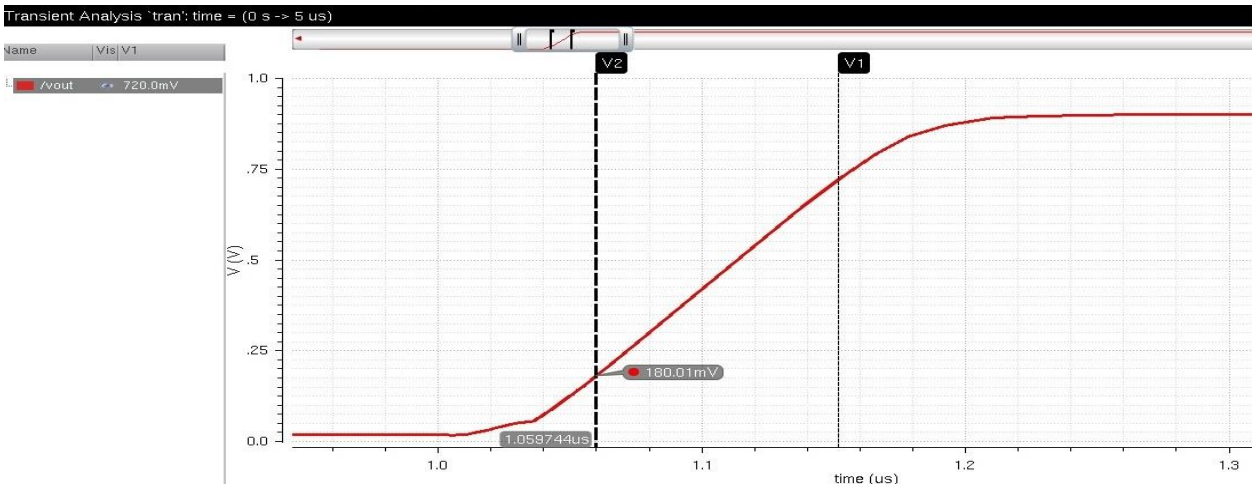


Fig 9: 20% of Output voltage

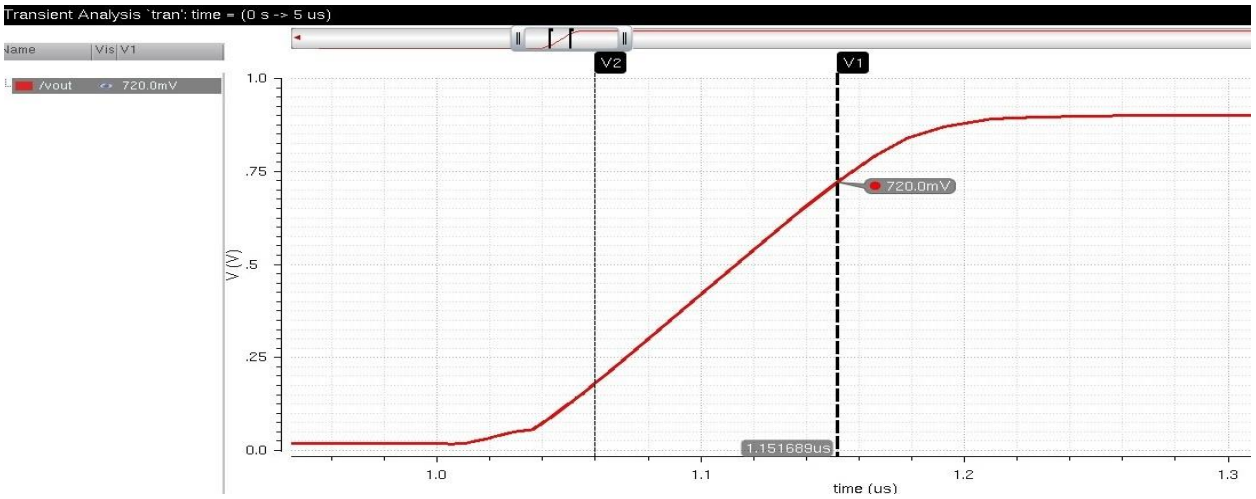


Fig 10: 80% of output voltage

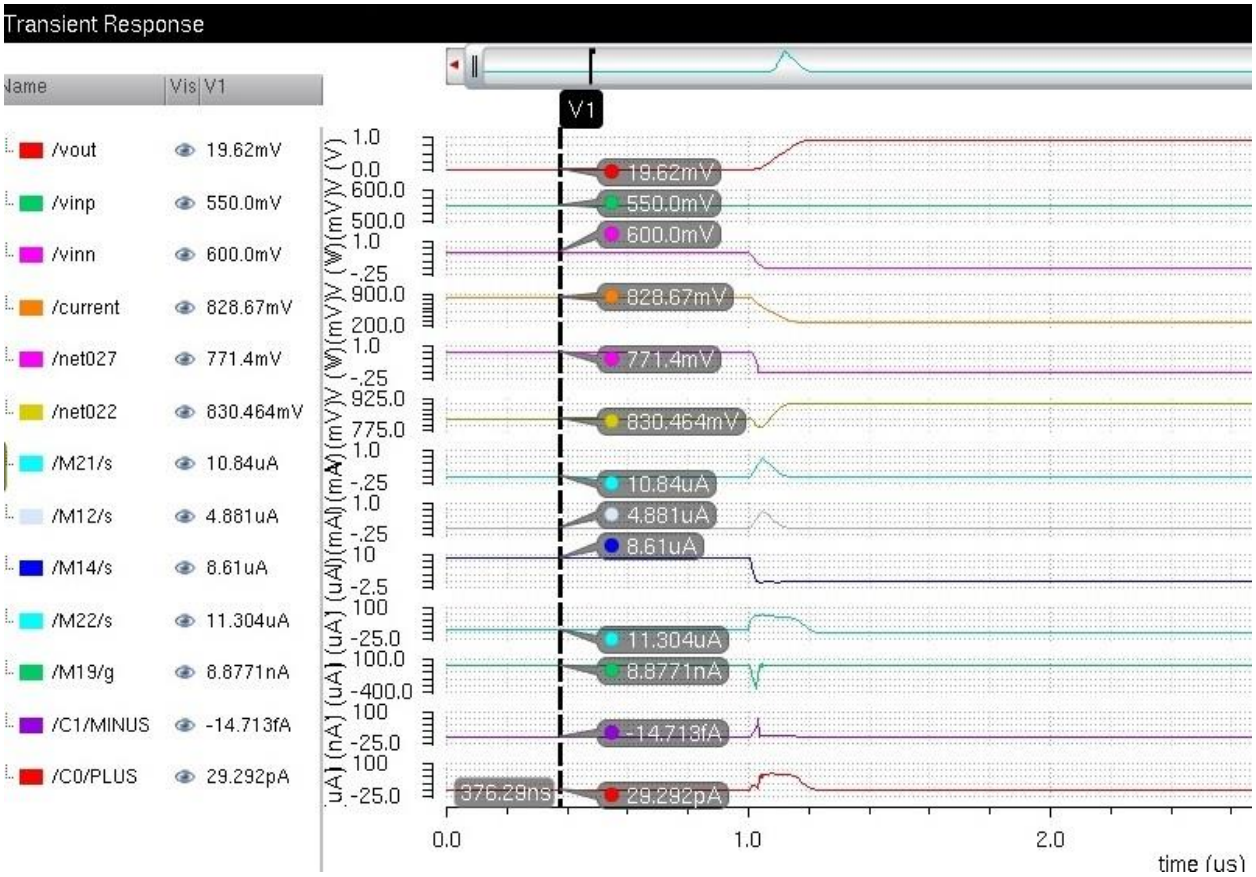


Fig 11: state when input voltage is greater than reference

We can see that when vinn is greater than vinp there is low output.

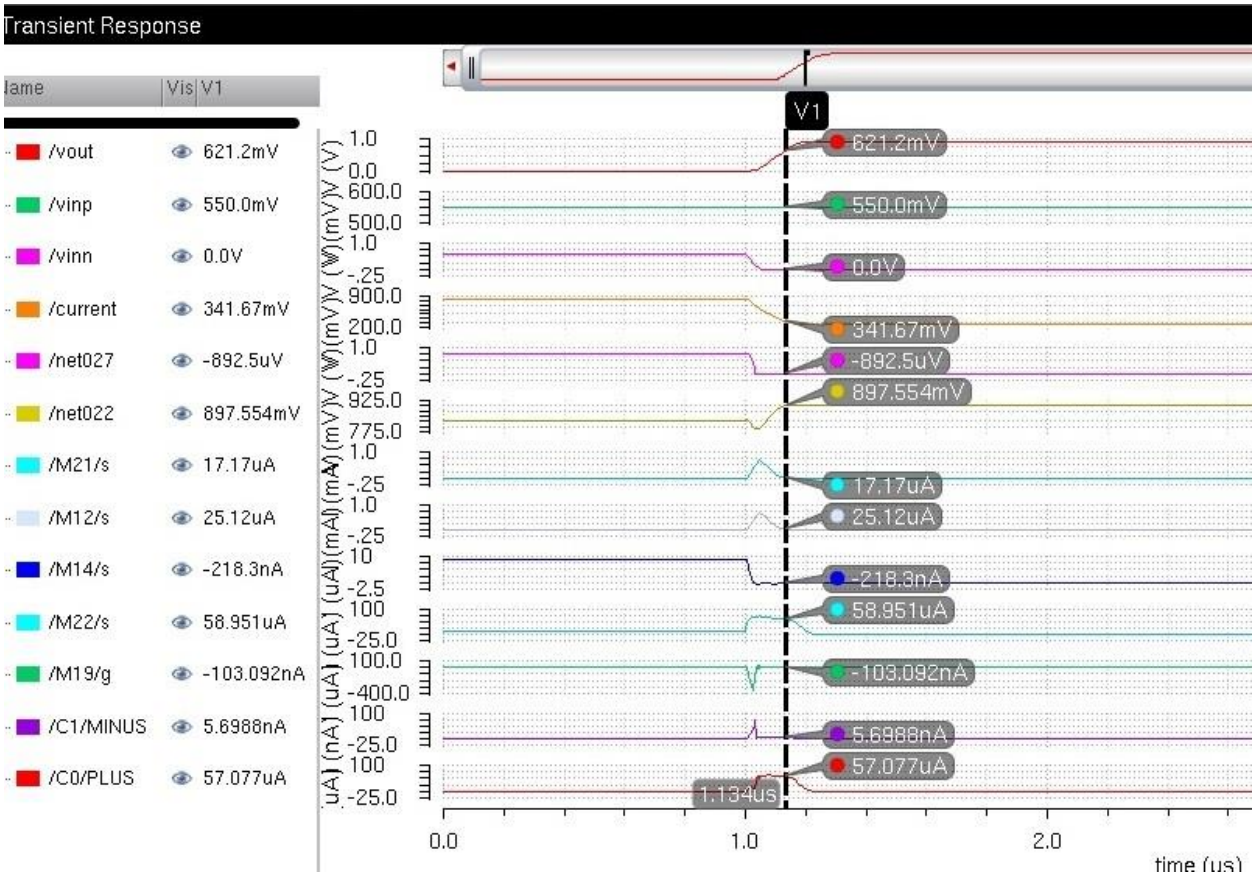


Fig 12: when input voltage is less than reference voltage, there is transition in output

During the transition there is about 100uA current flow at the output to make the slew very high.

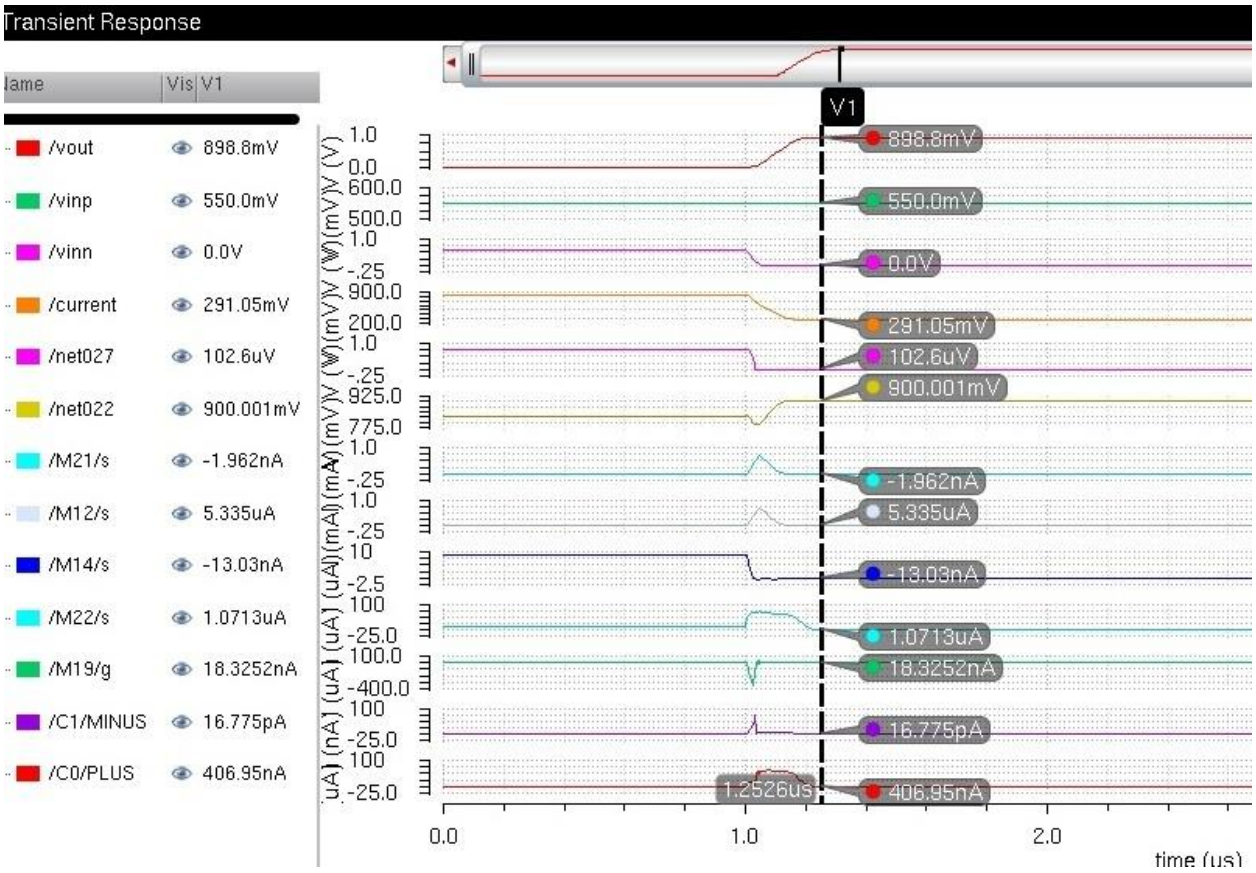


Fig 13: state just after comparison

After vout reached to vdd we can see that extra circuit gets turnoff as ont the input of pmos is vout also. This makes the circuit efficient to use.

5.3 Current Steering

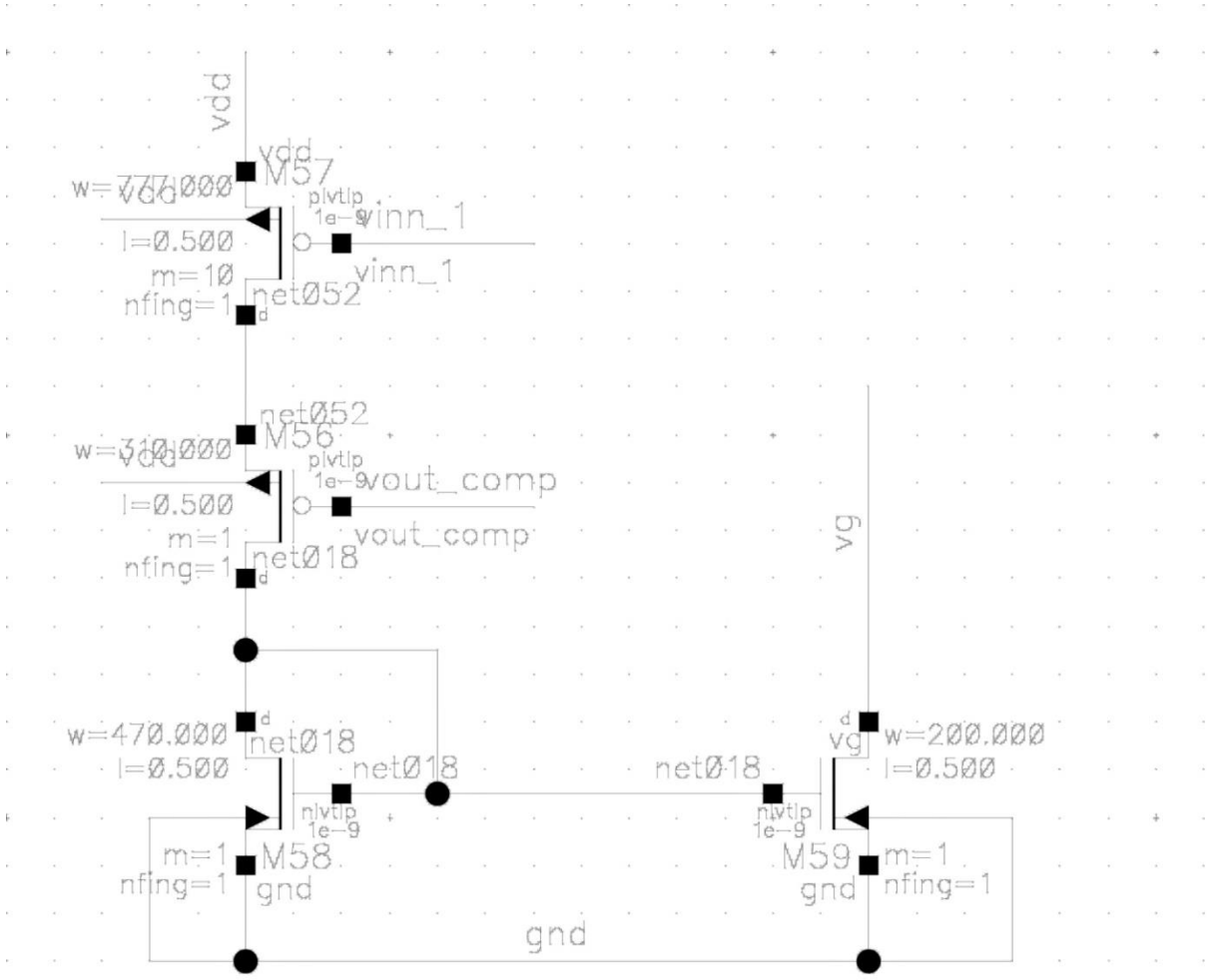


Fig 14: Current Steering Circuit

If we see the circuit, the output of comparator is connected to sandwiched pmos (between pmos which has the vout of LDO as the input and current mirror). This circuit fetch the transient current from the parasitic of gate of the passfet thus make the vg goes to low and hence helps in making large current from the passfet in a very less time. Once the comparator vout goes high this current attenuate to zero and after that only comparator will work.

5.4 Overshoot control

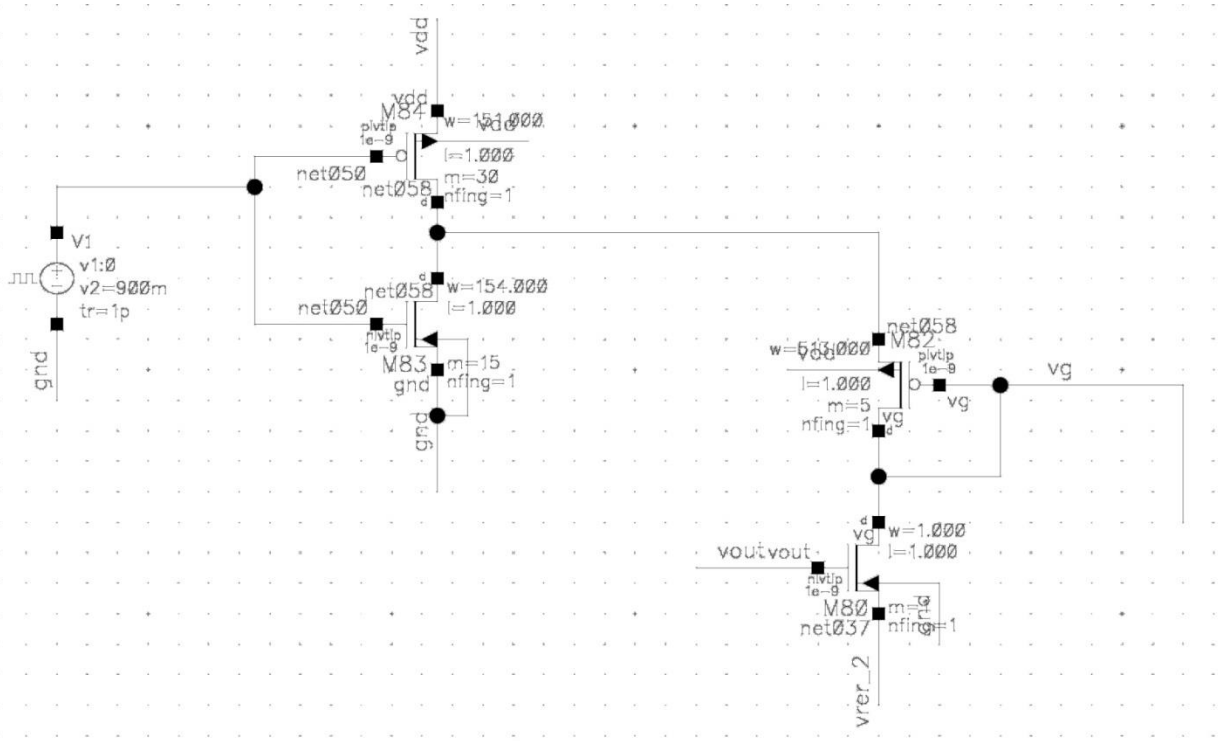


Fig 15: Overshoot Control

This circuit will control the gate of pmos of passgate directly when there is current change in load from 4mA to 0.5mA. We can see that the lower nmos is connected to vout and vref_2 (= 450mV), for the needed comparison of vout. If there is current in lower nmos when there is overshoot the equivalent voltage is generated at the diode connected pmos. The mechanism also include the excess current from pmos goes to parasitic of gate from path of drain to gate of pmos and thus the gate of the pass gate is charged quickly to compensate the extra current from the passgate.

5.5 Sub 1 V Bandgap Reference

5.5.1 Subthreshold Region

- Diode connected NMOS (Tech-65nm) is used in subthreshold region (weak inversion region) in place of diode connected BJT, as both have same current characteristic.

- Primary advantages:
    1. MOS only circuit
    2. Less area on device
    3. Voltage headroom can be decreased to 100mV
    4. gm is high hence higher current efficiency

- Design Constraint:
    1. VDS>4VT i.e VDS>100 mV at room Temp. (VT=Voltage Equivalent of Temp)
    2. VGS<Vth (Vth = Threshold Voltage)

5.5.2 Sub-1V BGR

- To generate a PVT compensated voltage.
- As the technology is scaling down, supply voltage is also scaled down. Sub-1V means the supply and the reference output voltages are lower than 1V.
- Note: Vth decreases linearly with temperature (CTAT).

5.5.3 Startup Circuit

- Since Supply independent loop is stable at Zero current, it needs starting current in the beginning of the operation. After the circuit start working it will be decoupled from the loop.

5.5.4 Current Mode Operation

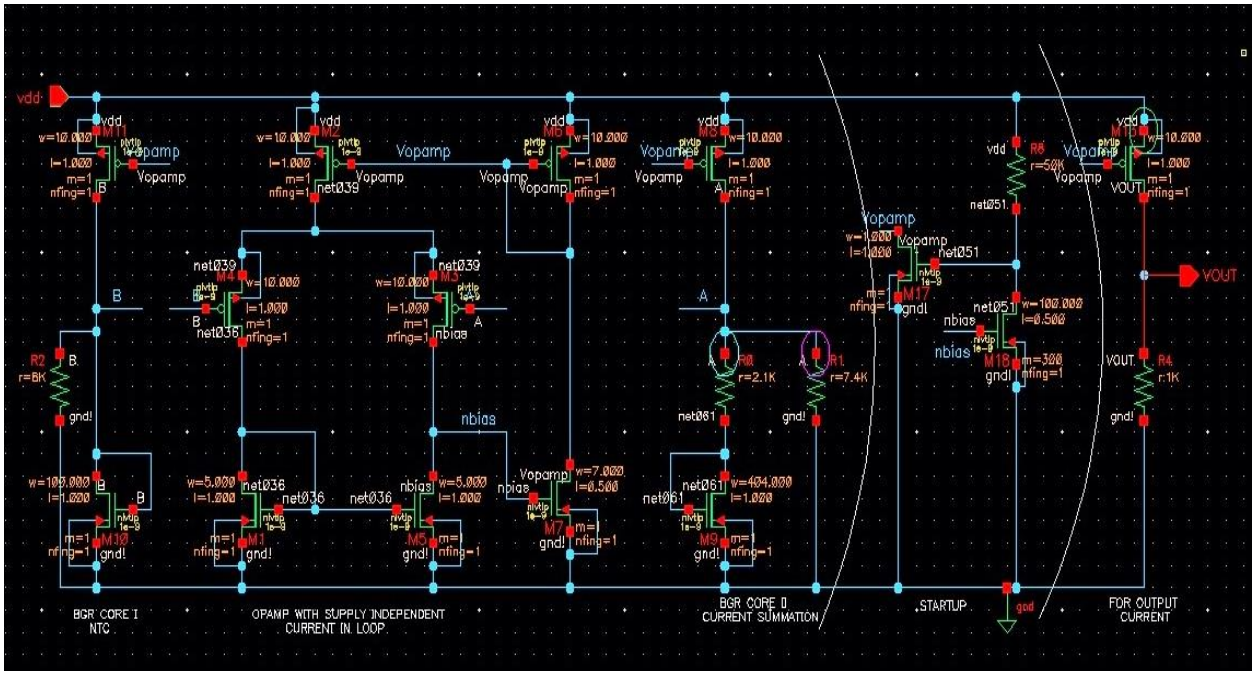


Fig 16: Schematic current mode

1. Current mirrors with current feedback mechanism are used to minimize supply dependence as opamp's supply current is derived from it's output itself.
2. This supply independent current is copied to generate CTAT voltage [LHS] and also PTAT current [RHS].
3. Core produces ICTAT and IPTAT; there is summation of both the currents which results in a reference current which is copied for the output. This current with the help of resistor is converted to reference voltage.

Result:

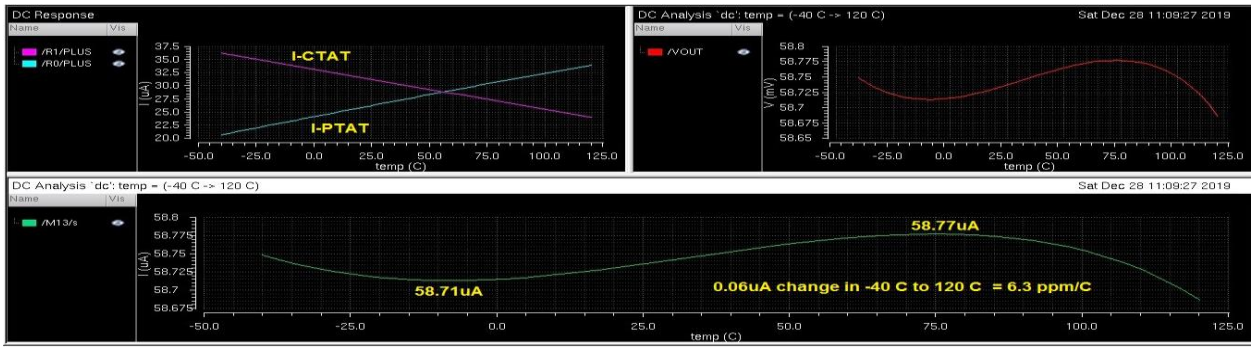


Fig 17: Current Variation

- Change in Reference Current / °C for -40°C to 120°C = 6.3ppm/°C
- Vdd = 950mV
- Iref = 58.4uA

5.5.5 Current Mode Operation with Curvature Compensation

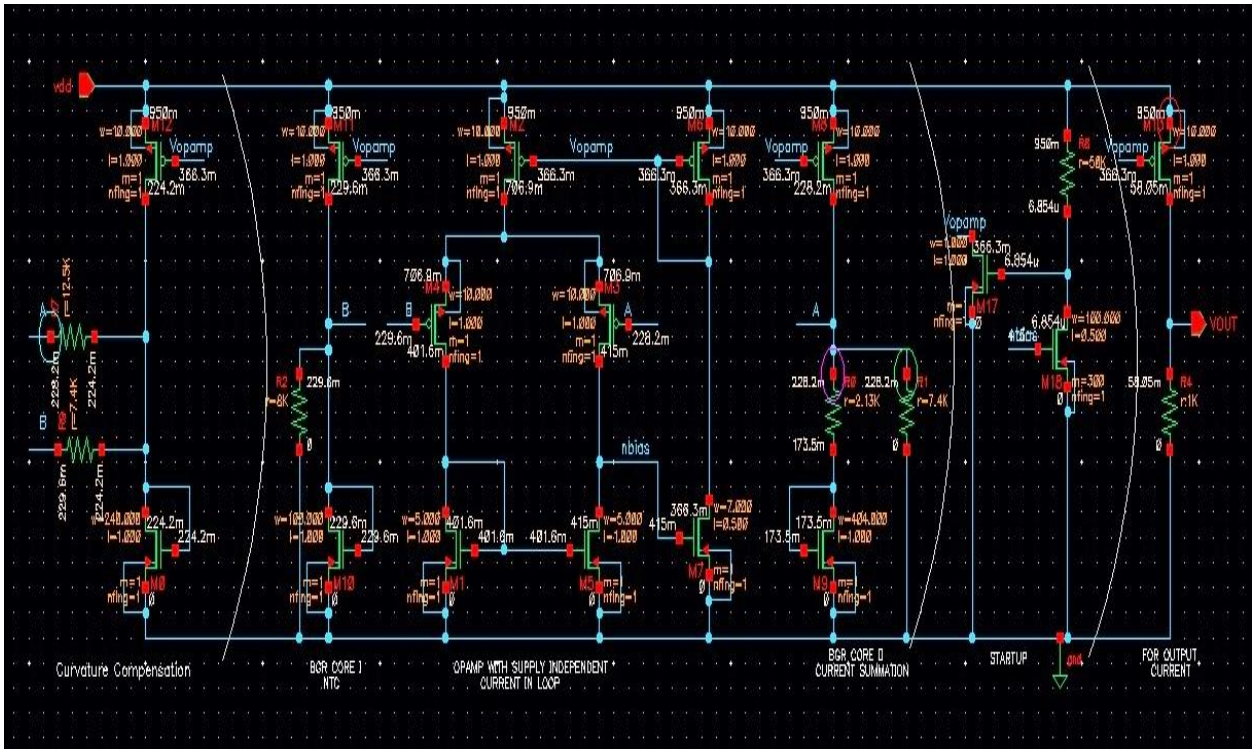


Fig 18: Schematic current mode with curvature correction

- The first order temperature compensation is done by BGR as depicted in sec. 2, thus leading to a second order temperature dependence.
- The basic idea is to correct the non-linear term by correcting the ICTAT current at extreme temperature i.e. avoiding second order.
- M10 generates VBE with IPTAT,
  M0 generates VBE with constant current
- Extra two resistors drain an additional current from M8 and M11, proportional to the above mentioned VBE difference, leads to the desired curvature correction.

Result:

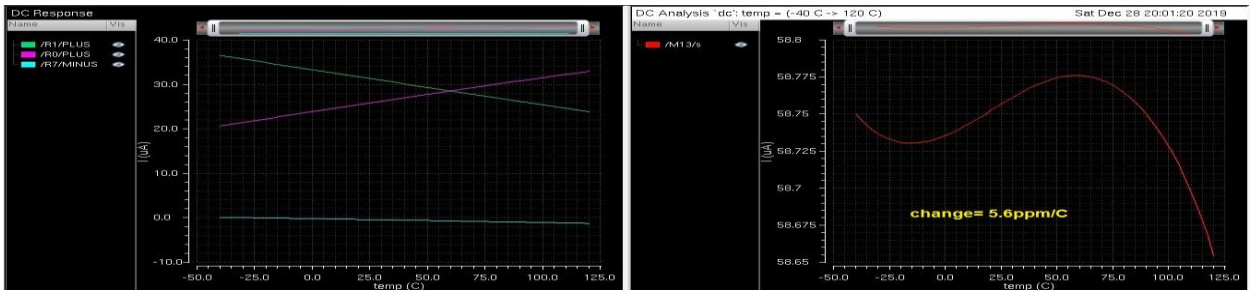


Fig 19: Current Variation

- Change in reference current /°C for -40°C to 120°C = 5.6 ppm/°C

5.5.6 Summary

- Current mode with second order curvature compensation is best suitable for low voltage reference generation. The temperature coefficient achieved is good in current mode.
- Voltage mode is simpler while design but has more variation in reference voltage.
- With 6ppm/°C it can be used as a reference.

5.6 Capless LDO

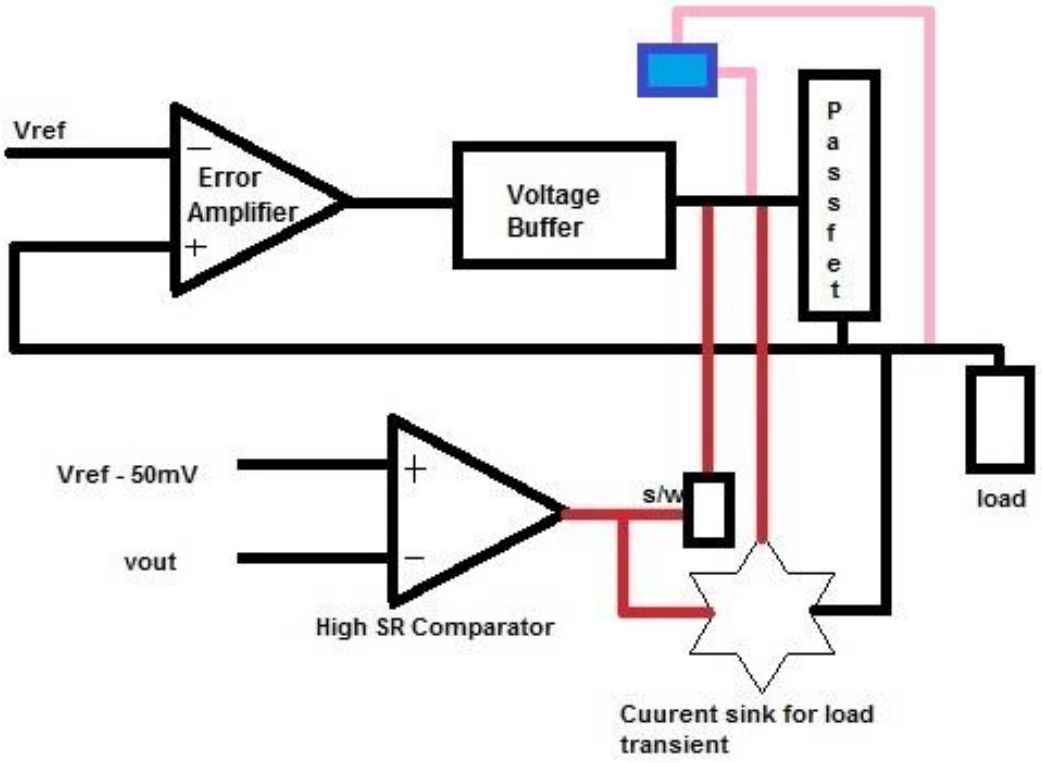


Fig 20: Capless LDO with High SR Comparator and High current sink

5.6.1 Components

1. Pmos based passfet
2. pmos input error amplifier
3. Source follower voltage Buffer
4. High Slew Rate Static Comparator
5. Current sink for load transient

6. Switch after Comparator

7. Current Load

5.6.2 Working Process

When load current is high then there is sudden drop in Vout which result in three parallel action:

1. Error amplifier output gets low which result in turning on of the pmos passfet, this is normal operation.

2. Along with this a current sink will also get starts when output voltage is still low and output of High SR comparator is not yet reach to vdd. It is used during step change in load current. It helps in providing high current from Passfet for a very short time like a spike.

If the transient is lower than Vref – 50mV, then high SR comparator output gets Vdd which will turn off the large current sink and turn on a nmos switch which will sink small amout the current from gate of pmos so that on required current can flow through passfet to load.

3. Static comparator is used for High SR Comparator so that when vout is stabled to above vref – 50mV it will get turn off.

5.6.3 Result

Vout=vref = 600mV

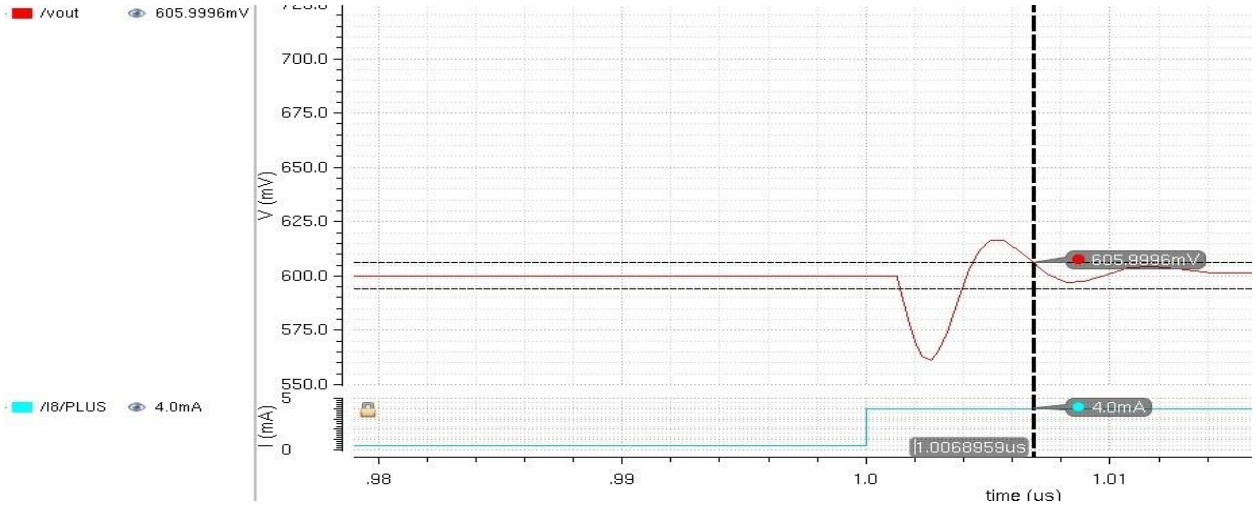


Fig 21: Undershoot in Output Voltage

This waveform shows that the undershoot and number of cycles before it gets stable to 600mV. For 1% dc Regulation it requires around 7ns of time, after that vout will remain close to 600mV.

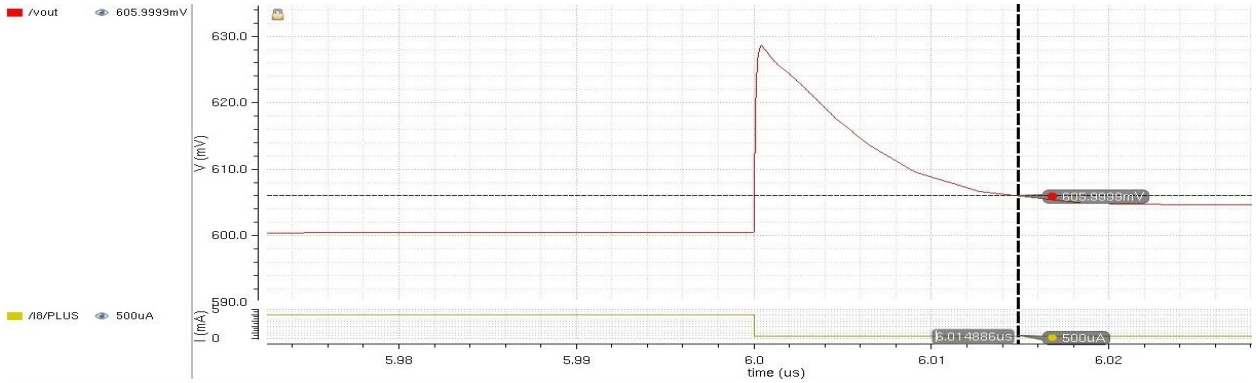


Fig 22: Overshoot in Output Voltage

When there is change in load current from 4mA to 0.5mA, we see that there is overshoot of 24mV which is essential in working of LDO and can't be completely removed.

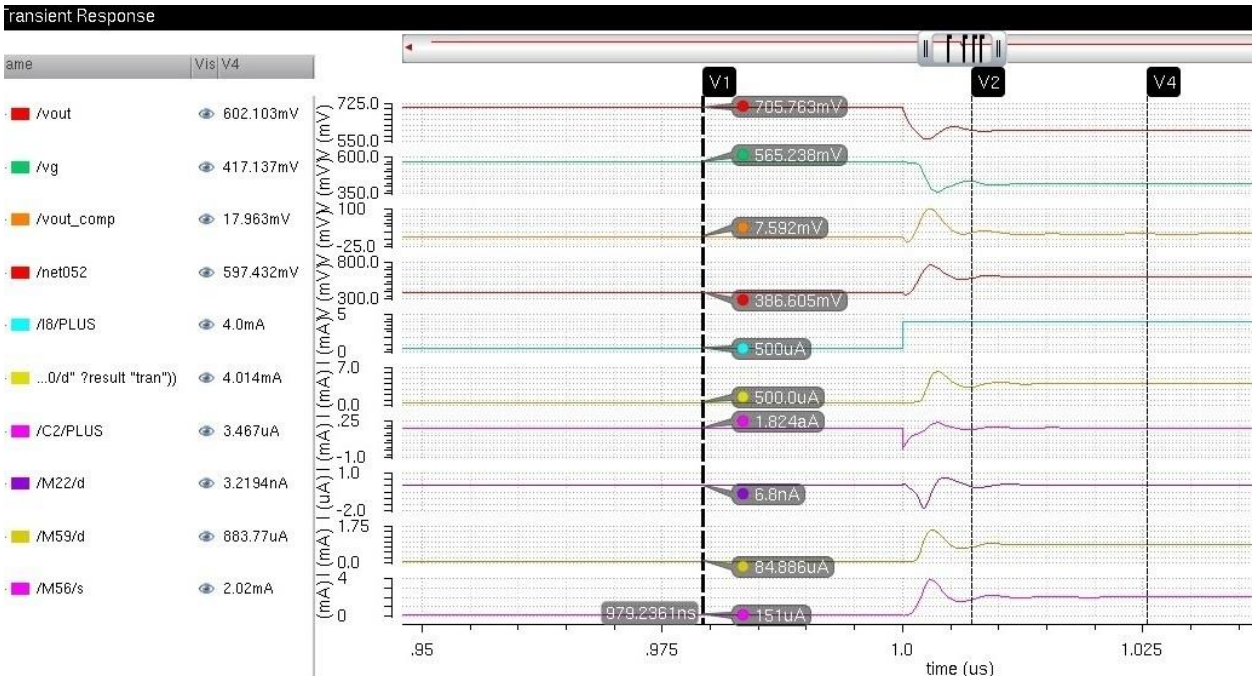


Fig 23: No Load Condition

At no load we need min value of load current of 0.5mA and it will be flowing thourgh pmos passfet for 600mV to be maintained. There is quotient current in the system.

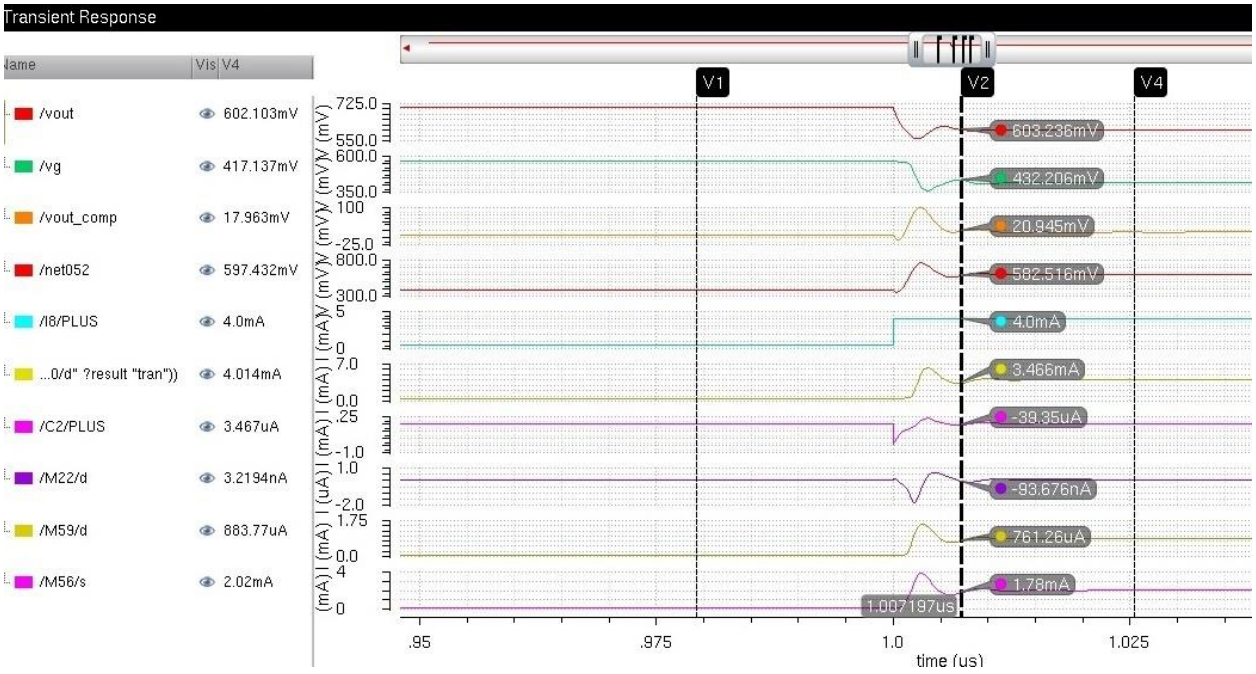


Fig 24: Output Voltage within 1% Load Regulation

From this waveform it can be seen that at full load the vout gets a dip, passfet current is still min value of load current i.e 0.5mA, a few of the current is provided by the capacitor. After this current and other circuits begin to work and made the vout to get back to 600mV fast.

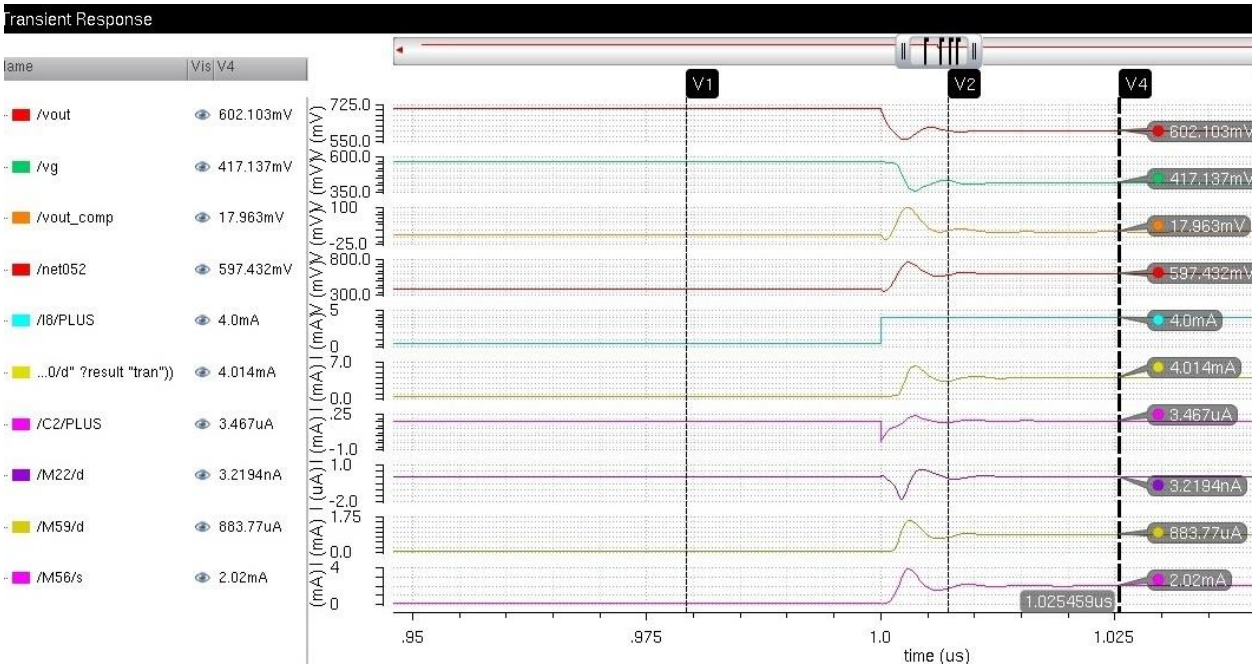


Fig 25: Output voltage after steady state

At steady state vout is maintained at 600mV and all other circuits are maintained at their normal operation value.

Chapter 6

Layout

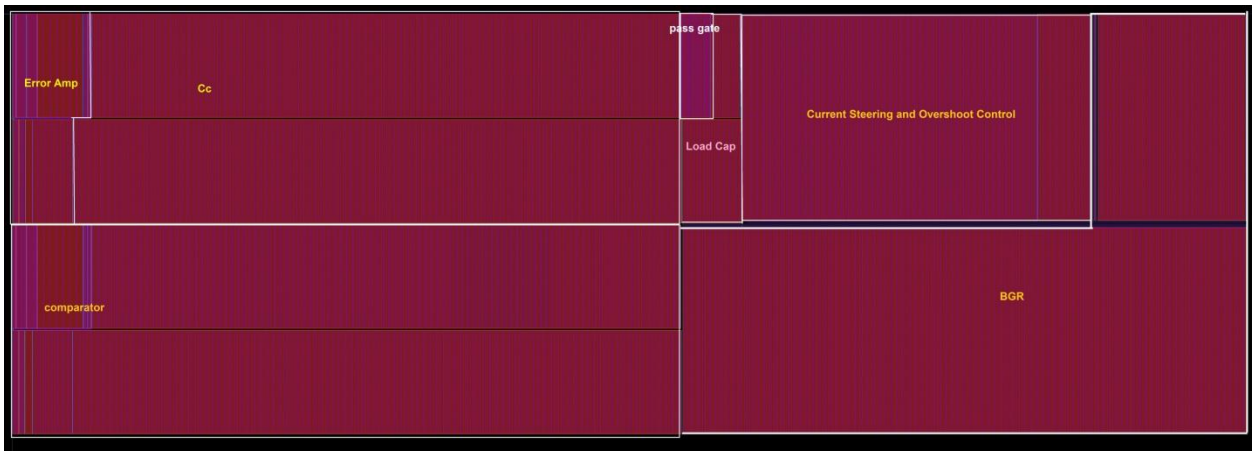


Fig 26: Layout

The total Area consumed for complete design is 406*204 umsq. We can see that the curative design of error amplifier lead to a very small area. The Bandgap reference takes a significant area on the chip. We have used nmos type mos capacitor for the layout.

Chapter 7

Result and Analysis

7.1 Result Comparison

	Ref 1	Ref 2	Ref 7	This work
Tech [Area]	180nm [41000 squm]	65nm	65nm	65nm [82824 squm]
Steady state Vout- Vref	< 10 mV	< 20 mV	N/A	<6 mV (1% of 600mV)
Iload max	10mA	10mA	50mA	4 mA
Time to rise Iload spike	2.5ns	1ns	N/A	0 to 4mA in 1ns
Voutref - Voutmin [undershoot]	150mV	82mV	133.9mV	39 mV
Voutmax - vref [overshoot]	70mV	40mV	N/A	24 mV
Tsettling	<40ns	1.15ns	150ns	7 ns

Cout	3nf	140pf	40pF	5 pf
Vin	-3.2V	1.15V	600mV	900 mV
Vout	-3 V	1V	550mV	600 mV
Iq	80 - 110 uA	50–90uA	32uA	10 - 150 uA
PSR@1Mhz	N/A	-12dB	-20.7dB	-23dB
Load Regulation	1mV/mA	1.1mV/mA	N/A	1.5mV/mA
PM	N/A	N/A	N/A	48degree
Vref - Trans peak	Vref-50mV	N/A	N/A	Vref-50mV
Vref+steady state regulation	Vref + 30 mV (1% of the vout)	N/A	N/A	Vref+6mV
FOM* (fs)	**495000**	**10332**	**68.5**	**182.5**

* F OM = $(C_{out} \times \Delta V_{peak} \times I_Q) \ / \ I^{\wedge 2}{}_{o,max}$

Table 2: Result comparison LDO

7.2 Result Analysis

The FOM of our design is 182.5 greater than 68.7 of ref 7 means there is scope for the improvement in our circuit. For 5pf the maximum change in output at load change is 39mV for 4mA load current, this change in vout is comparable to 133.9mV of ref 7. The PM is 48 degree which is sufficient but can be improved for better transient response. Setting time of 7ns is sufficient but this can also be improved much lower value as we see for ref 2, it is 1.1ns. So use of a correct topology is necessary for the design and usage of a suitable architecture is required.

Chapter 8

Conclusion and Future Work

8.1 Conclusion

Gm/id technique is good for designing for subthreshold region analog modules. Subthreshold opamp as error amplifier, LDO, comparator etc can be designed using gm/id method with solid understanding of each terminal voltage and currents. Capacitor less LDO with 7nsec tsettle for 1% of vout dc load regulation is obtained having 39mV of undershoot for 0-4mA load current. A 900mV is converted to 600mV using 5pF of load capacitance. A current sink circuit and a high SR static comparator with efficient current injection lead to control the gate of pmos passfet perfectly. There is no switching circuit or any clock is used which will become a source of noise. Dynamic circuits are also available as option for controlling the gate of pmos passfet but it results in high amount of switching power loss.

8.2 Future Work

When layout was observed carefully, the coupling capacitor for LDO is 70pf which takes the area much larger as compared to other components of the system; hence a capacitor multiplier circuit is needed which reduces the area but then the current requirement of the system will be increased. Also Current steering and overshoot control circuit area in the layout is significantly large because a current mirror mechanism is used, which again can be reduced but for that we need highly accurate circuit to compare the vout at the transient condition. Load capacitor is also added in the layout, which we can remove and see the area comparison.

Bibliography

LDO

[1] Choi, S.; Huh, Y.; Park, S.; Yoon, K.; Bang, J.; Shin, S.; Ju, Y.; Yang, Y.; Yoon, J.; Ahn, C.; et al. “A Quasi-Digital Ultra-Fast Capacitor-Less Low-Dropout Regulator Based on Comparator Control for x8 Current Spike of PCRAM Systems”. In Proceedings of the 2018 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA, 18–22 June 2018; pp. 107–108. **[Google Scholar]**

[2] Y. Lu et al., "A fully-integrated low-dropout regulator with full-spectrum power supply rejection", IEEE Trans. Circuits Syst. I Reg. Papers, vol. 62, no. 3, pp. 707-716, Mar. 2015. **[Google Scholar]**

[3] Park, J.; Ko, W.-J.; Kang, D.-S.; Lee, Y.; Chun, J.-H. “An Output Capacitor-Less Low-Dropout Regulator with 0–100 mA Wide Load Current Range”. Energies 2019, 12, 211. **[Google Scholar]**

[4] Milliken R. J., Silva-Martinez J., Sanchez-Sinencio E, "Full On-Chip CMOS Low-Dropout Voltage Regulator," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 54, issue 9, pp. 1879-1890, September 2007. **[Google Scholar]**

[5] S.-W. Wang, Y.-J. Woo, S.-H. Bae, T.-H. Kong, G.-H. Cho and G.-H. Cho, "A high stability DC-DC boost converter with ripple current control and capacitor-free LDOs for AMOLED display", Proc. IEEE Asian Solid-State Circuits Conf., pp. 41-44, Nov. 2011. **[Google Scholar]**

[6] Z. Qianneng, W. Yongsheng and L. Fengchang, "A capacitor-free CMOS LDO Regulator with AC-boosting and active-feedback frequency compensation", J. Semicond., vol. 30, no. 4, pp. 1879-1890, Apr. 2009. **[Google Scholar]**

[7] F. Yang and P. K. Mok, “5.11 A 65nm inverter-based low-dropout regulator with rail-to-rail regulation and over −20dB PSR at 0.2V lowest supply voltage,” in Proc. ISSCC, San Francisco, CA, USA, Feb. 2017, pp. 106–107.

Slew Rate Enhancement

[8] B. H. Kassiri and M. J. Deen, "Slew-rate enhancement for a single-ended low-power two-stage amplifier", Proc. IEEE ISCAS, pp. 1829-1832, May 2013. **[Google Scholar]**

[9] K. Nagaraj, "CMOS amplifiers incorporating a novel slew rate enhancement technique", Proc. IEEE 1990 Custom Integrated Circuits Conf., pp. 11.6.1-11.6.5, May 1990. **[Google Scholar]**

Bandgap Reference

[10] Yannick Wenger, Bernd Meinerzhagen, “Low-Voltage Current and Voltage Reference Design Based on the MOSFET ZTC Effect,” IEEE Transactions on Circuits and Systems I: Regular Papers, Volume: 66,Issue: 9, Sept. 2019

[11] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, “A CMOS bandgap reference circuit with sub-1-V operation,” IEEE J. Solid-State Circuits, vol. 34, pp. 670–674, May 1999.

[12] M. Gunawan, G. Meijer, J. Fonderie and H. Huijsing, ”A Curvature-Corrected Low-Voltage Bandgap Reference”,IEEE J. Solid State Circuits, Vol. 28, pp. 667-670, June 1993.

[13] B. Razavi, Design of Analog CMOS Integrated Circuits. Boston, MA: McGraw-Hill, 2001.

[14] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 2nd ed. New York: Wiley, 1984.

[15] Hafiz, Shafiullah, Chowdhury , “Design of a Simple CMOS Bandgap Reference”, IJECS, Vol:10 No:05

[16] NASHIRU ALHASSAN, " Low Power, High PSR cmos voltage reference ," 2016 Thesis, Texas A&M University.

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