DESIGN OF SUB 1V CAPACITORLESS LOW DROPOUT REGULATOR IN 65NM TECHNOLOGY

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CERTIFICATE

This is to certify that the thesis titled "**Design of Sub 1V Capacitorless Low Dropout Regulator in 65nm Technology**" being submitted by **Robinson Devasia** to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

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ACKNOWLEDGEMENT

I would like to thank my guide Prof. G.S Visweswaran for his support and guidance throughout this project. The technical discussion which I had with him gave me a vision and a different perspective of problem solving that helped me with this project and will surely help me in future.

I would also like to thank my college friends for the constant motivation. I would take this opportunity to thank Sapna Sharma for all the brainstorming sessions and technical discussions that helped me in moving the project to its final form.

Last but not the least, I would like to extend my special thanks to my parents, Mr. Devasia P V and Mrs. Rosamma Joseph for their blessings and my sister Jasmine Devasia for her emotional support.

Contents

List Of Figures

List Of Tables

Abstract

In recent times there has been tremendous research in the field of bio-medical, particularly towards implantable medical devices. Implantable devices must be compact and have good battery life with stable supply voltage. For example, pacemaker must have a long battery life and should be provided a constant supply voltage. This creates a growing demand for low power low dropout regulators (LDO). LDOs are circuits which provide constant supply voltage even when the power supply is fluctuating. The limited headroom for low power analog LDO can be challenging while designing.

In this work, the error amplifier is designed using a folded cascode structure. The work also targets having low line regulation and load regulation for a wide range of voltage and current variations. This type of design helps in providing longer battery life to implantable devices.

In this dissertation, we propose Low power sub-1V capacitorless Low Dropout Regulator (LDO) on 65nm Technology. The max driving current is 10mA working at a temperature range of -40^{o}C to 125^{o}C with a low quiescent current consumption. This work achieves line regulation of $5.45\,{}^{mV}/_{V}$ and load regulation of $0.005\,{}^{mV}/_{mA}$ and consumes $5.64\mu W$ power.

Chapter 1
Introduction

This chapter contains the motivation, objective and outline of the thesis. In this work an LDO has been developed on 65nm technology at 0.75-0.95 supply voltage. Design steps, challenges and simulation results have been discussed in detail.

1.1 Motivation

With the growth of technology, the demand for electronic devices having multiple features has increased. The device sizes are reducing and technology is being scaled down. This leads to more stringent and challenging design specifications. The most crucial specification is power. To ensure longer battery life, the power consumption of the device must be minimized. Resource management can be a solution to improve battery life, but there is a limit to it. To further increase the battery life power management integrated circuit is required. Low Dropout Voltage Regulator (LDO) is one of the fundamental blocks of power management integrated circuits. It can provide a regulated output voltage at varying load impedance, input voltage, and temperature at any point in time with minimum dropout voltage. Voltage regulators can give a regulated supply even if the battery is discharged to a certain level. Voltage regulators should have lower power fluctuations, which arise due to crosstalk and circuit switching. The variations in the voltage should be within specification; otherwise, it may damage the rest of the circuit.

In handheld and bio-medical devices portability is a critical feature. For example, in devices like smart wearables, pacemaker, insulin pumps, portability is an important feature. Portability is directly linked to area hence the area should be minimum possible in these devices. Implantable devices are area stringent, so the off-chip capacitors which stabilize the output voltages are not present in these systems. These constraints make low power capacitorless LDO cardinal in biomedical applications.

The project aims at designing a low power, minimum area, high accuracy LDO for bio-medical applications. The LDO designed is capable of minimizing current consumption, which is essential if circuits are working in sleep mode. The design is simple and a compact structure makes it suitable for implantable devices in bio-medical applications.

1.2 Objectives

The main objective of this work is to design a Low power LDO voltage regulator at 65nm Technology that gives a regulated output voltage of 0.6V for all load conditions. Since this is a capacitorless LDO the allowed output load capacitance is 100pF. The load current specification is in the range of 0 to 10mA.

The supply voltage variation is from 0.75V to 0.95V and maximum current consumed by the circuit should be less than $7\mu A$ in all conditions. The targeted temperature variation is $-40^{o}C\ to\ 125^{o}C$ which is a military standard.

In this thesis, design of Sub 1V capacitorless low power LDO regulator with its associated trade-offs is presented.

1.3 Design considerations for LDO

There are three main considerations for VLSI design – Power, Performance, Area. There are various figures of merit for Voltage regulators which directly impact these parameters.

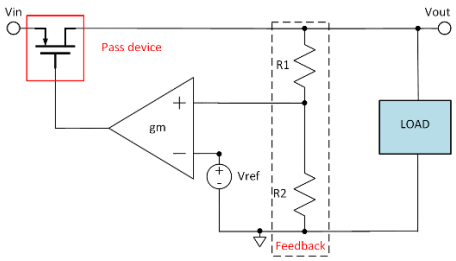

Figure 1 LDO general structure

This regulator is a low dropout regulator that means the pass transistor should have a low voltage dropout voltage across it as shown in figure 1. If we can reduce the dropout voltage across the pass transistor, we can reduce the power consumption. Another way is to reduce the difference in input current and output current which is a figure of merit for LDO. The current consumed by internal circuitry (quiescent current) should be minimum.

Stability is another parameter considered for design of voltage regulator. The phase margin of a regulator should remain in specified range for all the load conditions and supply variations. Line regulation defined as the percentage change in the output

voltage with supply voltage variation and Load regulation defined as the percentage variation in the output voltage with load variations are also figures of merit affected by stability. Bandwidth is another parameter considered while designing a voltage regulator. Bandwidth determines as to how quickly the circuit can respond to the input voltage changes to maintain a regulated output voltage. There is a trade off in the speed of response and the power consumption so we need to find spot which meets our specification maintaining the required speed of response.

Reducing the area is crucial for the portability of a device. If the area of the voltage regulator is small then we can use multiple regulators on the System on Chip (SoC). Multiple regulators on the same chip can help in incorporating voltage islands which can help in power reduction also. If multiple devices can be made onto same wafer, we can reduce the cost of manufacturing.

1.4 Outline

The rest of the thesis is organized as follows. Chapter 2 discusses the literature survey, LDO theory, its architecture and various parameter. Chapter 3 discusses in detail the design of LDO on 65nm technology, design approach, design challenges and its solutions. Chapter 4 gives the simulation results of the LDO designed. Chapter 5 concludes the presented work and also talks about the future work.

Chapter 2
Low Dropout Voltage Regulators

2.1 Fundamentals

Voltage regulators act as constant voltage source. The changes in load resistance is regulated by adjusting the internal resistance to maintain a regulated output.

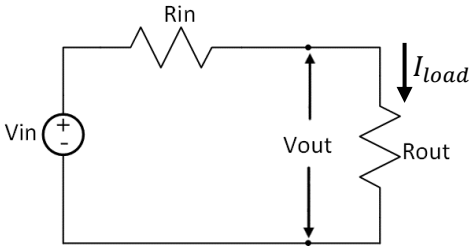

Figure 2 Voltage Source

In figure 6, V_{in} is the voltage source with R_{in} as the input resistance. R_{out} is the load impedance. Input impedance should be small so even if the load impedance or the load current (normally referred to as load) changes the output voltage remains constant.

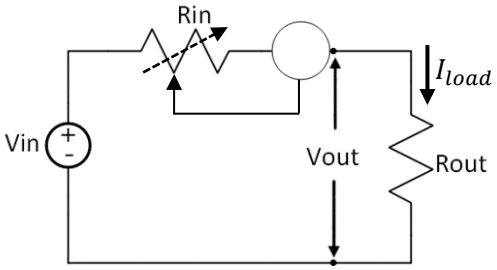

Figure 3 Regulator with feedback

Figure 7 represents a circuit where the input resistance can be changed as the load current changes. A feedback circuit is deployed to ensure that the output voltage is regulated. The relation between input impedance and output impedance of figure 7 is linear and can be expressed as $Rin = K \times Rout$.

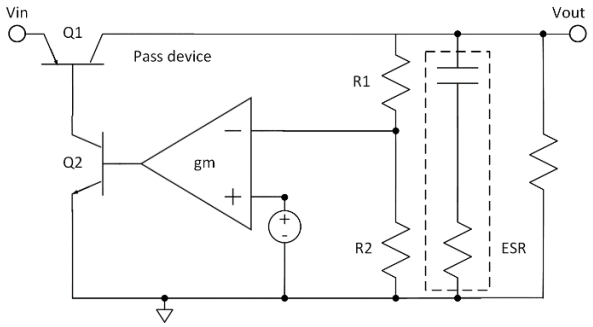

Figure 4 Traditional Linear Regulator

Figure 8 shows the traditional Linear regulator. In the early stages when linear regulators came into picture, they were designed using PNP or NPN bipolar transistor as pass device. As the demand for lower voltages and lower power needs became prominent, bipolar transistors were replaced by MOSFETs. Another reason for replacing bipolar transistors is that the base current in bipolar is proportional to load current. The dependency of load current on base current is undesirable. There is a trade-off associated with dropout voltage and current consumption in bipolar transistors.

2.2 System Architecture

Low Dropout Voltage Regulator, as the name suggest is a linear voltage regulator which has small dropout voltage. The difference between the input and output voltage is very small compared to traditional voltage regulator (Figure 8).

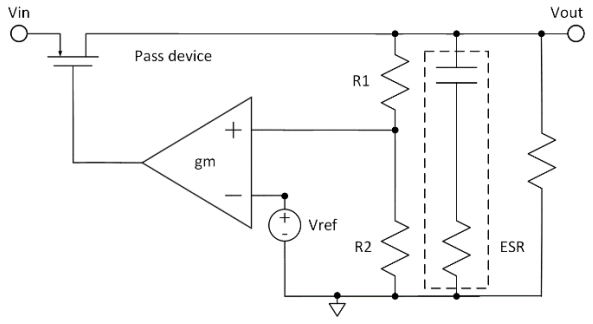

Figure 5 MOSFET based LDO

Figure 9 shows the basic structure of MOSFET based linear regulator. In this structure there is no base current. The current in the load flows based on the voltage at the gate of the MOSFET. The topology contains the error amplifier, pass element and feedback network. The feedback network provides scaled version of output voltage which is equal to reference voltage in nominal condition. The error amplifier continuously

compares both the voltage and amplifies the difference which is then fed into the pass element. The pass element keeps the output voltage regulated.

2.2.1 Error Amplifier

Error Amplifier is an important part of the LDO. This contributes the most to the power consumption. We should design to ensure that the internal branches consume minimum current. This will make sure that the current drawn from the input is as low as possible so the overall quiescent current will be low. There is a tradeoff between the current consumption and the performance of the circuit. The loop gain and the slew rate get impacted due to lowering the current. The gate capacitance of the pass element is large so the output impedance of the error amplifier should be slow. If the slew rate of the error amplifier is low, then it won't be able to charge the gate capacitance of the pass element. This is another trade-off. The DC loop gain should remain high for all the changing load conditions, this will help in improving accuracy in the voltage regulator. The bandwidth of the error amplifier should also be as high as possible as this will increase the speed of response of the regulator.

The error amplifier takes the scaled version of the output voltage and compares it with the reference voltage. It provides an error signal which is given to the input of the pass element. The impedance of the pass element changes such that the error signal can be brought to as close to zero as possible.

$$V_{fb} = V_{out} \frac{R2}{R1 + R2}$$

V_{fb} is the scaled down error signal. From the figure 4 we can write the error voltage.

$$V_{err} = V_{fb} - V_{ref}$$

If $V_{fb} = V_{ref}$ then,

$$V_{out} = V_{ref} \left(1 + \frac{R1}{R2}\right)$$

This shows that output voltage is the amplified version of the reference voltage.

2.2.2 Pass Element

The pass element drives a large current in full load condition and only quiescent current in no load condition. The advantages and disadvantages of using a PMOS or NMOS as pass element is discussed.

NMOS as pass element gives a source follower at the output which causes lower output impedance. This helps in improving the stability of the circuit. The disadvantage of using an NMOS based pass element is that the gate voltage should be higher than the output voltage which can be challenging in low power design. The solution to this problem is use of charge pump in the design.

PMOS can also be used as pass element. Since the source is directly connected to the supply, the voltage required at the gate of the pass element will be low. So, at lower voltage we can drive the pass element into saturation. The disadvantage of using PMOS as pass element is that there is a limit to lowering the input voltage. After a specific voltage the pass element will go into triode region which will degrade the open loop gain and accuracy. Certain amount of dropout voltage is necessary for PMOS pass element unlike NMOS where this voltage depends on the value on the gate voltage.

2.2.3 Feedback Network

Feedback network gives scaled version of the output voltage to the error amplifier. One can use a MOSFET based divider circuit because of the area density. Channel length needs to be large to get large output resistance but the parasitic capacitance will also increase. Resistive feedback is another feedback method. This can help in achieving low current consumption and lower parasitic capacitance but the area consumed will be more than MOSFET based feedback network.

In a feedback network, based on the impedance value we can decide the quiescent current. The impedance value of the feedback network can be decided on the basis of the design specifications.

2.3 LDO Parameters

This section discusses the basic LDO parameters.

2.3.1 Dropout Voltage

At a minimum input voltage, the voltage regulator ceases to regulate the output voltage. The voltage drop across the pass element at this instant is described as dropout

voltage. The voltage received after the dropout will be the output voltage. To prevent the pass transistor from going into triode region, the minimum input voltage limit must be set. The circuit also needs a certain amount of voltage to give high gain. The input voltage is limited by the headroom requirement of the circuit. If we go beyond that the gain of the circuit will start to deteriorate and ultimately the performance. The circuit cease to perform the way it was intended to perform.

2.3.2 Quiescent Current

The current consumed by the internal circuit, blocks and sub-blocks contribute to quiescent current. The quiescent current is defined as the difference between the input and output current.

$$I_Q = I_i - I_o$$

I_Q is the quiescent current, I_i is the input current and I_o is the output current.

Low quiescent current will increase the efficiency of the circuit. The power consumption is also decided by the value of quiescent current. This is also linked with the performance of the circuit. It can be difficult to increase speed of response with low quiescent current so we need to find the intermediate level which helps to meet our specification.

2.3.3 Line Regulation

Line regulation is the change in output voltage with respect to the change in input voltage.

$$Line\ Regulation = \frac{\Delta V_o}{\Delta V_i}\ {}^{mV}/_{V}$$

Line regulation tells the behavior of output voltage with the change in the input voltage. To improve line regulation, the loop gain of the circuit should be high. We cannot go on increasing the loop gain as this will impact the stability of the circuit.

2.3.4 Load Regulation

Load regulation is the change in the output voltage with respect to the change in the input current.

$$Load\ Regulation = \frac{\Delta V_o}{\Delta I_o}\ {}^{mV}/_{mA}$$

Load regulation gives the insight on the behavior of output voltage with increasing load currents.

$$Load\ Regulation = \frac{r_o}{1 + A_o}$$

In the above equation r_o is output impedance of circuit and A_o is loop gain of circuit. It can be seen that to improve the load regulation we need to increase the gain of the circuit. As discussed in latter section the stability is impacted at very high gain.

2.3.5 Figure of Merit (FOM)

For the purpose of comparison with the work done by other researchers in LDO regulator a figure of merit is defined. This is widely accepted by researchers across the world.

$$FOM = T_R \frac{I_Q}{I_{max}}\ [ps]$$

Where, I_Q is quiescent current, I_{max} is maximum load current and T_R is response time.

$$T_R = \frac{C * \Delta V_{out}}{I_{max}}$$

Where, C is load capacitance and ΔV_{out} is maximum load transient glitches at the output.

2.4 Literature Survey

The thesis focuses on the design of low power low dropout voltage regulator. LDO being one of the important blocks of any system, has attracted many researchers. There are numerous approaches to LDO design, some of which are discussed in this section.

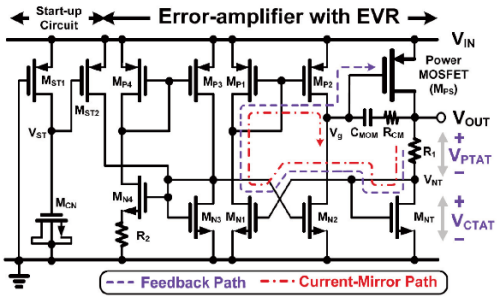

Figure 6 LDO with embedded voltage reference [1]

Chen and Su [1] used an innovative way to implement LDO with an embedded voltage reference in $21nm$ technology. The design is a simple differential structure with current feedback. Owing to the simple design structure, the design is able to achieve an undershoot of $10\ mV$. The feedback also acts as the voltage reference where a diode-connected transistor M_{NT} is used to get CTAT voltage and resistor R_1 to get PTAT voltage as shown in figure 2. The disadvantage of this design is that the loop gain of the circuit is low because of which we can see an impact on the line and load regulation. The area of this design is more which is another disadvantage.

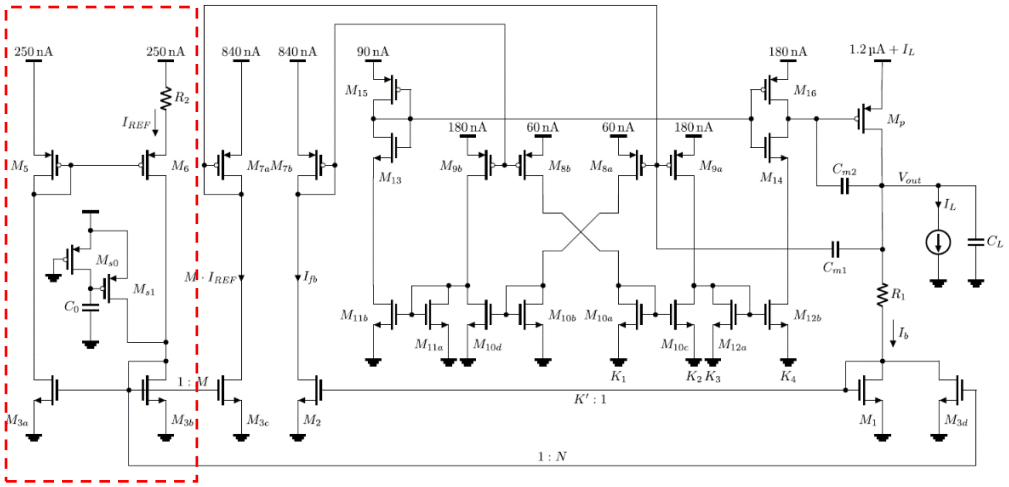

Figure 7 Current Feedback based LDO by [2]

Wang and Mirabbasi [2] implemented current feedback based LDO. The design uses a two-stage differential amplifier with a current feedback. The current feedback topology alleviates the issues of low voltage headroom. It decouples the relation between the DC loop gain and the output voltage by subtracting a portion of DC current from the main feedback path [2]. This helped them to get lower power consumption and increased loop gain for given output voltage. The design uses two compensation capacitors C_{m1} and C_{m2} for improving the stability of the circuit as shown in figure 3. For a $130nm$ process, the current consumption is small but the line and load regulation is impacted. The speed of response is low. The undershoot in this design is more than $100mV$ when the current change is $3mA$.

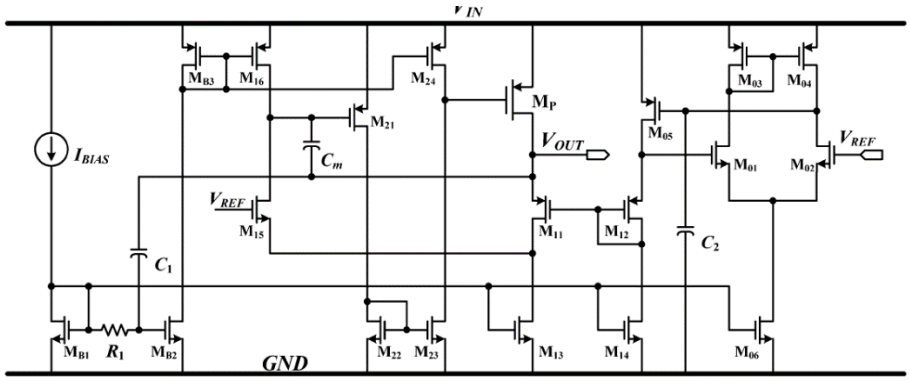

Figure 8 Flipped Voltage follower based LDO [3]

Guo and Leung [3] implemented an output capacitorless LDO which is originated from a flipped voltage follower (FVF) based structure. FVF is an evolution of classical common-drain amplifier, also known as voltage follower. This is implemented in $90nm$ process technology. They introduced a non-inverting gain stage between the pass element M_p and the error amplifier which has improved the line and load regulation. The error amplifier is formed by common gate differential pair (M_{11}-M_{16}) and non-inverting stage (M_{21}-M_{24}) as shown in figure 4. The non-inverting stage helps to improve the loop gain and increase the dynamic range of the structure at gate of M_p [3]. This innovative design can drive up to $100mA$ of load current. The disadvantage of this design is the higher quiescent current which is up to $8\mu A$.

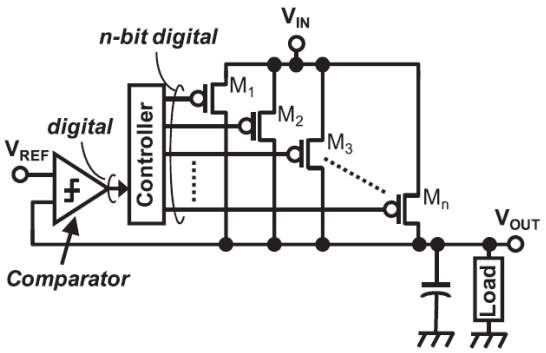

Figure 9 Schematic of Digital LDO [5]

Okuma and Ishida [5] implemented a digital LDO. The design comprises of a clocked comparator, shift register, and a switch array as shown in figure 5. The author has implemented the circuit at a very low supply voltage of $0.5V$ [5]. At this voltage it is difficult for the analog voltages to drive the pass transistors so digital LDO implemented by author [5]. The analog control is replaced by switch array, comparator and a controller. This helps in operating the pass transistors at supply voltage. The overall quiescent current consumption is $2.7\mu A$ which is low. This design uses an off-chip decoupling capacitor. Since it is not a capacitorless design,

it has an impact on the area. The maximum load current this design can drive is $200\mu A$ which is small. A capacitorless design with small area is a better alternative as it allows the block to be used multiple times for driving different blocks in an IC. If we increase the maximum load current drivability then we can drive more circuits with same LDO.

Chapter 3
LDO Design

Specification

Output Voltage 0.6V

Input Voltage from 0.75V to 0.95V

Output Capacitance Range 0 to 100pF (Since its Capacitorless)

Max Driving Current Upto 10mA

Temperature Range -40^{o}C to 125^{o}C

3.1 Design Approach

The thesis finds its application in biomedical field so specifications are decided based on it. The initial thought that comes to mind is the accuracy of result will play a crucial role. Along with that power and area is also important. Line and load regulation are a figure of merit in LDO for accuracy. To improve this, we require high gain in the circuit. Simple differential structure cannot provide very high gain. Telescopic cascode and folded cascode can be candidates for a higher gain structure.

Telescopic cascode tend to have high transistor stacking which can be a bane for low power design because of lower voltage headroom. The output swing offered by telescopic cascode is lower than the folded cascode. So, because of these reasons folded cascode structure was chosen for the LDO design.

Since the specification targets low supply voltage only a folded cascode structure cannot match with the required accuracy. So, improved Wilson current mirror was introduced in the structure. It helps to get high output impedance which help in further increasing the gain. An added advantage is that it eliminates systematic gain error. These measures were not enough so a second stage of push-pull inverting amplifier stage was introduced to get high gain at such low supply voltage. To improve the stability of the circuit miller compensation was introduced in the circuit. Pass element also contributes to the gain of the LDO. The pass element design is discussed in the later section.

3.2 Architecture

The LDO consists of an error amplifier, feedback circuit and a pass element. Each of these are discussed below.

3.2.1 Voltage Divider

Resistive feedback network was chosen for the design. This helps in achieving lower quiescent current. The parasitic capacitance is also small. In the voltage divider, we need to think about voltage divisions based on the resistor ratio.

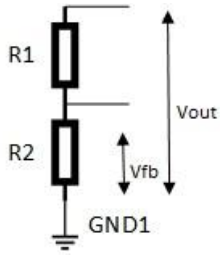

Figure 10 Voltage Divider

The feedback voltage is intentionally kept low to incorporate a lower reference voltage. Now we need to define a feedback factor β which is $\frac{Vfb}{Vout}$. The output voltage is 0.6V and the feedback voltage is 120mV.

$$\beta = \frac{Vfb}{Vout} = \frac{R2}{R2 + R1} = 0.2$$

The resistor ratios are defined now. We need to define the current consumption which will help in getting the absolute value of the resistors.

3.2.2 Pass element Design

The input/Supply voltage varies from 0.75V to 0.95V and the output voltage is defined at 0.6V. From this information, we can derive that the minimum dropout voltage to be 150mV and the maximum dropout voltage is 350mV.

Pass element can be PMOS or NMOS, PMOS requires lower input voltage for it to stay in saturation region compared to NMOS. So, considering the low power requirements it is logical to choose PMOS as a pass element. In the case of NMOS, if we want to work at lower voltage, extra circuitry is required which will further complicate the design.

The square law equation can be used to design the size of pass element. The equation is as followed.

$$\frac{W}{L} = \frac{I_D}{\frac{1}{2}\mu C_{ox}\,(V_{GS} - V_{TH})^2}$$

Since the current change in pass element is large there can be large change at the process corners. Solution would be to use larger $\frac{W}{L}$ ratio to reduce the process variations. Larger $\frac{W}{L}$ ratio will lead to larger gate capacitance which will demand a high-speed error amplifier if we need a lower undershoot and overshoot.

3.2.3 Error Amplifier

Initial design decision that we need to take is the topology of error amplifier. The constraints of the pass element need to be taken into consideration while designing error amplifier. The goal is to design an error amplifier which works at low quiescent current. The bias should remain stable under all the load current and input voltage conditions. To achieve a better accuracy the gain should be as high as possible so the architecture of the error amplifier also plays a major in the design process.

- **Differential pair selection**

  In an NMOS differential pair we need higher bias voltage for it to stay in saturation. Since this particular LDO is for biomedical applications low power is a crucial specification. The reference voltage for the LDO is decided to be 120mV, so NMOS based differential pair is not a suitable choice for the design.

  PMOS based differential pair is a good option for low power application as the input bias required to keep the transistor in saturation is low. One of the significant advantages that comes with the PMOS differential pair is low noise, which can be a crucial parameter for low power applications.

- **Error Amplifier Topology**

  The Amplifier topology is crucial for LDO design. If we choose differential amplifier topology, then we won't get enough GBW at low voltage. Similarly, if a Cascode amplifier is selected, then the swing will be limited. So, the topology for this low power design chosen is a two-stage PMOS based folded cascode amplifier. We have to ensure that this amplifier topology should be able to drive the buffer and thus the pass transistor for a wide range of load currents.

3.3 Final Design

In this section we will see more into the proposed LDO. The variation in the parameters can influence stability and bias conditions of the LDO. The final schematic is shown in the figure 11.

All the PMOS's substrate is connected to the Supply and all the NMOS's substrate are connected to the ground. M4, M5, M18, M19 transistors are mirror transistors which help in proper mirroring of current in both the branches. The second stage of the error amplifier is a push-pull amplifier (M31, M20) with PMOS mirror (M35) on top of it which helps in limiting the current. The target is to keep the total current consumption be less than $7\mu A$. At low power the current matching is a challenging task so larger length devices will be required when designing current mirrors. The trade-off that comes here is that the output resistance will increase which will reduce the stability of the circuit. We need to keep in mind while designing. Miller compensation is used in this circuit to improve the stability of the circuit. The reference voltage is coming from an ideal source.

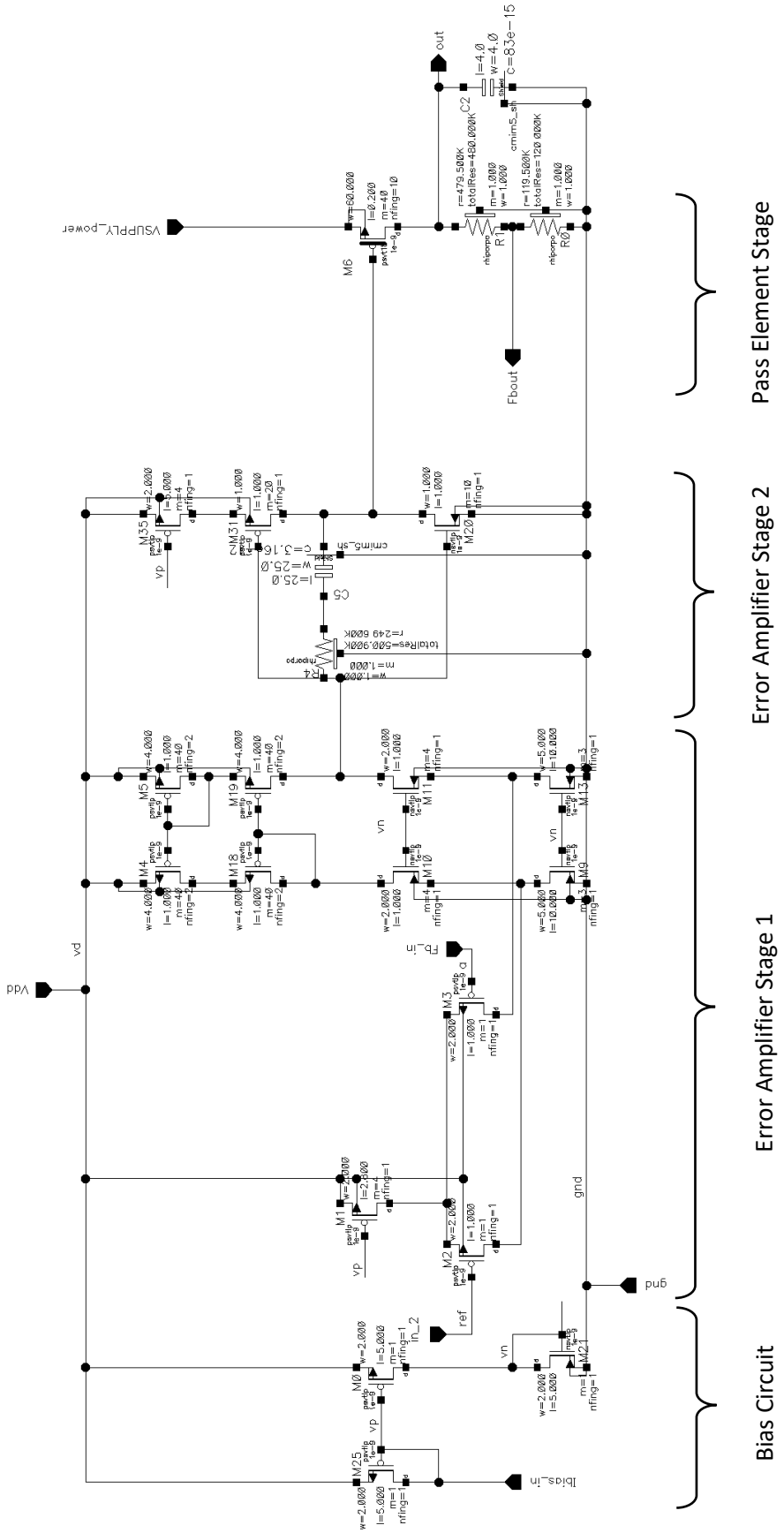

Figure 11 LDO Schematic Diagram

3.4 Design Challenges and its solutions

The challenges faced and the methods to solve them while designing the LDO are discussed in the section below. This section covers the challenges in terms of figures of merit and the choice of elements that is best fit considering the design.

3.4.1 Upper limit on gain due to output impedance limitation

While designing the LDO circuit we need to push the second pole beyond the unity gain bandwidth to get sufficient phase margin. This helps in getting stability in the circuit.

$$Second\ pole > Unity\ gain\ bandwidth$$

This puts a constraint of upper limit on the output impedance of the error amplifier. So, there is a limit to which we can increase the output impedance because it may degrade the stability of the circuit.

3.4.2 Loop gain characteristics

Getting a high loop gain for good line and load regulation was another challenge. The problem here is the upper limit on the output impedance which was discussed in the previous section. If output impedance is limited so is the gain as it is directly proportional to gain. Another method could be to increase the transconductance of the amplifier. The tradeoff here would the quiescent current. The transconductance (g_m) is directly proportional to current consumed. If we increase the g_m in the circuit it will also increase the current. Solution would be to squeeze out maximum g_m for a particular current consumption. Finding the sweet spot is be the key here.

3.4.3 Speed of response

The speed of circuit is directly proportional to the unity gain bandwidth. The gain bandwidth product of an amplifier remains constant. So, if the gain increases the bandwidth will reduce. Similarly, if we increase the bandwidth the gain will reduce. The tradeoff will exist here. Solution would be to achieve enough gain while maintaining the bandwidth number so as to get both the desired accuracy and good speed of response.

Another method could be to reduce the size of the pass element. This will reduce the load capacitance seen by the error amplifier. This will ensure that for the same quiescent current we get more speed of response. This will put a limit to the maximum

current the pass element can drive. So, there is a tradeoff between speed of response and maximum current through pass element. One solution to this problem is that we find out the worst-case current requirement of pass transistor and size it considering the worst case. This way the size of the pass transistor will be in check while maintain the current requirement. Another solution is to use pass element with larger charge density can also be used. It can drive more current for smaller size compared to a normal pass element. Type of transistor used for the pass element can also play a good role in speed of response.

3.4.4 Choice of capacitance for miller compensation

MOSFET can be used as a capacitor if source, drain and substrate is tied together.

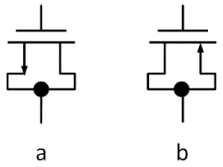

Figure 12 MOS capacitor (a) NMOS capacitor (b) PMOS capacitor

Figure 12 shows the structure of a capacitor using MOS transistors. The benefit of using a MOS capacitor is area density. However, the noise and variations of such capacitors are quite high. Another capacitor is MIM (Metal-Insulator-Metal) capacitor. MIM capacitors have less variations. To tackle the noise a shielded MIM capacitor is used. An experiment was carried out to test the effect of both types of capacitors. MIM capacitors outperformed MOS capacitors in terms of performance when both of them had equal area. To improve the performance of MOS capacitor area was increased. The increase in area of MOS capacitor to get same performance as MIM capacitor was too large. Hence considering the performance and area, MIM capacitor was chosen for the design.

3.4.5 Choice of resistance

We have multiple types of resistors in our 65nm technology. Metal resistors can provide small resistance of few ohms per μm length. This type of resistors is beneficial when we need very small resistance. Poly resistors are another type of resistors. There can be silicided/unsilicided, N+/P+ type of poly resistors which can go up-to few kilo ohms per μm length. For our case the resistance required is in range of ~100 kilo ohms for low quiescent current. There is a special resistor known as highly resistive poly

resistor which can give resistance of this range with only few μm of length. So, to save area this was chosen in the design.

3.4.6 Choice of transistor

There are mainly three types of transistors to choose from, low V_t low power (lvtlp), standard V_t low power (svtlp) and High V_t low power (hvtlp). Here V_t is referred to threshold voltage of transistor.

lvtlp transistor can help to increase the speed of the circuit as it turns on faster compared to other transistors. However, the leakage I such transistors is larger than the other transistors. hvtlp transistor can help in reducing the leakage in the circuit but this will turn on slowly as compared to other transistors. svtlp has sweet spot between the leakage and the turn on so, we can take advantage of both the characteristics in this type transistor. svtlp was chosen for the design of the LDO circuit.

Chapter 4
Simulation Results

This chapter contains the simulation results of the LDO. The circuit simulated for AC, DC and transient parameters. Figure of merits are calculated across different corners.

4.1 AC Simulations

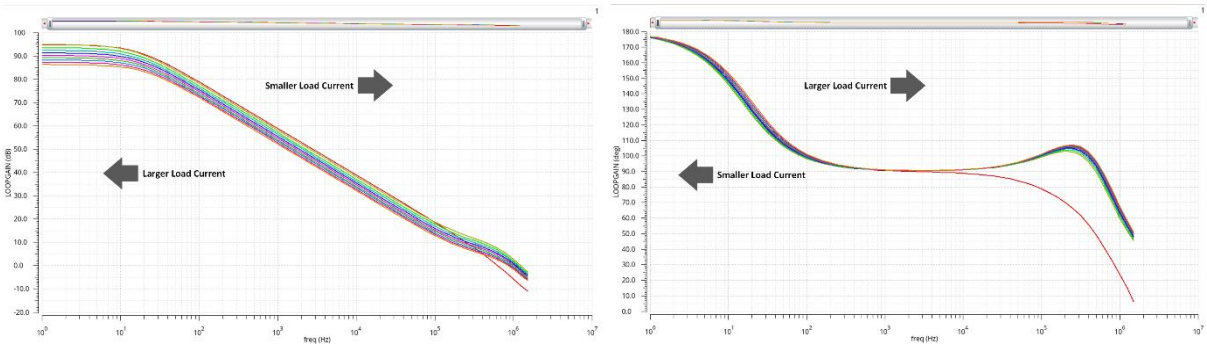

Figure 13 Change in gain and phase with increasing load current

In Figure 13 the loop gain graph shows that with the increase in the load current the gain of the circuit will reduce and phase will increase vice-versa effect can be seen if load current reduces. The supply voltage at this time is 0.75V.

4.2 DC Simulations

Load regulation and Line regulation for the nominal and worst case (FS) is shown.

4.2.1 Line Regulation

It is the ability of regulator to maintain desired output voltage with varying input voltage.

It is the change in output voltage with respect to the supply voltage.

$$Line\ Regulation = \frac{\Delta V_o}{\Delta V_i}$$

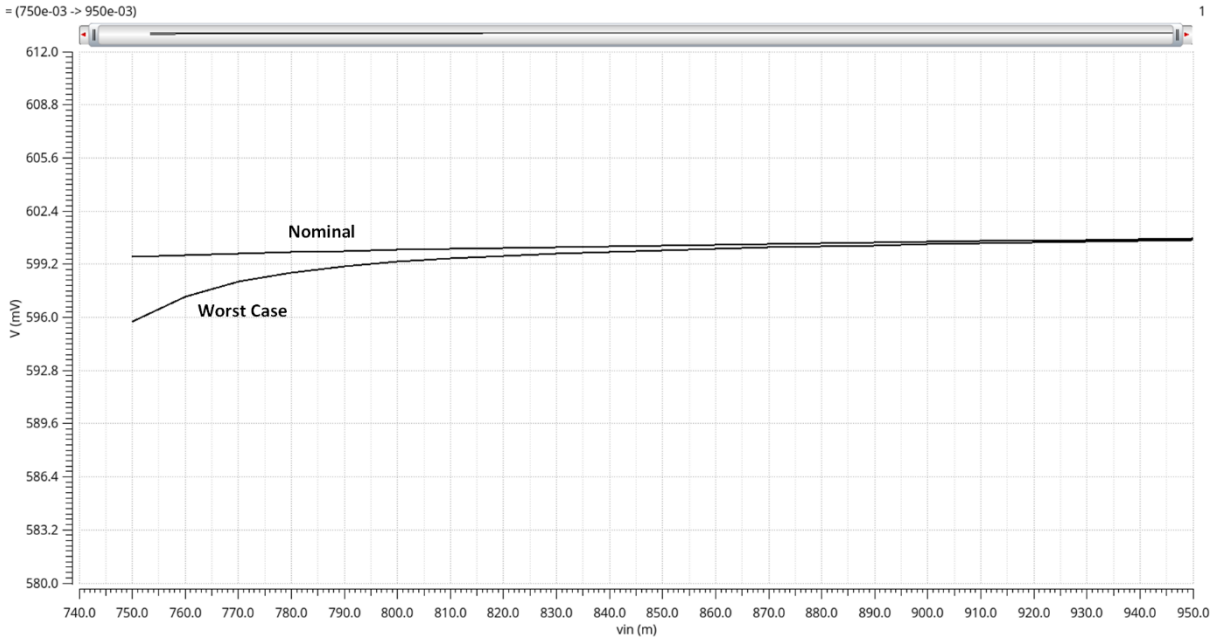

Figure 14 Line Regulation for nominal and worst corner

The graph shows that the line regulation in nominal case is 5.45 $^{mV}/_{V}$ and in the worst-case corner is 24.46 $^{mV}/_{V}$.

4.2.2 **Load Regulation**

Load regulation is the ability of the regulator to maintain the regulated output voltage with varying load currents. Since the amplifier is non-ideal, the loop gain of the circuit is finite. Hence, the regulator cannot entirely cancel the effect of changing load current.

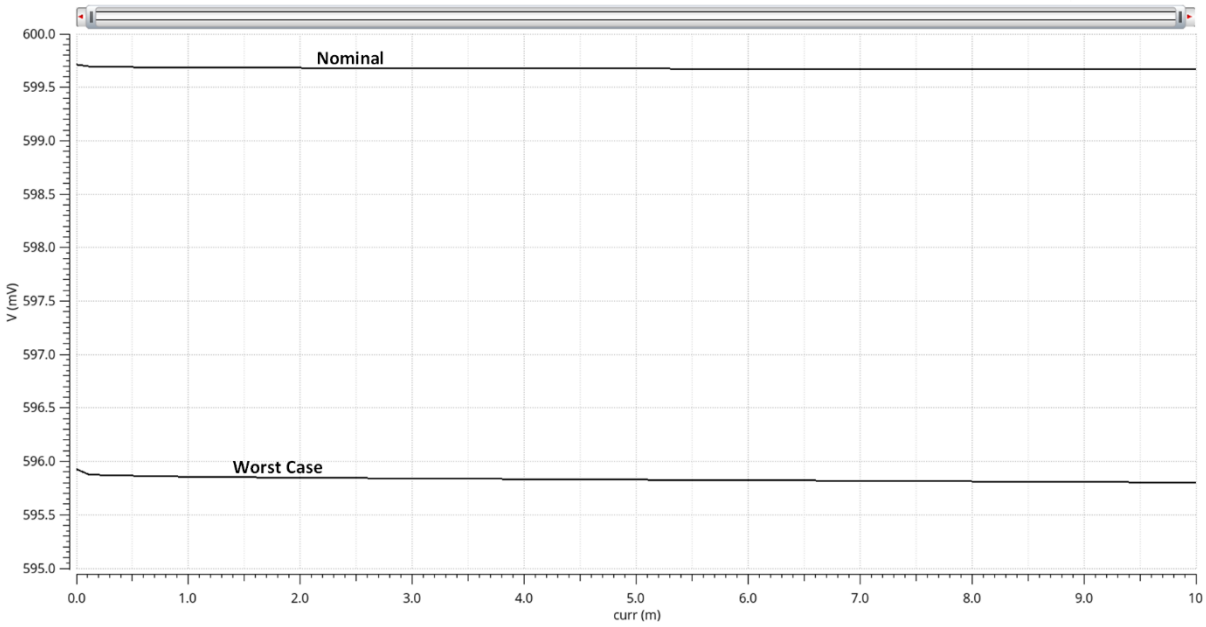

Figure 15 Load Regulation for nominal and worst corner

$$Load\ Regulation = \frac{\Delta V_o}{\Delta I_o}$$

The graph shows that the load regulation in nominal case is 0.005 $^{mV}/_{mA}$ and in the worst-case corner is 0.012 $^{mV}/_{mA}$.

4.2.3 Temperature Variation

Temperature variation is an important parameter to judge the change in output voltage with respect to the change in temperature. We know that the ambient temperature can vary based on the application.

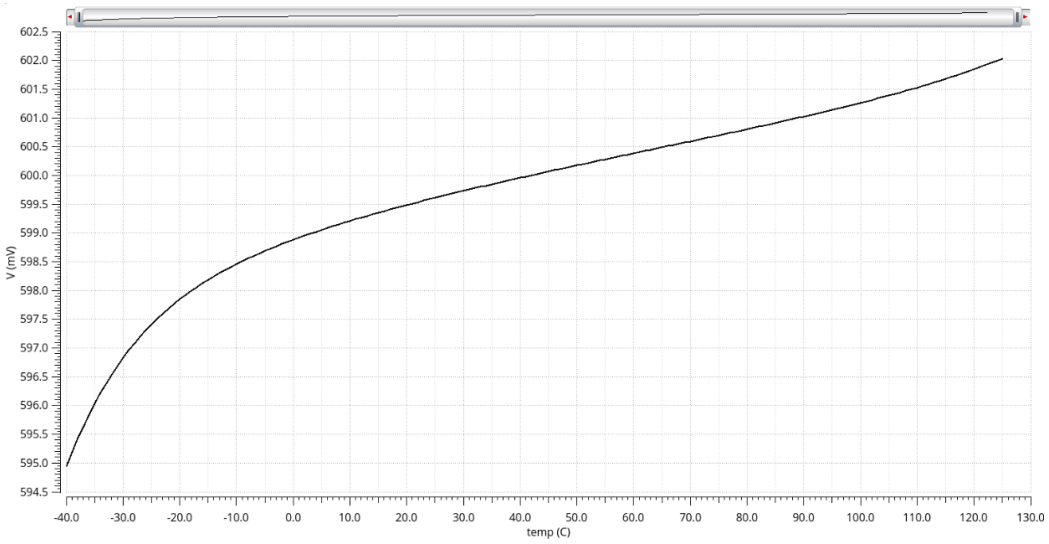

Figure 16 Output Voltage variation with temperature

4.3 Transient Simulations

It shows the real-time behavior of the circuit with the changing load currents.

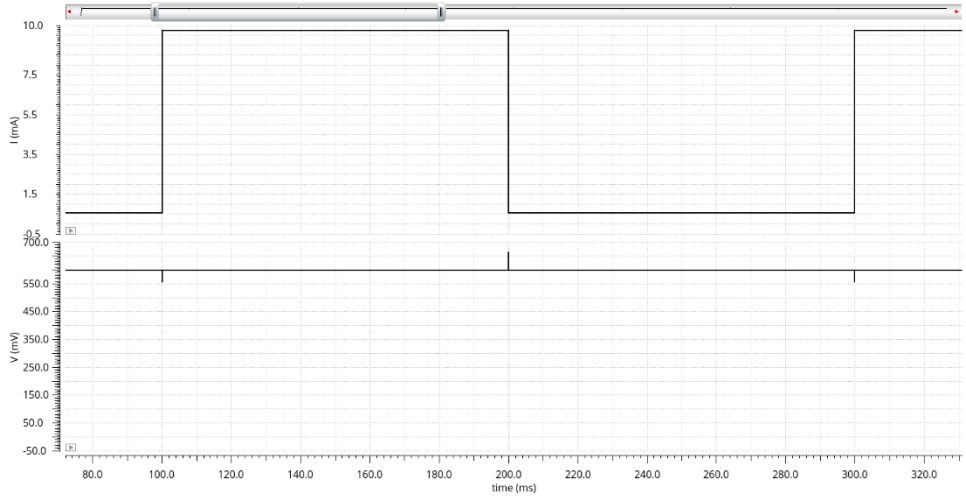

Figure 17 Transient Response of output voltage with load current

The undershoot for the nominal simulation is 41.30 mV and overshoot is 64.18 mV at supply voltage of 0.75V.

4.4 Corner Analysis

This is the last step in the analysis. The circuit is simulated and analyzed at the process corners. The change in figures of merit with the change in process corners are recorded in the below table.

Table 1 Figure of merits across different corners

	TT		SS		FF		SF		FS		Unit
Supply Voltage	0.75	0.95	0.75	0.95	0.75	0.95	0.75	0.95	0.75	0.95	V
Supply Current	5.94	5.94	4.76	5.78	5.57	6.10	5.23	5.95	5.11	5.94	uA
Output Voltage	599.7	600.8	597.7	600.3	600.4	601.2	600.1	600.8	595.8	600.7	mV
Output Capacitor	<100										pF
Load Range	0~10										mA
Line Regulation	5.45		13.03		3.90		3.37		24.46		mV/V
Load Regulation	0.005	0.003	0.006	0.003	0.005	0.005	0.003	0.003	0.012	0.004	mV/mA
Undershoot	41.30	44.97	47.74	50.33	38.42	40.95	43.18	45.78	46.15	45.70	mV
Overshoot	64.18	67.93	71.89	73.67	59.67	62.60	63.75	67.89	70.9	69.90	mV
PM	74.63	52.75	76.81	52.52	77.04	52.61	72.71	51.48	80.75	53.85	degree
Temp. Var (%)	1.18	0.47	8.39	0.43	0.8	0.76	0.57	0.57	14.17	0.78	%

Many iterations were performed across the corners to improve the figures of merit. The improved results are then recorded in the table 1 as a conclusion.

Chapter 5
Post Layout Simulations

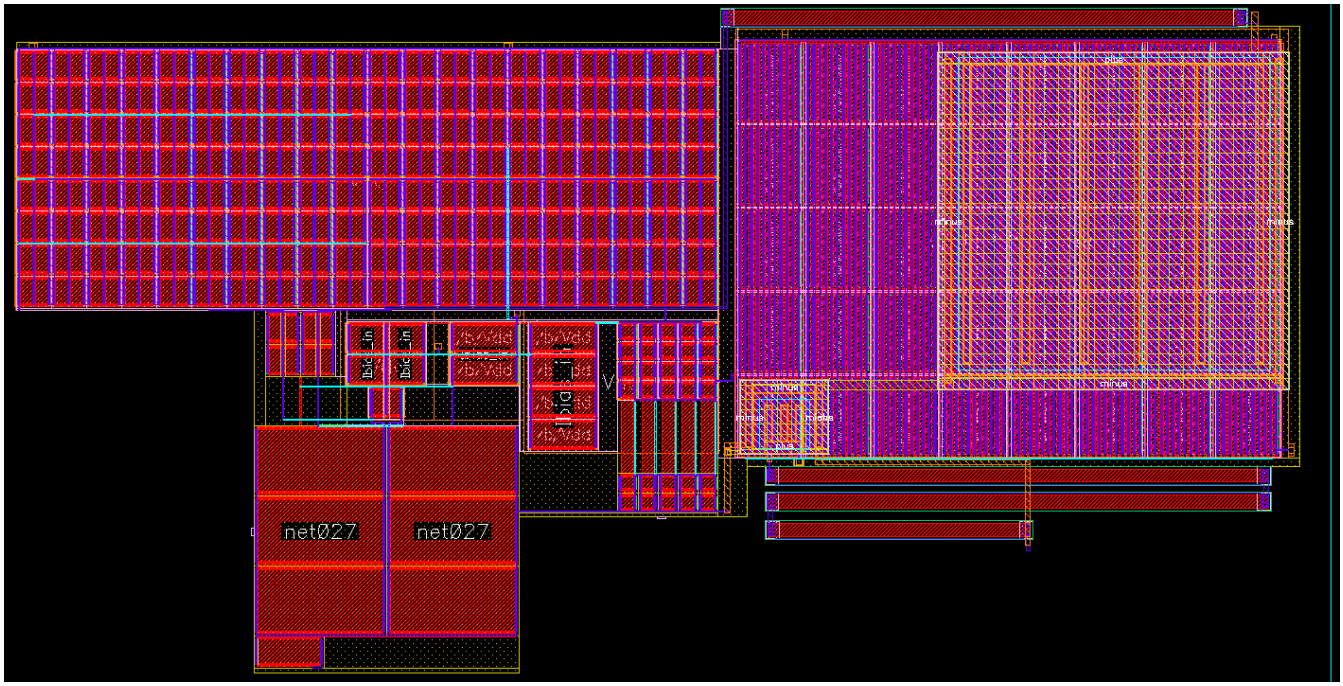

Figure 18 LDO Layout Design

Figure 18 shows the layout diagram of the LDO. Post layout simulations and its comparison with the pre layout is given in below sections.

5.1 AC Simulations

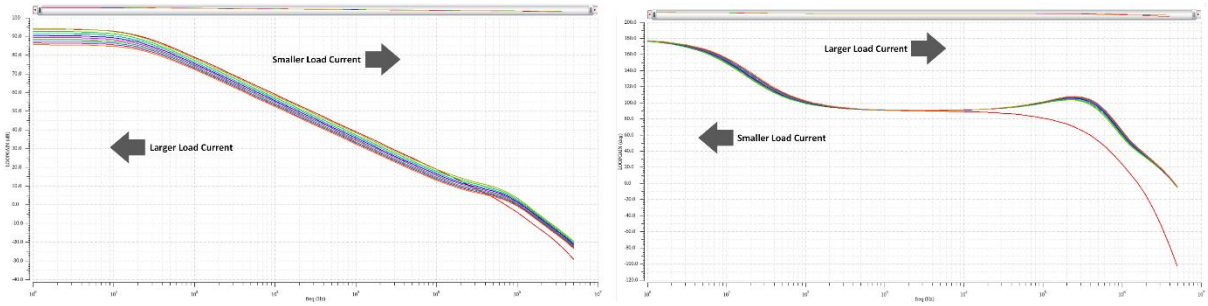

Figure 19 Change in gain and phase with increasing load current post layout

5.2 DC Simulations

Load and line regulation for pre and post layout simulations is shown.

5.2.1 Line Regulation

From the figure we can conclude that there is a 19.3% degradation in the line regulation compared to the pre-layout simulations.

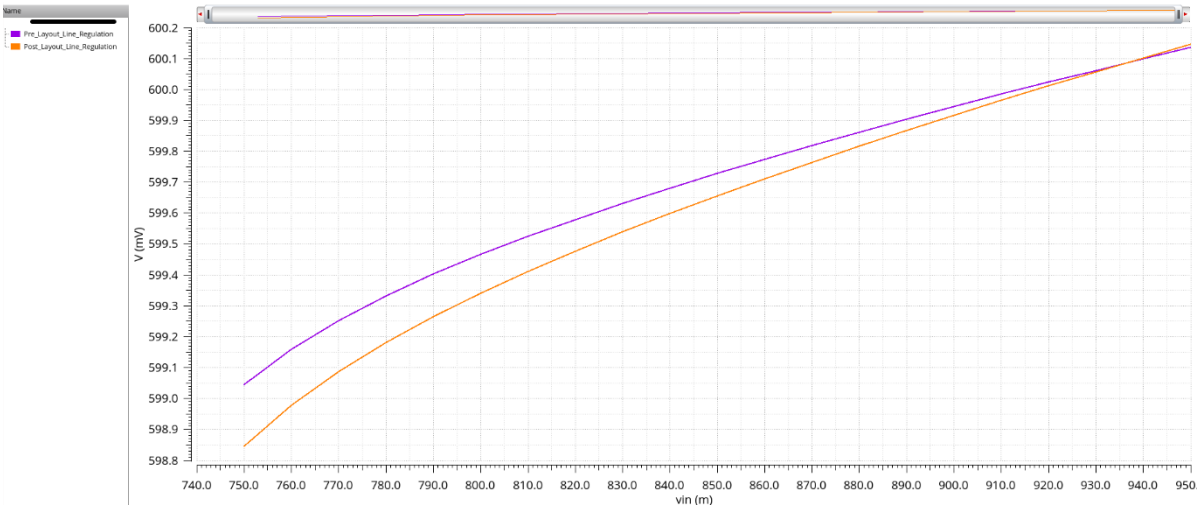

Figure 20 Line Regulation for Pre and Post Layout Simulations

5.2.2 Load Regulation

From the figure we can conclude that the load regulation has improved by 44% at 0.75V of input voltage compared to pre-layout simulations.

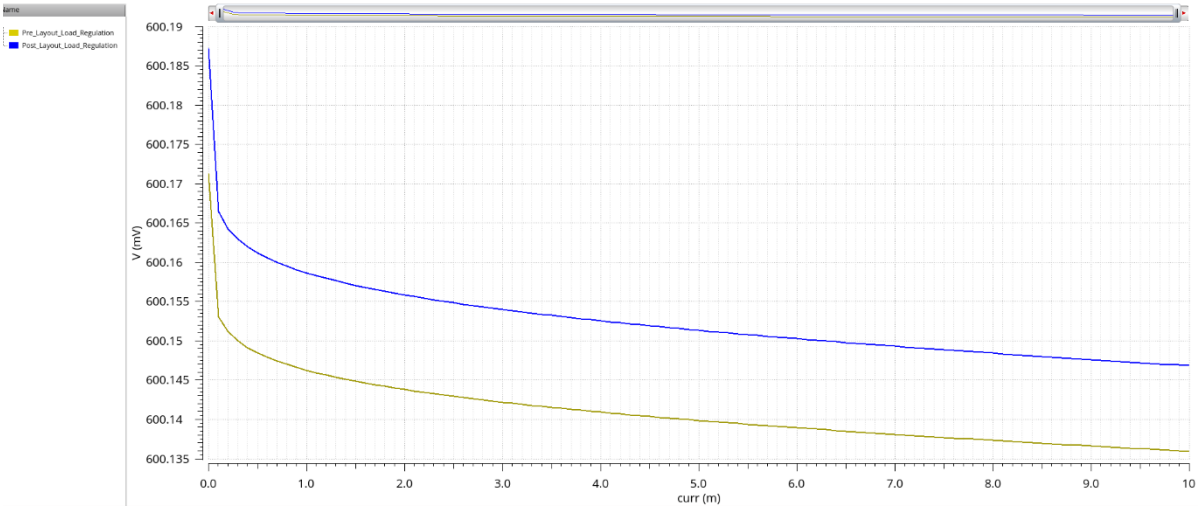

Figure 21 Load Regulation for Pre and Post Layout Simulations

5.2.3 Temperature Variation

From the below figure we can see that there is a degradation in the temperature variations

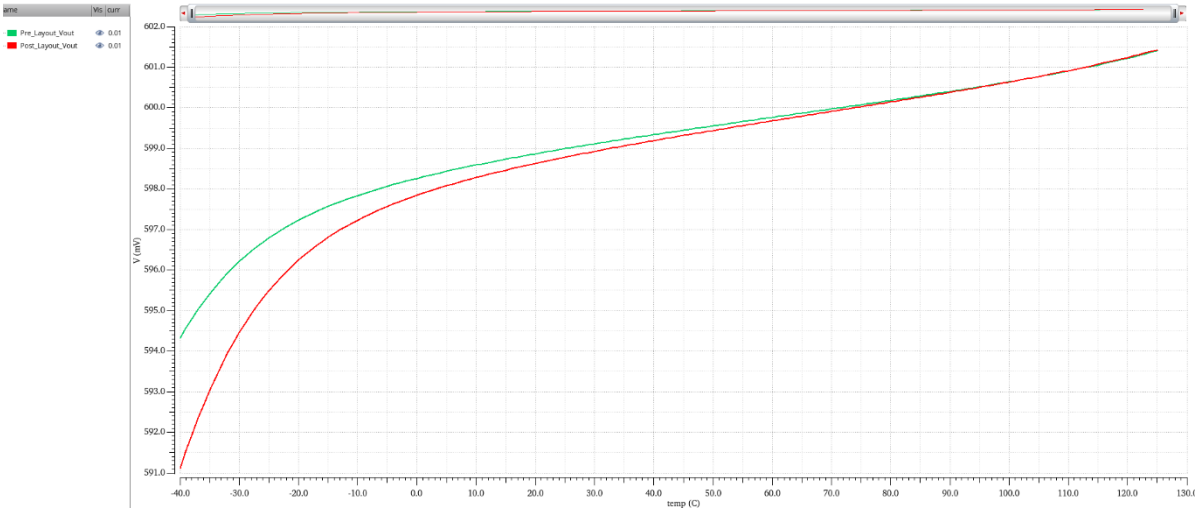

Figure 22 Output Voltage variation with temperature for Pre and Post Layout Simulations

5.3 Transient Simulations

It shows the real-time behavior of the post layout circuit with the changing load currents.

Figure 23 Post Layout Transient Response of output voltage with load current

5.4 Corner Analysis

The circuit is simulated and analyzed at process corner post layout. The results are recorded in the below table.

Table 2 Figure of merits across different corners

	TT		SS		FF		SF		FS		Unit
Supply Voltage	0.75	0.95	0.75	0.95	0.75	0.95	0.75	0.95	0.75	0.95	V
Supply Current	5.201	5.938	4.757	5.78	5.57	6.09	5.23	5.94	5.11	5.93	uA
Output Voltage	598.9	600.1	596.4	599.6	599.7	600.6	599.4	600.2	593.7	600	mV
Output Capacitor	<100										pF
Load Range	0~10										mA
Line Regulation	6.5		16.11		4.74		4.11		31.72		mV/V
Load Regulation	0.0028	0.0021	0.0038	0.0017	0.003	0.0032	0.002	0.0022	0.0068	0.0026	mV/mA
Undershoot	38.2	37.44	46.73	42.71	34.66	33.32	38.12	37.49	46.94	40.15	mV
Overshoot	62.61	60.83	71.8	68.29	56.30	55.31	59.25	56.92	71.62	65.72	mV
PM	68.94	44.83	74.81	45.5	68.66	43.67	63.67	42.42	78.08	46.91	degree
Temp. Var(%)	1.72	0.52	10.75	0.49	0.86	0.74	0.6	0.53	16.93	0.85	%

5.5 Pre and Post Layout Comparison

The comparison between the post and pre layout simulations presented in the below table.

Table 3 Comparison between pre and post layout simulations

	TT (Pre-Layout)		TT (Post-Layout)	
Supply Voltage	0.75	0.95	0.75	0.95
Supply Current	5.20	5.94	5.201	5.938
Output Voltage	599.7	600.8	598.9	600.1
Output Capacitor	<100			
Load Range	0~10			
Line Regulation	5.45		6.5	
Load Regulation	0.005	0.003	0.0028	0.0021
Undershoot	41.30	44.97	38.2	37.44
Overshoot	64.18	67.93	62.61	60.83
PM	74.63	52.75	68.94	44.83
Temp. Var (%)	1.18	0.47	1.72	0.52

From the comparison between the post and pre layout simulations are within the limit. The conclusion is as followed:

- Line regulation degraded by 19.3%
- Load regulation improved by 44% at 0.75V and 30% at 0.95V
- Stability degraded by 7.6% at 0.75V and 15% at 0.95V.
- Stability degradation has aided us in the undershoot and overshoot.

Chapter 6
Conclusion and Future Work

The present work aims at the design of an LDO regulator in 65nm Technology to meet the target specification. Different parameters were taken into consideration while designing. We discussed about the LDO basics and then the correlation of basic in the practical form. The comparison of designs from the state of the art are shown below.

Table 4 Comparison between different Publications

	This Work	[1]	[2]	[3]	[4]	[6]
Technology (nm)	65	21	130	90	65	65
Supply Voltage (V)	0.75-0.95	0.65-0.9	0.58-0.9	0.75-1.2	0.6	1.2
Supply(Quiescent) Current (uA)	5.20	5	4	8	32	50-90
Output Voltage (V)	0.6	0.6	0.53	0.5~1	0.3-0.55	1
Output Capacitor (pF)	<100	<100	0-120	<50	<40	140
Load Range (mA)	0~10	0~10	0.1~3	0~100	0~50	0~10
Line Regulation (mV/V)	6.5	16	29	3.78	-	37.1
Load Regulation (V/A)	0.0028	0.5	1.2	0.1	-	1.1
Undershoot (mV)	38.2	10	118	77	133.9	43
Figure of Merit (FOM)*	0.163 ps @ 50pF 0.0016 ps @500fF	0.025ps	3.147ps	0.002ps	0.137ps	5.74
Area (mm^2)	0.005	0.015	-	0.019	0.016	0.023

**Calculated at the mid value of output capacitor*

Future work would include following:

1. Increasing the response time.
2. Improving transient response by using complex feedback system.
3. Reducing current consumed while maintaining the circuit stability.

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[1] Chen, W.C., Su, Y.P., Lee, Y.H., Wey, C.L. and Chen, K.H., 2014, February. 17.10 0.65 V-input-voltage 0.6 V-output-voltage 30ppm/° C low-dropout regulator with embedded voltage reference for low-power biomedical systems. In 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC) (pp. 304-305). IEEE.

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