Department of Electronics and Communication Engineering

High-Resolution Digital Frequency Synthesizer for 77 GHz Automotive Radar Transmitters

by

Veeraj Pandey (M.Tech, IIITD)

Under the supervision of:

Ankur Bal (Principal Engineer, STMicroelectronics)

and

Dr. Shobha Sundar Ram (Associate Professor, IIITD)

Indraprastha Institute of Information Technology Delhi

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HIGH-RESOLUTION DIGITAL FREQUENCY SYNTHESIZER FOR 77 GHZ AUTOMOTIVE RADAR TRANSMITTERS

A THESIS

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Certificate

This is to certify that the thesis titled "**High-Resolution Digital Frequency Synthesizer for 77 GHz Automotive Radar Transmitters**" being submitted by Veeraj Pandey to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

June, 2020

Dr. Shobha Sundar Ram
Department of Electronics and Communication Engineering
Indraprastha Institute of Information Technology Delhi
New Delhi 110 020

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ABSTRACT

A high resolution 77GHz linear chirp signal synthesizer for a monostatic frequency modulated continuous wave (FMCW) radar is presented. The proposed linear frequency modulation design uses a fixed frequency multi-stage phase-locked loop (N-PLL) for generating a 77GHz chirp signal. The novel design feature is the incorporation of an additional digital control block clocked from a derived signal output from the N-PLL. A reference oscillator activates the chirp generator block. The clock provided to this block is from the intermediate stage of the N-PLL. Therefore, the generator is clocked at Gigahertz rather than a few Megahertz. This clocking signal can be seen as the sampling frequency of the chirp signal generated. The frequency resolution of the generated chirp signal increases, keeping the bandwidth of chirp intact. The digital block is based on lookup tables. Individual lookup tables and circuits are used when the clock provided by the PLL is of constant frequency, and when the clock provided is "chirpy" due to PLL itself being chirpy. Simulation results using an ideal PLL demonstrate the workability of the proposed method. The all-digital open-loop architecture is simulated with the PLL to generate a high resolution, low noise narrowband chirp with an SFDR performance above 100dB at the PLL output. The digital design does not constrain the fixed frequency PLL design in any way. The resulting chirp signal conformed to above 99.95% linearity. The phase noise modeling of first-order has also been done in the Voltage Controlled Oscillator block of PLL, and relative deviation results of simulation with Gaussian

random input have been considered. The approach provides excellent frequency resolution, thereby increasing the unambiguous range of the radar. The high bandwidth of chirp ensures an excellent radar range resolution while the moderate duration of chirp provides a right balance between velocity resolution and maximum unambiguous velocity. Also, the statistics pertaining to these two are improved as a whole. The distortion seen at output manifests only due to PLL non-idealities, of which analysis has been performed, and results have been discussed. The distortion seen at output manifests only due to PLL non-idealities, of which analysis has been completed, and results have been presented. The model can be used alongside applications that require high-frequency resolution chirps with large bandwidth.

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CHAPTER 1: INTRODUCTION

Automotive radars typically transmit linear frequency modulated continuous waveforms (Linear-FMCW). These waveforms offer significant advantages to the pulse-Doppler waveforms. Firstly pulse-Doppler radars send very high power for short durations. Hence, the dynamic power requirements of the system are very high, which makes the system bursty and sometimes mechanically unstable. Secondly, while the high-power impulse is transmitted, the receiver of the radar has to be turned off. This creates a blind spot of a few hundred meters in front of the radar. The FMCW waveforms, on the other hand, have a high duty cycle where the power is evenly distributed in time and frequency. Due to the moderate dynamic power requirements, there exists no need to turn off the receiver during transmission. Hence there exist no blind spots in front of the radar, and the system design complexity is not high.

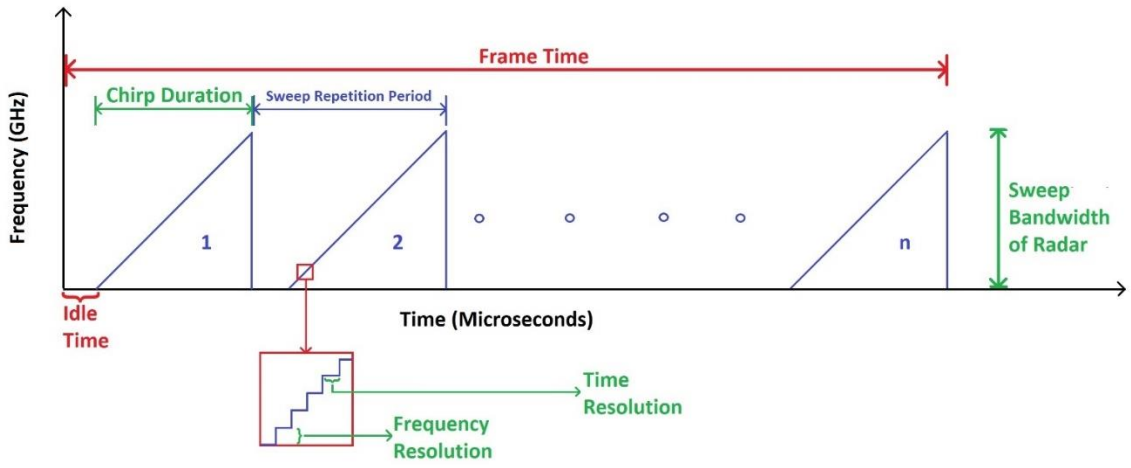

FIG. 1. FMCW RADAR FREQUENCY VS. TIME CHARACTERISTICS

Fig.1 shows a train of chirps being transmitted by an FMCW Radar transmitter in frequency vs. time-domain representation. The issue with FMCW state-of-the-art radars is its limited range, which is due to the low-frequency resolution of the chirp signal (discussed in detail below). We aim to resolve this issue in this research. The transmitter uses an analog Phase-locked loop to multiply input frequency up to the desired output frequency. The transmitter is allowed to transmit only when the signal is being modulated linearly in the frequency domain. The PLL contains a resistor-capacitor (RC) network as its loop filter ahead of the charge pump. Due to this network having a charging and discharging characteristic, the PLL takes time to stabilize before it can start providing the required chirp output.

Furthermore, just after the chirp has swept its required bandwidth, the PLL needs time to stabilize again before providing the initial frequency of the next chirp. The transmitter is turned off during both of these time durations when the PLL is not stable. These durations constitute the idle time of the radar. The frequency sweep takes place in steps which form the frequency resolution of the signal. The step size of the frequency is inversely related to the maximum unambiguous range and hence needs to be as low as possible. This is possible only when the chirp signal generator is provided with a high-frequency clock to increase the sampling rate.

Literature Review

There are currently several different designs of FMCW radar transmitters. The authors in [2]-[4] use a low-frequency clock to generate a chirp signal using a Direct Digital Synthesizer (DDS), as shown in Fig.2. The output signal is multiplied in a

fractional N-PLL to obtain a millimeter-wave signal. The issue with this design is that the frequency resolution of the signal being generated by the DDS is not very good as the sampling clock provided to it is of the order of few Megahertz.

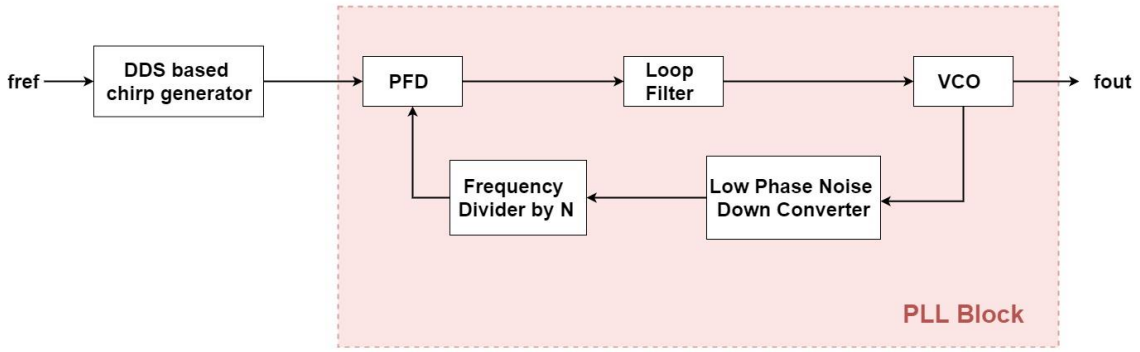

FIG. 2. CHIRP GENERATION USING DDS AND MODIFIED PLL

The authors in [5]-[7] propose slightly different designs in which the signal from the DDS is mixed with a high-frequency signal to upconvert it. The issue of low-frequency sampling in chirp generation persists in these designs as the reference clocks are in few hundred-megahertz ranges. Fig.3 below illustrates this architecture, wherein the multiplier x N multiplies the signal 2 or 3 times, followed by a bandpass filter (BPF). These multiplier stages can be repeated multiple times, thereby increasing the central frequency of the chirp signal. However, this results in adding noise to the low frequency sampled signal.

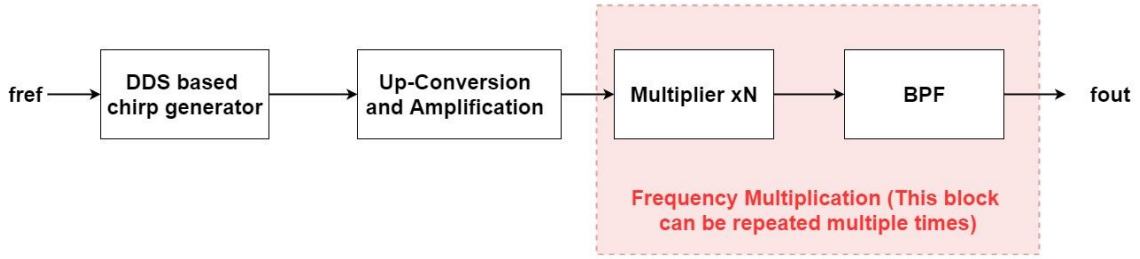

FIG. 3. CHIRP GENERATION USING DDS FOLLOWED BY FREQUENCY UP-CONVERSION USING A MIXER AND THEN MULTI-STAGED SIGNAL MULTIPLICATION BY N AND BPF BLOCKS

To overcome this issue, [8]- [11] uses another high-frequency generator before the chirp generator to provide a sampling clock of the Gigahertz frequency range. Different multi-stage mixers and modulations follow this signal. The issues with these designs are two folds, firstly the new high-frequency clock generation for chirp generator sampling required its circuitry, thereby increasing the power and area requirements of the system. Secondly, multi-stage modulations and mixing of signals induce noise at every stage, which is difficult to filter for microwave signals. This makes it difficult for the system to be implemented, and also the Spurious Free Dynamic Range (SFDR) is not very high. Fig.4 illustrates this architecture wherein the high-frequency clock provided to DDS based chirp generator can be modeled using either a Dielectric Resonator Oscillator (DRO) or an Xtal Oscillator followed by frequency multiplier using PLL.

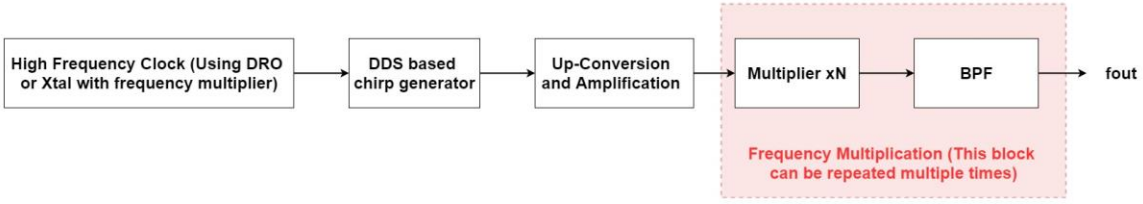

FIG. 4. CHIRP GENERATION WITH HIGH-FREQUENCY CLOCK INPUT TO DDS BASED GENERATOR FOLLOWED BY UP-CONVERSION AND MULTI-STAGE SIGNAL MULTIPLIER BY N WITH BPF

In Fig. 5, [12] and [13] put the chirp generator inside the PLL so that the signal synthesize is fed with the high-frequency clock output from the PLL's Voltage Controlled Oscillator. The issue with this design is quantization and truncation errors generated by the chirp generator inside PLL gets propagated in the loop through Phase Frequency Detector (PFD) of the PLL and thereby gets multiplied along with the chirp signal. This phenomenon decreases the SFDR of the signal. Other similar designs include using a sigma-delta modulator inside the feedback path of PLL. Again, the issue with that is that quantization and truncation error induces a massive distortion to the signal performance parameters. To avoid such distortions, we need a solution outside the PLL. While tuning of parameters of PLL can be performed, any architectural change to PLL will make fabrication processes difficult and induce errors such as above.

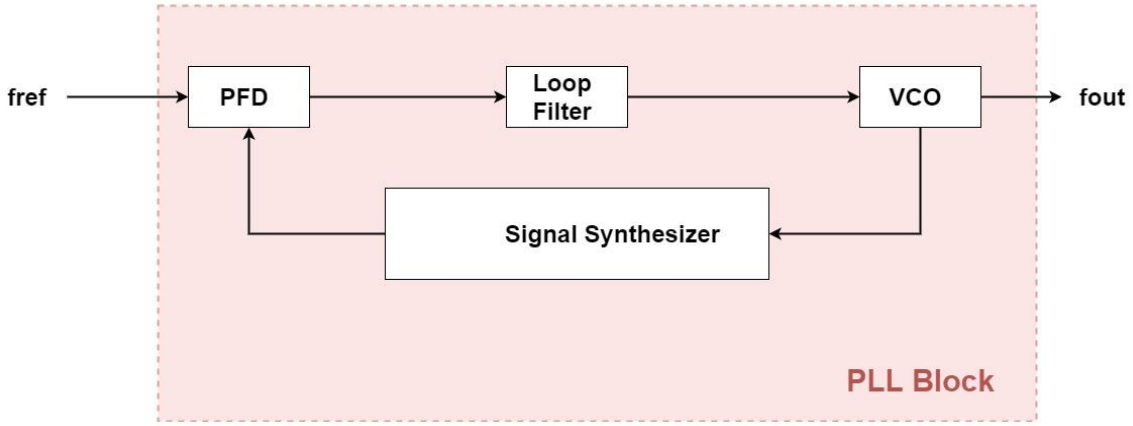

FIG. 5. GENERATION OF CHIRP USING SIGNAL SYNTHESIZER INSIDE THE FEEDBACK LOOP OF PLL

This work proposes a purely digital solution where we use the high frequency (10 GHz) clock from the PLL directly into our digital control block, which provides a high-resolution chirp as input to PLL. This chirp, when passed through the PLL, provides

a high-frequency resolution stepped frequency chirp from 75GHz to 78.75GHz. Two more contributions of this work are: (1) Demonstrate that chirp signal can be generated without a reference clock being applied during the generation and (2), a continuously varying frequency clock can be used to clock digital blocks to generate required signals.

CHAPTER 2: GENERATION OF HIGH PRECISION CHIRPS

Operational parameters of the FMCW Radar chirp signal generator design needs to be derived from radar specifications. Relationships between radar range, radar range resolution, maximum velocity and minimum velocity resolution with chirp parameters such as frequency resolution of chirp, the bandwidth of chirp, the sampling frequency of chirp and chirp duration have been defined below.

a) Relationship between Radar Range Resolution and Bandwidth of the chirp signal Radar

Range resolution (Δr) refers to the ability of the radar to resolve two targets spaced close to each other. radar range resolution can be found by:

$$\Delta r = \frac{c\,\Delta t}{2} \tag{1}$$

Where c is the speed of light in a vacuum (in meters per second), and Δt is the time resolution of radar (in seconds). Since the chirp sweeps a bandwidth B (in Hertz) in time T (in seconds), for a frequency resolution of 1/T, the time resolution of chirp becomes 1/B. Substituting this value of Δt in (1) gives us:

$$\Delta r = \frac{c}{2B} \tag{2}$$

Using this relationship, we can find the bandwidth of the required chirp signal corresponding to the radar range resolution.

b) Relationship between Radar Unambiguous Range and Frequency Resolution of the chirp signal

Radar unambiguous range (R) defines the maximum value of distance up to which the transmitted pulse can travel to the target and back from it between consecutive transmitted pulses. Maximum radar unambiguous range can be found by:

$$R = \frac{C}{2} T_{srp} \tag{3}$$

Where T_{srp} represents the sweep repetition period. To estimate the maximum unambiguous range, we need to consider receiver limitations as well. For the receiver part, we mix the transmitted signal with the received signal, which gives us a sum and difference of frequencies. This signal is passed through a low pass filter, which retains the difference of frequencies called Intermediate Frequency (IF). For a single object in front of the radar, this value remains to be constant throughout. This frequency can be calculated by multiplying the slope of the chirp (S) with T_{srp}. From (3) we can write the delay in terms of R. This gives us the following:

$$IF = ST_{srp} = S\frac{2R}{C} \tag{4}$$

The maximum value of range by this relationship depends upon the intermediate frequency. The system constraint remains that IF has to be less than or equal to sampling frequency (Fs) which gives us the following relationship:

$$S\frac{2R}{c} \leq F_s \tag{5}$$

Rearranging this relationship for corner value gives us the maximum unambiguous range:

$$R = \frac{F_s}{2}\frac{c}{S} \tag{6}$$

The term slope of chirp is defined as the ratio of frequency resolution (Δf) to time resolution. Time resolution we can take as sampling frequency. This gives us the following relationship:

$$S = F_s \Delta f \tag{7}$$

Using equation (6) and (7), we can correlate Radar Unambiguous Range with Sampling Frequency and Frequency Resolution of Chirp Signal. The constraint on maximum Sampling Frequency is hardware-oriented. In our

simulation, we have taken this value to be 10 GHz. With the above relationships, we can find the frequency resolution of the chirp signal corresponding to radar unambiguous range.

c) Relationship between Measurable Velocity Resolution, Maximum Detectable Velocity and Sweep Repetition Period

The maximum velocity a system can detect is dependent on the phase of the reflected signal with respect to the transmitted signal. We can define the phase Ø as:

$$\emptyset = 2\pi f_c T_{srp} \tag{8}$$

Where f_c is the central frequency of radar. Substitute value of f_c in terms of wavelength (λ) and T_{srp} in terms of R using equation (3) to get:

$$\emptyset = 4\pi \frac{R}{\lambda} \tag{9}$$

Substitute R= V * T_{srp} where V defines the velocity of the target and T_{srp} includes the chirp duration (Tc) and idle time to get:

$$\emptyset = 4\pi \frac{VT_{srp}}{\lambda} \tag{10}$$

For maximum detectable velocity (Vmax), we need to constraint $\emptyset \leq \pi$ which using (10) gives:

$$V_{\max} = \frac{\lambda}{4T_{srp}} \tag{11}$$

Measurable velocity resolution (Δv) refers to the minimum separation between two radial velocities of targets at the same range for the radar to distinguish between the two discrete reflections. Using equation (10) for two different phases Ø1 and Ø2 corresponding to two different frequency V1 and V2 we have:

$$Ø_2 - Ø_1 = 4\pi \frac{(V_2 - V_1)T_{srp}}{\lambda} \tag{12}$$

For FFT on the sequence of N chirps in a frame we require,

$$Ø_2 - Ø_1 \geq \frac{2\pi}{N} \tag{13}$$

From equations (12) and (13) we get a constraint on velocity resolution as:

$$\Delta v \geq \frac{\lambda}{2NT_{srp}} \tag{14}$$

From equation (11) and (14), we can observe that increasing Tsrp decreases velocity resolution but also reduces the maximum velocity the radar can detect. Acknowledging this trade-off, we get the value of T_{srp}. A second trade-off exists between the slope of chirp and chirp duration for a fixed number of points

and T_{sum}. If we increase the slope, we obtain an excellent frequency resolution, but the idle time for the receiver is also very high, which is undesirable. For this, we proceed with an iterative approach to find minimum idle time for chirp defined by a fixed number of points and hence find the appropriate chirp duration.

d) Relationship between the number of sample points, Chirp Duration and Sampling Frequency

The number of sample points in a chirp can be calculated by multiplying chirp duration with sampling frequency. These numbers of points are responsible for the reset of the system once the chirp signal reaches its maximum frequency.

Design Elaboration:

Equation (6) shows that the range of the radar is directly proportional to the sampling frequency. We intend to derive a high-frequency clock from the PLL and use it as a clock source for our digital chirp generation block.

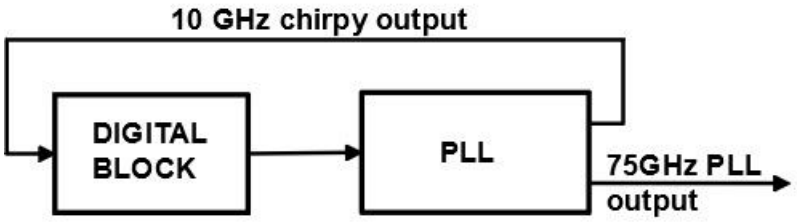

FIG. 6. HIGH-LEVEL BLOCK DIAGRAM REPRESENTATION OF HIGH RESOLUTION 77GHZ CHIRP GENERATOR

The issue with the feedback clock from PLL is that along with the PLL output as chirp, and the feedback clock also has an increasing frequency. This is called a chirpy clock. The digital block must produce the required linear chirp as output for the PLL despite being fed with a variable frequency clock instead of a constant frequency clock.

2.1 FRACTIONAL N-PLL DESIGN

The fractional N-PLL in our design serves the purpose of multiplying the input clock frequency by 750 and providing it as an analog output as well as providing a 10GHz clock output. To achieve this, we use a charge pump based PLL.

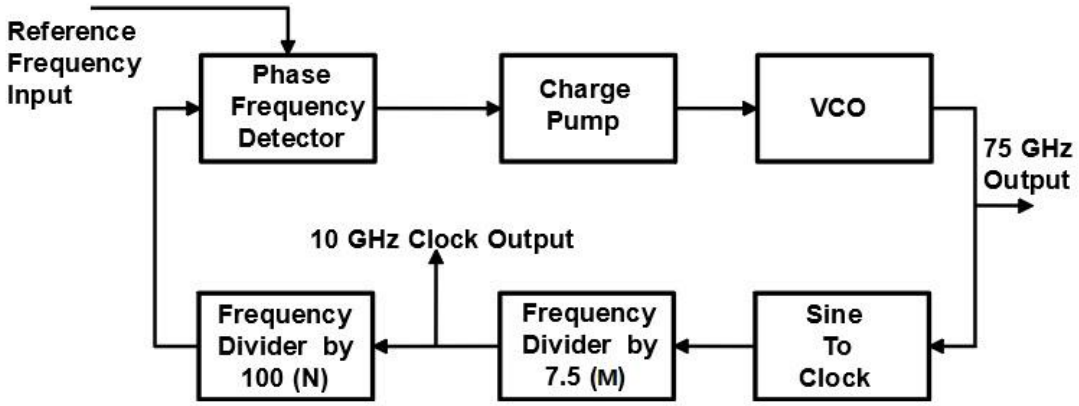

FIG. 7. BLOCK DIAGRAM REPRESENTATION OF FRACTIONAL N-PLL

In Fig.7. We can see that instead of a single block of 750, we have used two blocks of frequency division. This is to obtain a clock output of 10GHz from the output of the 7.5 frequency division block. We discuss these blocks in detail below.

2.1.1. Phase Frequency Detector (PFD)

Phase frequency detector has the purpose of generating the phase mismatch signal between the feedback signal and the reference clock. The phase mismatch signal, or error signal, directs the VCO to increase or decrease the frequency of the signal in the

feedback path. The architecture for digital phase frequency detector as defined in [15] and [16] uses Finite State Machine (FSM) based modeling. Fig.8 below illustrates the FSM model defined for PFD in our design.

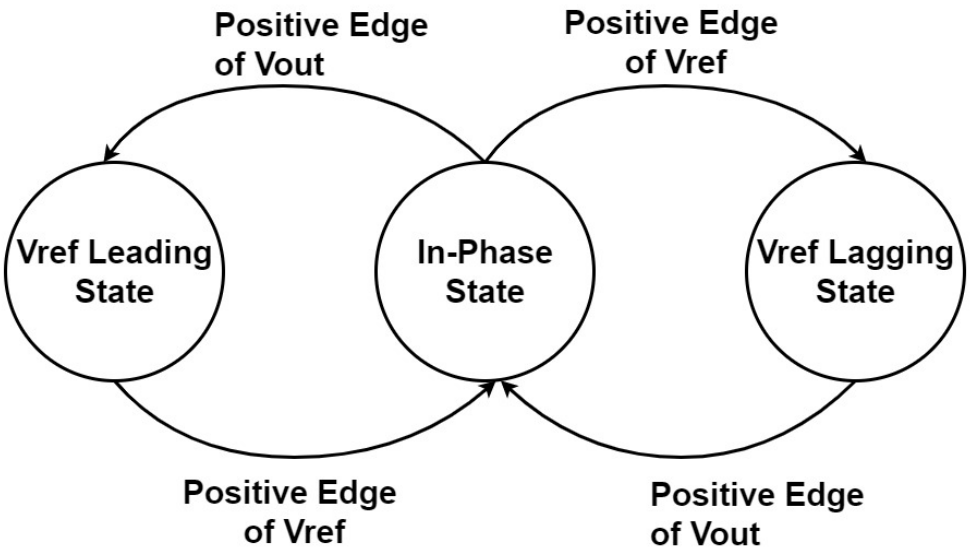

FIG. 8. FINITE STATE MACHINE MODEL FOR PHASE FREQUENCY DETECTOR USED IN THE DESIGN

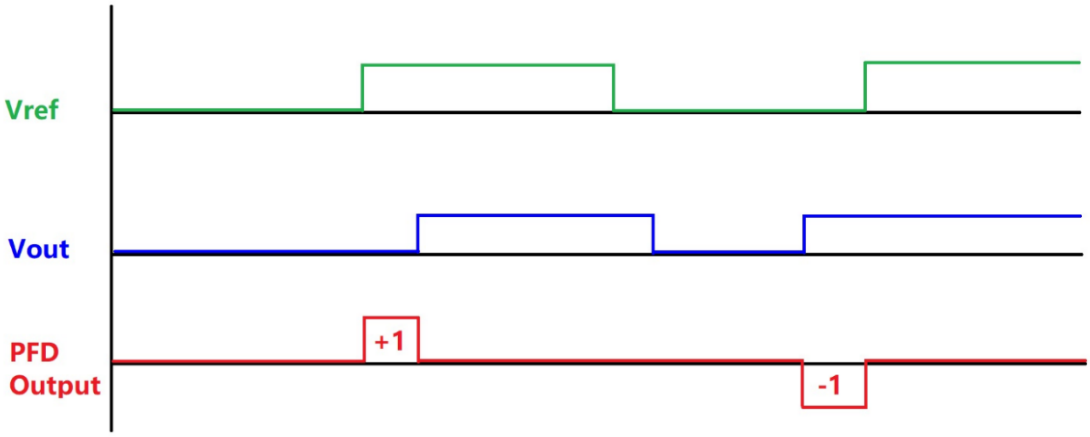

FIG. 9. ILLUSTRATION TO DEMONSTRATE THE FUNCTIONING OF PFD

In this model, the In-Phase State defines when both the reference clock signal and feedback clock are entirely in the same phase. As per fig.9, when they are in the same phase, the output of PFD remains 0. PFD outputs when the reference signal comes. The feedback signal is lagging for the same duration of lag. This positive voltage provided to VCO increases the frequency of output, and thereby the feedback path frequency increases. In case the feedback signal comes before the reference clock, or in other words, the feedback system leads the reference clock, the PFD generates a negative voltage for VCO. This makes the feedback path frequency lesser, thereby trying to bring the reference signal and feedback signal in the same phase, also called Phase Lock.

2.1.2. Charge Pump and Loop Filter

For the charge pump, we have modeled a third-order control system. Here the error would depend on the integration of frequency, and phase error is zero when locked to a fixed rate of change of frequency.

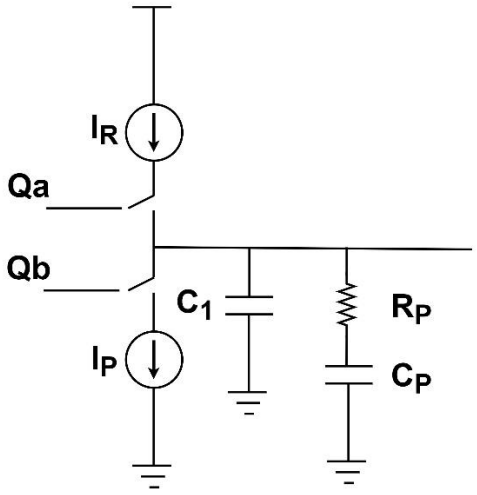

FIG. 10. THIRD-ORDER CHARGE PUMP PLL

We used the following method to find the values of passive components in the charge pump filter:

Step 1. Define a third-order open-loop transfer function as T(s) where

$$T(s) = \frac{I_p K_v}{s^2} \frac{\left(1 + \frac{s}{\omega_z}\right)}{2\pi MN(C_p + C_1)\left(1 + \frac{s}{\omega_{p3}}\right)} \tag{15}$$

Where I_p is the charge pump current

K_v is the gain of Voltage Controlled Oscillator

ω_z is the zero of transfer function also,

$$\omega_z = \frac{1}{R_p C_p} \tag{16}$$

ω_{p3} is the 3rd pole of transfer function also,

$$\omega_{p3} = \frac{C_p + C_1}{R_p C_p C_1} \tag{17}$$

M is the first frequency division block; N is the second frequency division block, and M*N is the number by which reference clock frequency is multiplied.

Cp and C1 are the capacitors used as per Fig.9.

Step 2. Take $C_p = 10C_1$

Step 3. Take |T(s)|=1 for Gain Crossover

Step 4. Define a ratio for k where,

$$k = \sqrt{\frac{1+\sin\theta}{1-\sin\theta}} \tag{18}$$

where Θ is the phase margin required

Step 5. Take the value of gain crossover frequency ω_c as 10% of reference clock frequency

Step 6. Select the poles and zeros of this system around the gain crossover frequency such that,

$$\omega_z = \frac{\omega_c}{k} \tag{19}$$

and

$$\omega_{p3} = k\omega_c \tag{20}$$

Step 7. Put these values in |T(s)|=1 to get total capacitance and then use the following relationship to get C_1,

$$C_1 = \frac{C_{net}}{k^2} \tag{21}$$

Where $C_{net} = C_p + C_1$

Step 8. Subtract C_1 from Cnet to get C_p

Step 9. Use equation (16) to get the value of R

PLL Tuning Plots:

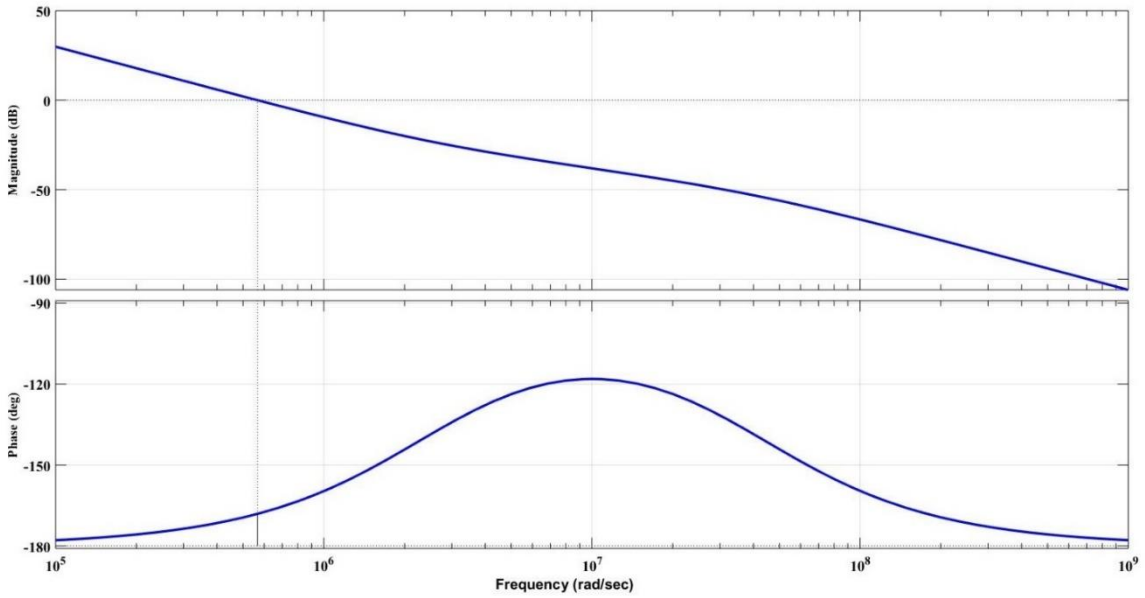

FIG. 11A. BODE PLOT OF THE 3RD ORDER CHARGE PUMP PLL

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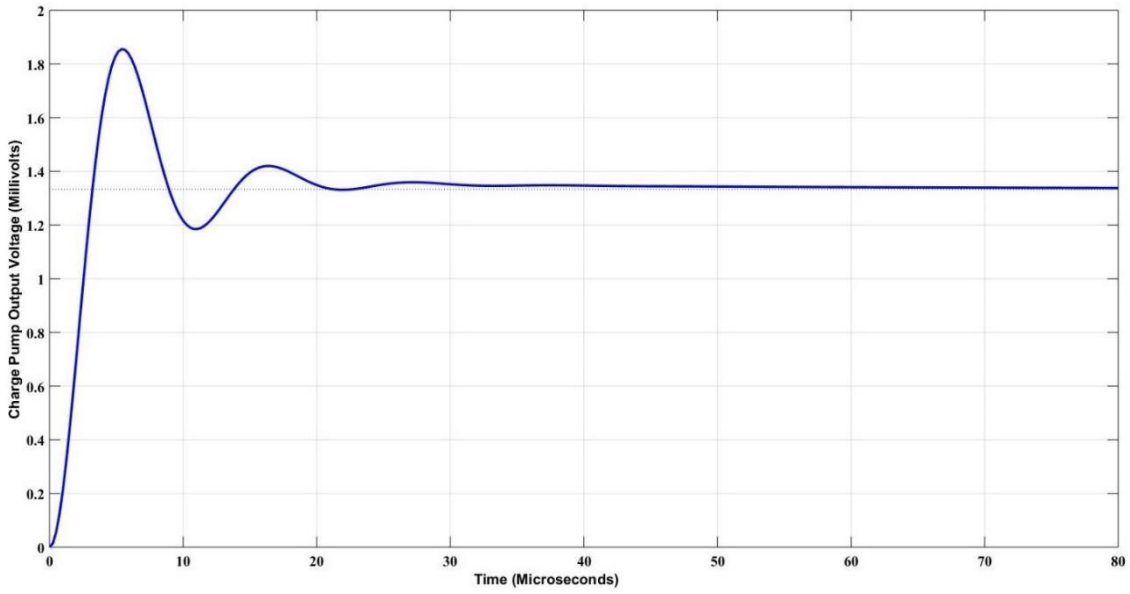


FIG. 11B. STEP RESPONSE OF THE SYSTEM

From Fig.11a and Fig.11b. We can conclude that the system is stable for the configurations we have taken and hence can now be used in our design.

2.1.3. Voltage Controlled Oscillator (VCO)

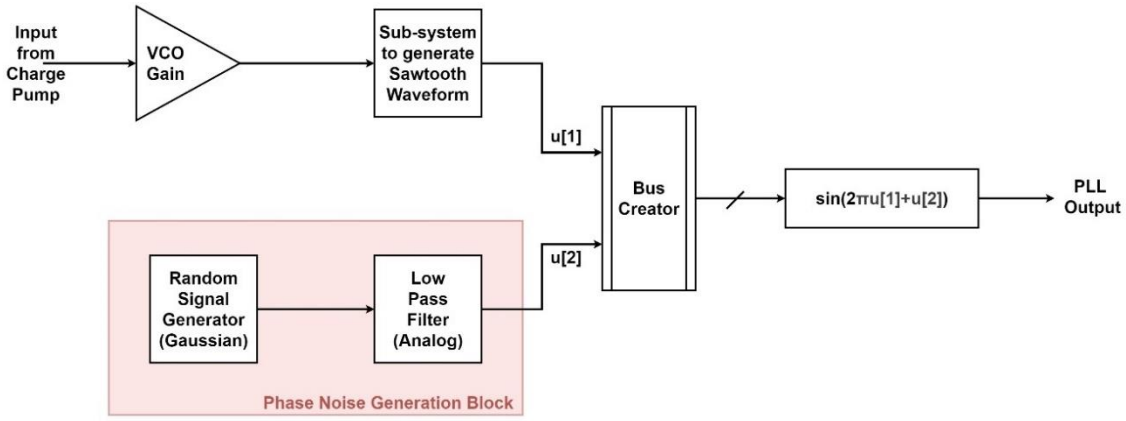


FIG. 12. BLOCK DIAGRAM REPRESENTATION OF VCO

The VCO has the role of generating a sinusoidal signal of frequency proportional to the input voltage from the charge pump with minimum noise. Fig. 12. gives a block diagram representation of VCO. The VCO gain block is used to define a linear relationship between the input voltage and the output frequency of the signal. The next block is a sub-system to generate a sawtooth waveform. This block uses a discrete accumulator, which adds the input voltage based on the sampling frequency of the signal, thereby generating a ramp. This is followed by a modulo block to reset the ramp to generate the sawtooth waveform. This signal is combined as a bus using a bus creator with a phase noise generator (PNG) Block. The PNG block uses a random signal generator modeled by a Gaussian function followed by an analog Butterworth low pass filter of frequency less than or equal to sawtooth waveform frequency. This signal is then passed through a sine function, where the signal is used as the frequency of sine while the

noise as its phase. The output of this is the final output of the system. The feedback path also initiates from this output node.

2.1.4. Sine to Square

The output of VCO needs to be converted from an analog signal to square wave. To achieve that, we use a simple threshold comparator. The comparator outputs positive "1" logic when the sine signal is positive and "0" logic when the sine signal is negative.

2.1.5. Frequency Divider

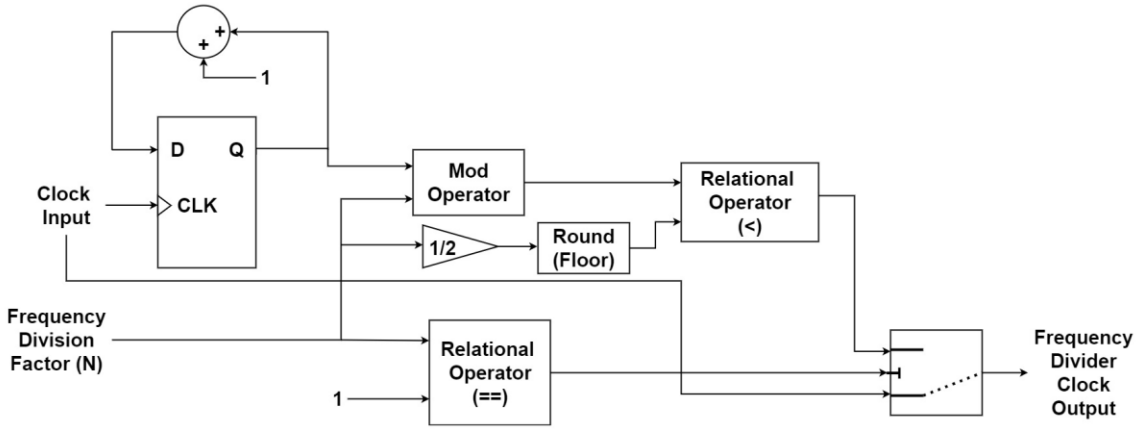


FIG. 13. BLOCK DIAGRAM REPRESENTATION OF FREQUENCY DIVIDER CIRCUIT

The system can be implemented using a shift register-based frequency division. Still, for genericity (we can perform both integral and decimal division by this method),

we have implemented the block diagram shown in fig.13. The design elaboration begins by taking input as a clock to the clock input of D flip flop (DFF), where the output of DFF is accumulated and passed as input to DFF. This output is then passed through the Mod operator, which finds the mod of this frequency division factor (N). This mod value is compared with N/2, and if this value is less than round (N/2), 1 is given as output to switch connected to the output. Else 0 would be given as output using lesser than relational operator (<). If the value of N is 1, this would mean no division of frequency is required, hence using an equality comparison operator, we direct the clock input as the output of the divider circuit using a switch connected to the output of the sub-circuit.

2.2 DIGITAL CONTROL BLOCK DESIGN

The digital block is designed to drive the reference clock input of the PLL momentarily. During the brief chirp generation interval, the external reference clock is decoupled from the PLL input, and a digital circuit feeds a modulated reference clock. The linear frequency modulated clock generated by the digital block ranges from 100MHz to 105MHz in very fine quantization steps. This is multiplied by the PLL to produce an output signal chirp between 75GHz and 78.75GHz. Derivation of the digital block parameters is explained in detail.

By the property of linear chirp, we can define its instantaneous frequency as:

$$f_i(t) = \alpha t + f_0 \tag{22}$$

Where α is the rate of change of frequency defined as:

$$\alpha = \frac{f_1 - f_0}{T} \tag{23}$$

Where f_1 is the final frequency of chirp, and f_0 is the initial frequency. Integrating frequency, we get the phase as:

$$\theta(t) = 2\pi \frac{\alpha}{2} t^2 + 2\pi f_0 t + \phi \tag{24}$$

For a cosine chirp, we take the value of ϕ as $\pi/2$.

The chirp equation thus becomes:

$$Y = A\sin(2\pi \frac{\alpha}{2} t^2 + 2\pi f_0 t + \frac{\pi}{2}) \quad \text{or}$$

$$Y = A\cos(2\pi \frac{\alpha}{2} t^2 + 2\pi f_0 t) \quad (25)$$

Equation (25) can be written as:

$$Y = \cos(at^2 + bt) \quad (26)$$

Where 'a' and 'b' are coefficients of t^2 and t respectively in (25). We can see that for a chirp signal, the phase of cosine is parabolic.

Digital Block Architecture:

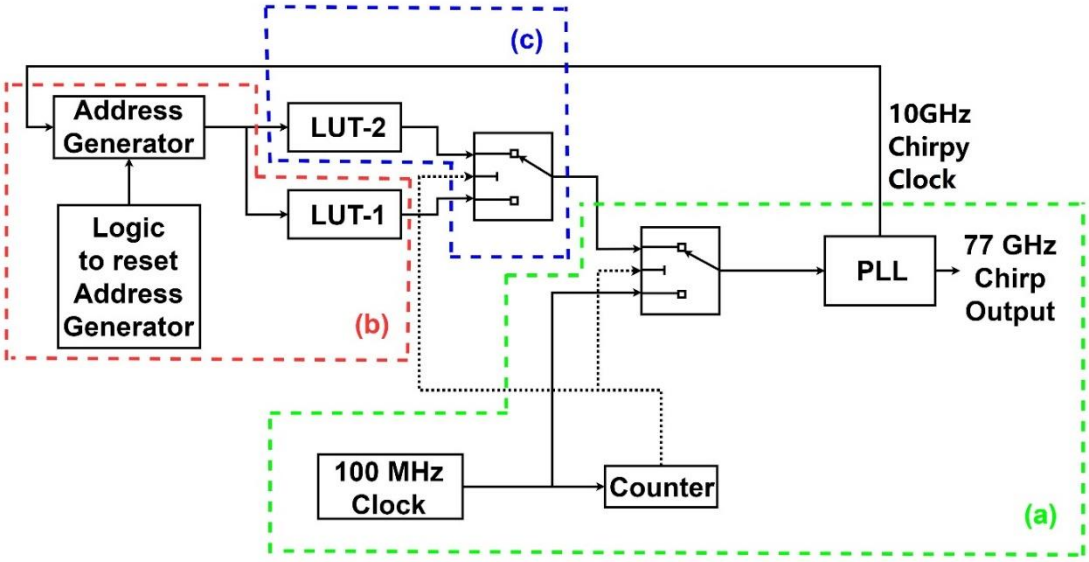
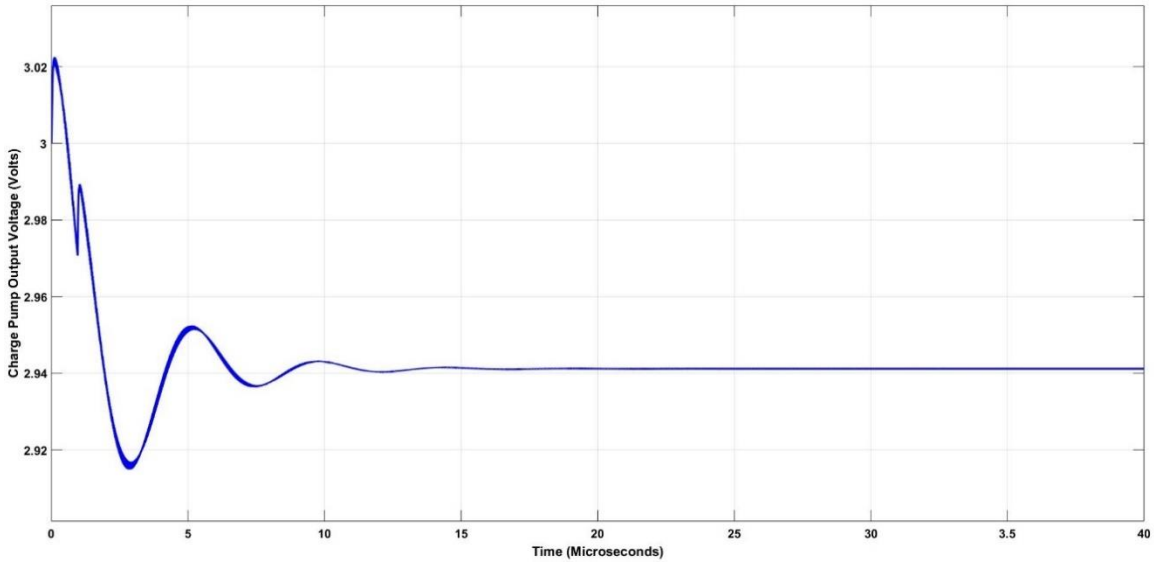
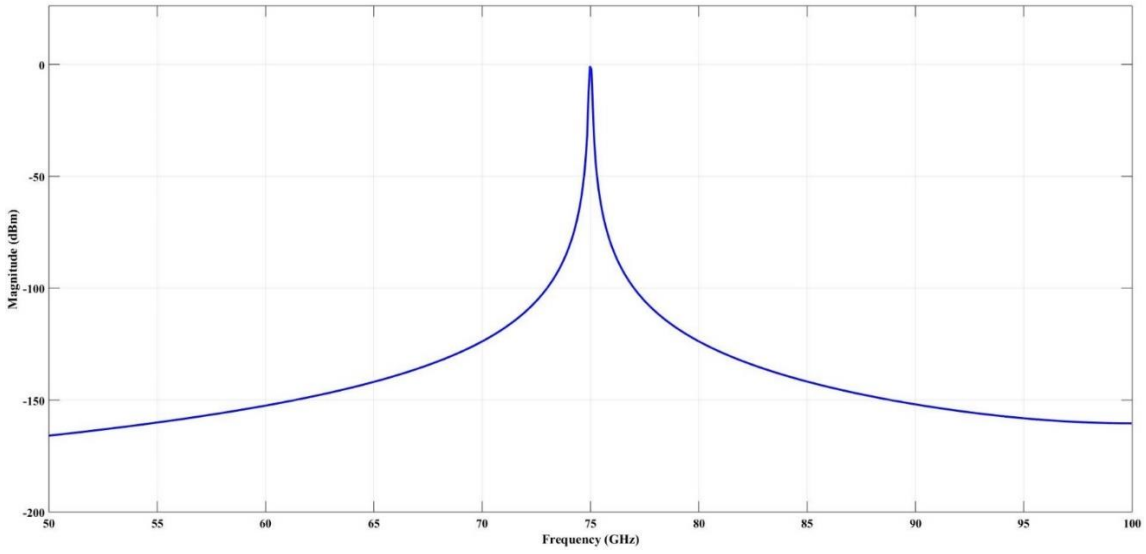


FIG. 14. BLOCK DIAGRAM OF HIGH-FREQUENCY RESOLUTION 77 GHZ FMCW RADAR CHIRP GENERATOR. (A) THE DIRECT CLOCK INPUT TO PLL. (B) CHIRP GENERATION FOR 10 GHZ CONSTANT FREQUENCY CLOCK INPUT. (C) SWITCHED CIRCUIT TO GENERATE REQUIRED CHIRP FOR CHIRPY CLOCK INPUT FROM PLL

The design flow begins when with the above-configured PLL, we add an up-counter clocked at a constant frequency of 100MHz (Fig.14a). The design is simulated in MATLAB Simulink. A stability check of this stage is necessary before switching to other blocks of the circuit. The stable output of PLL is seen as a settled value at the charge pump output (Fig.15a) and a low phase noise analog output on the spectrum scope (Fig.15b) below.



(a)



(b)

FIG. 15. THE OUTPUT OF PLL FOR CONSTANT 100MHZ CLOCK INPUT (A) CHARGE PUMP OUTPUT OBSERVED ON TIME SCOPE (B) PLL OUTPUT OBSERVED AT VCO OUTPUT NODE IN THE FREQUENCY DOMAIN USING SPECTRUM SCOPE

This output validates the proper functioning of our PLL to provide a constant 75GHz output for a 100MHz reference clock input. This output also provides "inertia" to the system, which means even if we remove the clock input, the PLL will still be providing outputs for some cycles. This property of PLL is used by other blocks further after the input to PLL is switched from 100MHz clock to output from Look Up Tables (refer to fig.14).

Fig 14b. Illustrates the circuit switching mechanism for the PLL reference clock. Once the PLL output is stable and phase-locked to 100MHz input clock reference, we use the constant 10GHz divided clock output from as the functional clock to an accumulator used for addressing a Lookup Table (LUT-1). This LUT-1 store's binary clock-like samples of a high-resolution chirp signal generated at 10GHz having a frequency range from 100MHz to 105MHz.

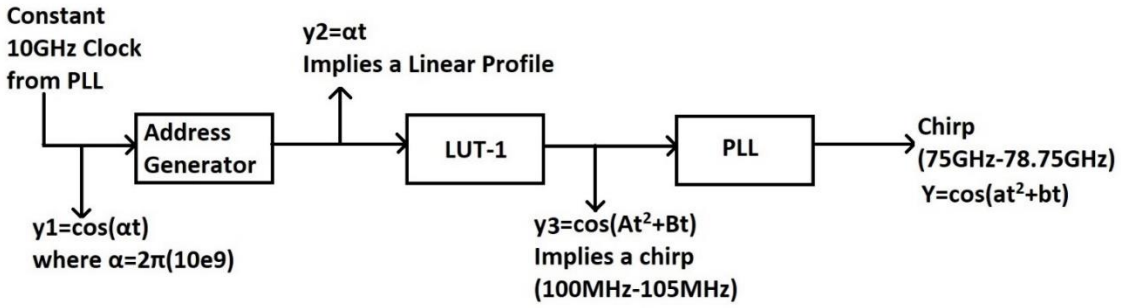


FIG. 16. STAGE-WISE REPRESENTATION OF SIGNAL FOR CONSTANT FREQUENCY CLOCK

As in fig.16, a constant 10GHz clock can be modeled as a cosine of a linear profile in the time domain. When this clock is passed through the addressing accumulator, we get the phase of cosine, and thus a linear profile. This linear profile, when mapped to a chirp of frequency range 100MHz to 105MHz using LUT-1 values,

produces another chirp of 75GHz to 78.75GHz at the PLL outputs. The quality of the chirp at the PLL output is very closely linked to the spectral purity of the 10GHz clock that runs the accumulator. At the beginning of the chirp generation phase, the reference clock input source is switched for a locked state PLL. The switching phase is managed synchronously such that it doesn't disturb the PLL lock. Post switching, the PLL output frequency continues to be constant for a while, even when the input reference starts changing. This is due to the inertial circuit elements used in the design of a PLL. Once the input reference clock modulation starts reflecting at the PLL output, the 10GHz constant frequency output from the feedback divider starts to vary. This means that we no longer have the continuous 10GHz clock for running the digital addressing accumulator, and eventually, it is a chirpy clock with a frequency range of 10GHz to 10.46GHz. The output of the accumulator, which was linear for a constant clock, now acquires a parabolic profile. As seen in Fig. 17, this would saturate the VCO and distort the PLL output indefinitely if left unchecked and uncompensated.

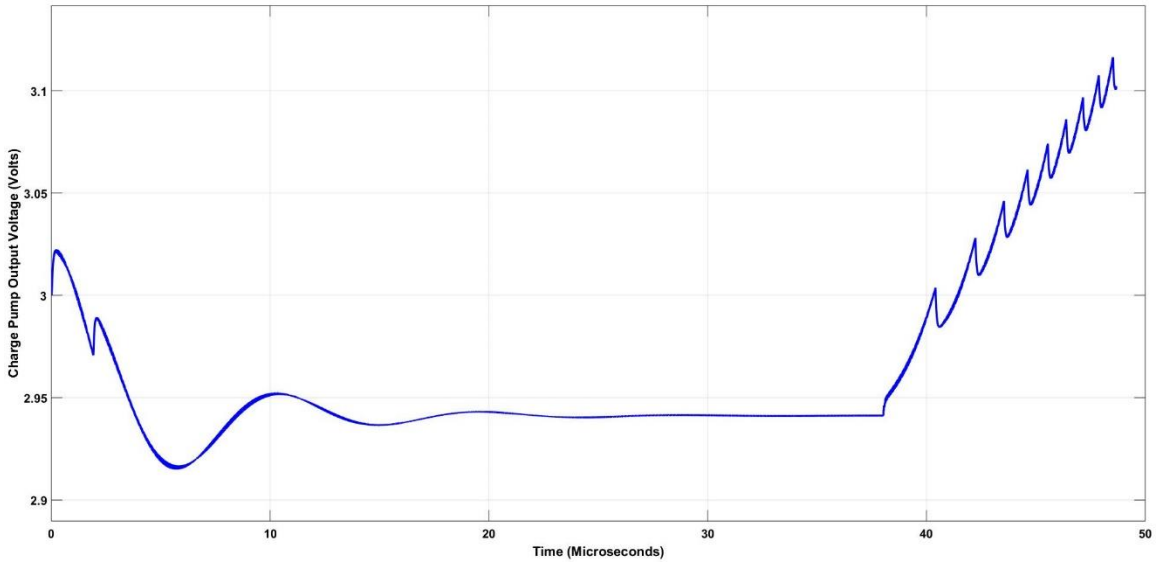


FIG. 17. DISTORTION IN PLL OUTPUT OBSERVED AT CHARGE PUMP OUTPUT DUE TO CHIRPY CLOCK USED FOR ADDRESSING OF LUT-1

Fig 14c. Illustrates the circuit switching from LUT-1 to LUT-2. This is developed to provide the required compensation for the chirpy clock driving the accumulator. The switching takes place precisely when the 10GHz clock from PLL starts to become chirpy. The LUT-2 stores a cosine function of 100 MHz clock sampled at 10GHz. This LUT-2 gives the same chirp as LUT-1 only when the clock to the addressing accumulator starts to vary. This circuit continues its operation until the accumulator reaches its maximum value, following which the complete system is reset to its initial state. Fig. 18. is a block diagram of the active signal path when the digital clock becomes chirpy.

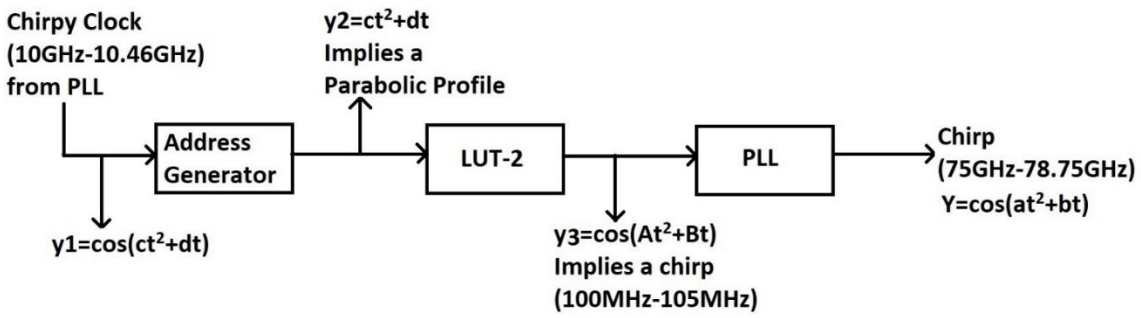


FIG. 18. STAGE-WISE REPRESENTATION OF SIGNAL FOR THE CHIRPY CLOCK

The chirpy clock has a form of the cosine of a parabola (equation 26). This clock, when given to the accumulator, provides the phase of the cosine. When this variable clock is applied to LUT-2 containing a cosine, the output becomes cosine of a parabola, which itself is a chirp signal. This chirp signal is identical to the output from LUT-1 for a fixed frequency clock. Now, this chirp signal continues to rise up the frequency ramp until a frequency of 78.75 GHz is attained. Then the system resets to the initial situation where the reference oscillator is again brought into the picture, and the whole cycle repeats. The reset of the complete system takes place constrained to the maximum limit to the number provided as output by an accumulator in the addressing block. Once the accumulator reaches this number, the system is forced reset, and the PLL starts to fall from 78.75GHz to 75GHz as in reset condition, the input is 100MHz, and hence the expected output is 75GHz. In our design, the time taken by PLL to get settled at 75GHz output after getting reset from 78.75 GHz output is the minimum time margin we need to keep even in the first cycle run of the system so that the system functions stably through its expected duration. By trial and error method, we have found that the

reference clock needs to be present for at least 1900 cycles before it can switch, and the inertia of PLL remains just for 50 cycles after the application of LUT-1, so we need to switch to LUT-2 after 50 more cycles. Hence, the reference clock runs for 1900 cycles, the circuit-switched to LUT-1 runs for another 50 cycles, and the rest with LUT-2.

CHAPTER 3: SIMULATION RESULTS

The presented chirp generator for FMCW Radar Transmitter was developed as a mixed-signal model in MATLAB Simulink. The results corresponding to the charge pump output were obtained using a time scope. In contrast, the frequency domain spectrum was obtained by sampling the analog output signal using a zero-order hold circuit and then using a frequency spectrum scope.

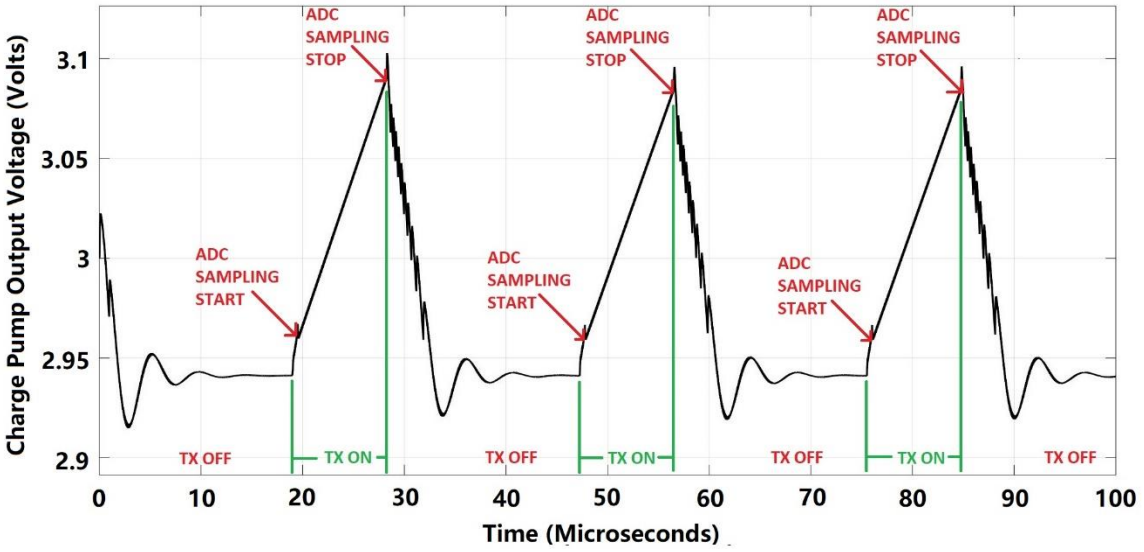


FIG. 19. CHARGE PUMP OUTPUT OF THE TRANSMITTER

From Fig.19, we observe that the chirp obtained from our design is highly linear, and the resolution along amplitude and time is very high. The circuit transmits after the PLL starts to generate a linear chirp continuously. During the remaining duration, the transmitter is off.

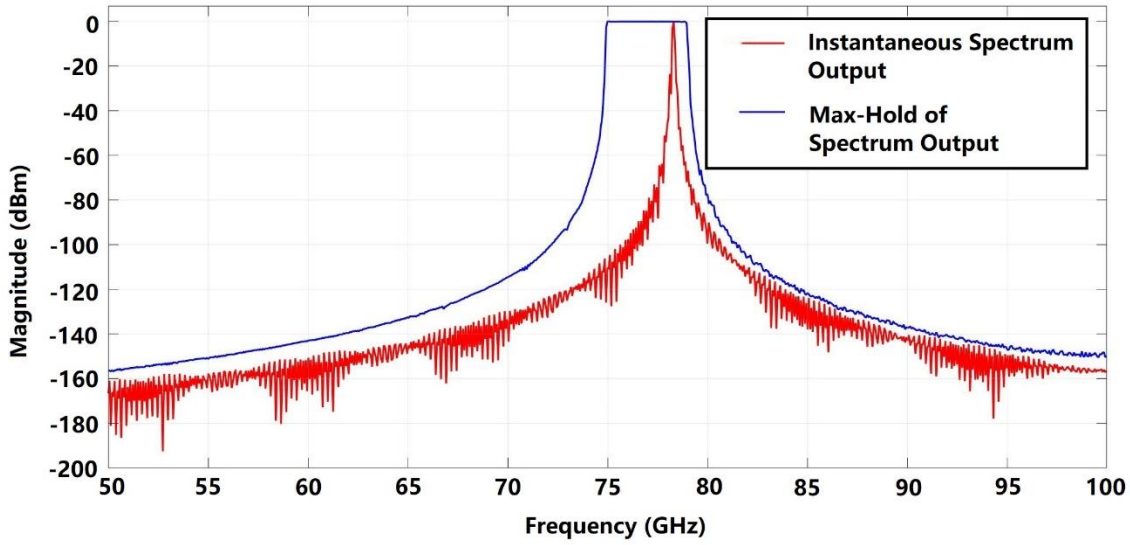


FIG. 20. SPECTRUM RESULT OF PLL OUTPUT OF TRANSMITTER

Fig.20 is the spectrum result of the charge pump output through an ideal VCO. The result shows a very high SFDR of over 100dB for the chirp frequency from 75GHz to 78.75GHz. The red plot shows the frequency of the signal at a random time instance in simulation, and the blue plot shows the complete frequency band swept by the proposed chirp generator. The system has an excellent frequency rejection for frequencies of less than 75 GHz and more than 78.75 GHz, and no spurs due to truncation or quantization error are seen deteriorating the output spectrum of the system.

Test of Linearity of Charge Pump Output:

We use the curve fitting tool to the output of the charge pump to figure out how much out result deviates from a linear response, which is essential for a Linear FMCW Radar. We use a 1st order polynomial to model the curve.

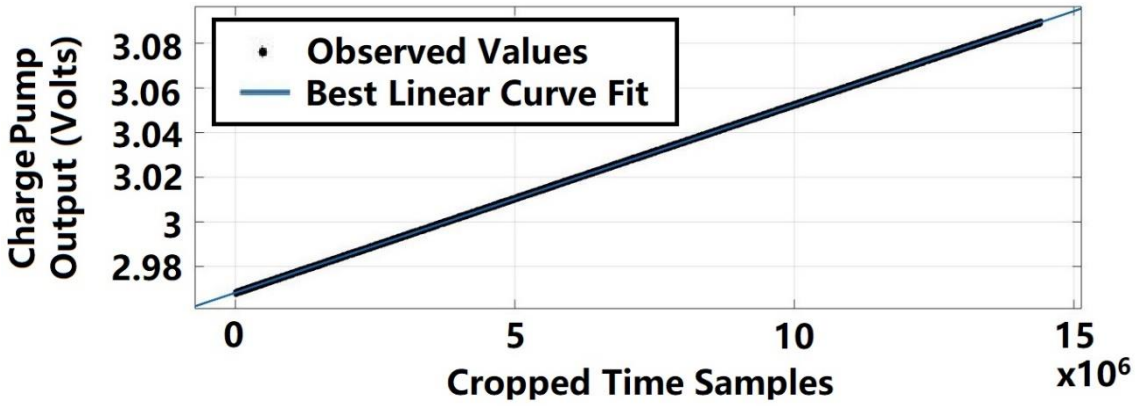


FIG. 21. LINEARITY TEST FOR CHARGE PUMP OUTPUT WITH RESPECT TO A LINEAR FUNCTION

Fig.21 shows the best-estimated line using the curve fitting tool for the charge pump output. This line represents a set of all collinear points having the least variance from the data points of the charge pump output. Diversion of charge pump output from this equation signifies non-linearity. The error estimates are as follows in Table I:

Errors	**Value**
Sum of Square	3.629
R-Square	0.9998
Adjusted R-Square	0.9998
Root Mean Square	0.0005018

TABLE I. ESTIMATE OF NON-LINEARITIES IN SIMULATION OUTPUT OF PROPOSED LINEAR FMCW RADAR CHIRP GENERATOR

Test with 1st order Phase Noise in VCO:

We test the output of the charge pump with the addition of phase noise to it in the VCO block. We simulate four conditions for Gaussian noise as mean = "0" or "1" and variance= "0" or "1" combination for voltage. This step is followed by plotting the down-sampled signal with non-ideal conditions with respect to the signal corresponding to the ideal condition (mean=0 and variance=0). Fig.22 below shows the results of this test. We observe from the plot that even after adding Gaussian noise, our system produces results that are close to ideal.

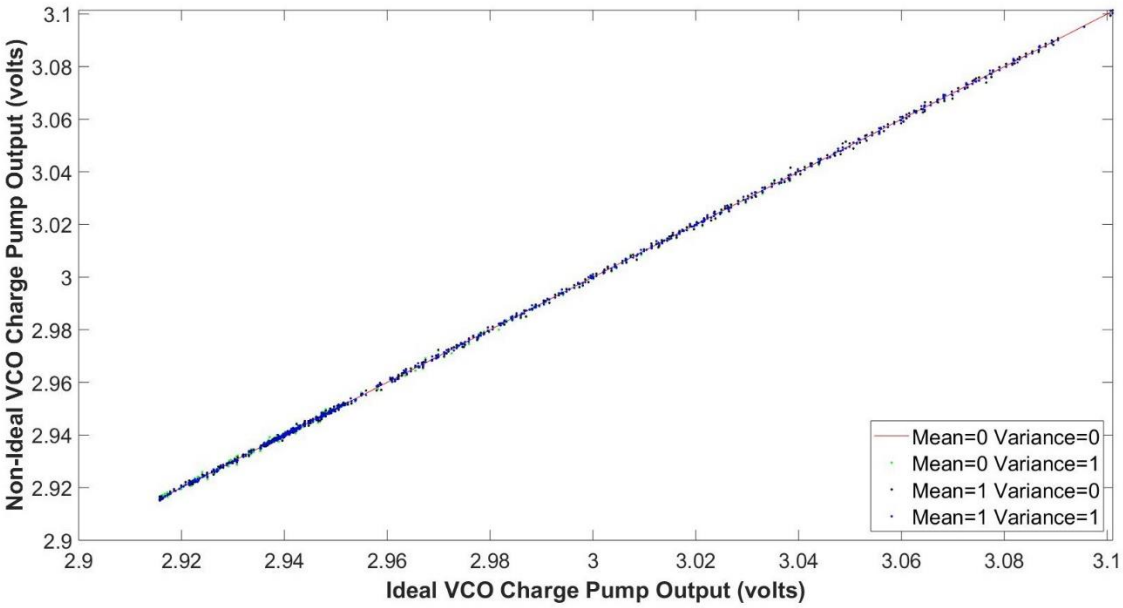


FIG. 22. RELATIVE OUTPUT OF NON-IDEAL VCO WITH RESPECT TO IDEAL VCO

Condition	RMSE (Volts)
Mean=0 Variance=1	0.0006938
Mean=1 Variance=0	0.0006171
Mean=1 Variance=1	0.0006967

TABLE II. COMPARISON OF CHARGE PUMP OUTPUT DUE TO NON-LINEARITIES IN VCO

The above Table II shows error induced in the output of the charge pump relative to phase noise being added to VCO. The errors are relative to charge pump output with the ideal condition (Mean=0 and Variance=0 of noise). From this test, we can conclude that having variance=1 produced more Root Mean Square Error (RMSE) than having mean=1 for a noise modeled as Gaussian Random Distribution and added as voltage. Hence, while designing the system and performing its statistical analysis, we must try to focus on getting the least variance before the least value of the mean.

Comparative Results:

We compare our simulation results with state-of-the-art systems of other manufacturers. Out of many other similar radar chips, we found Long Range and Ultra-Short-Range chips for Linear FMCW radar applications best in the class. We present a comparative study of these two, with results corresponding to our own proposed design in Table III below. The figures of merit of radar are the maximum unambiguous range, range resolution, maximum unambiguous velocity, and velocity resolution. The table below discusses these on a comparative scale. It also shows a comparison of other parameters such as chirp duration, number of chirps in a frame, samples per chirp, and frame time. These parameters, although are not figures of merit for a radar directly but these values are essential for comparison of designs for various aspects such as computability, design costs, technology to be used, and so on. Hence, these parameters are included in the comparative study of the proposed design with state of the art commercial FMCW radar.

Parameter	Long Range (Texas Instruments)	Ultra-Short Range (Texas Instruments)	Proposed System (Simulation Results)
Max Unambiguous Range (m)	225	22.5	4000
Range Resolution (m)	0.5	0.1	0.04
Chirp Duration (μsec)	30	50	10
Number of Chirps in a frame	256	128	1024
Max Unambiguous Velocity (Kmph)	92.28	35.30	131.52
Velocity Resolution (Kmph)	0.72	0.55	0.25
Samples per Chirp	500	250	100000
Frame Time (msec)	9.728	12.8	28.87

TABLE III. COMPARATIVE RESULTS WITH STATE-OF-THE-ART SYSTEMS

Comparative results show that the proposed design performs better in terms of radar maximum unambiguous range, radar range resolution, maximum unambiguous velocity, and velocity resolution using a single PLL. The system design, however, is also computationally expensive. This issue is not going to affect the simulation results drastically when fabricated due to the advancements of processors for GigaHertz based processing along with pipelining.

CHAPTER 4: CONCLUSION

A new technique for the generation of a high-frequency resolution chirp signal using a single fixed frequency phased locked loop is presented. The proposed method involved taking the output from the intermediate stage of the PLL as the clock input to the digital control block to obtain a high-frequency output chirp signal that will be used as the radar transmitted waveform.

The solution presented is a complete technology-independent digital solution with minimal computation elements and design overhead. The design maintains compatibility with the current constraints of fabrication. All components used in the design are synthesizable. The frequency of operation for the internal lookup table is identical to state-of-the-art lookup tables in the industry. Simulation results, provided in the thesis, demonstrate a proof-of-concept of the proposed design.

The linearity of the chirp signal has been tested statistically by using curve fitting with a first-order polynomial and estimating the root mean square error of the observations with the modeled best fit line. Another test was performed to analyze the effect of non-linearities in the VCO. In this test, the VCO is added with phase noise modeled as a Gaussian random variable. Combinations for mean and variance of noise voltage have been considered. The output of the charge pump in those cases has been analyzed. The results show a couple of things. Firstly the error due to this noise with respect to the ideal situation is extremely low because of compensation provided by the Phase Frequency Detector. Secondly, an increase in variance has a more significant effect on error compared to the increasing mean of the Gaussian Random Noise.

The future work of this project shall be to test the design with a silicon tested phase-locked loop. This shall be followed by providing compensation methods to variances in different corners for the transistors. The next milestone shall be implementation using Register Transfer Language followed by synthesis of the netlist, placement and routing, timing and parasitic analysis, and lastly, tape out the chip, testing, and validation of results on the practical chip. The next milestone after tape out would be to use the chip along with power amplifiers and phased array radar antennas and chips to implement the complete FMCW radar. The roadmap shows an effective way of generating high-frequency resolution chirp signals using minimum cost in area and analog portion, thus reducing the cost of radar and increasing the quality of the signal being generated.

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