LOW POWER LOW PHASE NOISE LC VCO FOR SUB GHZ RANGE IN 40nm TECHNOLOGY

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CERTIFICATE

This is to certify that the thesis titled " **LOW POWER LOW PHASE NOISE LC VCO FOR SUB GHZ RANGE IN 40nm TECHNOLOGY**" being submitted by **Sapna Sharma** to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original research work carried out by her under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

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Abstract

One of the most widely used blocks in Communication System design is Phase locked loop (PLL). PLLs are used as clock generators, frequency synthesizers, clock recovery in microprocessors and many other applications. The key block in design of PLL is the Voltage Controlled Oscillator (VCO). Latest gadgets like smartphones, smart watches, televisions, car electronics are synced to a clock generated by VCO.

This thesis focuses on design of LC voltage-controlled oscillators on 40nm technology. With the technology being scaled down, the supply voltage is also scaled down to prevent device breakdown. This results in reduced output swing and degraded phase noise. The quality factor of the LC resonator is low at higher frequency which makes it very difficult to design a low voltage VCO. The main challenges are phase noise, area, performance and variations.

This thesis presents the design of low power, low phase noise LC VCO at 800MHz output frequency. The design is implemented on 40nm technology at 1.31V supply voltage achieving a phase noise of -131.7dBc/Hz. The power consumption is 4.3mW. The PVT variations of the design are 4% of nominal value for frequency and 6.8% of nominal value for phase noise. Monte Carlo analysis is also carried out and results are reported.

Chapter 1

INTRODUCTION

This chapter provides the motivation and objective behind the present work. In this work a low power low phase noise LC VCO at 800MHz output frequency is implemented on 40nm technology. The design steps, problems encountered, and solutions are discussed in subsequent chapters. We have designed an LC VCO at 3.2GHz frequency and used divider circuit to achieve 800MHz output frequency.

1.1 MOTIVATION

The rapid growth in wireless communication has led to an increased demand for fully integrated low power, small size RF transceivers. To reduce the noise of the overall system, RF front end is designed with minimum noise. This way the noise requirement from the baseband amplifiers and filters can be relaxed. Very low phase noise local oscillators prevent the degradation of signal-to-noise ratio. Phase Locked Loop (PLL) frequency synthesizer is one of the key blocks of RF system. PLL is a circuit that synchronizes two signals both in frequency and phase. One of the signals is an output signal from the oscillator and other one is reference or input signal. In synchronized state, or locked state, the phase error between the two signals is zero or a constant. In other words, the phase of the output signal is locked to the phase of the input signal, hence the name phase locked loop[1].

VCO is an important block of PLL. In a VCO the oscillator frequency is controlled by input voltage. VCO is main contributor to phase noise and power dissipation of entire PLL circuit. Hence VCO must be designed to have minimum possible phase noise and power dissipation.

This project aims at building low power low phase noise VCO which works at sub GHz frequency. This kind of a design offers multiple advantages, such as lower data rate, use of pre-existing 2G infrastructure.

Lower data rate is directly tied to more power efficient designs. This means a single coin cell battery should be able to sustain the sensing nodes for a very long time of the product cycle. The existing infrastructure for 2G will ensure the cost of implementation is kept to minimum and also the design can be deployed quite early compared to other

frequency band. Also, sub GHz band can be exploited to transmit the signal at a much longer distances compared to the conventional Bluetooth. Based on these calculations, the project aims to design a sub GHz, low power low phase noise VCO for smart cities application.

1.2 OBJECTIVE

Objective of the project are as follows:

- To design a LC VCO core at 3.2GHz frequency with low phase noise and low power dissipation.
- To design other blocks like capacitor bank for tuning and divider block to achieve the desired frequency of 800MHz.
- To analyze the type of transistor, resistor and capacitor to be used in order to have minimum PVT variation and area.

1.3 ORGANISATION OF THESIS

The rest of the thesis is organized as follows. Chapter 2 discusses about Phased Lock Loop and gives a brief introduction on it's blocks. Chapter 3 presents the literature review and theory of LC VCO. Chapter 4 discusses the design of LC VCO, challenges faced and solution. Chapter 5 presents the simulation results. Chapter 6 presents the future work and achievements of this work.

Chapter 2

PHASED LOCKED LOOP

This chapter includes discussion of PLL and its blocks. A brief introduction of PLL and blocks is discussed. Oscillators are discussed in detail and a comparison between ring and LC VCO is presented.

2.1 INTRODUCTION TO PLL

In 1965, Linear Phase Locked Loop (LPLL) came into the picture and PLL was considered to be a linear circuit. After few years, in 1970, Digital Phased Locked Loop (DPLL) became available. Looking closely at the schematic of the DPLL, it was observed that it contains both digital and analog blocks and can be considered as a hybrid block. The two categories, LPLL and DPLL, are unified and commonly known as "mixed signal PLL" for the sake of simplicity.

PLL circuit helps a system to track with another one. It is a synchronizer that synchronizes the frequency coming from local oscillator to a reference or input frequency. The synchronization is both in terms of frequency and phase. In synchronized state, also called locked state, the phase error is zero or constant. There are instants when the phase error is not constant or zero. In that case a control mechanism is deployed to reduce the phase error to zero or to a minimum possible[2].

2.1.1 BLOCKS OF A PLL

A PLL consists of phase frequency detector, charge pump, loop filter, VCO and frequency divider. Fig. 1 represents the block diagram of a PLL.

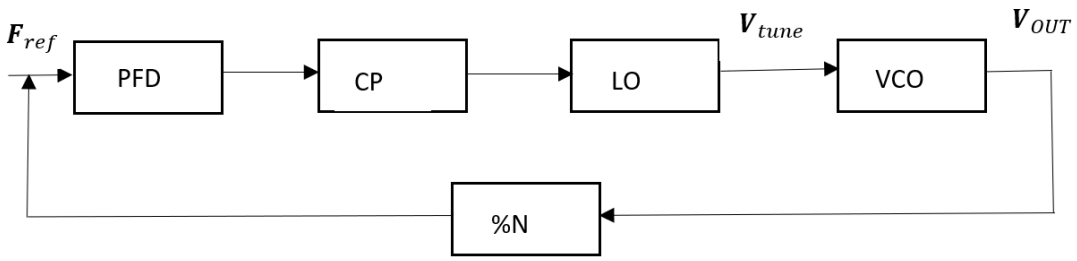

Figure 1 Blocks of PLL

Phase Detector (PD) is a circuit that generates an output signal proportional to the phase difference between the two input signals. Phase Frequency Detector (PFD) is a circuit whose output depends on both phase error and frequency error before the PLL has acquired lock. The PFD circuit can be realized using D Flip Flops. Based on whether the reference frequency is higher or lower than the feedback frequency, PFD generates “up” or “down” signal. The generated signal decides whether the VCO’s frequency needs to be pulled up or down. This signal goes to next block, charge pump.

The charge pump is a circuit that is used to achieve a higher voltage. It can be realized using capacitors and diodes. Based on the signal received from PFD, charge pumps either drives the current into the loop filter or draws current from the loop filter. If the signal received is “up” then the current is driven into the loop filter and when the signal is “down” the current is drawn from the loop filter.

Loop filter is a low pass filter that suppresses the higher frequencies and allows the lower frequencies to pass. In most of the designs the loop filter (LP) is first order low pass filter. Based on the signal received, up or down, the loop filter generates a voltage known as “control voltage”. The control voltage is fed as an input to the VCO. This voltage controls the frequency of oscillation of the VCO. The frequency is increased when the signal is up and decreased when the signal is down. The frequency is increased/decreased until the reference clock and feedback clock frequency and phase are same. This is when the VCO stabilizes [3].

A divider circuit may be used in the feedback loop. This will increase the VCO output frequency above the reference frequency by a factor of ‘N’.

$$V_{OUT} = N.F_{ref}$$

2.1.2 TYPES OF VCO

There are two types of oscillator based on the type of waveform produced.

1. Harmonic Oscillator
2. Relaxation Oscillator

Harmonic oscillator produces sinusoidal output waveform whereas relaxation oscillator produces triangular or square output waveform. LC VCO is an example of harmonic oscillator whereas ring oscillator is an example of relaxation oscillator. The

advantage of harmonic over relaxation oscillator is frequency stability with respect to temperature, noise and power supply. The tank circuit of harmonic oscillators ensures good frequency control [4].

A study of both types of VCOs is done and comparison table is presented In Table 1.

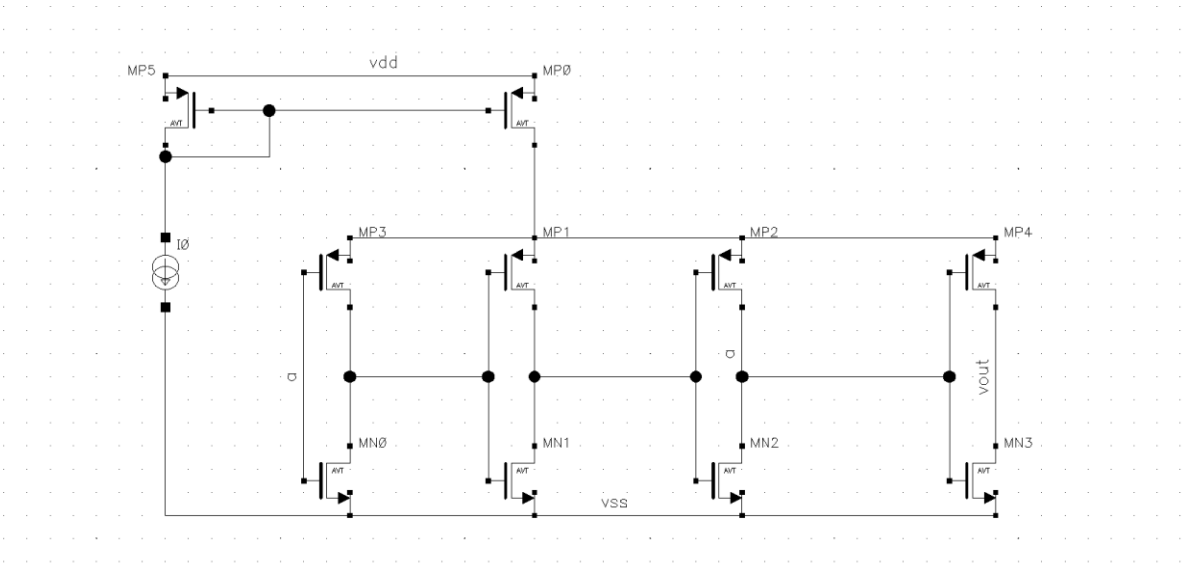

Figure 2 Ring Oscillator Circuit

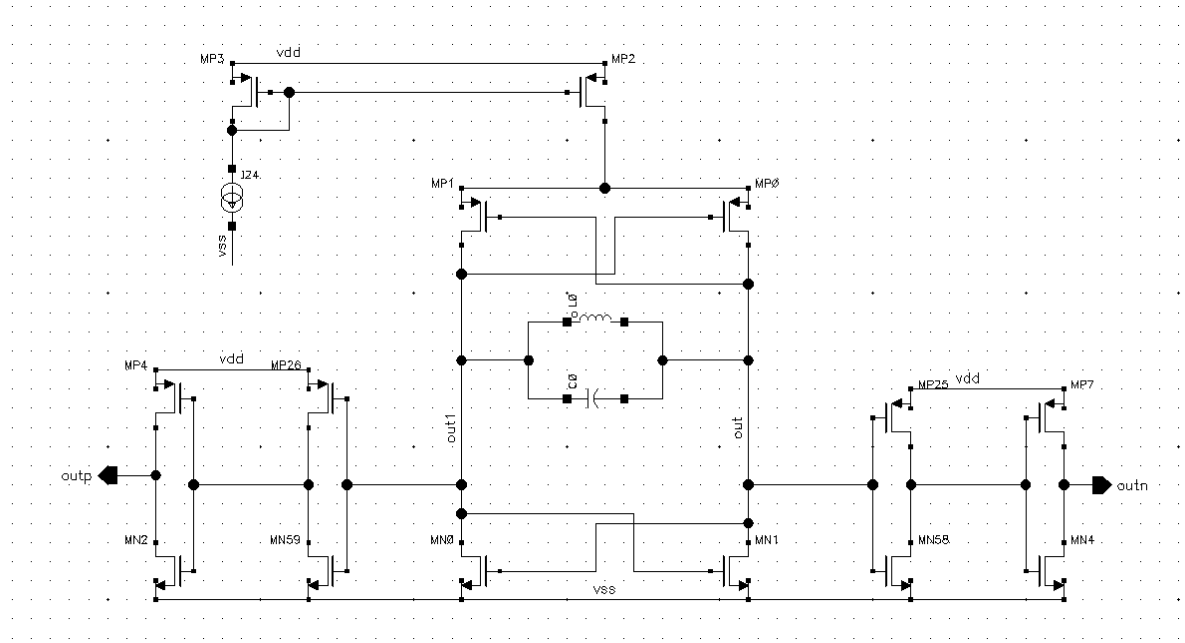

Figure 3 LC VCO circuit

Ring oscillator and LC VCO is implemented in 40nm technology at 1.31V supply voltage. The frequency of oscillation is 3.2 GHz. Figure 2 represents the circuit diagram of ring oscillator and figure 3 represents the circuit diagram of LC VCO.

Table 1 Comparison between RO and LC VCO

S.NO	PARAMETER	RING OSCILLATOR	LC VCO
1.	Technology	40nm	40nm
2.	Supply	1.31V	1.31V
3.	Target Frequency	3.2GHz	3.2GHz
4.	Bias Current	45uA	2mA
5.	Current Consumption	105uA	3.9mA
6.	Power Dissipation	.137mW	5.1mW
7.	Phase Noise @ 1MHz	-77dBc/Hz	-123.3dBc/Hz

From the comparison table it can be concluded that the choice of oscillator depends on the application targeted. Ring oscillator dissipates less power but has poor phase noise. LC VCO dissipates more power but has fairly good phase noise numbers. For low power applications ring oscillator is preferred over LC VCO. For applications involving stringent noise requirement LC VCO is preferable.

Chapter 3

LC VCO

An oscillator gives a periodic output. It uses a self-sustaining mechanism that allows its own noise to grow and become a periodic signal. From the discussion in chapter 2, we can say that LC VCO has better noise performance than other oscillators. However due to the use of inductor, LC VCO needs more area than other oscillators. Inductor occupies almost half of the area. In order to reduce the area generally, VCO core is designed at higher frequency. This is to keep the inductor value and hence it's size to the minimum. Divider circuit maybe used to achieve the required output frequency.

The LC VCO is based on the principle of resonance. L and C produces resonance and sets the frequency of the oscillator. The frequency can be given by the formula,

$$1/2\pi\sqrt{LC}$$

Ideally in parallel resonant circuit the admittance of the inductor and capacitor are equal and opposite creating infinite impedance at the resonance frequency. In non-ideal cases the inductor has some series resistance and capacitance a shunt resistance. The quality factor 'Q' of inductor can be defined as the ratio of inductor reactance to series resistance and that of capacitance can be defined as the ratio of capacitive reactance to shunt resistance. Resistance can be given by the formula,

$$R = L\omega/Q \quad \text{for inductor}$$

$$R = 1/\omega QC \quad \text{for capacitor}$$

Generally, capacitors have very high Q (in hundreds) and inductors have small Q (in tens) so the shunt resistance of capacitor can be neglected. The overall tank circuit considering series resistance of inductor can be presented as shown in fig. 4.

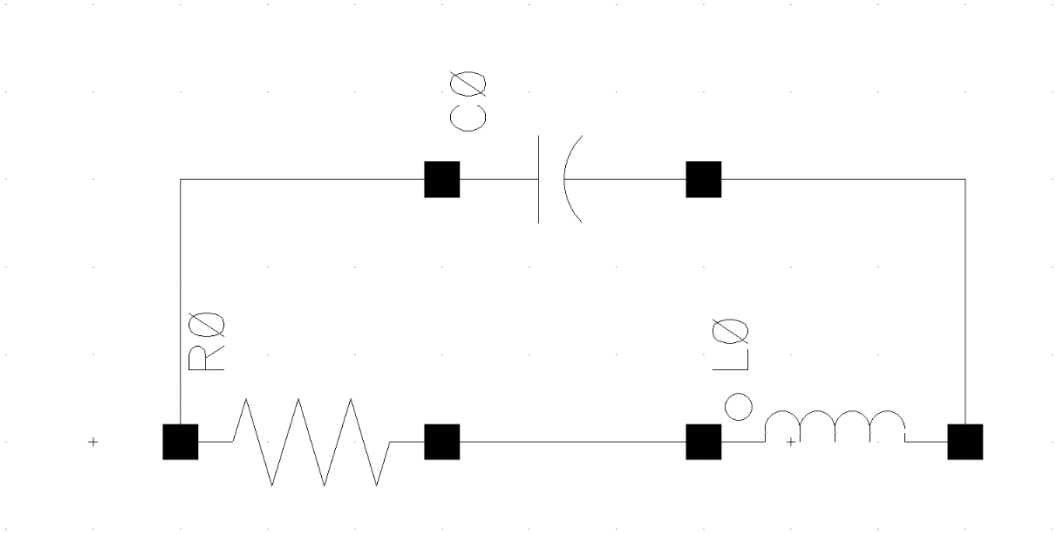

Figure 4 LC circuit with series loss resistance

For simplicity in calculation we convert the series resistance to equivalent shunt resistance. For two resistances to be equivalent,

$$(L_S + R_S) = {(R_P L_P S)}/{(R_P + L_P S)}$$

Substituting $S = j\omega$,

$$(L_S R_P + L_P R_S)j\omega + R_S R_P\text{-}L_S L_P \omega^2 = L_P R_P j\omega$$

If,

$$(L_S R_P + L_P R_S) = L_P R_P \text{ and } R_S R_P - L_S L_P \omega^2 = 0 \text{ then,}$$

$$R_P = {L^2{}_S \omega^2}/{R_S} \text{ since } L_P \approx L_S, \text{ and } L_P = L_S\left(1 + \frac{R^2{}_S}{L^2{}_S \omega^2}\right) \text{ [5]}$$

The circuit can be now represented as in fig. 5.

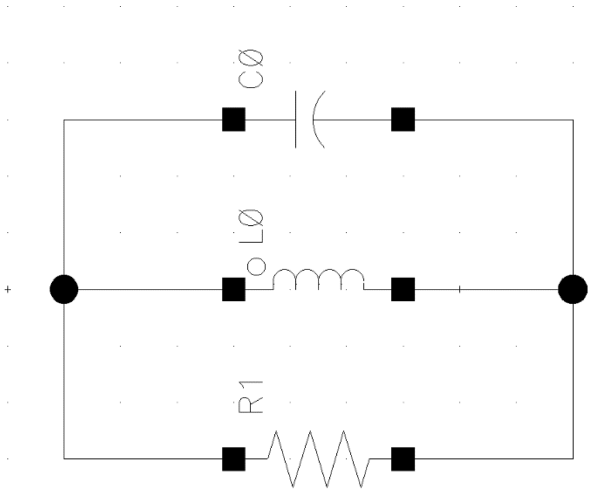

Figure 5 Series loss resistance converted to parallel resistance

Due to this resistance of inductor, the oscillations induced in the tank circuit decays with time. To sustain the oscillations induced, negative resistance should be provided in parallel to R_P so that, $R_P//-R_P = \infty$. The circuit in fig. 6 represents parallel resistance and negative resistance.

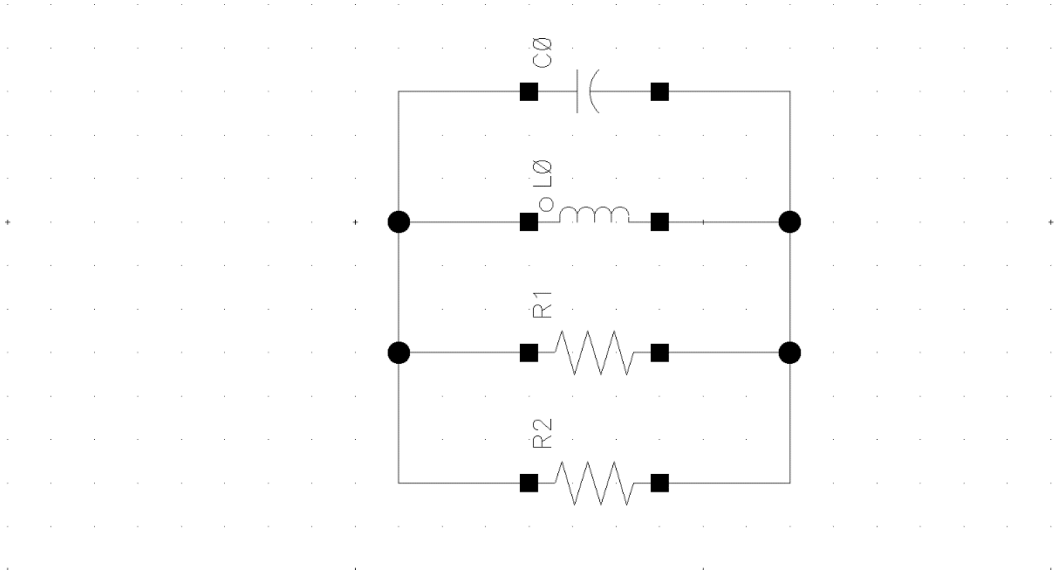

Figure 6 Parallel resistance and negative resistance

Negative resistance can be obtained by two cross coupled transistors in positive feedback as shown in fig. 7.

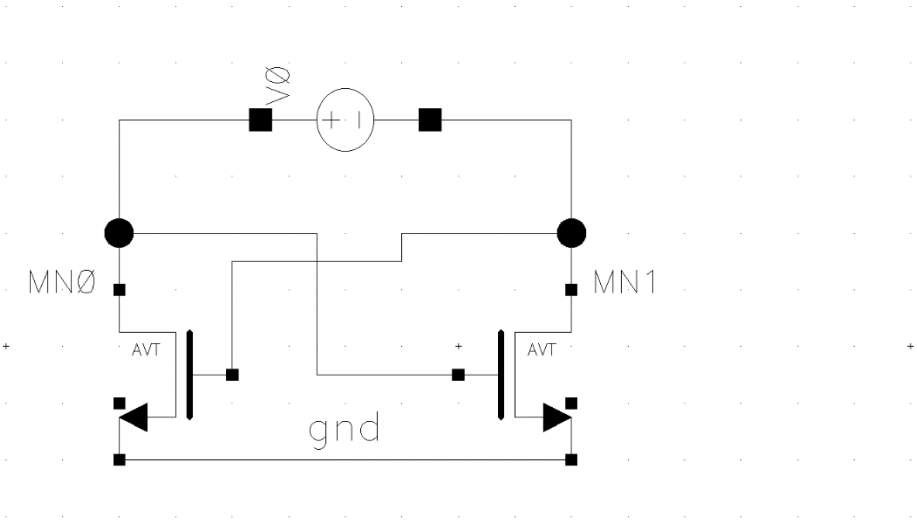

Figure 7 Negative resistance circuit

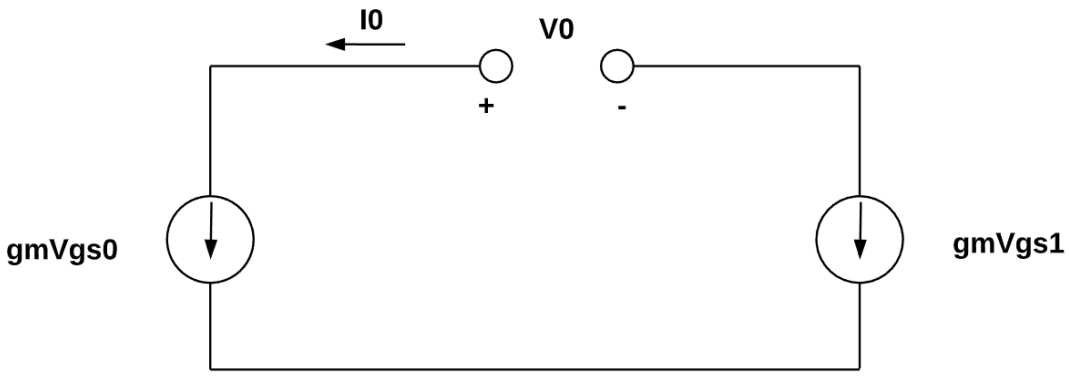

Figure 8 Small Signal equivalent circuit

From the small signal equivalent circuit in figure 8,

$$V_0 = V_{gs1} - V_{gs0}$$

And,

$$I_0 = -g_m V_{gs1} = g_m V_{gs0}$$

Since the transistors are ideal,

$$V_{gs0} = -V_{gs1}$$

Hence,

$$V_0 = 2V_{gs1}$$

The equivalent resistance can be given as,

$$R_{eq} = \frac{V_0}{I_0} = \frac{2V_{gs1}}{-g_m V_{gs1}} = -\frac{2}{g_m}$$

Addition of negative resistance to the circuit will ensure proper and sustained oscillations.

3.1 LITERATURE REVIEW

With the advent of technology, cities are becoming smart cities. Every device is connected to internet to make life more comfortable. For example, cars have embedded RF chips in them. These chips allow the communication from certain distance enabling a person to control the features. These devices are synced to clock which is generated by VCO.

For smart city applications noise is a stringent criterion for design of LC VCO. Reducing the noise of the oscillator has been a prime concern for the researchers in the past. In [6], DAC has been used to cancel the noise from the loop filter. In this solution there is a trade-off between area, noise and performance. Due to use of DAC the overall performance is limited by linearity and resolution of DAC. It also increases the overall area of the circuit.

In [7], digital noise cancellation is proposed by using time-to-digital converter (TDC). It does not require the use of DAC but TDC's performance is also limited as it requires linearity, resolution and matching.

Researchers have reported several low voltage LC VCO designs in [8-14]. These designs propose solution to achieve low phase noise, low power and area. Most of the solutions revolve around current filter techniques. The limitation of these technique is large area and high PVT variations.

The current work presents a design with high performance, low power, low phase noise LC VCO for sub GHz IOT applications. It provides a solution to above reported problems while maintaining the PVT variations within 7% for both frequency and phase noise.

3.2 LC VCO TOPOLOGY

There are different topologies of LC VCO. Each one of them has certain advantages and disadvantages over others. Based on the application, one can choose the topology.

3.2.1 NMOS TOPOLOGY

NMOS topology as shown in fig. 9, has NMOS cross coupled pair and NMOS tail current source and has high transconductance per unit area. For a given negative resistance NMOS transistor can be smaller than PMOS transistor. This means that NMOS topology can achieve the same negative resistance at lower current than the its PMOS counterpart. Hence NMOS topology is more power efficient than its PMOS counterpart. Another advantage of NMOS topology is that due to its smaller size it can achieve a higher tuning range for the same transconductance value.

This topology is suitable if the phase noise requirement is not stringent. NMOS transistors have higher flicker noise density than PMOS transistors. One more point to note is that PMOS topology filters the supply voltage noise through the impedance of the tail transistor. The supply voltage noise is FM modulated and is another component of phase noise. Hence from Phase noise point of view PMOS topology is much better than NMOS topology [15].

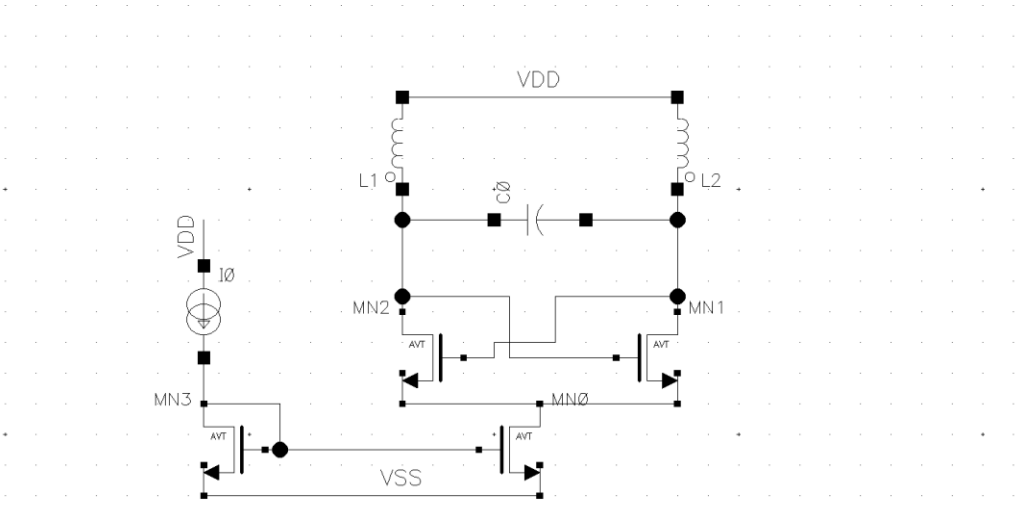

Figure 9 NMOS topology circuit

3.2.2 PMOS TOPOLOGY

PMOS topology as shown in fig. 10, uses PMOS cross coupled pair with PMOS tail current source and is used when noise requirement is stringent. It offers lower phase noise but dissipates more power due to larger size compared to NMOS topology. The

drain current thermal noise which is one of the main components of phase noise is reduced by the use of PMOS transistors. As discussed in earlier section, noise due to supply voltage is also shielded in PMOS topology. The PMOS topology also reduces the noise appearing due to bias of the transistors. All these properties make PMOS based topology a good choice when targeting minimum phase noise [15].

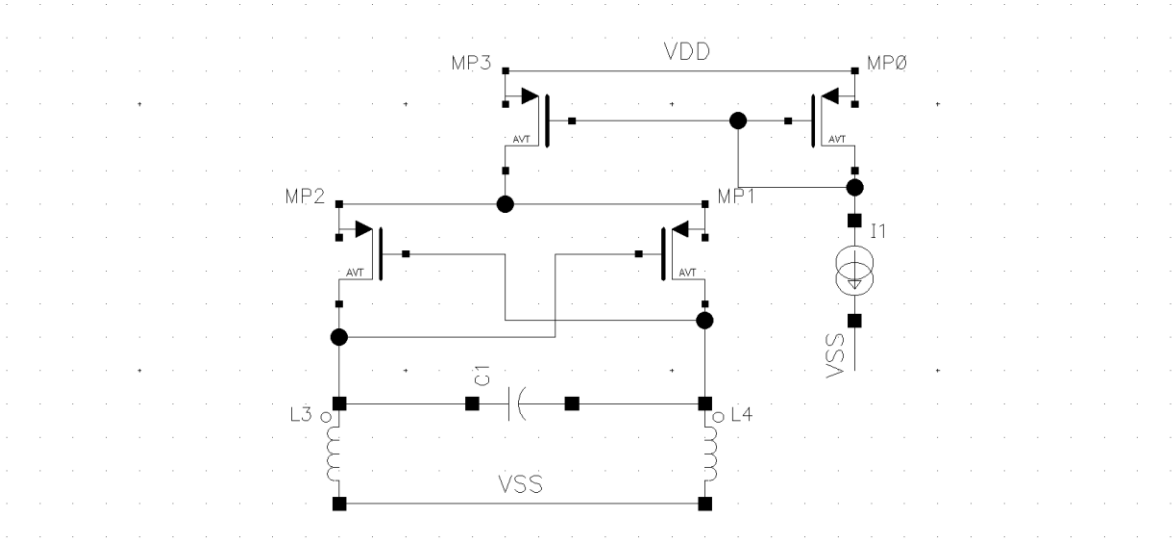

Figure 10 PMOS topology circuit

3.2.3 COMPLEMENTARY NMOS/PMOS TOPOLOGY

Complementary NMOS/PMOS topology as shown in fig. 11, uses both NMOS and PMOS transistors. This topology is suitable only if we have enough headroom to keep every transistor in saturation. This might be difficult at low voltage supply. Advantage of this topology is lower power dissipation. The cascode structure allows us to have same “gm” in less bias current. Less bias current ensures less power dissipation.

Another advantage of CMOS topology is better phase noise. Phase noise is inversely proportional to power dissipation. As this topology uses half the bias current compared to other topologies, the tail current can be increased without much worry of the power dissipation.

This topology offers full swing in the output voltage. Since this topology offers more uniform swing due to use of both NMOS and PMOS transistors, the phase shift introduced during both rising and falling edge will be similar [16].

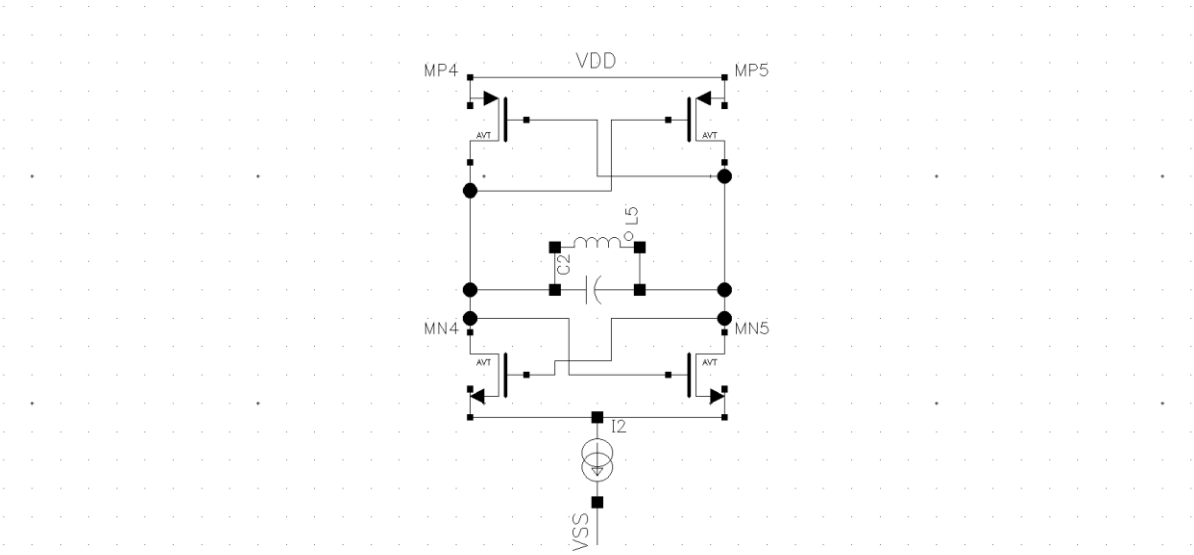

Figure 11 Complementary PMOS/NMOS topology circuit

3.3 PERFORMANCE PARAMETER

VCO is an important block of RF transceiver. It has two main requirements in terms of performance. They are system specification and interface specification. System specification includes parameters like frequency and purity of signal whereas interface specification includes parameters like output swing and drive capability.

3.3.1 FREQUENCY

Frequency of operation of the output comes under system specification. The oscillator must be designed such that it's frequency can be varied over a range, known as tuning range. It is designed such that the oscillator is able to attain the decided tuning range and an additional margin is taken to cover the process and temperature variations.

3.3.2 OUTPUT SWING

The oscillators must produce full-output swing. An oscillator is one of the blocks of PLL and is connected to other blocks. It must have full output swing to ensure complete switching of the transistors in the next stage.

3.3.3 DRIVE CAPABILITY:

The drive capability of the VCO must be sufficiently high so that it can drive blocks which are directly connected to it. For example, in this design the oscillator has to drive the input capacitance of a divider and hence high drive capability of oscillator is required.

3.3.4 TUNING RANGE

Tuning range is the range of frequency which we can achieve by tuning the VCO. The center frequency should be consistent with the frequency of application. The tuning can be done through capacitors. The tuning can be discrete or continuous. Discrete tuning is achieved through discrete cap bank and continuous tuning is achieved through varactor. Both of them are connected in parallel with the fixed capacitor of LC tank. Control voltage helps tuning the VCO [3][17].

3.3.5 PHASE NOISE

Phase Noise is the noise relative to the clean oscillation frequency. For ideal oscillator zero crossing occur at $T_C = \frac{2\pi}{W_C}$

Noise of the oscillator changes the zero crossing of the oscillator randomly. This leads to random variation in frequency of the oscillator which is highly undesirable.

Phase noise is quantified at a certain frequency offset. Bandwidth of 1Hz is considered at an offset of Δf. Power is measured in this bandwidth and the result of carrier power is normalized. It is expressed in units $dBc/_{Hz}$ (dB with respect to carrier/Hz) which signifies normalization of the noise power with respect to carrier power [3][17].

3.3.6 POWER DISSIPATION

VCO block usually consumes most of the power consumed by entire PLL block. Hence it is an important parameter in designing. Other parameters like phase noise, tuning range are also affected by the power consumption so it must be taken into account [3][17].

3.3.7 SUPPLY SENSTIVITY

This refers to the noise that might enter the system through supply voltage. The supply noise can change the frequency of operation of the oscillator which is highly undesirable. The oscillator can suffer from flicker noise and due to its low frequency content it is difficult to remove it by bypass capacitors.

3.4 SUMMARY

In this chapter we discussed about the LC VCO, its topology and performance parameters. The topology should be decided keeping in mind the performance parameter and application of the design. This work targets low phase noise, low power

and low area LC VCO. To achieve low power and low phase noise, complementary NMOS/PMOS topology is chosen. To reduce the flicker noise due to supply sensitivity, PMOS based biasing where the bias current is provided through PMOS transistor has been adopted. Other parameters are taken into account and discussed in the next chapter with design considerations.

Chapter 4

DESIGN OF LC VCO AT 3.2GHz

This chapter discusses about design of LC VCO at 3.2GHz frequency. It discusses about the design consideration, design methodology for core and other blocks. The challenges faced in design and solutions are discussed.

4.1 DESIGN CONSIDERATION

Choosing the devices to design a circuit is one important step in circuit designing. In this project transistors, resistors, capacitors and inductor have been used. The type of devices used affect the overall variation, area, power consumption of the design. In short, entire PPA is affected. Following are the points for selecting the devices used.

- **Transistor:** For LC VCO core and capacitor bank avt (analog Vt transistors) are used. These transistors have higher gm and lower threshold voltage. For the same gm as achieved by any other transistor, these transistors will burn less current hence reducing the overall power dissipation. Due to high gm, these transistors can create enough negative resistance for the LC tank to oscillate at much lower V_{dd} . For divider circuit, svt (standard Vt) transistors have been used. As this is a digital circuit noise margin is an important criterion. With the help of standard Vt transistor, we can achieve better noise margin.

- **Resistors:** Poly resistors with high resistivity have been used. Poly resistors have less variations compared to metal resistors. High resistivity helps in achieving high resistance with minimum area thus saving overall area of the design.

- **Capacitor:** There are mainly two types of capacitors that can be used. They are MIM (Metal Insulated Metal), MOM (Metal Oxide Metal). MIM capacitors are reported to have less variations over PVT and hence preferable. For this work MOM cap has been used as MIM was not available in the library and realization of MIM using MOS transistors could lead to more variations. There were number of MOM capacitors available. Capacitor with very high Q in GHz range was chosen. If the Q of the cap is in 100s, losses due to capacitor is negligible and can be ignored.

- **Inductor:** Inductor with Q value of 15 was chosen from the library for schematic simulations.

4.2 LC VCO CORE

This work aims at designing a low power low phase noise LC VCO at 800MHz. The core is designed at 3.2GHz frequency and then divider circuit is implemented to get the required frequency. From above discussions it is clear that choice of architecture is very important. The architecture was chosen keeping following points in mind.

- For low phase noise PMOS based current biasing was chosen to shield the core from supply noise.
- CMOS topology was chosen to reduce the power dissipation and ensure good output voltage swing.

STEPS OF DESIGNING:

Following are the steps taken for sizing:

- **STEP 1**: An inductor with 'Q' value of 15 was chosen from the library. The frequency of operation is 3.2GHz. The value of series resistance of inductor was calculated according to the following formula.

$$R = {}^{L\omega}/_{Q}$$

- **STEP 2**: The transconductance of the cross coupled transistors was chosen so as to satisfy the following formula.

$$-\frac{2}{g_m} \leq R$$

- **STEP 3**: Tail current was calculated from the following formula,

$$g_m = \frac{2I_d}{V_{gs} - V_{th}}$$

Where V_{gs} is gate-to-source voltage and V_{th} is threshold voltage of the transistor. To ensure that the devices are in saturation, strong inversion, as a rule of thumb the expression following expression was taken.

$$V_{gs} - V_{th} = 200mV$$

Hence,

$$g_m = \frac{I_d}{100mV}$$

So,

$$g_m = 10I_d$$

Or,

$$I_d = \frac{g_m}{10}$$

- **STEP 3**: Having found the value of transconductance and current, core transistors were sized. First paper pen calculation was done followed by tweaking according to the simulator results.
- **STEP 4**: The inverters were sized to ensure that the up resistance and down resistance seen by output node is same. This ensures maximum output resistance. This also ensures that the trip point is in the middle which helps in achieving better noise margin. The inverters perform two main functions in this design. First, they convert the sinusoidal wave to square wave and second, they help in achieving full output swing.

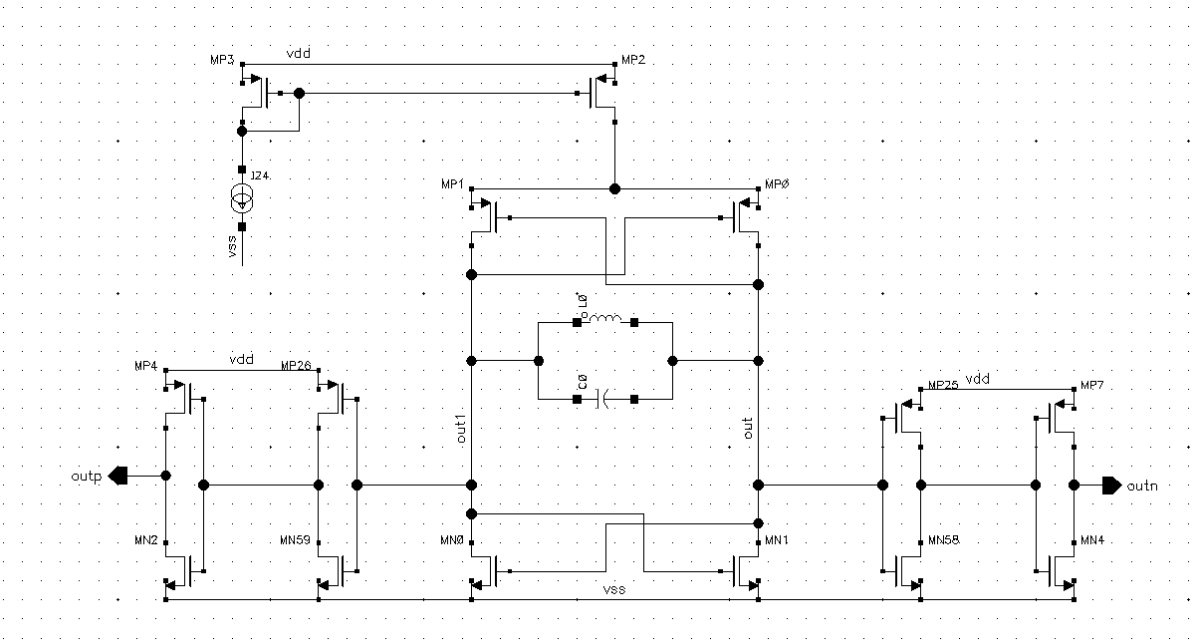

Figure 12 LC VCO core circuit

Fig. 12 shows the circuit of core LC VCO. The circuit gives an output voltage that oscillates at frequency of 3.2GHz.

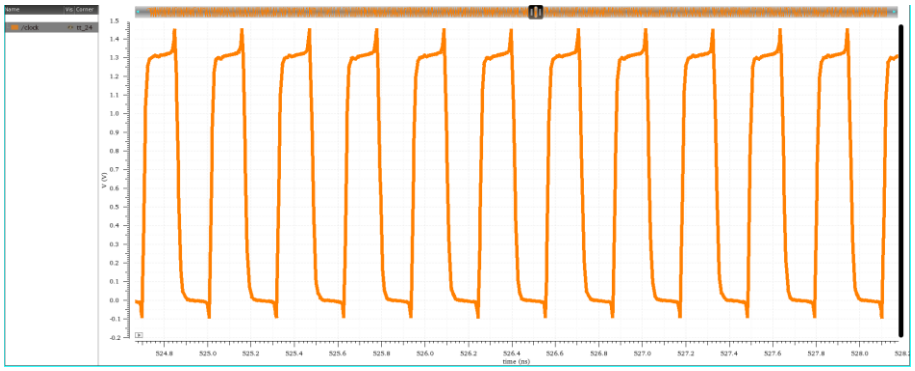

Figure 13 Transient graph of LC VCO core

Fig. 13 shows the transient behavior of the circuit implemented. This is the output received after the inverter stage.

4.3 PROGRAMIBLITY OF LC VCO

This section explains the tuning of LC VCO. It talks about the design challenges and solutions.

TUNING OF LC VCO:

Tuning of the VCO is done to achieve a range of frequencies that the VCO output can provide. In this project the range is 3.14GHz to 3.24GHz. The range is 100MHz. To achieve each frequency in this range we tune the VCO. The first tuning that we do is digital tuning also known as coarse tuning. After that we go for analog tuning also known as fine tuning.

4.3.1 DIGITAL TUNING

Digital Tuning helps us to get closer to the required value of frequency by setting the digital code. For example if we need a frequency of 3.152GHz, we need to set the digital code that can achieve 3.15GHz. Then analog tuning can be done to get the exact value of frequency.

- **Design of cap banks for programmability of VCO:**

  For digital tuning binary weighted cap bank has been implemented. In this design the cap increases by 2X as we move above in the ladder. The tuning range is 100MHz and step size chosen is 2MHz. Hence the number of bits required is 6 ($2^n = 100MHz$). There can be two ways of implementing the cap bank.

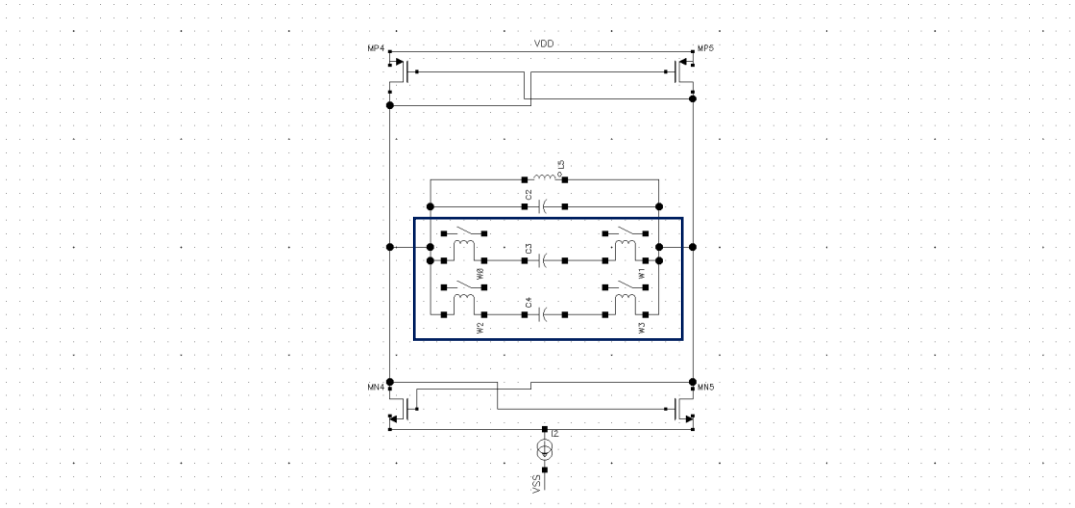

Figure 14 Cap bank structure 1

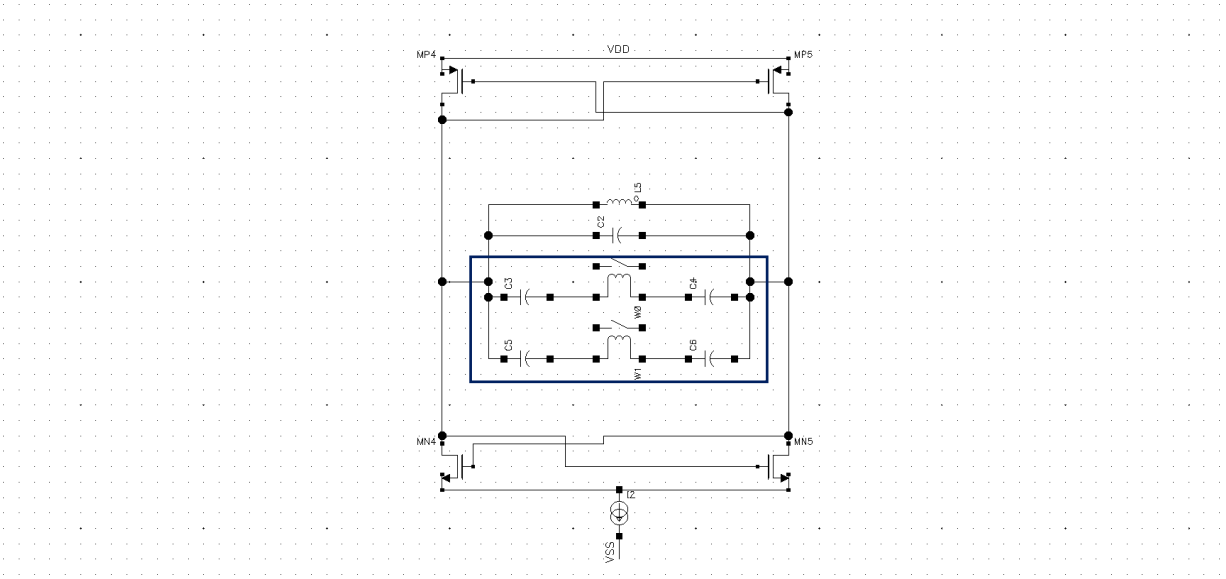

Figure 15 Cap bank structure 2

The highlighted parts in figure 14 and 15 represent the capacitor bank. In fig.14 the switch nodes will be directly connected to the output. This will make the witch resistance change every time the VCO oscillates. This in turn will result in poor Q (quality factor) and oscillations may die out. In contrast in the circuit shown in fig. 15 the switch is isolated from output node of the VCO and hence the above reported problem will not occur. Having decided the type of cap bank for tuning, the next thing to decide is the type of switch.

- **Design of Switch:**

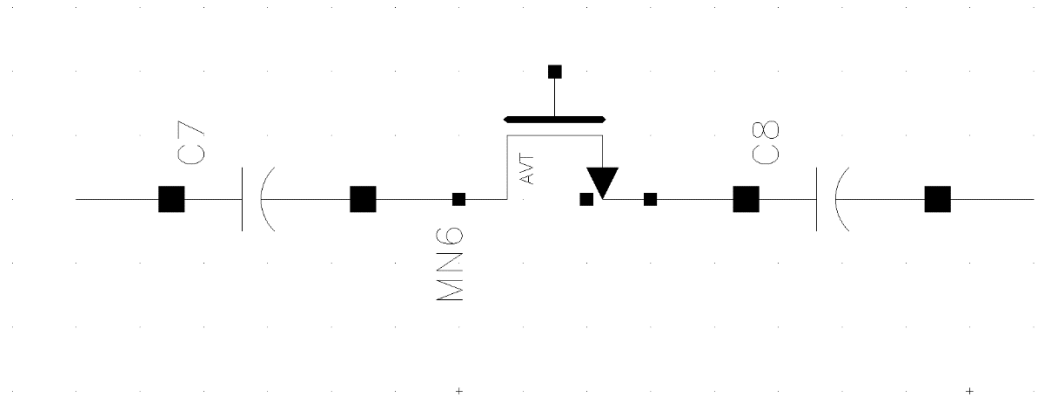

Figure 16 Switch structure 1

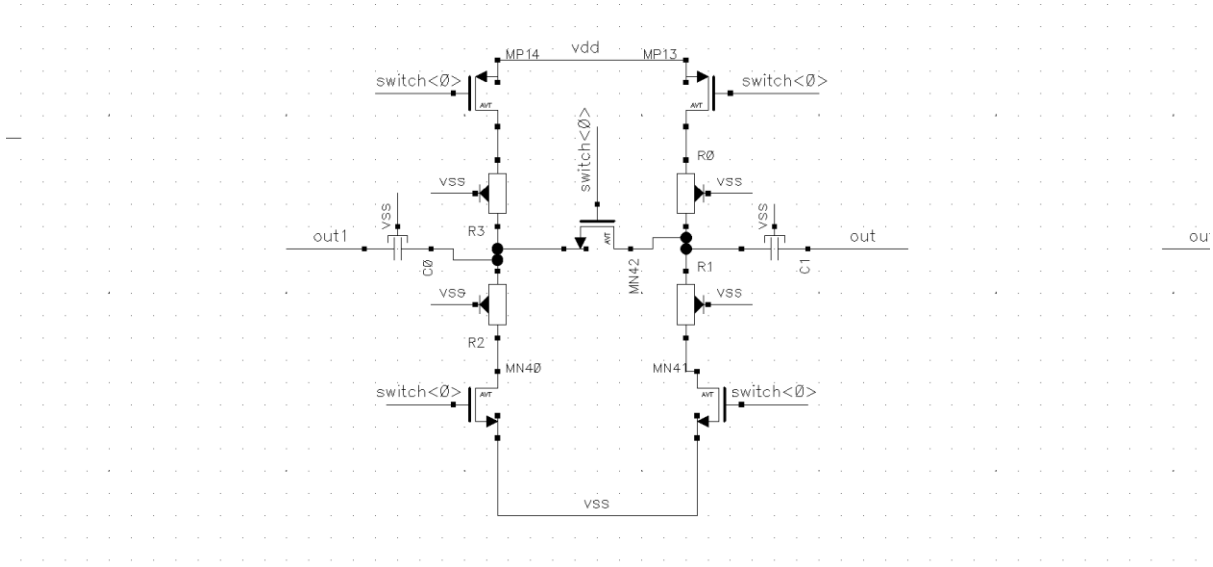

Figure 17 Switch structure 2

In fig. 16, we need low R_{ON} when switch is ON. If R_{ON} is not lower then Q of caps will go down due to higher loss. This needs a larger size of the switch. When the same switch is OFF, we need high R_{OFF} which means the switch size should be small. Small switch size will ensure lower parasitic. We see a direct trade off here.

On the other hand, the switch represented in fig. 17, uses a pull-up/pull-down concept. Here the switch size is kept at a moderate value. When the switch is ON, the pull-down network is also ON. The pull-down network tries to bring the source of the switch transistor to zero whereas the gate is pulled up. Hence the V_{gs} of the transistor increases making R_{ON} low. Similarly, when switch is OFF, pull-up network is ON. The source of the switch transistor is pulled up to V_{dd} when the gate is being pulled down to zero. This way the V_{gs} can be reduced and R_{OFF} can be high.

From above discussion, the choice of switch structure is clear. Having decided the type of cap bank and switch structure we can go for the design of cap bank.

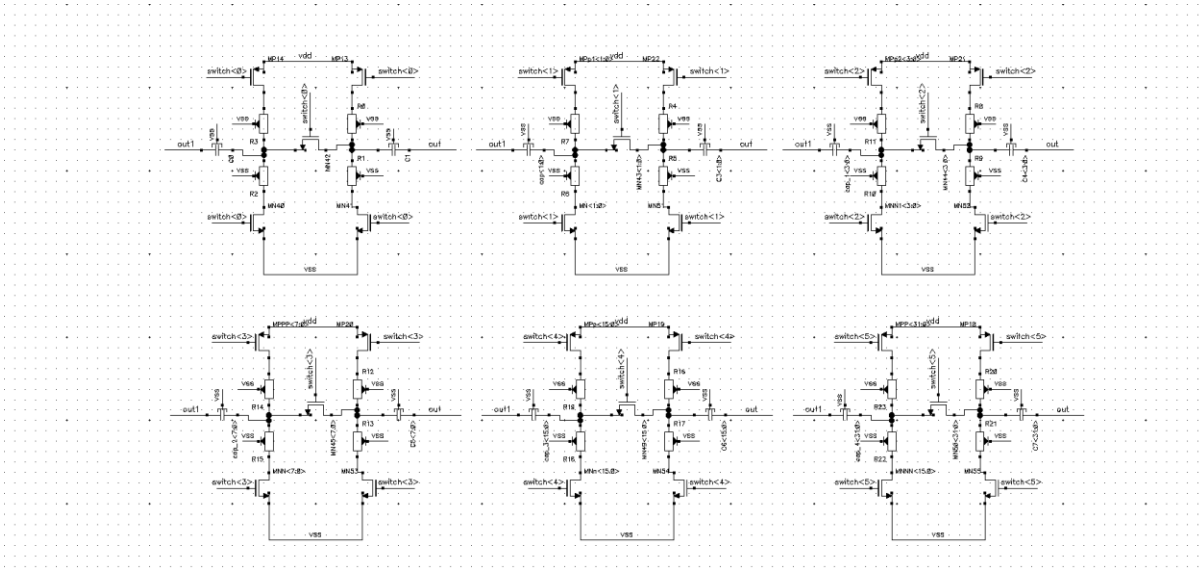

Figure 18 Implemenatiton of cap bank for digital tuning

Fig. 18 represents the cap bank implemented. The digital value of the switch has been changed from 1 to 63 to get the required tuning range.

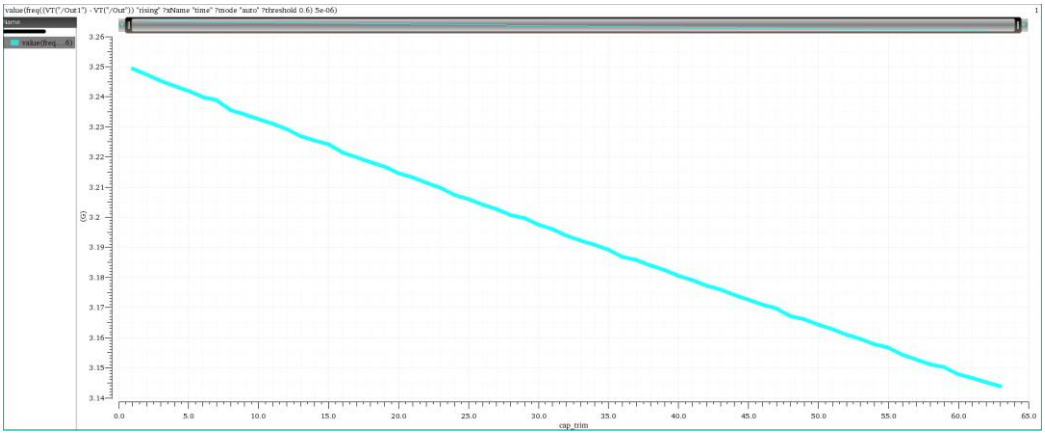

Figure 19 Frequency tuning graph for 3.2GHz

Fig. 19 represents the graph for digital tuning when the cap_trim value is varied from 1 to 63. The tuning range is 3.14GHz-3.24GHz.

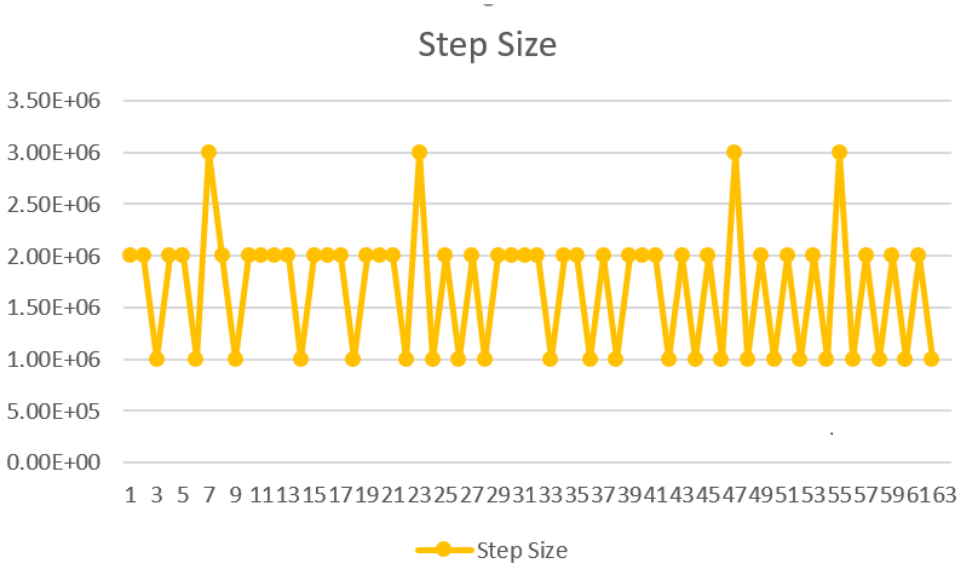

Figure 20 Step size graph for 3.2GHz frequency

Fig. 20 shows the step size graph. The step size is 2MHz at most of the cap_trim values. At some values it varies from 1MHz to 3MHz.

4.3.2 ANALOG TUNING

Through digital tuning we can get the frequency 3.15GHz or 3.16GHz. To get the value 3.152GHz we need analog tuning. Through analog tuning we can achieve all the values between 3.15GHz to 3.16GHz. For this we need a varactor cap whose tuning range is greater than the maximum step size obtained. In current case since the maximum step size was 3MHz, a varactor capable of achieving up to 6MHz of frequency as the tuning voltage is varies from 0 to V_{dd} is implemented.

- **Design of varactor:**

Varactor circuit is back to back connected MOS capacitors and is realized as shown in figure 21. Whenever the voltage applied on MOS is changed, the capacitance of MOS changes. This property is used to get variable capacitance across LC tank. In figure 21, V_{bias} is the tuning voltage which is varied from 0 to V_{dd} to get the desired range capacitance which in turn help in achieving the desired range of frequencies. Varactor is connected parallel to the LC tank.

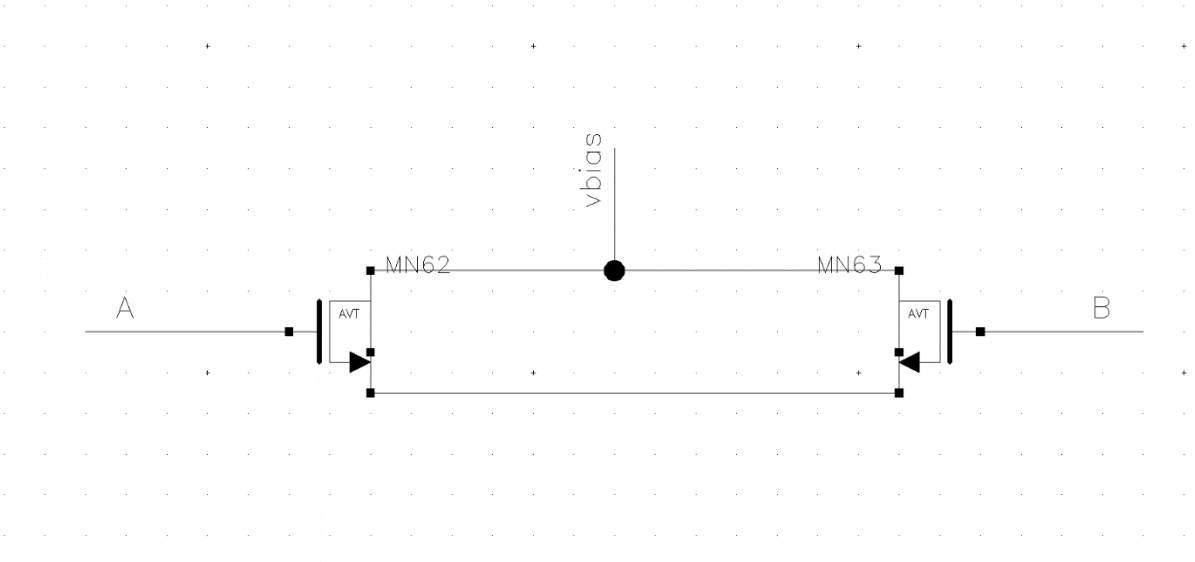

Figure 21 Varactor Implementation

In figure 21, V_{bias} is the tuning voltage which is varied from 0 to V_{dd} to get the desired range capacitance which in turn help in achieving the desired range of frequencies. Varactor is connected parallel to the LC tank.

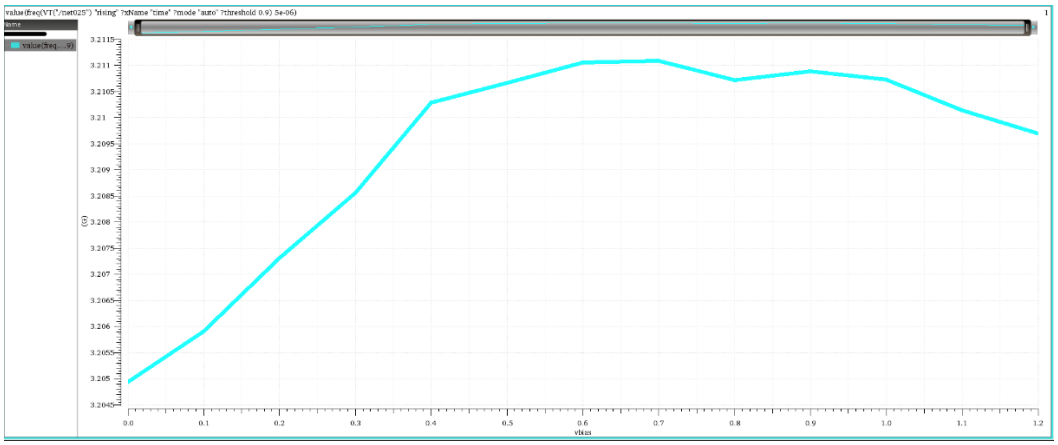

Figure 22 Analog Tuning graph

Fig. 22 shows the output of varactor as V_{bias} , an analog voltage, is varied from 0 to V_{dd}. It can be seen from the graph that by changing the bias voltage one can achieve all the frequencies which could not be achieved through digital tuning alone. The graph represents a condition when inductance, fixed capacitance and digital tuning capacitance are at a constant value and only the bias voltage is changed.

Since the desired frequency for this work is 800MHz, we need to implement a divider circuit. A D Flip flop has been implemented which has been used to further realize the divider circuit.

4.4 DIVIDER CIRCUIT

Divider circuit is used to divide the output frequency of the LC VCO. The output frequency of the core in this work is 3.2GHz and required frequency is 800MHz. Divided by four divider is implemented using TSPC D flip flops.

4.4.1 DESIGN OF TSPC D FLIP FLOP

TSPC (True Single Phase Clock) D Flip Flop is a dynamic flip flop. TSPC D Flip Flop has better power delay product (PDP) compared to the static D flip flops. At very high frequencies, GHz, static D flip flops become very slow hence TSPC is a better choice for high frequency circuit design [18].

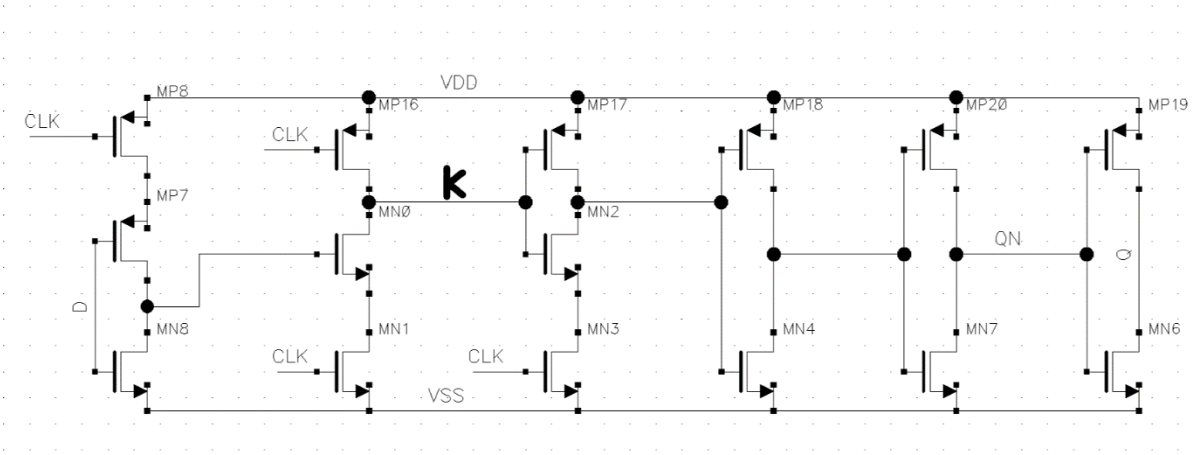

Figure 23 Implementation of TSPC D Flip Flop

Fig. 23 shows the circuit design of a TSPC D Flip Flop. When the clock is low, node 'K' is pre-charged and the input is isolated from output node 'QN'. In this case output node retains its previous value. When clock is high, there is no effect on node 'K'. In this case also the input is isolated from output. Hence, in the stable state of the clock, either high or low, the input and output are isolated from each other. When there is a transition of the clock from low-to-high, the input is latched and the input will be passed to the output.

4.4.2 DESIGN OF DIVIDED BY FOUR CIRCUIT

One D flip flop can give divided by two output. To get divided by four, two D flip flops are used. The input to the first flip flop is clock generated by core of LC VCO. The second flip flop receives the output of the first clock as input. The output of the second flip flop gives final divided by four output.

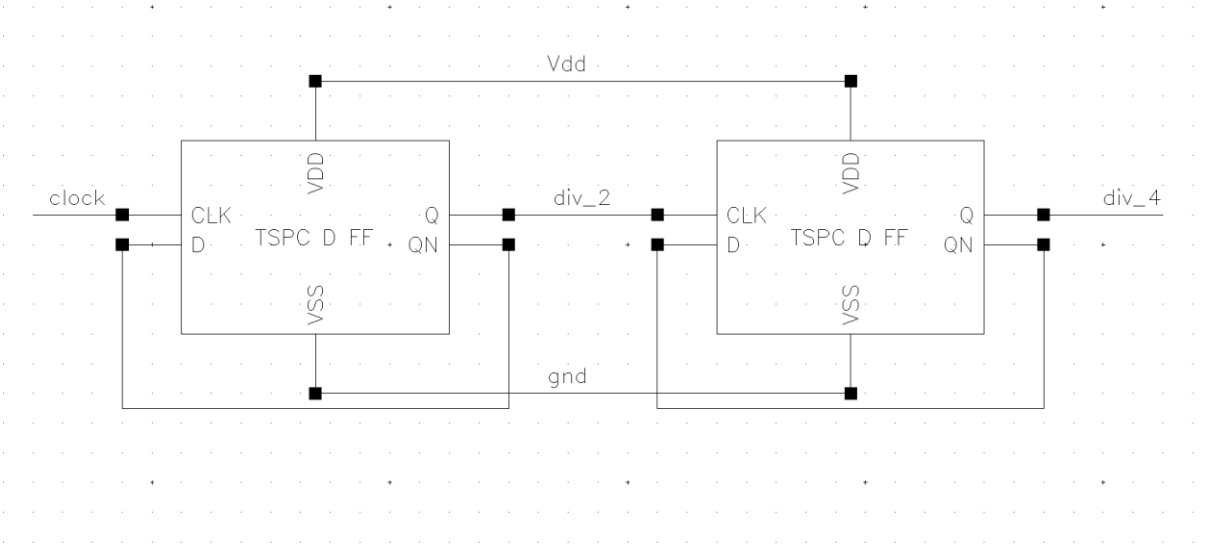

Figure 24 Implementation of divided by four circuit

Fig. 24 shows the implementation of the divided by four circuit. Here clock is the output of the VCO core. Clock gives frequency of 3.2GHz, Div 2 gives 1.6GHz and div 4 gives the desired frequency of 800MHz.

4.5 REALISATION OF FINAL CIRCUIT

All the blocks designed are connected to realize the final circuit.

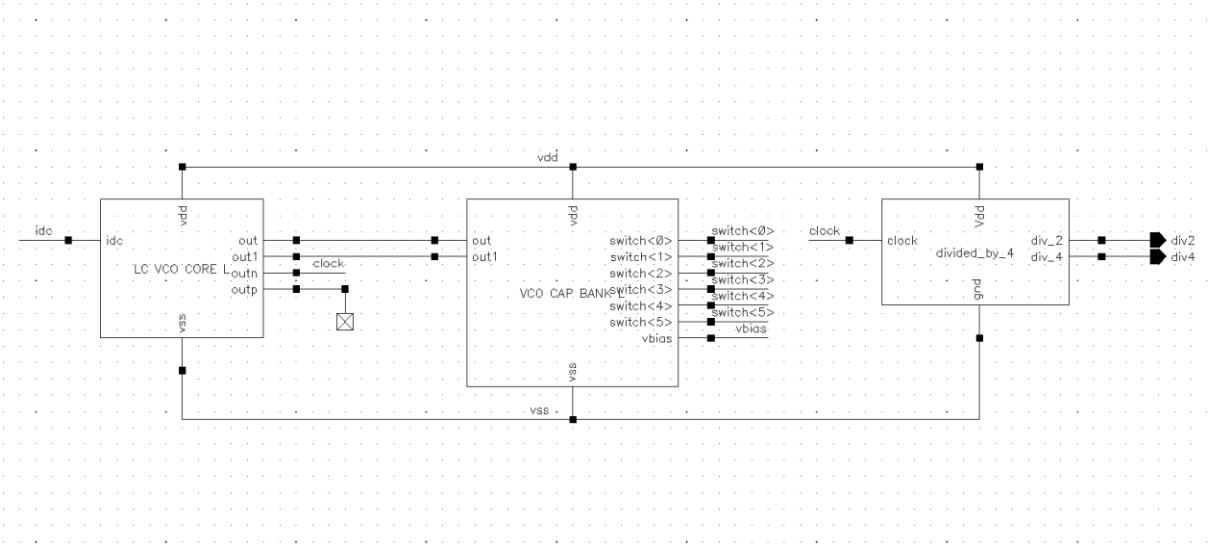

Figure 25 Integration of all blocks and realization of final circuit

Fig. 25 shows the realization of final circuit.

Chapter 5

SIMULATION RESULT

This chapter contains the simulation results of the final circuit realized. It contains the transient response, PVT variation and Monte carlo simulation result of both tuning range and phase noise.

5.1 TRANSIENT

The transient response of the circuit is shown. Clock is the output of the core LC VCO oscillating at 3.2GHz. Div2 and Div4 are the divider outputs oscillating at 1.6GHz and 800MHz respectively.

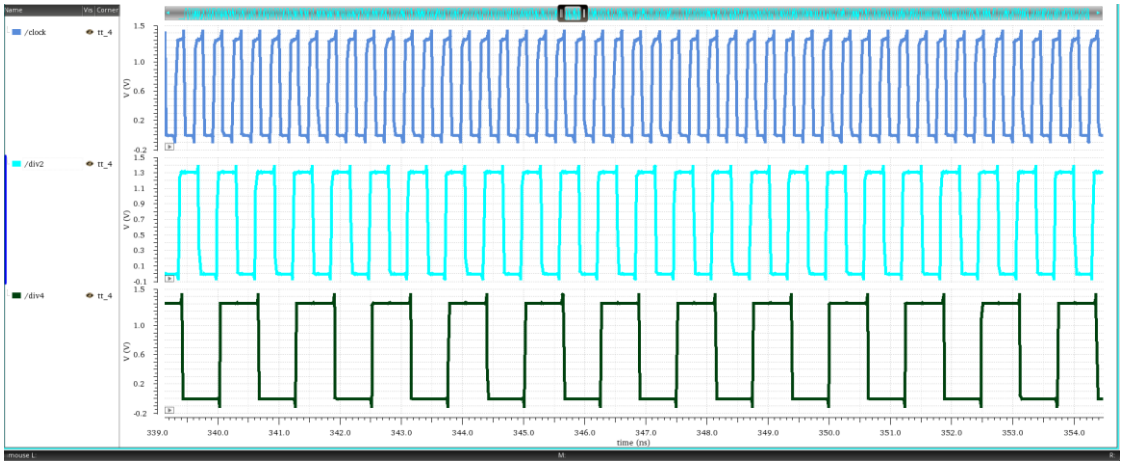

Figure 26 Transient graph of LC VCO implemented

Fig. 26 represents the final output of the circuit after integration

5.2 TUNING RANGE

Digital tuning range of the circuit is 792MHz-816MHz as can be seen from fig. 23 The trim bit value is varied from 1 to 63 to achieve different frequencies of tuning range.

5.2.1 NOMINAL

This section presents the simulation result of circuit for nominal case. Nominal case is when supply voltage is 1.31V, temp is 25C, process is typical.

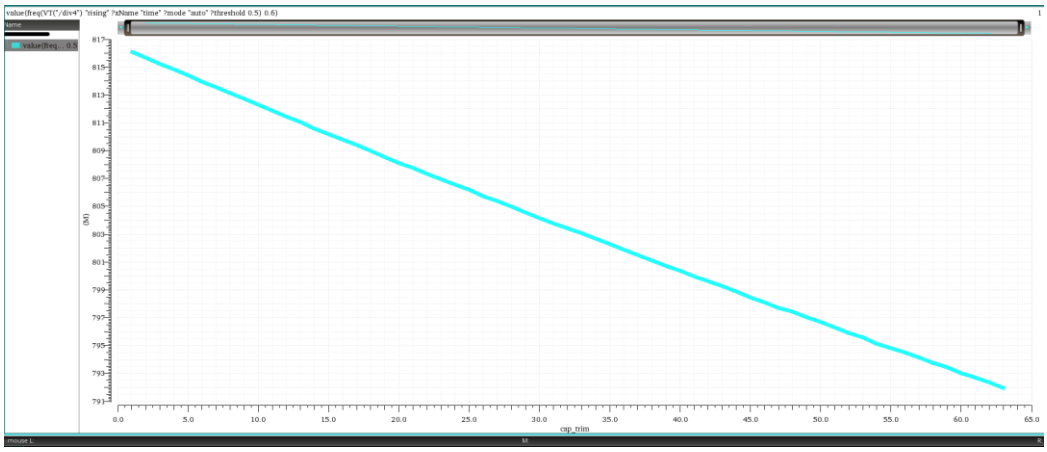

Figure 27 Frequency tuning graph of LC VCO implemented

Fig. 27 represents freq. Vs. Cap_Trim graph for final output of 802.6MHz. The Cap_Trim value is varied from 1 to 63 to achieve the desired frequency range.

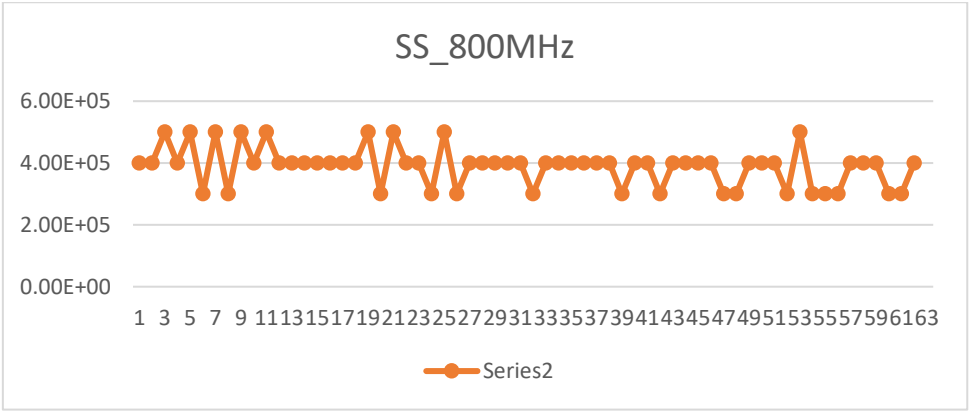

Figure 28 Step size graph 800MHz output

Fig. 28 shows step size graph for 802.6MHz. Step size is the frequency jump from one trim bit value to another. The expected step size for this design is 0.4MHz and it varies between .5MHz to .3MHz.

5.2.2 ACROSS PVT

This section provides simulation result of the circuit across PVT. Monte Carlo simulations covers the PVT mentioned above and the mismatches. PVT is checked for following corners, voltages and temperatures:

Corners: SLOW, SS, SF, TT, FS, FF, FAST

Voltages: 1.18, 1.31, 1.44 (+/- 10%of Nominal Voltage)

Temperatures: -45C, 25C, 125C

Parameter
supply
temperature
topinclude_nxp.scs
vbias

Test	Output	Spec	Weight	Pass/Fail	Min	Max
nxf55911:LC_VCO_THESIS_L:1	/clock					
nxf55911:LC_VCO_THESIS_L:1	/div2					
nxf55911:LC_VCO_THESIS_L:1	/div4					
nxf55911:LC_VCO_THESIS_L:1	value(freq(VT("/clock") "rising" ...				3.121G	3.343G
nxf55911:LC_VCO_THESIS_L:1	value(freq(VT("/div2") "rising" ?...				1.561G	1.672G
nxf55911:LC_VCO_THESIS_L:1	value(freq(VT("/div4") "rising" ?...				780.3M	835.9M

Figure 29 PVT result window for frequency output

Fig. 29 shows the result window for frequency across PVT variation. The nominal values are 3.21G, 1.606G, 802.6M. The minimum and maximum are obtained at following PVT conditions.

- **Minimum**: FF, 1.44V, 25C
- **Maximum**: SS, 1.18V, -40C

5.2.3 MONTE CARLO ANALYSIS

Monte Carlo simulations covers the PVT mentioned above and the mismatches.

Test	Name	Yield	Min	Target	Max	Mean	Std Dev	Cpk	Errors
Yield Estimate: 100 %(198 passed/198 pts)	Confidence Level: <not set> Filter: <not set>								
nxf55911:LC_VCO_THESIS_L:1									
	value(freq(VT("/div4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 0.6)(summary)	100	776.4M		834.4M	805.8M	8.195M		0
	value(freq(VT("/div4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 0.6)_globalmc_localmc_0	100	790.7M	info	834.4M	814.7M	8.195M		0
	value(freq(VT("/div4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 0.6)_globalmc_localmc_1	100	789.1M	info	831.5M	812.9M	8.047M		0
	value(freq(VT("/div4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 0.6)_globalmc_localmc_2	100	793.2M	info	834.2M	816.1M	7.724M		0
	value(freq(VT("/div4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 0.6)_globalmc_localmc_3	100	783.5M	info	823.9M	804.9M	7.695M		0
	value(freq(VT("/div4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 0.6)_globalmc_localmc_4	100	781.1M	info	821.1M	802.9M	7.652M		0
	value(freq(VT("/div4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 0.6)_globalmc_localmc_5	100	784.9M	info	823.3M	806.1M	7.334M		0
	value(freq(VT("/div4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 0.6)_globalmc_localmc_6	100	780.9M	info	818.4M	799.6M	7.233M		0
	value(freq(VT("/div4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 0.6)_globalmc_localmc_7	100	776.4M	info	813.9M	796.2M	7.311M		0
	value(freq(VT("/div4") "rising" ?xName "time" ?mode "auto" ?threshold 0.5) 0.6)_globalmc_localmc_8	100	779M	info	815.8M	798.8M	7.041M		0

Figure 30 Monte Carlo result window for frequency output

Fig. 30 shows the monte-carlo simulation result window for frequency.

5.3 PHASE NOISE

The phase noise of the circuit is -131dBc/Hz at nominal. This section provides the phase noise results at nominal, PVT and Monte carlo.

5.3.1 NOMINAL

This section presents the simulation result of circuit for nominal case. Nominal case is when supply voltage is 1.31V, temp is 25C, process is typical.

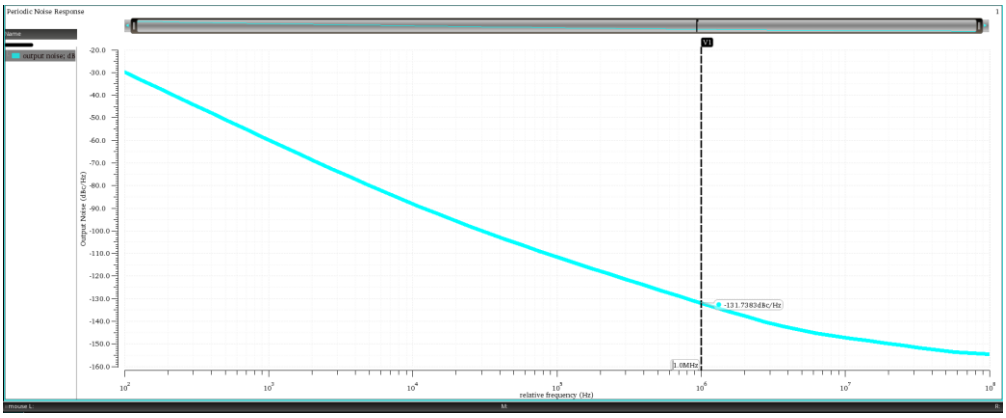

Figure 31 Phase noise graph for implemented LC VCO

Fig. 31 represents the Phase Noise graph of the circuit. The phase noise is -131.7dBc/Hz.

5.3.2 ACROSS PVT

This section provides simulation result of the circuit across PVT. Monte Carlo simulations covers the PVT mentioned above and the mismatches. PVT is checked for following corners, voltages and temperatures:

Corners: SLOW, SS, SF, TT, FS, FF, FAST

Voltages: 1.18, 1.31, 1.44 (+/- 10%of Nominal Voltage)

Temperatures: -45C, 25C, 125C

Parameter					
supply					
temperature					
topinclude_nxp.scs					
vbias					
Output	**Spec**	**Weight**	**Pass/Fail**	**Min**	**Max**
fOutputNoise("dBc/Hz" ...				-132.6	-122.5

Figure 32 PVT result window for phase noise output

Fig. 32 shows the result window for phase noise across PVT variation The nominal value is -131.7 dBc/Hz. The minimum and maximum are obtained at following PVT conditions.

- **Minimum**: FF, 1.31V, -40C
- **Maximum**: SF, 1.18V, -125C

5.3.3 MONTE CARLO ANALYSIS

Monte Carlo simulations covers the PVT mentioned above and the mismatches.

Test	Name	Yield	Min	Target	Max	Mean	Std Dev	Cpk	Errors
Yield Estimate: 100 %(200 passed/200 pts)	Confidence Level: <not set> Filter: <not set>								
nxf55911:LC_VCO_THESIS_L:1									
	value(rfOutputNoise("dBc/Hz" ?result "pnoise") 1000000)(summary)	100	-136		-126.4	-132.3	801.6m		0
	value(rfOutputNoise("dBc/Hz" ?result "pnoise") 1000000)_globalmc_localmc_0	100	-136	info	-131.2	-134.9	801.6m		0
	value(rfOutputNoise("dBc/Hz" ?result "pnoise") 1000000)_globalmc_localmc_1	100	-133.9	info	-130.1	-133	593.7m		0
	value(rfOutputNoise("dBc/Hz" ?result "pnoise") 1000000)_globalmc_localmc_2	100	-128.5	info	-126.4	-127.6	388.9m		0
	value(rfOutputNoise("dBc/Hz" ?result "pnoise") 1000000)_globalmc_localmc_3	100	-136	info	-132.7	-135	488.6m		0
	value(rfOutputNoise("dBc/Hz" ?result "pnoise") 1000000)_globalmc_localmc_4	100	-135.2	info	-132.2	-134.3	391m		0
	value(rfOutputNoise("dBc/Hz" ?result "pnoise") 1000000)_globalmc_localmc_5	100	-130.3	info	-128.4	-129.5	338m		0
	value(rfOutputNoise("dBc/Hz" ?result "pnoise") 1000000)_globalmc_localmc_6	100	-133.2	info	-130	-131.6	670.1m		0
	value(rfOutputNoise("dBc/Hz" ?result "pnoise") 1000000)_globalmc_localmc_7	100	-135	info	-132.5	-134.1	385.9m		0
	value(rfOutputNoise("dBc/Hz" ?result "pnoise") 1000000)_globalmc_localmc_8	100	-131.3	info	-129.8	-130.6	315.2m		0

Figure 33 Monte Carlo result window for phase noise output

Fig. 33 shows the monte-carlo simulation result window for Phase Noise.

Chapter 6

CONCLUSIONS

This work describes the design of LC VCO on 40nm technology. Phase noise from core has been reduced by using high transconductance transistors and from capacitor bank by optimization of switches. High gm transistors also helps in reducing power. In LC VCO inductor occupies most of the area. Size of inductor increases as the frequency of operation decreases. To keep the inductor area to minimum, core is designed at higher frequency and the divider is used to achieve required frequency. Capacitors and resistors chosen help in minimizing the variation.

Presented design has a phase noise of -131dBc/Hz at 1MHz offset and consumes 4.3mW of power. Through this work a good understanding of the design and working of LC VCO is developed. Various aspects of the design were explored and taken into consideration while designing. A table with current work and other works in this domain is presented in Table 2.

Table 2 Comparison Table

S.NO	**PARAMETER**	**THIS WORK**	**[19]**	**[20]**	**[21]**	**[22]**
1.	TECHNOLOGY (nm)	40	40	65	90	180
2.	IMPLEMENTATION	LC VCO	Pass. IL- Ring	Ring VCO	LC IL	LC VCO
3.	FREQUENCY	800MHz	28GHz	800MHz	20GHz	900MHz
4.	SUPPLY VOLTAGE (V)	1.31V	1V	1.1-1.3V	1.5V	1.5V
5.	CURRENT CONSUMED	3.29mA	-	-	-	3.8mA
6.	PHASE NOISE (dBc/Hz)@1MHz	-131.7	-124.5@10MHz	-98.0	-123.0	104.7
7.	POWER (mW)	4.3	.88	.51	70	5.7

FUTURE WORK:

Future work includes following:

- Layout of LC VCO.
- Design of other blocks of PLL and integration of complete circuit.

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