Impact of Testability on PPAS

by

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Certificate

This is to certify that the Thesis titled **“Impact of Testability on PPAS”** being submitted by **Gangaprasad Horke (MT23214)**, to the **Indraprastha Institute of Information Technology Delhi**, for the award of the degree of **Master of Technology**, is an original research work carried out by him under my supervision.

In my opinion, the Thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The contents of this project, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Abstract

As semiconductor technology advances toward higher integration and functional density, the challenges associated with Design-for-Testability (DFT) have become increasingly significant, particularly in terms of power consumption during testing and chip manufacturing. To analyze the impact of testability on sustainability, this thesis introduces a novel sustainability framework to assess the carbon footprint generated during the testing and manufacturing phases of integrated circuits.

The study explores the implementation of DFT using multiple scan insertion techniques, including normal scan chain insertion, DFTmax, and DFTmax Ultra, and compares their impact on sustainability. Experimental results demonstrate up to a **10% reduction in test time** and a **30% reduction in test data volume** owing to shorter scan chain lengths achieved in DFTmax and DFTmax Ultra, while also analyzing their impact on sustainability.

The aim of introducing this framework is to provide intelligent guidance, helping designers make informed decisions to reduce environmental impact. The metric is expressed in energy units, which can later be converted into CO_2 equivalents, providing an estimate of the potential environmental impact.

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Chapter 1

Introduction

1.1 Motivation

The swift evolution of semiconductor technology has resulted in the design of higher-density chips in an attempt to achieve an optimal balance in Power, Performance, and Area (PPA) trade-offs [1]. This accomplishment, however, comes at the cost of the environment, given the fact that intricate manufacturing processes and high power usage in testing raise sustainability issues. As such, the VLSI industry needs to widen its scope beyond traditional assessment metrics like PPA to include sustainability (S) as a built-in element, thereby forming a Power, Performance, Area, and Sustainability (PPAS) assessment framework.

To mitigate these challenges, the Very-Large-Scale Integration (VLSI) sector is moving away from traditional Power, Performance, and Area (PPA) evaluations towards a more comprehensive framework including Sustainability (S), thus creating a framework for Power, Performance, Area, and Sustainability (PPAS) evaluation. Large semiconductor corporations, including TSMC, Apple, Samsung, STMicroelectronics, Intel, and Qualcomm, have already released sustainability roadmaps detailing their commitment towards achieving carbon neutrality [13–18]. For example, in a report by Bloomberg in 2022, the annual energy consumption of TSMC was over the entire energy consumption of Sri Lanka [12].

As emphasized in [11], the ongoing advancement in semiconductor manufacturing technology leads to a tremendous increase in energy consumption, thereby escalating their environmental footprint [10]. Despite significant advancements in sustainability research in the last two decades, most of this work has been largely at higher levels of abstraction for integrated circuits (ICs) or end products. A comprehensive sustainability framework is necessary to assess the environmental footprint of Design-for-Testability (DFT) since chip testing can account for anywhere between 500 kWh and 1000 kWh during heavy test periods, which is a substantial amount. This framework enables intelligent decisionmaking during the scan insertion process so that testing strategies are chosen in a way to reduce environmental footprint while ensuring operational efficiency.

1.2 Design for Testability (DFT)

Design for Testability (DFT) is a methodology of designing electronic devices and chips in a way that makes them easier to test for faults. As chips become more complex, identifying internal faults becomes increasingly difficult. DFT addresses this by introducing special features that allow engineers to observe and control the internal operations of the chip during testing. The primary goal of DFT is to detect as many errors as possible while minimizing testing costs and time. DFT focuses on identifying common issues such as stuck-at faults, bridging faults, or broken connections. Even with advanced fabrication technologies and clean manufacturing environments, tiny defects can still occur due to the extremely dense nature of modern chips.

1.2.1 Scan-Based Structural Testing

Scan-based structural testing is a widely used and effective method for testing complex digital circuits. It modifies the original design slightly by incorporating **scan cells**, which are enhanced flip-flops. These scan cells behave like regular flip-flops during normal operation but switch to test mode during testing. When connected in series, they form a **scan chain**, essentially a shift register that enables test data to be shifted in and out of otherwise inaccessible circuit regions.

This configuration simplifies the detection of structural faults, such as broken or misconnected gates, without requiring exhaustive input testing. Moreover, it facilitates efficient test generation by targeting the circuit's structure rather than complete functional behavior. Tools called Automatic Test Pattern Generators (ATPG) generate fault-specific test vectors, which are then applied using Automatic Test Equipment (ATE) to validate actual outputs against expected values.

Mode	**TM**	**SE**
Functional	0	0
Test (Shift)	1	1
Test (Capture)	1	0

Table 1.1: Scan Design Operation Modes.

Scan-based testing is highly scalable, efficient, and automatable, making it indispensable in modern semiconductor manufacturing processes where circuit complexity continues to grow exponentially.

Chapter 2

Literature Survey

2.1 Sustainability contributions in VLSI

The last two decades have seen numerous research studies play a crucial role in encouraging sustainability-based VLSI design. Studies in the early days, as in research in 2000 [21], utilized the EE-toolbox to analyze semiconductor materials based on recyclability, toxicity, energy consumption, and environmental effects of processing. In 2017, another study [22] suggested a scalable approach to assessing the ecological effects of fabrication over technology nodes of 130 nm to 32 nm, pointing out the effect of variations in metal stack configurations to markedly contribute to System-on-Chip (SoC) design environmental impact. In 2022 research [14], a Life Cycle Analysis (LCA) of commonly used products also revealed that, while algorithms, software, and hardware have become more energy efficient, the environmental footprint from the manufacturing of hardware and infrastructure has surpassed operational energy consumption as the highest source of emissions.

Subsequently, in 2024 [23], the Eco-Reliability metric was proposed, which combines environmental and reliability aspects for VLSI sustainability evaluation. The metric combines traditional reliability metrics like Mean Time to Failure (MTTF) and Mean Time Between Failures (MTBF) with environmental elements like lifecycle carbon footprint, System Earth equivalent time, and global resource availability. In expanding the evaluation from the PPA model to incorporate sustainability (S), the approach provides a more comprehensive PPAS evaluation.

Use of a sustainability framework is important in assessing the environmental impact of Design-for-Testability (DFT). Chip testing is very energy-intensive, usually between 500 kWh and 1000 kWh during extensive testing activities. DFT methods over the years have developed from conventional scan insertion to various scan compression methods, mainly aimed at shrinking scan chain lengths, which in turn reduces both test time and test data size. Additionally, several methods have been developed to reduce test power consumption, including Q-gating with multi-bit flip-flop mapping, X-fill methods, and several scheduling methods. Through the use of a sustainability framework, designers are in a better position to make more informed decisions throughout the scan insertion process, not just ensuring efficiency in testing but also reducing its environmental footprint.

2.2 Test Power Reduction Methodologies

Test power has emerged as one of the most critical parameters in Design-for-Testability (DFT), ranking just behind fault coverage in overall importance. Although a wide range of test power reduction techniques have been proposed in theory and academic literature, only a select few are truly implementable in practical, real-world designs. Even among those, only limited techniques consistently deliver meaningful reductions in power consumption during testing. This chapter highlights a set of practical, architecture-conscious methodologies that effectively reduce test power without compromising test coverage or significantly increasing test application time. The most prominent and industry-relevant power reduction strategies are explained in the sections below.

2.2.1 Q-gating Technique with multi-bit flip-flop mapping

This method is concerned with minimizing the excessive power usage during chip testing that leads to failures and low yield. Conventional scan-based testing draws huge dynamic power, particularly during scan shifting when switching activity is as high as 30% of the circuit. It emphasizes on the importance of power-aware methods that offer fault coverage with lower power dissipation, meeting reliability and sustainability goals in semiconductor design.

A flow baseline was created from a design of 500K instances in 22 nm technology. The flow had synthesis, DFT insertion, ATPG pattern generation, simulation, and power analysis using Synopsys tools. Experiments revealed that the static power remained constant at 150 mW, while the dynamic power contributed the most to test power with an average of 670–710 mW per pattern, resulting in total power values of 820–860 mW. Such high switching activities during scan operations necessitated low-power testing optimization methods.

To minimize power, the study proposed three methods: multibit mapping, which minimizes switching and clock activity using multibit flip-flops; multibit reordering, which reduces toggles by directing low-activity bits out to scan-out; and Q-gating, which avoids unnecessary transitions in combinational logic during scan shifting. Applied where possible, the above methods lowered dynamic power by approximately 25–30%, lowering average test power to 620–660 mW without modifying static power. The results show that the adoption of the above methods in EDA flows is a feasible and practical way to green and power-aware semiconductor testing.

2.2.2 Scan Cell Reordering methodology

Scan cell reordering is a DFT method by which scan cells in a chain are rearranged for improved testing. It is primarily used to minimize routing congestion as well as minimize test power. Scan chains, without physical placement, have the potential to interconnect far-apart flip-flops and lead to long wires and overhead. It is an optimization technique similar to the Travelling Salesman Problem (TSP), for which the shortest path is to be determined.

Element reordering also reduces switching activity during scan shift and thus conserves power. For example, flip-flop sequence reordering can reduce test vector transitions and save energy. Advanced techniques like DC-SCAN and WTM optimize the ordering mechanism by grouping cells of similar characteristics and favoring transitions that induce higher power consumption. Even though such techniques work well, they are highly computationally intensive, especially for large designs, and are applied only after design completion.

2.2.3 X-fill Methods

Software-based test power reduction methods primarily exploit the availability of don't care bits (Xbits) in test patterns. A test cube represents a partially specified pattern containing both care and don't care bits, while a test vector is a fully defined pattern derived from it. In deterministic ATPG, the tool assigns '0' or '1' values to all scan elements based on a targeted fault set. Bits essential for fault detection are referred to as care bits. Early test vectors often have a high density of care bits, but as coverage increases, many scan elements become irrelevant to remaining faults, allowing these positions to be filled with either '0' or '1' without affecting test coverage. These are the don't care bits, and they often constitute 95–98% of industrial test cubes. The strategic assignment of values to X-bits can significantly reduce power by minimizing signal transitions during shift and capture.

Several X-filling techniques have been developed:

- 0-filling: Replaces all Xs with logic '0'.
- 1-filling: Replaces all Xs with logic '1'.
- Minimum Transition filling (MT-filling): Assigns each X-bit the value of its preceding care bit, reducing transitions—this is widely preferred for its effectiveness.

These techniques are supported in most commercial ATPG tools and can target shift power, capture power, or both.

Advanced X-filling strategies include:

- DC-LCP (Double-Capture Low-Capture-Power) by Wen et al., using probability-weighted transition metrics for capture power reduction.
- Input-dominated X-filling by Yang and Xu, focused on minimizing Weighted Switching Activity (WSA).
- Post-ATPG pattern replacement by Wu et al., which replaces high-power test patterns with X-filled low-power alternatives.
- Bounded Adjacent X-Fill by Chandra and Kapurt, optimizing based on correlations between scan-in and scan-out vectors.
- iFill by Li et al., which first minimizes capture power and then applies X-filling for shift power.
- Structure-based filling by Badereddine et al., targeting toggling in combinational logic.

While these methods offer significant test power reduction, they can also lead to increased ATPG runtime and test data volume (TDV) due to pattern inflation from transition minimization.

Chapter 3

DFT Techniques

3.1 Basic Scan Architecture

Consider the simple sub-circuit, which performs a 6-input AND operation. The inputs (I_1 to I_6) are processed using a combination of AND gates (A_1–A_4) and flip-flops (F_1–F_{10}) that propagate intermediate results across clock cycles. It typically takes three clock cycles for the inputs to be fully processed and the result to appear at the output O_1.

asic$_and$

If we treat the circuit as a black box, $2^6 = 64$ test vectors are required to evaluate its full functionality. Alternatively, structural-level analysis can verify each gate individually:

- Each 2-input AND gate requires 4 test combinations.
- The 3-input AND gate requires 8 test combinations.

However, internal nodes cannot be directly accessed. For instance, while inputs $a1a$ and $a1b$ can be controlled to test gate A_1, its output $a1z$ cannot be observed externally. Similarly, isolating and testing inputs of the 3-input gate A_4 is difficult.

A practical solution involves adding multiplexers (MUXes) before flip-flop inputs (Figure **??**). Each flip-flop input can be switched between normal functional data and a scan input (SI), controlled by a Test Mode (TM) signal:

- **TM = 0**: Functional mode — normal data is passed to flip-flops.
- **TM = 1**: Scan mode — scan data is shifted in.

When TM=1, the circuit reconfigures into a scan chain . Flip-flop F_1 receives its input from the Scan-In (SI) pin, acting as a serial input, while subsequent flip-flops form a shift register. This enables efficient loading and observation of test data, improving controllability and observability of internal nodes.

For this design, 9 clock cycles are needed to load a complete test vector into the scan chain. The test sequence works as follows:

- **Shift-in:** With TM=1, the circuit becomes a serial chain. Data is fed via SI over 9 clock cycles.
- **Capture:** With TM=0, the circuit returns to functional mode. Outputs of AND gates $(a1z, a2z, a3z, a4z)$ are latched into flip-flops F_7–F_{10}.
- **Shift-out:** With TM=1 again, captured data is shifted out serially via the Scan-Out (SO) pin.

This process ensures efficient testing and high fault coverage.

3.2 Scan Compression

3.2.1 DFTMAX

Scan-based testing has long been a cornerstone of DFT, but as IC sizes grew, limitations emerged: increasing logic density led to larger test data volumes, new fault models required more test patterns, and scan chains grew longer due to I/O constraints, extending test time and cost.

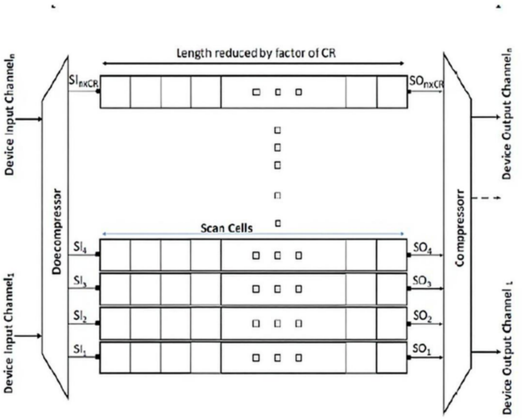

Figure 3.1: DFTMAX scan compression architecture [25]

Scan compression solves these challenges by reducing test data volume and shortening scan chain lengths. As shown in Figure 6.3, a scan compression architecture consists of:

- A **Decompressor**, which expands limited tester inputs into multiple shorter internal scan chains.
- A **Compressor**, which collects scan responses and reduces them to match tester I/O bandwidth.

The effectiveness is measured by the **Compression Ratio (CR)**, defined as:

$$CR = \frac{\text{Number of internal scan chains}}{\text{Number of scan input channels}}$$

Higher CR reduces test time and data size but risks:

- Increased correlation in scan data (lower test coverage if CR is excessive).
- Routing congestion due to decompressor–scan chain connections.
- Area overhead from extra hardware.

Thus, CR must be carefully optimized. In modern SoCs, scan compression has become mainstream, significantly reducing test costs and time .

3.2.2 DFTMAX Ultra

DFTMAX Ultra is an advanced compression method built on DFTMAX, optimized for hierarchical SoC testing. It enables very high compression with minimal I/O pins, while preserving high fault coverage and low area/timing overhead.

The architecture includes:

- A shift register that separates incoming scan data into **control bits** and **data bits**.
- A decompression multiplexer that distributes data across multiple scan chains.
- An XOR-based output compactor with redundancy to handle unknown (X) values.

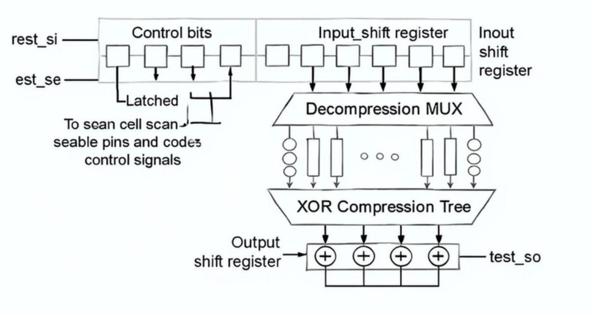

Figure 3.2: DFTMAX Ultra scan compression architecture [25]

Test data is streamed through a single SI and SO using the scan clock, minimizing pin usage. DFTMAX Ultra is typically used as an add-on to DFTMAX, automatically generating optimized compression logic based on user-specified scan inputs/outputs and chain counts.

3.3 Test Pattern Generation

Automatic Test Pattern Generation (ATPG) is a crucial component of modern chip testing, responsible for creating input patterns that detect faults caused by manufacturing defects. ATPG operates based on **fault models**, which are standardized assumptions about possible circuit malfunctions. The goal of ATPG is to generate the smallest set of test patterns that achieves the highest fault coverage, thereby minimizing test time, cost, and the reliance on expensive testers with large memory and pin counts.

One of the key applications of ATPG is in **Built-In Self-Test (BIST)** systems. In BIST, the circuit itself generates and applies test patterns internally, enabling self-testing without external testers. This is particularly beneficial for systems requiring frequent testing or in-field diagnostics. ATPG strategies for BIST typically combine both deterministic and probabilistic methods.

3.3.1 Deterministic ATPG

Deterministic ATPG generates specific test patterns tailored to activate and detect particular faults. These patterns are algorithmically designed to propagate fault effects to observable outputs, often through scan chains. The objective is to maximize fault coverage with the minimum number of patterns. This method is highly effective but can be computationally intensive for large-scale designs.

3.3.2 Probabilistic ATPG

Probabilistic ATPG employs **Pseudorandom Pattern Generators (PRPGs)** to produce random input patterns. These are then validated through fault simulation to determine their fault coverage. Although not as precise as deterministic approaches, probabilistic ATPG is useful in the early testing stages for broad fault coverage and is frequently integrated with deterministic ATPG in BIST systems.

3.3.3 Fault Models

The effectiveness of ATPG heavily depends on the chosen fault model. Common fault models include:

- **Stuck-at Fault Model:** Assumes a circuit node is permanently stuck at logic '0' or '1'. ATPG generates patterns that attempt to force the node to the opposite value and verify correct propagation to outputs.

These fault models provide the basis for efficient ATPG algorithms, enabling systematic test generation and improving fault coverage in modern integrated circuits.

Chapter 4

DFT Parameters

4.1 Test Coverage

Test Coverage, also referred to as **fault coverage**, measures the percentage of detectable faults identified in a System-on-Chip (SoC) during testing. It is primarily determined by two key factors:

- **Controllability:** The ease of applying the desired logic values to the inputs of a gate.
- **Observability:** The ability to observe the effect of input changes at the outputs.

The use of scan chains significantly enhances both controllability and observability, improving fault detection. Although the theoretical goal is to achieve 100% test coverage, practical limitations such as design complexity and fault masking make this unrealistic. In practice:

- Consumer-grade SoCs typically achieve 95–98% coverage.
- Automotive-grade and safety-critical systems often require 99% or higher fault coverage to meet strict reliability standards.

Achieving 80–90% coverage is relatively straightforward with a modest number of test patterns, but pushing coverage beyond this threshold requires exponentially more patterns and advanced DFT techniques.

4.2 Test Time

Test Time refers to the total duration required to apply all test patterns to a chip. It can be estimated as:

$$\text{Test Time} = (\text{Longest Scan Chain Length}) \times (\text{Clock Period}) \times (\text{Number of Test Patterns})$$

For example, consider a design with 7500 scan cells split into 7 chains (one per scan input channel). Each chain then contains 1065 scan cells. If 440 patterns are applied at a 40 MHz clock frequency:

$$T = \frac{1065 \times 440}{40 \times 10^6} \approx 0.0117 \text{ seconds per chip}$$

Although 0.0117 seconds per chip may seem negligible, testing 1 million dies would take:

$$0.0117 \times 10^6 \approx 3.25 \text{ hours}$$

To reduce test application time (TAT), scan compression techniques such as **DFTmax** and **DFTmax Ultra** are applied. By shortening scan chain lengths to 40 and forming 188 chains (compression ratio = 188/7) in DFTmax and 248 chains (compression ratio = 248/7) in DFTmax Ultra:

- Number of patterns increases slightly (1671 for DFTmax, 1125 for DFTmax Ultra).
- Test coverage remains high despite compression overhead.
- Test time per chip drops significantly to 0.00167s (DFTmax) and 0.001125s (DFTmax Ultra).

For 1 million dies, the total test time reduces from 3.25 hours to just 0.3125 hours, demonstrating the dramatic impact of compression.

4.3 Comparative Results

Table 4.1: Comparison of Scan Insertion Techniques

Parameters / Methods	**Normal Scan Chain**	**DFTmax**	**DFTmax Ultra**
Test Coverage (%)	95.1	95.23	95.31
No. of Test Patterns	440	1671	1125
Compression Ratio	1	188/7	247/7
Test Data Volume	10,307,630	3,205,443	2,827,295
No. of Scan Cells per Chain	1065	40	40
Shift Frequency	40 MHz	40 MHz	40 MHz
Test Time (s)	0.011715	0.001671	0.001125
Test Time for 1 million devices	3.25 hours	0.46 hours	0.31 hours

Chapter 5

Sustainability Framework

In this chapter, a proposed framework is presented to evaluate the sustainability of circuits, designs, or architectures using a **Life Cycle Assessment (LCA)** approach. The sustainability of a VLSI design is assessed in terms of its *embodied* and *operational* carbon footprints.

Estimating the Carbon Footprint (CFP) of any product is inherently data-intensive, and detailed information may not be available during early stages of the Product Development Life Cycle (PDLC), when critical design decisions are made. To address this limitation, our framework leverages historical trends and available datasets to enable reasonable comparisons between design alternatives.

The framework does not aim to deliver an exact CFP but rather to provide intelligent guidance, helping designers make informed decisions to reduce environmental impact. The metric is expressed in energy units, which can later be converted into CO_2 equivalents, providing an estimate of the potential environmental impact.

5.1 Embodied Carbon Footprint (eCFP)

The embodied carbon footprint encompasses the environmental impact associated with design, prototyping, raw material selection, processing, and chip fabrication. Key influencing factors include:

- Technology node
- Die size
- Number of interconnect layers
- Supply chain efficiency

For example, producing a 300 mm wafer at 65 nm with a six-layer metal stack may require around 4204 kWh of energy. The embodied footprint is normalized by die size and modeled as a function of metal layer count, ensuring adaptability across different design complexities.

Case Studies

- Case 1: For 6 metal layers

$$eCFP = 4204 \times 10^6 \times \frac{\text{Design Area}}{\text{Wafer Area}}$$

- Case 2: For 8 metal layers

$$eCFP = 4895 \times 10^6 \times \frac{\text{Design Area}}{\text{Wafer Area}}$$

- Case 3: For 10 metal layers

$$eCFP = 5586 \times 10^6 \times \frac{\text{Design Area}}{\text{Wafer Area}}$$

Generalized Formula

The generalized equation is expressed as:

$$eCFP = \frac{\text{Design Area}}{\text{Wafer Area}} \times (4895 + (\text{Metal Layers} - 8) \times 345.5) \times 10^6$$

where:

- eCFP is in mWh
- Design Area and Wafer Area are in consistent units (e.g., μm^2)

5.2 Operational Carbon Footprint (oCFP)

The operational carbon footprint (oCFP) measures the carbon footprint(CF) associated with the energy consumed by hardware during its operational life. The proposed oCFP estimates the energy consumed across all operational modes and testing of the device. In Equation (5.1), oCFP is calculated by summing the dynamic power and leakage power over the total operational period of the device, denoted as Ttotal and the energy consumption during testing. This total period varies depending on the specific requirements of the application and the conditions of use. The energy consumption by ATE machine during intense testing phase is 500 - 1000 kWh.

Equation 5.1 gives the general formulation:

$$\text{oCFP} = T_{total} \times \left(\frac{\text{Dynamic Power} \times ATR}{100} + \frac{\text{Leakage Power} \times STR}{100} \right) + \frac{500 \times 10^6}{\text{No. of Chips per Hour}} \tag{5.1}$$

The number of chips processed per hour is given by:

$$\text{No. of Chips per Hour} = \frac{3600}{\text{Test Time} + \text{Setup Time}}$$

5.2.1 Application-Specific Operation Profile

Electronic devices operate in different modes depending on their application requirements. For this thesis, we focus on **IoT applications**, which exhibit the following operating time ratios:

Table 5.1: Operating Time Ratios for IoT Applications

Operating Mode	**Time Ratio**
Active (ATR)	5%
Standby (STR)	25%
Switched Off (SOTR)	70%

The operational lifetime is considered to be approximately 20,000 hours (2.28 years). In IoT devices, the circuit remains active for only a small percentage of its life but contributes significantly to overall oCFP.

5.2.2 Setup Time in ATE Operations

Setup time in Automatic Test Equipment (ATE) refers to the duration required for loading and unloading a chip. It is estimated as:

$$\text{Setup Time} = \frac{3600}{\text{Throughput}}$$

For example, the **M4841 Device Handler** delivers a throughput of 18,500 devices per hour, which directly impacts test efficiency and sustainability analysis.

Chapter 6

Results

This chapter presents a comparative analysis of Design-for-Testability (DFT) parameters and sustainability metrics across three techniques: **Normal Scan Chain Insertion**, **DFTmax**, and **DFTmax Ultra**.

6.1 Comparison of DFT Parameters

Table 6.1 summarizes the results obtained from synthesis, testing, and power analysis tools for all three methods.

Table 6.1: Comparison of DFT Parameters across Techniques

Parameters / Methods	**Normal Scan Chain**	**DFTmax**	**DFTmax Ultra**
Test Coverage (%)	95.1	95.23	95.31
No. of Test Patterns	440	1671	1125
Compression Ratio	1	188/7	247/7
Test Data Volume	10,307,630	3,205,443	2,827,295
No. of Scan Cells per Chain	1065	40	40
Shift Frequency	40 MHz	40 MHz	40 MHz
Test Time (s)	0.011715	0.001671	0.001125
Dynamic Power (mW)	96.2371	60.1660	59.8458
Leakage Power (mW)	0.1378	0.1193	0.1365
Area (μm^2)	179,925.718	184,605.198	202,604.478
Test Time for 1 million devices	3.25 hours	0.46 hours	0.31 hours

From the table, it is evident that while compression-based methods (**DFTmax, DFTmax Ultra**) slightly increase area overhead, they significantly reduce **test data volume** and **test time**, with DFTmax Ultra showing the best overall balance in performance and power.

6.2 Comparison of Sustainability Metrics (eCFP vs oCFP)

The sustainability framework discussed in Chapter 3 is applied to compute the **Embodied Carbon Footprint (eCFP)** and **Operational Carbon Footprint (oCFP)** for all three DFT techniques. The results are summarized in Table 6.2.

Table 6.2: Comparison of eCFP and oCFP across DFT Techniques

Carbon Footprint Metric	**Normal Scan**	**DFTmax**	**DFTmax Ultra**
eCFP (mWh)	10700.98	10979.28	12049.78
oCFP (mWh)	125571.23	88008.47	87731.77
Total Footprint (mWh)	166272.2	98987.75	99781.55

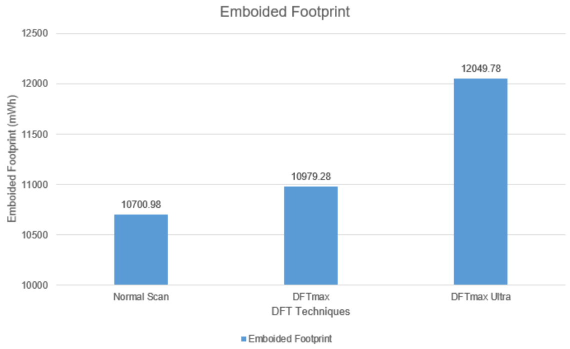

Figure 6.1: Emboided Footprint

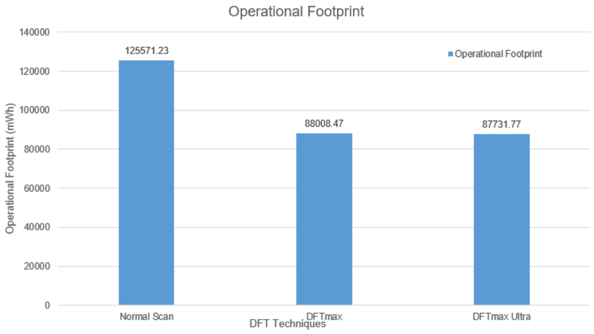

Figure 6.2: Operatioanl Footprint

It can be observed that:

- **Normal Scan** achieves the lowest eCFP due to lower area overhead but exhibits the highest oCFP due to longer test time.
- **DFTmax and DFTmax Ultra** show a moderate increase in eCFP (attributed to added compression.

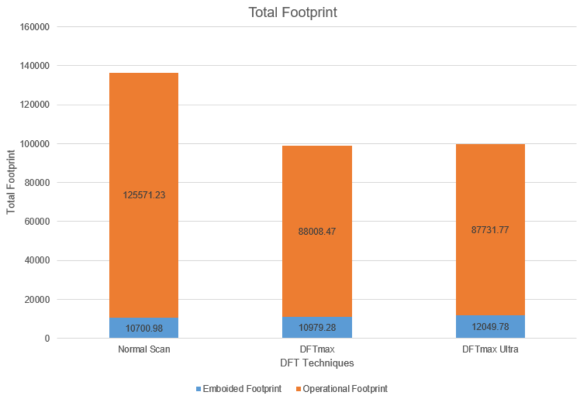

Figure 6.3: Total Footprint

It can be observed that:

- **T**he Total Footprint of DFTmax is 59.53 percent lower than normal Scan and DFTmax Ultra is 60 percent lower than Normal Scan
- **T**he Total Footprint of DFTmax Ultra is 0.2 percent lower than DFTmax
- **A**s per Total Footprint DFTmax is the better option considering Sustainability.

Conclusion

This thesis examined the influence of different Design-for-Testability (DFT) methods on both conventional design parameters and sustainability factors. The study compared three approaches—standard scan chain insertion, DFTMAX, and DFTMAX Ultra—for all metrics such as fault coverage, testing time, data volume, power, and area. Compression-based results, particularly DFTMAX and DFTMAX Ultra, are significantly efficient for testing. The test duration was reduced by almost ten times relative to conventional scan chains, and test data requirements dropped by over 30 percent.

On observing the results of the embodied footprint, it was observed that compression methods slightly increase the embodied carbon footprint (eCFP) due to additional circuitry. However, the operational carbon footprint (oCFP) was notably reduced with DFTMAX Ultra, achieving the lowest oCFP. Overall, this work shows that assessing DFT solely through the lens of Power, Performance, and Area (PPA) is no longer sufficient. By extending the evaluation to include sustainability (S) within a unified PPAS framework, designers can make more responsible and forward-looking decisions.

Among the tested methods, DFTMAX proved to be the most effective and sustainable, offering a well-rounded balance of testing efficiency, coverage, and reduced environmental impact. This study highlights the need to treat sustainability as a core design metric in VLSI, setting the stage for more eco-friendly semiconductor technologies in the years ahead.

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