Impact of Flip-Flop Design Choices on Sustainability for IoT Application

by

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New Delhi - 110020

14 May, 2025

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May 2025

Impact of Flip-Flop Design Choices on Sustainability for IoT Application

A Thesis Report

submitted by

Najeeb Mohammad Khan

in partial fulfilment of the requirements
for the award of the degree of

Master of Technology

to

Electronics and Communication Engineering
Indraprastha Institute of Information Technology Delhi
New Delhi - 110020

14 May, 2025

Certificate

This is to certify that the thesis titled "**Impact of Flip-Flop Design Choices on Sustainability for IoT Application**" being submitted by **Najeeb Mohammad Khan**, to the Indraprastha Institute of Information Technology Delhi, for the award of the degree of **Master of Technology**, is an original research work carried out by him under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 14 May 2025

Acknowledgements

I want to express my gratitude to my thesis advisor, Dr. Anuj Grover, for his invaluable guidance, support, and encouragement throughout my MTech thesis. His insightful feedback, continuous motivation, and expertise have played an important role in shaping the direction and outcome of my work. It has truly been a privilege to learn under his mentorship. I am profoundly thankful to my parents for their unwavering love, patience and support. Finally, I extend my heartfelt thanks to the Indraprastha Institute of Information Technology Delhi (IIIT-Delhi) for providing me with an excellent academic environment, resources, and opportunities that significantly enriched my learning experience.

Abstract

With the rise of semiconductor devices, there has been an exponential increase in their demand. By 2030, approximately 40 billion IoT devices are projected to exist globally. These devices' design, fabrication, and operation require substantial energy, leading to significant greenhouse gas emissions and a detrimental environmental impact due to climate change. Traditional analyses of Power, Performance, and Area (PPA) are no longer sufficient to address this pressing issue. There is a crucial need for a framework that guides designers in making informed choices during the initial design phase, ensuring that their designs are more sustainable and have a reduced environmental impact.

In this study, we present and validate a sustainability framework designed to conduct analyses of embodied, operational, and total carbon footprints, utilizing flip-flop architectures specifically optimized for IoT applications. Our analysis included the implementation of Transmission Gate Flip-Flop (TGFF), Change Sensing Flip-Flop (CSFF), and Contention-Free Change Sensing Flip-Flop (C2SFF) architectures with varied design choice variations. We compared their conventional performance metrics, such as Power, Performance, and Area, while also evaluating their impact on sustainability through the proposed framework. We demonstrated how our framework can aid designers in making informed decisions to achieve the most sustainable designs.

The findings reveal that design choices are closely linked to the specific requirements of the target application, significantly influencing the design decisions necessary to attain an optimal level of sustainability. For the proposed formula and assumed factor values, for embodied carbon footprint the area of the design plays a crucial role, whereas for the operational carbon footprint, leakage and dynamic power are pivotal for estimating the sustainability of the design. Additionally, we emphasized the importance of total carbon footprint for sustainability analysis that should be considered alongside PPA to address the growing issue of climate change effectively.

Keywords: Flip-flop, IoT, Power, Performance, Area, Sustainability, Embodied Carbon Footprint, Operational Carbon Footprint, Total Carbon Footprint

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Abbreviations

IIITD	Indraprastha Institute of Information Technology Delhi
IoT	Internet Of Things
SoC	System On Chip
VLSI	Very Large Scale Integration
IC	Integrated Circuit
TGFF	Transmission Gate Flip-Flop
CSFF	Change Sensing Flip-Flop
C2SFF	Contention Free Change Sensing Flip-Flop
ClkBuff	Clock Buffer
GHG	Green House Gas
PVT	Process Voltage Temperature
ECP	Embodied Carbon Footprint
OCP	Operational Carbon Footprint
C2Q	Clock To Q Delay
D2Clk	Data To Clock Delay

Notation

V	Volts
Hz	Hertz
°C	Degree Celsius
F	Farad
s	Seconds
h	Hour
W	Watt
M	Mega (10^6)
k	Kilo (10^3)
m	Milli (10^{-3})
μ	Micro (10^{-6})
n	Nano (10^{-9})
p	Pico (10^{-12})
f	Femto (10^{-15})

CHAPTER 1

Introduction

1.1 Motivation

A flip-flop serves as a fundamental building block in any sequential circuit and is one of the most commonly fabricated structures on silicon chips. Its performance and power efficiency are crucial for the success of VLSI designs. Typically, flip-flops are produced as standard cells and play a vital role in the VLSI design flow. The main characteristics that influence the selection of a particular standard cell implementation relative to the target application are Power, Performance, and Area. For small, battery-powered IoT devices, minimizing power and area are particularly critical in the design process.

A single flip-flop circuit can be implemented in various design configurations. Designers face numerous choices, such as the threshold voltage of transistors, their sizes, the metal layers utilized, and the selected routing style etc. These design decisions are optimized based on trade-offs among power, performance, and area, tailored for specific applications. However, with the rise of IoT devices, the environmental impact of these decisions has become increasingly apparent.

During the design process, sustainability is often overlooked due to the lack of a dedicated framework that specifically addresses the needs of designers. Such a framework would clearly illustrate how their design choices impact the overall sustainability of chip designs. Therefore, there is a vital need for a designer-focused sustainability benchmarking framework tailored to flip-flop designs, which can guide designers in making informed decisions throughout every stage of their design journey.

1.2 Basics of Flip-Flop Circuit

All digital circuits are comprised of combinational and sequatial logic. Combinational logic is the one which takes the input and directly provides us the output depending on the actual logic implementation. A full adder is one of the most commonly used combinational logic which has three inputs InputA, InputB and CarryIn, and has two outputs Sum and CarryOut. This can be implemented using OR, AND and XOR gates. At any point of time the output is not stored anywhere, the continuous input singals consistently drive the output signals.

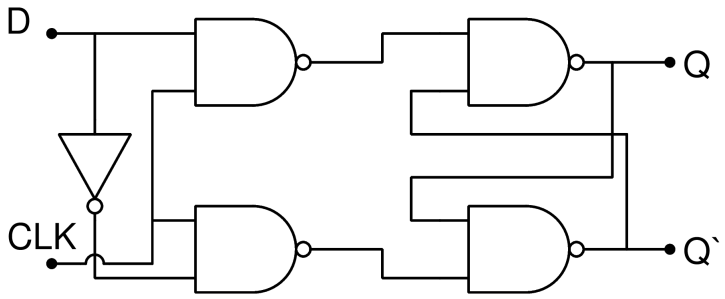

Figure 1.1: Schematic of NAND gate based D-Latch.

Table 1.1: Truth Table of D-Latch

Enable (E)	**Data (D)**	**Q (Next State)**	**Description**
0	X	Q (no change)	Latch holds its state
1	0	0	Latch resets (Q = 0)
1	1	1	Latch sets (Q = 1)

There are many circuits which require us to store the output into some memory element such that it could be used as input to next round of logic evaluation. Such logic is called sequential logic and latch is the most common type of such sequential logic element. A simple positive level triggered latch can be made with coss-coupled NAND gates as shown in Fig. 1.1. The working of NAND Latch is presented in Table 1.1 where 'Enable' is the level sensitive 'CLK' signal depicted in Fig. 1.1. When 'Enable' is low, the latch preserves its data and acts as a memory element. When 'Enable' is high the latch is said to be transparent, it stores the data provided by 'D' into itself, updating the memory element.

Latches are small and compact devices, but they are level-sensitive, which can result in race conditions. Additionally, when they are enabled, they can transmit glitches from the input data to the output signals, potentially corrupting the entire sequential logic. To address these issues, flip-flops were introduced. These components are edge-sensitive, which resolves the drawbacks of latches and provides a consistent and reliable storage element.

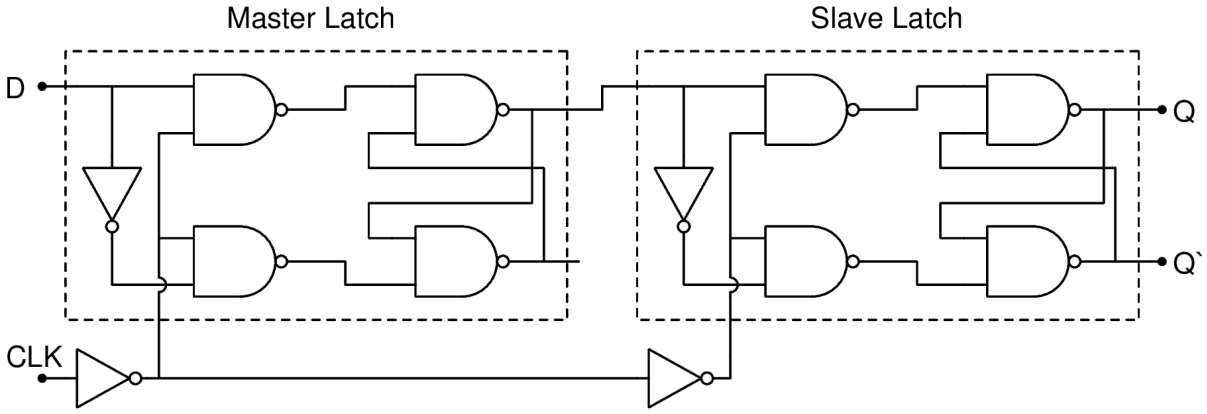

Figure 1.2: Schematic of NAND gate based D Flip-Flop.

Table 1.2: Truth Table of D-Flip Flop

Clock Edge	**Data (D)**	**Q (Next State)**	**Description**
No clock edge	X	Q (no change)	Flip-Flop holds its state
Rising edge (↑)	0	0	Q is reset to 0
Rising edge (↑)	1	1	Q is set to 1

A flip-flop consists of two latches arranged in a master-slave configuration. The input is applied to the master latch, while the output is taken from the slave latch. The clock edge that causes a flip-flop to latch the input data is referred to as the active edge of the clock for that specific flip-flop. A simple positive edge-triggered flip-flop can be constructed using two NAND latches connected in the master-slave configuration, as shown in Figure 1.2.

When the clock signal is low, the master latch operates in a transparent mode, storing the input 'D' on its output node. This output then serves as the input for the slave latch. Conversely, when the clock signal is high, the slave latch becomes transparent and latches the output of the master latch, which is then reflected on its own output node 'Q'. Overall, the flip-flop is only transparent during the positive edge of the clock signal, effectively addressing glitches and race condition issues commonly encountered in latch circuits.

The operation of the D flip-flop is described in Table 1.2. When there is no clock edge or inactive clock edge, the flip-flop remains in a memory state, retaining the previous data stored in it. When an active edge occurs (in this case, a positive edge), the input data signal 'D' is saved at the output node 'Q', which represents the memory update state for the flip-flop.

CHAPTER 2

Background and Related Work

2.1 Low Power Flip-Flop Architectures

2.1.0.1 Transmission Gate Flip-Flop (TGFF)

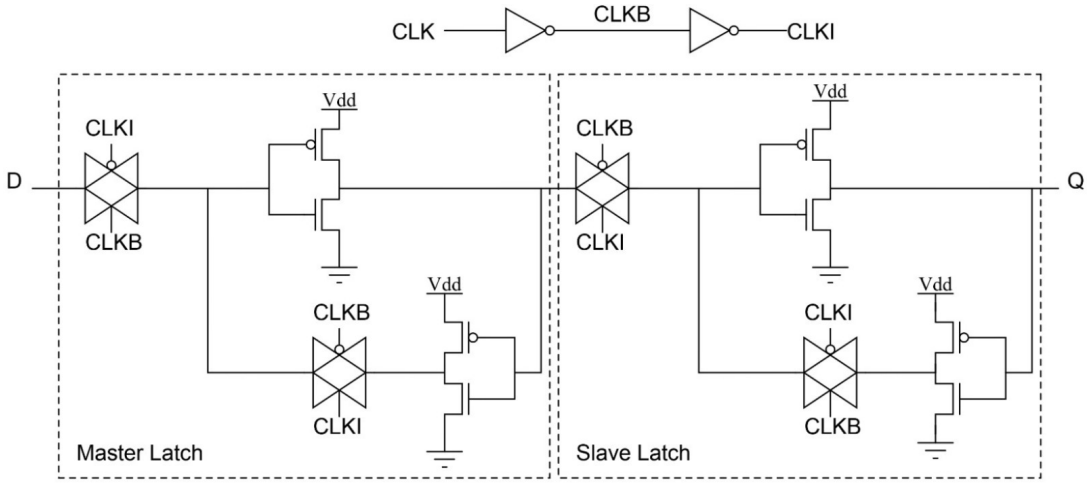

Figure 2.1: Schematic of Transmission Gate Flip-Flop (TGFF).

There are several implementations of flip-flops, with the Transmission Gate flip-flop (TGFF) being one of the most straightforward and fundamental architectures. As shown in Fig. 2.1, this flip-flop comprises of two transmission gate latches configured in a master-slave arrangement. Each latch is identical, featuring two transmission gates and two inverters. One of the transmission gates, along with two inverters, are arranged in a feedback configuration, while the second transmission gate connects to the latch's input.

The TGFF utilizes transmission gates, which require both a clock signal and an inverted clock signal. An internal clock buffer (ClkBuff) generates two internal clock signals: Clock Internal (CLKI) and its inverted counterpart, Clock Bar (CLKB). These signals are then fed as inputs to the transmission gates in the two latches.

It's worth noting that, instead of using a clock buffer, one could generate CLKB with a single inverter and use the actual input clock source directly (inplace of CLKI). However, this method is not commonly adopted in the industry, and we will discuss the reasons for this in the upcoming section.

Despite being a static, compact and simple implementation, the TGFF has a significant drawback: the presence of clock buffers results in substantial dynamic power consumption, even when there is no input change [1]. Specifically, when the clock is active but the input remains constant, the TGFF continues to consume considerable dynamic power due to unwanted toggling at the clocked nodes (CLKI and CLKB).

In IoT applications, devices typically operate at low voltage and low frequency levels and are frequently battery powered. To maximize battery life, it is essential to minimize leakage and dynamic power. Additionally, many IoT devices, such as wearables and small sensors, are compact, necessitating designs that maximize functionality within the limited silicon area. The TGFF (Transmission Gated Flip-Flop) is a small and straightforward flip-flop design; however, it experiences high dynamic power consumption.

Consider a scenario where a small IoT sensor is installed in a warehouse. This sensor continuously monitors its environment and alerts other devices when it detects a specific concentration of gas. Such a sensor IC needs to be small and power efficient. It should operate at a very low operating voltage, frequency and activity factor to prolong battery life. Moreover, the sensor will spend the majority of its operational time in sleep mode, awaiting a gas concentration to trigger a programmed interrupt routine. During this period, having a low power consumption will extend the battery life of this device.

If clock gating is not implemented, utilizing TGFF in this application could significantly drain battery power during sleep mode, as it continues to consume dynamic power due to the presence of clock buffers. Therefore, there is a need for a flip-flop architecture that relies solely on a single clock signal (and not on Clock Bar), which is known as a single-phase clocked flip-flop. Such flip-flops must have very low dynamic and leakage power to effectively extend battery life.

It is important to note that simply eliminating the clock buffer is not sufficient when proposing a new flip-flop architecture, as there could still be internal node transitions occurring even without input changes. When the flip-flop is expected to maintain its memory state, there should be minimal to no changes in the state of the internal nodes. These unwanted internal node transitions are referred to as redundant transitions.

In the following subsections, we will explore two flip-flop architectures that are single-phase clocked and free from redundant transitions.

2.1.0.2 Change Sensing Flip-Flop (CSFF)

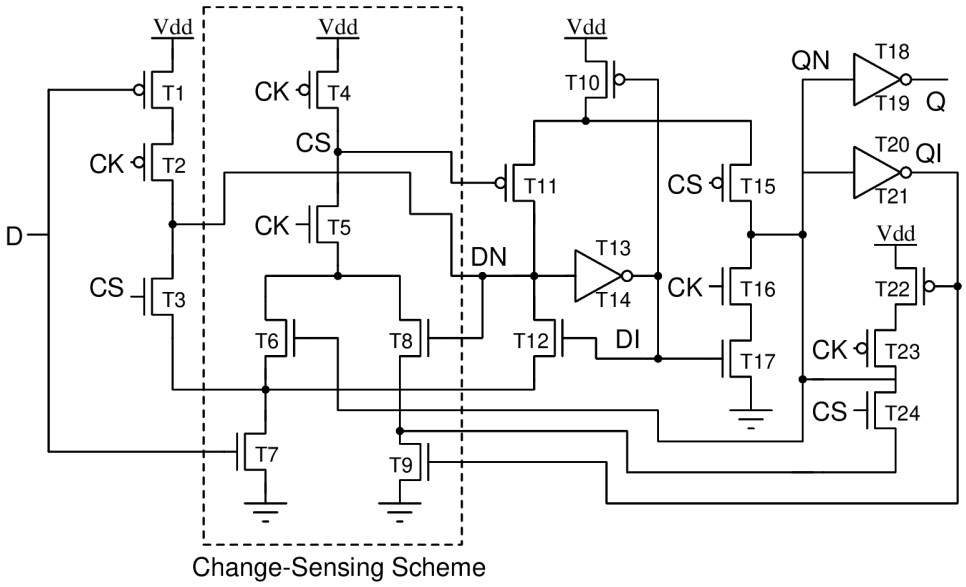

Figure 2.2: Schematic of Change-Sensing Flip-Flop (CSFF).

The Change Sensing Flip-Flop (CSFF) is a single-phase clocked flip-flop architecture designed to reduce power loss caused by unnecessary transitions in internal clocked nodes [1]. The schematic of CSFF is presented in Fig. 2.2, which is composed of 24 CMOS transistors, including 11 PMOS and 13 NMOS transistors. It has master and slave latches configuration. As its name implies, the CSFF features a unique dynamic Change-Sensing circuit that includes a dynamic node called the Change-Sensing Node (CS). This node detects changes in the input and allows data transfer from master latch to slave latch by performing transitions of internal nodes only when there is a change in the input signals. If there is no change in the input 'D', then there will be no transition in the internal nodes.

The brief of the CSFF working is as follows : When CK is low, CS is pre-charged to operating voltage. At the same time PMOS T10 is turned on if input 'D' is low or NMOS T17 is turned on if input 'D' is high. Till now no transition has taken place. Now when CK becomes high, if the input has changed, one of the discharge paths (either T5,T6,T7 or T5,T8,T9) will be turned on to discharge the dynamic node CS. This will trigger the updation of master latch and at the same time slave latch becomes transparent and this new master latch data is fed into slave latch to reflect it on the output of the flip-flop. So, When there is a change in input 'D' during CK is low, both master and slave latches hold thier previous data inside them, but certain transistors are turned on during this stage which will update the master latch with the new data when CK is high. When CK turns high, master latch becomes transparent and gets its value updated with the transistor which got turned on during the CK low stage. At the same time this new master values is captured by slave latch and the output of the flip-flop is updated.

2.1.0.3 Change Sensing Node (CS) Working in CSFF

The Change-Sensing Scheme used in CSFF is illustrated in Fig. 2.3. This dynamic logic detects changes in the input signal 'D'. When a change is detected, the CS node discharges, and internal transitions occur to latch the new data. If there are no changes in 'D', no unnecessary transitions take place. It is important to note that 'D' represents the input signal, 'QI' is the internal copy of the output node, 'DN' is the internal signal that is the inverse of 'D,' and 'QN' is the inverse of the output signal 'Q.'

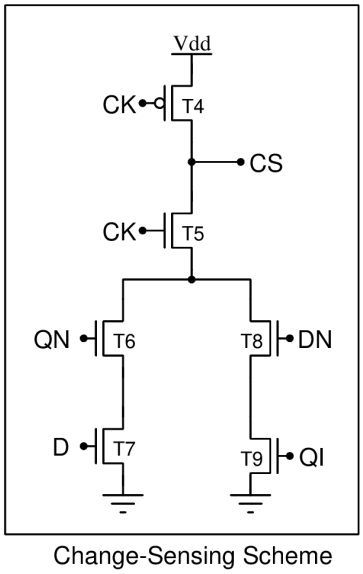

Figure 2.3: Schematic of Change-Sensing Circuit.

Its detailed working is explained below:

1. During the pre-charge phase, when the clock signal is low, the node CS is charged to the operating voltage through the PMOS transistor T4. The node CS is dynamic in nature and holds its voltage until the evaluation phase, when the clock signal transitions to high.

2. During the evaluation phase, if it was found that input 'D' was changed during the pre-charge phase, the node CS is discharged through either the transistors T5, T6 and T7, or T5, T8 and T9; otherwise, it retains its voltage. Internal transitions occur only when the node CS is discharged, which helps to prevent unnecessary transitions in the CSFF (Change Sensing Flip-Flop) architecture.

3. If the current value of the input 'D' is low, Clock (CK) is also low, then 'QI' will also be low, while 'QN', 'CS' and 'DN' will be high. Now if Data is changed during the pre-charge phase, those transistors will be turned on which will update 'DN' to its new value of low in evaluation phase. In the evaluation phase, when the clock signal is high, 'DN' will be updated to its new value which marks the updation of master latch, a discharge path for the CS node is created through the NMOS transistors T5, T6, and T7. This path discharges the dynamic node CS and triggers the flip-flop to initiate internal transitions and store the new data from 'D'.

4. Conversely, if the current value of input 'D' is high, CK is low, CS is high, then 'QI' will also be high, while 'QN' and 'DN' will be low. If in the pre-charge phase 'D' changes to low, those tranistors will be turned on which will update 'DN' to its new value to high in evaluation phase. During the evaluation phase ie when CK is high, due to change in input 'D', a discharge path for the CS node will be provided by the NMOS transistors T5, T8, and T9. This will also discharge the dynamic node CS, triggering the flip-flop to commence internal transitions and store the new data from 'D'.

2.1.0.4 Potential Contention Issues in CSFF

Due to the dynamic nature of Change Sensing Flip-Flop, there may exist contention conditions which could lead to failure of the flip-flop functionality. This raises issues for circuit robustness and stability specially at very low voltages. The author in [2] performed detailed analysis and found possible contention conditions for CSFF. A brief explanation of one of the contention condition is given below.

- If D transitions from low to high while CK is high, and CS has not yet discharged and remains somewhat high, and both DN and QN are also high. This condition may cause the CS node to stay high for a longer duration. As we discussed earlier, in order to update the master latch, the CS node must be discharged. Ideally, the high value of DN should be stored inside the master latch as soon as CS is discharged. However, if CS remains floating for too long, there is a discharge path for DN, which poses a risk of it discharging through T3 and T7. If DN discharges before CS, incorrect data may be latched inside the master latch and subsequently transferred to the slave latch.

Additional contention conditions are discussed in the [2]. To address the contention issues of the Change-Sensing Flip-Flop (CSFF), the author proposes a new flip-flop architecture described below.

2.1.0.5 Contention Free Change Sensing Flip-Flop (C2SFF)

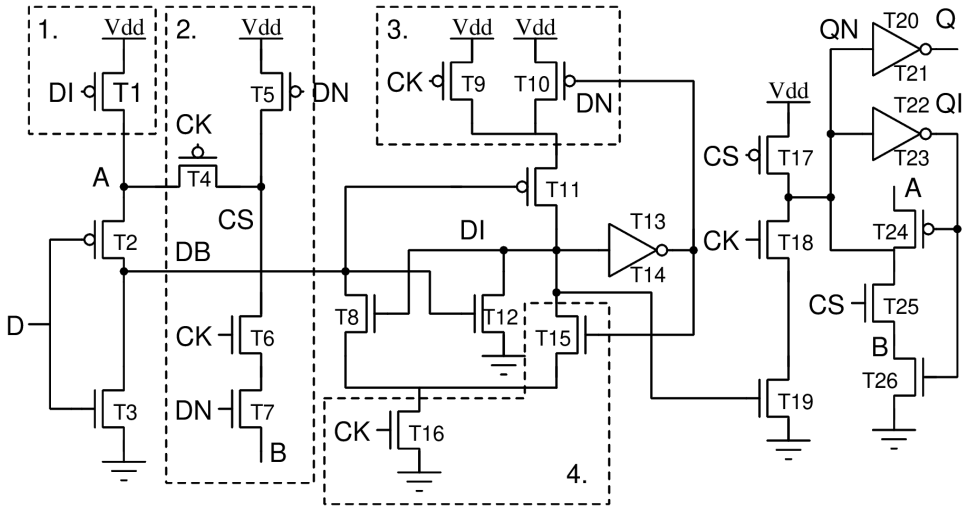

Figure 2.4: Schematic of Contention-Free Change-Sensing Flip-Flop (C2SFF).
1. Keeper Circuit.
2. Revised Change Sensing Scheme.
3. Conditionally Functional Pullup Network.
4. Pull Down Network For DN.

To enhance the robustness and efficiency of the Change Sensing Flip-Flop (CSFF), the authors of [2] introduced a new flip-flop architecture called the Contention-Free Change Sensing Flip-Flop (C2SFF), which addresses the shortcomings of the original CSFF design.

One major issue with the CSFF was its dynamic operation, primarily due to the Change-Sensing (CS) node, which led to several contention conditions that challenged the robustness of the design. One of the improvement made in C2SFF is the introduction of a revised change-sensing scheme, which reduces the pull-down path from two in CSFF to one in the new architecture.

To tackle the contention issues mentioned earlier, a conditionally functional pull-up network was incorporated. This network ensures that the node voltage at DN remains high by preventing any unintentional pull-down paths that arise during contention. Additionally, a keeper was introduced to address further contention issues related to the pull-up paths for the DN and QN nodes. Lastly, a pull-down network for DN was added to resolve contention caused by the absence of a pull-down path for DN.

Detailed information regarding the contention conditions in CSFF and their proposed solutions and working can be found in [2]. With these modifications, the architecture in C2SFF becomes a contention-free flip-flop, featuring lower leakage and dynamic power consumption compared to the CSFF architecture.

2.1.0.6 Presence of Clock Buffer in Flip-Flop Design

The Transmission Gate Flip-Flop (TGFF) requires both a clock signal (CLK) and its inverted counterpart (CLKB) for proper functioning, due to the presence of a transmission gate. To create CLKB from CLK, at least one inverter is needed. However, using the clock tree's clock signal directly in the design is not standard practice in the VLSI industry. Instead, a local copy of the clock signal is generated using a clock buffer known as Clock Internal (CLKI), which is then utilized for the internal operation of the flip-flop. This approach offers several advantages:

1. Restoration of Clock Signal Integrity: The clock buffer helps restore the slope of the clock signal, which is crucial for ensuring proper timing within the circuit.
2. Load Management on the Clock Tree Network: A single clock tree driver cannot efficiently drive thousands of flip-flops on its own, so using a local copy helps manage this load.

As a result, whenever a standard cell for a flip-flop is designed, a clock buffer is included. However, the presence of this clock buffer increases the area required for the design and also consumes a significant amount of dynamic power.

The CSFF and C2SFF were introduced as alternatives that do not require CLKB and can potentially use the clock tree's clock signal directly, as no inverters are needed. But if there are no clock buffers, it is assumed that the clock buffer is present outside the flip-flop circuit and is shared by several flip-flop cells.

During the layout implementation, we decided to include clock buffers in the CSFF and C2SFF designs due to the reasons mentioned above. For a comprehensive evaluation, we also removed the clock buffer (and assumed to be shared at SoC level by multiple flip-flop cells) from one version each of the CSFF and C2SFF designs to assess their performance and sustainability with and without the clock buffer.

2.2 Sustainability

2.2.1 Introduction to Sustainability

Since the invention of the transistor, there has been an exponential growth in the total number of devices using integrated circuits. This growth has led to a massive increase in the manufacturing and operation of such devices. The fabrication of Very-Large-Scale Integration (VLSI) designs requires a considerable amount of energy. For instance, semiconductor manufacturing companies like Taiwan Semiconductor Manufacturing Company Limited (TSMC) use more electricity than the whole nation of Sri Lanka [3]. A recent report indicated that TSMC alone

consumed 250 gigawatts (GW) of energy in 2023, a quantity sufficient to satisfy the energy needs of a large nation [4].

Moreover, it is expected that the total number of Internet of Things (IoT) devices will grow to 40 billion by 2030 [5]. This surge will necessitate an enormous amount of energy, both for fabricating these devices and for powering them throughout their operational lifetime. The production of such significant amount of power will inevitably lead to a huge amount of carbon emissions, contributing to global warming and climate change.

In response to the increasing environmental impact caused by carbon emissions, major semiconductor manufacturing companies have committed to net-zero, or carbon neutrality, targets. For example, Apple has set an ambitious goal to achieve carbon neutrality by 2030. In their environmental impact report, Apple stated that approximately 59% of their carbon emissions come from product manufacturing [6].

Hence, there is an urgent need to develop integrated circuits with minimal environmental impact, a concept known as sustainable design. This can be accomplished if designers have access to methods for identifying sustainable design architectures and making choices that promote sustainability by requiring the least possible energy to fabricate and operate during their lifetime.

2.2.2 Related Work in Sustainability

Life Cycle Assessment (LCA) is a widely used method for evaluating the sustainability of a product. It provides valuable information about the emissions generated at various stages of a product's life cycle. For example, STMicroelectronics, in its LCA report, stated that the production of MEMS devices involves five life cycle stages. Among these stages, the stage of manufacturing at the STMicroelectronics site contributes to 57% of total carbon emissions [7]. This highlights that reducing emissions during the fabrication and manufacture of semiconductor devices has significant potential for lowering total carbon emissions.

The Greenhouse Gas (GHG) emissions protocol provides quantifiable levels of carbon emissions, which are categorized into three scopes [8]. These scopes are defined based on the life cycle stage at which the emissions occur.

1. Scope 1: These are the direct emissions produced during operations at the company's office or facilities. For example, carbon emissions from running the facility, refrigerants, transportation, etc.

2. Scope 2 : It refers to indirect emissions that are not produced directly by a company, but rather occur as a result of the services utilized by the company. For instance, this includes the emissions generated during the production of electricity used for the company's operations.

3. Scope 3 : These emissions refer to indirect emissions associated with the processes that facilitate a product's life cycle. This includes the extraction of raw materials, product transportation, logistics, and supply chains.

There have been several attempts to evaluate sustainability of semiconductor devices and their fabrication processes over the years. In 2000, the EE-Toolbox was introduced as a sustainability assessment methodology aimed at evaluating materials based on their toxicity and recycling potential [9]. In 2012, the Eco-Reliability concept was introduced, which follows a life cycle assessment (LCA) approach; however, it lacks a quantitative assessment [10].

In 2017, a parameterized sustainability framework was developed that demonstrated the impact of changing metal stack, but it was primarily focused on product-level design rather than the standard cell level, which is of greater interest to designers [11].

In 2022, a paper presented a detailed assessment of the carbon footprint for common products, using the GHG protocol. However, it operates at a very high abstraction level, making it less useful for designers [12].

In 2024, the Eco-Reliable framework was launched, which evaluated environmental impact in conjunction with manufacturing overhead, with consideration on environmental factors. [13]. Furthermore, in 2024, an open-source framework was created to gauge the sustainability of chiplets based heterogeneous design [14]. Both frameworks did not include decision-driven analysis specifically aimed at standard cell levels for designers.

2.2.3 Overview of Sustainability Analysis

The product life cycle assessment can be used to conduct a sustainability analysis based on the greenhouse gases (GHG) emitted into the environment [12]. From a designer's perspective, there are two main areas where carbon emissions occur: during the fabrication of the device, referred to as the embodied carbon footprint, and throughout its operational lifetime, known as the operational carbon footprint. Both footprints can be estimated based on the energy consumed in each area, which can then be converted into equivalent CO_2 emissions. Increased energy consumption leads to higher CO_2 emissions and indicates a less sustainable design.

However, looking at the embodied and operational carbon footprints individually provides an incomplete picture of sustainability. Therefore, they are added together to calculate the total carbon footprint, which gives a comprehensive view of the design's sustainability.

2.2.3.1 Embodied Carbon Footprint

These are the emissions that occur during the manufacturing and fabrication of a design. By the time a device reaches the end user, these emissions have already been produced. Such emissions include those from designing, fabrication, testing, shipping, and more. From a designer's perspective, fabrication and manufacturing are the primary areas of concern.

There is a need for a designer-focused framework that can assist designers in making informed choices regarding design decisions, such as the architecture, cell area, layout, routing style, and metal layers used. This will help achieve sustainable fabrication of the design.

Area is one of the most important parameter influencing the embodied sustainability of the design. A compact and small area leads to a more sustainable design, as it requires less silicon area on the wafer. This means that the same wafer area can produce more design dies. Also, smaller area increases the yield of the fabrication process. Consequently, the greenhouse gas emissions (GHG emissions) are spread over a larger number of designs, reducing the GHG emissions associated with each die and making them more sustainable.

2.2.3.2 Operational Carbon Footprint

These are the emissions generated at the user end during the operation of the design. If the design consumes a large amount of energy during its operation, it will lead to higher greenhouse gas (GHG) emissions due to the electricity production required. From a designer's perspective, both power consumption and performance are primary concerns when estimating the operational carbon footprint.

High power consumption means that more energy is used over the device's lifetime, resulting in greater GHG emissions. Conversely, a better-performing device can complete the same computations in less time, which reduces its active time. This shorter operating duration leads to lower energy consumption and, consequently, reduced power usage. As previously mentioned, less energy consumption results in lower GHG emissions and contributes to more sustainable design. The packing size and material often depend on the power consumption and heat dissipated by the design. A design with high power consumption leads to increased heat dissipation, which may require more complex and larger packaging to manage that heat. This can impact the overall embodied footprint and may result in a less sustainable design. Therefore, lower power consumption contributes to a more sustainable design.

CHAPTER 3

Post-Layout Analysis

3.0.1 Introduction

In the previous section, we discussed three flip-flop architectures: TGFF, CSFF, and C2SFF. We implemented various versions of all three flip-flop architectures using the 65nm technology node, utilizing the Low Standby Power technology provided by STMicroelectronics. For the layout implementation, we employed Cadence Virtuoso, and for post-layout simulations, we used Eldo.

After successfully completing the layouts using Cadence Virtuoso, we conducted Design Rule Checks (DRC) and Layout Versus Schematic (LVS) checks on all design implementations. Following these checks, we performed layout extraction to capture the parasitic capacitances and resistances, and then conducted post-layout simulations using the Eldo tool. For the IoT application we have taken 0.7V as standard voltage of operation and 10% swtching factor with 100MHz frequency and 40% switching factor with 400MHz frequency during power calculations.

3.0.2 Layout Implementations

As flip-flops are primarily designed and utilized as standard cells, we have implemented all designs accordingly, maintaining a track height of 13 tracks (relative to the Metal 1 or M1 layer). The single track height is determined by summing the minimum width of M1 and the minimum distance required between two M1 layers, known as the minimum DRC (Design Rule Check) between them. As both the minimum width and minimum DRC for M1 are $0.1\mu m$, the resultant single track height is calculated to be $0.2\mu m$. Given that the standard cell layout consists of 13 tracks or 13T, the overall height of all layout implementations totals $2.6\mu m$.

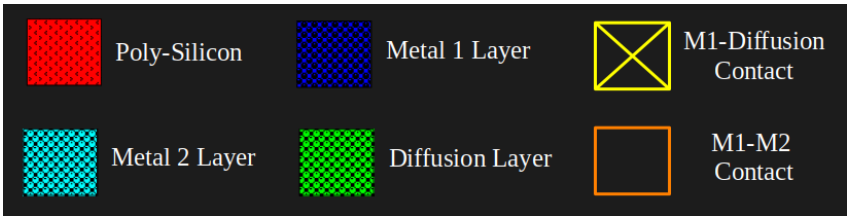

Figure 3.1: Legend for metal layers and contacts utilized in layout implementation.

In our layout designs, we have used different layers and contacts which can be found in Fig. 3.1. During the layout implementations we primarily utilized the M1 metal layer for routing purposes. However, to evaluate the effects of using a higher metal layer (M2 in our case), we strategically incorporated the M2 layer to create different layout implementation variations. This approach helps us gain a deeper understanding of the impact of using a higher metal layer on sustainability of the design.

As discussed before, while implementing the CSFF and C2SFF we have implemented the clock buffer. But we also implemented one each flip-flop architecture without clock buffer to see the impact of clock buffer on flip-flop performance and sustainability.

For a fair comparison we have sized all the flip-flops for 300ps propagation delay at Slow/Slow, 1.08V and 125C with a load capacitance of 20fF connected at the node 'Q'

3.0.2.1 TGFF (M1 Only)

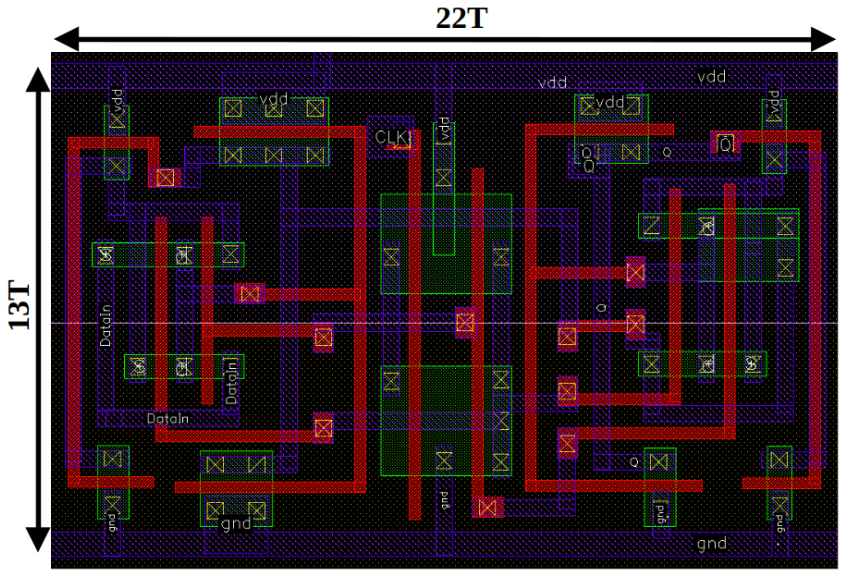

Figure 3.2: Layout of Transmission Gate Flip-Flop (M1 Only).

The layout of the Transmission Gate Flip-Flop (TGFF) is depicted in Fig. 3.2. This implementation utilizes only the Metal 1 layer. The design dimensionally measures a height of 13 tracks (13T) and a width of 22 tracks (22T). Consequently, the total area occupied by the layout is calculated to be $11.44\mu m^2$. Moving forward this layout will be recognized as TGFF(M1 Only).

3.0.2.2 TGFF (M1 + 2M2)

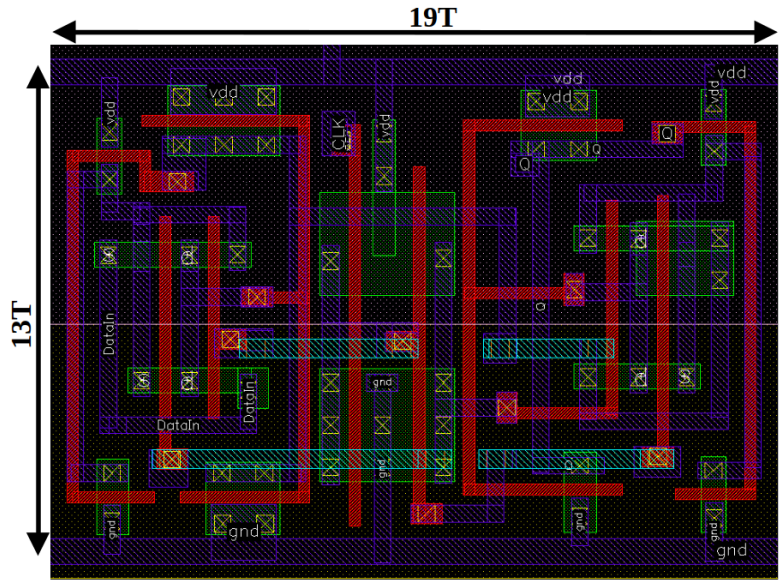

Figure 3.3: Layout of Transmission Gate Flip-Flop (M1 + 2M2).

The layout depicted in Fig. 3.2 can achieve greater compactness in terms of area by incorporating higher-level metal layers. As illustrated in Fig. 3.3, we have employed two additional Metal 2 layers to create a more compact design. Therefore, the width of the layout has reduced from 22T to 19T, while the height remains unchanged at 13T. This modification has led to a decrease in area from 11.44μm^2 to 9.88μm^2. We will call this layout design as TGFF(M1+2M2).

3.0.2.3 CSFF (M1 + 1M2)

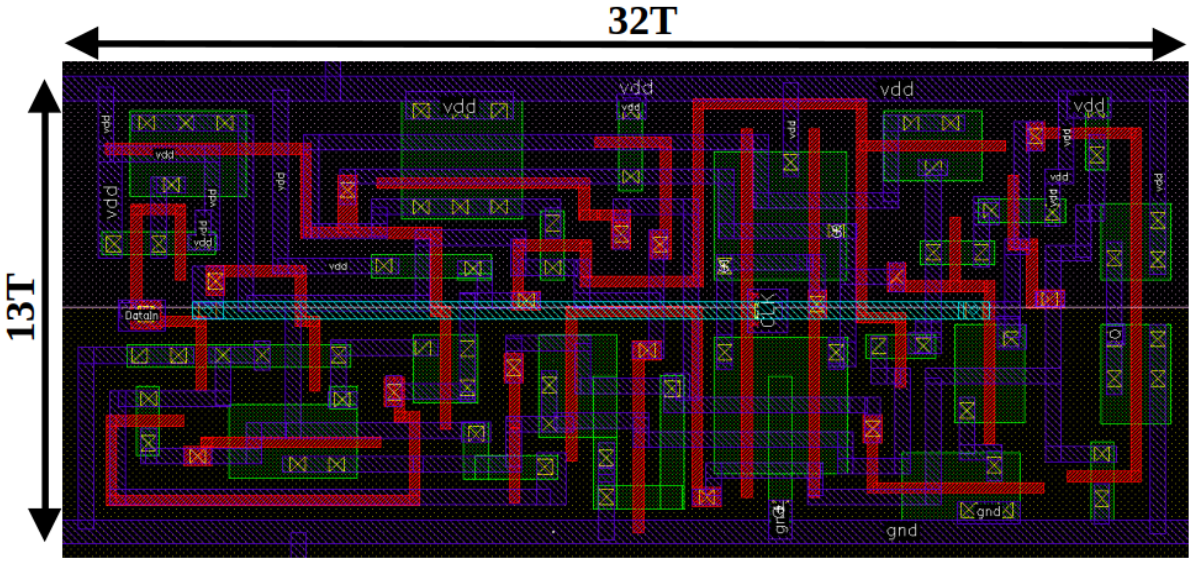

Figure 3.4: Layout of Change-Sensing Flip-Flop (M1 + 1M2).

As shown in Fig. 3.4, we have successfully implemented the Change Sensing Flip-Flop (CSFF) in along with a clock buffer, utilizing primarily Metal 1 layers and a single Metal 2 layer. The design features a height of 13T and a width of 32T, resulting in a total area of 16.64μm^2. This design will be referred to as CSFF(M1+1M2). As we observed with the TGFF, by increasing the Metal 2 layer in this design, we can expect further reduction in the overall area.

3.0.2.4 CSFF (M1 + 2M2)

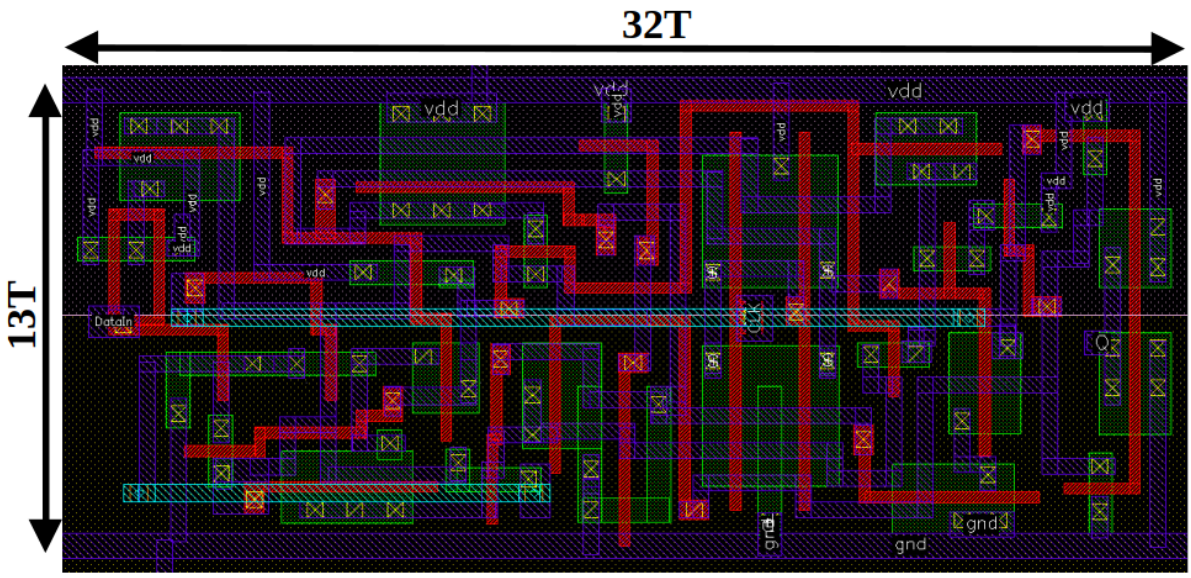

Figure 3.5: Layout of Change-Sensing Flip-Flop (M1 + 2M2).

Upon introducing an additional Metal 2 layer during the layout implementation, we observed that there was no reduction in the overall area of the design. As illustrated in Fig. 3.5, while some free space was generated within the layout, the overall design width remained unchanged at 32T. Being a 13 Track standard cell design, the height of the design stayed constant at 13T. Hence, the total area of the design remained at 16.64μm^2. We will refer this design as CSFF(M1+2M2).

3.0.2.5 CSFF (M1 + 3M2)

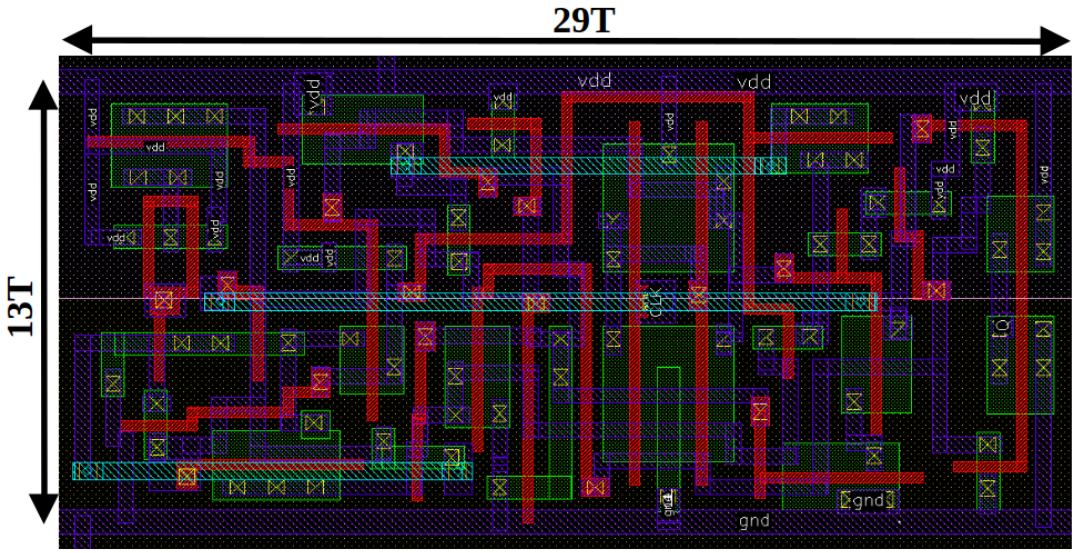

Figure 3.6: Layout of Change-Sensing Flip-Flop (M1 + 3M2).

After observing the creation of additional free space in the CSFF (M1 + 2M2), we concluded that there was potential for area reduction by introducing a third Metal 2 layer. As illustrated in Fig. 3.6, the addition of this third M2 layer resulted in a reduction of the design width from 32T to 29T, while the height remained unchanged at 13T. Consequently, the introduction of the third M2 layer led to a decrease in area from 16.64μm^2 to 15.08μm^2. We will refer to this design implementation as CSFF (M1 + 3M2). It is important to note that all CSFF design implementations discussed above have been carried out with a clock buffer.

3.0.2.6 C2SFF (M1 + 3M2)

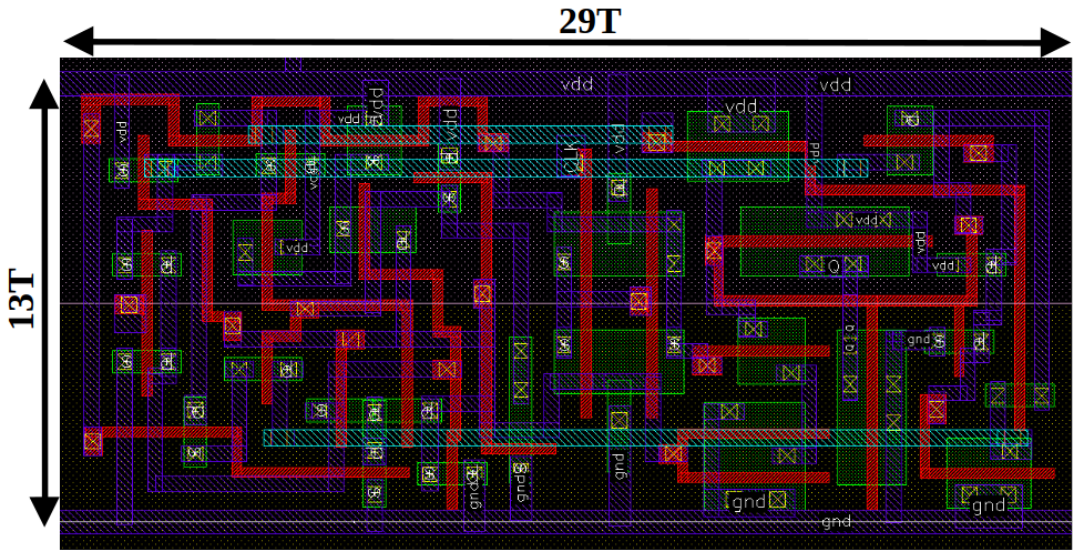

Figure 3.7: Layout of Contention-Free Change-Sensing Flip-Flop (M1 + 3M2).

The layout implementation of the Contention Free-Change Sensing Flip-Flop (C2SFF) is depicted in Fig. 3.7. We opted to utilize three Metal 2 layers to facilitate a comparative analysis with the CSFF (M1+3M2), which represents the most dense and compact layout configuration for the CSFF. This approach was taken to enable an evaluation of both the compact CSFF and the C2SFF implementation, which employs three Metal 2 layers and occupies the least area, against the TGFF in terms of sustainability. We will refer to this implementation as C2SFF(M1+3M2). It is to be noted that like CSFF implementations, this design also has clock buffer within it. Our layout findings indicate that, similar to the CSFF (M1+3M2), both the width and height of C2SFF(M1+3M2) remain consistent at 29T and 13T, respectively. Hence, the area also remains unchanged at 15.08μm^2.

3.0.2.7 CSFF (M1 + 3M2) with No Clock Buffer

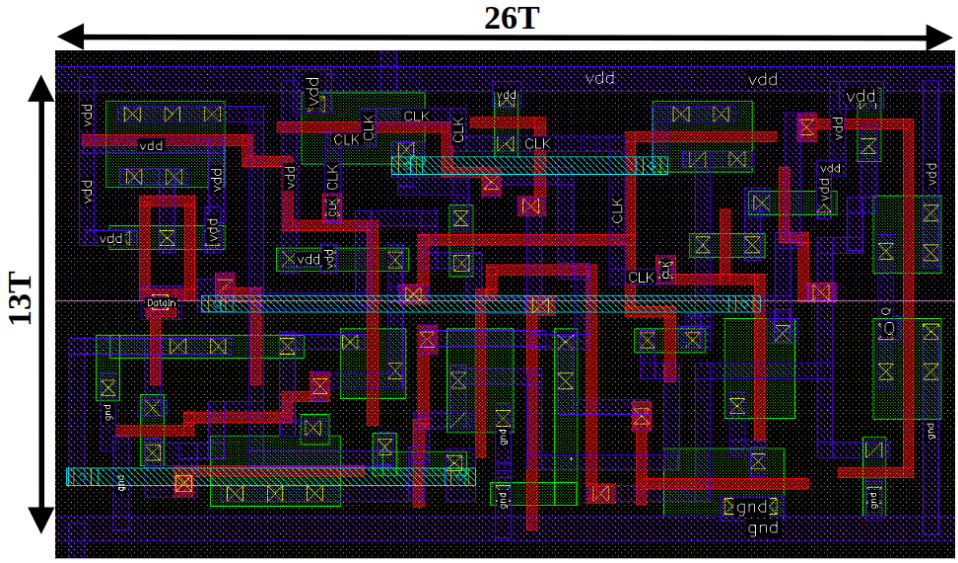

Figure 3.8: Layout of Change-Sensing Flip-Flop (M1 + 3M2) with No Clock Buffer.

The original paper intended for the CSFF to be implemented without a clock buffer; however, we included a clock buffer for practical reasons. To conduct a comparative analysis of CSFF (M1+3M2) without a clock buffer against TGFF design implementations, we removed the clock buffer (assumed to be shared at SoC level). After this adjustment, in Fig. 3.8, we observed that the width of the flip-flop decreased from 29T to 26T, while the height remained constant at 13T. This led to a reduction in area, from 15.08μm^2 to 13.52μm^2. We will refer to this design as "CSFF(M1+3M2) No ClkBuff," where 'No ClkBuff' indicates the absence of clock buffers in the design layout implementation.

3.0.2.8 C2SFF (M1 + 3M2) with No Clock Buffer

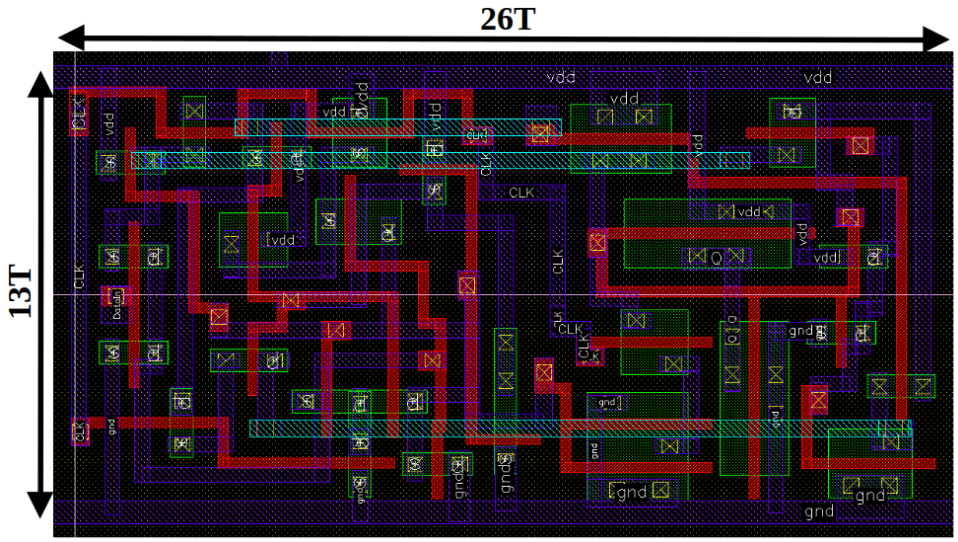

Figure 3.9: Layout of Contention-Free Change-Sensing Flip-Flop (M1 + 3M2) with No Clock Buffer.

We have also eliminated the clock buffers from the C2SFF(M1+3M2) design implementation for reasons similar to those applied to CSFF(M1+3M2). It can be seen in Fig. 3.9 that we have achieved a reduction in design width from 29T to 26T, while the height remains unchanged at 13T. Additionally, the total area has decreased from 15.08μm^2 to 13.52μm^2. This design will be refered as "C2SFF(M1+3M2) No ClkBuff"

It is important to clarify that, in this work, clock buffers are assumed to be included in the design unless stated otherwise. For example, when we refer to CSFF(M1+3M2), it is understood that a clock buffer is implemented within it. However, if we mention CSFF(M1+3M2) with "No ClkBuff," this indicates that clock buffers have been removed from the design.

3.0.3 Figure of Merits

In VLSI design, it is crucial to conduct a comparative analysis of various design alternatives to evaluate trade-offs among power, performance, and area. This analysis is guided by specific figures of merit that align with our target features and overall project objectives. By assessing these metrics, we can make informed decisions that best suit our design goals.

In any digital circuit, power consumption is primarily composed of two key components: Dynamic Power and Leakage Power. For flip-flops, important performance metrics include Clock To Q delay, Setup Time, and Hold Time. Additionally, the area of the design is another critical figure of merit that often influences the selection of the architecture to be implemented in our design.

3.0.3.1 Leakage Power

Leakage refers to the unwanted flow of current in a circuit even when the transistors are turned off. In the case of a flip-flop, we calculate leakage by keeping the clock signal low and maintaining a static value on the data pin. For instance, if we set both the clock and data pins to low and integrate a small interval of time for the current I(VD) during this state, we can calculate the total leakage charge. Once we have the total charge, we divide it by the time interval to determine the leakage current when the data pin is low. A similar analysis can be conducted when the data pin is high while the clock pin remains low. This value will represent the leakage current when the data pin is high. The overall leakage of the flip-flop is the average of these two leakage current values. Typical-Typical, 0.7V and 25°C is the PVT condition taken and load capacitance of 20fF was removed during the simulation.

Now leakage current could be used to determine the leakage power by using the Eq. 3.1.

$$\text{Leakge Power} = (V \times I_{leakage}) \tag{3.1}$$

where, '$I_{leakage}$' is the leakage current of the flip-flop and 'V' is the operating voltage.

3.0.3.2 Dynamic Power

For a flip-flop with two input signals, Data and Clock, we calculate the dynamic power for each separately. As shown by Eq. 3.2, adding the data power and clock power gives us the dynamic power consumed by the flip-flop.

$$\text{Dynamic Power (Flip-Flop)} = (DataPower + ClockPower) \tag{3.2}$$

We know for a CMOS circuit, dynamic power is consumed mainly for charging and discharging of the load and parasitic capacitance. The total power drawn from supply is represented by Eq. 3.3.

$$\begin{aligned} \text{Dynamic Power} &= (C \times V) \times V \times f \times \alpha \\ &= Q_{dyn} \times V \times f \times \alpha \end{aligned} \tag{3.3}$$

where, 'C' represents the total capacitance being charged or discharged, 'V' denotes the

operating voltage, 'f' indicates the operating frequency, 'α' is the switching factor, and 'Q_{dyn}' refers to the dynamic charge consumed.

With the exception of Q_{dyn}, all the other variables are known to us in Eq. 3.3. We have determined Q_{dyn} using post-layout simulations conducted with the Eldo simulation tool. During the simulation we have removed the load capacitance of 20fF which was connected to the output node 'Q'. This makes the dynamic power analysis independent of load, and we can say that dynamic power consumed now will only be due to the internal node transitions which will be unique to each design implementation. Typical-Typical, 0.7V and 25°C is the PVT condition taken during the simulation.

Data Power : To calculate data power, we first kept the clock signal low and then made low-to-high transitions on the data input pin. This resulted in a peak in the current (I(VD)). By integrating this peak, we obtained the total charge, and after subtracting the leakage component, we determined the dynamic charge consumed. This value represents the total dynamic charge consumed when the data pin transitions from low to high. Using Equation 3.3, we can calculate the dynamic power for the data pin during the low-to-high transition. A similar analysis can be conducted for the data pin transition from high to low to find the dynamic power during that change as well. The average of both dynamic power values will be considered as the overall data dynamic power for the flip-flop.

Clock Power : The calculation for clock power closely resembles that for data power. First, we need to set up the Data pin so that, upon the arrival of the clock edge, the state of the flip-flop changes, meaning that the output node 'Q' must toggle when the clock edge occurs. For instance, if the current state of 'Q' is low, we will set the Data high well before the clock edge is applied. Once the clock edge is given, the output node 'Q' will switch from low to high. This transition results in a peak in the I(VD) curve. We then integrate this peak to obtain the total charge consumed during this transition and subtract the leakage component to find the total dynamic charge used by the flip-flop to store the high Data state upon the arrival of the clock edge. Equation 3.3 can then be used to calculate the clock dynamic power when the Q pin transitions from low to high. A similar analysis can be performed when the Q pin goes from high to low. The average of these two values is considered the clock power.

3.0.3.3 Clock to Q Delay

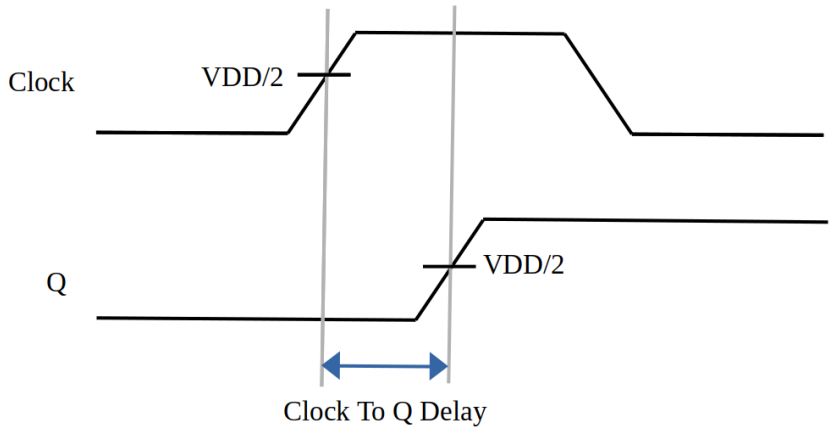

Figure 3.10: Timing diagram showing Clock to Q Delay.

At the active edge of the clock, the input signal D is latched into the flip-flop and subsequently transferred to the output node Q. The time delay between the occurrence of the active edge and the change in output at node Q is referred to as the Clock to Q delay (C2Q). As shown in Fig. 3.10, C2Q delay for the transition of the output node Q from low to high is called tplh, while the C2Q delay for the output node Q transitioning from high to low is called tphl. In this work, we calculated the C2Q delays (tplh and tphl) and computed their average to estimate the overall propagation delay. We used the worst case PVT condition for delays ie Slow/Slow, 0.63V, 125°C for the calculation of Clock To Q delays for the flip-flop designs. The load capacitance of 20fF was present during the simulation.

3.0.3.4 Setup Time and Hold Time

Setup time is the minimum duration before the active edge of the clock, during which the input data 'D' must stay stable to ensure the data is latched correctly. If the data signal D changes during this setup period, it leads to a setup time violation, which makes it impossible to guarantee whether the latched data is the input 'D' or not.

Hold time refers to the minimum period after the active edge of the clock, during which the input data must remain stable to prevent corruption of the latched input data. If the data signal D changes within this hold window, it results in a hold time violation, making it uncertain whether the latched data is correct or corrupted.

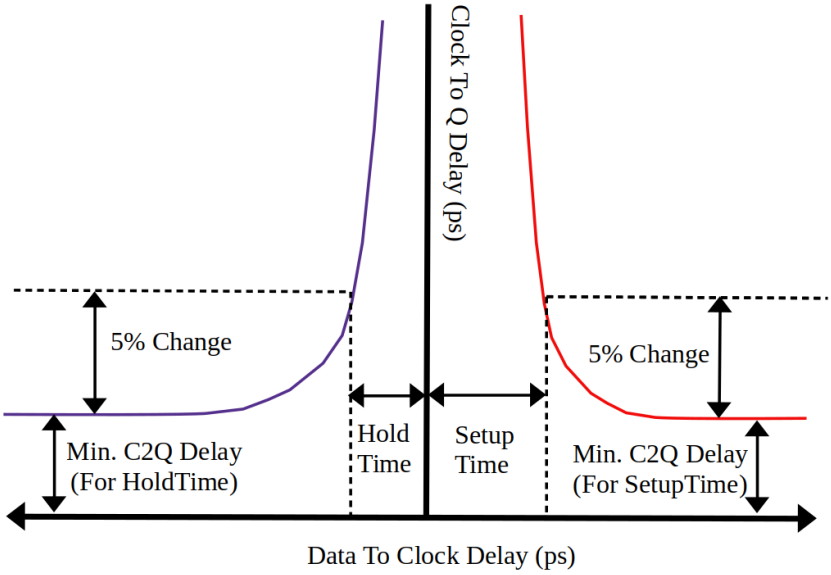

Figure 3.11: Showing how to calculate Setup and Hold Time using D2Clk vs C2Q Plot.

To determine setup time, we bring the change in the 'D' input closer to the active clock edge before the edge occurs, which increases the Clock to Q (C2Q) delay and leads to a setup violation. Conversely, to find hold time, we introduce the change in 'D' after the clock edge closure to the active clock edge, resulting in an increase in C2Q delay due to a hold violation. As illustrated in Fig. 3.11, when a flip-flop begins to experience setup or hold time violations, the C2Q delay increases compared to the scenario without violations. The C2Q delay under normal conditions, without violations, is referred to as the minimum C2Q delay.

In this study, we estimated the setup and hold times by calculating the D to Clock (D2Clk) delay values when we observed a 5% increase in C2Q delay with respect to its minimum value. The setup and hold times were determined through separate simulations. For setup time, we examined the Process, Voltage, and Temperature (PVT) conditions of Slow/Slow at 0.63V and 125°C, which represent the worst-case scenario for setup time. For hold time, we utilized the PVT conditions of Fast/Fast at 0.77V and -40°C, which represent the worst-case scenario for hold time. For evaluation of setup and hold time, load capacitance of 20fF was present during simulation. Setup and hold time can be found when we want to store 0 or 1 into the flip-flop. In Table 3.1, we have noted only the worst case among them.

3.0.3.5 Area

The area of a design is calculated by multiplying its height by its width. For example, the height of the TGFF (M1 Only) is 13 tracks, which is equivalent to 2.6 μm (as size of single track is 0.2μm), and the width is 22 tracks, which is equal to 4.4μm . Therefore, the total area of the design is calculated as 2.6 multiplied by 4.4 , resulting in an area of 11.44μm^2 .

3.0.4 Post Layout Simulations Results and Observations

The post-layout analysis results concerning performance (delays) and area are summarized in Table 3.1. We note that TGFF (M1 + 2M2) has the smallest design area at 9.88μm^2, while CSFF (M1 + 1M2) and CSFF (M1 + 2M2) show the largest area at 16.64μm^2. The TGFF layout data suggests that adding an additional M2 layer can help reduce the design area. In contrast, the CSFF layout implementations indicate that adding a single M2 layer may not consistently lead to area reduction. Therefore, it might be necessary to incorporate an additional M2 layer to achieve area savings. We conclude that if adding one M2 layer does not reduce the area, designers should consider adding more M2 layers in hopes of eventually saving area. This heavily depends on the layout and routing style chosen by the designer.

Additionally, when clock buffers were removed from CSFF and C2SFF, we observed a significant reduction in area. Although their design areas are still larger than that of TGFF, the values have become more comparable.

Table 3.1: Summary of Post Layout Simulation - Delay and Area Results

Design Name	**M2 Metal Used**	**Propagation Delay (ps)**	**Setup Time (ps)**	**Hold Time (ps)**	**Design Area(μm^2)**
TGFF	0	1388.4	286.75	32.5	11.44
	2	1391.2	287.5	32.3	9.88
CSFF	1	1600.8	571.6	62.6	16.64
	2	1601.2	573.2	62.2	16.64
	3	1578.9	467.6	12.9	15.08
C2SFF	3	1587.8	967.9	-162.6	15.08
CSFF No ClkBuff	3	1221.8	757.7	-81.16	13.52
C2SFF No ClkBuff	3	1154.9	1314.8	-266.7	13.52

Upon analyzing the performance results, we observe that C2SFF, which has no clock buffer, exhibits the shortest propagation delay. In contrast, the CSFF (M1 + 2M2) with clock buffer has the longest propagation delay. It is important to note that both the CSFF and C2SFF designs, when equipped with a clock buffer, have worse propagation delays compared to the TGFF implementation. However, the CSFF and C2SFF designs without a clock buffer demonstrate the best propagation delays, even outperforming the TGFF implementations.

The delay results presented in Table 3.1 are consistent with the findings of [2]. The author of that paper compared TGFF, CSFF No ClkBuff, and C2SFF No ClkBuff, concluding that C2SFF exhibits the least propagation delay. Additionally, the paper indicates that TGFF has the best

setup time, while C2SFF demonstrates the best hold time. These trends are also reflected in our Table 3.1.

Table 3.2: Summary of Post Layout Simulation - Power Results(At 10% Switching Factor | 100Mhz)

Design Name	M2 Metal Used	Leakage Current(nA)	Leakage Power(nW)	Dynamic Power(nW)	Total Power (nW)
TGFF	0	0.276	0.1932	55.0	55.1932
	2	0.285	0.1995	53.2	53.3995
CSFF	1	5.14	3.598	84.7	88.298
	2	4.48	3.136	80.1	83.236
	3	4.66	3.262	78.8	82.062
C2SFF	3	0.941	0.6587	83.0	83.941
CSFF No ClkBuff	3	4.56	3.192	20.21	23.402
C2SFF No ClkBuff	3	0.311	0.2177	27.53	27.847

The table 3.2 presents the post-layout results related to power at an operating voltage of 0.7V, a switching factor of 10%, and an operating frequency of 100MHz. In contrast, the table 3.3 displays the power results for the same voltage of 0.7V but with a switching factor of 40% and an operating frequency of 400MHz.

Table 3.3: Summary of Post Layout Simulation - Power Results(At 40% Switching Factor | 400Mhz)

Design Name	M2 Metal Used	Leakage Current(nA)	Leakage Power(nW)	Dynamic Power(nW)	Total Power (nW)
TGFF	0	0.276	0.1932	880.0	880.1932
	2	0.285	0.1995	850.0	850.1995
CSFF	1	5.14	3.598	1354.0	1357.598
	2	4.48	3.136	1282.0	1285.136
	3	4.66	3.262	1263.0	1266.262
C2SFF	3	0.941	0.6587	1328.0	1328.941
CSFF No ClkBuff	3	4.56	3.192	322.3	325.492
C2SFF No ClkBuff	3	0.311	0.2177	441.0	441.311

From both tables, we can observe that C2SFF (both with and without the clock buffer) exhibits comparable leakage power when compared to TGFF design implementations. However, CSFF implementations demonstrate significantly higher leakage power than both C2SFF and TGFF designs. This trend is further confirmed by [2], which reveals a similar pattern. From both tables, we can observe that the power consumed by the clock is greater than the power

consumed by the data. This difference occurs because, when calculating data power, only the data pin toggles. In contrast, during the clock power calculation, the clock toggles in such a way that the output node 'Q' also toggles, causing many internal nodes to toggle and resulting in more power consumption.

The authors in papers [1] and [2] demonstrated that the dynamic power consumed by CSFF and C2SFF is less than that of TGFF. This reduction is attributed to the removal of redundant transitions and the clock buffer. When we compare the dynamic power values from both tables for TGFF implementations with clock buffer implementations of CSFF and C2SFF, we find that the presence of clock buffers significantly increases dynamic power. In this scenario, TGFF displays lower dynamic power.

However, when we compare TGFF implementations with CSFF and C2SFF implementations that do not include a clock buffer, we observe a significant decrease in dynamic power, resulting in TGFF consuming more dynamic power than both CSFF and C2SFF without a clock buffer.

CHAPTER 4

Sustainability Metric and Analysis on Circuits

4.1 Proposed Sustainability Framework

Traditionally, VLSI circuits are assessed based on three key metrics: Power, Performance, and Area (PPA). As the negative impact on the environment becomes increasingly evident, there is a growing demand to incorporate sustainability considerations into VLSI circuit design and evaluation. While some existing models do benchmark sustainability, they often lack a design-centric approach. This gap complicates the ability of designers to make informed choices when selecting the most sustainable design options in the early stages of VLSI circuit design.

A novel framework is proposed for conducting sustainability analysis at the design level. This analysis is divided into two main areas: the Embodied Carbon Footprint and the Operational Carbon Footprint. The proposed framework can be applied to different types of standard cells. This work will primarily focus on flip-flops, specifically those used in IoT applications. The analysis is done in metric related to energy units, which can be converted to CO_2 equivalent for estimating the GHG emissions. There is a positive relation between energy and GHG emission, where more energy consumption is related to more GHG emission and less sustainable design. So, in this work a design consuming low energy is considered to be more sustainable design. The framework is explained below.

4.1.0.1 Embodied Carbon Footprint (ECP)

The emissions generated before a device begins operating for the user are referred to as Embodied Cabon Footprint (ECP). This encompasses various stages, including material collection, assembly, manufacturing, fabrication, testing, and shipping to its final destination. From a designer's perspective, we will specifically focus on the fabrication aspect. The Eq. 4.1 represents the proposed formula for calculating the Embodied Carbon Footprint.

$$ECP = WFE \times Design\ Area \times MCI \times EPI \tag{4.1}$$

1. Wafer Fabrication Energy (WFE) : It refers to the amount of energy consumed per μm^2 during the fabrication of a standard wafer. It is calculated by dividing the total energy used for the fabrication process by the total area of the wafer. Since the area is measured

in μm^2, Wafer Fabrication Energy is expressed in terms of energy per μm^2. In this work, we have taken a 300 mm diameter wafer with six metal tracks fabricated using a 65 nm technology node. The energy consumption data, sourced from [11], amounts to 4204 kWh per wafer. Hence, with this information WFE is calculated to be $59.5 nWh/\mu m^2$ per wafer.

2. Design Area : It is the total area consumed by the layout of standard cell design.

3. Metal Congestion Impact (MCI) : It measures the congestion that arises from using higher-level metal layers in routing, such as the M2 layer. While these layers can create a denser layout, they may also limit routing resources at the System-On-Chip (SoC) level. This can lead to routing congestion and increase the area required for routing at SoC level, negatively impacting the ECP of the whole SoC. MCI is quantified using the formula presented in Eq. 4.2.

$$MCI = 1 + \left[\frac{Total\ Tracks\ Available\ In\ Metal\ 2\ Layer}{Tracks\ Available\ For\ Routing\ In\ Metal\ 2\ Layer} - 1 \right] \times CF \quad (4.2)$$

CF represents the Congestion Factor and is estimated to be 0.3 based on RISC V processor example. This factor reflects the effect of elevated routing congestion on the Embodied Carbon Footprint of the design. Total tracks available in M2 layer are 13 as track size for M1 and M2 metal layers are same. For finding the available tracks for routing in M2 layer at SoC level, we just subtract 13 with M2 layers used during layout implementation. For example, for TGFF(M1+2M2) we have used two M2 layers for routing so available tracks for routing at SoC level will become (13-2 = 11 M2 tracks).

4. Extra Process Impact (EPI) : Depending on the technology node and foundry used for fabrication, using special devices like devices with different threshold voltages or different capacitor types etc can cause the fabrication steps to have extra processes thereby increasing the energy required to fabricate the wafer. This effect is captured by EPI estimated using the Eq. 4.3.

$$EPI = ((Total\ Masks - Reference\ Masks) \times MF) + 1 \quad (4.3)$$

MF refers to Mask Factor. We assume that each extra step necessitates an additional 4.5% of energy, and according to the information provided in [11], MF estimated as 0.045. Total Masks is given by adding Reference Masks with Extra Masks. We have not used any special device (Extra Masks are 0); hence, for the 65nm technology used for this work, Total Masks and Reference Masks are the same and equal to 36. Hence, using Eq. 4.3, EPI gets reduced to 1.

4.1.0.2 Operational Carbon Footprint (OCP)

The carbon footprint caused during the operation of the device is called the operating carbon footprint. Energy-efficient circuits have a lower OCP. As shown in Eq. 4.4, The OCP is made up of mainly two components - Dynamic Power, Leakage Power. Then sum of these two powers is then multiplied with the total lifetime duration of device operation (T_{total}) for the device. For

IoT we have considered the total lifetime duration of 20,000 hours (24 hours of operation for 2.5 - 3 years).

$$\text{OCP} = T_{\text{total}} \times (\text{Dynamic power} + \text{Leakage power}) \tag{4.4}$$

For operational carbon footprint analysis we have divided the whole operational lifetime duration in three components; Active Mode, StandBy Mode and SwitchedOff Mode.

1. Active Mode : In this mode the device work with its full capacity. During this mode we get the both dynamic power and leakage power consumption.
2. StandBy Mode : In this mode the device is not actively working and instead is in sleep mode and just maintaining its current state of the device. During this mode, we only get leakage power consumption.
3. SwitchedOff Mode : In this mode the device is not consuming any power. The device is considered to be switched off.

In our analysis, as we considered an IoT device application that operates over a total of 20,000 hours. We have assumed the device spends 5% of this time in Active Mode, 25% in Standby Mode, and the remaining 70% in Switched Off Mode. Consequently, the Active Time Percentage (ATP) is 5% = $\frac{5}{100}$ = 0.05, the Standby Time Percentage (STP) is 25% = $\frac{25}{100}$ = 0.25, and the Switch Off Time Percentage (SOTP) is 70% = $\frac{70}{100}$ = 0.7 . As no power consumption occur during Switched Off Mode, hence SOTP will not be used in any equation.

Dynamic Power : It is the power consumed due to logic node switching during the Active Mode of the operation. It is calculated using the Eq. 4.5.

$$\begin{aligned} \text{Dynamic power} &= Q_{\text{dyn}} \times \alpha \times V_{\text{active}} \times f \times ATP \\ &= Q_{\text{dyn}} \times \alpha \times V_{\text{active}} \times f \times 0.05 \end{aligned} \tag{4.5}$$

where, Q_{dyn} is the total dynamic charge consumed by the flip-flop. This can be estimated using the Total Power from Table 3.2 and Table 3.3. α is the switching factor, f is the frequency of operation and V_{active} is the voltage of operation during the active mode. Active Time Percentage (ATP) is used to scale down the dynamic power value such that it represents the dynamic power which occurred only when device is in active mode.

Leakage Power: This term refers to the power consumption due to leakage that occurs in both Active and StandBy Modes. The consumption is adjusted based on the Active Time and Standby Time Percentages. In our calculations of leakage power, we have introduced two new concepts: Performance Ratio (PR) and Pulse Width Modulation (PWM).

The Performance Ratio (PR) is defined as the ratio of the propagation delay of the particular design to the worst propagation delay among all the designs being evaluated. For instance, in our analysis, the CSFF (M1 + 2M2) has the worst propagation delay of 1601.2 ps. If we want to calculate the PR for TGFF (M1 only), which has a propagation delay of 1388.4 ps, the PR while calculating leakage power for TGFF (M1 only) is calculated as $\frac{1388.4}{1601.2} = 0.867$.

This value indicates that a faster design (TGFF (M1 Only)) will spend less time in active mode and more time in standby mode compared to the design with the worst propagation delay (CSFF(M1+2M2)). This adjustment will apply only when PWM is activated (i.e., PWM = 1) in the design. If PWM is not activated, the entire leakage in active mode will be considered without any adjustment for faster operation.

The equation used to calculate Leakage Power is represented in Equation 4.6. In this equation, the first term accounts for leakage power consumption in Active Mode, while the second term corresponds to Standby Mode.

$$\begin{aligned} \text{Leakage power} &= \left[I_{\text{active}} \times V_{\text{active}} \times \left(ATP \times PR^{PWM}\right)\right] \\ &\quad + \left[I_{\text{standby}} \times V_{\text{standby}} \times (STP + (PWM \times ATP \times (1 - PR)))\right] \\ &= \left[I_{\text{active}} \times V_{\text{active}} \times (0.05 \times PR)\right] \\ &\quad + \left[I_{\text{standby}} \times V_{\text{standby}} \times (0.25 + (0.05 \times (1 - PR)))\right] \end{aligned} \tag{4.6}$$

where, I_{active} and $I_{standby}$ are the leakage current during active and standby mode respectively. V_{active} and $V_{standby}$ are the voltage of operation during active and standby mode respectively. PR is Performance Ratio, ATP is Active Time Percentage, STP is Standby Time Percentage and PWM is Pulse Width Modulation (We assumed PWM as 1). For simplicity, we have assumed the voltage of operation for Active and StandBy Modes to be same as 0.7V.

4.1.0.3 Total Carbon Footprint

The embodied and operational carbon footprints alone do not provide a complete sustainability analysis. Therefore, we integrate both the embodied carbon footprint and the operational carbon footprint to calculate the total carbon footprint. Alongside Power, Performance, and Area (PPA) in their designs, total carbon footprint is a crucial metric for designers to tackle the environmental impact of their design. It can be calculated with the Eq. 4.7.

$$\text{Total Carbon Footprint} = (\text{Embodied Carbon Footprint} + \text{Operational Carbon Footprint}) \tag{4.7}$$

4.2 Design Analysis for Embodied Carbon Footprint

The Table 4.2 presents the summary of the embodied carbon footprint results.

Table 4.1: Summary of Embodied Carbon Footprint Results

Design Name	M2 Used	Track Height	Track Width	Total Area (μm^2)	Embodied Footprint (mWh)
TGFF	0	13	22	11.44	0.681
	2	13	19	9.88	0.620
CSFF	1	13	32	16.64	1.01
	2	13	32	16.64	1.04
	3	13	29	15.08	0.978
C2SFF	3	13	29	15.08	0.978
CSFF No Clock Buffer	3	13	26	13.52	0.877
C2SFF No Clock Buffer	3	13	26	13.52	0.877

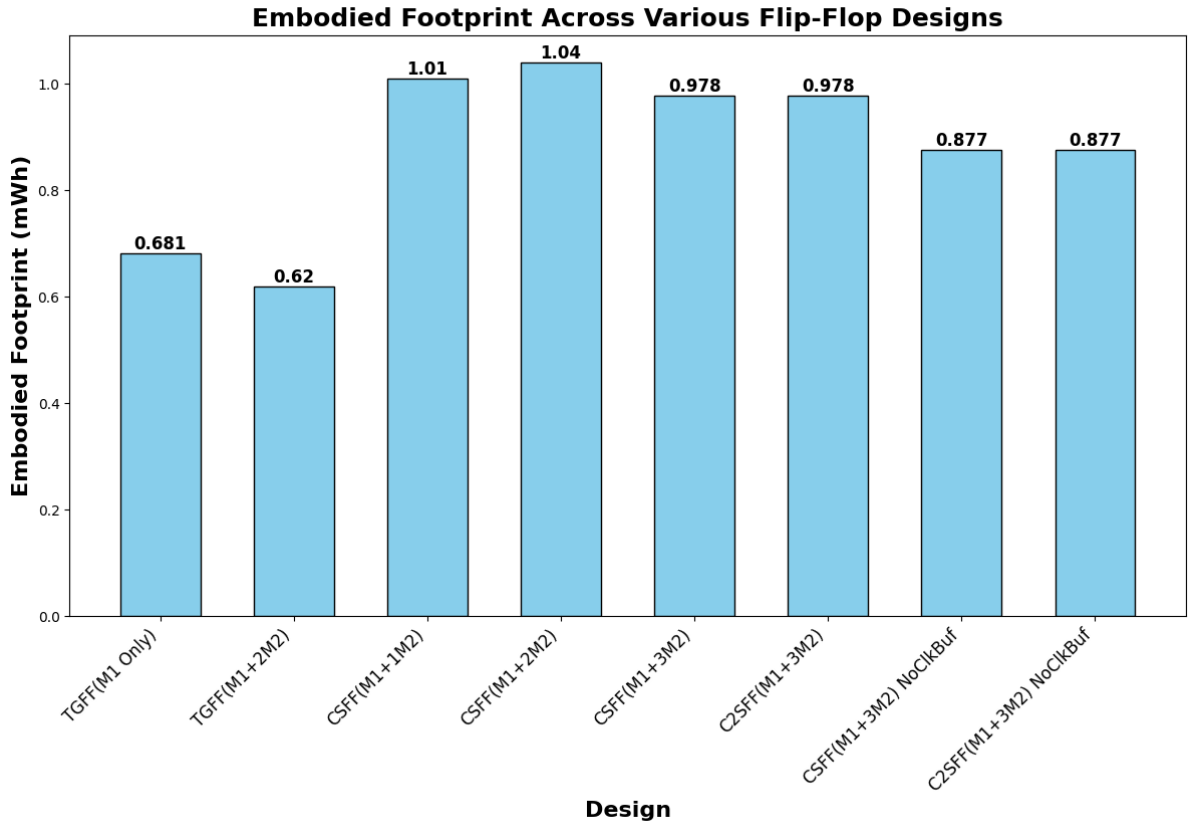

Figure 4.1: Plot showing the embodied carbon footprint comparison of all design implementations.

The plot in Fig. 4.1 indicates that the embodied footprint of TGFF(M1+2M2) is the lowest, while that of CSFF(M1+2M2) with clock buffer is the highest. When considering only the embodied footprint, the CSFF(M1+3M2) design without a clock buffer is the most sustainable option among all CSFF design implementations. Similarly, the design C2SFF(M1+3M2) without a clock buffer is the most sustainable among all the implemented designs of C2SFF. However, several interesting observations will be discussed in the following section.

4.2.0.1 Effect of Area – TGFF Implementations

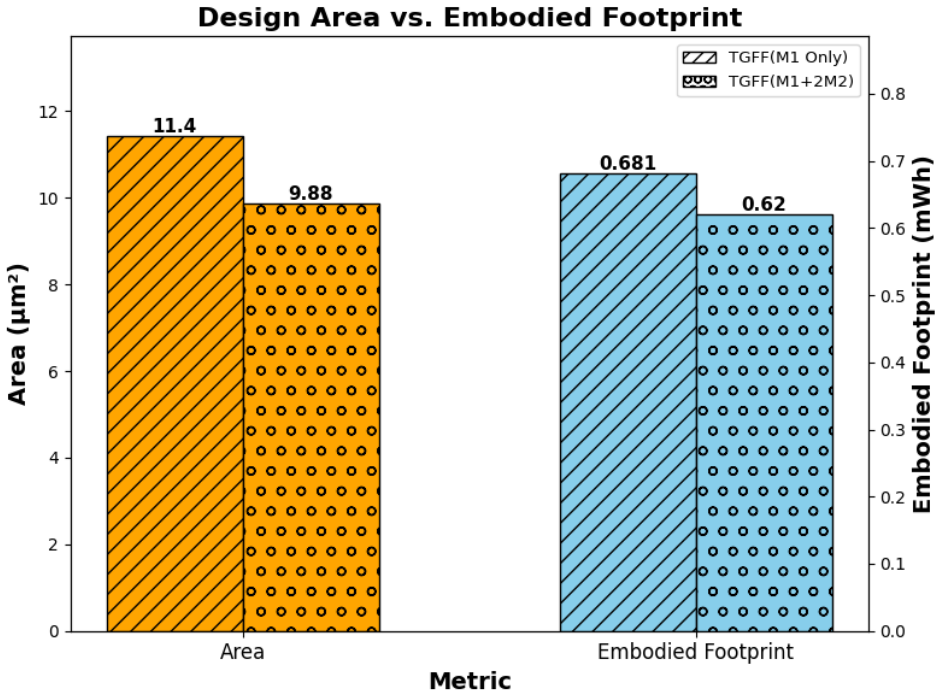

Figure 4.2: Plot showing the area and embodied carbon footprint comparison of both TGFF implementations.

The analysis of Fig. 4.2 shows that by employing two additional M2 metal layers, there is an increase in system-level congestion; however for the formula and factors used in this study, area emerges as the predominant factor. This is evident in the reduction of the area from 11.4 μm^2 to 9.88 μm^2, which consequently decreases the embodied footprint from 0.681 mWh to 0.62 mWh. Therefore, when focusing solely on the embodied footprint, the TGFF implementation utilizing two M2 layers represents a more sustainable design choice.

4.2.0.2 Effect of Area – C2SFF(With and Without Buffer) Implementations

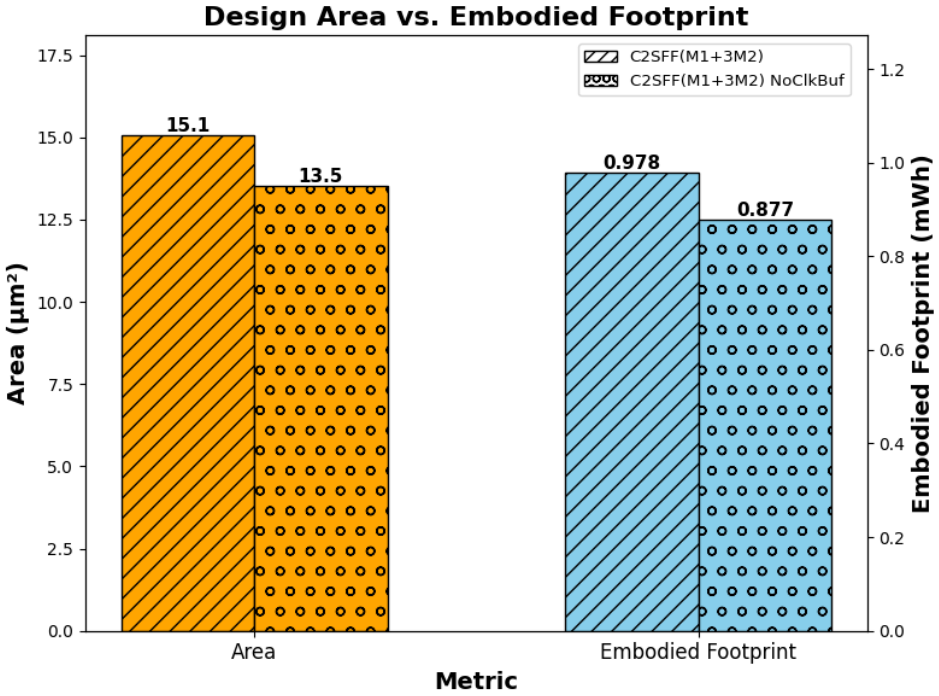

Figure 4.3: Plot showing the area and embodied carbon footprint comparison of C2SFF(M1+3M2) with and without Clock Buffer implementations.

The previously discussed C2SFF(M1+3M2) design incorporates a clock buffer, which serves to reduce the capacitive load on the clock tree network. However, it is possible to achieve the same flip-flop functionality without this clock buffer, albeit at the expense of an increased capacitive load on the clock tree. Upon removing the clock buffer from the layout and conducting simulations, we observed a reduction in area from 15.08 μm^2 to 13.52 μm^2. This area reduction corresponds directly to a decrease in the embodied footprint from 0.978 mWh to 0.877 mWh. In quantitative terms, eliminating the clock buffer results in an 10.34% reduction in area and a 10.32% decrease in embodied carbon footprint. Therefore, as shown in Fig. 4.3, we can conclude that if we can effectively manage the stability of flip-flop and the increased load on the clock tree network due to the shared clock buffer, the C2SFF(M1+3M2) design without the clock buffer presents a more sustainable design option regarding embodied carbon footprint. The analysis is consistent for the CSFF(M1+3M2) design, as it exhibits the same layout area and number of metal layers utilized for both configurations—with and without the clock buffer—when compared to the C2SFF(M1+3M2) design.

4.2.0.3 Effect of Congestion – CSFF Implementations

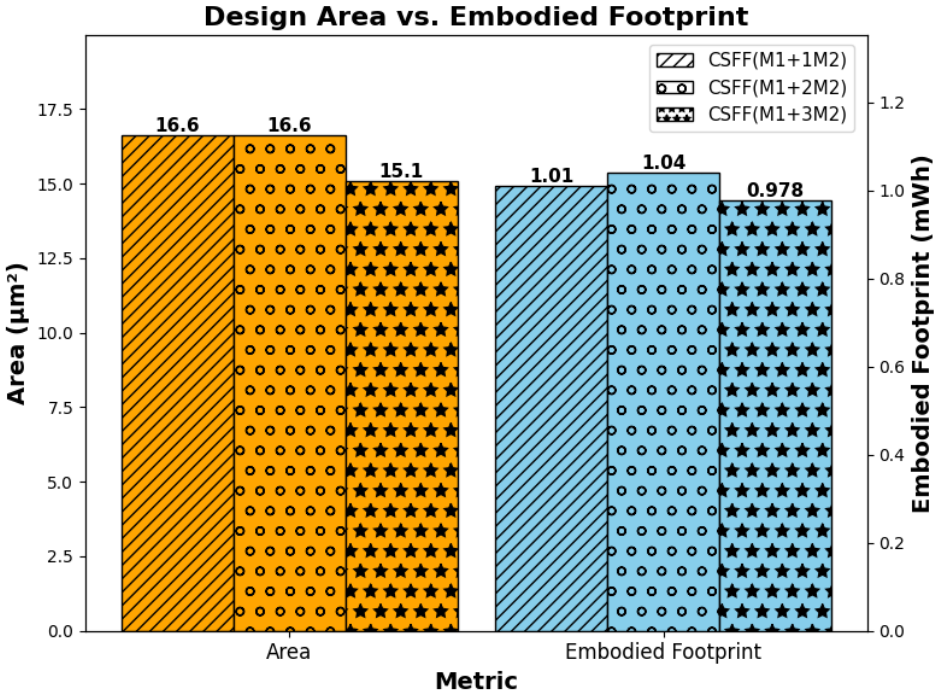

Figure 4.4: Plot showing the area and embodied carbon footprint comparison of all the 3 CSFF implementations.

The incorporation of an additional upper metal layer (M2 Layer) does not always lead to a reduced area in standard cell designs. However, it can contribute to increased system-level congestion. This is illustrated in Fig. 4.4. The designs CSFF(M1+1M2) and CSFF(M1+2M2) utilize one and two M2 layers, respectively. Notably, the addition of a second M2 layer in the CSFF(M1+2M2) implementation does not result in a decrease in area, as both designs maintain the same area of 16.64 um². The implications for system-level congestion are evident in Fig. 4.4, where the embodied footprint of CSFF(M1+2M2) is 2.97% larger than that of CSFF(M1+1M2). Conversely, when an additional third M2 layer is employed in the CSFF(M1+3M2), we find that the 5.96% reduction in area outweighs the increase in the congestion due to additional third M2 layer, making CSFF(M1+3M2) a more sustainable design (with respect to embodied carbon footprint) choice than the prior two designs.

4.3 Design Analysis for Operational Carbon Footprint

The operational footprint analysis is summarized in Table 4.2. In this table, the dynamic and leakage powers are calculated using Eq. 4.5 and Eq. 4.6 where the scaling due to ATP and STP are already included inside them. Total power is just sum of leakage and dynamic powers. Like before we have plotted the operational carbon footprint for two scenarios: a 10% switching

Table 4.2: Summary of Operational Carbon Footprint Results

Design Name	M2 Metal Used	Leakage Power (nW)	Dynamic Power at 10 | 100 (nW)	Total Power at 10 | 100 (nW)	Operational Footprint at 10 | 100 (mWh)	Dynamic Power at 40 | 400 (nW)	Total Power at 40 | 400 (nW)	Operational Footprint at 40 | 400 (mWh)
TGFF	0	0.0579	2.75	2.808	0.0562	44.016	44.074	0.881
	2	0.0598	2.66	2.719	0.0544	42.56	42.6198	0.852
CSFF	1	1.0794	4.235	5.3144	0.106	67.76	68.839	1.38
	2	0.9408	3.99	4.9308	0.0986	63.84	64.781	1.3
	3	0.9786	3.95	4.928	0.0987	63.28	64.2586	1.29
C2SFF	3	0.19761	4.165	4.363	0.0873	66.64	66.837	1.34
CSFF No ClkBuff	3	0.9576	1.01	1.967	0.0393	16.128	17.0856	0.342
C2SFF No ClkBuff	3	0.06531	1.37	1.435	0.0288	22.01	22.075	0.441

- 10 | 100 : 10% switching factor and 100MHz frequency
- 40 | 400 : 40% switching factor and 400MHz frequency

factor at 100 MHz and a 40% switching factor at 400 MHz, as shown in Figures 4.5 and 4.6, respectively.

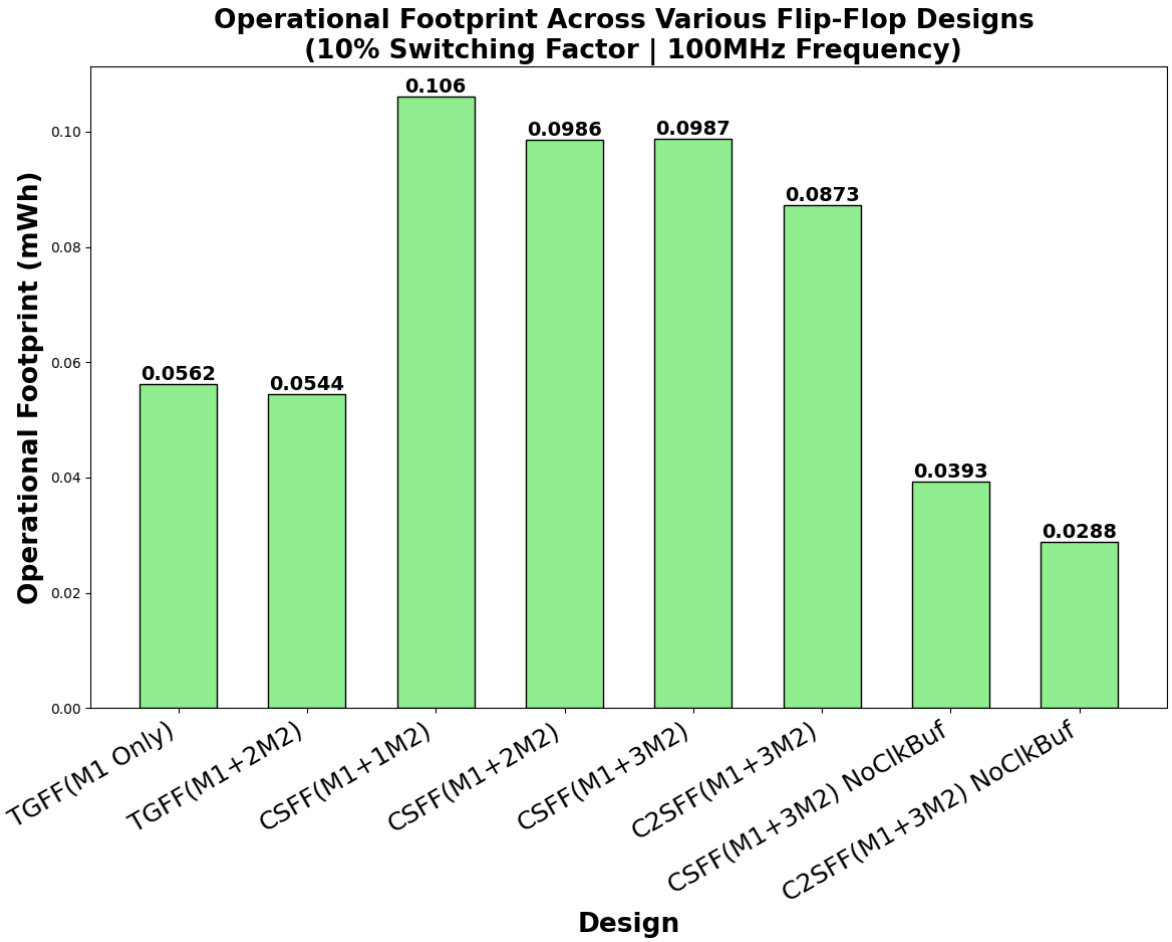

Figure 4.5: Plot showing operational carbon footprint comparison of all the design implementations at 10% switching factor and 100MHz frequency.

The first notable observation can be seen in Fig. 4.5, where the operational carbon footprint for CSFF(M1+3M2) is greater than that of C2SFF(M1+3M2). However, this trend changes

in Fig. 4.6, where the operational carbon footprint for C2SFF(M1+3M2) exceeds that of CSFF(M1+3M2). We will explore this observation in more detail in the next section.

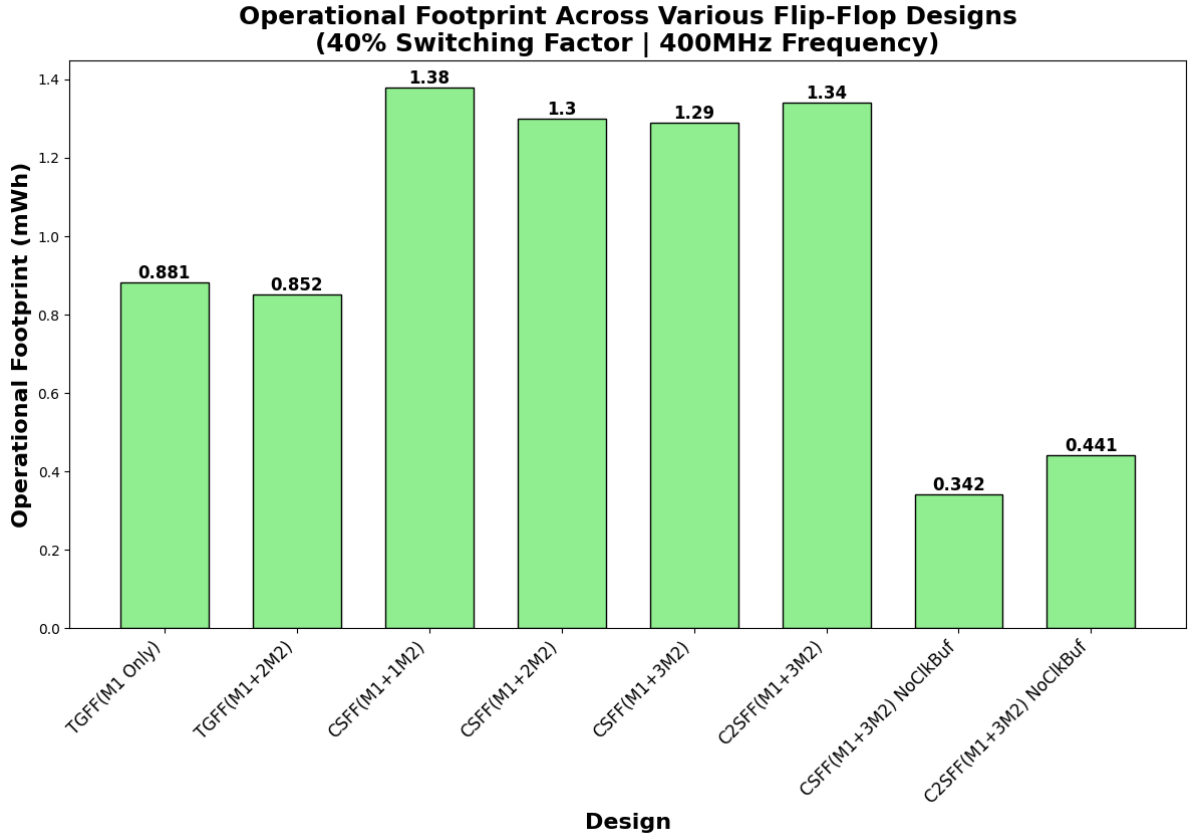

Figure 4.6: Plot showing operational carbon footprint comparison of all the design implementations at 40% switching factor and 400MHz frequency.

4.3.0.1 Effect of Dynamic and Leakage Power – CSFF and C2SFF with Clock Buffer

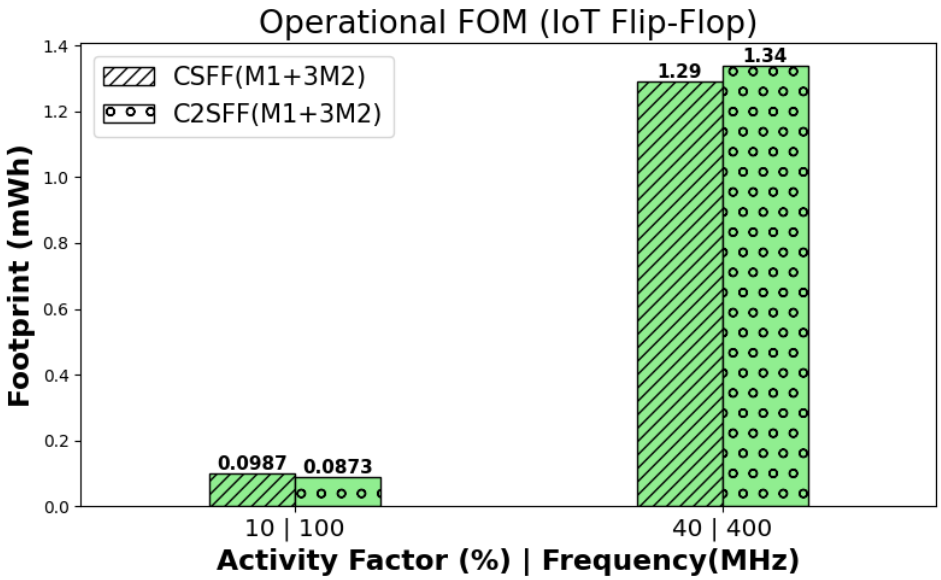

Figure 4.7: Plot showing the operational carbon footprint comparison of CSFF(M1+3M2) and C2SFF(M1+3M2) with Clock Buffer implementations at different switching factor and frequency.

As we have discussed previously, there are two primary types of power consumed by any design: dynamic power and leakage power. We observed that for the proposed formula and assumed values, at low switching factors and frequencies, leakage power may dominate, while at higher switching factors and frequencies, dynamic power becomes the prevailing factor. This distinction is illustrated in Figure 4.7.

During simulations, as shown in Table 4.2, it was found that CSFF(M1+3M2) has higher leakage power than C2SFF(M1+3M2). However, the dynamic power of CSFF(M1+3M2) is lower than that of C2SFF(M1+3M2). Leakage power does not change with switching factor and frequency, while dynamic power scales with these parameters.

Using ATP and STP, we scaled both types of power according to assumed IoT operational conditions (5% Active, 25% Standby, and 70% Switched Off). We observed that when the switching factor and frequency are low, dynamic power becomes comparable to leakage power. As a result, leakage power contribute considerably to the total power consumption. Thus, a design with higher leakage power and lesser dynamic power may end up consuming more total power. When considering only the operational carbon footprint—given that leakage power is the dominant factor in this scenario—C2SFF(M1+3M2) proves to be a more sustainable option than CSFF(M1+3M2).

Conversely, under high switching factor and frequency conditions, dynamic power scales up and becomes the dominant factor, ultimately influencing the sustainability of the design while

leakage power have a insignificant impact. Therefore, a design with lower dynamic power, such as CSFF(M1+3M2), emerges as the more sustainable choice.

4.3.0.2 Effect of Dynamic and Leakage Power – CSFF and C2SFF without Clock Buffer

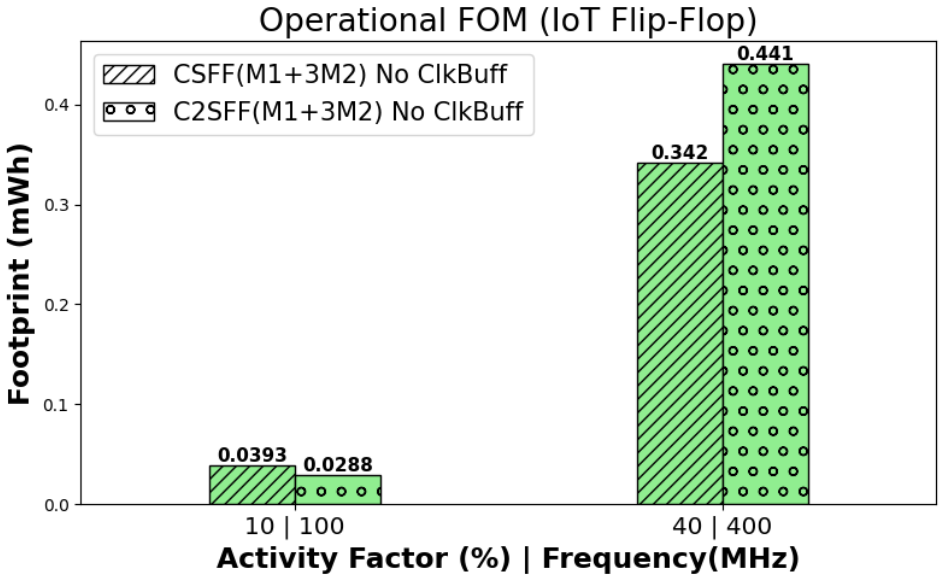

Figure 4.8: Plot showing the operational carbon footprint comparison of CSFF(M1+3M2) and C2SFF(M1+3M2) without Clock Buffer implementations at different switching factor and frequency.

The leakage and dynamic power analysis conducted in previous section holds true even in the absence of clock buffers. The configuration C2SFF(M1+3M2) without a clock buffer exhibits lower leakage power but higher dynamic power compared to CSFF(M1+3M2) without a clock buffer. This mirrors the conditions illustrated in 4.7, resulting in a similar trend depicted in 4.8. Considering only operational carbon footprint, C2SFF(M1+3M2) without a clock buffer is the more sustainable option for scenarios with a low switching factor and frequency, while CSFF(M1+3M2) without a clock buffer due to its lower dynamic power becomes the more sustainable choice when higher switching factors and frequencies are involved.

4.3.0.3 Effect of Dynamic and Leakage Power – TGFF and CSFF without Clock Buffer

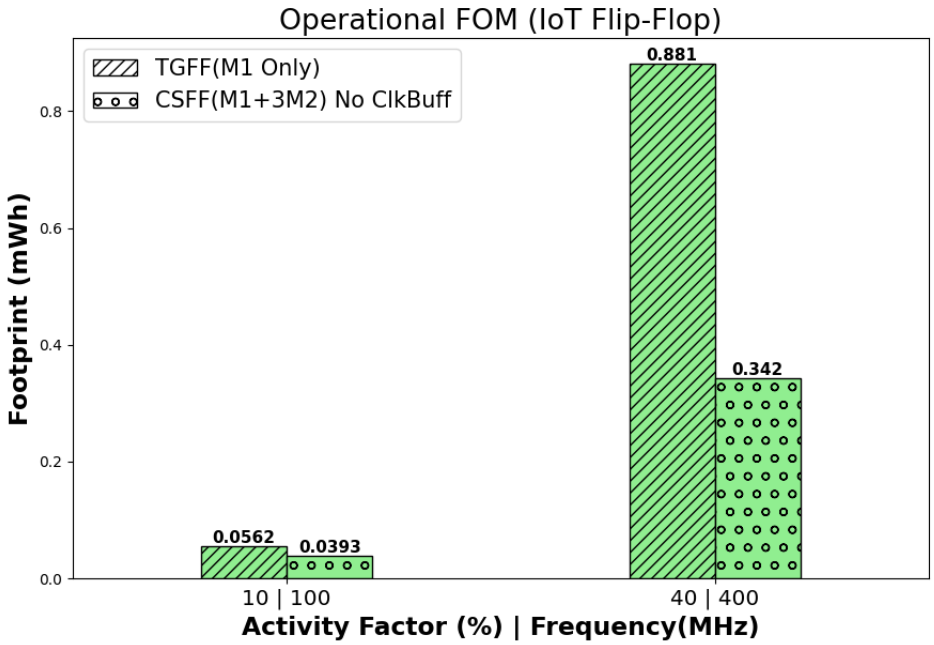

Figure 4.9: Plot showing the operational carbon footprint comparison of TGFF(M1 Only) and CSFF(M1+3M2) without Clock Buffer implementations at different switching factor and frequency.

In Figures 4.7 and 4.8, we observed that when we have low switching factors and frequencies, configurations with larger leakage power and smaller dynamic power can result in a higher operational carbon footprint compared to designs with lower leakage power and higher dynamic power. However, this trend is not universal; we cannot simply determine the sustainability of a design by examining the leakage and dynamic power values shown in Table 3.2 and 3.3.

For instance, the TGFF (M1 Only) design has lower leakage power than the CSFF (M1+3M2) design without a clock buffer. Furthermore, the TGFF(M1 Only) design exhibits higher dynamic power than the CSFF(M1+3M2) No ClkBuff design. This pattern was also evident in the design examined in Figure 4.7.

The key distinction presented in Figure 4.9 is that despite having lower leakage power, the TGFF (M1 Only) design still has greater operational carbon footprint than the CSFF (M1+3M2) design without a clock buffer for low switching factor and frequency conditon. In this case, the CSFF (M1+3M2) No ClkBuff design has such minimal dynamic power that, despite its higher leakage power, its total power consumption does not exceed that of the TGFF (M1 Only) design, making it a more sustainable choice.

This example highlights the importance of proposed framework and illustrates that simply analyzing leakage and dynamic power may not yield an accurate assessment of sustainability.

4.4 Design Analysis for Total Carbon Footprint

Evaluating only the embodied or operational carbon footprint can provide an incomplete picture of which design is more sustainable overall. Therefore, it is essential to combine both embodied and operational footprints before conducting a sustainability analysis. Along with Power, Performance and Area, Total carbon footprint is a figure of merit that should be used to access the sustainability of the design. We have plotted the total carbon footprint for all our designs at a 10% switching factor and 100 MHz frequency, as well as at a 40% switching factor and 400 MHz frequency, as shown in Fig. 4.10 and Fig. 4.11, respectively.

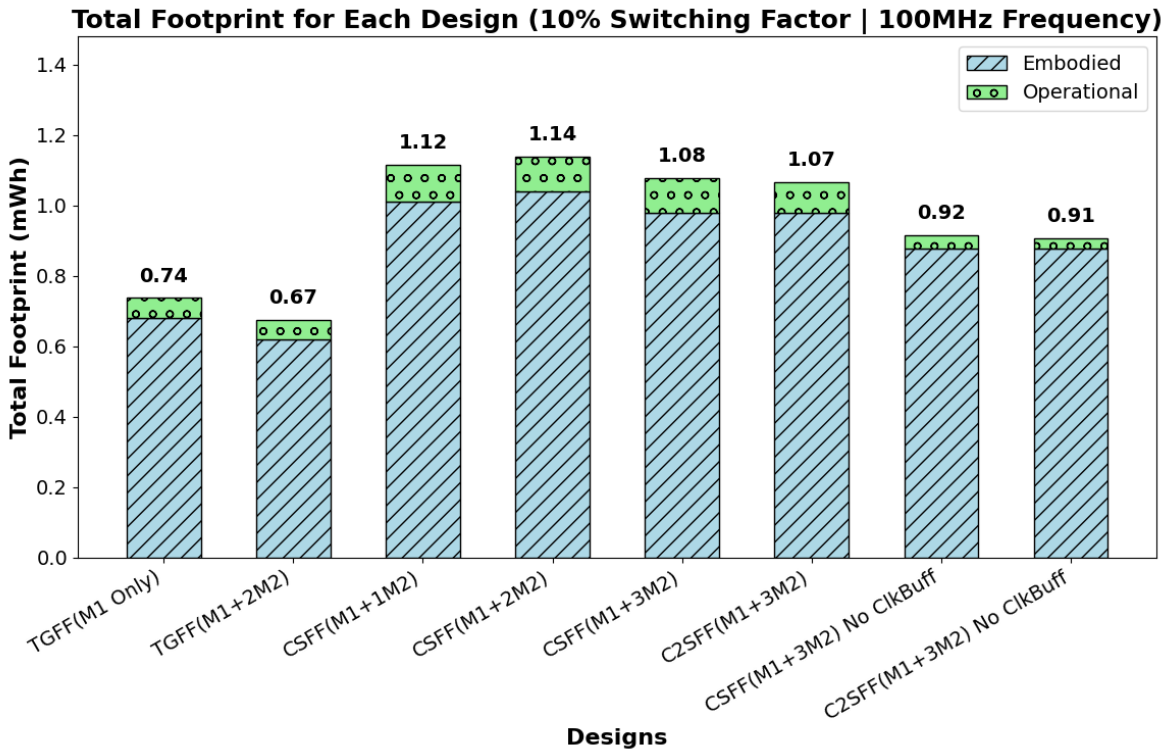

Figure 4.10: Plot showing the total carbon footprint comparison of all the design implementations at 10% switching factor and 100MHz frequency.

In Fig. 4.10 and Fig. 4.11, it can be observed that the overall sustainability of many designs depends on the switching factor and frequency at which they operate. For instance, in Fig 4.10 both the CSFF(M1+3M2) and C2SFF(M1+3M2) design options appear to be nearly equally beneficial in terms of sustainability. However, as shown in Fig 4.11 at higher switching factors and frequencies, CSFF(M1+3M2) clearly demonstrates greater sustainability.

A more detailed examination of the total carbon footprint results is presented in the following sections. These examples highlight the significance of total carbon footprint in the overall sustainability analysis, helping designers make informed decisions regarding the most sustainable design choices.

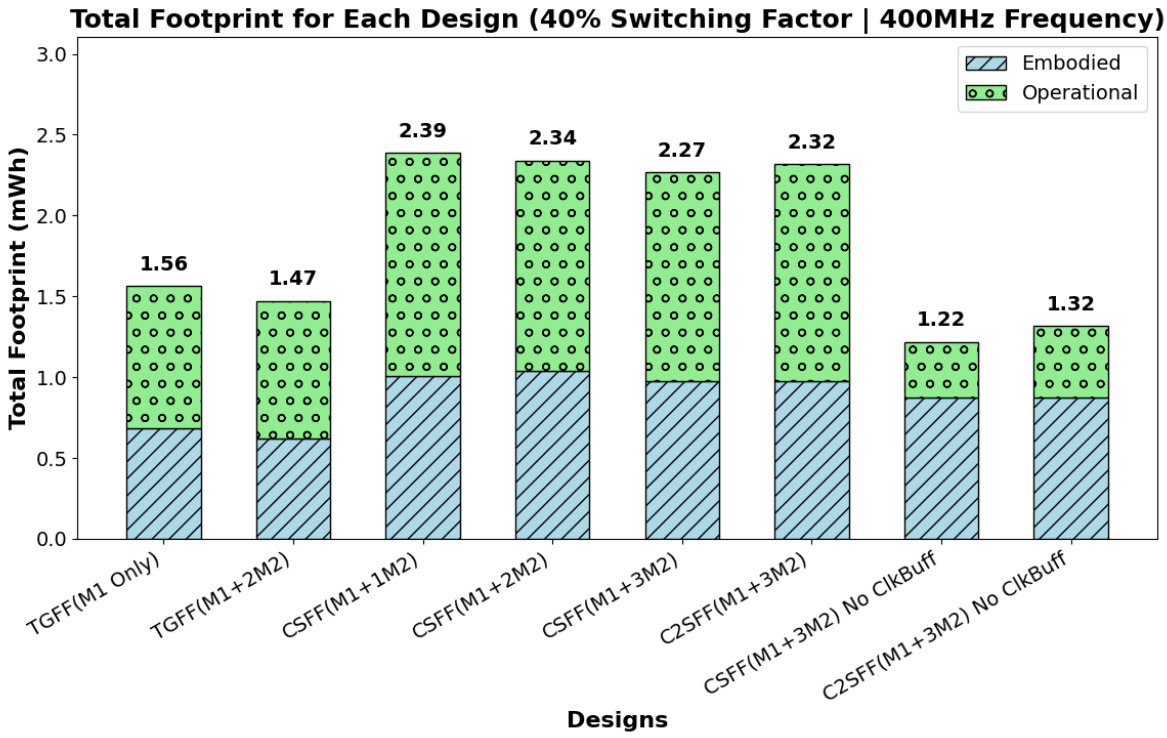

Figure 4.11: Plot showing the total carbon footprint comparison of all the design implementations at 40% switching factor and 400MHz frequency.

4.4.1 Examples Showing Importance of Total Carbon Footprint

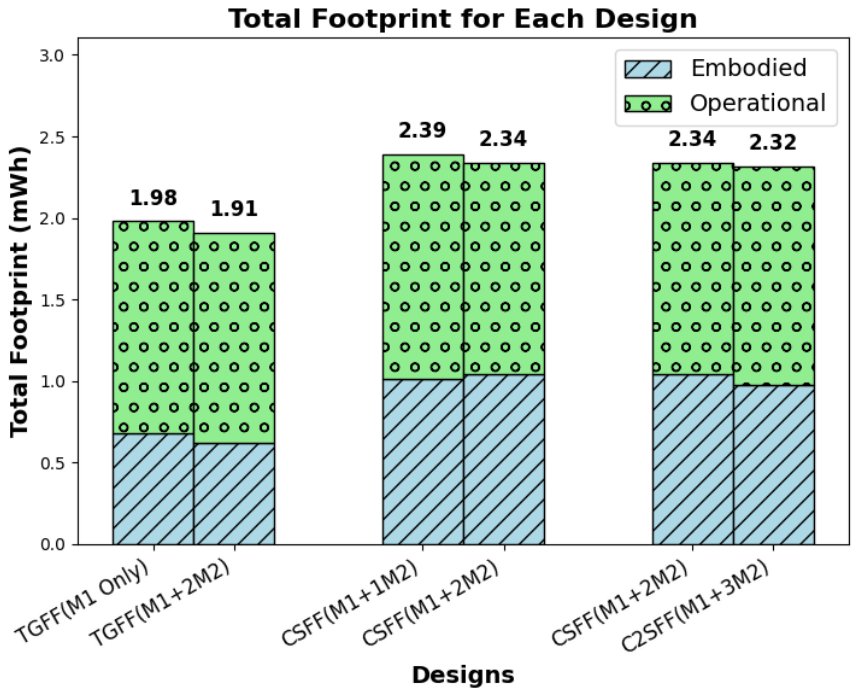

Figure 4.12: Plot showing the total carbon footprint comparison of various TGFF, CSFF and C2SFF design implementations at high switching factor and frequency.

Importance of total carbon footprint is illustrated through three examples presented in three clusters, as shown in Fig. 4.12. A switching factor of 40% and an operating frequency of 400 MHz are used to estimate the operational carbon footprint.

The first cluster outlines the total carbon footprint for TGFF(M1 Only) and TGFF(M1+2M2). The embodied and operational carbon footprints for TGFF(M1 Only) are 0.681mWh and 0.881mWh respectively, while those for TGFF(M1+2M2) are 0.620mWh and 0.852mWh respectively. For both embodied and operational metrics, TGFF(M1+2M2) demonstrates lower values, making it the more sustainable design choice overall. This shows the basic conclusion that when both embodied and operational carbon footprint are small, it is the ideal and straightforward sustainable design choice.

However, usually the sustainability analysis may not be this simple and may require careful examination to determine the best and most sustainable design. In the second cluster, which depicts CSFF(M1+1M2) and CSFF(M1+2M2), an analysis based solely on the embodied footprint might lead us to conclude that the former is more sustainable. However, in Fig. 4.12 when operational footprint is also take into account, we find that although the former has a smaller embodied carbon footprint, it incurs a significantly larger operational carbon footprint. As a result, the total carbon footprint of CSFF(M1+1M2) surpasses that of CSFF(M1+2M2). Therefore, when considering the total carbon footprint, CSFF(M1+2M2) emerges as the more sustainable design choice.

In the third cluster, we have the designs CSFF(M1+2M2) and C2SFF(M1+3M2). If we focus solely on the operational footprint, the former has a smaller operational carbon footprint than the latter. Thus, one might initially conclude that the former is the more sustainable design choice based on operational carbon footprint alone. However, when we take embodied carbon footprint into account, we find that the former has a higher embodied footprint, which significantly increases its total carbon footprint. Consequently, when considering the total carbon footprint, C2SFF(M1+3M2) emerges as the more sustainable design option.

4.4.2 Designs with Same Embodied Carbon Footprint – Total Carbon Footprint Analysis

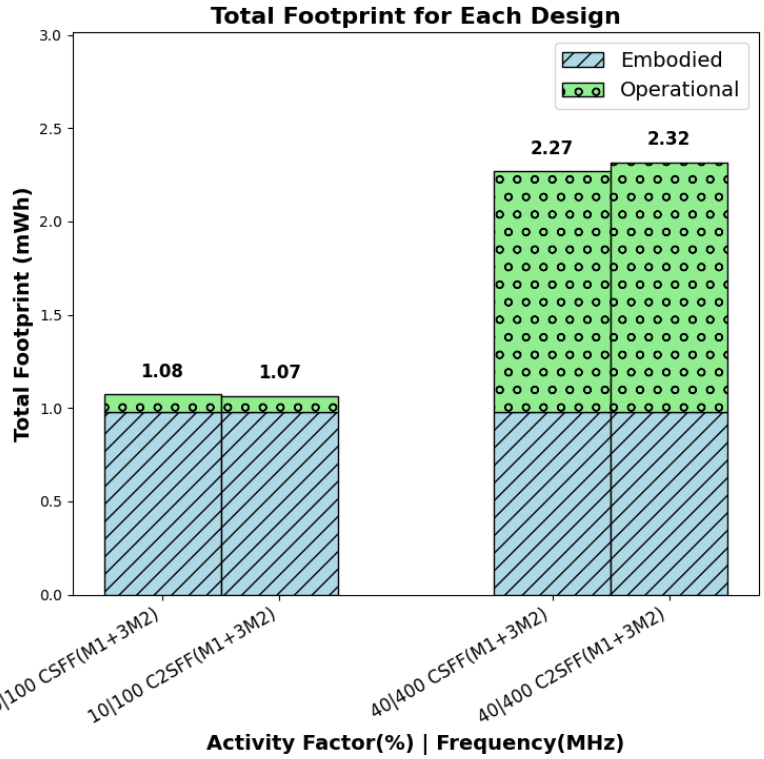

Figure 4.13: Plot showing the total carbon footprint comparison of CSFF and C2SFF with clock buffers at different switching factors and frequencies.

The designs CSFF(M1+3M2) and C2SFF(M1+3M2), both featuring clock buffers, occupy an identical design area of 15.08 μm^2. Additionally, they utilize three M2 metal layers, which results in identical effects on system-level congestion. Hence, as illustrated in Fig. 4.13, both designs exhibit the same embodied carbon footprint of 0.978 mWh. Alone from this perspective, one might conclude that both designs have an equivalent impact on sustainability.

However, a comprehensive assessment that includes operational carbon footprint reveals a more nuanced sustainability profile. As discussed in Section 4.3.0.1 and Fig. 4.7, it was noted that C2SFF(M1+3M2) demonstrates lower leakage power, whereas CSFF(M1+3M2) exhibits reduced dynamic power. But more detailed analysis of these designs revealed that in scenarios with low switching factors and frequencies, leakage power prevailed and C2SFF(M1+3M2) emerges as the more sustainable choice. Conversely, at high switching factors and frequencies, where dynamic power is the primary concern, CSFF(M1+3M2) becomes the more sustainable design alternative. As both designs have same embodied carbon footprint, operational carbon footprint analysis holds true in total carbon footprint and which design will be more sustainable will depend on the application of the device. For applications with low switching factor and

frequency C2SFF(M1+2M3) is overall a best sustainable design choice, otherwise applications with high switching factor and frequencies CSFF(M1+3M2) turns out to be overall better and sustainable choice.

This analysis underscores the importance of considering both embodied and operational carbon footprints for a holistic evaluation of sustainability while considering various design choices.

4.4.3 Designs Working at Low Switching Factor and Frequency – Total Carbon Footprint Analysis

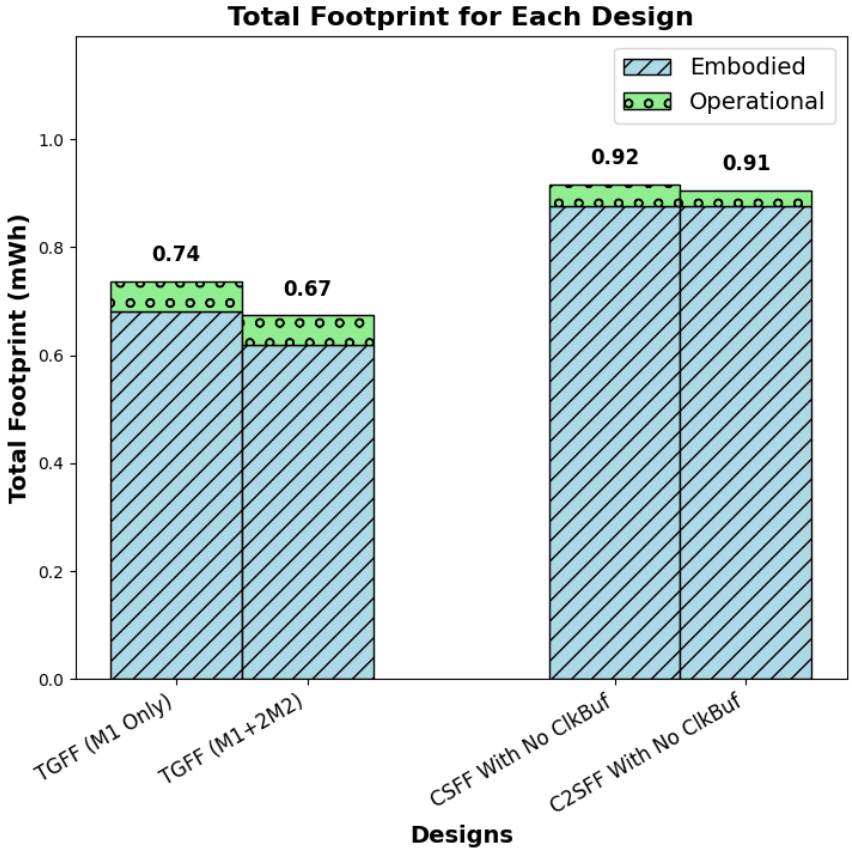

Figure 4.14: Plot showing the total carbon footprint comparison of TGFF implementations, CSFF and C2SFF without clock buffers at low switching factor and frequency.

Typically, papers discussing CSFF and C2SFF do not incorporate clock buffers. However, clock buffers are crucial for maintaining flip-flop stability and reducing the capacitive load on the clock tree, that is why flip-flop are often implemented with clock buffers in industry. For a holistic analysis, we have also examined the sustainability of CSFF(M1+3M2) and C2SFF(M1+3M2) both without clock buffers along with TGFF(M1 Only) and TGFF(M1+2M2) configurations. Figure 4.14 illustrates the embodied and operational carbon footprints, for a

10% switching factor and a frequency of 100 MHz. Our observations indicate that, when considering only the operational footprint, both TGFF implementations exhibit a higher footprint than CSFF(M1+3M2) and C2SFF(M1+3M2) without clock buffers. The observed phenomenon can be attributed to the fact that both implementations of TGFF exhibit higher total power when compared to the latter two implementations that do not incorporate clock buffers, the reason for such behavior is already explained in Section 4.3.0.3 and Fig. 4.9. Furthermore, we also observed that both TGFFs have significantly lower area and correspondingly lower embodied carbon footprint than CSFF (M1+3M2) and C2SFF (M1+3M2) without clock buffer implementations. However, when embodied footprint is also taken into account to assess the total carbon footprint, we find that at low switching factors and frequencies, both TGFF configurations represent a more sustainable design choice compared to the latter two options. This is because at low switching factors and frequencies, the embodied footprint is crucial for performing the overall carbon footprint analysis. Among these options, TGFF(M1+2M2) stands out as the most sustainable design choice due to its minimal embodied footprint compared to the other three designs.

4.4.4 Designs Working at High Switching Factor and Frequency – Total Carbon Footprint Analysis

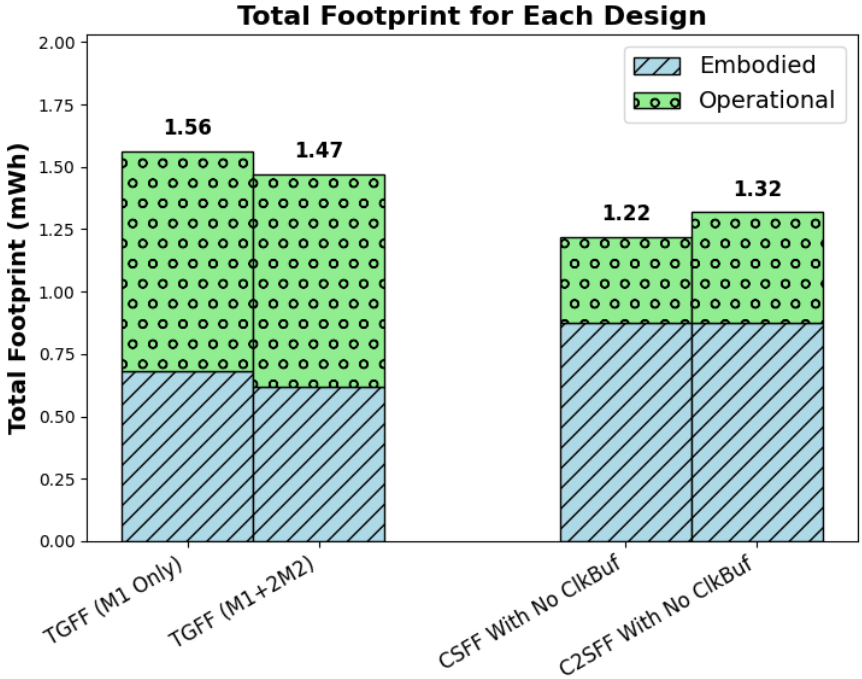

Figure 4.15: Plot showing the total carbon footprint comparison of TGFF implementations, CSFF and C2SFF without clock buffers at high switching factor and frequency.

In a similar manner to the analysis presented for Fig. 4.14, we conducted a study using a higher switching factor and frequency of 40% and 400 MHz, respectively. The results are illustrated in Fig. 4.15, where we observed significant changes in operational carbon footprint. Both TGFF configurations exhibited a higher operational carbon footprint compared to CSFF(M1+3M2) and C2SFF(M1+3M2) when clock buffers were absent. Although the latter two showed a higher embodied carbon footprint, the significant increase in dynamic power in both TGFF implementations led to a substantial rise in operational carbon footprint. Hence, when comparing the overall carbon footprint, it becomes evident that CSFF(M1+3M2) and C2SFF(M1+3M2) without clock buffers represent a more sustainable design choice when dealing with high switching factor and operating frequency. Among the two designs without clock buffers, as seen in Section 4.3.0.2 and Fig. 4.8, CSFF demonstrated lower dynamic power compared to C2SFF, ultimately making it the most sustainable option among all four designs.

4.4.5 CSFF and C2SFF With and Without Clock Buffer – Total Carbon Footprint Analysis

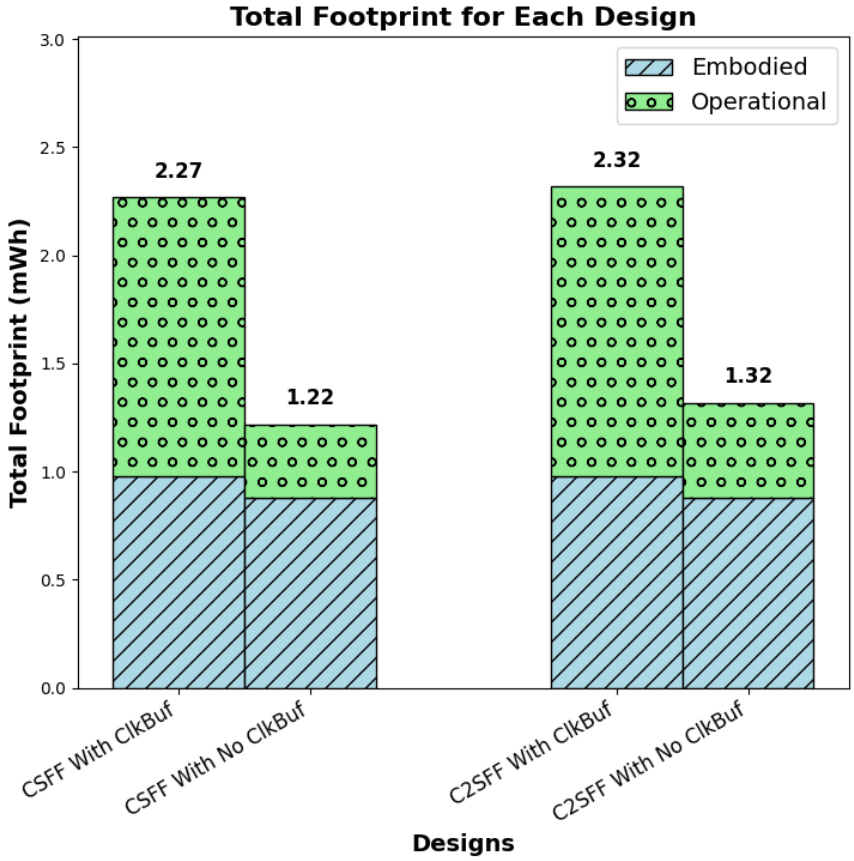

Figure 4.16: Plot showing the total carbon footprint comparison of CSFF and C2SFF with and without Clock Buffer implementations.

In our sustainability analysis of the CSFF (M1+3M2) and C2SFF(M1+3M2) designs, we examined both configurations with and without clock buffers. The results are illustrated in Fig. 4.16, indicating that the exclusion of the clock buffer not only leads to a reduction in design area but also significantly decreases the embodied carbon footprint associated with these designs.

A similar trend was observed concerning the operational carbon footprint; the removal of clock buffers contributed to reduced leakage and dynamic power consumption. This finding highlights a crucial conclusion for both design configurations that the absence of a clock buffer correlates with a reduction in total carbon footprint, thereby presenting a more sustainable design alternative.

Provided that the designer effectively manages design stability and addresses the implications of increased load on the clock tree network due to the shared clock buffers, opting for a CSFF or C2SFF designs without a clock buffer offers enhanced sustainability.

CHAPTER 5

Conclusion

In this work, we proposed a sustainability framework for the estimation of embodied and operational carbon footprint. Then we validated this framework by comparing the various implementations of Transmission Gate Flip-Flop(TGFF), Change Sensing Flip-Flop(CSFF) and Contention Free Change Sensing Flip-Flop(C2SFF) for overall sustainability of the design.

The results indicate that design choices for sustainability are dependent on the specific needs of the intended application, greatly impacting the design decisions required to achieve an optimal level of sustainability. For the proposed formula and assumed factor values, for the embodied carbon footprint, the design area is a vital factor, while for the operational carbon footprint, leakage and dynamic power are essential in assessing the sustainability of the design. Furthermore, we highlighted the significance of the total carbon footprint in sustainability analysis, which should be taken into account alongside PPA to effectively tackle the increasing challenge of climate change.

In reference to the thesis-

Our research paper, titled "**Sustainability Framework for Computing Element Design**" has been accepted at ICT4S 2025, which will be presented on 9-13 June 2025 in Ireland.

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List of papers based on Thesis

1. A. Grover et al., “Sustainability Framework for Computing Element Design,” 2025 International Conference on ICT for Sustainability (ICT4S), Dublin, Ireland, June 2025.