Design of a fully on-chip Linear Regulator

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IIIT-D-MTech-ECE-VLSI-15-17

19th May, 2017

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Submitted in partial fulfillment of requirements for the Degree of M.Tech. in Electronics and Communication Engineering, with specialization in VLSI and Embedded Systems

Certificate

This is to certify that the thesis titled "**Design of a fully on-chip linear regulator**" being submitted by **Rimjhim Khandelwal** to the Indraprastha Institute of Information Technology Delhi, for the award of the Master of Technology, is an original research work carried out by her under my supervision. The thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree/diploma.

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Abstract

Power conditioning circuits form an integral part of a memory chip. Various blocks on a memory chip require uninterrupted power supply that are independent of the load conditions. The program, erase and read operations in a memory chip work at a particular supply voltage. The input / output pins start toggling immediately after the chip is turned on. Therefore, the faster startup of the regulator is also required.

In this thesis, the systematic design of a two-stage linear regulator with an input supply of 3.3V ±10% and output voltage of 2.5V having ±3% accuracy on 300nm technology is stated. Quiescent current of the regulator is 20µA and full load current is 20mA. Load capacitor of the regulator varies from 50pF to 200pF and DC PSRR of the regulator is 60dB. The required startup time of the regulator is less than 1µs.

Various techniques like tail current enhancement, load current enhancement, fast gate node discharge circuit, and splitting Miller capacitance have been tried to acquire the desired startup time of the regulator. The drawbacks of each methodology have been stated. Lastly, a novel capacitor splitting Miller network has been implemented to obtain startup time of less than 1µs. The tail current enhancement along with this technique provides the desired startup time. The technique has been tested across process, input supply voltage and temperature variations (PVT). The comparison between the startup time of the conventional regulator architecture and the new regulator circuit is stated as well.

Acknowledgement

First and foremost, I would like to convey my heartfelt thanks to my internal supervisor, Dr. Mohammad Hashmi for his support and guidance throughout the thesis. I would also like to thank my external thesis supervisor, Pradeep Anantula who introduced me to an interesting research challenge. I would also express my deepest gratitude to Deep Saxena, Pushpita Dutta and Vivek Saraf for their constant support, patience, and encouragement. Their belief in my abilities is the sole factor behind the successful completion of this work. Inspiration and motivation needs a suitable platform to be converted into a meaningful work, I would thus like to thank Jayanth Thimmaiah and the entire analog team for providing such an inspirational and supportive environment to work.

Specially, I would like to thank Mr. Arindam Mishra for his invaluable suggestions and technical support during the last phase of my thesis project. I would also like to express my gratitude to my family and friends whose support and affection kept my moral high in all difficult and challenging situations. Their cheering presence gave me emotional strength to face tough challenges lightly.

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Chapter 1 **Introduction**

1.1 Background and Motivation

Power Conditioning circuits are the integral part of the electrical devices. Every portable device such as mobile phones and laptops requires a constant supply voltage to perform its functions properly. The voltage must be ripple free and load independent. The global supplies such as batteries, generators provide a supply voltage that is very jittery, noisy, and dependent upon the environmental conditions. Moreover, it is dependent upon the varying load attached to it which may be of very high speed, requiring a lot of varying current. Voltage regulators are the circuits that provide this stable supply voltage. They take the ill-regulated load supply as input, and generate a required regulated voltage level as an output. They also reduce load transient deviations, such as voltage droops and frequency spurs. They also prevent the voltage level to reach beyond a regulated DC voltage, thus preventing the IC from breakdown.

Similarly, in the memory system multiple input output ports are connected to a regulator supply. No sooner did the chip is turned on, the I/O ports start toggling. Thus, it is required that the regulator voltage supply is available. Thus, the start-up time of the regulators is very crucial for proper operation of the chip. The faster the supply comes up, the faster the system will respond. It will increase the overall throughput of the memory.

A voltage regulator can be either linear or a switching. A linear regulator is a DC- DC converter that consists of a transistor switch placed in series with the input power supply and the output voltage. The conductance of the pass transistor is linearly controlled through feedback. A switching regulator is an AC-AC, DC- DC, AC-DC or DC-AC converter that energizes the inductor/ capacitor to a certain level and then de-energizes them to obtain the regulated output. Though linear regulators have limited output range ($V_{OUT} < V_{IN}$) and lesser efficiency in comparison to switching regulators ($V_{OUT} \leq V_{IN}$ or $V_{OUT} \geq V_{IN}$), switching regulators are very slow than linear regulators due to their complex circuitry. They have high noise content and are unsuitable for low power applications. Thus, linear regulators are preferred over switching regulators for low power application.

1.2 Target Specifications

The input voltage of the regulator to be designed on 300 nm is a constant supply of 3.3 V that is available for all the circuits. This external supply also has ±10% variation. The regulator converts the 3.3 supply to 2.5V for the local blocks such as input/output pins. These blocks require the regulator to provide the regulated supply very quickly. For the early operation of the memory chip, the regulator must start within 1 µs with 2 % settling tolerance. Since, the power dissipation from the LDO must be less, the quiescent current has a maximum of 20 µA. The internal I/O logic and data path logic operates at a high speed, huge current is consumed in their operation. At the regulator output, I/O pins are connected each of which consume 4mA of load current. Thus, the maximum load current that is seen at the regulator output is 20 mA.

A minimum 50 pF of decoupling capacitor is present always at the output of the regulator circuit. The input capacitance of each I/O pin is around 30 pF. Therefore, the maximum capacitance that is seen at the regulator output is 200 pF. The variation allowed in the output due to all the factors (supply variations, random and systematic variations and gain error) is only ± 3%. The DC PSRR of the regulator is 60 dB. The leakage current of only 200 nA is allowed in the MOS devices. The specifications of the regulator to be designed are summarized in Table 1.1

Serial Number	Parameters	Values
1.	Input Voltage	3.3V±10%
2.	Output Voltage	2.5V
3.	Full Load Current	20 mA
4.	Output Load Cap range	50pF to 200 pF
5.	Startup time	< 1 μs
6.	Quiescent current	< 20 μA
7.	Accuracy	± 3%
8.	DC PSRR	60 dB
9.	Leakage current	200 nA
10.	% Tolerance	2%

Table 1.1: Specifications of linear regulator to be designed

1.3 Thesis Outline

The thesis organization is as follows:

Chapter 1 discusses the motivation and the introduction behind this work.

Chapter 2 discusses the conventional linear regulator architecture, the specifications of the regulator and other related works.

Chapter 3 explains the various building blocks of the regulator. Herein, variation of MOS parameters has been characterized. The different blocks such as single stage amplifier, current mirrors and differential amplifier are also discussed.

Chapter 4 describes the design of basic regulator circuit, derivation of device sizes, stability analysis as well as mismatch analysis.

Chapter 5 discusses the startup time enhancement techniques. It states various nonlinear techniques that were implemented, the drawbacks of each of them. It also describes the delay circuit that was used for providing the pulse. Finally, the technique used for startup time enhancement was explained with results and findings.

Chapter 6 concludes the thesis and state the future work.

Chapter 2 Literature Survey

2.1 Conventional linear regulator architecture

The linear regulator is a DC-DC converter which provides a constant voltage output. It supplies stable, constant, accurate and load independent voltage. Linear Regulator consists of a pass transistor and error amplifier to regulate the output. The block diagram of the linear regulators is shown in Figure 2.1. The pass transistor takes the V_{IN} (or V_{DD}) as input and give V_O as output. This output is regulated through the negative feedback loop which consist of a resistor divider network and the error amplifier. A fraction of the output is fed into the error amplifier which compares it with a reference voltage level. The output of the error amplifier controls the conductance of the pass transistor, eventually regulating the output.

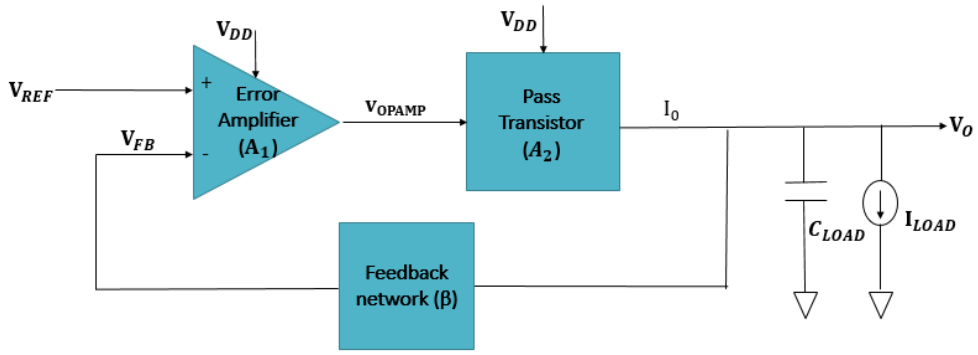

Figure 2.1: Block Diagram of Linear Regulator

2.2 Specifications of linear regulator

The linear regulator has a number of design specifications as discussed below [1], [7-9]

- **Headroom Voltage** - The difference between the input and output voltage is headroom for the regulator circuit.

$$Headroom\ voltage = V_{IN} - V_{OUT} \quad (2.1)$$

The headroom of the linear regulator to be designed is 800mV.

- **Quiescent Current**- It is the maximum current required to operate the internal circuitry of the regulator. The internal circuitry consists of an error amplifier, output pass transistor stage, and the feedback network.

$$I_Q = I_{IN} \quad (2.2)$$

The quiescent current of the regulator must be less than or equal to 20 µA.

- **Load Regulation (LDR)** - The ability of the regulator to maintain the constant output voltage when the load current is varying is called load regulation. It is measured when the output voltage has reached steady state.

$$Load\ Regulation = \Delta V_{OUT} / \Delta I_Q |_{t->\infty} \quad (2.3)$$

- **Line Regulation (LNR) -** It is the ability of the regulator to maintain the constant output voltage when the input voltage is varying. It is measured when the output voltage has reached steady state.

$$Line\ Regulation = \Delta V_{OUT} / \Delta V_{IN} |_{t->\infty} \quad (2.4)$$

- **Gain Error (GE)** - The deviation of the gain from its original value in a feedback loop is known as gain error.

  Transfer function of a regulator circuit from V_{REF} to the output voltage (Figure 2.1),

$$\frac{V_{OUT}}{V_{REF}} = \frac{A_0}{1+A_0\beta} \approx \frac{1}{\beta}\left(1 - \frac{1}{A_0\beta}\right), GE = \frac{1}{A_0\beta} \quad (2.5)$$

- **Power Supply Rejection Ratio (PSRR)** - It is the measure of how well the variation in the supply voltage is suppressed by the circuit so that they do not affect the output voltage.

$$PSRR = -20 \log (Vout/ Vin) \quad (2.6)$$

  DC PSRR is equal to the line regulation of the circuit. Its value must be 60 dB.

- **DC Accuracy** - The total variation of the output voltage due to load regulation, line regulation, PSR, gain error i.e. the systematic error as well as the random variation in the circuit accounts to the complete accuracy of the LDO circuit.

$$Accuracy = (\Sigma\ systematic\ variation + \Sigma\ random\ variation)/ Vout = (LDR + LNR + Ge + random\ variation)/ Vout \quad (2.7)$$

  For the regulator circuit, the dc accuracy must be at least ±3%.

- **Startup time** - The time taken by the complete regulator circuit to turn on and provide the required constant output voltage after it is enabled, is the startup time. It is the sum of the dead time, slew time and the settling time of the circuit.

$$\Delta\ t\_startup = \Delta\ t\_dead + \Delta\ t\_slew + \Delta\ t\_settling \quad (2.8)$$

  - **Dead time** is the time for which the output remains zero after the circuit is enabled. It is the time taken by the pass transistor to turn on the output stage.
  - **Slew time** is the time taken by the output capacitor to charge until the voltage which when fed back the regulator operates in small signal region.
  - Rest of the start-up time is the **settling time** of the transistor. It is dependent on the unity gain bandwidth of the circuit.

  Thus, the startup time is dependent upon the load capacitance, current in each stage as well as the gain- bandwidth of the regulator circuit. The startup time of the regulator circuit must be less than 1µs according to the specifications.

- **Stability** - The stability of the regulator circuit is a very crucial design requirement. It is dependent on the pole location of each stage, and the unity gain bandwidth of the circuit. Various compensation techniques can be used to stabilize the regulator circuit, viz. dominant pole compensation, Miller compensation and nested Miller compensation [5,10]. The stability of the circuit is enhanced by keeping the non-dominant poles much outside the unity gain frequency. This will raise the phase margin of the circuit.

2.3 Summary and Related Work

Different architectures of the regulator circuit can be used as per the specifications. If the gain requirement of the regulator is small, then a single stage error amplifier can be used [2]. A higher gain requirement is met either through a two-stage error amplifier [3] or using other single stage configurations such as cascode or folded cascode amplifiers [5].

A voltage buffer stage can also be introduced between the error amplifier and the pass transistor stage for faster transient response and improved stability [4,7]. Voltage buffer reduces the impedance seen by the large parasitic gate capacitance of the pass transistor. Thus, shifting the pole at that node outward. It helps in improving the bandwidth of the circuit. It also helps in providing extra current to discharge the parasitic capacitance at the gate terminal of the pass transistor. Thus, boosting the transient performance of the circuit.

Various compensation techniques can be used to enhance the stability of the regulator circuit, viz. Miller compensation [5], nested Miller compensation technique [6,11], and damping factor compensation circuit [3]. The stability of the circuit has a direct impact on the startup time of the circuit. Thus, the faster the circuit achieve stability, the lesser is the startup time.

Several nonlinear techniques can be used to improve the startup time like enhancing tail current [2], load current enhancement, and adding voltage buffer stage [4].

Chapter 3 **Building Blocks**

3.1 MOS Characterization

3.1.1 Effect of variations of MOS dimensions on threshold voltage

In a MOS transistor, the gate region can be represented as the capacitor. When the potential is applied at the gate terminal, first the depletion of holes occurs at the substrate, then as the gate potential is increased, inversion occur i.e. minority carriers (electrons for p-substrate) are collected near the gate forming a channel. The gate potential at which the channel is formed is known as the threshold voltage. Threshold voltage shows variation with different parameters, such as MOS dimensions, temperature, etc.

3.1.1.1 Variation of Threshold voltage with length

Ideally, threshold voltage measurement is derived considering the potential applied only at the gate terminal. However, in typical transistors drain and source region are also included resulting reverse biased source-substrate and drain-substrate regions (Figure 3.2). Therefore, the part of the depletion charge which must otherwise be entirely imaged by gate is now contributed by source and drain terminals. This reduced depletion charge contribution solely from gate terminal eventually results in lesser threshold voltage. This effect is predominant in short channel devices because depletion charge contribution from drain and source are significant. Keeping width constant, as the length of a transistor is reduced (Figure 3.1) the threshold voltage continues to decrease. This phenomenon is called **short channel effect.** [5].

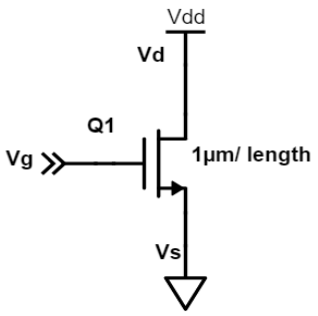

Figure 3.1: NMOS transistor with constant width and varying length

Several techniques such as LDD, non-uniform substrate doping is used to counter this effect. All these techniques help in reducing depletion charge contribution from drain and source. Thus, the threshold voltage remains constant with decreasing length. Moreover, for small lengths as the channel length increases the effective doping per unit channel length decreases. Therefore, the threshold voltage appears to decrease with increasing length. At higher length, it becomes constant.

In Figure 3.3, for a particular region of length, the threshold voltage rises significantly. This in literature is known as reverse short channel effect (RSCE). The threshold voltage is increased by

implanting extra channel doping for that specific length. Small channel MOS devices are extensively used in digital circuits for their high-speed applications. Since digital systems comprises of billions of transistors, it is extremely important to minimize the leakage current thereby reducing power dissipation of the system in the standby mode. Thus, threshold voltage is deliberately made high to reduce the leakage current at particular length. As an example, the device used in Figure 3.1 has minimum leakage for certain lengths.

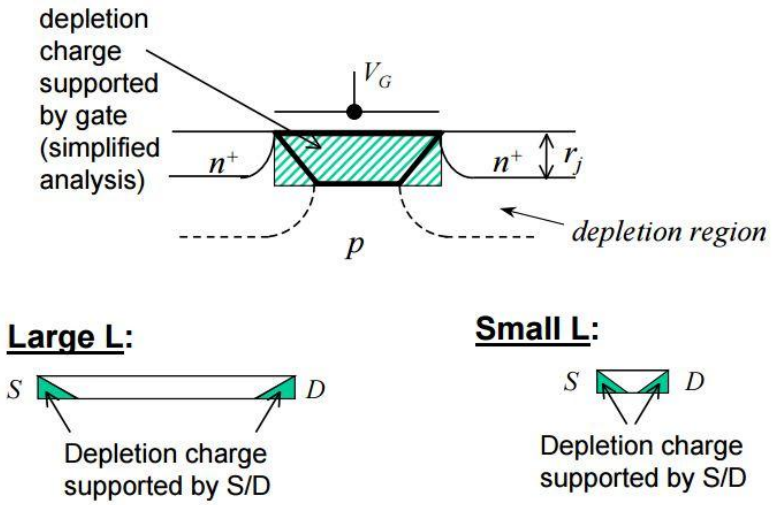

Figure 3.2: Depletion charge supported by gate terminal in small and large channel length [14]

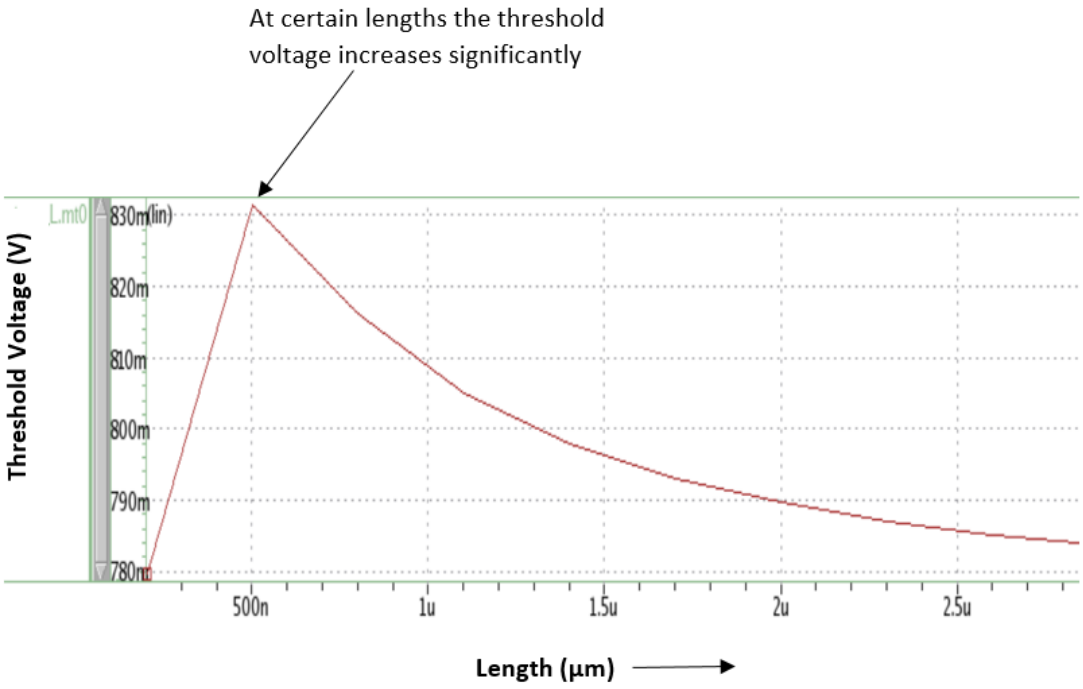

Figure 3.3: Graph showing variation of threshold voltage with length

3.1.1.2 Variation of Threshold voltage with width

The variation of threshold voltage with small channel width (Figure 3.4) is known as narrow channel or reverse narrow channel effect [1].

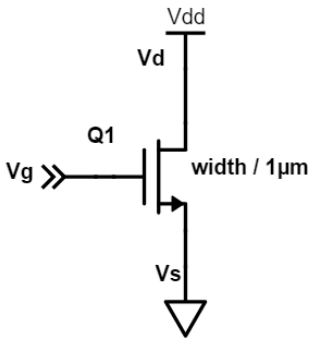

Figure 3.4: NMOS transistor with constant length and varying width

Before a MOS device is formed on p-substrate, the oxide layer is grown on the top of the substrate. Looking at the MOS device across the width, the thin gate oxide layer and channel are surrounded by the LOCOS from both the sides and the transition from LOCOS to thin oxide is not abrupt but gradual (Figure 3.5). This results in increment in the effective width of the MOS transistor. Thus, the threshold voltage of the MOS device increases as the width is decreased. This effect is predominant for narrower channel.

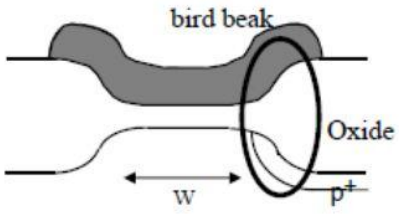

Figure 3.5: Buck beak in transition from LOCOS to thin oxide [14]

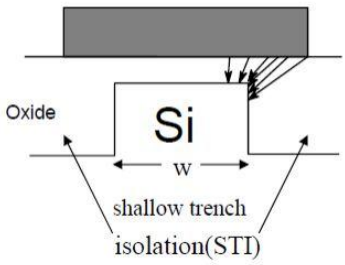

Figure 3.6: STI process for MOS fabrication [14]

To counter this effect, a new method of MOS device fabrication is used called Shallow Trench Isolation (STI) (Figure 3.6). In this process, a trench instead of the oxide layer provides the isolation between two MOS devices. This ensures that the effective width of the device remains constant even at narrower devices. This is called **reverse narrow channel effect** (Figure 3.7).

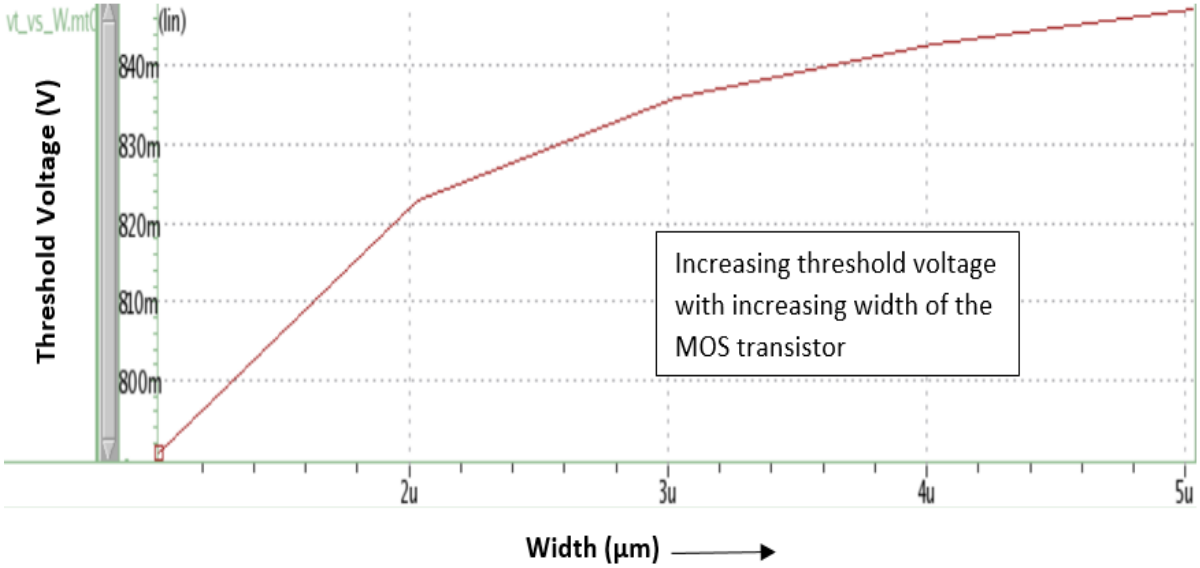

Figure 3.7: Graph showing variation of threshold voltage with width

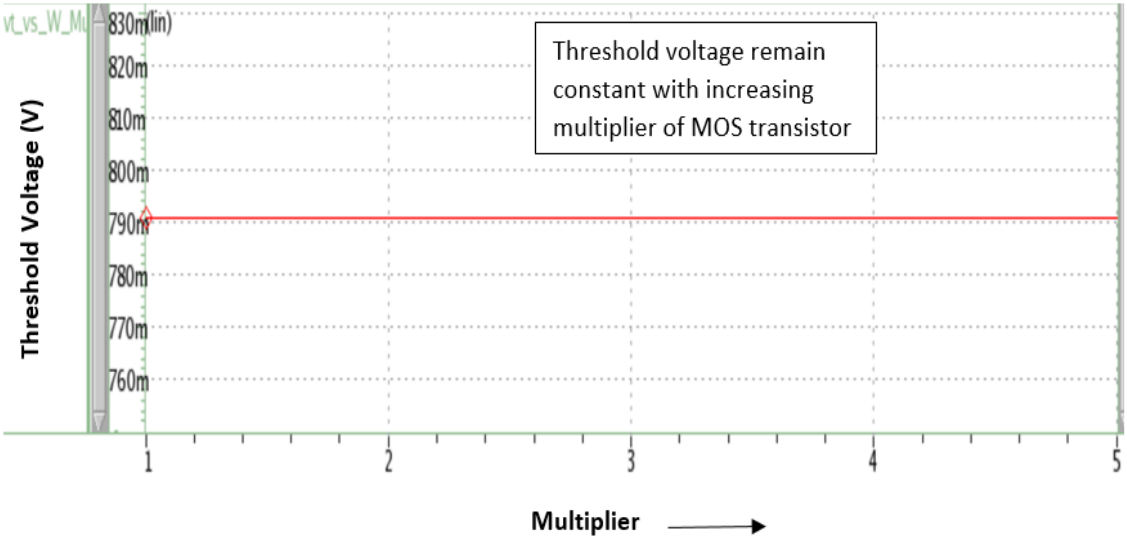

Figure 3.8: Graph showing variation of threshold voltage with increasing multiplier

If instead of varying the width of the MOS device, the multiplier is varied, then the threshold voltage remains constant. The results can be seen in Figure 3.8. Adding the multiplier means

adding multiple similar sized transistors in parallel. Thus, the threshold voltage of each unit remains constant.

3.2 Building blocks of amplifier

3.2.1 Single stage common source amplifier

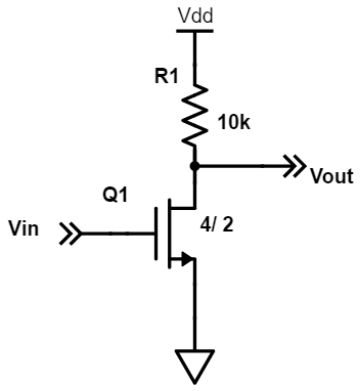

Figure 3.9: Common Source Amplifier with resistor load

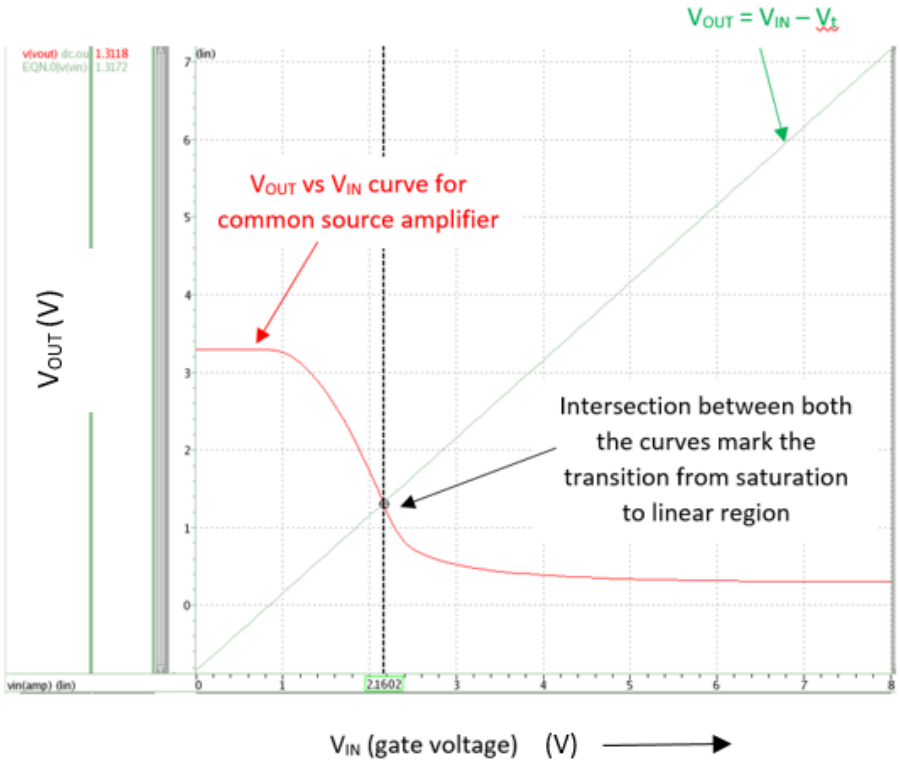

Figure 3.10: The V_{OUT} vs V_{in} curve for common source amplifier with resistor load

The common source amplifier has the source terminal common between the input (gate) and the output (drain) terminals (Figure 3.9). Until the input voltage is below threshold voltage, the MOS transistor is off. Thus, no current flows through the MOS transistor, i.e. no current through the resistor resulting into output equal to the supply voltage. As the input voltage increases, the current starts to flow and the output voltage begins to drop. The current increases with increase in input voltage resulting in decrease in the output voltage. Until the point V_{OUT} is greater than $V_{IN} - V_t$ the device is in saturation. After that, it enters linear region. The intersection between V_{OUT} vs V_{IN} curve and $V_{OUT} = V_{IN} - V_t$ curve gives the transition point from saturation to linear region as shown in Figure 3.10.

The gain of the common source amplifier is, $A_V = - g_m R_1$. Since, g_m increases in saturation region and decreases in linear region (Figure 3.11), MOS is preferably operated in saturation.

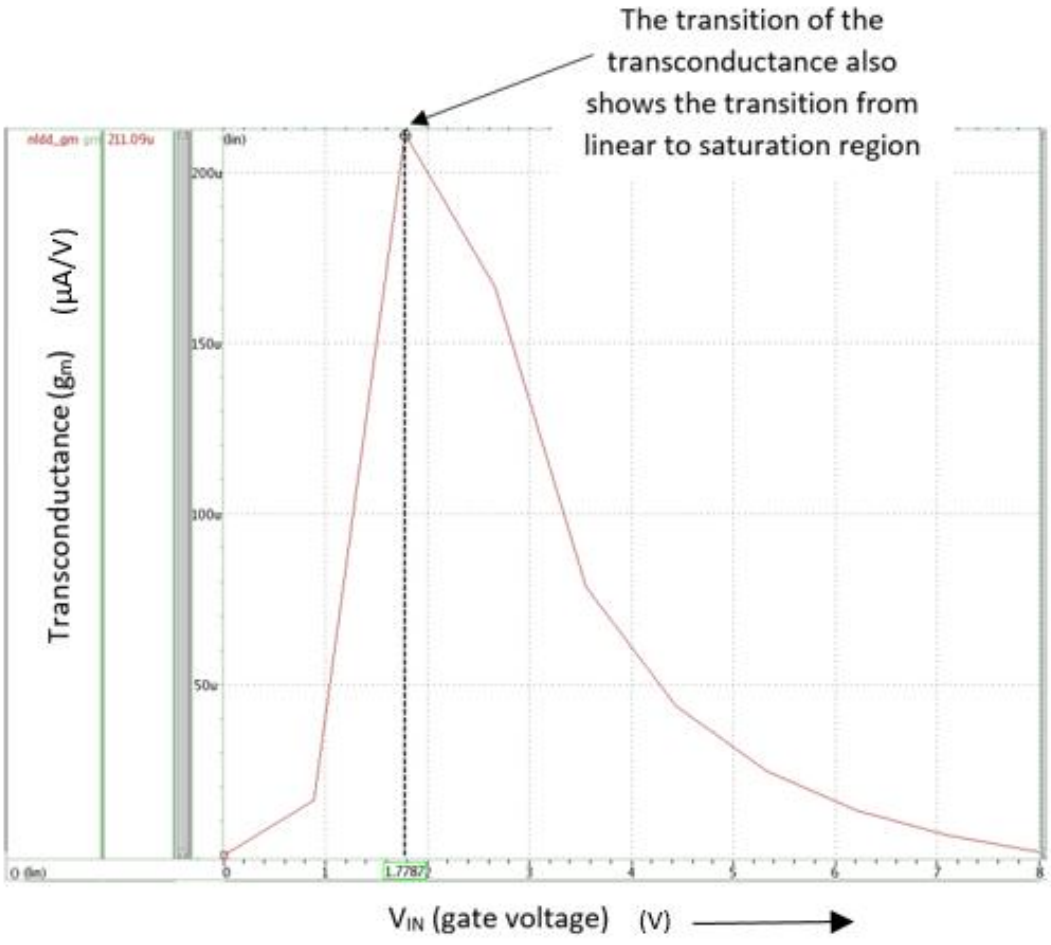

Figure 3.11 Graph showing Variation of g_m with V_{IN}

3.2.2 Common source amplifier with diode connected load

The resistor (R1) in the common source amplifier of Figure 3.9 can be realized using the diode connected MOS load as shown in Figure 3.12. The small signal resistance of the diode load device is $1/g_m$. Thus, the small signal gain of the MOS amplifier is,

$$A_v - g_{mINP0}/\ g_{mLOAD0} \tag{3.1}$$

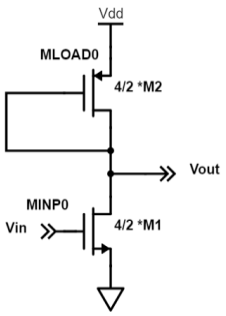

Figure 3.12: Common source amplifier with Diode Connected load

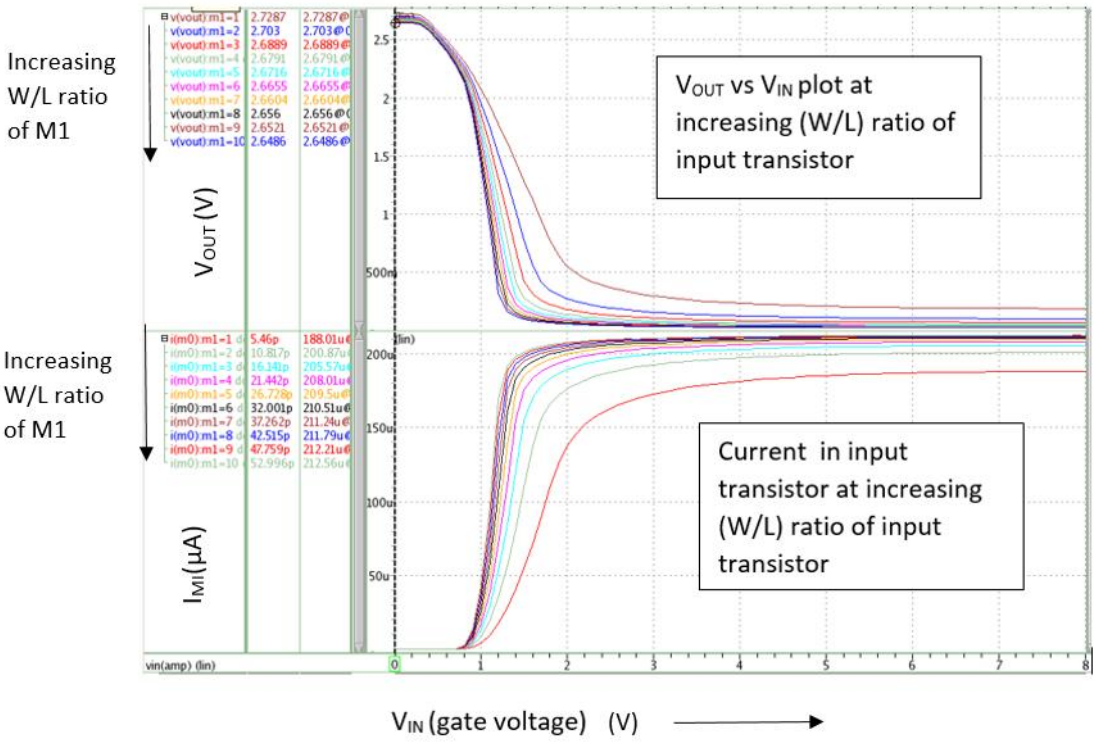

Figure 3.13: Plot of output voltage and input transistor current vs VIN at different W/L ratio of input transistor

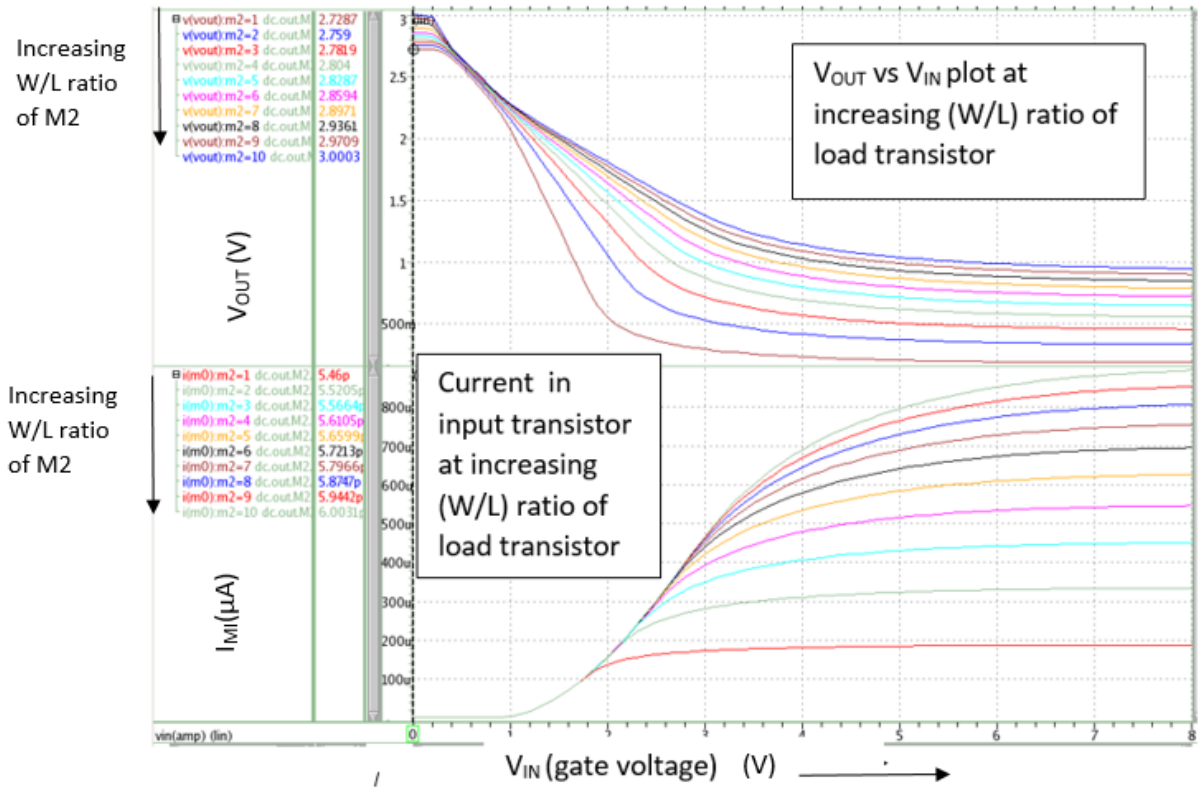

Figure 3.14: Plot of output voltage and input transistor current vs VIN at different W/L ratio of diode load transistor

The variation of the gain with varying W/L of the input transistor is shown in Figure 3.13. When $(W/L)_{MINP0}$ is increased, g_{mINP0} increases. This leads to increase in the rate of change of V_{OUT} w.r.t V_{IN}. The current in the entire amplifier also increases. Not only this, the leakage current (due to subthreshold conduction) also increases 10 times when the size is increased by 10 times. As the W/L ratio of the load MOS device is increased (Figure 3.14), subthreshold leakage current increases. It leads to higher value of the output voltage when MINP0 is off. The g_{mLOAD0} also increases with increase in W/L resulting in decrease in the gain or slope of the graph of V_{OUT} vs V_{IN}.

3.2.3 Current Mirrors

The current mirror (Figure 3.15) copies the current of one transistor into the other transistor. If two transistors are in saturation and their V_{gs} is same, ignoring the second order effect the current through them is also as per the current equation,

$$I = \frac{1}{2}\,\mu_n C_{OX}\frac{W}{L}\,(V_{gs} - V_t)^2 \tag{3.2}$$

Thus, the current from one transistor is copied into other. By varying the W/L ratio of the second transistor, multiple values of current can be generated in it, i.e.

$$\frac{I_{CURR1}}{I_{CURR2}} = \frac{(W/L)_{CURR1}}{(W/L)_{CURR2}} \tag{3.3}$$

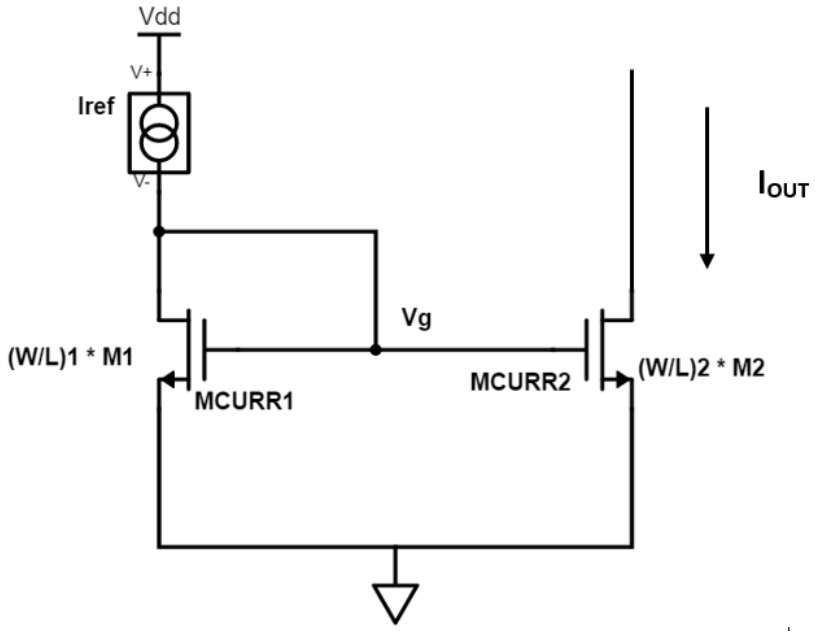

Figure 3.15: Current Mirror circuit

Matching of current in both the transistors is a prime requirement in the current mirror. The accuracy of the circuit designed using the building blocks must be budgeted according to the mismatch. The mismatch can be due to systematic or random variations. The systematic variations are caused mainly due to difference in the V_{ds} value. If second order effects are also included, the complete current equation is

$$I = \frac{1}{2}\,\mu_n C_{OX}\,\frac{W}{L}\,(V_{gs} - V_t)^2\,(1 + \lambda\,V_{ds}), \tag{3.5}$$

Where λ is channel length modulation parameter.

$$\frac{I_{CURR1}}{I_{CURR2}} = \frac{\left(\frac{W}{L}\right)_{CURR1}(1 + \lambda\,V_{ds\_CURR1})}{\left(\frac{W}{L}\right)_{CURR2}(1 + \lambda\,V_{ds\_CURR2})} \tag{3.6}$$

Various configurations such as cascode current mirror are used to reduce the systematic variations. The random mismatch in the current mirror is calculated by the difference in the current that occurs due to variations such as V_t mismatch, β mismatch and V_{gs} mismatch.

The mismatch in the current mirror if $\Delta V_{gs} = 0$ is [13],

$$\frac{\Delta I}{I} = \frac{\Delta\beta}{\beta} - \frac{g_m}{I}\,\Delta V_t \tag{3.7}$$

If Δβ = 0, then standard deviation in current,

$$\frac{\sigma\,(I\Delta)}{I} = \frac{g_m}{I}\,\sigma(\Delta V_t) = \frac{2}{(V_{gs} - V_t)}\,\sigma(\Delta V_t) \tag{3.8}$$

where $\sigma(\Delta V_t) = \frac{A_{Vt}}{\sqrt{(W\,L)}}$ and A_{Vt} is threshold mismatch constant.

Thus, the W/L ratio of current mirror circuits must be small to give high overdrive and lesser mismatch. However, the individual width and length values must be higher to decrease the threshold voltage variations.

3.2.4 Differential Amplifier

The differential amplifier consists of two common source amplifiers whose source terminals are connected to a common potential. The common source potential is connected to a current source. This implies that the total current in the differential pair remains constant. When differential voltage is applied at the input of respective transistors, the current increases in one branch and decreases in other, resulting in difference in output voltage.

The output of the differential amplifier can be made single ended by using a current mirror load. In such a configuration, the current in one branch is mirrored into the load transistor of the other branch (Figure 3.16). The differential amplifiers are the transconductance amplifiers converting the difference in input voltage into output current mismatch.

The small signal gain of the 5-transistor differential amplifier is $A_v = g_m r_o$, where $r_o = r_{o2} \parallel r_{o4}$.

There are other topologies of the differential amplifier such as cascode or folded cascode differential amplifier as discussed in Appendix B.

Mismatch in the differential amplifier.

For the differential input pair, if current in both the branches is equal, then the V_{gs} of both the devices must be same. The random offset in V_{gs} offset can be derived [13] as

$$\Delta V_{gs} = -\frac{\Delta\beta}{\beta}\,\frac{I}{g_m} + \Delta V_t \tag{3.9}$$

If the β variation is not considered, then

$$\sigma\left(\Delta V_{gs}\right) = \sigma\,(\Delta V_t) \tag{3.10}$$

Total mismatch for the complete differential amplifier with the current mirror load is

$$\sigma\left(\Delta V_{gs}\right)_{total} = \sqrt{(\sigma\left(\Delta V_{t_{inp}}\right))^2 + (\frac{g_{m_{LOAD}}}{g_{m_{inp}}}\,\sigma\left(\Delta V_{t_{LOAD}}\right))^2} \qquad (3.11)$$

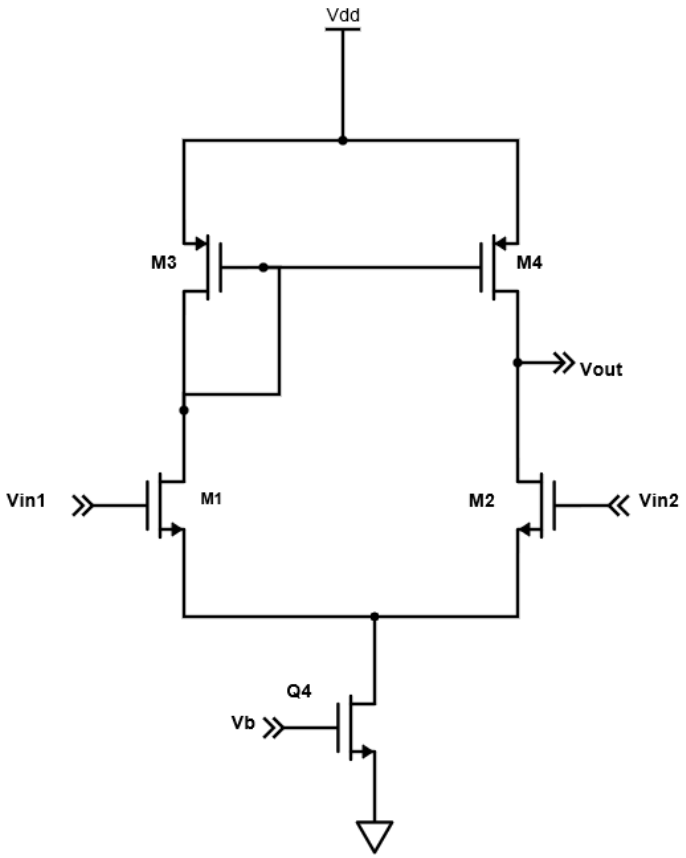

Figure 3.16: Differential Amplifier with current mirror load

Chapter 4 Conventional Linear Regulator Design

4.1 Can a single stage be used to design the regulator?

The block diagram of the single stage regulator is shown in Figure 4.1. The single stage linear regulator comprises of an amplifier connected in feedback using the feedback network (Figure 4.2) where I_Q is the total tail current in the differential amplifier, C_{LOAD} is the load capacitor and ΔV_{OUT} is change in output voltage in Δt time.

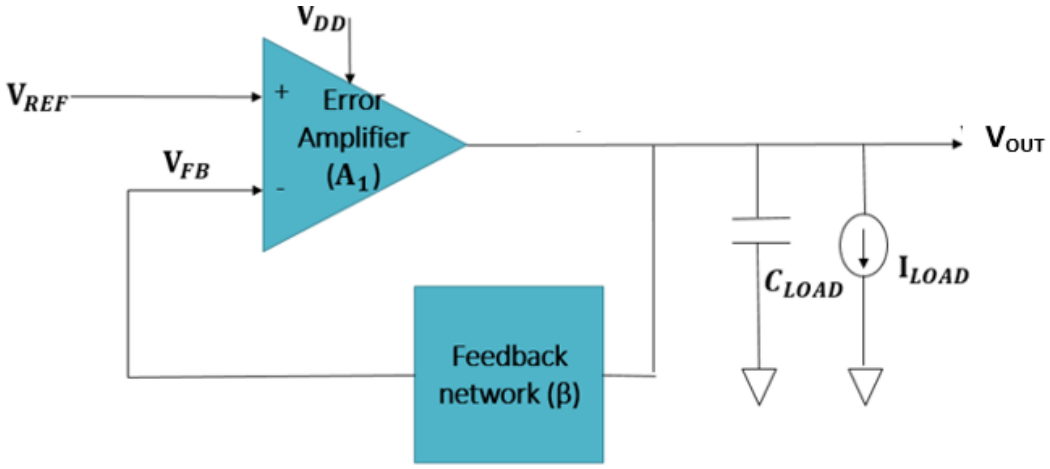

Figure 4.1: The block diagram of single stage linear regulator

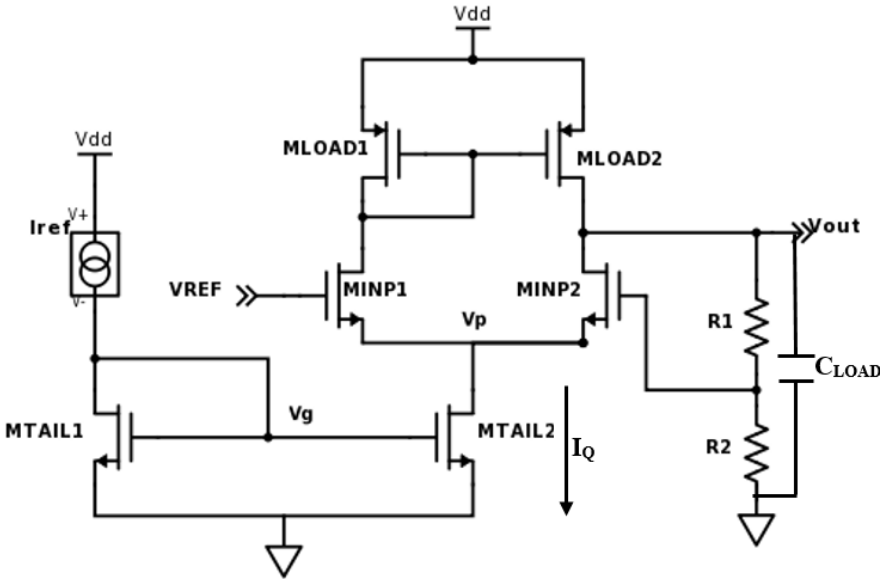

Figure 4.2: Single stage regulator circuit

It is assumed that the circuit slews for the entire startup period and then settles to its desired output, then the current requirements to achieve the desired startup time can be calculated as below,

Case 1: If the entire startup time is consumed by slewing,

$$\text{Slew rate, } \frac{\Delta V_{OUT}}{\Delta t} = \frac{I_Q}{C_{LOAD}} \tag{4.1}$$

When $\Delta V_{OUT} = 2.5$, $C_{LOAD} = 200$ pF, $\Delta t = 100$ ns, from equation (4.1) $I_Q = 5$ mA

Case 2: If the entire startup time is governed by settling time,

$$V_{OUT}(t) = V_{OUT(final)}\left(1 - e^{-\frac{t_{settling}}{\tau}}\right) \tag{4.2}$$

For 2% settling, when $V_{OUT\ (final)} = 2.5$, t=100ns, time constant, $\boldsymbol{\tau} = 25.56$ ns. So, Unity Gain Bandwidth (UGB), $\omega = 1/\boldsymbol{\tau} = 39$ M rad/s. For a single stage amplifier with transconductance and overdrive voltage of input pair as g_{m1} and V_{OD1} respectively.

$$\omega = \frac{g_{m1}}{C_{LOAD}} \tag{4.3}$$

$$g_{m1} = \frac{I_Q}{V_{OD1}} \tag{4.4}$$

Since $V_{REF} = 1.2$ V, if threshold voltage of NMOS, $V_t = 1$V, then $V_{OD1} \approx 0.1$V, then from equation 4.3 and 4.4, $I_Q = 0.782$ mA.

The current requirement in both the cases is much larger than the I_Q specification of 20 µA. Thus, the single stage is not sufficient to provide the required startup time. Moreover, single stage differential amplifier cannot support the extra DC load current required during full load condition keeping its differential operation intact.

4.2 Design of the two stage Linear Regulator

4.2.1 Derivation of gain and gain error:

In a linear regulator, DC PSRR is equal to open loop gain. Since, DC PSRR is 60 dB according to the specifications, A_0 has to be more than or equal to 1000 V/V or 60dB

$$\text{And, } A_0 = A_1 \times A_2 \tag{4.5}$$

Where A_0 is the total DC loop gain of the linear regulator, A_1 and A_2 are the loop gains for first and second stages respectively.

$$\text{Closed Loop gain, } \frac{V_{OUT}}{V_{REF}} = \frac{A_0}{1+A_0\beta} \approx \frac{1}{\beta}\left(1 - \frac{1}{A_0\beta}\right) \tag{4.6}$$

From equation 4.6,

$$\text{Precision or gain error, } G.E. = \frac{1}{A_0\beta} \tag{4.7}$$

$$\text{The feedback factor, } \beta = \frac{V_{FB}}{V_{OUT}} = \frac{1.2}{2.5} \tag{4.8}$$

From equation 4.7 and 4.8, Gain error = $\frac{1}{A_0\beta}$ = 0.092 %

Thus, the remaining 2.9% of the accuracy can be accommodated for other variations such as systematic offset, random mismatch and noise.

In a linear regulator circuit, the pass transistor operates in different regions as per the load current drawn. When there is no load current, the pass transistor operates in subthreshold region while in full load condition it operates in saturation or linear region. Thus, the gain varies in the pass gate accordingly. Therefore, it is assumed that the entire gain requirement is met from the first stage of the linear regulator. Thus, A_1 = 60 dB or 1000 V/V, A_2 = 1 V/V for hand calculating sizes of transistors.

4.2.2 Selection of the pass transistor stage

The pass transistor forms the second stage of the linear regulator circuit. It is an extra common source / common drain stage which can independently support required load current without influencing the differential operation of the first stage under worst-case process, temperature and input supply conditions. Since, the maximum load capacitance is small (200pF), the circuit is made input pole dominant. Miller compensation is used to improve the stability of the circuit.

Using NMOS (Figure 4.3) as pass transistor helps in improving speed. NMOS is used in source follower configuration. The output impedance of such configuration is $1/g_m$. Thus, speed of the regulator is improved and the output pole moves farther from the input pole improving stability. In NMOS pass transistor, if the source terminal of the transistor (output terminal of the regulator) suddenly droops, then V_{gs} will be increased. This will help in increasing the current supplied by the pass transistor, thus reducing the recovery time.

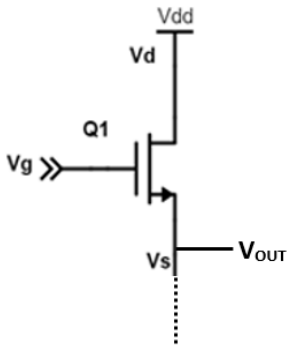

Figure 4.3: NMOS as pass transistor

For turning on the NMOS pass gate, the gate voltage of the pass transistor must be at least one threshold voltage greater than the output voltage, i.e. $V_g \geq 3.5$ V, if V_t = 1V. Since the lowest supply voltage available is 3 V, it is not possible to use the NMOS device as pass transistor. Moreover, using the intrinsic NMOS devices with lower V_t will result in excessive leakage. Hence, PMOS device (Figure 4.4) is used as the pass transistor.

Sizing of PMOS pass transistor - During full load the pass transistor has to support as large as 20mA of current. Which becomes the worst case for sizing the transistor. Again, for no load it carries only 15µA of current. Thus, g_{m_PASS} is very low causing the output load to be closer to first pole degrading the overall stability.

The size of the pass transistor also determines the gate to source and gate to drain parasitic capacitance of the circuit. Thus, the response time is limited by the large W/L ratio.

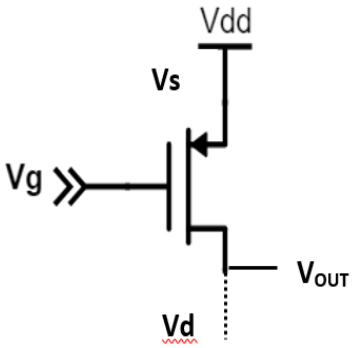

Figure 4.4: PMOS as pass transistor

For PMOS to be in saturation,

$$V_{dg} \leq |V_t| \tag{4.9}$$

For V_{OUT} = 2.5 V and V_t = 1V, from equation (4.9), $V_g \geq 1.5$V

The current in the PMOS device,

$$I_{OUT} = \frac{1}{2}\,\mu_p C_{OX} \frac{W}{L}\,(V_{sg} - |V_t|)^2 \tag{4.10}$$

For V_g =1.5, V_s = 3.3 V, and I_{OUT} = 20 mA, from equation 4.10, the size of the pass transistor is

$$\left(\frac{W}{L}\right)_{PASS} = 480$$

4.2.3 Distribution of current in different stages of the regulator

The primary design requirement of the regulator circuit is to have a low startup time. The current distribution in different branches of the regulator circuit will greatly influence the regulator startup time. The higher the tail current of error amplifier, lesser is the slew time. The higher current in the output stage reduces the settling time. Thus, it is very important to determine the current distribution of the quiescent current between the two stages of the linear regulator (Figure 4.5).

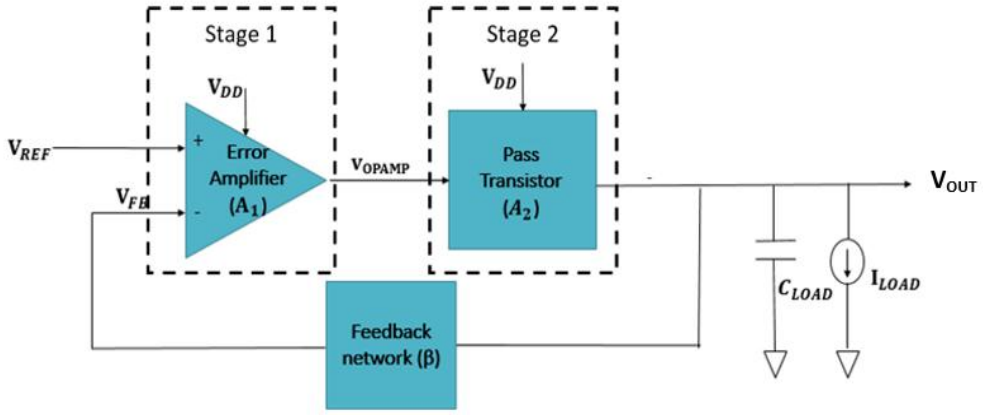

Figure 4.5: Linear regulator architecture

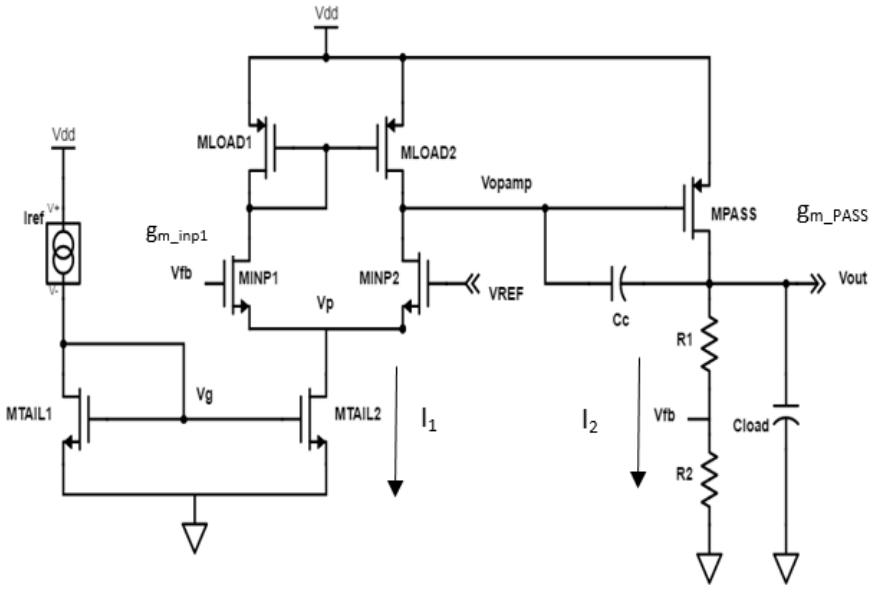

Figure 4.6: Conventional linear regulator

Total quiescent current for the regulator is, $I_Q = 20$ µA. Miller compensation is used for improving stability of the circuit. Assuming f_1 and f_2 the pole locations of first and second stage respectively,

f_0 is the Unity Gain Bandwidth, g_{m_inp1}, g_{m_PASS} be the transconductance of the input of each stage (Figure 4.6), distributed quiescent current in each stage is, $I_1 + I_2 = I_Q$, V_{OD1} is the overdrive voltage of input pair of stage 1, C_c is the compensation capacitor (=10pF) and C_{LOAD} is the output capacitor (=200pF). The phase margin of the system is assumed to be 45°. At such condition, the second pole lie at the unity gain frequency and the system behaves as a single pole system.

$$f_2 = \frac{g_{m\_PASS}}{2\pi C_{LOAD}} \tag{4. 11}$$

For 45° Phase Margin,

$$f_2 = f_0 \tag{4. 12}$$

The unity gain bandwidth is also equal to,

$$f_0 = \frac{A_1 \times A_2}{2\pi \times A_2 \times C_C \times r_{o1}} = \frac{g_{m\_inp1}}{2\pi C_C} \tag{4. 13}$$

$$g_{m\_inp1} = \frac{I_1}{V_{ODinp1}} \tag{4. 14}$$

The time consumed in slewing when $\Delta V_{OUT} = 2.5$,

$$\Delta t_{slew} = \frac{C_C \times \Delta V_{OUT}}{I_1} \tag{4. 15}$$

The settling time for 2% settling is calculated from equation 4.2, where $V_{OUT(final)} = 2.5$, and Time constant, $\boldsymbol{\tau} = \frac{1}{2\pi f_0}$, and t is the settling time.

The possible current distribution and the comparison of the total required slewing and settling time is shown in Table 4.1,

S.No.	I_1 (µA)	I_2 (µA)	Unity Gain Bandwidth (kHz)	Slew time (µs)	Settling time (ns)
1	5	15	1000	5	622
2	10	10	889	2.5	700
3	15	5	628	1.67	990

Table 4.1: Distribution of current in two stages

Since the transition point between the settling and slewing cannot be distinguished clearly, the assumption is made that the output node is slewing in the entire voltage range. Similarly, for settling, the assumption is that the node voltage is settling at 2.5 with zero initial value. Thus, the calculations made are highly approximated.

So, it can be seen that the slewing time increases as the input stage current decreases. Similarly, the bandwidth decreases or the settling time increases as the output stage current is reduced (Figure 4.7). For enhancing the slew time some non-linear techniques are used such as increasing the current of first stage for slew duration or disconnecting the compensation capacitor for the slew time.

Thus, to minimize the settling time and maximizing bandwidth and transconductance of second stage, 5 µA and 15 µA are budgeted as the first and second stage quiescent currents respectively. Requirement of high gain from first stage and stability also necessitates having such a distribution.

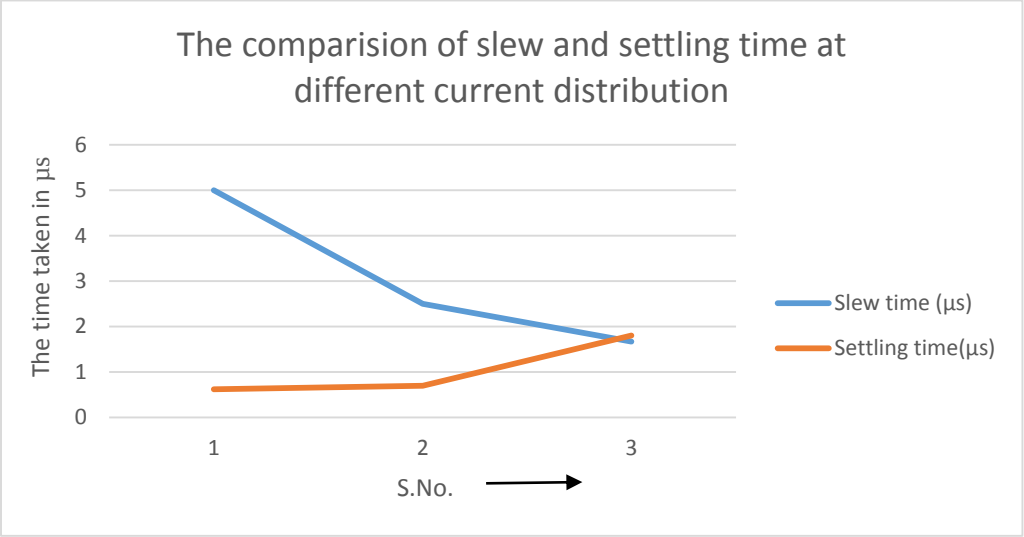

Figure 4.7: Chart showing comparison of slewing and settling time at different current distribution

4.2.4 Error amplifier design

As calculated in section 4.2.1, the total gain required by the differential amplifier is 60dB. Since the available current for the error amplifier is less (only 5µA) and gain required is less, five transistors differential amplifier configuration (Figure 4.8) can be used as error amplifier stage.

Calculation of the sizes for the error amplifier

The transconductance of the input pair is,

$$g_{m_{inp1}} = \sqrt{2 \times \beta \times \left(\frac{W}{L}\right)_{inp1} \times \frac{I_1}{2}} \quad (4.16)$$

From equations 4.11, 4.12, 4.13 and 4.16, $\left(\frac{W}{L}\right)_{inp1}$ = 3. From equation 4.14, $V_{OD\_inp1} = 0.079\ V$.

Since V_{REF} = 1.2 V, if threshold voltage of NMOS, V_t = 1V, then V_p (Figure 4.8) ≈ 0.1V.

Total power consumption of the circuit is

$$P_{TOTAL} = 3.3 \times 20\ \mu A = 66\ \mu W \quad (4.17)$$

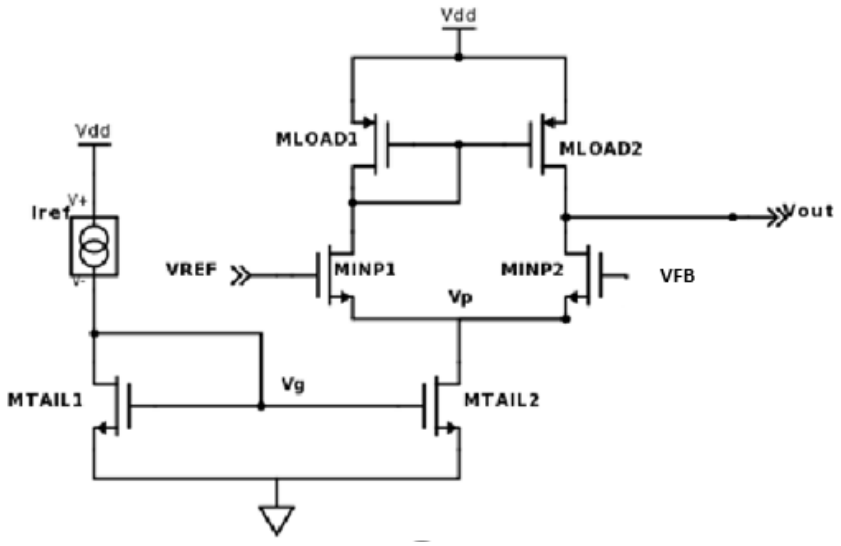

Figure 4.8: Error amplifier architecture

For 5 % power consumption in standby mode, the current through the MTAIL1 (Figure 4.8) MOS is kept 1µA. From section 3.2.3, the higher the mirrored current, lower is mismatch per unit current. Therefore, if the current in MTAIL2 is kept higher, the mismatch is lower in that transistor. The mismatch analysis also shows that the mismatch is lower for the devices with larger sizes but lower W/L ratio. Therefore, if current of a unit transistor is less, W/L is much lesser for a particular V_{gs} value.

Using V_p and Iref =1µA, $(W/L)_{MITAIL1} = 1$, $(W/L)_{MITAIL2} = 1 \times 5$

To maintain equal current density for NMOS input differential pair transistor and PMOS current mirror load, the size of the PMOS load transistors is chosen as, $(W/L)_{MLOAD1} = 3\times 2.5 \approx 8$.

S.No.	Corner	Theoretical Calculation					Simulation	
		g_{m_INP} (µA/ V)	g_{ds_INP} (nA/V)	g_{ds_LOAD} (nA/V)	Gain (dB)	Unity Gain Bandwidth (kHz)	Gain (dB)	Unity Gain Bandwidth (kHz)
1.	TTTVTT	37.5	41.65	61.68	51.2	597.13	51.18	579.66
2.	SSLVHT	30.49	35	32.5	52.95	485.5	53	476.55
3.	FFHVLT	45	51.28	98	49.58	716.56	49.57	647

Table 4.2: Theoretical and simulated calculation of gain and bandwidth of single stage amplifier at 10pF load capacitor and 3.3 V supply voltage

The gain of the differential amplifier can further be increased by increasing the W/L ratio of the input transistor that in turn helps the tail bias transistor (MINP2) to support extra current during tail current enhancement. Higher value of the W/L ratio can move the input pair into subthreshold region. This make it susceptible to input noise. So, the size is decided such that the transistor operates in saturation region. The output resistance, r_{ds} of a MOS device is directly proportional to

its length. Increasing the resistance increases the gain of the transistor. Mismatch is also reduced as the length is increased.

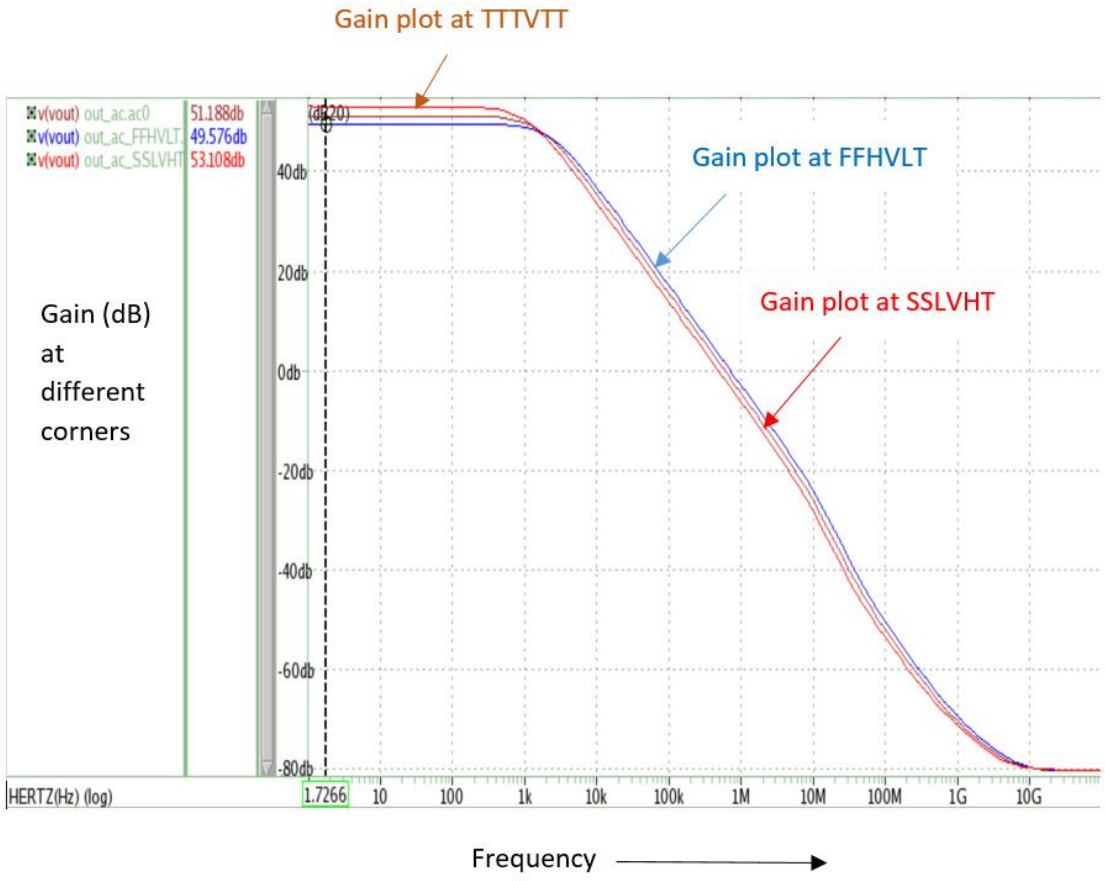

Figure 4.9: Gain plot of error amplifier

Table 4.2 contains the theoretical and simulation calculations of the single stage amplifier. Figure 4.9 presents the bode plot of the error amplifier designed.

4.2.4 The resister divider feedback network

The values of the resistor in the feedback can be derived as follows

The Feedback factor,

$$\beta = \frac{V_{FB}}{V_{OUT}} = \frac{R_2}{R_1 + R_2} = \frac{1.2}{2.5} \quad (4.16)$$

and from the output stage (Figure 4.10)

$$\left(R_1 + R_2 \right) \times I_{OUT} = V_{OUT} \quad (4.17)$$

From equation 4.18 and 4.19, $R_1 = 80\ k\Omega, R_2 = 86.67\ k\Omega$

4.2.5 The complete regulator architecture

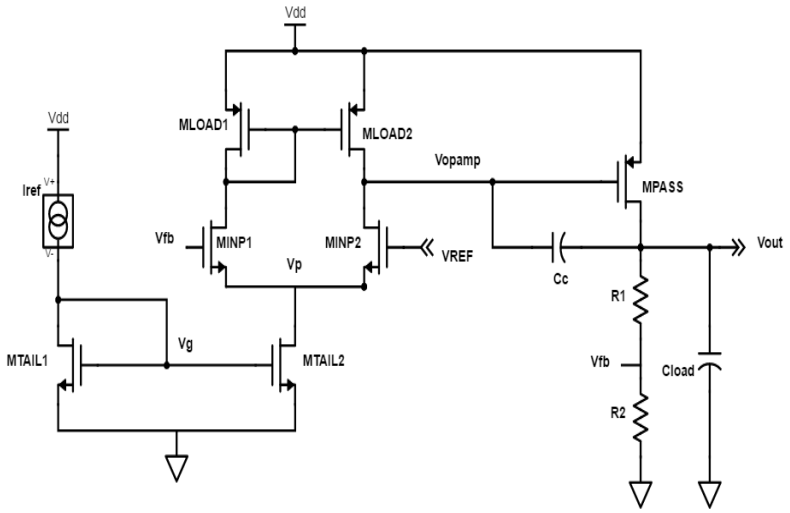

Figure 4.10 Complete regulator architecture

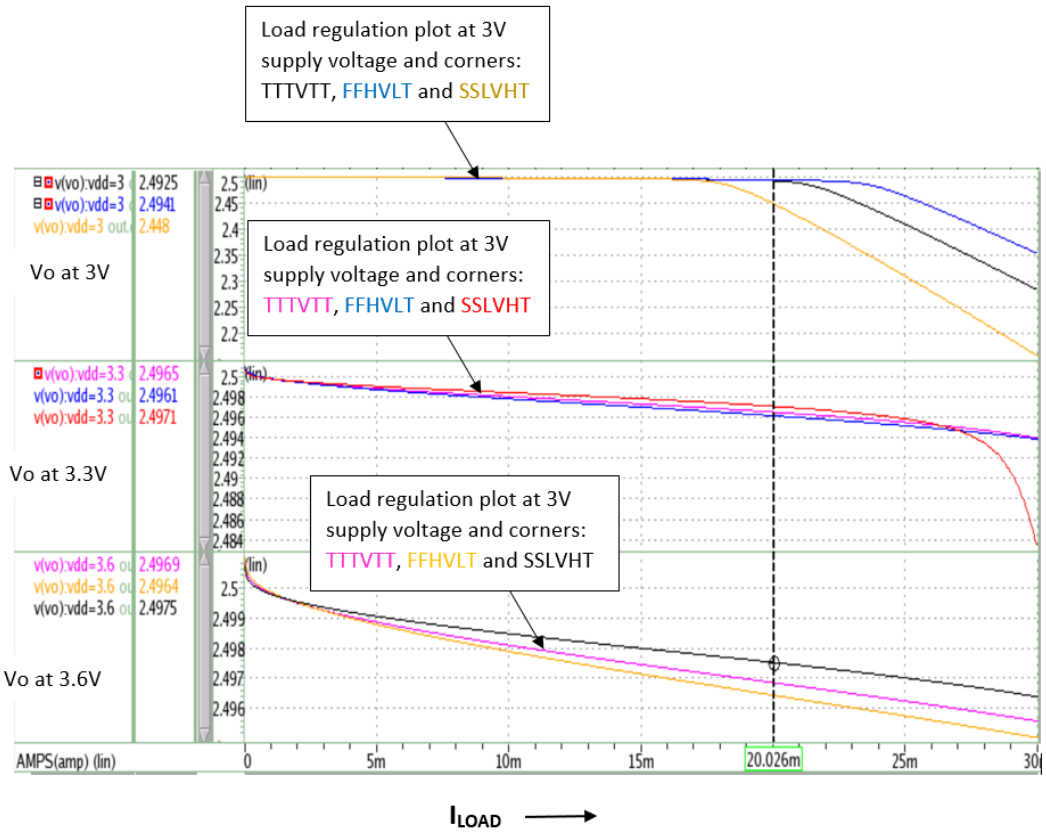

Figure 4.11: Load regulation waveform

In the regulator circuit, the error amplifier and the pass transistor stage are cascaded and connected in feedback using the resistor divider network. The regulator structure is shown in Figure 4.10. The size of the pass transistor is increased according to the load regulation at the supply voltage VDD 3 V. The variation of the output voltage with increasing load current is shown in Figure 4.11. In the waveform, the current is on the x-axis and output voltage is plotted on y-axis at different supply conditions and corners.

4.2.6 Stability Analysis

The Table 4.3 and Table 4.4 shows the theoretical calculation and simulated results of the uncompensated regulator structure.

S.No	I_{LOAD} (mA)	Region of pass transistor	A_1 (V/V)	A_2 (V/V)	A_0 (dB)	f_1 (kHz)	f_2 (kHz)	UGB (MHz)	Comments
1	0	Sub threshold	377.3234	17.152997	76.22108	684	124.99	4428.65	Output pole dominant
2	5	saturation	516.0745	14.798601	77.65866	593.7	909.23	4534.52	Input pole dominant
3	10	saturation	524.055	5.1087243	68.55379	610.5	3039	1634.48	Input pole dominant

4	15	linear	501.3149	1.9286095	59.7071	662.2	7472.13	640.28	Input pole dominant
5	20	linear	437.1429	0.9808822	52.6448	791.6	12743.63	339.45	Input pole dominant

Table 4.3 : Theoretical calculation of gain and pole location of the complete regulator without compensation

S.No	I_{LOAD} (mA)	A_0 (dB)	UGB (MHz)	Phase Margin
1	0	69	1.19	-0.843
2	5	71	8	-7.784
3	10	62	8.05	8.9588
4	15	53	5.84	42.58
5	20	46	0.36	65.87

Table 4.4 : Simulation result for uncompensated regulator circuit at SSLVHT and 200pF load capacitor

The results show that the system is unstable. When the load current is zero (I_2= 15 µA) and the load capacitance is maximum (200pF), i.e. the worst case for the system, the output pole becomes dominant (Table 4.3). Whereas in the other load condition, the input pole is dominant. The phase margin of the system is also poor (Table 4.4).

Miller Compensation is used to improve the system stability [5,10]. In this a compensation capacitor (Cc) is connected between the gate of the pass transistor and its drain (Figure 4.10 Complete regulator architecture). Miller compensation results in pole splitting. The input pole moves further inside and the output pole moves outside. It makes the system input pole dominant. Due to Miller capacitor, a capacitance of (1 +A_2 Cc) is created at node Vopamp, where A_2 is gain of second stage of the regulator circuit. The input pole now is 1/ R_{o1} (1 +A_2 Cc). Here, R_{o1} is output resistance of first stage, the output pole is pushed out to g_{m_PASS}/C_{LOAD}.

S.No	I_{LOAD} (A)	A_0 (dB)		UGB (kHz)		Phase Margin (°)		Gain Margin (dB)	
		FFHVLT	SSLVHT	FFHVLT	SSLVHT	FFHVLT	SSLVHT	FFHVLT	SSLVHT
1	0m	70.9	74.4	294.65	205.025	46.5	45.85	-49.39	-32.23
2	5m	71.1	76.19	410.82	280.74	91.72	90.49	-43.15	-48.2
3	10m	67.1	67.03	398	249.25	91.92	90.68	-42.2	-47.69
4	15m	61.04	58.33	365	193.85	91.87	90.64	-42.53	-49.12
5	20m	54.23	51.04	304.9	143.88	91.64	90.62	-44	-51.24

Table 4.5: Gain, UGB, Phase Margin and Gain Margin results at two corners after compensation

The drawback of Miller compensated structure is that it creates a right half plane zero of magnitude g_{m_PASS}/ Cc due to feed forward connection from input to output through Cc. A resistor is added in the compensation path to compensate this right hand zero. When the magnitude of the resistance is 1/ g_{m_PASS} the zero move to infinity. The magnitude of resistance can be further increased to move the zero into the left half plane to cancel the first non-dominant pole such that the system behaves as single order system. However, as the MOS parameters vary according to the process corner it is very difficult to ensure that the zero exactly cancels the pole. So, R_z is calculated for the worst case such that the requirement across corners and load condition is met.

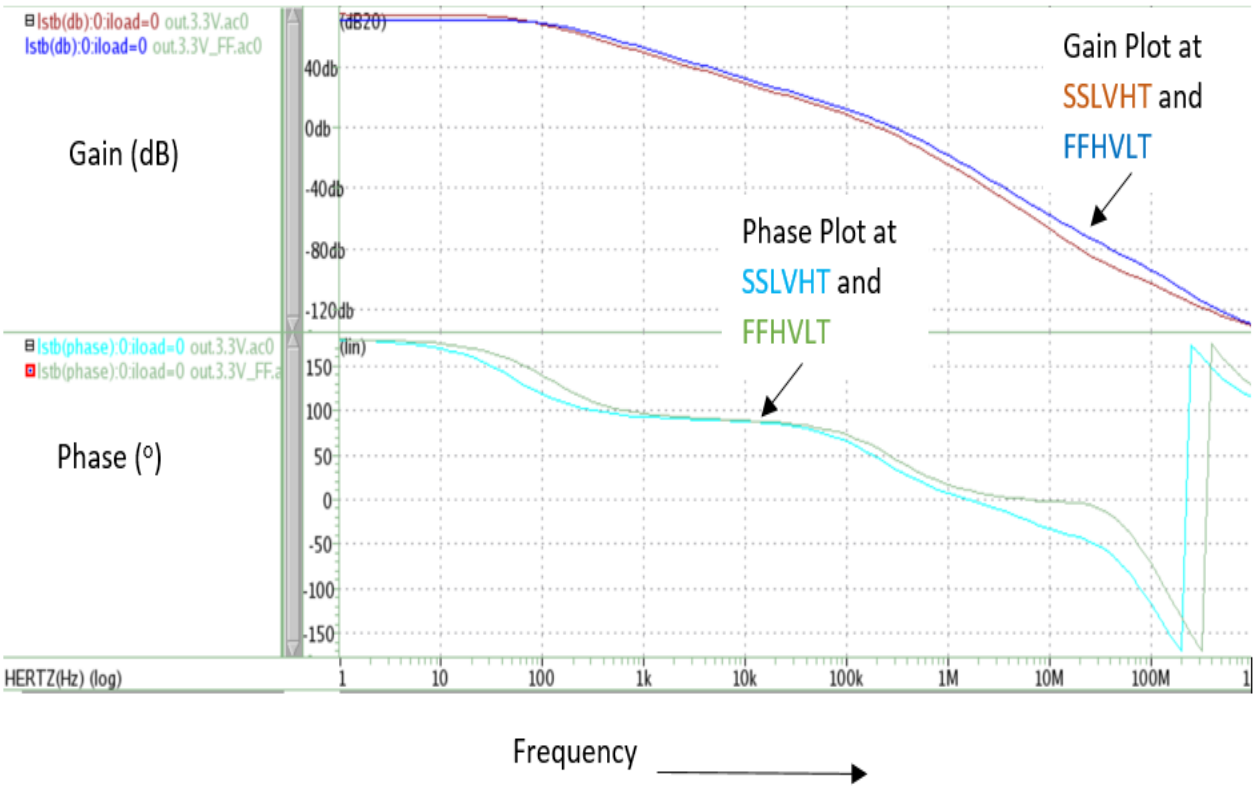

Figure 4.12: Bode plot of regulator at no load current and 200 pF load capacitance

As, $((g_{m\_PASS} \times R_z) - 1) > 0$, implies that $R_z > 1/g_{m\_PASS}$. Thus, minimum value of the transconductance of the pass transistor (i.e. at no load condition and slow corner) must be used for calculating R_z. The value of R_z is calculated to be 4 kΩ. The simulations show that 8pF compensation capacitor along with 4 kΩ of resistance in the miller path results in the phase margin of 45°

The gain, bandwidth, phase margin results after compensation at 200pF load capacitance and are presented in Table 4.5. The phase margin is worst (only 45°) in no load condition and slowest corner. The gain plot and the phase plot of the regulator circuit is present in Figure 4.12. The plot shows the results at two corners SSLVHT and FFLVHT under zero load current and 200 pF load capacitance.

4.2.6 Mismatch Analysis

Monte-Carlo simulation has been done on the circuit designed to calculate the random variations in the circuit, which shows (Figure 4.13)1σ variations as 8.651mV. This implies that 3σ variation are 25.95 mV that is 1% of the output and well within the accuracy limit. At SSLVHT corner, the Monte-Carlo analysis results in 1σ variations of 8.673 mV, resulting in 3σ variation of 26 mV.

The DC mismatch analysis also shows 1σ variations of 8.875 mV. Thus, 3σ variation is 26 mV.

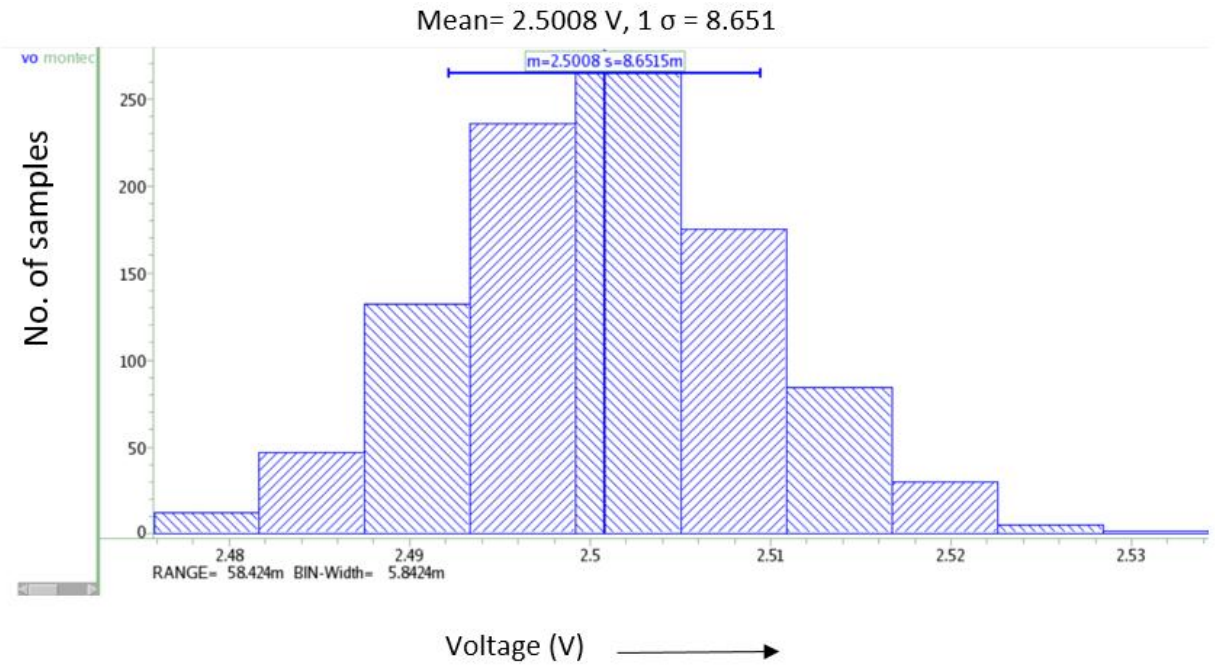

Figure 4.13: Histogram of Monte-Carlo analysis at TTVTTT

Chapter 5 **Startup time enhancement**

5.1 What is startup time?

The time taken by the regulator circuit (Figure 5.1) to reach its steady state regulated value (2.5V) from reset state (initial output 0V) is called the startup time. The faster the startup time, the faster the regulator will supply regulated voltage to the load circuits, improving the overall performance of the DIC.

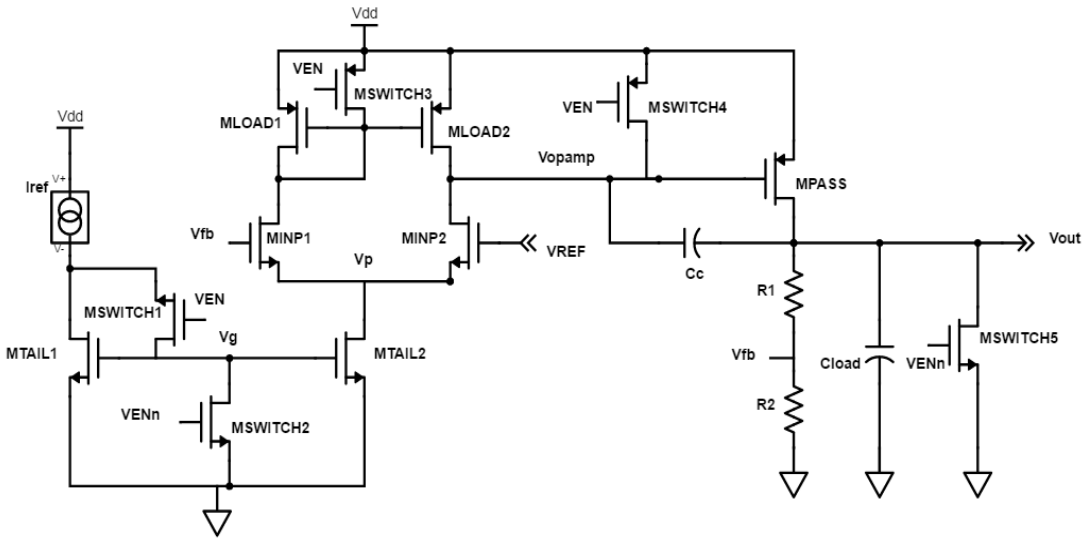

Figure 5.1: Linear regulator circuit

Startup time can be divided into three components- **dead time, slew time** and **settling time**. The dead time is the time taken by the gate node of the pass transistor to go one threshold (V_t) below V_{DD} to switch on the output pass transistor. If ΔV_{OPAMP} (Figure 5.1) is the change in gate node voltage, I_{TAIL} is the tail current of the error amplifier, C_C is the compensation capacitance and Δ t_dead is the time taken to recover dead time, the gate node slews linearly by the rate,

$$\frac{\Delta V_{OPAMP}}{\Delta t\_dead} = \frac{I_{TAIL}}{C_C} \quad (5.1)$$

Once the pass transistor is turned on, the output voltage V_{OUT} would be rising at the rate given in equation 5.2, till it reaches a sufficient voltage which when fed back into the regulator brings the whole circuit in small signal region and further settling is taken over by circuit bandwidth.

$$\frac{\Delta V_{OUT}}{\Delta t\_slew} = \frac{I_{TAIL}}{C_C} \quad (5.2)$$

The settling time Δ t_settling depends on bandwidth of the circuit and can be calculated with 2% tolerance, $V_{OUT(final)} = 2.5$, ω the Unity Gain Bandwidth (UGB) and time constant, $\boldsymbol{\tau} = 1/\omega$, using the formula

$$V_{OUT}\,(t) = V_{OUT(final)}\left(1 - e^{-\frac{t_{settling}}{\tau}}\right) \quad (5.3)$$

Thus, the total startup time t_startup is,

$$\Delta\, t\_startup = \Delta\, t\_dead + \Delta\, t\_slew + \Delta\, t\_settling \quad (5.4)$$

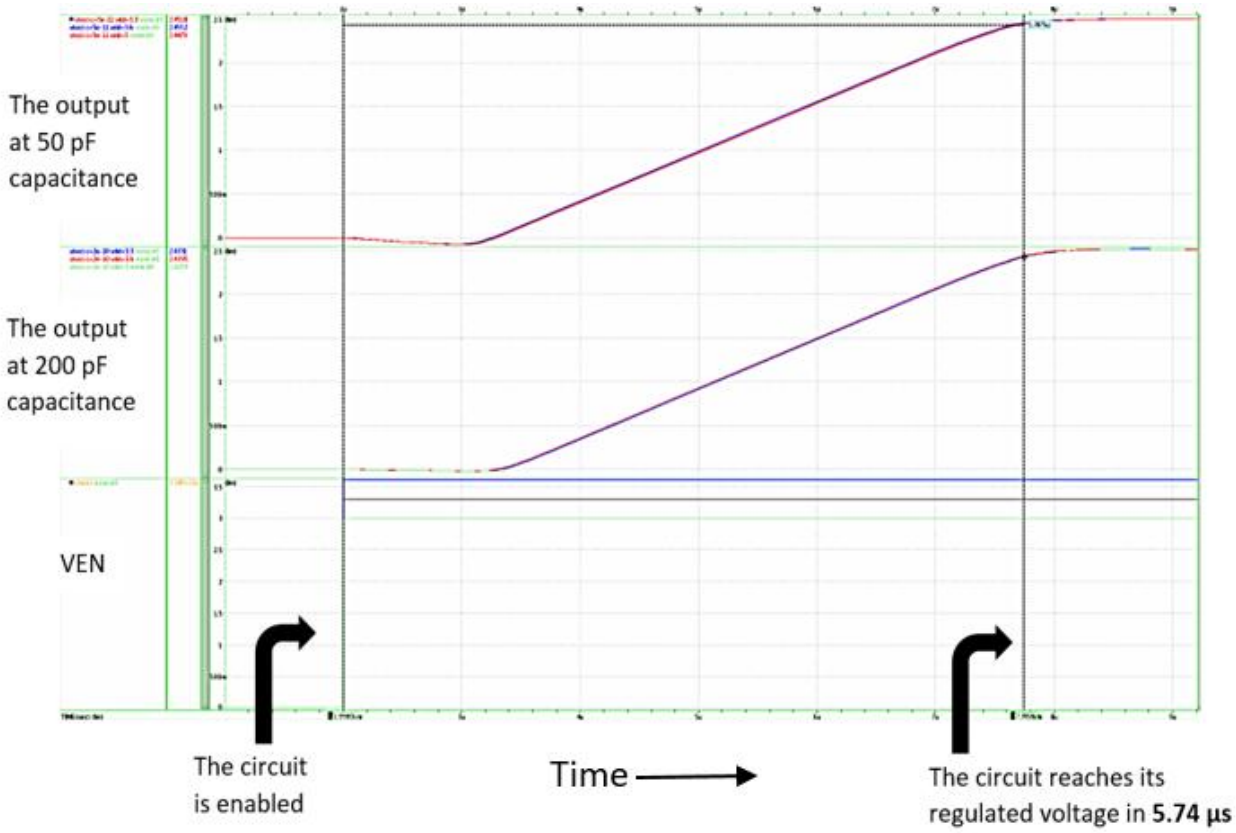

Figure 5.2: Waveform of startup time of regulator circuit without any additional techniques

S.No.	VDD (V)	Corner	Startup time at different load capacitance					
			50pF			200pF		
			Dead Time (µs)	Slew + Settling time(µs)	TOTAL TIME (µs)	Dead Time(µs)	Slew + Settling time(µs)	Total time(µs)
1	3.6	FFHVLT	1.299	4.261	5.56	1.34	4.29	5.63
2		SSLVHT	1.196	4.584	5.78	1.24	4.62	5.86
3		TTTVTT	1.29	4.36	5.65	1.34	4.4	5.74
4	3.3	FFHVLT	1.32	4.26	5.58	1.36	4.29	5.65
5		SSLVHT	1.21	4.6	5.81	1.26	4.6	5.86
6		TTTVTT	1.31	4.36	5.67	1.36	4.4	5.76
7	3	FFHVLT	1.34	4.258	5.598	1.38	4.29	5.67
8		SSLVHT	1.21	4.58	5.79	1.26	4.61	5.87
9		TTTVTT	1.33	4.36	5.69	1.38	4.4	5.78

Table 5.1: Startup time at different supply voltages and load capacitor on different corners

The startup time taken by the circuit in Figure 5.1 when enabled is shown in Figure 5.2. The results are stated in Table 5.1.

5.2 How to improve startup time?

The startup time of the linear regulator can be improved by either reducing dead time, slew time or settling time. Dead time and slew time can be reduced by increasing the tail current of the differential amplifier. Slew rate can be increased by supplying more current directly in the output stage. The settling of the regulator can be reduced by increasing bandwidth of the loop. However, this requires more current, thus more power such that the output pole is pushed out further. Since, the maximum permissible quiescent current that can be used in the circuit is limited, these linear techniques cannot be used to improve the startup time of the circuit.

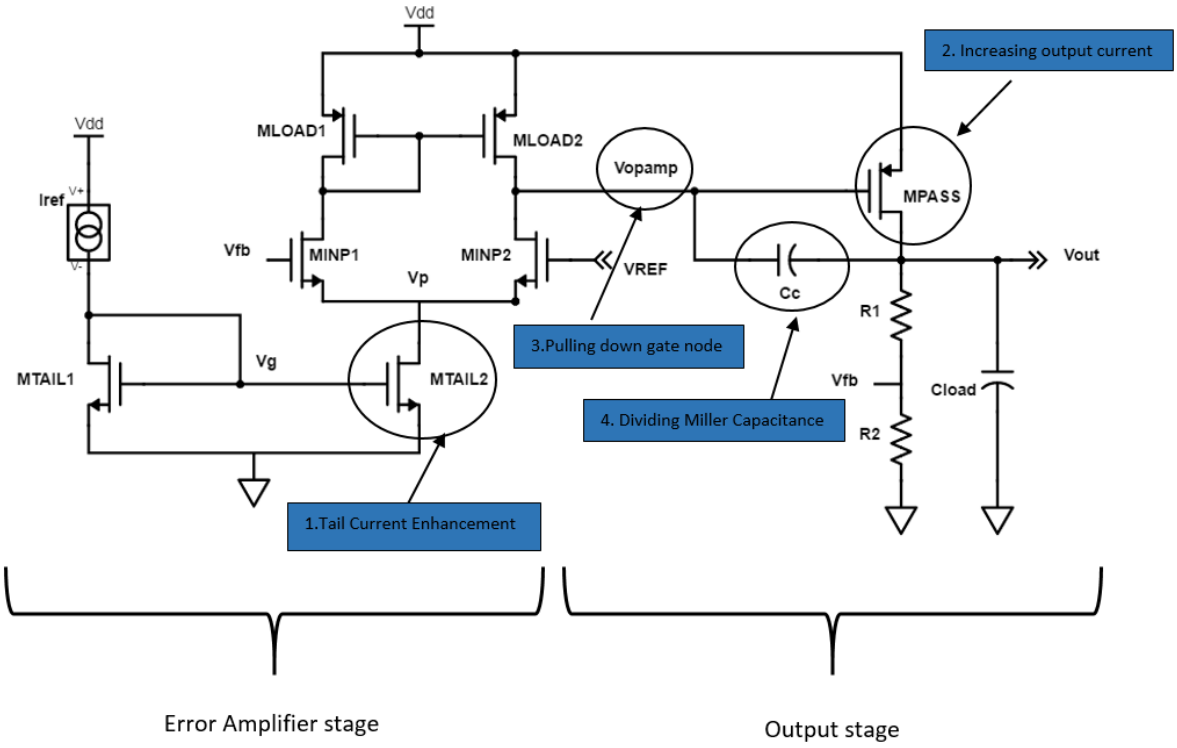

Figure 5.3: Linear regulator architecture with startup time improvement techniques

Another method to improve startup time is using a voltage buffer stage between the error amplifier and the pass transistor. This technique pushes out the pole at the gate of the pass transistor and provides extra current to charge the gate node quickly. This helps to improve the transient speed of the circuit. However, the linear regulator topology designed (Figure 5.1) is input pole dominant. Including the voltage buffer stage pushes out the input pole, degrading the phase margin and stability of the circuit.

There are various nonlinear techniques that can be used to mitigate this problem. Some of them are shown in Figure 5.3. Few of these techniques compromise on the power consumption during

startup phase of the circuit, while other compromise on the area. The optimum of all the techniques can be used to improve the startup time.

5.2.1 Tail current enhancement

From the above explanation, it becomes quite evident that if tail current is increased, both the dead time and the slew time is decreased proportionately. Thus, adding an external tail current source improves the startup time. The required tail current for overcoming the slew (Figure 5.4) is,

$$I_{TAIL} = \frac{\Delta V_{OUT} \times C_C}{\Delta t} \tag{5.5}$$

For $\Delta V_{OUT} = 2.5$, $C_C = 8$ pF, $\Delta t = 100$ ns, Required $I_{TAIL} = 200$ µA

The increased current is provided through the additional tail current circuitry as shown in Figure 5.5. An NMOS device is added with a switch in series. The gate input of the additional NMOS current source is biased with the same gate voltage (Vg) as that of the original tail current mirror circuit. The switch takes an external pulse (VTAILn) as input. The pulse is high when the tail current is on (i.e., during startup) and is otherwise low.

When the external current source is applied for 1µs, the total startup time obtained in SS corner is 665 ns, which has 130 ns of dead time, and 535 ns of slew and settling time as shown in Figure 5.6. The dead time is 20 % of the total startup time.

Technique	Dead Time	Slew + Settling Time	Startup time
Tail current enhancement	130 ns	535 ns	665 ns

Table 5.2: Startup time results for tail current enhancement circuitry at FFHVLT and 200pF of load capacitance

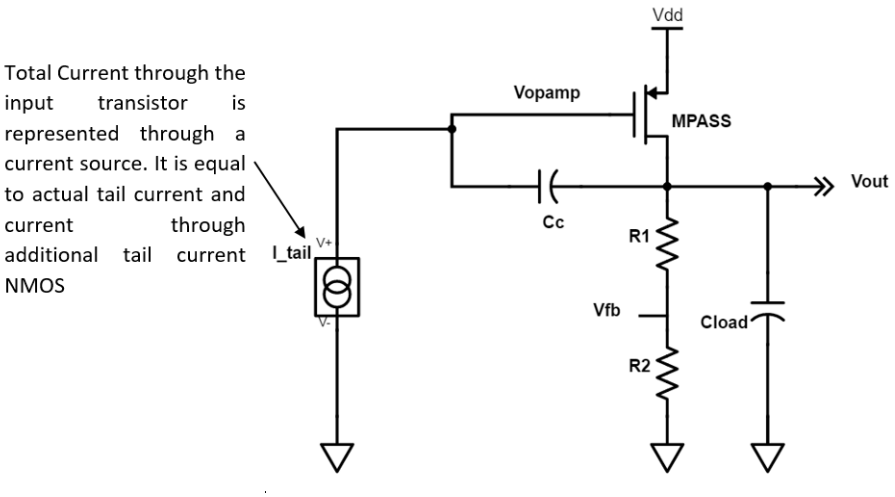

Figure 5.4: Tail current Enhancement

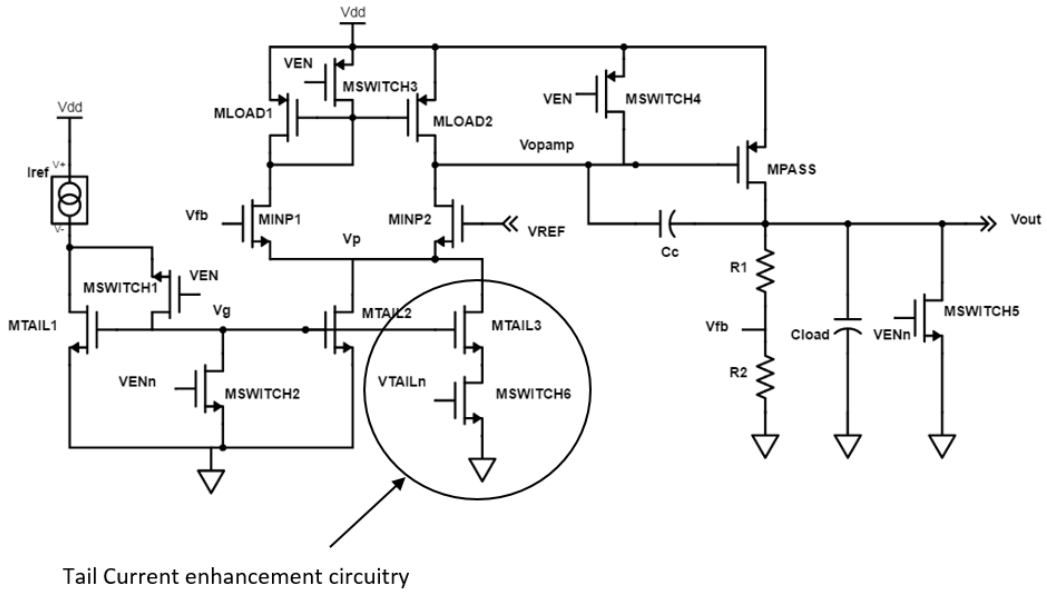

Figure 5.5: Circuitry for tail current enhancement

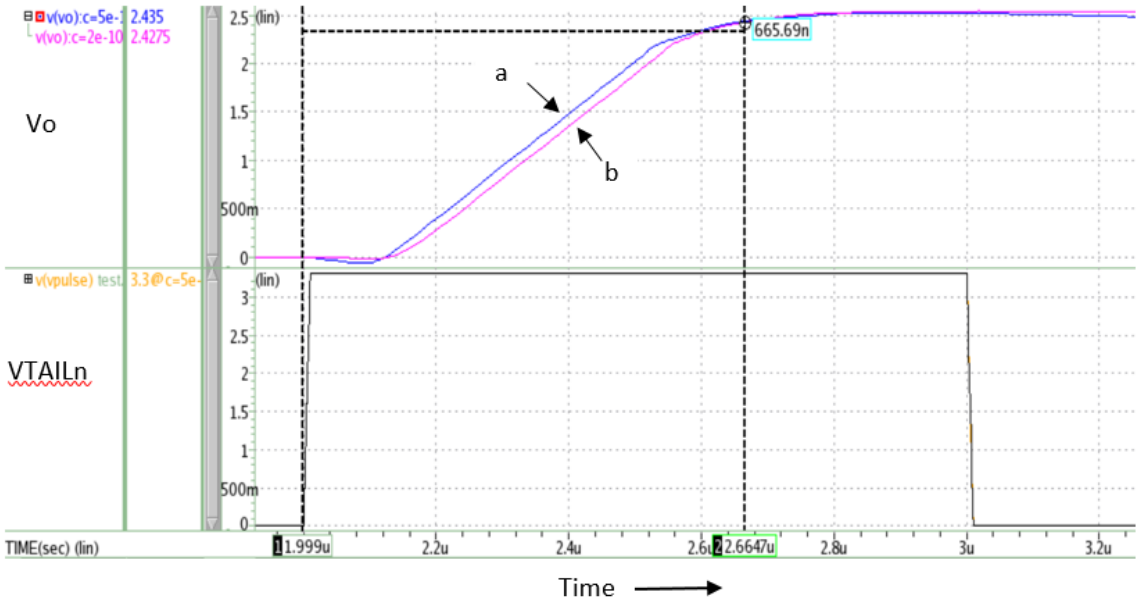

Figure 5.6: Output waveform of tail current enhancement technique, (a) 50 pF of load capacitance, (b) 200 pF load capacitance at FFHVLT

Limitation

The tail current can be increased only till a certain limit. As the tail current is increased the source follower nature of the differential input transistor pushes its source node to even lower level (as

input is fixed), forcing the tail current source to operate in linear region. Thus, current strength is restricted.

5.2.2 Output current enhancement

The slewing can be improved further by directly adding extra current in the output stage of the linear regulator (Figure 5.7). The current will be divided between the output capacitor and the resistor (no current can go into the compensation capacitor as 5 µA fixed current source is attached to its other end as shown in Figure 5.4). Thus, the output capacitor will be charged according to the current coming from the external current source,

$$\frac{\Delta V_O}{\Delta t} = \frac{I_{C\_LOAD}}{C_{LOAD}}. \tag{5.6}$$

For $\Delta V_{OUT} = 2.5$, $C_{LOAD} = 200$ pF, $\Delta t = 100$ ns, Required $I_{C\_LOAD} = 5$ mA. The sizing of the current source is done accordingly.

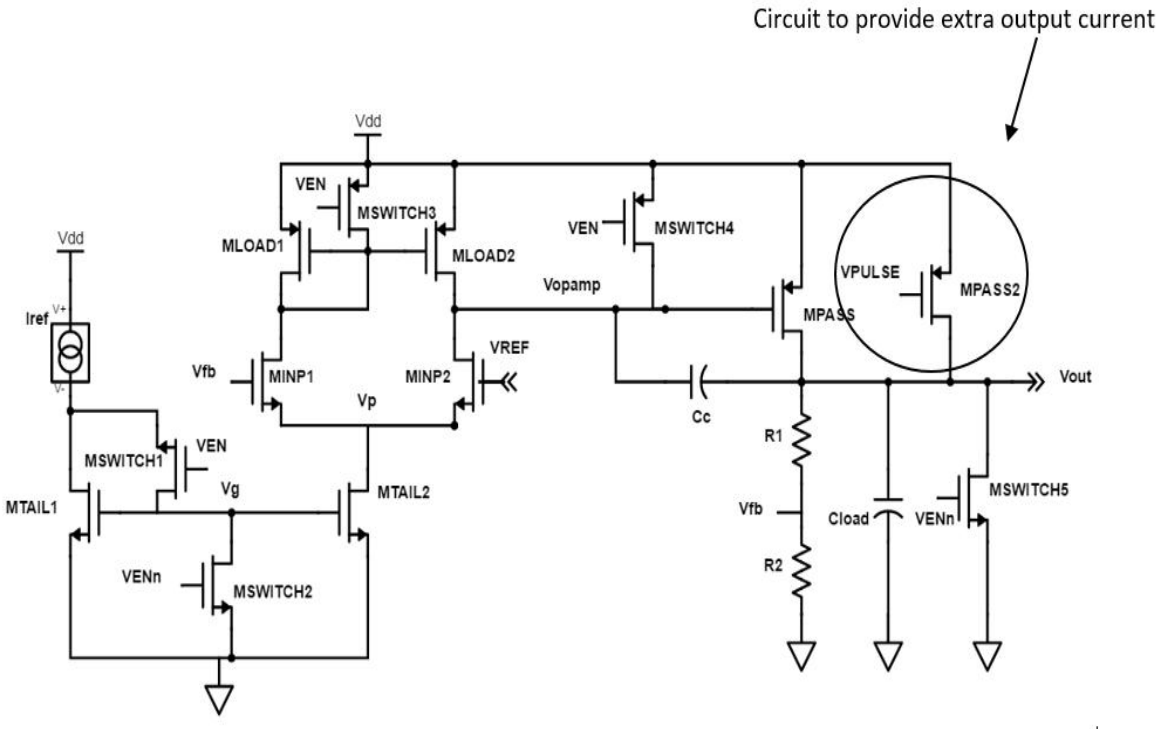

Figure 5.7: Regulator circuit with output current enhancement

The dead time of the circuit is reduced to zero. The total startup time is reduced to 4µs as shown in Figure 5.8.

Limitation

When the output current is increased, the gate node of the pass transistor also rises due to capacitive coupling (Figure 5.8). Once the external output current source is removed during the normal

operation, the gate node has to decrease from a higher voltage to its steady state value to support operating current through the PMOS, resulting in delayed overall startup. Moreover, it is not appropriate to apply nonlinear techniques directly at the final output node because the effect of error will be straightaway reflected at the output in contrast to the nonlinear techniques applied on the internal nodes, for which the error is suppressed by the gain as well as feedback.

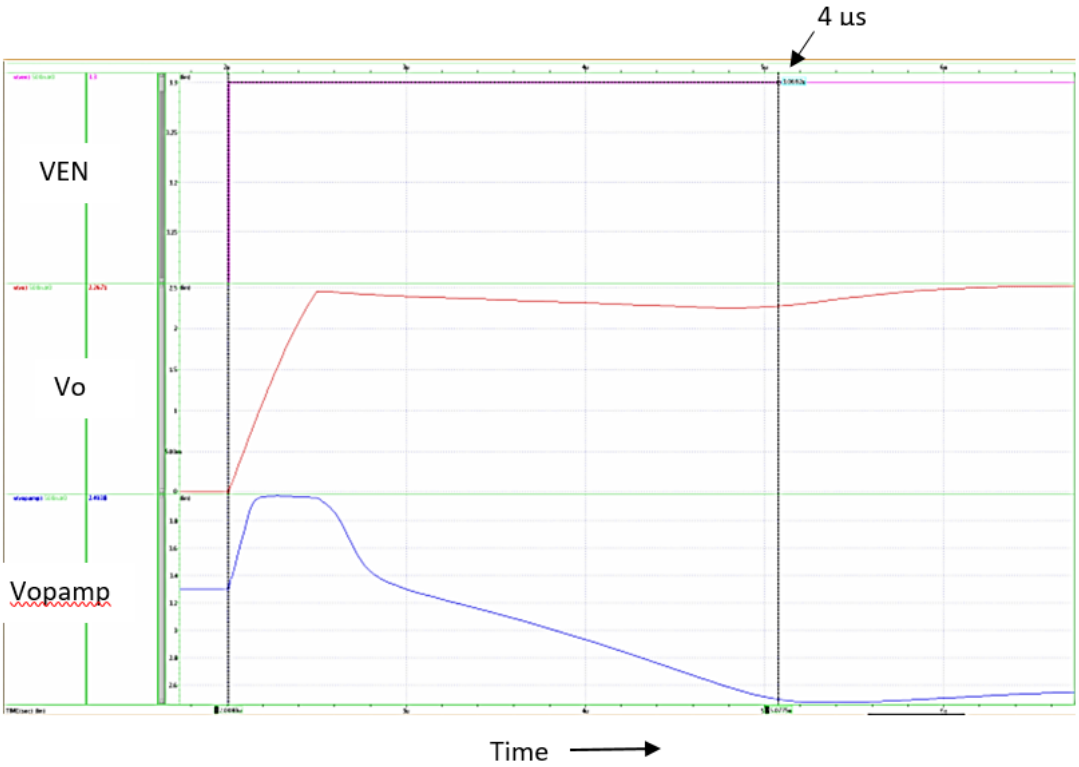

Figure 5.8 Waveform for output current enhancement technique at FFHVLT and 200 pF load capacitor

Technique	Corner	Dead Time	Slew + Settling Time	Startup time
Load current enhancement	FFHVLT	0 s	4 µs	4 µs
	SSLVHT	0 s	9 µs	9 µs

Table 5.3: Startup time results for load current enhancement circuitry at 200 pF load capacitance

5.2.3 Pulling down the gate node of pass transistor

To improve the startup time, the rate of decrease of gate node is increased by pulling it down through an external pull down circuit as shown in Figure 5.9. This reduces the dead time of the regulator. Moreover, the current required by the output capacitor to charge up to the regulated supply voltage can be calculated and the gate node can be pulled down further to provide that current. This will charge the output node faster eventually reducing the startup time.

From equation 5.6, I_{OUT} = 5mA is required to reduce the slewing time of the output to 100ns. From the current equation of the transistor in saturation,

$$I_{OUT} = \frac{1}{2}\,\mu_p C_{OX}\frac{W}{L}\,(V_{sg} - |V_t|)^2 \qquad (5.7)$$

The gate node must reach value, V_g (V_{OPAMP}) = 2V such that output stage can provide this much current. So, Change in the gate voltage, ΔV_{OPAMP} = 3.3-2 = 1.3V
If gate node take 10ns time to discharge up to 2 V

- ⇨ Required current at gate node, $I_{VOPAMP} = \frac{\Delta V_{OPAMP} \times C_C}{\Delta t}$ = 1.04 mA
- ⇨ The W/L ratio of the pull down NMOS transistor is nearly equal to 2

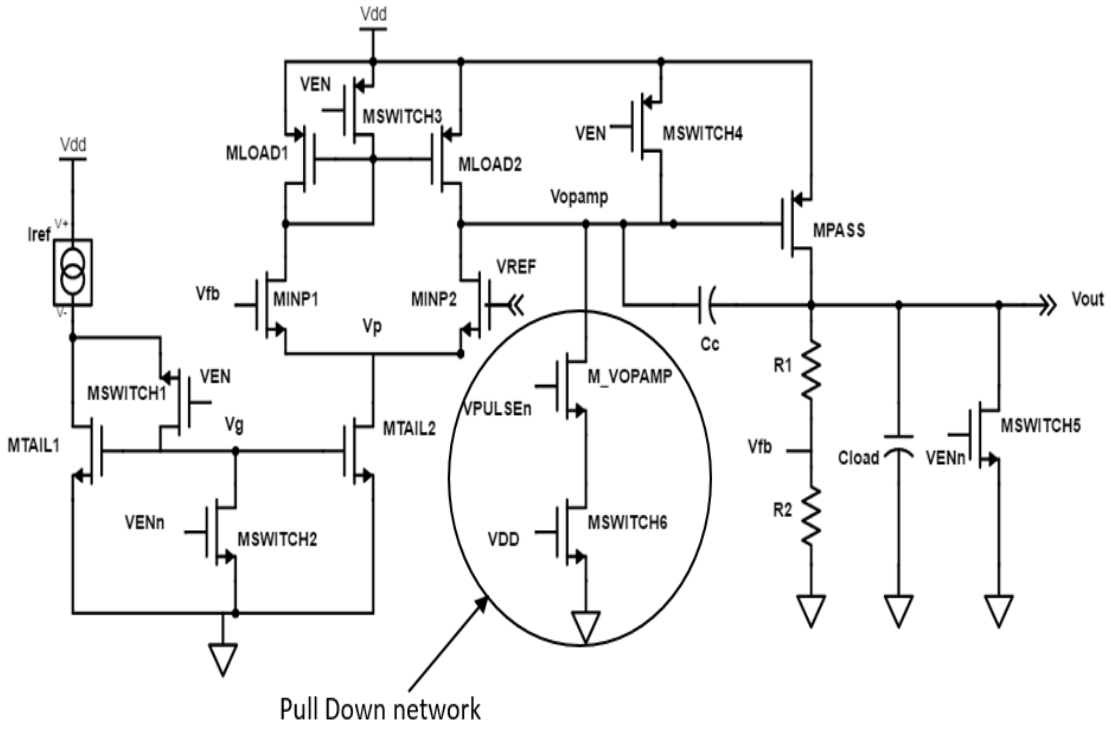

Figure 5.9: Regulator circuit with pull down path at gate node of the pass transistor

Technique	Corner	Dead Time	Slew + Settling Time	Startup time
Load current enhancement	FFHVLT	12 ns	1.32 µs	1.334 µs
	SSLVHT	41 ns	3.81 µs	3.9 µs

Table 5.4: Startup time results for load current enhancement circuitry at 200 pF load capacitance

Limitation

Even when the pull-down path is removed, current will continue to come through the compensation capacitor till the gate node remains at low voltage. Since, the pull-down path is not present, this current will charge the gate of the pass transistor to a higher voltage resulting in overshoot. Eventually, more time is taken to pull down the gate node to final steady state value.

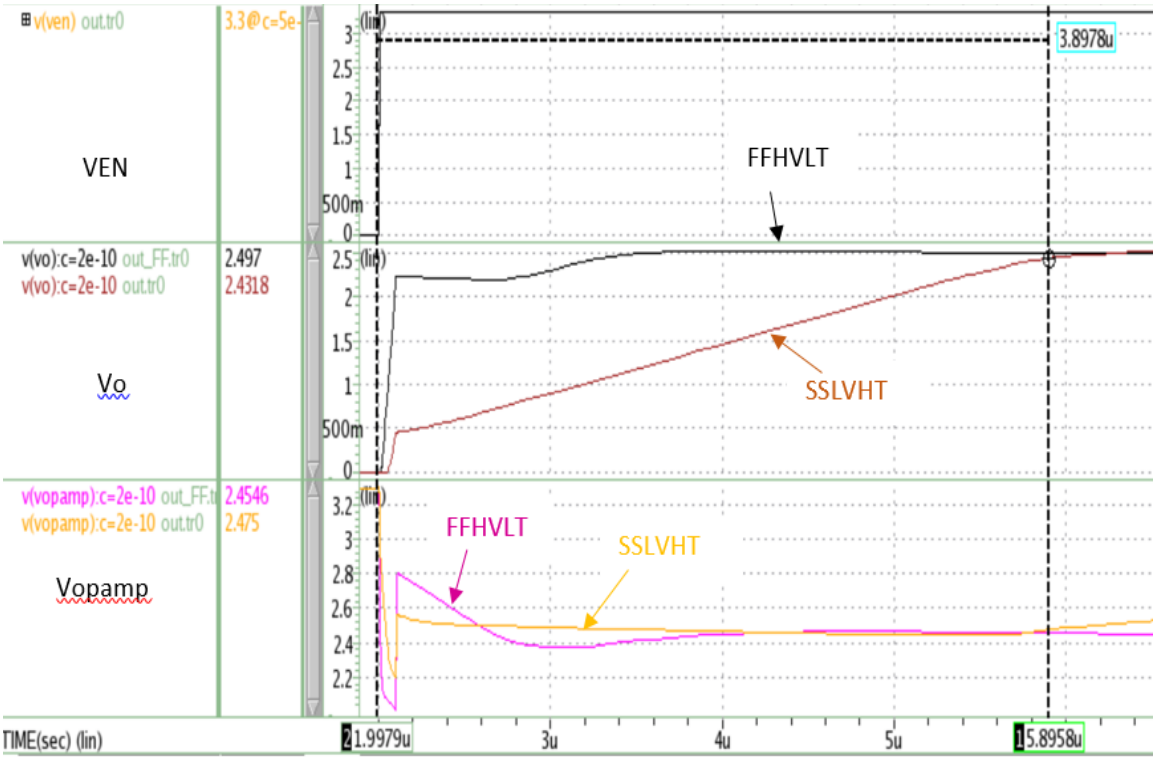

Figure 5.10: Waveform for technique with pull down path at gate node of pass transistor 200 pF load capacitor

5.2.4 Capacitor Divider Miller Network

The slewing of both, the Vopamp node (dead time) as well as the output node (slew time) is inversely proportional to the compensation capacitor. If the Miller capacitor is reduced during dead zone and slewing, then the total startup time can be decreased. Compensation cap can be connected later using a switch which will result in a sudden drop in the gate voltage due to charge distribution. As the gate node will dip, the current in pass transistor will increase, charging the output stage faster. The gate node will recover with rising output voltage due to negative feedback of the circuit.

Limitation

The gate node will droop according to the capacitor divider ratio. The more the gate node drops, larger will be the amount of current flowing through the output pass transistor. Since the compensation capacitor is about 10 times the C_{gd} of the pass gate, if the entire compensation capacitance is removed and then reconnect it then the droop at the gate terminal will be more. This will increase the rate of rise of the output voltage resulting in overshoot in the output. Therefore, instead of removing the entire Miller capacitor, during the dead time smaller value of compensation capacitor is connected in the circuit. After that, entire compensation capacitor is connected. The capacitor divider ratio must be properly chosen for fast slewing and avoiding overshoot. Once this fast settling due to charge distribution settles the further slew is overtaken by I_{TAIL} and total compensation cap as given in equation 5.2.

5.3 Final Implementation

5.3.1 Startup time analysis using ideal delay pulse

S.No.	VDD	Corner	Startup time at different load capacitance					
			50pF			200pF		
			Dead Time (ns)	Slew + Settling time (ns)	TOTAL TIME (ns)	Dead Time (ns)	Slew + Settling time (ns)	Total time (ns)
1	3.6	FFHVLT	51	205.67	256.67	51.03	286.58	337.61
2		SSLVHT	51.07	92.32	143.39	51.11	209.22	260.33
3		TTTVTT	51.1	181.52	232.62	51.1	282.6	333.7
4	3.3	FFHVLT	51.2	695.42	746.62	51.15	766.19	817.34
5		SSLVHT	51.23	724.69	775.92	51.27	724.63	775.9
6		TTTVTT	51.29	695.16	746.45	51.25	779.26	830.51
7	3	FFHVLT	51.36	1155.26	1206.62	51.45	1225.45	1276.9
8		SSLVHT	51.5	1159.29	1210.79	51.41	1240.19	1291.6
9		TTTVTT	51.51	1167.77	1219.28	51.51	1250.17	1301.68

Table 5.5: Startup time with capacitor divider technique at different supply voltages and load capacitor on different corners

S.No.	VDD	Corner	Startup time at different load capacitance					
			50pF			200pF		
			Dead Time (ns)	Slew + Settling time(n)	TOTAL TIME (n)	Dead Time (n)	Slew + Settling time (ns)	Total time (ns)
1	3.6	FFHVLT	28.93	52.65	81.58	28.93	125.97	154.9
2		SSLVHT	50.78	53.66	104.44	50.78	146.37	197.15
3		TTTVTT	44.8	74.96	119.76	45.98	165.36	211.34
4	3.3	FFHVLT	29.57	481.73	511.3	29.75	588.15	617.9
5		SSLVHT	50.92	516.71	567.63	50.94	623.8	674.74
6		TTTVTT	48.03	567	615.03	49.37	649.21	698.58
7	3	FFHVLT	30.75	961.75	992.5	31.15	1059.62	1090.77
8		SSLVHT	51.12	1071.58	1122.7	51.16	1150.55	1201.71
9		TTTVTT	50.63	1046.47	1097.1	50.69	1125.11	1175.8

Table 5.6: Results of startup time at different supply voltages, corners and load capacitance of 50pF and 200pF for capacitor divider network + tail current enhancement using ideal delay pulse

The total compensation capacitor of 8pF is divided into two in ratio 1:7. Initially, 1pF capacitor is connected to the regulator. After the dead zone, remaining 7pF is connected in the circuit. Thus, improving the startup time significantly. The results are stated in Table 5.5. The worst startup time is of 1.3µs in case of typical corner and lowest supply voltage (3 V). The best startup time of 232 ns is obtained at the highest voltage.

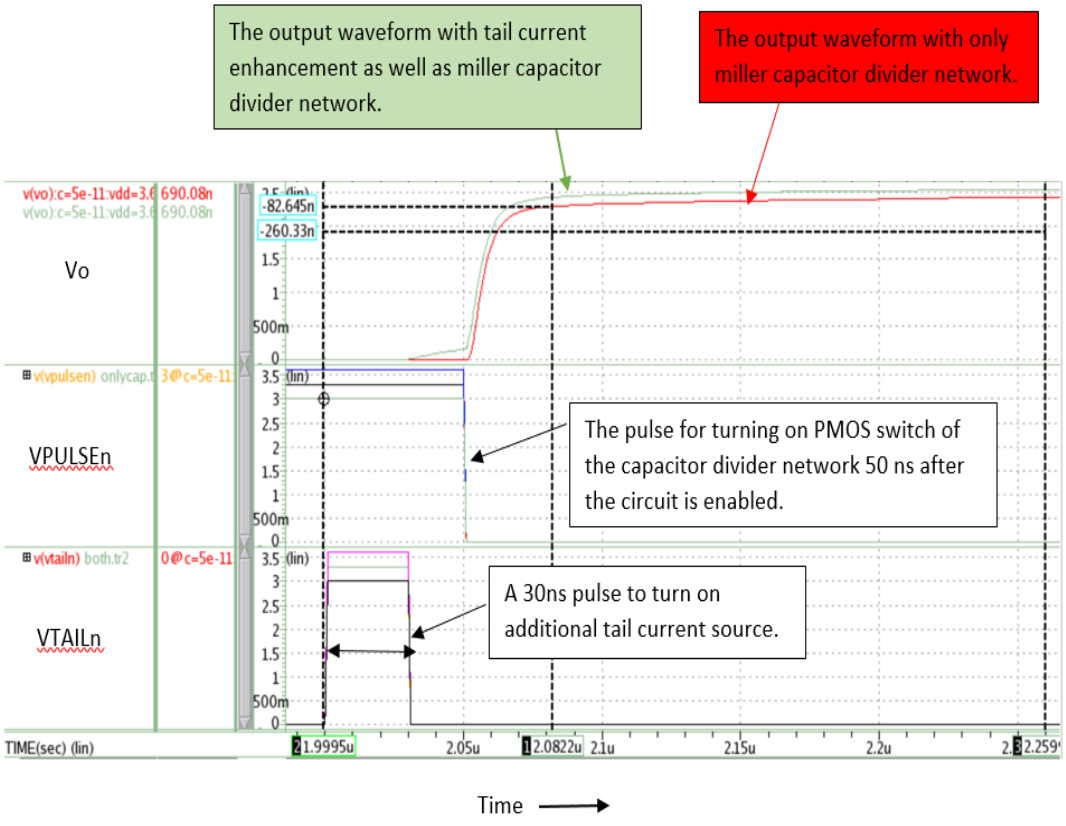

Figure 5.11: Comparison of the output waveform of two techniques at FFHVLT and 50 pF load capacitance – (a) Only Miller divider network and (b) Miller divider network + tail current enhancement

If the tail current is also enhanced during the dead time then the startup time further improves. As the circuit is enabled, the external tail current circuitry is also turned on for 30 ns which provides current of 20 µA. It reduces the regulator dead band to 30ns. After that, for 20 ns the output voltage slews through the compensation capacitor (C_{c1}) by the tail current of 5 µA. Then, capacitor divider network is turned on. Now, the output voltage reaches its final value faster as the initial value of output voltage is greater than 0V (Figure 5.11). The results of startup time with the capacitor divider network as well as tail current enhancement are given in Table 5.6.

5.3.2 Startup time analysis using an external delay circuitry

A control is required to operate the switches that enable the capacitor divider network and tail current control. A delayed enable pulse can be used to operate these switches. This delay circuit is discussed below.

Delay Circuit

The delay introduced by a single inverter is approximately equal to 30-40ps. If delay of around 30-50ns is required, a long chain of inverter needs to be used. To avoid this, the transition period of an inverter is increased by starving the charging or discharging current and increasing the load (output) capacitance (Figure 5.13). Since a pulse with high to low transition is needed, the time

period is increased only during discharging by limiting the current in discharging path. When the output of this inverter is fed to another transistor, the overall delay is increased. To minimize the transition between high to low pulse, skewed inverter is used as the last inverter stage of the circuit.

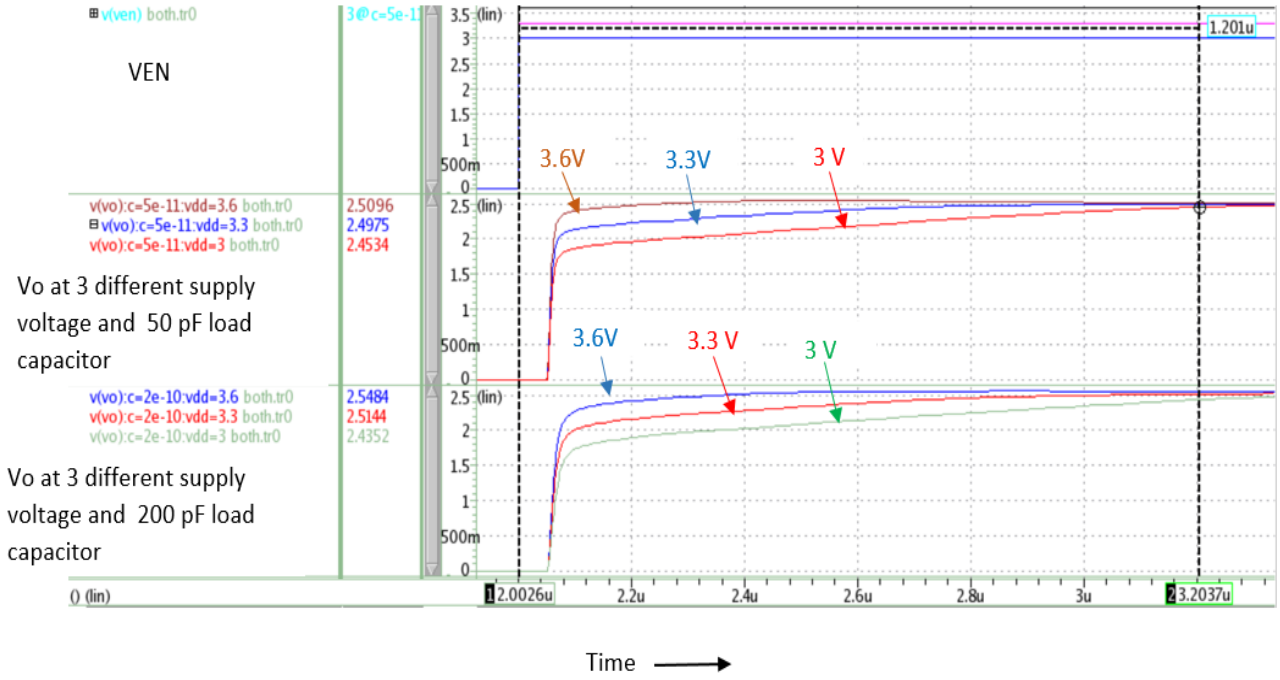

Figure 5.12: Output results at TTVTTT for tail current enhancement + capacitor divider network technique using ideal delay pulse

S.No.	VDD	Corner	Startup time at different load capacitance					
			50pF			200pF		
			Dead Time (n)	Slew + Settling time(n)	TOTAL TIME (n)	Dead Time(n)	Slew + Settling time(n)	Total time(n)
1	3.6	FFHVLT	25.52	41.83	67.35	25.79	86.63	112.42
2		SSLVHT	29.65	64.86	94.51	29.66	169.52	199.18
3		TTTVTT	30.88	95.43	126.31	30.91	194.69	225.6
4	3.3	FFHVLT	30.38	565.69	596.07	30.49	635.52	666.01
5		SSLVHT	24.65	575.62	600.27	24.65	684.11	708.76
6		TTTVTT	23.64	635.9	659.54	23.65	721.31	744.96
7	3	FFHVLT	21.15	1075.88	1097.03	21.1	1147	1168.1
8		SSLVHT	21.66	1131.46	1153.12	21.67	1214.13	1235.8
9		TTTVTT	19.45	1127.8	1147.25	19.45	1212.35	1231.8

Table 5.7: Results of startup time at different supply voltages, corners and load capacitance of 50pF and 200pF for capacitor divider network + tail current enhancement using external delay circuit

The results obtained after using the delay circuit are stated in the Table 5.7. The waveforms of the result at different corners and supply voltage with the delay circuit is shown in Figure 5.14 .The

best startup time is 67 ns at 3.6 V supply and the fast corner at 50 pF load capacitance. The worst startup time is of 1.235 µs at 3V supply and slow corner and 200 pF or load capacitance.

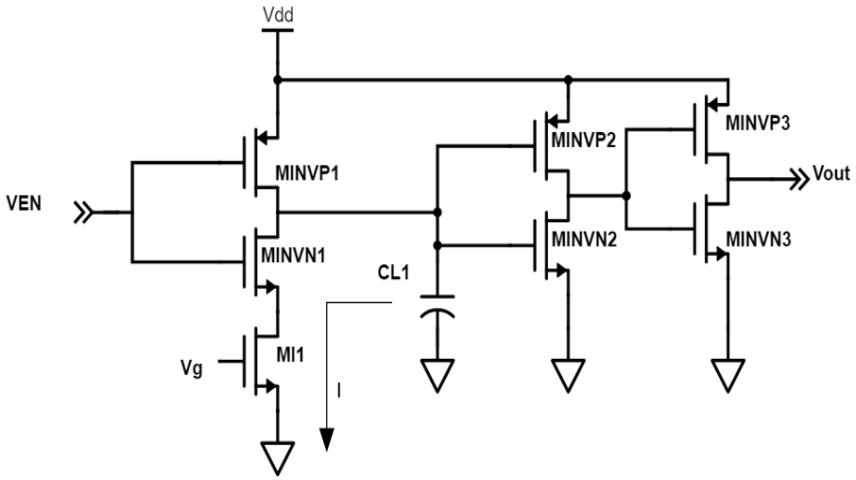

Figure 5.13: Delay circuit with current starved inverter

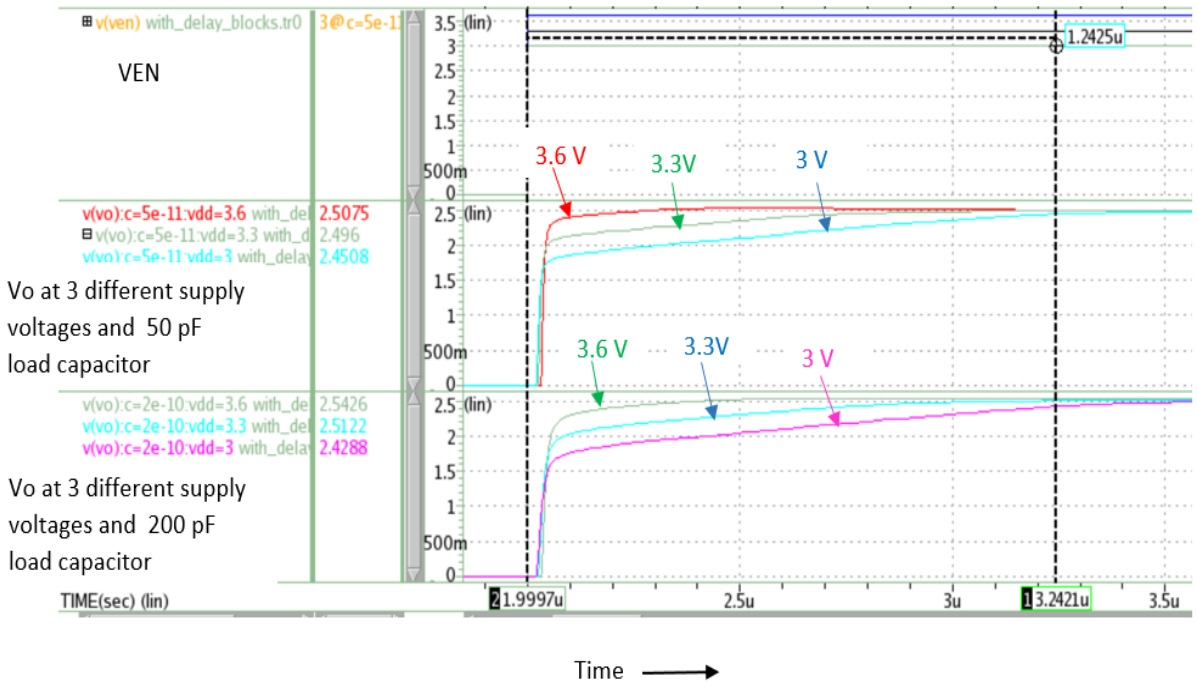

Figure 5.14: The output results at TTVTTT for tail current enhancement + capacitor divider network using external delay circuit

5.4 Reason for vast variation of startup time across supply voltage

Since the value of source to drain voltage (V_{SD}) is different for different supply voltages, the pass transistor current is different for both. The higher the supply voltage, higher is the pass transistor current. This leads to different charging time of the output voltage in the case of different supply voltages. Thus, slew time is lesser for larger supply (3.6 V) and higher for smaller supply voltage (3.3 V) (Figure 5.15).

This results in decrease in the overall startup time at high voltage supply.

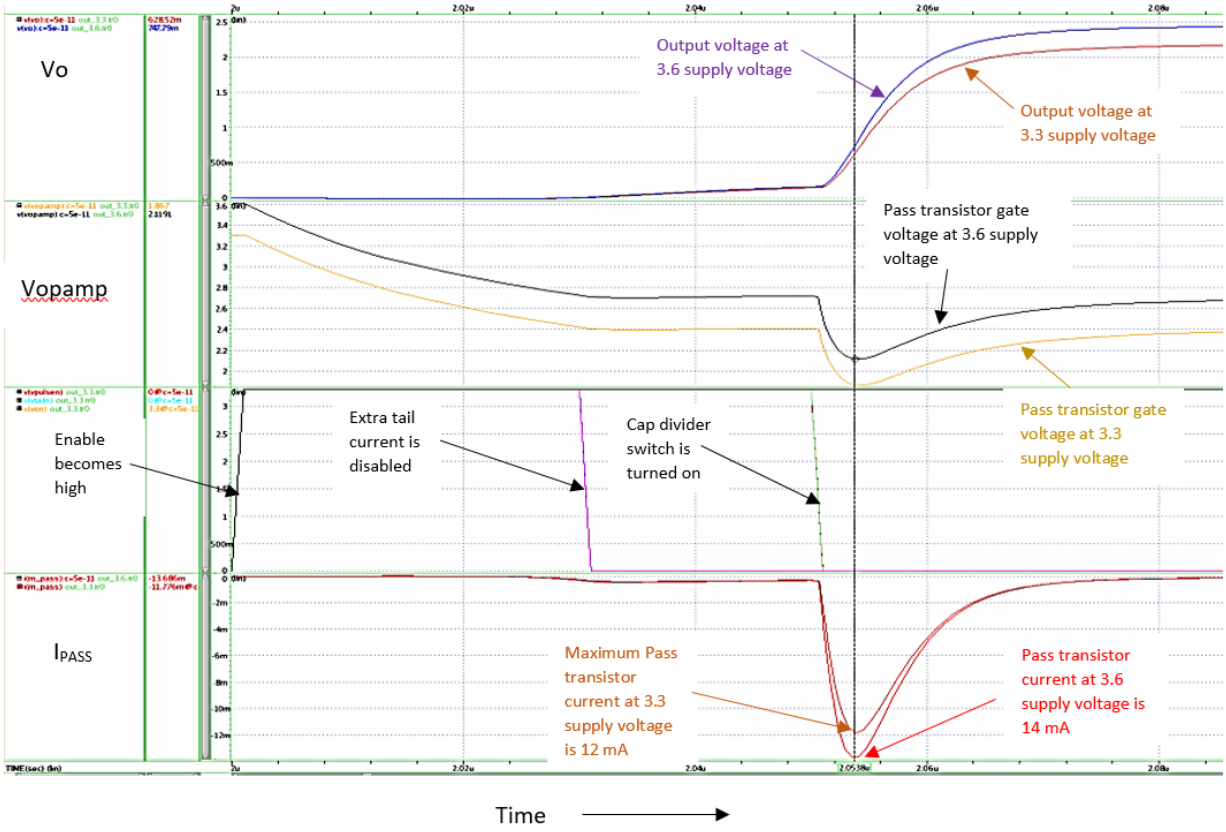

Figure 5.15 Waveform showing comparison of output waveform at supply voltages 3.6V and 3.3.V

Chapter 6 **Conclusion and Future Work**

In this thesis, general MOS characteristics are outlined. The basic building blocks of linear regulator are also discussed. A linear regulator with 2.5V supply at 3.3V input voltage is designed. The startup time of the conventional regulator at TTTVTT and 3.3 supply voltage is 5.67 µs for 50pF load and 5.76 µs for 200pF load with dead time consuming 20% of the total startup time.

Various design techniques are compared and been analyzed to decrease the startup time of the regulator such as tail current enhancement, load current enhancement, and fast gate node discharge circuit. A novel capacitor divider architecture has been introduced to reduce the startup time of the conventional regulator structure. This technique shows significant improvement without consumi9ng any additional power. At TTTVTT and 3.3V supply voltage, the startup time is reduced to 747ns and 830ns for load capacitance of 50pF and 200pF respectively. For 3.6 supply voltage, at TTTVTT, the startup time is reduced to 232ns and 333ns for load capacitor of 50pF and 200pF respectively. If tail enhancement is also given along with the capacitor divider topology, then the startup time further improves by 100ns.

The penalty of using Miller compensation is poor high frequency PSRR of the system. It creates a direct path between supply voltage and output at high frequency because of which the fluctuations in the input are straightaway visible at the output. Since this is a first step towards regulator design, many techniques can be used in future to improve the PSRR of the circuit. Using higher pole cancellation resistance in the Miller path or using current buffer type Miller compensation improves the PSRR. Making regulator output pole dominant also enhances PSRR as it leads to high RC filtering at the output. Using folded cascode configuration in the error amplifier stage improves the gain of that stage. It also helps in improving the PSRR. Moreover, a comparator can be used to control the switches used instead of a delayed pulse. The tail current enhancement can be given after the capacitor divider network settles to enhance second slewing.

Appendix

A. Variation of gain of MOSFET with drain to source voltage

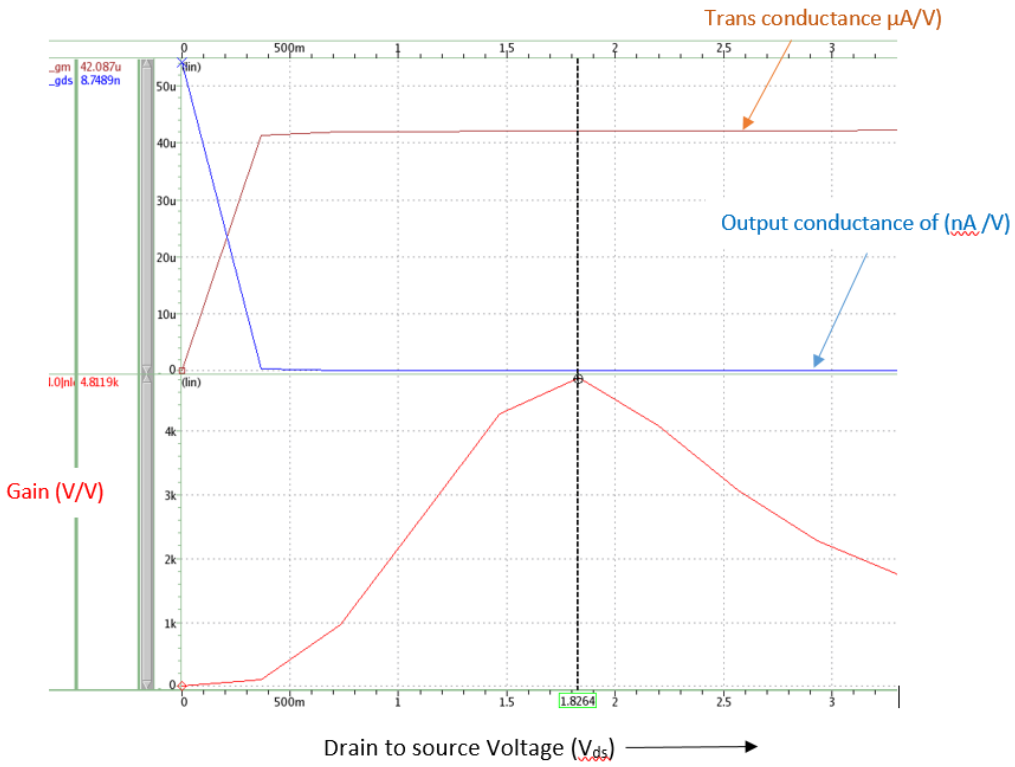

Figure 0.1: Curve showing variation of transconductance, output conductance and gain with drain to source voltage

If g_m is the transconductance of the MOS and g_{ds} is the output conductance, then, gain of the MOS transistor is,

$$Av = \frac{g_m}{g_{ds}} \tag{1}$$

In triode region,

$$g_m = \mu_n C_{OX} \frac{W}{L} V_{ds} \tag{2}$$

⇨ g_m increases linearly with V_{ds}

$$g_{ds} = \mu_n C_{OX} \frac{W}{L} \left(V_{gs} - |V_t| - V_{ds}\right) \tag{3}$$

⇨ g_{ds} decreases linearly as V_{ds} increase

⇨ Gain increases with V_{ds} increase

In saturation region,

$$g_m = \mu_n C_{OX} \frac{W}{L} \left(V_{gs} - |V_t|\right)(1 + \lambda V_{ds}) \quad (4)$$

⇨ g_m increases as V_{ds} increase

$$g_{ds} = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} \left(V_{sg} - |V_t|\right)^2 \lambda \quad (5)$$

⇨ g_{ds} must remain constant with V_{ds}

However, as V_{ds} increases ΔL increases, resulting in rate of increase of depletion region around source. Thus, r_o increases incrementally or g_{ds} decreases incrementally [5]. When V_{ds} further increases, due to Drain Induced Barrier Lowering (DIBL), threshold voltage decreases increasing the current through the MOS and decreasing output resistance. But the output resistance becomes constant nullifying previous effect. So, g_{ds} also becomes constant. When V_{ds} further increases, current through MOS further increases due to Impact Ionization, decreasing r_o i.e. increasing g_{ds}. This states that the maximum gain that can be obtained after increasing the output resistance of the MOS device is limited.

⇨ The gain first increase in saturation region then decreases (Figure 0.1).

B. Comparison of cascode and folded cascode amplifier

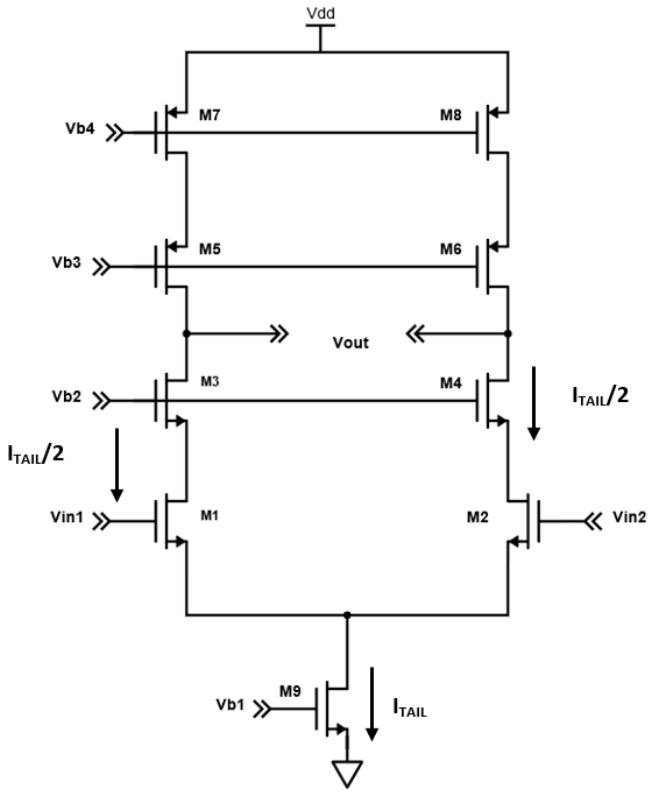

Figure 0.2: Cascode amplifier

Cascode and Folded cascode differential amplifier can be used to meet high gain requirement. The output resistance of both the devices is higher than the five-transistor differential amplifier. This increases the gain of these configurations.

S.No.	Property	Cascode	Folded Cascode	Conclusion
1.	ICMR-	$V_{OD9} + V_{OD1} + V_{t1}$	$V_{OD11} + V_{OD1} + V_{t1}$	ICMR- remains the same
2.	ICMR+	$VDD - V_{OD3} - V_{OD5} - V_{OD7}$	$VDD - V_{OD5}$ (top transistor which provides current in both the branches)	The ICMR+ of the cascode is much lesser than folded cascode
3.	Output resistance (R_{OUT})	$\approx g_{m6} r_{o6} r_{o8}$	$\approx g_{m4} r_{o4} (r_{o6} \| r_{o2})$	Output resistance of both the transistors id same
4.	Gain	$\approx g_{m1} g_{m6} r_{o6} r_{o8}$	$\approx g_{m1} g_{m4} r_{o4} (r_{o6} \| r_{o2}$	Gain of cascode amplifier is twice of that of folded cascode because the transconductance of input transistor of cascode amplifier is twice
5.	3db pole	$1/ R_{OUT} C_{OUT}$	$1/ R_{OUT} C_{OUT}$	3db pole of both the transistor are at same locations if C_{OUT} is equal for both.
6.	Unity Gain Bandwidth (UGB)	g_{m1} / C_{OUT}	g_{m1} / C_{OUT}	Since the transconductance of input transistor of cascode is twice of that of folded cascode, UGB of folded cascode is half of the cascode amplifier.

Table 0.1: Comparison of different parameters of cascode and folded cascode configuration

For the comparison between the cascode and folded cascode differential amplifier, the total power consumption is assumed to be equal, i.e. current is assumed to be same in both the configurations. The operating points at all the locations is also same (the sizes of both the devices are varied to ensure similar operating point). The input pair is NMOS transistor for both the configurations. It is known that the output resistance of a MOS transistor is inversely proportional to the current through it and the transconductance is directly proportional to the current for constant overdrive.

The comparison is present in the Table 0.1.

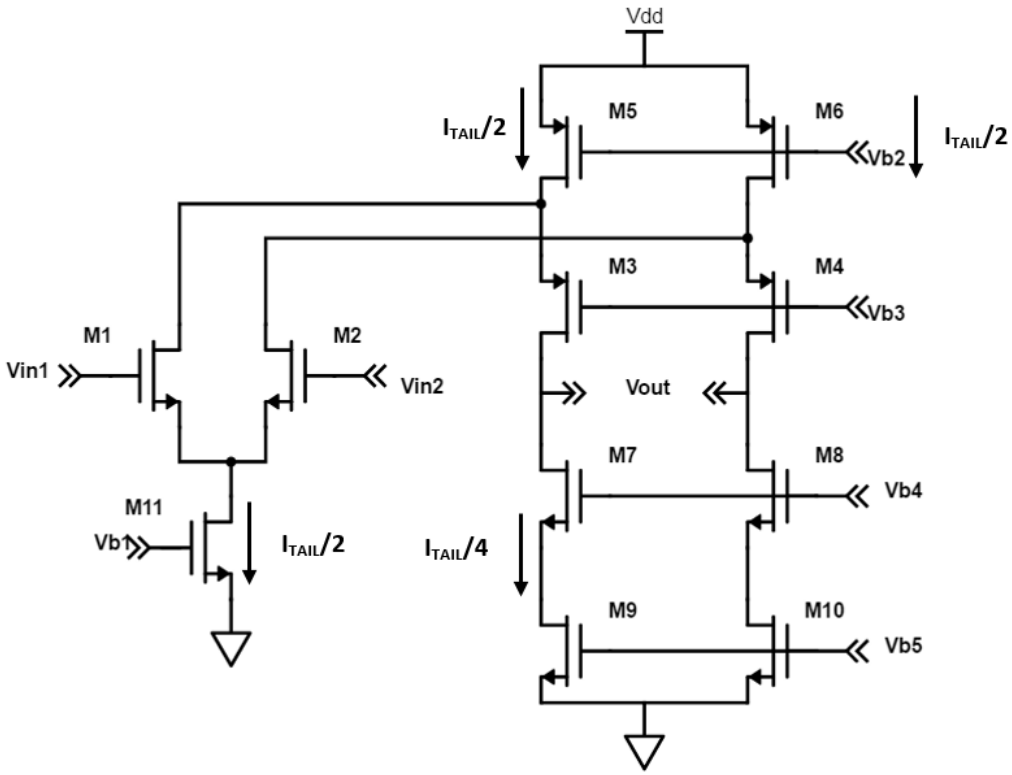

Figure 0.3: Folded cascode amplifier

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