Impact And Detection Of Partial Resistive Defects and Bias Temperature Instability on SRAM Decoder

Shivendra Singh

Indraprastha Institute of Information Technology

New Delhi

Guide

Dr. Anuj Grover

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Certificate

This is to certify that the thesis titled **"Impact And Detection Of Partial Resistive Defects and BTI on SRAM Decoder."** submitted by **Shivendra Singh** for the partial fulfillment of the requirements for the degree of *Master of Technology* in *VLSI & Embedded Systems* is a record of the bonafide work carried out by him under my guidance and supervision in the Security and Privacy group at Indraprastha Institute of Information Technology, Delhi. This work has not been submitted anywhere else for the reward of any other degree.

Dr. Anuj Grover
Department of Electronics and Communication Engineering
Indraprastha Institute of Information Technology
New Delhi, 110020

Abstract

As technology advances,semiconductor devices are becoming less predictable. This means device failure rate increases as we move down to lower technology nodes. According to ITRS roadmap upto 80% of SOC (Silicon On Chip) area would be occupied by embedded SRAMs (eSRAM) in the next few years. These SRAM units are high density devices and is more susceptible to defects compared to other logic blocks. Along with defects, these SRAM units also suffer from reliability issues like aging impact. There are several computer applications which require extremely high level of reliability of computing system like in Automotive Industry. It is therefore becoming a growing need to detect as well as to find the impact of these defects and reliability issue on SRAM units.

In this work, we analyze the impact of these Partial resistive defects on Static Random Access Memory(SRAM) address decoders side which is the leading cause of small delays in Wordline activation or deactivation; these are hard to detect and may result in escapes and reliability problems. Here we investigate the impact of BTI as well as resistive defects at a different location in address decoders. This work also contains the combined effect of both BTI and resistive errors on the decoders. This thesis work also suggests the test mode design for its detection mechanism for these defects. In this test mode, I have shown that the proposed detection mechanism should able to detect the error resistance more than 5K ohm.

Acknowledgments

First and foremost, I would like to express my special gratitude to my research advisor Dr. Anuj Grover for providing excellent guidance and encouragement throughout the journey of this work. This thesis would have been impossible without his knowledge, guidance, and feedback

This work is dedicated to my parents. I am very grateful to my Mother and Father for giving full support and having faith in me.

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Chapter 1

Introduction

1.1 Motivation

The semiconductor industry has advanced significantly over the decades, and it has integrated systems onto single chips that enable various portable device and IoT application, which makes our life more comfortable.

Memories are one of the essential building blocks in such highly integrated circuits. Memory density will continue to grow over the next years, according to Moore's Law. This is confirmed by the SIA (Semiconductor Industry Associations) Roadmap, which forecasts a memory density approaching 94 % of System on Chip (SoC) silicon area in the next ten years [SIA05]. Moreover, the memory will continue to be used as a process development vehicle for new digital technologies. Therefore, memories are becoming the main contributor to the overall SoC yield loss. Critical systems (like for Automotive Industry) must contain highly reliable semiconductor memories. The faults in memories result in yield loss. In critical systems, these may cause a system's catastrophic failure. As we are going towards lower technology nodes, the chance of having faults in memories get increases due to the increase in process variation as well as reliability issues. Consequently, efficient detection mechanism, as well as repair schemes, are needed for memories to achieve high yield value for SOC.

These memories suffer from variability and reliability issues. Variability in the shrunk interconnects leads to resistive/open defects. Moreover, the presence of resistive-open defects is becoming more and more critical due to the ever-growing number of interconnections between the layers. Reliability failure mechanisms, such as BTI (Negative Bias Temperature Instability (NBTI) in PMOS transistors, and Positive Bias Temperature Instability (PBTI) in NMOS transistors), degrade transistors performance during the operational lifetime.

1.2 Basic Of SRAM

A simplest SRAM array architecture is shown in Figure 1.1. It consists of memory cells, bitline conditioning (pre-charge circuit), row decoder, column decoder and column circuitry. Row decoder decodes the row address and a particular word line is activated. A column decoder and column MUX then selects a particular memory cell of a row which was activated by row decoder. The output of selected memory cell is then latched with the help of sense amplifier in column circuitry [1].

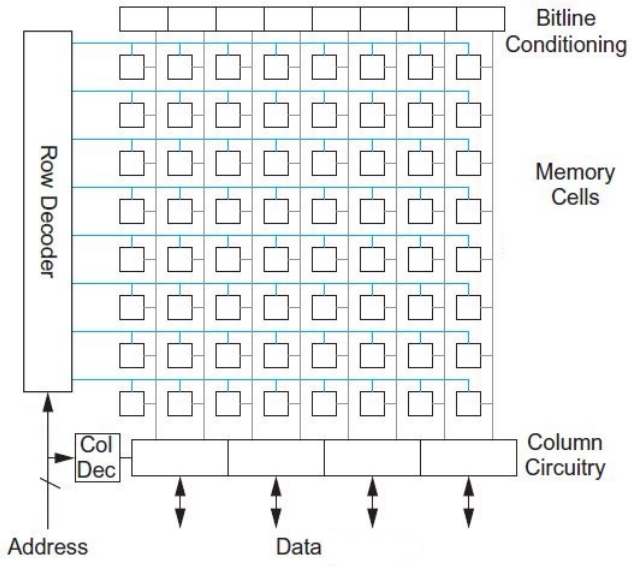


Figure 1.1: SRAM Architecture [1]

The 6T SRAM bit-cell contains two back to back inverters forming a latch so that it can hold a stable state and two pass gate (PG) transistors to read or write into the bit-cell. The positive feed-back ensures the state of a cell such that any disturbance or noise should not affect the data. For writing into bit cell and reading from bit cell, sizing of transistors plays an important role.

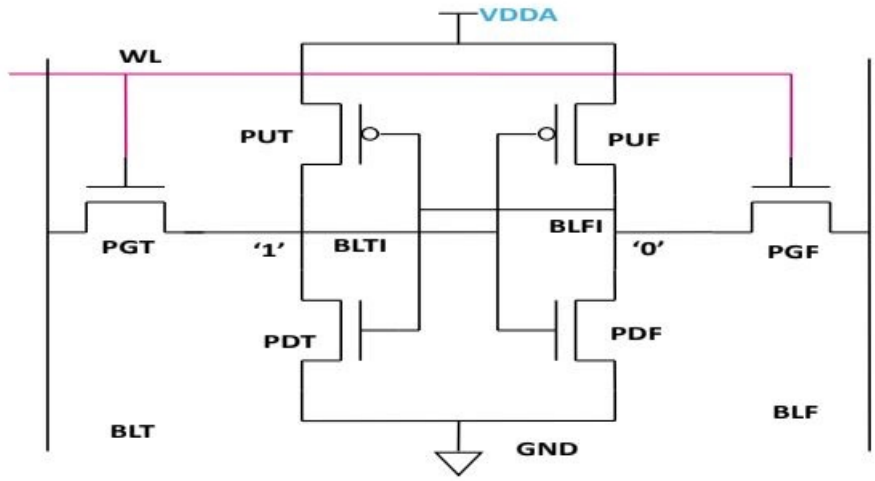


Figure 1.2: 6T SRAM Bit-Cell

Before reading a bit cell both BLT and BLF are pre-charged to supply voltage using a pre-charge circuit. When the word line is high BLT and BLF interact with BLTI and BLFI. Suppose BLTI is at logic 1 and BLFI is at logic 0 then BLF will try to charge BLFI due to its large capacitance. To avoid this, size of PD device is larger than PG. During write operation if we want to write logic 0 and bit-cell stored with logic 1 then BLT will be discharged to ground and BLF will be charged to V_{DD}. BLT should be able to discharge BLTI to ground; this can be ensured if PU is weaker than PG [2]. Basic 6T SRAM bit cell is shown in Figure 1.2.

1.3 Thesis Organization

Thesis is organized as follows. Chapter 2 explains basic of Bias Temperature Instability (NBTI as well as PBTI) and Resistive faults. It also explains the cause and impact of these faults in SRAM architecture and its impact on various Figure of Merits. In chapter

3, we review the basics of ASIL standards. This ASIL is defined as Automotive Safety Integrity Level and is a risk classification method designed by ISO-26262. Here we also highlight about the latent faults that impact the SRAM architecture over the period of time. In chapter 4, we used to explain Row decoder design where we examine the impact of NBTI and resistive faults. We present the results in chapter 5 and detection mechanism in chapter 6. Finally we concluded and presented the future work in chapter 7.

Chapter 2

Basics Of BTI and Resistive Faults

2.1 Introduction Of Bias Temperature Instability

Bias temperature instability is a serious reliability issue since it degrades the performance of p- and n- channel MOSFETs used in CMOS circuits [3]. BTI cause gradual shift in MOS characteristics such as threshold voltage (V_{th}), transconductance (g_m), subthreshold slope (S) and change in linear and drain saturation current (I_{Dlin} and I_{Dsat}), etc., over the period which leads to degradation in the performance of various digital, memory and analog circuits. As a result operational lifetime of CMOS devices and circuits get reduced and if unchecked then it leads to failure of Integrated chips (ICs).

Figure 2.1 shows the biasing condition for p-MOS and n-MOS having HKMG gate insulators. The generation of interface traps near the oxide layer under the negatively applied stress voltage on the gate side ($V_{gs} = -V_{dd}$) at elevated temperature in PMOS transistor is called Negative Bias Temperature Instability. Similarly, the one that occurs under positive gate stress in the NMOS transistor is called Positive Bias Temperature Instability. Due to PBTI negative charge particle get accumulated near to the gate insulator and increases in V_{th}. There are two BTI phase for MOS transistors namely stress phase [4] and relaxation phase [5].

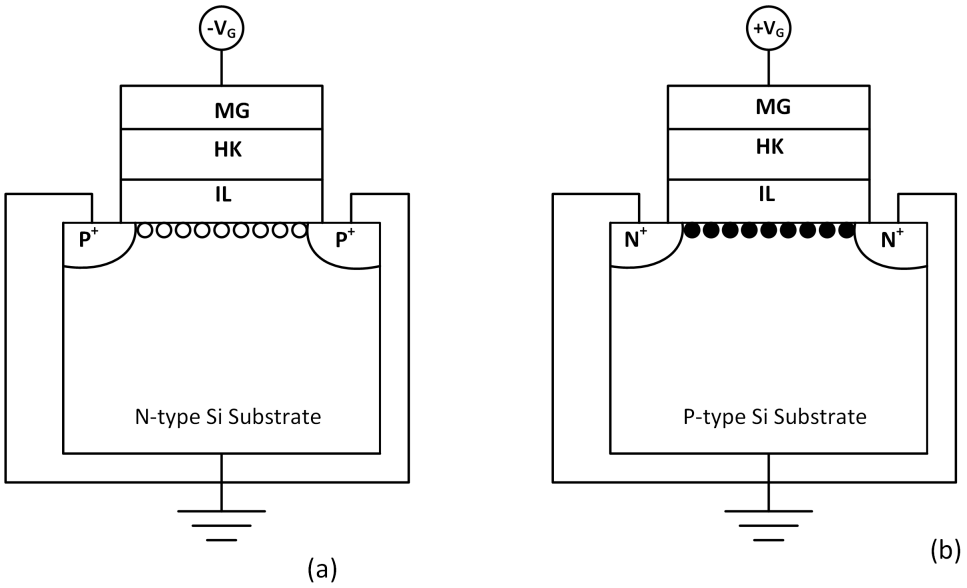


Figure 2.1: Physical Mechanism of p- channel and n- channel MOS showing NBTI and PBTI setup respectively

2.1.1 Stress Phase

During the MOS fabrication process, hydrogen passivation is done just after the oxidation to remove the loosely coupled Si atoms. In stress phase and at elevated temperature, these weak Silicon hydrogen bonds break at Silicon-Oxide interface. This leads to the generation of broken Silicon bonds that remain at the interface and known as interface traps. The released H atoms/molecules slowly diffuse towards the poly gate. The number of interface traps (N_{IT}) generated under stress time (t) is given by 2.1 :

$$N_{IT} = (\frac{N_o.k_f}{k_\tau})^{2/3}. \quad (\frac{k_H}{k_{H_2}})^{1/3}. \quad (6.D_{H_2}.t)^{1/6} \tag{2.1}$$

Above equation represents the Reaction Diffusion (R-D) model that explains the physical mechanism of interface traps generation. As per the R-D model, the rate of generation of interface traps (N_{IT}) initially depends on rate of dissociation of the Si-H bonds,which is controlled by the forward rate constant (k_f) and local self annealing process that is controlled by the rate constant (k_τ).

2.1.2 Relaxation Phase

During this relaxation phase, there is no Silicon Hydrogen bond breaking. However, the H atoms/molecules try to diffuse back towards the interface and anneal with Silicon bonds. The number of interface traps that do not anneal with silicon bonds during this relaxation phase is given by 2.2 :

$$N_{IT}(t_o + t_\tau) = \frac{N_{IT}(t_o)}{1 + \sqrt{\frac{\xi.t_\tau}{t_o + t_\tau}}} \tag{2.2}$$

where N_{IT} $(t_o + t_\tau)$ is the number of interface traps after this relaxation phase. These interface traps cause increase in threshold voltage (V_{th}) that leads to degradation in on current (I_{on}). The equation that relates interface traps and increment in (V_{th}) is given by 2.3 :

$$\Delta V_{th} = \frac{(1 + m).q.N_{IT}}{C_{ox}.\chi.\gamma} \tag{2.3}$$

2.2 Impact Of NBTI aging On SRAM Performance Metrics

SRAM cells have several key performance characteristics, which have adverse effect with NBTI aging [5]. Table 2.1 shows the impact of NBTI aging effects on SRAM performance metrics. According to table SNM is critical reliability metric in an SRAM cell while considering aging effects. The SNM during the read operation is called as Read Noise Margin and in this case SRAM cells become more susceptible to failures.

As the table outlines shows, read and write delay get the minimal effect from NBTI aging, and these small defects are hard to detect. The overall effect of NBTI is most prominent in the SNM and Data Retention Voltage (DRV), which leads to read stability failures and power saving potential respectively.

Performance Metrics	Description	NBTI effects
Read Delay	Latency	Min Degradation
Write Delay	Latency	Modest Improvement
SNM	Smallest voltage causing data flip	Significant Degradation
DRV	Min supply voltage require to retain Data	Significant Degradation
Read Stability	Read Data Failures	Negatively affected
Write Stability	Write Data Failures	Modest Improvement

Table 2.1: NBTI Impact on SRAM performance metrics

2.3 Partial Resistive Defects

There are mainly resistive open defects. These Resistive open defects are defined as unconnected nodes in manufactured CMOS circuits that were initially connected in the design and represented the degradation in conductivity within the CMOS circuit's interconnects. These faults lead to timing failures and reliability risks whose magnitude is not only voltage-sensitive but also influenced by the electrical properties of driving and driven CMOS circuits.

Electromigration is one of the other reason that leads to interconnect open over the period. With the increase in functionality and passive devices, the total interconnect length is exploding as well, which means that there are more wires present on the die that are prone to EM effects. This Electromigration is defined as the gradual displacement of metal ions in a semiconductor. This comes under the condition when the current density is high enough to cause drift of metal ions in the direction of electron flow.

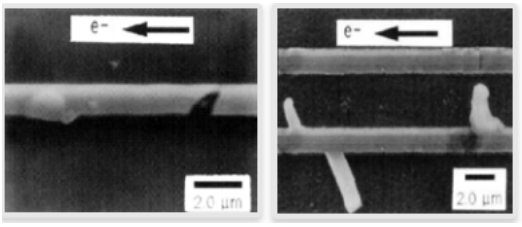


Figure 2.2: Open circuit and short circuit in Interconnects

Figure 2.2 shows that when outgoing flux exceeds the incoming ion flux, results

in open circuits and if incoming ion flux exceeds the outgoing flux then that results in a short circuit.

These partial open-resistive affects differentially on SRAM architecture. It produces various types of faults in SRAM based on the location where it occurs. Here there are some of the faults that generally occur due to this open-resistive defects :

- Stuck at Fault (SAFs) : This fault comes in memory when the logic value of a cell is always 0 or 1. Figure 2.3 shows the state diagram for stuck-at faults.

Figure 2.3: State Diagram For Stuck-AT Faults

- Transition Faults (TFs) : In transition faults a cell fails to make a transition either from 0 to 1 or from 1 to 0. These transition faults mainly occur due to signal delay. Figure

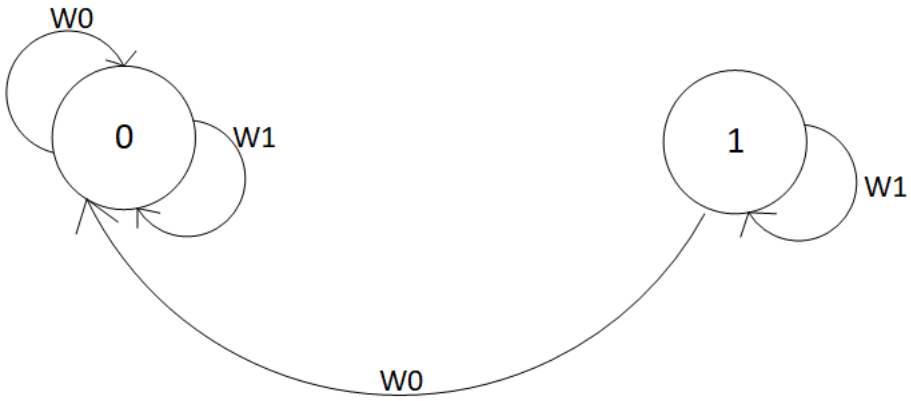


Figure 2.4: State Diagram For Transient Faults

- Write destructive faults (WDFs) : A memory cell is said to have WDFs fault if non

transition operation cause transition in memory cell. For example if memory cell is in state 0, write 0 on it then cell becomes 1. This is denoted as <0w0/1/->

- Read destructive Faults (RDFs): A read operation is performed to the memory cell causes inversion of the value in the memory cell and returns the incorrect value. For example if memory cell is in state 0, read 0 on it and cell becomes 1. It is denoted by <0r0/1/1>

- Incorrect read Faults (IRFs): A memory cell is said to have incorrect read faults if cell returns an incorrect value during read operation while the state of memory is not changed. For example if cell is in state 0 but read operation return value 1 while cell remains in state 0.

- Deceptive read destructive faults (DRDFs): A cell is said to have DRDFs if read operation performed to the cell cause inversion in the cell state. For example if cell is in state 0, read 0 on it but due to read operation cell state becomes 1.

- Address decoder Faults (ADFs) : Faults in row and column decoder comprises address decoder faults in memory. There are certain faults like with certain address multiple wordline get selected or any particular wordline get selected by multiple addresses.

2.4 Summary

In this chapter, we have discussed the Bias temperature instability (BTI) and Partial resistive defects. We have also reviewed the impact of aging as well as resistive faults on SRAM performance metrics. As we observed that NBTI has minimal effects on delay, but in this work, we will show that NBTI, along with open-resistive defects, leads to a significant degradation in SRAM operation. Since they are hard defects that come over the period, so at last, we have also suggested the detection mechanism for these defects.

Chapter 3

ASIL: Automotive Safety Integrity Level

Automotive Safety Integrity Level (ASIL) is a risk classification scheme defined by ISO-26262. It is an adaptation of the Safety Integrity Level used in IEC 61508 for the automotive industry. The ISO-26262 sets the international standards for functional safety related to Automotive car system including Electrical/Electronic system. Functional safety is defined as the absence of unwanted risk due to hazards caused by malfunctioning behavior of electrical or electronic systems. ASIL establish safety requirements—based on the probability and appropriateness of harm—for automotive electronic/electrical components that must be compliant with ISO 26262. There are four ASIL levels- A, B, C, and D. ASIL A represents the lowest degree, and ASIL D presents the highest degree of automotive hazards. So as we move towards higher ASIL level designing electronics equipment that satisfies with ISO-26262 is getting stringent. The reason behind explaining this ASIL standard is to give a clear view regarding systematic as well as random error. This random error mainly consists of latent fault that occurs in any electronic system over the period. ISO 26262 address the requirements, process, and methods to deal with the effects of systematic and random hardware failures. This thesis work consists of Resistive-open along with BTI that affects the embedded SRAM operation over the period, so it comes under latent faults. Figure 3.1 shows the work flow structure based on ASILs standard.

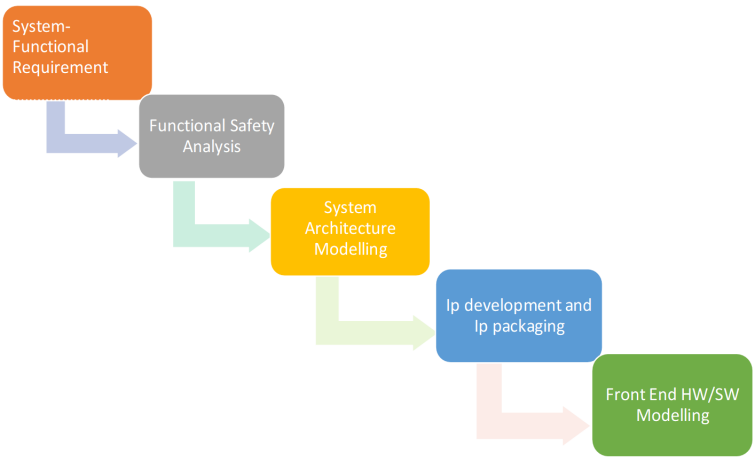


Figure 3.1: ASIL Based WorkFlow

3.1 ASIL Parameter

In this section, we will explore how does ASILs work. Automotive Safety Integrity Level standards are characterized by performing hazard analysis and risk assessment. For every electronic equipment used in automotive vehicle, engineers should measure three specific variables :

- Severity : It defines the seriousness of damage to the people's life.
- Exposure : It is the measure of how often vehicle is exposed to the hazardous situation.
- Controllability : This determines the extent to which driver of the vehicle can control, if safety goal is breached in case of failure.

Each of these variables is further classified into sub-classes. Severity has four classes starting from "no injuries" (S0) to "survival uncertain" (S3). Exposure has five classes covering the "incredibly unlikely" (E0) to the "highly probable" (E4). Controllability has four classes ranging from "Generally controllable" (C0) to "uncontrollable" (C3).

3.2 Fault Classification According to ASIL- ISO 26262

In this section we will explore about the Hardware faults that are defined under ASIL standard document while designing Electrical/Electronics component. These faults are listed below :

- Single Point Fault : The fault that directly leads to the violation of safety goals.
- Residual Fault : Portion of fault that are not covered under safety mechanism portion of a fault, that by itself leads to the violation of a safety goal.
- Multiple Point Fault : Combination of multiple independent faults that leads to the violation of safety mechanism.
- Latent Fault : Faults that are initially act as silent fault and not detected by safety mechanism but becomes hazardous over the time. In this Thesis work we mainly consider this fault like open-resistive defects along with BTI cause latent fault over the period of time.
- Soft Error : Error/faults whose occurrence will not significantly affect the violation of a safety goal. For example bit flips due to transition fault caused by alpha particles from the radiation induced events.

3.2.1 Requirements For ASILs Level

Depending on the knowledge of the failure modes of the hardware elements and their consequences at a higher level, we need to define every aspect to satisfy particular ASIL level. For example, the brake system in an automobile must comply with ASIL D level of safety goal.

Table 3.1 shows the target value for single-point fault metric (SPFM) and latent fault metric (LFM) required by different ASILs Level. This quantitative target value analysis shall consider:

- the architecture of hardware element.

- estimate failure rate for different failure modes of hardware element (electronic system) that would cause either single point fault or latent fault.
- the diagnostic coverage of safety-related electronic elements by safety mechanisms.

Fault Metric	ASIL A	ASIL B	ASIL C	ASIL D
SPFM	Nominal	$\geq 90\%$	$\geq 97\%$	$\geq 99\%$
LFM	Nominal	$\geq 60\%$	$\geq 80\%$	$\geq 90\%$

Table 3.1: Quantitative Target Value For Different Fault Metric

3.3 Diagnostic Coverage For Memory Fault

In this section, we will discuss how can we increase the diagnostic coverage for memory under ASIL standards by analyzing different failure modes.

- Including Stuck-at fault (fault having continuous "0", "1" or "on" at the pin element) model detection scheme for data,address and control interface lines leads to the diagnostic coverage of 60%.
- Along with Stuck-at fault model if we include d.c. (direct current) fault model for data, address and control interface lines then it leads to diagnostic coverage of 90%. This d.c. fault model covers stuck-at fault, open fault, and fault related to high impedance outputs as well as short circuits between lines.
- Along with these two faults if we cover soft error fault then our diagnostic coverage increases upto 99%. This soft error model includes bit flips due to transition fault caused by alpha particles from radiation induced events.

3.4 Safety Mechanism

In this section, we will learn about some of the safety mechanism that are suggested under ASIL standards to qualify particular ASILs level of safety.

- RAM pattern test : Here a bit pattern followed by complement of that bit pattern is written into the cells of memory. This test is effective at detecting stuck-at failure and transition failures but cannot detect most soft errors, addressing faults and linked cell faults.

- Parity bit : A pattern of 0s and 1s is written into cells of memory in specified pattern and verified in that specific order. This safety mechanism is generally used to detect single corrupted bit failures in a word.

- Memory monitoring : Every word of memory is extended by several redundant bits to obtain modified Hamming code with Hamming distance of at least 4. Every time a word is read, checking of redundant bits determine whether or not a data corruption has taken place. If some difference is found then failure message is signaled. This safety mechanism is used to detect each single bit failure, each two bit failure and some multi bit failure.

- Memory signature : Here content of memory is compressed into one or more bytes using cycle redundancy check (CRC) algorithm then continuous polynomial division is carried out using polynomial generator, the remainder represent the signature of memory and is stored and compared at later stage. A failure message is generated if there is a difference. This safety mechanism is mainly used to detect one-bit failures and multi-bit failures.

3.5 Summary

In this chapter, we have discussed the Automotive Safety Integrity Level that describes the risk classification for different electronics element. Here we deal with the fault that comes under static random access memory (SRAM) block. In this thesis work, we are dealing with the latent fault that comprises open-resistive defect along with NBTI. We also describe in a later chapter about the detection mechanism to detect these latent faults which help to satisfy higher safety of ASIL level.

Chapter 4

Impact Of Partial Resistive Defects and BTI on SRAM Address Decoder

In this last chapter, we discussed the impact of an open-resistive defect as well as bias temperature instability on the SRAM address decoder. Firstly we will explain the row decoder design then we analyze the effect of open errors and bias temperature instability on address decoder individually and finally at the end of the chapter we will explain the simultaneous impact of both on address decoder.

4.1 Address Decoding

Address Decoder is an important digital block in SRAM which takes up to 50% of the total chip access time and notable amount of the total SRAM power in normal read/write cycle. To design address decoder need to consider two objectives, first selecting the good circuit technique and second sizing of transistors in circuit. Row decoders are required to select one row of wordlines out of a set of rows in the array as per the address bits. A fast decoding scheme can be implemented using AND/NAND gates or OR/NOR gates. There are mainly two different type of decoding schemes i.e. static and dynamic decoding.

The choice of different decoding schemes depends on the SRAM area, power

consumption and performance considerations. The static NAND-type structure is chosen because of its low complexity and low power consumption. While dynamic decoding style is highly complex and need more precision but having high speed and better power improvement than static ones. Figure 4.1 is static 2:4 decoder. Figure 4.2 is dynamic 2:4 NAND decoder.

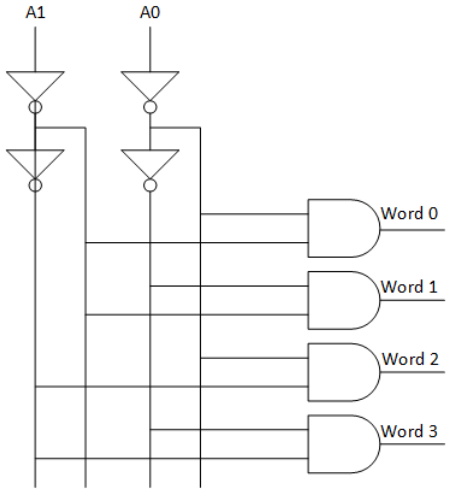


Figure 4.1: Static Decoder

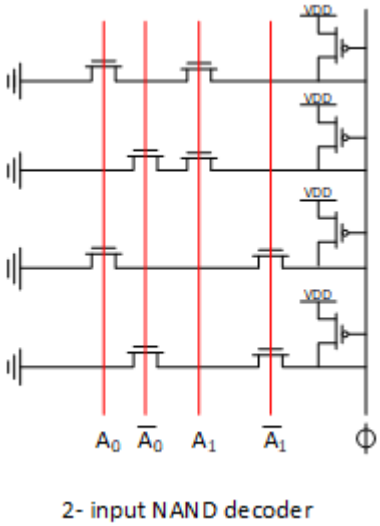


Figure 4.2: Dynamic 2:4 NAND Decoder

For vast SRAM array where we have four address lines requires 4 input NAND gates. As the number of address line increases, the input size of the NAND gate also increases. Then NAND gate with more than three or four input has a significant pull-down delay because of the stacking of more number of NMOS transistors in the pull-down

circuitry. Even also as we move down to lower technology mode, there is a reduction in operational voltage supply that also leads constraint in using high inputs gates. Hence we cannot use more than three input gates since it takes more time to activate the word line, which increases the memory read and write access time. So we can solve this problem by using some pre-decoding and some post decoding. Figure 4.3 present NOR-NAND based pre and post decoding address inputs.

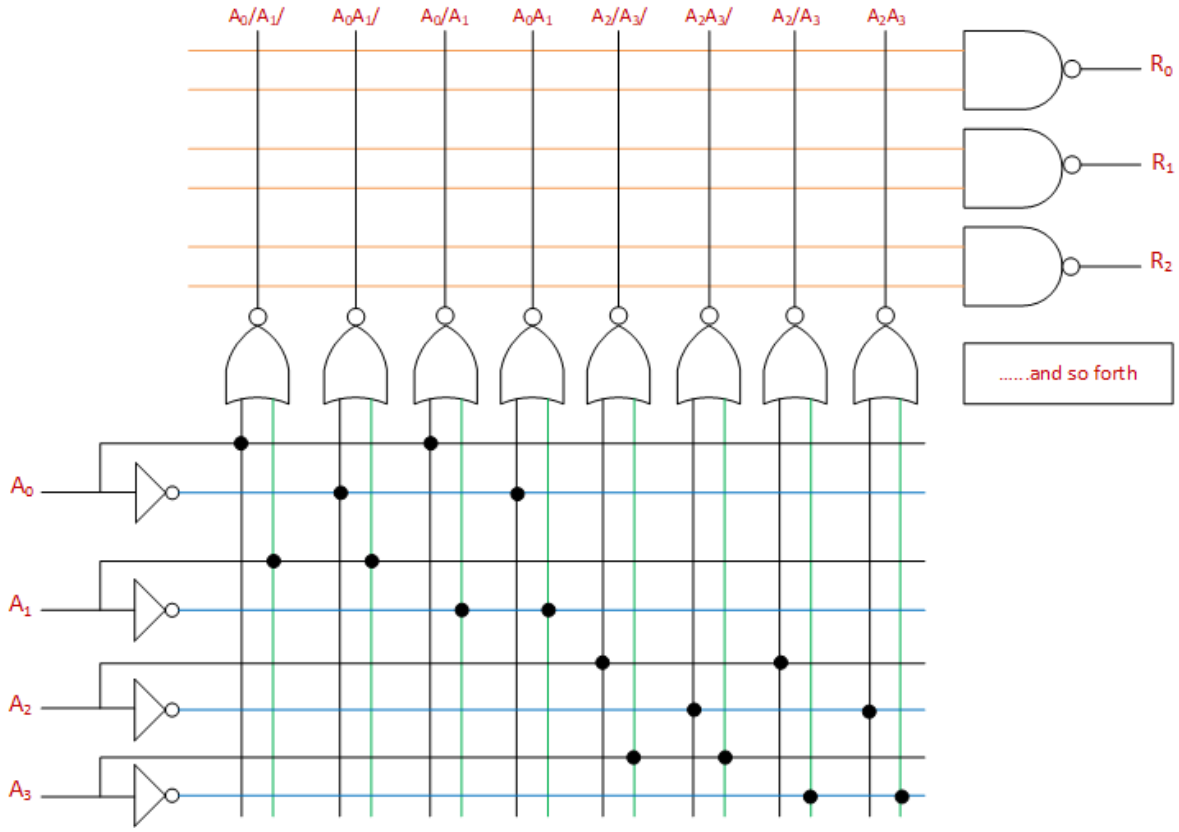


Figure 4.3: Pre-Decoding Address Inputs

There are some other split type decoder structure that can also be applied to implement large decoder structures. One possible scheme is to divide the structure into local and global address lines i.e. divide word line structure.

4.1.1 Divide word line architecture

When the decoder structure becomes large, at least two-stage structures are used to implement an address decoder. Divided word line decoder structure divide the single static address random memory into small blocks. To read or write a block, the local word line is switched on when both the global word line and block select are activated together by address line.

Since at a time only one block is selected and being activated, hence reducing word line delay and power consumption of SRAM. In figure 4.4 block diagram of DWL structure where decoder are divided into two types, first MSB of address is decoded into global word line and rest are as local word line.

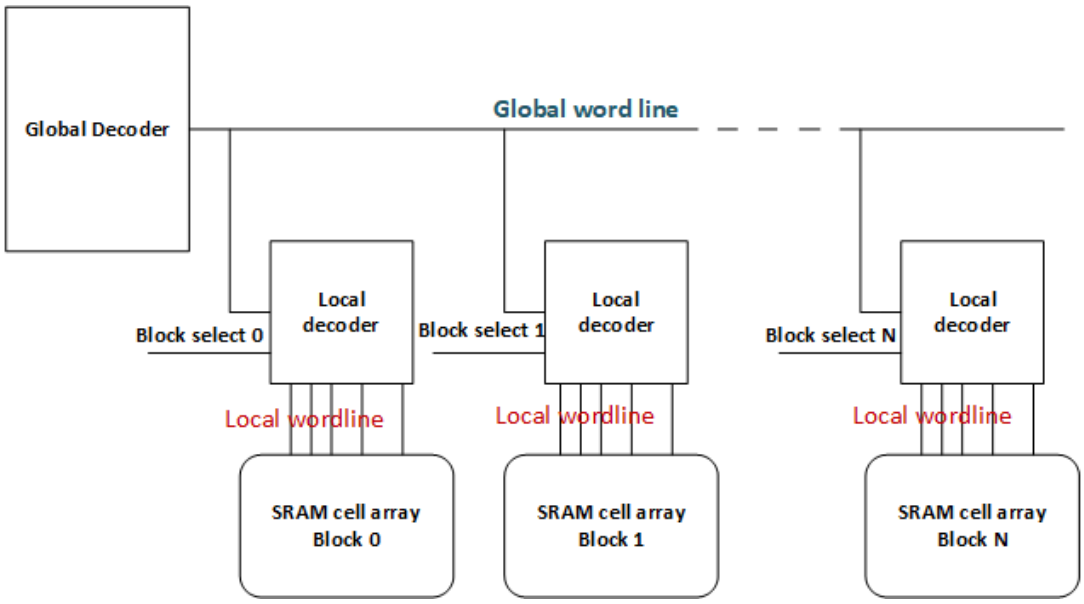


Figure 4.4: Block diagram of DWL structure

In this work we implemented 2:4 static decoder and analyze the impact of open resistive defect on both PMOS and NMOS side. We also analyze the NBTI impact on PMOS transistors, since this work is done on 55nm technology node at which NBTI is having more concern with respect to PBTI.

4.2 Impact Of Partial Resistive Defects On Address Decoder

In this work out of the whole memory structure, we focus our attention on address decoders for resistive open defect analysis. When defect appears between gates i.e. inter gate defects can be detected by standard March tests. In case when defect is located between source and ground for NMOS or source and supply for PMOS, it is called dynamic fault due to its sequential behavior. As an example shown in figure 4.5 we have inserted an resistive open defect at PMOS side as well as NMOS side. The resistive defects in decoder of figure 4.5 can be classified as followings.

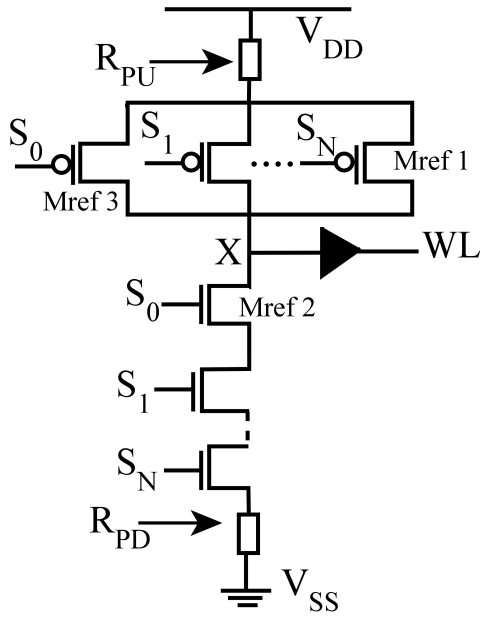


Figure 4.5: Address selection circuit

- Inside pull-up network : R_{pu} is an example of a defect in the pull-up network of the decoders shown in figure 4.5 which is inserted between the supply and parallel PMOS transistors. This defect has symmetric impact on every input address line.
- Inside pull-down network : R_{pd} is an example of defect in pull-down network of the decoders. There are many ways of resistive defect locations in the pull-down network of the decoder but defect between final NMOS transistor and ground has major impact so we consider this.

The presence of Resistive open fault in the address decoder leads to delay in selection or deselection of the word line (WL) [6]. Here Firstly the Resistance Rpu and Rpd affects the current that charge or discharge the node X. Secondly, the voltage drop across these resistive defect would be high enough to prevent the transition at node X. The resistive defect in the pull-up network of the decoder affects the rising transition at node X, consequently the deactivation of the word line. Similarly the resistive defect in the pull-down network of the decoder affects the falling transition at node X, that results in the delay of activation of word line. In case of resistive defects between any particular PMOS to node X, leads to delay the transition of that signal (1->0).

4.2.1 Simulation Results

The impact of resistive open defects in pull up and pull down network of cmos decoder affects the timing of the wordline.

Inside Pull-up Network

The resistive defect at pull-up network of the decoder shown in figure 4.5 affects the rising transition at the node X consequently deactivation of wordline.

Figure 4.6 shows the wordline transition for various resistive defects; R_{pu} between 0kΩ to 100kΩ at worst temperature of 125 ℃across different corners. This analysis shows that FS would be the worst case for defect at pull up side. For worst corner FS at 100kΩ we observe that there is incremental change of nearly 48% in wordline width. These higher resistance are easy to catch during manufacturing test but small resistance which cause small delays are hard to detect and may skip the tests and cause reliability issues.

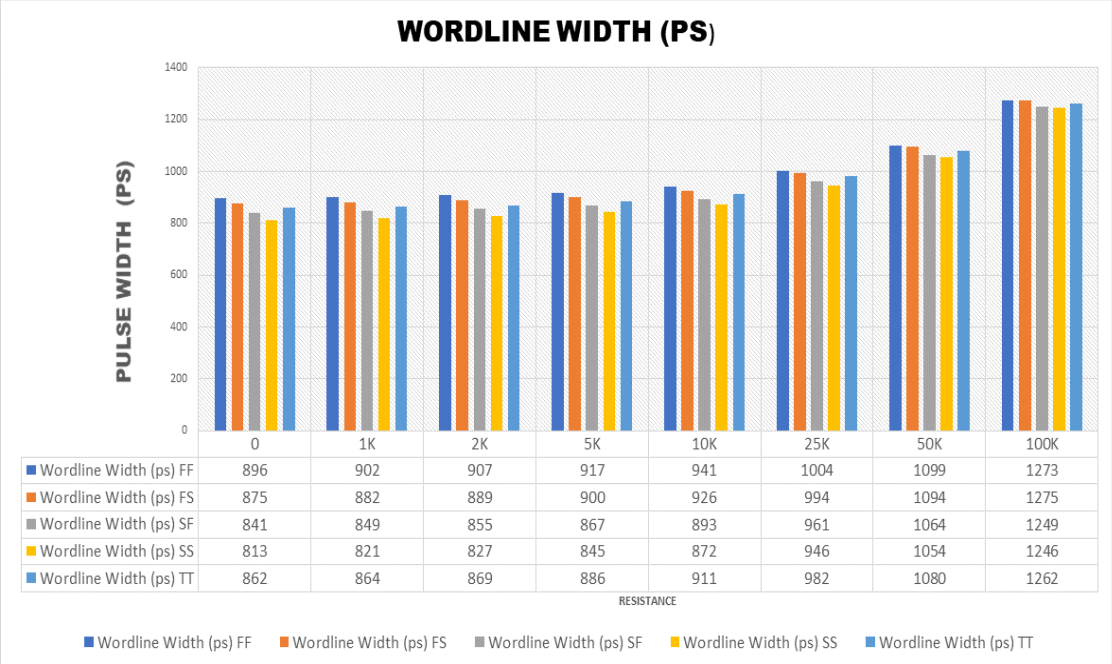


Figure 4.6: Impact of Resistance in Pull-up Network at worst temperature across different corners at different resistance value

Inside Pull-down Network

The resistive defect at pull-down network of the decoder shown in figure 4.5 affects the falling transition at the node X consequently activation of wordline.

Figure 4.7 shows the wordline transition for various resistive defects; R_{pd} between 0kΩ to 100kΩ at worst temperature of 125 ℃across different corners. This analysis shows that SS would be the worst case for defect at pull down side. For worst corner SS at 100kΩ we observe that there is decrease in word line pulse width of nearly 43% and if the resistance value is 200kΩ then we observe that there is transition failure at node X, since pull down network is not strong enough to drive node X to zero. This cause failure for wordline driver to activate the wordline.

Figure 4.8 shows the impact of low resistance on wordline activation and deactivation. Here we can clearly observe that resistance has more impact on pull-up network comparing to pull-down network. The figure depicts the percentage of delay increment

from 0 to 5KΩ.

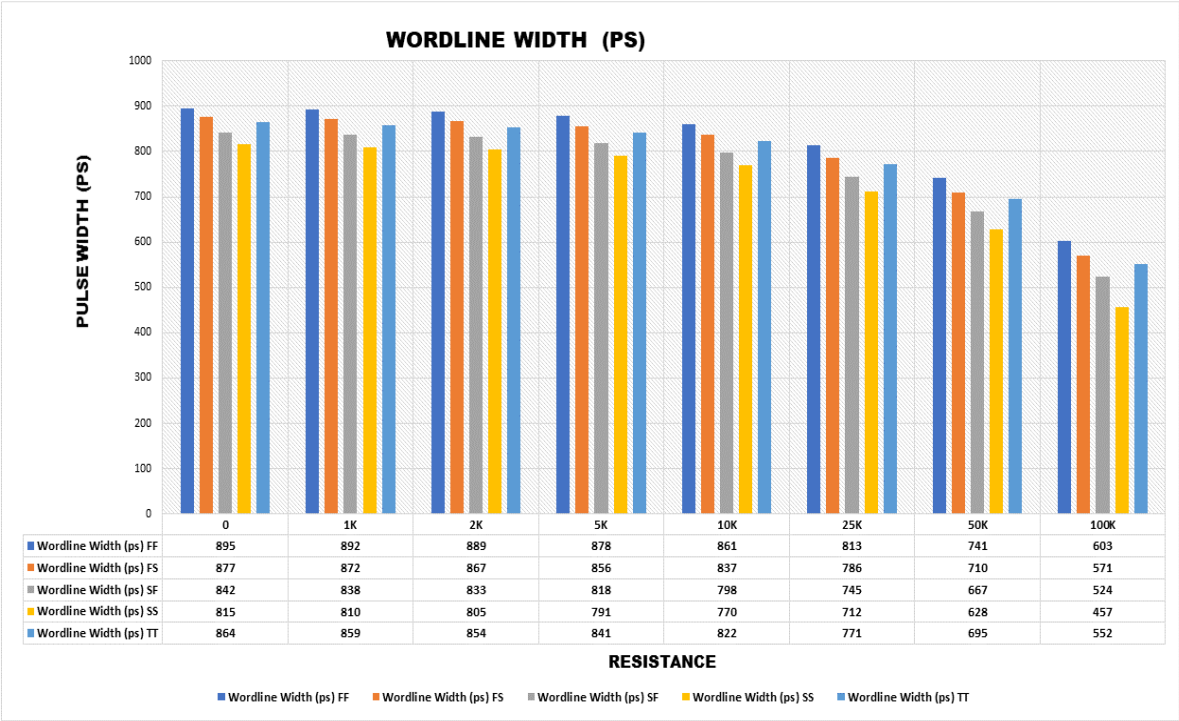


Figure 4.7: Impact of Resistance in Pull-down Network at worst temperature across different corners at different resistance value

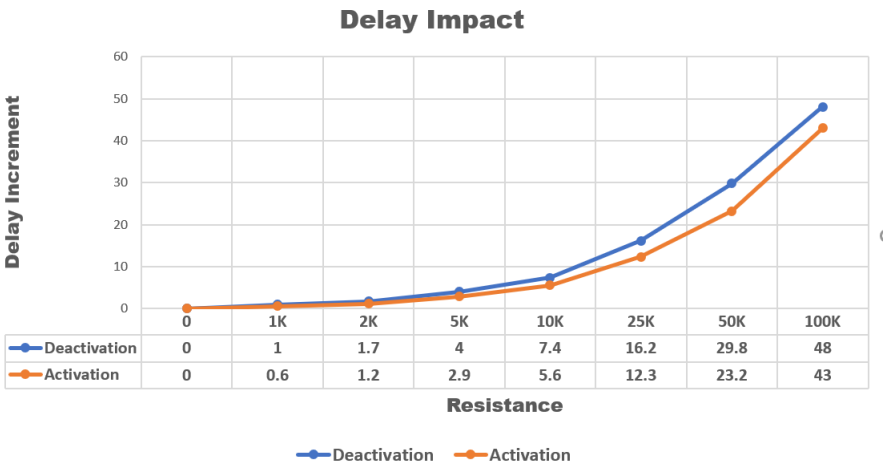


Figure 4.8: Impact of Variable Resistance in Pull-up and Pull-down Network

Since these resistance in either pull-down or pull-up network leads to change in activation or deactivation of wordline, consequently it also impact the readability and

writability. Table 4.1 shows that upto certain level of pull-down resistive defects in Decoder section leads to delay in SRAM Read/Write Operation because it leads to delay in activation of wordline. After huge resistive defects it fails in its logic operation.

Resistance	Read time		Write time	
	value (ps)	corner	value (ps)	corner
0	552	SS 125 c	472	SS 125 c
1K	563	SS 125 c	476	SS 125 c
2K	568	SS 125 c	481	SS 125 c
5K	600	SS 125 c	496	SS 125 c
10K	656	SS 125 c	526	SS 125 c
20K	IRF	SF -40 c		
50K			UWD	SF -40 c

Table 4.1: Read and Write Time Analysis Across Different Resistance at Pull-down side

- IRF : Incorrect read fault, In this case due to resistive defect at NMOS WL enables after SEN signal which leads to data read based on the leakage. If sense amplifier has low sensing capability it can easily provide incorrect data read based on leakage.
- UWD : Unable to write data because due to reduction in pulse width of Wordline, Data can't be able to store value at internal nodes.

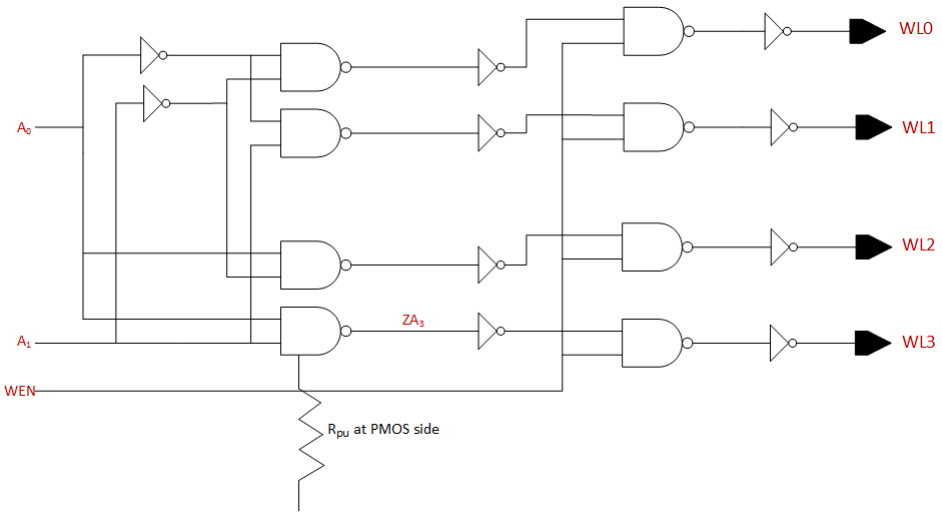


Figure 4.9: NAND Based Address Decoder With Pull-up Resistive Defect

Figure 4.9 shows the example of static address decoder where we use to insert resistance at pre-decoding stage. Due to the presence of pull up resistive-defects, the

incorrect dual WL selection persists [7] for a portion of the sensing phase of operation because this pull up operation leads to increase in wordline deactivation time. From figure 4.10 we can observe that address transition occur exactly at Ts before WEN activation. In this case WL3 is erroneously selected for a certain time which means at a time two WL get selected i.e. WL3 and WL2. This type of defect can be detected through MARCH test.

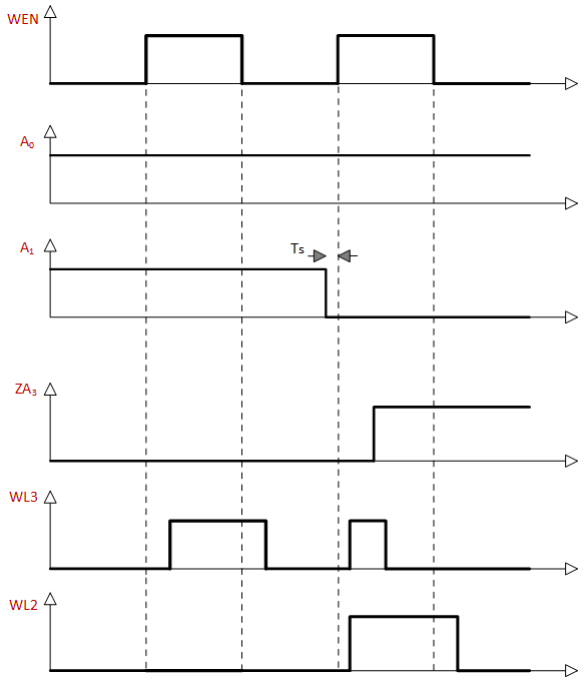


Figure 4.10: NAND Based Address Pre-Decoder waveform With Pull-up Resistive Defect

4.3 Impact Of NBTI On Address Decoder

The ΔVth in MOS transistors due to BTI affect the wordline activation and de-activation delays. Both NBTI and PBTI impact the delays uniquely, i.e., NBTI in PMOS transistors affect the de-activation delay while PBTI in the NMOS transistors affect the activation delay. In addition, different decoding schemes stress the transistors differently, resulting in different delays. Here, we assume linear-up addressing schemes for 2×4 decoder. In our work we depicted the impact of NBTI at the PMOS of NAND decoder, which leads to delay in deactivation of wordline.

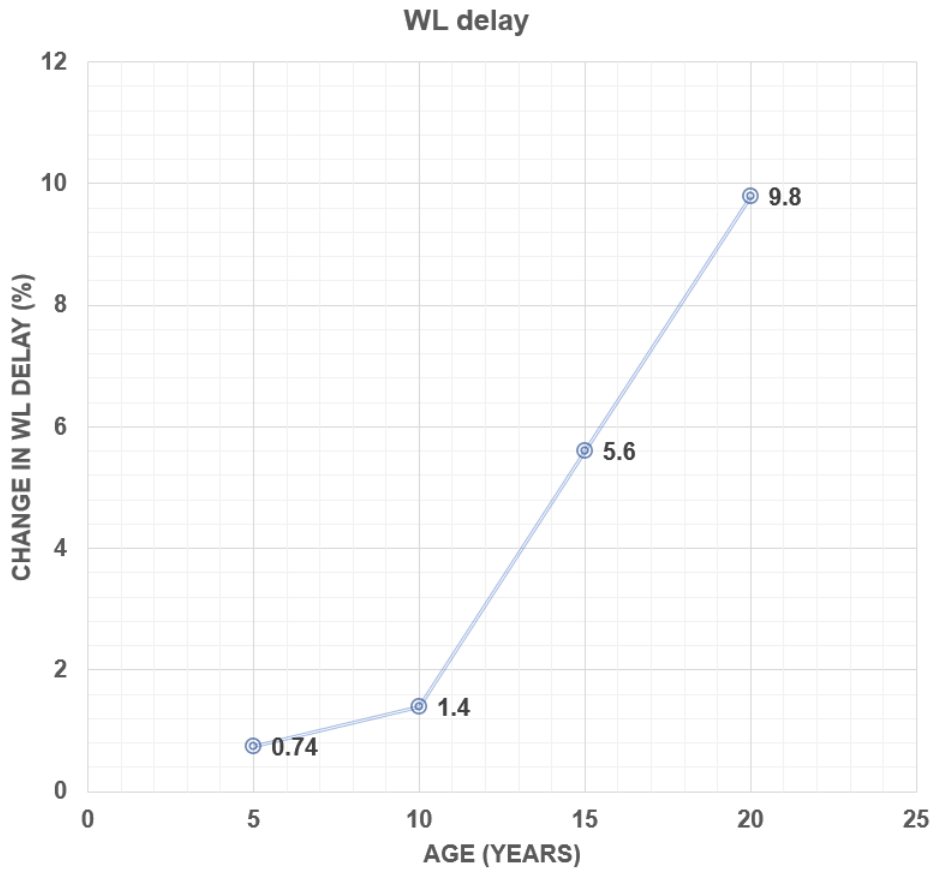


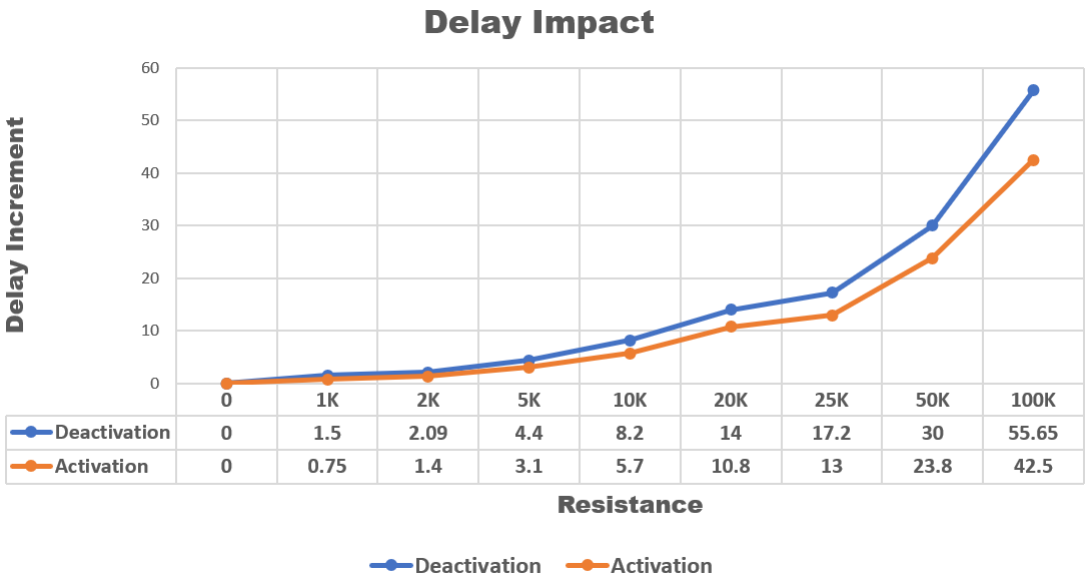
Figure 4.11: NBTI Impact On Address Decoder

Figure 4.11 shows that performing aging analysis for 10 years leads to the change in delay of wordline deactivation by 1.4 %. This change will increase as we go towards high input gates, like 5-input or higher input NAND decoder due to increase in number of transistors.

4.4 Impact Of BTI and Resistive Defects On SRAM

In this experiment we analyze the combined impact of BTI as well as resistive defect on pull-up and pull-down side of address decoders [5]. Figure 4.12 shows the effect of BTI as well as Resistive defects on activation and deactivation of address decoders. Here we can clearly observe that NBTI along with resistive defect cause delay in wordline deactivation

by more than 50 %. In this experiment BTI impact has been observed for aging of 10 years. In next chapter we will present the detection mechanism which will capture the resistive defect equal or greater than 5KΩ.



	0	1K	2K	5K	10K	20K	25K	50K	100K
Deactivation	0	1.5	2.09	4.4	8.2	14	17.2	30	55.65
Activation	0	0.75	1.4	3.1	5.7	10.8	13	23.8	42.5

Figure 4.12: Combined Impact Of BTI and Resistive Defects On Address Decoder

4.5 Summary

In this chapter, we have discussed the impact of partial resistive defect on pull-up and pull-down side of address decoders. We also analyze the impact of NBTI on PMOS transistors. Finally we presented the combined impact of both Bias temperature instability and partial resistance on address decoders. The overall analysis presented in this chapter for BIT and resistive defects clearly shows that the life time degradation in the presence of small open defects in the memory decoders accelerate the failures. Therefore it is extremely important to develop the test techniques that will capture these small defects at design stage.

Chapter 5

Detection Mechanism

In this chapter,detection mechanisms are discussed. Higher resistive defect can be detected using various types of MARCH TESTs, here we mainly concern about small resistive defect which cause small delay in wordline and that are considered as hard fault. We will discuss about the test mode, whenevere this test mode get activated it will test the wordline for its resistive defects. Test Mode schematics are designed in Cadence Virtuoso and simulated using Spectre simulators in 55nm low power process. Characterization has been done for all corners which are FNFP, FNSP, SNFP, SNSP, and TT. Temperature range has been taken from -40 to 130 C.

5.1 TEST MODE SCHEMATIC

Figure 5.1 shows the test mode architecture for detecting the wordline defect due small resistance. From the figure we can observe that when T = 1, test mode become activated this leads to $\bar{A}$ and $\bar{B}$ becomes 1. So for test mode case every wordline get activated and compare to its adjacent using EXOR gate. Here we consider 2:4 address decoder. This test mode performes in following ways:-

- In case of Error between WL0 and WL1: First compare WL0 and WL1 using exor gate . If we get EXOR_0 output as high, then must be error in between WL0

or WL1.Again if EXOR_1 output of comparison between WL1 and WL2 also gets high, it means that there is an error on wordline WL1 and if output is 0, then it means error is in WL0.

- Similarly in figure5.1 if EXOR_1 is high and other exor output is low then it means WL2 is defective.
- At last if all the exor output is 0 except EXOR_2, then error is in WL3.

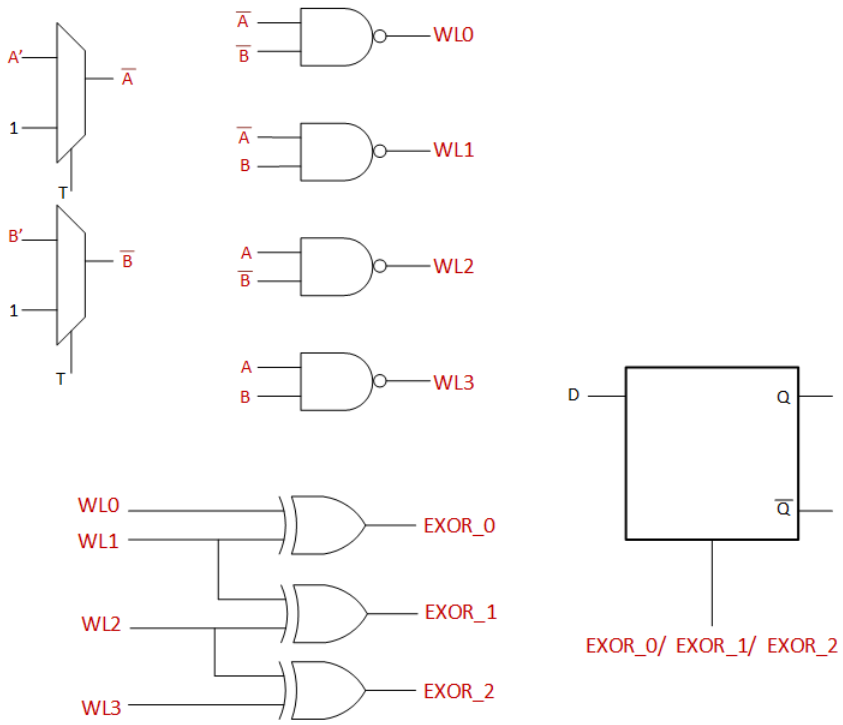


Figure 5.1: Test Mode Architecture

Figure5.1 shows that we use exor output as clock to D-flip flop. Whenever this D flip flop get activated, it propagates 1 which is initially stored their. This D flip flop is positive edge triggered, it depends on the positive edge of exor output. This will help us to detect small resistance defects.

5.2 Simulation Results For Detection Mechanism

Figure 5.2 shows the analysis of Test mode mechanism at voltage of 1.2V and temperature -40℃. Here we can clearly observe that worst case would be FNFP because from figure 4.6, we observe that for Fast case there is wordline delay of 42 % whereas for slow corners there is a deviation of 53 % in wordline due resistance of 100KΩ. It means that would be critical case to detect. Figure 5.4 shows the analysis at 130℃and results in worst case at 5kΩ at FNFP.

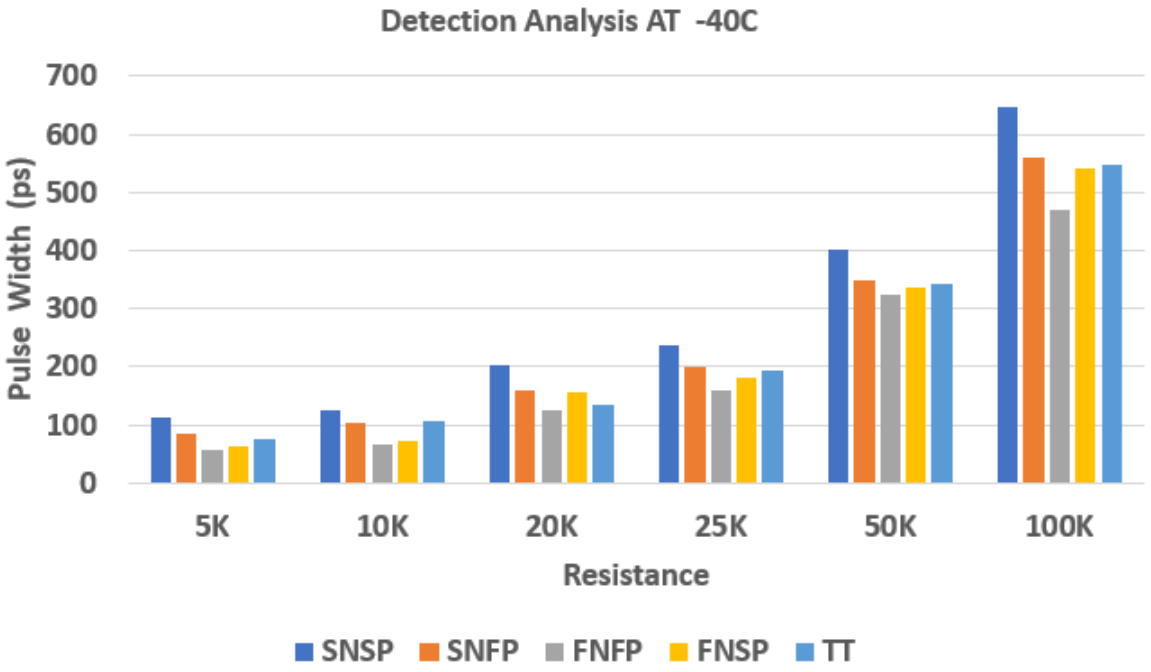


Figure 5.2: Detection Analysis At -40℃

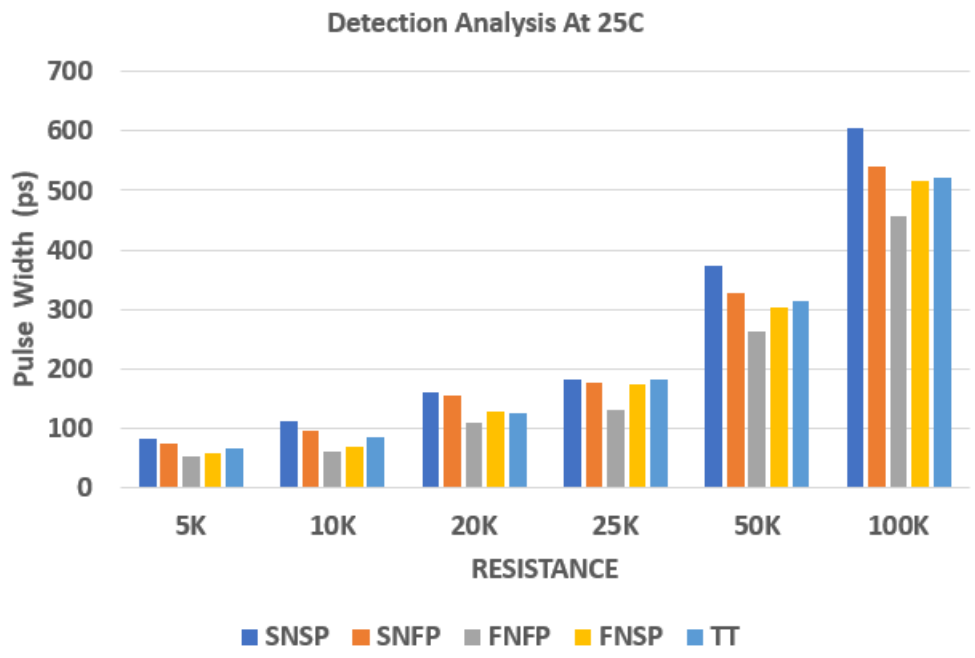


Figure 5.3: Detection Analysis At 25℃

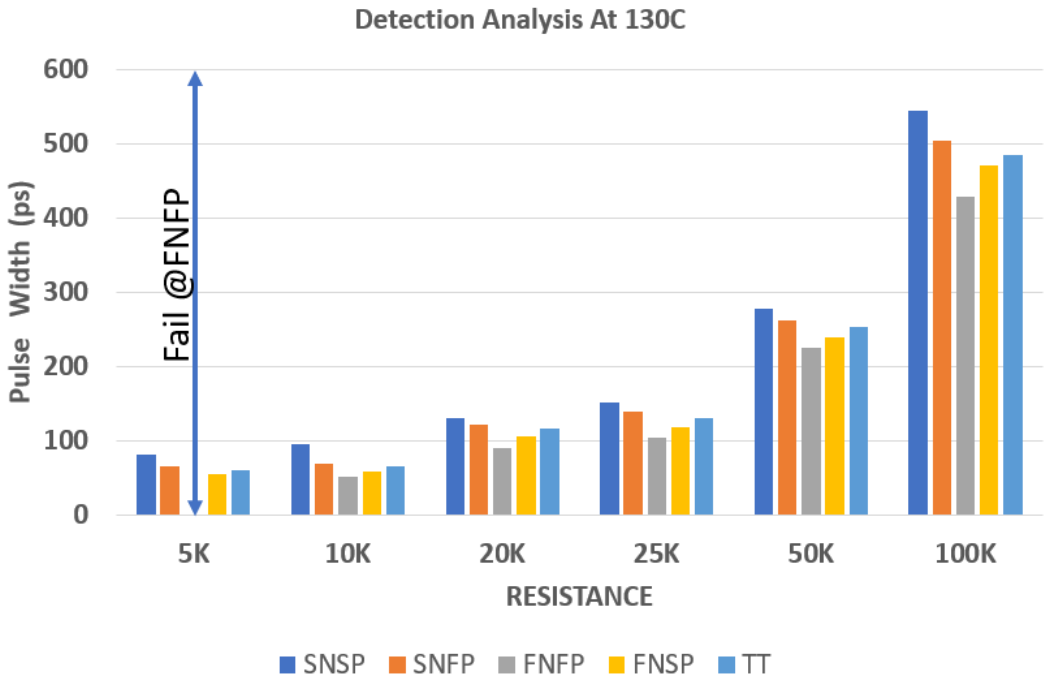


Figure 5.4: Detection Analysis At 130℃

Chapter 6

Conclusion and Future Work

In this dissertation, our main concern is towards the impact of these partial resistive as well as bias temperature instability on SRAM address decoders. Here we have analyzed the defect impact across all the corners as well as for varying resistance from 0 to 5KΩ. Due to these defects there is delay in wordline activation and deactivation. At SNSP worst case we get 0.6 % to 0.88% delay at activation side of wordline for every 1KΩ of resistance at pull down side of NAND decoders. Similarly in case of pull up side resistance we observe 0.98 % to 1.25 % of delay in deactivation of wordline for every 1KΩ of resistance.

In this work we also analyze the impact of aging along with resistive defects. For combined defects we get 1.35 % to 1.65 % of delay in deactivation of wordline whereas 0.74 % to 1.05 % of delay in activation of wordline. So we get to conclusion that this resistance along with BTI have more impact on PMOS side compare to NMOS side.

For Future work we can do analysis for all peripherals portion of SRAM memory architecture like for pre-charging side also and we should develop test mode that will able to detect these defects.

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